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Kind regards,

Team Nexperia

DATA SHEET

CBT16211

24-bit bus switch with 12-bit output enables

Product data

2001 Jun 13

PHILIPS

PHILIPS

24-bit bus switch with 12-bit output enables

CBT16211

FEATURES

- 5 Ω switch connection between two ports

- TTL compatible control input levels

- Package options include plastic shrink small outline (SSOP), thin shrink small outline (TSSOP)

- ESD protection exceeds 1000 V CDM per JESD22-C101

- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA

DESCRIPTION

The CBT16211 provides 24 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as a dual 12-bit bus switch with separate output-enable ($\overline{OE}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When $\overline{OE}$ is low, the associated 12-bit bus switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and a high-impedance state exists between the ports.

The CBT16211 is characterized for operation from –40 to 85 °C.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50 pF; V_{CC} = 5 V	0.25	ns
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	4.3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0 V or V_{CC}	6.9	pF
I_{CC}	Total supply current	Outputs disabled; V_{CC} = 5.5 V	3.0	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
56-Pin Plastic SSOP Type III	–40 to 85 °C	CBT16211DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40 to 85 °C	CBT16211DGG	SOT364-1

FUNCTION TABLE

INPUTS		OUTPUTS	
1$\overline{OE}$	2$\overline{OE}$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

LOGIC SYMBOL

SA00510
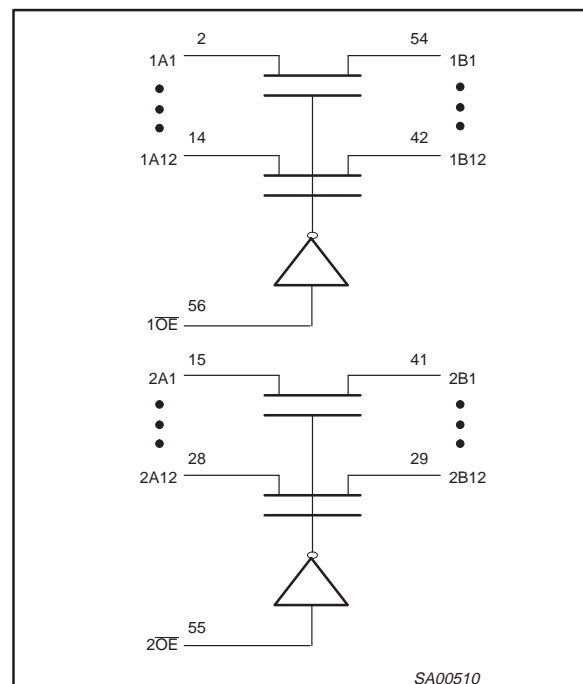
24-bit bus switch with 12-bit output enables

CBT16211

PIN CONFIGURATION

SA00509
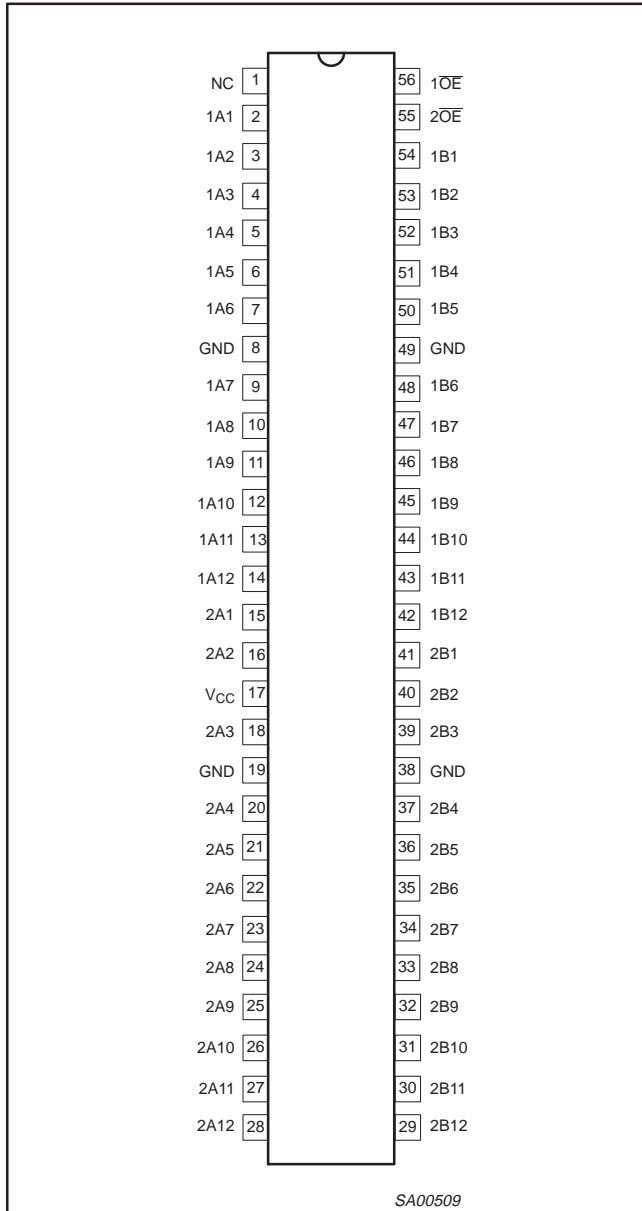
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	NC	No internal connection
56, 55	1$\overline{OE}$, 2$\overline{OE}$	Output Enables
2, 3, 4, 5, 6, 7, 9, 10, 11, 12, 13, 14	1A1-1A12	Inputs
54, 53, 52, 51, 50, 48, 47, 46, 45, 44, 43, 42	1B1-1B12	Outputs
15, 16, 18, 20, 21, 22, 23, 24, 25, 26, 27, 28	2A1-2A12	Inputs
41, 40, 39, 37, 36, 35, 34, 33, 32, 31, 30, 29	2B1-2B12	Outputs
8, 19, 38, 49	GND	Ground (0 V)
17	V$_{CC}$	Positive supply voltage

24-bit bus switch with 12-bit output enables

CBT16211

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage[3]		−0.5 to +7.0	V
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2.0	—	V
V_{IL}	Low-level Input voltage	—	0.8	V
T_{amb}	Operating free-air temperature range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_{amb} = −40 to +85 °C			UNIT
			Min	Typ[1]	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V; I_I = −18 mA	—	—	−1.2	V
V_P	Output high pass voltage	V_{IN} = V_{CC} = 5.0 V; I_{OUT} = −100 μA	3.4	3.6	3.9	V
I_I	Input leakage current	V_{CC} = 0 V; V_I = 5.5 V	—	—	10	μA
		V_{CC} = 5.5 V; V_I = GND or 5.5 V	—	—	±1	
I_{CC}	Quiescent supply current	V_{CC} = 5.5 V; I_O = 0, V_I = V_{CC} or GND	—	—	3	μA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5 V, one input at 3.4 V, other inputs at V_{CC} or GND	—	—	2.5	mA
C_I	Control pins	V_I= 3 V or 0	—	4.5	—	pF
$C_{I(OFF)}$	Port OFF capacitance	V_O = 3 V or 0, $\overline{OE}$ = V_{CC}	—	6.9	—	pF
r_{on}[3]		V_{CC} = 4.0 V; V_1 = 2.4 V; I_I = 15 mA	—	14	20	Ω
		V_{CC} = 4.5 V; V_1 = 0 V; I_I = 64 mA	—	5	7	
		V_{CC} = 4.5 V; V_1 = 0 V; I_I = 30 mA	—	5	7	
		V_{CC} = 4.5 V; V_1 = 2.4 V; I_I = −15 mA	—	8	12	

NOTES:
1. All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch.
   On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

AC CHARACTERISTICS

GND = 0 V; t_R; C_L = 50 pF

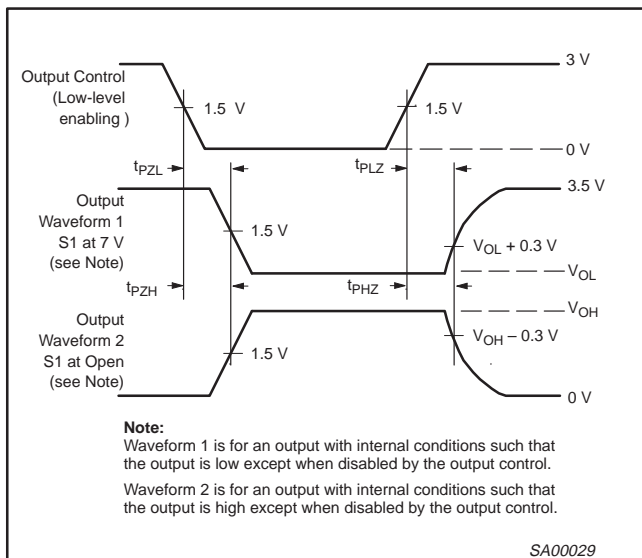| SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5.0 V ±0.5 V		UNIT
				Min	Max	
t_{pd}	Propagation delay[1]	A or B	B or A	—	0.25	ns
t_{en}	Output enable time to High and Low level	$\overline{OE}$	A or B	1.5	6.0	ns
t_{dis}	Output disable time from High and Low level	$\overline{OE}$	A or B	1.5	6.0	ns

NOTE:

1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).
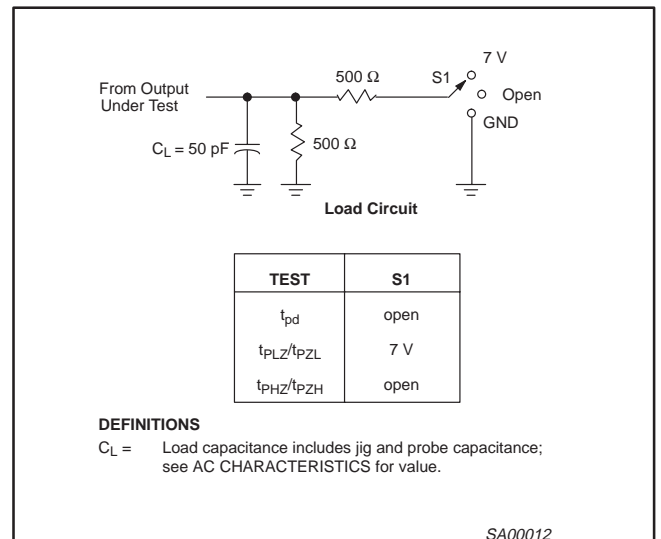
AC WAVEFORMS

V_M = 1.5 V, V_{IN} = GND to 3.0 V.
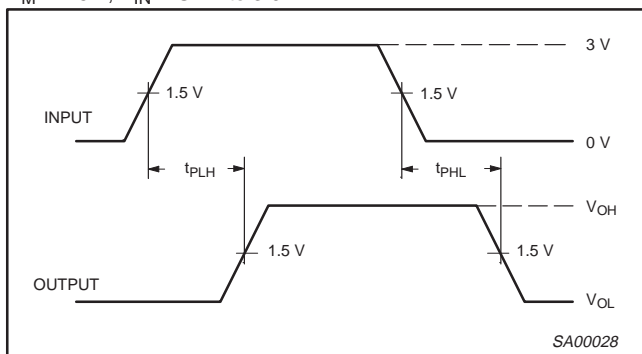
Waveform 1. Input (An) to Output (Yn) Propagation Delays

Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS

Load Circuit

TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
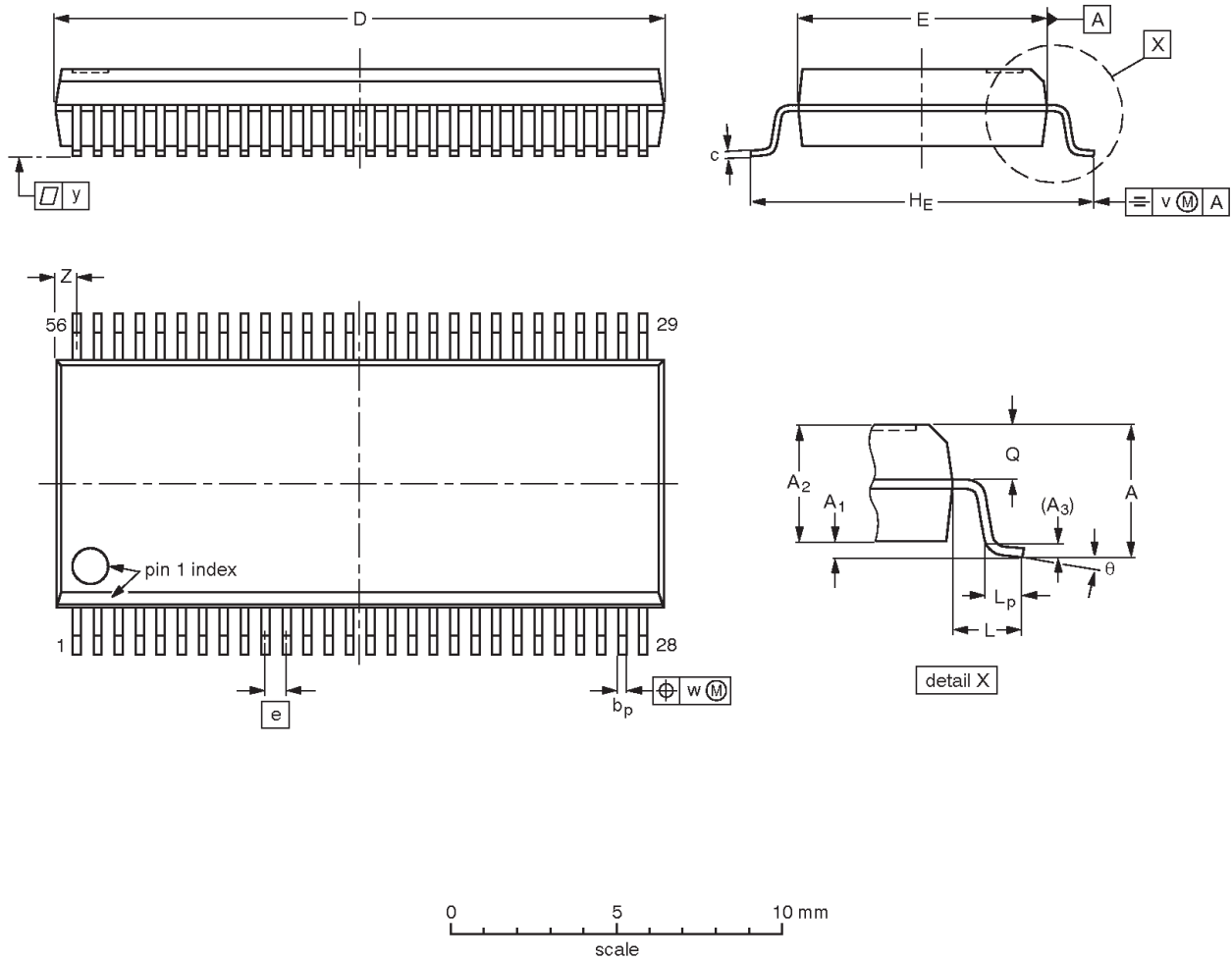
24-bit bus switch with 12-bit output enables

CBT16211

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.8	0.4 / 0.2	2.35 / 2.20	0.25	0.3 / 0.2	0.22 / 0.13	18.55 / 18.30	7.6 / 7.4	0.635	10.4 / 10.1	1.4	1.0 / 0.6	1.2 / 1.0	0.25	0.18	0.1	0.85 / 0.40	8° / 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118				~~95-02-04~~ 99-12-27

24-bit bus switch with 12-bit output enables

CBT16211

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

scale: 0   2.5   5 mm
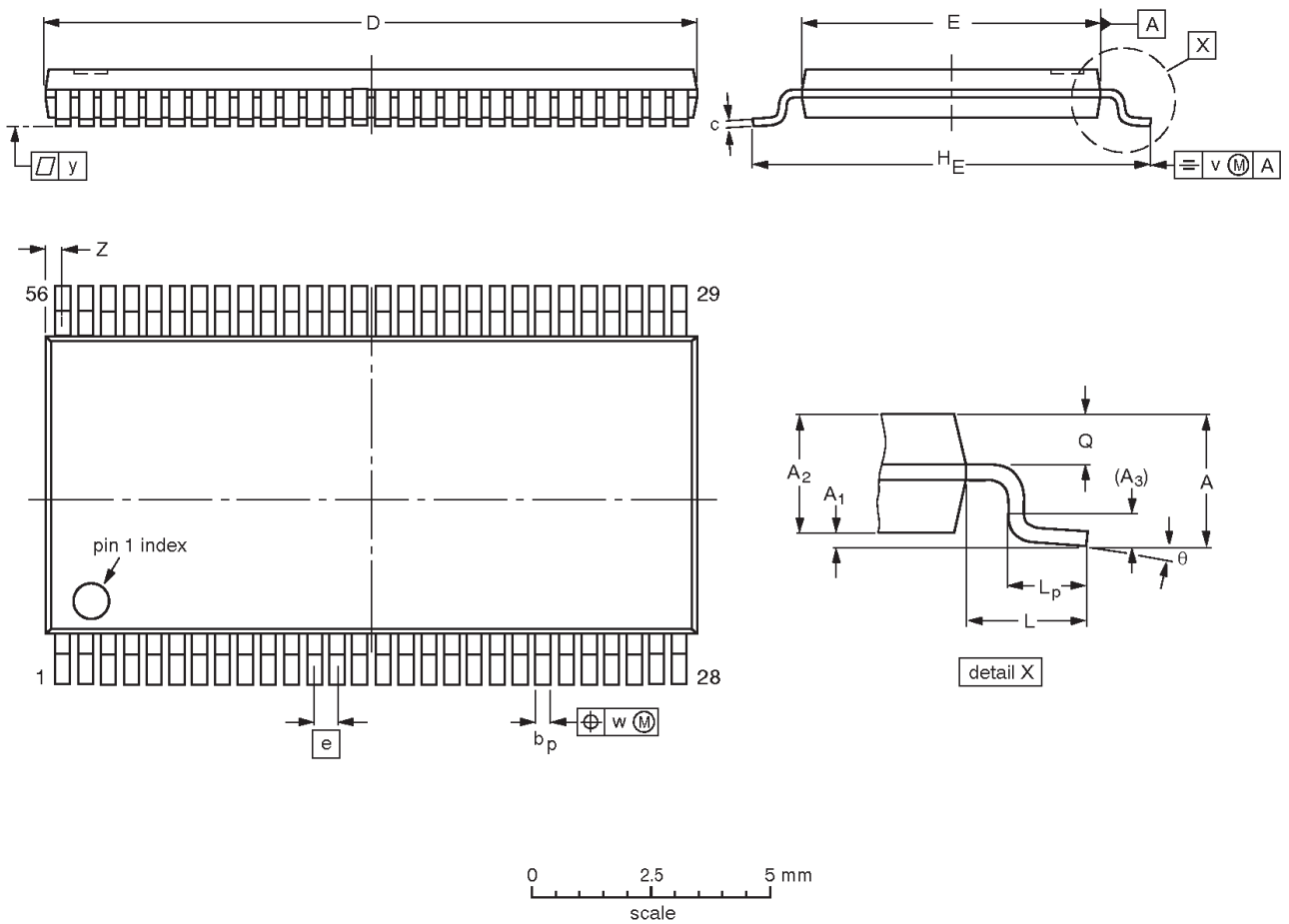
DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D(1)	E(2)	e	H_E	L	Lₚ	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153				~~95-02-10~~ 99-12-27

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Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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