



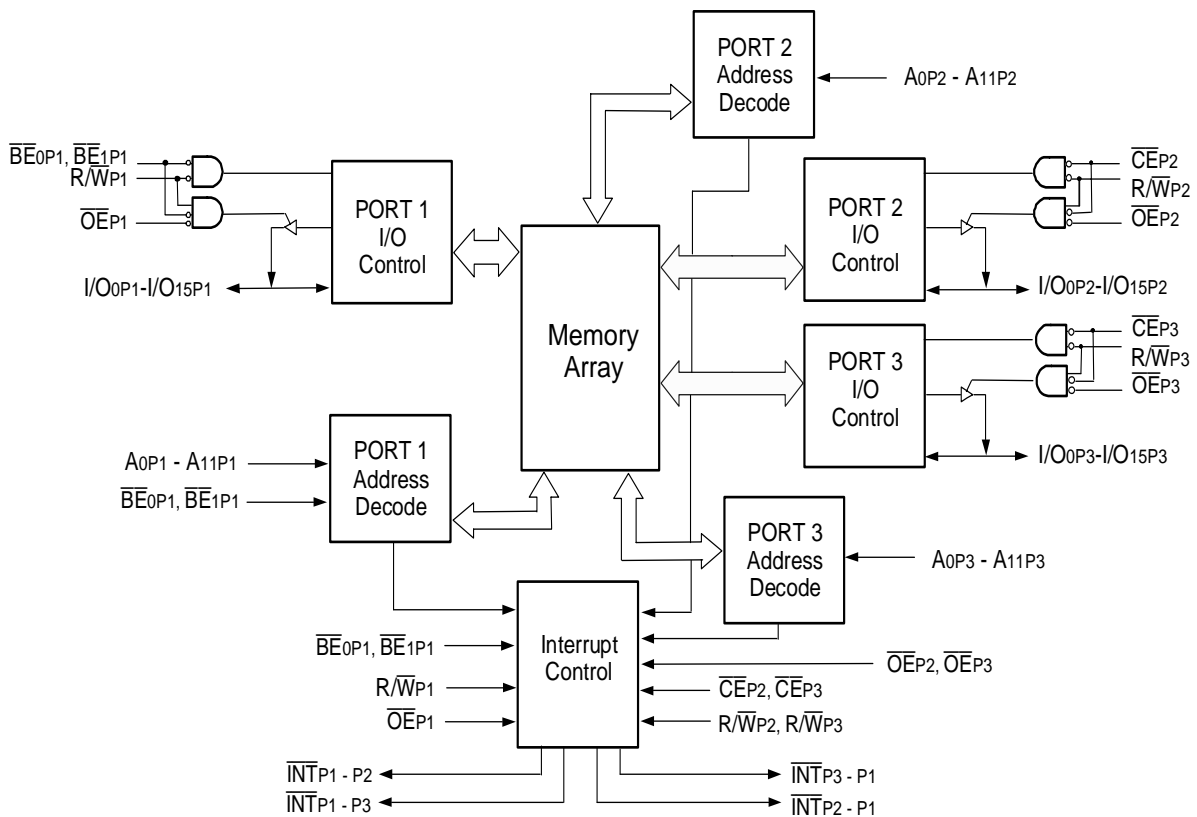
**HIGH-SPEED
8K x 16 TriPort
STATIC RAM**

**IDT70P5258ML
IDT70P525ML
IDT70V525ML**

Features

- ◆ **High-speed access**
 - Industrial: 55ns (max.)
- ◆ **Low-power operation**
 - IDT70P5258ML and IDT70P525ML
 - Active: 54mW (typ.)
 - Standby: 7.2μW (typ.)
 - IDT70V525ML
 - Active: 450mW (typ.)
 - Standby: 250μW (typ.)
- ◆ TriPort architecture allows simultaneous access to the memory from all three ports
- ◆ Fully asynchronous operation from each of the three ports: P1, P2, and P3
- ◆ IDT70P5258 supports 3.0V and 1.8V I/O's
- ◆ Available in 144-ball 0.5mm-pitch fpBGA
- ◆ Industrial temperature range (-40°C to +85°C)
- ◆ Green parts available, see ordering information

Functional Block Diagram



5681 dnw 01

JANUARY 2009

Description

The IDT70X525X is a high-speed 8K x 16 TriPort Static RAM designed to be used in systems where multiple access into a common RAM is required. This TriPort Static RAM offers increased system performance in multiprocessor systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

The IDT70X525X is also designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrated or withstand contention when more than one port

simultaneously accesses the same TriPort RAM location.

The IDT70X525X provides three independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from multiple ports. An automatic power down feature, controlled by \overline{BE}_0 and \overline{BE}_1 on Port 1 and \overline{CE} on Port 2 and on Port 3, permits the on-chip circuitry of each port to enter a very low power standby power mode.

The IDT70X525X is packaged in a 144-ball 0.5mm-pitch *fp*BGA.

Pin Configurations^(1,2,3)

70(P/V)525XBZ BZ-144

Top View

12/19/03

A1 I/O7P3	A2 I/O6P2	A3 I/O4P3	A4 I/O3P2	A5 I/O1P2	A6 \overline{OE}_P3	A7 R/ \overline{WP}_2	A8 NC	A9 A11P2	A10 A9P2	A11 A7P2	A12 A6P2
B1 I/O7P2	B2 I/O6P3	B3 VDD ⁽¹⁾	B4 I/O2P3	B5 I/O0P3	B6 \overline{OE}_P2	B7 \overline{CE}_P3	B8 NC	B9 A10P3	B10 A8P3	B11 A6P3	B12 A5P3
C1 I/O9P2	C2 VSS	C3 I/O5P2	C4 I/O2P2	C5 I/O0P2	C6 R/ \overline{WP}_3	C7 \overline{CE}_P2	C8 A11P3	C9 A10P2	C10 A8P2	C11 A5P2	C12 A4P3
D1 I/O10P3	D2 I/O8P2	D3 I/O5P3	D4 I/O3P3	D5 I/O1P3	D6 VDD	D7 VDD ⁽¹⁾	D8 VSS	D9 A9P3	D10 A7P3	D11 A4P2	D12 A3P2
E1 I/O11P3	E2 I/O11P2	E3 I/O8P3	E4 I/O4P2	E5 VDD	E6 VSS	E7 VSS	E8 VSS	E9 A0P3	E10 A3P3	E11 A2P3	E12 A2P2
F1 I/O12P3	F2 I/O12P2	F3 I/O9P3	F4 VDD ⁽¹⁾	F5 VDD ⁽¹⁾	F6 VSS	F7 VSS	F8 VSS	F9 VSS	F10 VDD	F11 A1P3	F12 A0P2
G1 I/O15P2	G2 I/O13P3	G3 I/O10P2	G4 I/O13P2	G5 VSS	G6 VSS	G7 VSS	G8 VSS	G9 VSS	G10 VDD	G11 A1P2	G12 VDD ⁽¹⁾
H1 I/O15P3	H2 I/O14P3	H3 I/O14P2	H4 VDD	H5 VSS	H6 VSS	H7 VSS	H8 VSS	H9 VDD	H10 VDD	H11 \overline{INT}_{P3P1}	H12 \overline{INT}_{P2P1}
J1 I/O2P1	J2 I/O1P1	J3 VDD	J4 VSS	J5 VSS	J6 VSS	J7 VSS	J8 VDD	J9 VDD	J10 A0P1	J11 \overline{INT}_{P1P3}	J12 \overline{INT}_{P1P2}
K1 I/O3P1	K2 I/O0P1	K3 I/O4P1	K4 VSS	K5 VDD	K6 VSS	K7 VDD	K8 VDD	K9 A10P1	K10 A3P1	K11 A2P1	K12 A1P1
L1 I/O6P1	L2 I/O5P1	L3 I/O8P1	L4 I/O10P1	L5 I/O12P1	L6 I/O14P1	L7 \overline{OE}_P1	L8 \overline{BE}_0P1	L9 NC	L10 A9P1	L11 A7P1	L12 A4P1
M1 I/O7P1	M2 VDD	M3 I/O9P1	M4 I/O11P1	M5 I/O13P1	M6 I/O15P1	M7 R/ \overline{WP}_1	M8 \overline{BE}_1P1	M9 A11P1	M10 A8P1	M11 A6P1	M12 A5P1

NOTES:

1. VDDQ for 70P5258.

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Pin Configurations^(1,2)

Symbol	Pin Name
A0P1 - A11P1	Address Lines - Port 1 (Input)
A0P2 - A11P2	Address Lines - Port 2 (Input)
A0P3 - A11P3	Address Lines - Port 3 (Input)
I/O0P1 - I/O15P1	Data I/O - Port 1
I/O0P2 - I/O15P2	Data I/O - Port 2
I/O0P3 - I/O15P3	Data I/O - Port 3
R/WP1	Read/Write - Port 1 (Input)
R/WP2	Read/Write - Port 2 (Input)
R/WP3	Read/Write - Port 3 (Input)
CEP2	Chip Enable - Port 2 (Input)
CEP3	Chip Enable - Port 3 (Input)
OE _{P1}	Output Enable - Port 1 (Input)
OE _{P2}	Output Enable - Port 2 (Input)
OE _{P3}	Output Enable - Port 3 (Input)
BE _{0P1}	Bank Enable 0 - Port 1 (Input)
BE _{1P1}	Bank Enable 1 - Port 1 (Input)
INTP1 - P2	Interrupt P1 - P2 - Port 1 (Output)
INTP1 - P3	Interrupt P1 - P3 - Port 1 (Output)
INTP2 - P1	Interrupt P2 - P1 - Port 2 (Output)
INTP3 - P1	Interrupt P3 - P1 - Port 3 (Output)
VDD	Power (Input)
VDDQ	Port Power Supply (Input) ^(3,4)
VSS	Ground (Input)

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NOTES:

1. All VDD pins must be connected to the power supply.
2. All VSS pins must be connected to the ground supply.
3. IDT70P5258 only.
4. For Port 2 and Port 3.

Capacitance⁽¹⁾

(TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Port	Conditions ⁽²⁾	Max	Unit
C _{IN}	Input Capacitance	Port 1	V _{IN} = 3dV	18	pF
		Port 2 & 3	V _{IN} = 3dV	9	pF
C _{OUT}	Output Capacitance	Port 1	V _{OUT} = 3dV	20	pF
		Port 2 & 3	V _{OUT} = 3dV	11	pF

NOTES:

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1. This parameter is determined by device characterization but is not production tested.
2. 3dV references the interpolated capacitance when the input and the output signals switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	Device	V _{SS}	V _{DD}
Industrial	-40°C to +85°C	70P525 70P5258	0V	1.8V ± 100mV
		70V525	0V	3.0V ± 300mV

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NOTE:

1. This is the parameter TA. This is the "instant on" case temperature.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Industrial	Unit
V _{TERM}	Supply Voltage on V _{DD} with Respect to GND	-0.5 to +2.9	V
V _{TERM}	Supply Voltage on V _{DDQ} with Respect to GND	-0.5 to +3.6	V
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to V _{DD} + 0.3 ⁽⁴⁾	V
T _{BIAS} ⁽³⁾	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
T _{JN}	Junction Temperature	+150	°C
I _{OUT} (for 70V525)	DC Output Current	50	mA
I _{OUT} (for 70P525 and 70P5258)	DC Output Current	20	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{DD} + 10% for Port 1 or V_{DDQ} + 10% for Port 2 and Port 3 for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ V_{DD} + 10% (Port 1) or V_{DDQ} + 10% (Port 2 and Port 3).
- Ambient Temperature under DC Bias. No AC Conditions. Chip Deselected.
- V_{DDQ} + 0.3V for 70P5258.

Recommended DC Operating Conditions

Symbol	Device	Port	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	70P5258	All	Supply Voltage	1.7	1.8	1.9	V
	70P525			1.7	1.8	1.9	
	70V525			2.7	3	3.3	
V _{DDQ}	70P5258	Port 2 & 3	I/O Supply Voltage ⁽¹⁾	2.7	3	3.3	V
	70P525	N/A		—	—	—	
	70V525	N/A		—	—	—	
V _{SS}	All	All	Ground	0	0	0	V
V _{IH}	70P5258	Port 1	Input High Voltage	1.2	—	V _{DD} +0.2	V
		Port 2 & 3		2	—	V _{DDQ} +0.2	
	70P525	All		1.2	—	V _{DD} +0.2	
	70V525	All		2	—	V _{DD} +0.2	
V _{IL}	70P5258	Port 1	Input Low Voltage	-0.2	—	0.4	V
		Port 2 & 3		-0.2	—	0.6	
	70P525	All		-0.2	—	0.4	
	70V525	All		-0.2	—	0.6	

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NOTES:

- The supply voltage for all ports on the IDT70P525 and IDT70V525 is supplied by V_{DD} so there are no V_{DDQ} pins on these devices.
- V_{IL} ≥ -1.5V for pulse width less than 10ns.
- V_{TERM} must not exceed V_{DD} + 10% for Port 1 or V_{DDQ} + 10% for Port 2 and Port 3.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range^(1,4)

Symbol	Parameter	Test Condition	Version	70P5258 70P525 Ind'l Only		70V525 Ind'l Only		Unit
				Typ. ⁽¹⁾	Max.	Typ. ⁽¹⁾	Max.	
I _{DD}	Dynamic Operating Current (Both Ports Active - CMOS Level Inputs)	$\overline{CE} = V_{IL}$, Outputs Open $f = f_{MAX}^{(2)}$	IND'L L	30	50	150	180	mA
ISB1	Standby Current (Both Ports - CMOS Level Inputs)	\overline{CE}_R and $\overline{CE}_L = V_{IH}$ $f = f_{MAX}^{(2)}$	IND'L L	.004	.016	5	10	mA
ISB2	Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^{*A} = V_{IL}$ and $\overline{CE}^{*B} = V_{IH}^{(3)}$, Active Port Outputs Open $f = f_{MAX}^{(2)}$	IND'L L	17	28	90	110	mA
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{DD0} - 0.2V$, $V_{IN} \geq V_{DD0} - 0.2V$ or $V_{IN} \leq 0.2V$ $f = f_{MAX}^{(2)}$	IND'L L	4	16	84	150	μA
ISB4	Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^{*A} < 0.2V$ and $\overline{CE}^{*B} > V_{DD0} - 0.2V^{(3)}$ $V_{IN} \geq V_{DD0} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port Outputs Open $f = f_{MAX}^{(2)}$	IND'L L	17	28	90	110	mA

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NOTES:

- V_{DD} = 1.8V for 70P5258 and 70P525. V_{DD} = 3.0V for 70V525, T_A = +25°C, and are not production tested. I_{DD} DC = 15mA (typ.)
- At f = f_{MAX}, address and control lines are cycling at the maximum frequency read cycle of 1/trc, and using "AC Test Conditions".
- For the 70P5258, if Port "A" is Port 1 then Port "B" may be either Port 2 or Port 3. If Port "A" is either Port 2 or Port 3, Port "B" must be Port 1.
- V_{DD} = 1.8V ± 100mV for 70P525 and 70P5258. V_{DD} = 3.0V ± 300mV for 70V525.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽²⁾

Symbol	Device	Port	Parameter	Test Conditions	Min.	Max.	Unit
I _{LI}	70P5258	All	Input Leakage Current	V _{DD} = 1.8V, V _{IN} = 0V to V _{DD}	—	1	μA
	70P525	All		V _{DD} = 1.8V, V _{IN} = 0V to V _{DD}	—	1	
	70V525	All		V _{DD} = 3.0V, V _{IN} = 0V to V _{DD}	—	1	
I _{LO}	70P5258	All	Output Leakage Current	$\overline{CE}_X = \overline{BE}_X = V_{IH}$, V _{OUT} = 0V to V _{DD}	—	1	μA
	70P525	All		$\overline{CE}_X = \overline{BE}_X = V_{IH}$, V _{OUT} = 0V to V _{DD}	—	1	
	70V525	All		$\overline{CE}_X = \overline{BE}_X = V_{IH}$, V _{OUT} = 0V to V _{DD}	—	1	
V _{OL}	70P5258	Port 1	Output Low Voltage	I _{OL} = +0.1mA	—	0.2	V
		Port 2 & 3		I _{OL} = +2mA	—	0.4	
	70P525	All		I _{OL} = +0.1mA	—	0.2	
	70V525	All		I _{OL} = +2mA	—	0.4	
V _{OH}	70P5258	Port 1	Output High Voltage	I _{OH} = -0.1mA	1.4	—	V
		Port 2 & 3		I _{OH} = -2mA	2.1	—	
	70P525	All		I _{OH} = -0.1mA	1.4	—	
	70V525	All		I _{OH} = -2mA	2.1	—	

5681 tbl 07

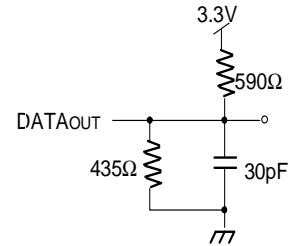
NOTE:

- At V_{DD} ≤ 2.0V input leakages are undefined.
- V_{DD} = 1.8V ± 100mV for 70P525 and 70P5258. V_{DD} = 3.0V ± 300mV for 70V525.

AC Test Conditions

Input Pulse Levels	GND to 3.0V/GND to 1.8V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V/0.9V
Output Reference Levels	1.5V/0.9V
Output Load	Figures 1, 2 and 3

5681 tbl 08

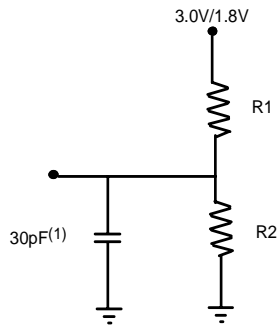


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Figure 2. AC Output Test Load for the 70V525

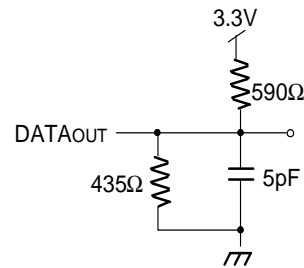
	3.0V	1.8V
R1	1022Ω	13500Ω
R2	729Ω	10800Ω

5681 tbl 09



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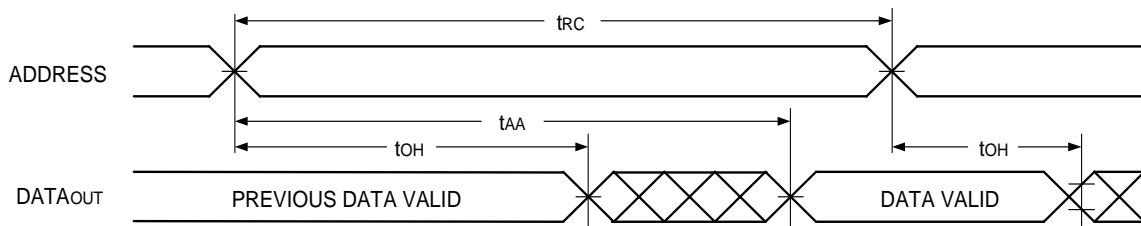
Figure 1. AC Output Test Load for the 70P525 and 70P5258



5681 drw 06

Figure 3. AC Output Test Load for the 70V525 (for tHZ, tLX, tWZ, tOW)

Timing Waveform of Read Cycle No. 1, Any Port⁽¹⁾



NOTE:

1. $R/\bar{W} = V_{IH}$ and $\bar{C}\bar{E}$ (or $\bar{B}\bar{E}x$) = V_{IL} .

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AC Electrical Characteristics Over the Operating Temperature and Supply Voltage

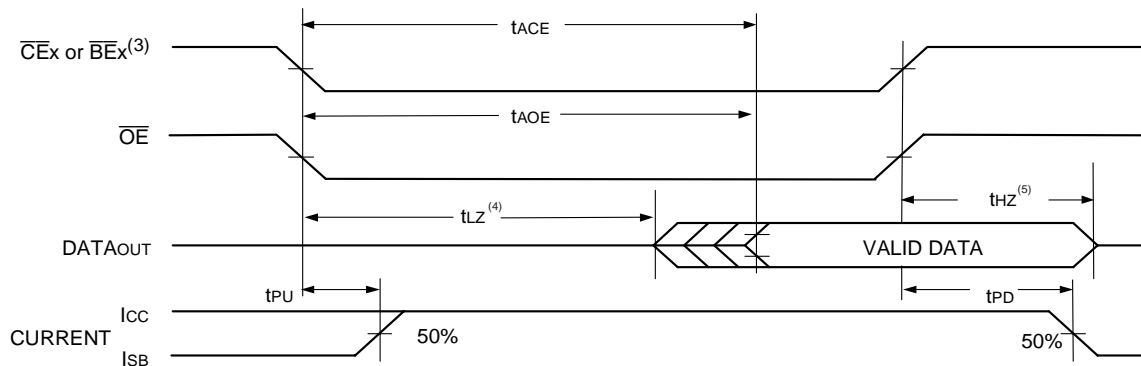
Symbol	Parameter	70X525X Ind'l Only		Unit
		Min.	Max.	
READ CYCLE				
t _{RC}	Read Cycle Time	55	—	ns
t _{AA}	Address Access Time	—	55	ns
t _{ACE}	Chip Enable Access Time	—	55	ns
t _{AOE}	Output Enable Access Time	—	30	ns
t _{OH}	Output Hold from Address Change	5	—	ns
t _{LZ}	Output Low-Z Time ^(1,2)	5	—	ns
t _{HZ}	Output High-Z Time ^(1,2)	—	25	ns
t _{PU}	Chip Enable to Power Up Time ⁽²⁾	0	—	ns
t _{PD}	Chip Disable to Power Down Time ⁽²⁾	—	55	ns

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NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.

Timing Waveform of Read Cycle No. 2, Any Port^(1, 2)



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NOTES:

1. $R/\overline{W} = V_{IH}$ for Read Cycles.
2. Addresses valid prior to or coincident with \overline{CEx} (or \overline{BEx}) transition LOW.
3. \overline{CEx} for Port 2 or Port 3, \overline{BEx} for Port 1.
4. Timing depends on which signal is asserted last, \overline{CEx} (or \overline{BEx}) or \overline{OE} .
5. Timing depends on which signal is deasserted first, \overline{CEx} (or \overline{BEx}) or \overline{OE} .

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage

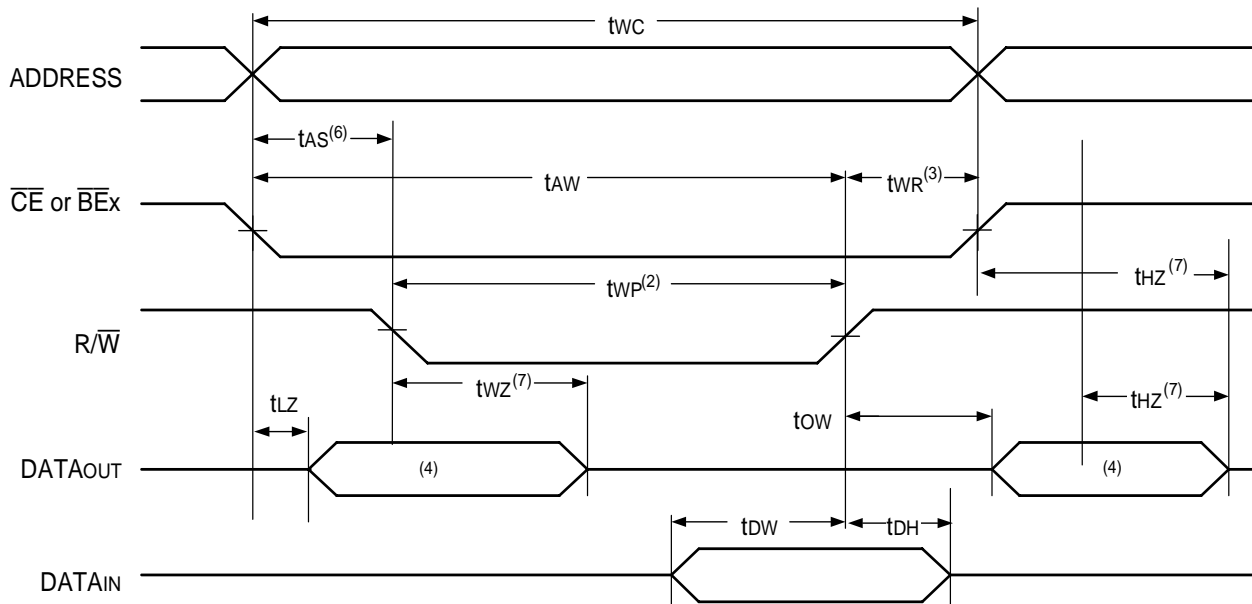
Symbol	Parameter	70X525X Ind'l Only		Unit
		Min.	Max.	
WRITE CYCLE				
t _{WC}	Write Cycle Time	55	—	ns
t _{EW}	Chip Enable to End-of-Write	45	—	ns
t _{AW}	Address Valid to End-of-Write	45	—	ns
t _{AS}	Address Set-up Time	0	—	ns
t _{WP}	Write Pulse Width ⁽³⁾	40	—	ns
t _{WR}	Write Recovery Time	0	—	ns
t _{DW}	Data Valid to End-of-Write	30	—	ns
t _{HZ}	Output High-Z Time ^(1,2)	—	25	ns
t _{DH}	Data Hold Time	0	—	ns
t _{WZ}	Write Enable to Output in High-Z ^(1,2)	—	25	ns
t _{OW}	Output Active from End-of-Write ^(1,2)	0	—	ns

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NOTES:

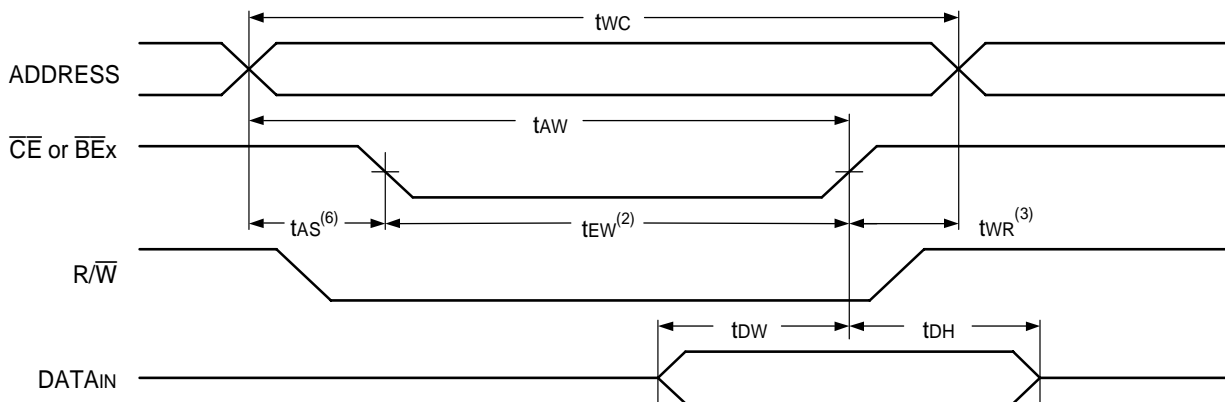
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.

Timing Waveform of Write Cycle No. 1, R/\bar{W} Controlled Timing⁽⁵⁾



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Timing Waveform of Write Cycle No. 2, \bar{CE} Controlled Timing^(1,5)



5681 drw 10

NOTES:

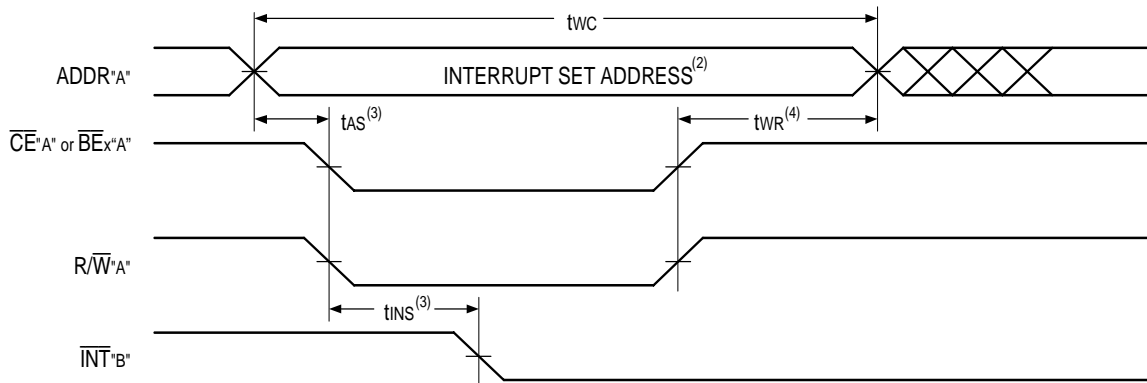
1. R/\bar{W} or \bar{CE} (or $\bar{BE}x$) = V_{IH} during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a \bar{CE} (or $\bar{BE}x$) = V_{IL} and a R/\bar{W} = V_{IL} .
3. t_{WR} is measured from the earlier of \bar{CE} (or $\bar{BE}x$) or R/\bar{W} = V_{IH} to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the \bar{CE} (or $\bar{BE}x$) LOW transition occurs simultaneously with or after the R/\bar{W} = V_{IL} transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, \bar{CE} (or $\bar{BE}x$) or R/\bar{W} .
7. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 3). This parameter is guaranteed but is not production tested.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

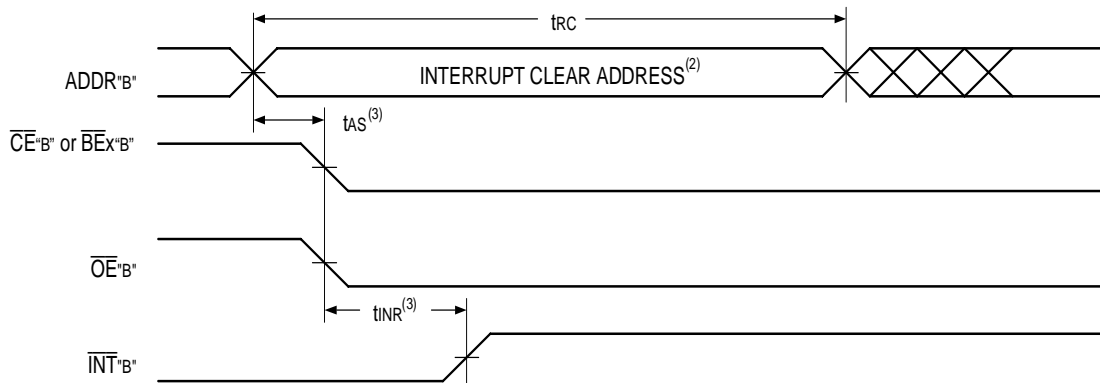
Symbol	Parameter	70X525X Ind'l Only		Unit
		Min.	Max.	
INTERRUPT TIMING				
tAS	Address Set-up Time	0	—	ns
tWR	Write Recovery Time	0	—	ns
tINS	Interrupt Set Time	—	45	ns
tNR	Interrupt Reset Time	—	45	ns

5681 tbl 12

Waveform of Interrupt Timing⁽¹⁾



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5681 drw 13

NOTES:

1. If Port A is Port 1, Port B may be either Port 2 or Port 3. If Port A is either Port 2 or Port 3, Port B must be Port 1.
2. See Interrupt Truth Table II.
3. Timing depends on which enable signal (CE or R/W) is asserted last.
4. Timing depends on which enable signal (CE or R/W) is de-asserted first.

Functional Description

The IDT70X525X provides three ports with separate control, address, and I/O pins that permit independent access for reads or writes to the two banks of memory. These devices have an automatic power down feature controlled by \overline{BE}_0 and \overline{BE}_1 on Port 1 and \overline{CE} on Port 2 and Port 3. The \overline{CE} (or \overline{BE}_x) controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected (\overline{CE} or $\overline{BE}_x = V_{IH}$). When Port 1 is enabled, it has access to the full memory. When Port 2 is active it has access to Bank 1 of the memory. When Port 3 is active it has access to Bank 2 of the memory. See Truth Table I for a description of the Read/Write operation.

Truth Table I – Read/Write Control

	\overline{BE}_0	\overline{BE}_1	R/W	\overline{CE}	\overline{OE}	D0-D15	Function
PORT 1	H	H	X	X	X	Z	Port Deselected
	L	H	L	X	X	DATA _{IN}	Data on port written into Memory Bank 0
	L	H	H	X	L	DATA _{OUT}	Data in Memory Bank 0 output on port
	H	L	L	X	X	DATA _{IN}	Data on port written into Memory Bank 1
	H	L	H	X	L	DATA _{OUT}	Data in Memory Bank 1 output on port
	X	X	X	X	H	Z	Outputs Disabled
	L	L	X	X	X	X	Not Allowed
PORT 2 or PORT 3	X	X	X	H	X	Z	Port Deselected
	X	X	L	L	X	DATA _{IN}	Data on port written into Memory Bank ⁽²⁾
	X	X	H	L	L	DATA _{OUT}	Data in Memory Bank ⁽²⁾ output on port
	X	X	X	X	H	Z	Outputs Disabled
	H	H	X	H	X	Z	$\overline{BE}_0 = \overline{BE}_1 = \overline{CE}_{P3} = V_{IH}$, Sleep mode

5681 tbl 13

NOTE:

- Both \overline{BE}_0 , and \overline{BE}_1 cannot be active ($\overline{BE}_x = V_{IH}$) simultaneously.
- Memory Bank 0 for Port 2. Memory Bank 1 for Port 3.

Interrupts

If the user chooses the interrupt function, a memory location (mailbox or message center) is assigned to each port. Interrupt $P_1 - P_2$ of Port 1 ($\overline{INT}_{P_1 - P_2}$) is asserted when Port 2 writes to memory location FFE (HEX), where a write is defined as $\overline{CE} = R/\overline{W} = V_{IL}$ per Truth Table II. Port 1 clears the interrupt by accessing address location FFE when $\overline{BE}_0 = V_{IL}$, R/\overline{W} is a "don't care". Interrupt $P_1 - P_3$ of Port 1 ($\overline{INT}_{P_1 - P_3}$) is asserted when Port 3 writes to memory location FFE (HEX), where a write is defined as $\overline{CE} = R/\overline{W} = V_{IL}$. Port 1 clears the interrupt by accessing address location FFE

when $\overline{BE}_1 = V_{IL}$, R/\overline{W} is a "don't care". Port 2's interrupt flag ($\overline{INT}_{P_2 - P_1}$) is asserted when Port 1 writes to memory location FFF (HEX), where a write is defined as $\overline{BE}_0 = R/\overline{W} = V_{IL}$. Port 2 clears the interrupt by accessing address location FFF when $\overline{CE} = V_{IL}$, R/\overline{W} is a "don't care". Likewise, Port 3's interrupt flag ($\overline{INT}_{P_3 - P_1}$) is asserted when Port 1 writes to memory location FFF (HEX), where a write is defined as $\overline{BE}_1 = R/\overline{W} = V_{IL}$. Port 3 clears the interrupt by accessing address location FFF when $\overline{CE} = V_{IL}$, R/\overline{W} is a "don't care".

Truth Table II - Interrupt Flag

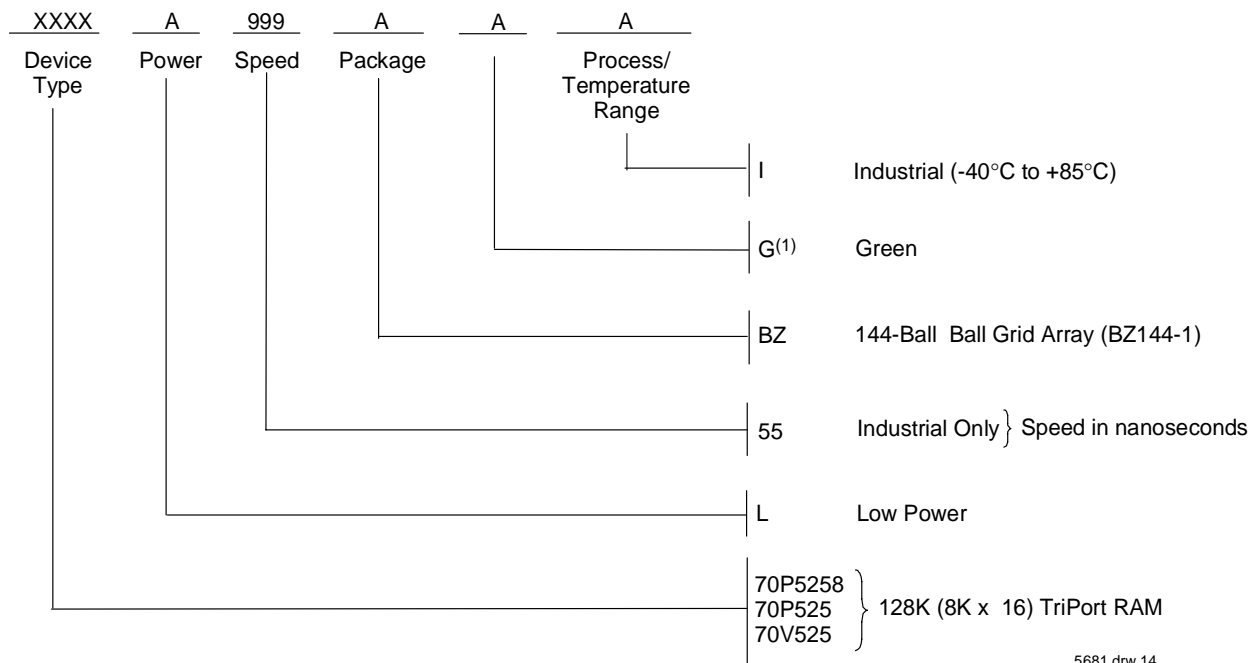
Port 1							Port 2 or 3					Function
R/ \overline{W}	\overline{BE}_0	\overline{BE}_1	\overline{OE}	A11 - A0	$\overline{INT}_{P_1 - P_2}$	$\overline{INT}_{P_1 - P_3}$	R/ \overline{W}	\overline{CE}	\overline{OE}	A11 - A0	$\overline{INT}_{P_x - P_1}$	
L	L	H	X	FFF	X	X	X	X	X	X	L	Set P2 \overline{INT} Flag
X	X	X	X	X	X	X	X	L	L	FFF	H	Reset P2 \overline{INT} Flag
L	H	L	X	FFF	X	X	X	X	X	X	L	Set P3 \overline{INT} Flag
X	X	X	X	X	X	X	X	L	L	FFF	H	Reset P3 \overline{INT} Flag
X	X	X	X	X	L	X	L	L	X	FFE	X	Set P1 $\overline{INT}_{P_1 - P_2}$ Flag ⁽¹⁾
X	L	H	L	FFE	H	X	X	X	X	X	X	Reset P1 $\overline{INT}_{P_1 - P_2}$ Flag
X	X	X	X	X	X	L	L	L	X	FFE	X	Set P1 $\overline{INT}_{P_1 - P_3}$ Flag ⁽²⁾
X	H	L	L	FFE	X	H	X	X	X	X	X	Reset P1 $\overline{INT}_{P_1 - P_3}$ Flag

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NOTE:

- Port 2 sets the $\overline{INT}_{P_1 - P_2}$ flag on Port 1 so all signals refer to Port 2.
- Port 3 sets the $\overline{INT}_{P_1 - P_3}$ flag on Port 1 so all signals refer to Port 3.

Ordering Information



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NOTE:

1. Green parts available. For specific speeds, packages and powers contact your sales office.

Datasheet Document History

10/14/03:	Initial datasheet
03/23/04:	Page 7 Corrected to _H spec min to 5ns in AC Electrical Characteristics Table 10
5/26/05:	Page 1 Added green availability to features
	Page 13 Added green indicator to ordering information
	Page 1 & 13 Replaced old logo ® with new ™ logo
05/08/06:	Page 5 Updated V _{TERM} in Absolute Maximum Ratings table and added footnote 3 & 4
07/25/08:	Page 6 Corrected a typo in the DC Chars table
01/19/09:	Page 14 Removed "IDT" from orderable part number



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