

RoHS-Compliant 1.063/1.25/2.125 Gbps 850 nm SFP Transceiver

PLRXPL-VI-S24-22



Key Features

- Compliant with industry-wide physical and optical specifications
- Lead free and RoHS compliant
- Cost-effective SFP solution
- Triple-rate FC/Ethernet performance
- Enables higher port densities
- Enables greater bandwidth
- Proven high reliability

Applications

- High-speed storage area networks
 - Switch and hub interconnect
 - Mass storage systems interconnect
 - Host adapter interconnect
- Computer cluster cross-connect
- Custom high-speed data pipes
- Short-reach Ethernet

This lead-free and RoHS-compliant multirate small form factor pluggable (SFP) transceiver provides superior performance for Fibre Channel and Ethernet applications, and is another in our family of products customized for high-speed, short-reach SAN and intra-POP applications. The multirate feature enables its use in a wider range of system applications. It is fully compliant with FC-PI 100-M5/M6-SN-I, 200-M5/M6-SN-I, and 1000BASE-SX specifications. The housing provides improved EMI performance for demanding applications. This transceiver features a highly-reliable 850 nm oxide vertical-cavity surface-emitting laser (VCSEL) coupled to an LC optical connector. Its small size allows for high-density board designs that, in turn, enable greater total aggregate bandwidth.

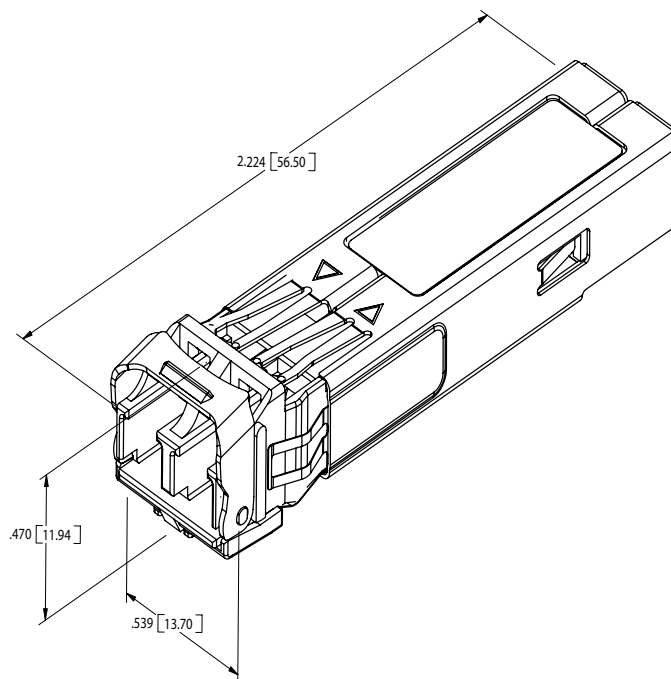
Highlights

- 1 G FC, 2 G FC, and 1 GE triple-rate performance enables flexible system design and configuration
- Lead free and RoHS compliant per European Directive 2002/95/EC
- Enhanced digital diagnostic feature set allows real-time monitoring of transceiver performance and system stability
- Bail mechanism enables superior ergonomics and functionality in all port configurations
- Extended voltage and extended temperature
- MSA-compliant small form factor footprint
- Serial ID allows customer- and vendor-system-specific information to be placed in transceiver
- All-metal housing provides superior EMI performance

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PLRXPL-VI-S24-22 Features

- Uses a highly-reliable, high-speed, 850 nm, oxide VCSEL
- Lead free and RoHS compliant
- Hot pluggable
- Digital diagnostics, SFF-8472 rev 9.5 compliant
- Compliant with Fibre Channel 200-M5/M6-SN-I and 100-M5/M6-SN-I
- Compliant with 1000BASE-SX, IEEE 802.3
- Low nominal power consumption (400 mW)
- -40°C to 85°C operating temperature range
- Single +3.3 V power supply
- $\pm 10\%$ extended operating voltage range
- Bit error rate $< 1 \times 10^{-12}$
- Open Collector Transmit disable, loss of signal and transmitter fault functions
- CDRH and IEC 60825-1 Class 1 laser eye safe
- FCC Class B compliant
- ESD Class 2 per MIL-STD 883



Dimensions in inches [mm]

An eye-safe, cost effective serial transceiver, the PLRXPL-VI-S24-22 features a small, low-power, pluggable package that manufacturers can upgrade in the field, adding bandwidth incrementally. The robust mechanical design features a unique all-metal housing that provides superior EMI shielding.

Section 1 Functional Description

The PLRXPL-VI-S24-22 850 nm VCSEL Gigabit transceiver is designed to transmit and receive 8B/10B encoded serial optical data over 50/125 μm or 62.5/125 μm multimode optical fiber.

Transmitter

The transmitter converts 8B/10B encoded serial PECL or CML electrical data into serial optical data meeting the requirements of 100-M5/M6-SN-I, 200-M5/M6-SN-I Fibre Channel specifications and 1000BASE-SX Ethernet. Transmit data lines (TD+ & TD-) are internally AC coupled with 100 Ω differential termination.

An open collector compatible Transmit Disable (Tx_Dis) is provided. This pin is internally terminated with a 10 k Ω resistor to Vcc_T. A logic 1 or no connection on this pin will disable the laser from transmitting. A logic 0 on this pin provides normal operation.

The transmitter has an internal PIN monitor diode that is used to ensure constant optical power output across supply voltage and temperature variations.

An open collector compatible Transmit Fault (TFault) is provided. The Transmit Fault signal must be pulled high on the host board for proper operation. A logic 1 output from this pin indicates that a transmitter fault has occurred, or the part is not fully seated and the transmitter is disabled. A logic 0 on this pin indicates normal operation.

Receiver

The receiver converts 8B/10B encoded serial optical data into serial PECL/CML electrical data. Receive data lines (RD+ & RD-) are internally AC coupled with 100 Ω differential source impedance, and must be terminated with a 100 Ω differential load.

The receiver's bandwidth has been optimized for fully compliant operation at 1.063/1.25/2.125 Gbps line rates without the use of rate select.

An open collector compatible Loss of Signal is provided. The LOS must be pulled high on the host board for proper operation. A logic 0 indicates that light has been detected at the input to the receiver. A logic 1 output indicates that insufficient light has been detected for proper operation.

Power supply filtering is recommended for both the transmitter and receiver. Filtering should be placed on the host assembly as close to the Vcc pins as possible for optimal performance.

Application schematics are shown in Figure 2 on page 5.

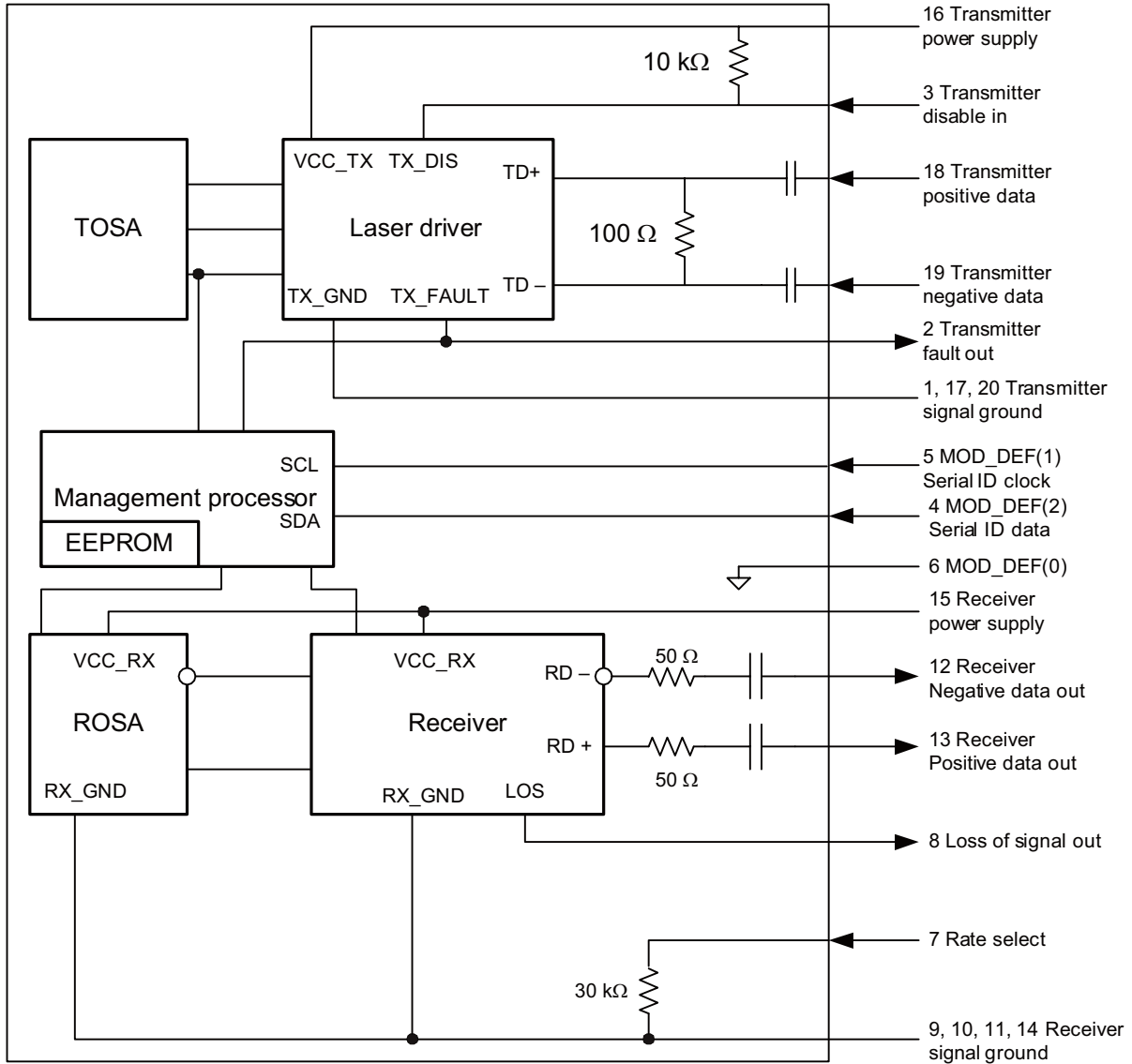
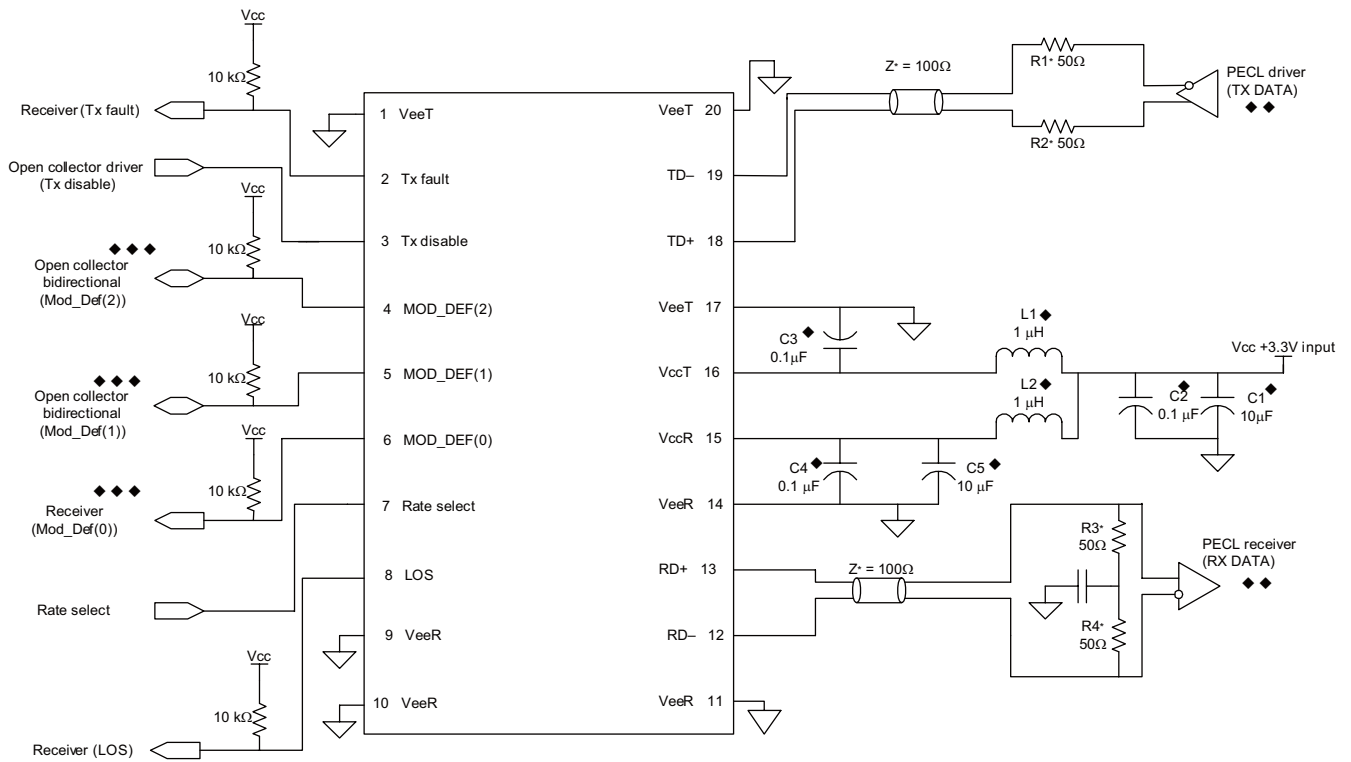


Figure 1. Block diagram

Section 2 Application Schematics

Recommended connections to the transceiver are shown below.



Notes

- ◆ Power-supply filtering components should be placed as close to the V_{cc} pins of the host connector as possible for optimal performance.
- ◆◆ The PECL driver and receiver will require biasing networks. Please consult application notes from suppliers of these components. CML I/O on the PHY are supported.
- ◆◆◆ MOD_DEF(2) and MOD_DEF(1) should be bi-directional open collector connections in order to implement serial ID (MOD_DEF[0,1,2]) PLRXPL-VI-S24-22 transceiver.
- ◆◆◆◆ R1 and R2 may be included in the output of the PHY. Check application notes of the IC in use.
- * Transmission lines should be 100 Ω differential traces. It is recommended that the termination resistor for the PECL receiver (R3 + R4) be placed beyond the input pins of the PECL receiver. Series source termination resistors on the PECL Driver (R1+R2) should be placed as close to the driver output pins as possible.

Figure 2. Recommended application schematic

2.1 Technical Data

Technical data related to the transceiver includes:

- Section 2.2 Pin Function Definitions
- Section 2.3 Absolute Maximum Ratings
- Section 2.4 Electrical Characteristics
- Section 2.5 Optical Characteristic
- Section 2.6 Link Lengths
- Section 2.7 Regulatory Compliance
- Section 2.8 PCB Layout
- Section 2.9 Front Panel Opening
- Section 2.10 Module Outline
- Section 2.11 Transceiver Belly-to-Belly Mounting

2.2 Pin Function Definitions

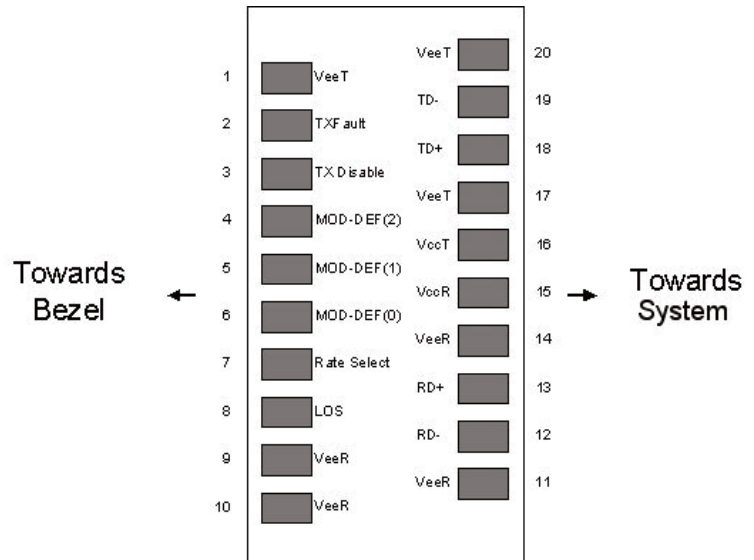


Figure 3. Transceiver pin descriptions

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Table 1. Transceiver Pin Descriptions

Pin Number	Symbol	Name	Description
Receiver			
8	LOS	Loss of signal out (OC)	Sufficient optical signal for potential BER $< 1 \times 10^{-12}$ = logic 0 Insufficient optical signal for potential BER $< 1 \times 10^{-12}$ = logic 1 This pin is open collector compatible, and should be pulled up to Host Vcc with a 10 k Ω resistor.
9, 10, 11, 14	VeeR	Receiver signal ground	These pins should be connected to signal ground on the host board.
12	RD-	Receiver negative DATA out (PECL)	Light on = Logic 0 output Receiver DATA output is internally AC coupled and series terminated with a 50 Ω resistor.
13	RD+	Receiver positive DATA out (PECL)	Light on = Logic 1 output Receiver DATA output is internally AC coupled and series terminated with a 50 Ω resistor.
15	VccR	Receiver power supply	This pin should be connected to a filtered +3.3 V power supply on the host board. See Application Schematics for filtering suggestions.
7	Rate select	Rate select (LVTTL)	This pin has an internal 30K pulldown to ground. The signal level should not change during module operation.
Transmitter			
3	TX disable	Transmitter disable in (LVTTL)	Logic 1 input (or no connection) = laser off Logic 0 input = laser on This pin is internally pulled up to Vcc _T with a 10 k Ω resistor.
1, 17, 20	VeeT	Transmitter signal ground	These pins should be connected to signal ground on the host board.
2	TX fault	Transmitter fault out (OC)	Logic 1 output = laser fault (laser off before t _{fault}) Logic 0 output = normal operation This pin is open collector compatible, and should be pulled up to Host Vcc with a 10 k Ω resistor.
16	VccT	Transmitter power supply	This pin should be connected to a filtered +3.3 V power supply on the host board. See Application Schematics for filtering suggestions.
18	TD+	Transmitter positive DATA in (PECL)	Logic 1 input = light on Transmitter DATA inputs are internally AC coupled and terminated with a differential 100 Ω resistor.
19	TD-	Transmitter negative DATA in (PECL)	Logic 0 input = light on Transmitter DATA inputs are internally AC coupled and terminated with a differential 100 Ω resistor.
Module Definition			
4, 5, 6	MOD_DEF(0:2)	Module definition identifiers	Serial ID with SFF 8472 diagnostics (see section 3.1) Module definition pins should be pulled up to Host Vcc with 10 k Ω resistors.

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2.3 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Storage temperature	T_{st}	-40 to +95	°C
Operating case temperature	T_c	-40 to +85	°C
Power supply voltage	V_{cc}	0 to +4.0	V
Transmitter differential input voltage	V_D	2.5	V_{p-p}
Relative humidity	RH	5 to 95	%

2.4 Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply voltage	V_{cc}	2.97	3.3	3.63	V	
Data rate		1.0	2.125	2.2	Gbps	BER < 1×10^{-12}
Operating temperature range	T_c	-40		85	°C	
Transmitter						
Supply current	I_{CCT}		40	70	mA	
Data input voltage swing	V_{TDP-p}	250	800	2200	mV_{p-p}	Differential, peak to peak
Data input rise/fall time		60		175	ps	20% – 80%, differential 2 Gbd operation ³
Data input rise/fall time		60		350	ps	20% – 80%, differential 1 Gbd operation ³
Data input skew				20	ps	
Data input deterministic jitter	DJ			0.12	UI	$\pm K28.5$ pattern, δ_{Tj} , @1.062 Gbps ^{1,5}
Data input deterministic jitter	DJ			0.14	UI	$\pm K28.5$ pattern, δ_{Tj} , @2.125 Gbps ^{1,5}
Data input deterministic jitter	DJ			0.1	UI	$\pm K28.5$ pattern, TP1, @1.25 Gbps ^{1,5}
Data input total jitter	TJ			0.25	UI	2^7-1 pattern, δ_{Tj} , BER < 1×10^{-12} , @1.062 Gbps ^{1,5}
Data input total jitter	TJ			0.26	UI	2^7-1 pattern, δ_{Tj} , BER < 1×10^{-12} , @2.125Gbps ^{1,5}
Data input total jitter	TJ			0.24	UI	2^7-1 pattern, TP1, BER < 1×10^{-12} , @1.25 Gbps ^{1,5}
Transmit disable voltage level	V_{IH} V_{IL}	$V_{cc} - 1.0$ 0		V_{cc} 0.8	V V	Laser output disabled after T_{TD} if input level is V_{IH} ; laser output enabled after T_{TEN} if input level is V_{IL} .
Transmit disable/enable assert time	T_{TD} T_{TEN}			10 1	μs ms	Laser output disabled after T_{TD} if input level is V_{IH} ; laser output enabled after T_{TEN} if input level is V_{IL} .
Transmit fault output voltage level	V_{OH} V_{OL}	$V_{cc} - 0.5$ 0		V_{cc} 0.5	V V	Transmit fault level is V_{OH} and laser output disabled T_{Fault} after laser fault.
Transmit fault assert and reset times	T_{Fault} T_{Reset}			100	μs μs	Transmitter fault is V_{OL} and laser output restored T_{INI} after transmitter disable is asserted for T_{Reset} , then disabled.
Initialization time	T_{INI}			300	ms	After hot plug or $V_{cc} \geq 2.97V$.

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2.4 Electrical Characteristics

(continued)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver						
Supply current	I_{CCR}		85	120	mA	
Data output voltage swing		600			mV _{p-p}	$R_{LOAD} = 100 \Omega$, differential
Data output rise/fall time			90	200	ps	20% - 80%, differential
Data output skew				50	ps	$R_{LOAD} = 100 \Omega$, differential
Data output deterministic jitter	DJ			0.36	UI	$\pm K28.5$ pattern, δ_R , @1.062 Gbps ^{1,9}
Data output deterministic jitter	DJ			0.39	UI	$\pm K28.5$ pattern, δ_R , @2.125 Gbps ^{1,5}
Data output deterministic jitter	DJ			0.46	UI	$\pm K28.5$ pattern, TP4, @1.25 Gbps ^{1,5}
Total jitter	TJ			0.61	UI	2 ⁷ -1 pattern, δ_R , BER < 1×10^{-12} @1.062 Gbps ^{1,5}
Total jitter	TJ			0.64	UI	2 ⁷ -1 pattern, δ_R , BER < 1×10^{-12} @2.125 Gbps ^{1,5}
Total jitter	TJ			0.75	UI	2 ⁷ -1 pattern, TP4, BER < 1×10^{-12} @1.25 Gbps ^{1,5}
Loss of signal voltage level	V_{OH}	$V_{cc} - 0.5$		V_{cc}	V	LOS output level V_{OL} T_{LOSD} after light input > LOSD ²
	V_{OL}	0		0.5	V	LOS output level V_{OH} T_{LOSA} after light input < LOSA ²
Loss of signal assert/deassert time	T_{LOSA}			100	μ s	LOS output level V_{OL} T_{LOSD} after light input > LOSD ²
	T_{LOSD}			100	μ s	LOS output level V_{OH} T_{LOSA} after light input < LOSA ²

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2.5 Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Wavelength	λ_p	830	850	860	nm	
RMS spectral width	$\Delta\lambda$		0.5	0.85	nm	
Average optical power	P_{AVG}	-9.5		-2.5	dBm	
Optical output rise/fall time	$t_{rise/fall}$			150	ps	20% – 80%
Optical modulation amplitude	OMA	200	500	1125	μ W	
Extinction ratio	ER	9			dB	
Deterministic jitter	DJ			0.21	UI	\pm K28.5 pattern, γ_T , @1.062 Gbps ^{1,5}
Deterministic jitter	DJ			0.26	UI	\pm K28.5 pattern, γ_T , @2.125 Gbps ^{1,5}
Deterministic jitter	DJ			0.20	UI	\pm K28.5 pattern, TP2, @1.25 Gbps ^{1,5}
Total jitter	TJ			0.43	UI	2^7-1 pattern, γ_T , @1.062 Gbps ^{1,5}
Total jitter	TJ			0.44	UI	2^7-1 pattern, γ_T , @2.125 Gbps ^{1,5}
Total jitter	TJ			0.43	UI	2^7-1 pattern, TP2, @1.25 Gbps ^{1,5}
Relative intensity noise (OMA)	RIN_{12} OMA		-125	-117	dB/Hz	2 GHz, 12 dB reflection
Receiver						
Wavelength	λ	770	850	860	nm	
Maximum input power	P_m	0			dBm	
Sensitivity (OMA)	S_1		12	31	μ W _{p-p}	1 Gbps operation, maximum is equivalent to -17 dBm @9 dB ER 2 Gbps operation
	S_2		16	49	μ W _{p-p}	
Stressed sensitivity (OMA) $S_{S1.06}$	ISI = 0.96 dB	55			μ W _{p-p}	1.0625 G operation
	ISI = 2.18 dB	67			μ W _{p-p}	1.0625 G operation
Stressed sensitivity (OMA) $S_{S1.25}$	ISI = 2.2 dB	69			μ W _{p-p}	1.25 G operation
	ISI = 2.6 dB	87			μ W _{p-p}	1.25 G operation
Stressed sensitivity (OMA) $S_{S2.12}$	ISI = 1.26 dB	96			μ W _{p-p}	2.125 G operation
	ISI = 2.03 dB	109			μ W _{p-p}	2.125 G operation
Loss of signal assert/deassert level	LOSD		-21	-17	dBm	Chatter-free operation
	LOSA	-30			dBm	
Low frequency cutoff	F_c		0.2	0.3	MHz	-3 dB, $P < -16$ dBm

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2.6 Link Length

Data Rate / Standard	Fiber Type	Modal Bandwidth @850 nm (MHz*km)	Distance Range (m)	Notes
1.0625 GBd	62.5/125 μ m MMF	200	.5 to 300	6
Fibre Channel	50/125 μ m MMF	500	.5 to 500	6
100-M5-SN-I	50/125 μ m MMF	900	.5 to 630	6
100-M6-SN-I	50/125 μ m MMF	1500	.5 to 755	6
	50/125 μ m MMF	2000	.5 to 860	6
1.25 Gbps	62.5/125 μ m MMF	200	.5 to 275	6
IEEE 802.3	50/125 μ m MMF	500	.5 to 550	6
1000Base-SX	50/125 μ m MMF	900	.5 to 595	6
	50/125 μ m MMF	1500	.5 to 740	6
	50/125 μ m MMF	2000	.5 to 860	6
2.125 GBd	62.5/125 μ m MMF	200	.5 to 150	6
Fibre Channel	50/125 μ m MMF	500	.5 to 300	6
200-M5-SN-I,	50/125 μ m MMF	900	.5 to 350	6
200-M6-SN-I	50/125 μ m MMF	1500	.5 to 430	6
	50/125 μ m MMF	2000	.5 to 500	6

Specification notes:

1. UI (Unit Interval): one UI is equal to one bit time. For example, 2.125 Gbps corresponds to a UI of 470.588ps.
2. For LOSA and LOSD definitions see Loss of Signal Assert/Deassert Level in Optical Characteristics.
3. When operating the transceiver at 1.0 – 1.3 GBd only, a slower input rise and fall time is acceptable. If it is planned to operate the module in the 1.0 – 2.12 GBd range, faster input rise and fall times are required.
4. Measured with stressed eye pattern as per FC-PI (Fibre Channel) and 1000BASE-SX using the worst-case specifications.
5. All jitter measurements performed with worst case input jitter according to FC-PI and 1000BASE-SX.
6. Distances, shown in the Link Length table, are the distances specified in the Fibre Channel and Ethernet standards. Link length distances are calculated for worst-case fiber and transceiver characteristics based on the optical and electrical specifications shown in this document using techniques utilized in IEEE 802.3 (Gigabit Ethernet). In the nominal case, longer distances are achievable.

2.7 Regulatory Compliance

The PLRXPL-VI-S24-22 complies with international electromagnetic compatibility (EMC) and international safety requirements and standards (see details in Table 2 below). EMC performance is dependent on the overall system design. Information included herein is intended as a figure of merit for designers to use as a basis for design decisions.

The PLRXPL-VI-S24-22 is lead free and RoHS compliant per Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Table 2. Regulatory Compliance

Feature	Test Method	Performance
Component safety	UL 60950 UL94-V0 IEC 60950	UL File E209897 TUV Report/Certificate (CB scheme)
Lead-free and RoHS-compliant	Directive 2002/95/EC	Compliant per the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.
Laser eye safety	U.S. 21CFR (J) 1040.10 EN 60825	CDRH compliant and Class 1 laser safety.
Electromagnetic Compatibility (EMC)		
CE	EU Declaration of Conformity	Compliant with European EMC and Safety Standards.
Electromagnetic emissions	EMC Directive 89/336/EEC FCC CFR47 Part 15 IEC/CISPR 22 AS/NZS CISPR22 EN 55022 ICES-003, Issue 4 VCCI-03	Noise frequency range: 30 MHz to 12 GHz. Good system EMC design practice required to achieve Class B margins.
Electromagnetic immunity	EMC Directive 89/336/EEC IEC /CISPR/24 EN 55024	
ESD immunity	EN 61000-4-2	Exceeds requirements. Withstands discharges of: 8 kV contact, 15 kV and 25 kV air.
Radiated immunity	EN 61000-4-3	Exceeds requirements. Field strength of 10 V/m RMS, from 10 MHz to 1 GHz. No effect on transceiver performance is detectable between these limits.

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2.8 PCB Layout

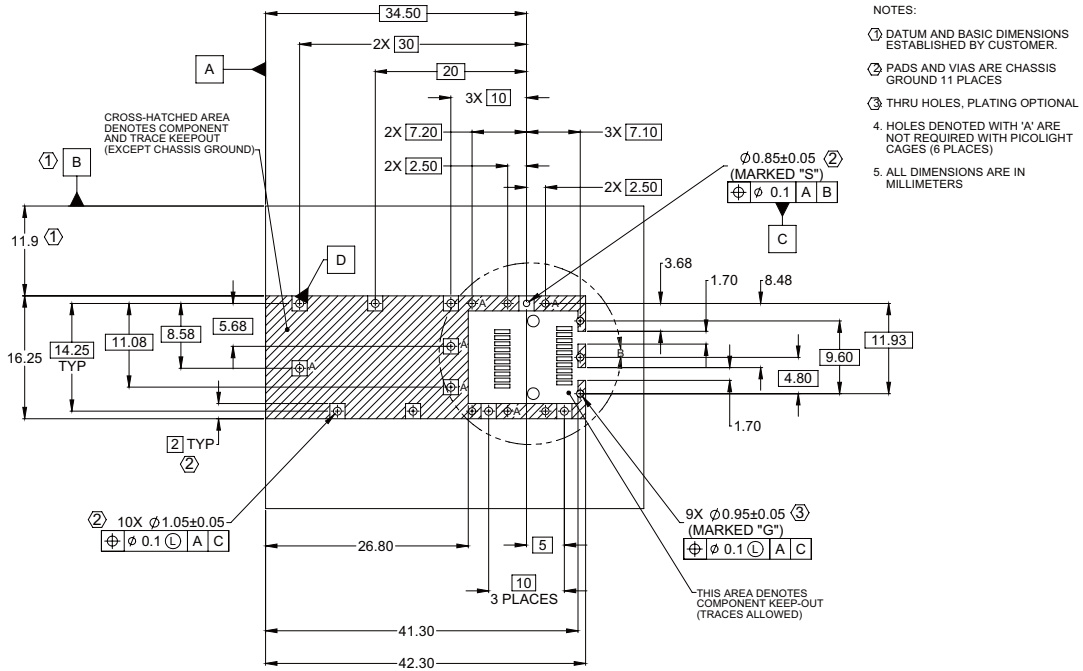


Figure 4. Board layout

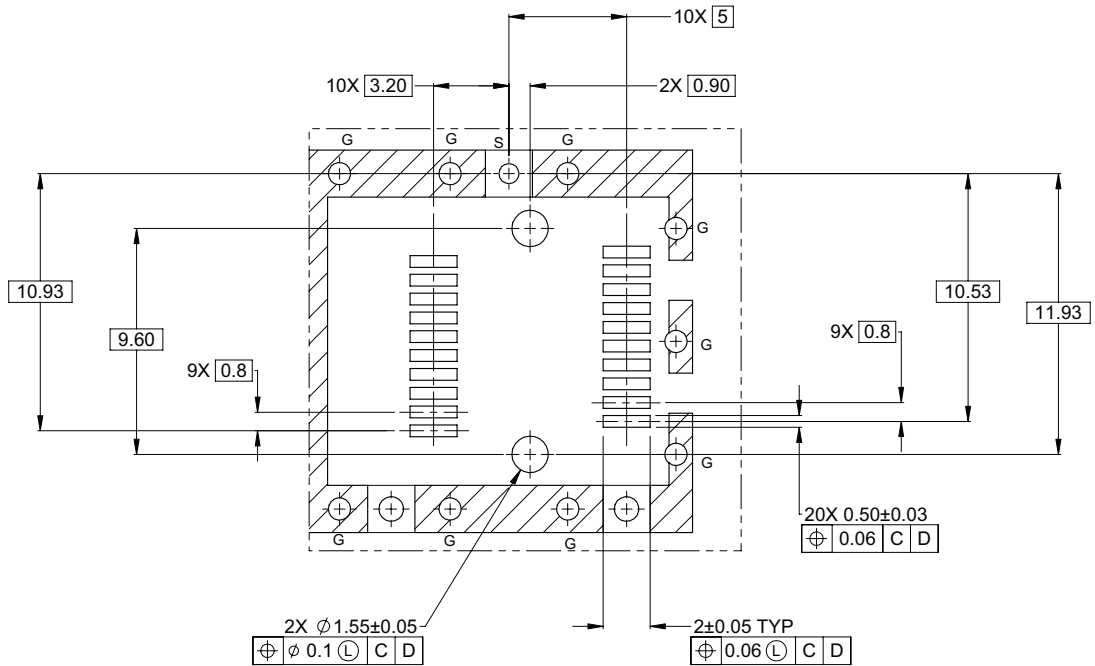


Figure 5. Detail layout

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2.9 Front Panel Opening

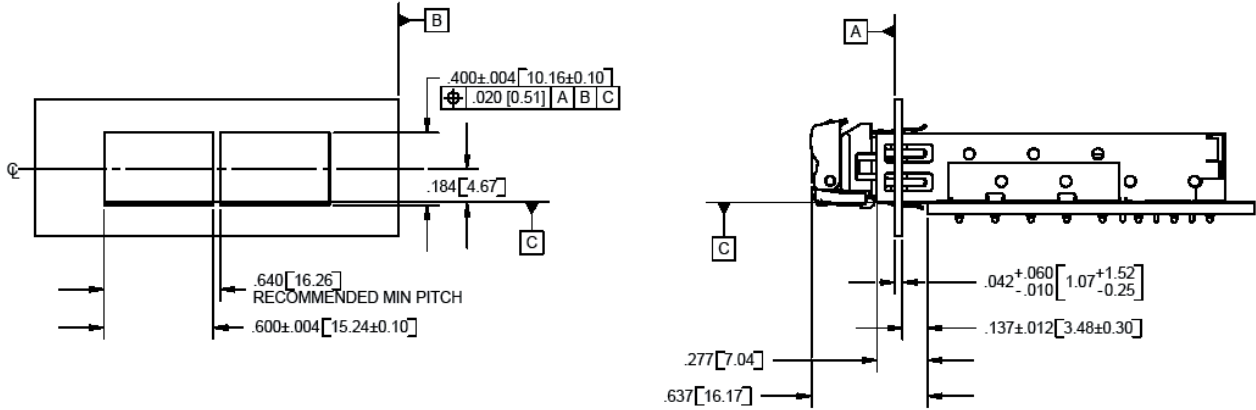
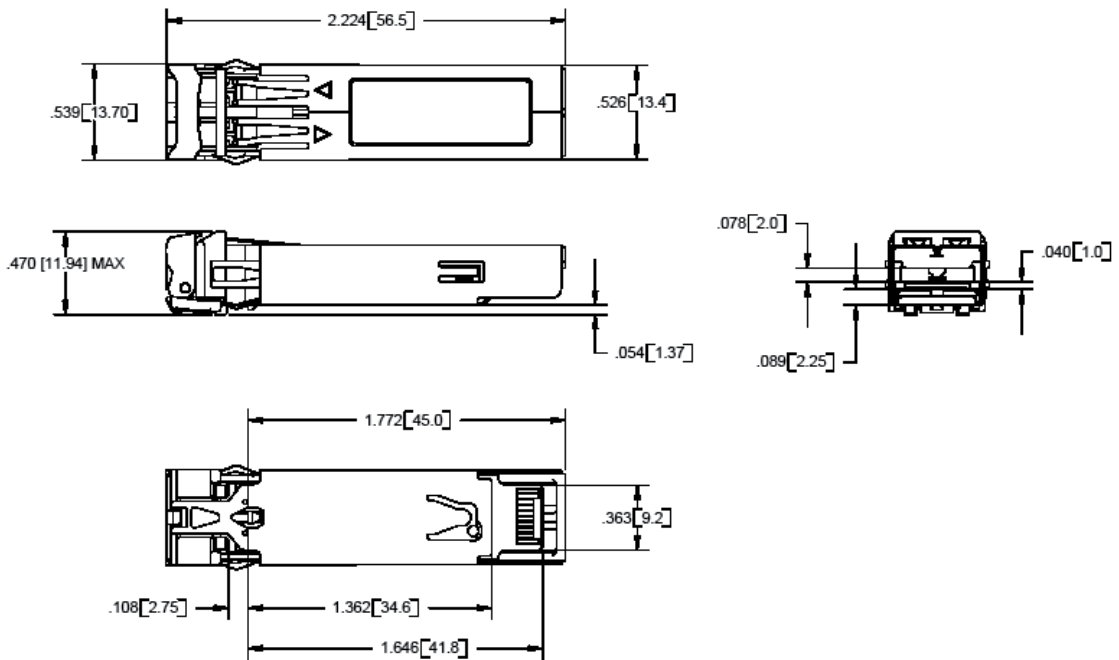


Figure 6. Front panel detail

2.10 Module Outline



All dimensions in inches [mm]

Figure 7. Module detail

2.11 Transceiver Belly-to-Belly Mounting

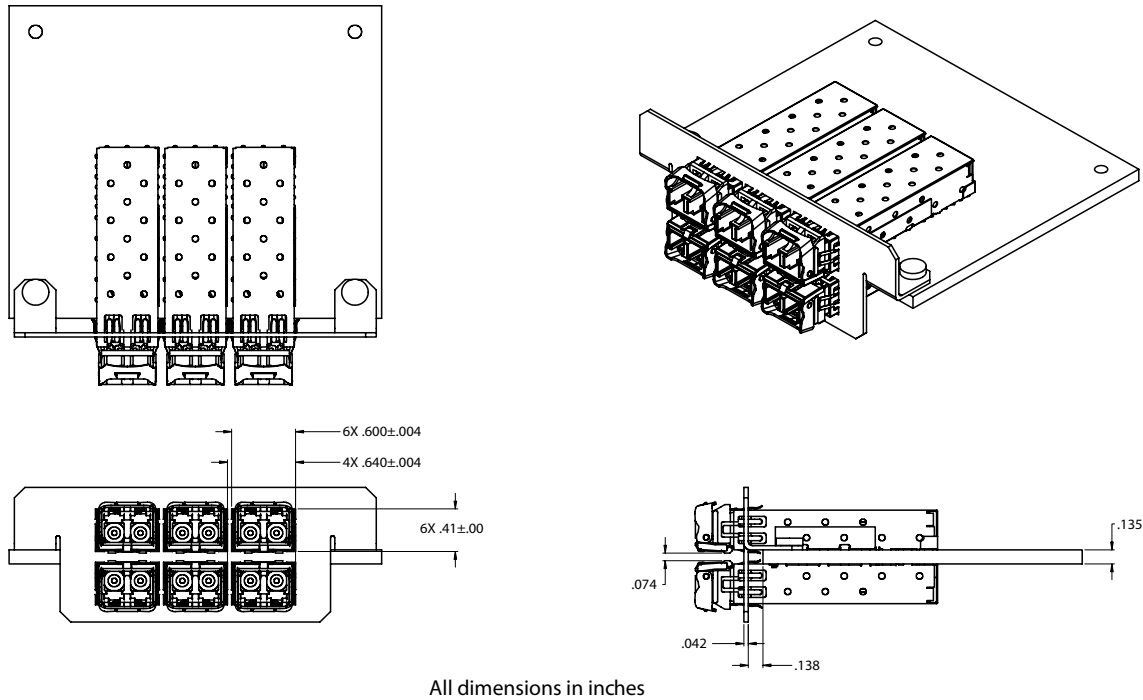


Figure 8. Mounting detail

Section 3 Related Information

Other information related to transceiver includes:

- Section 3.1 Digital Diagnostic Monitoring and Serial ID Operation
- Section 3.2 Package and Handling Instructions
- Section 3.3 Electrostatic Discharge (ESD)
- Section 3.4 Eye Safety

3.1 Digital Diagnostic Monitoring and Serial ID Operation

The PLRXPL-VI-S24-22 is equipped with a 2-wire serial EEPROM that is used to store specific information about the type/identification of the transceiver as well as real-time digitized information relating to the transceiver's performance. See Section IV, "Module Definition Interface and Data Field Description" of the SFP-MSA Pin Definitions and Host Board Layout document for memory/address organization of the identification data and the Small Form Factor Committee's document number SFF-8472 Rev 9.5, dated June 1, 2004 for memory/address organization of the digital diagnostic data.

The enhanced digital diagnostics feature monitors five key transceiver parameters which are internally calibrated and should be read as absolute values and interpreted as follows:

Transceiver temperature in degrees Celsius: internally measured. Represented as a 16-bit signed two's complement value in increments of $1/256^{\circ}\text{C}$ from -40 to $+125^{\circ}\text{C}$ with LSB equal to $1/256^{\circ}\text{C}$. Accuracy is $\pm 3^{\circ}\text{C}$ over the specified operating temperature and voltage range.

Vcc/supply voltage in volts: internally measured. Represented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value (0-65535) with LSB equal to $100\ \mu\text{V}$ with a measurement range of 0 to $+6.55\ \text{V}$. Accuracy is $\pm 3\%$ of nominal value over the specified operating temperature and voltage ranges.

TX bias current in μA : represented as a 16-bit unsigned integer with current defined as the full 16-bit value (0-65535) with LSB equal to $2\ \mu\text{A}$ with a measurement range of 0 – 131 mA. Accuracy is $\pm 10\%$ of nominal value over the specified operating temperature and voltage ranges.

TX output power in mW: represented as a 16-bit unsigned integer with the power defined as the full 16-bit value (0-65535) with LSB equal to $0.1\ \mu\text{W}$. Accuracy is $\pm 2\ \text{dB}$ over the specified temperature and voltage ranges over the range of $100\ \mu\text{W}$ to $800\ \mu\text{W}$ ($-10\ \text{dBm}$ to $-1\ \text{dBm}$). Data is not valid when transmitter is disabled.

RX received optical power in mW: represented as average power as a 16-bit unsigned integer with the power defined as the full 16-bit value (0-65535) with LSB equal to $0.1\ \mu\text{W}$. Accuracy over the specified temperature and voltage ranges is $\pm 3\ \text{dB}$ from $30\ \mu\text{W}$ to $1000\ \mu\text{W}$ ($-15\ \text{dBm}$ to $0\ \text{dBm}$).

Reading the Data

The information is accessed through the MOD_DEF(1), and MOD_DEF(2) connector pins of the module. The specification for this EEPROM (ATMEL AT-24CO1A family) contains all the timing and addressing information required for accessing the data.

The device address used to read the Serial ID data is $1010000\text{X}(\text{A0h})$, and the address to read the diagnostic data is $1010001\text{X}(\text{A2h})$. Any other device addresses will be ignored. Refer to Table 3, Table 4, and Table 5 for information regarding addresses and data field descriptions.

MOD_DEF(0), pin 6 on the transceiver, is connected to Logic 0 (ground) on the transceiver.

MOD_DEF(1), pin 5 on the transceiver, is connected to the SCL pin of the EEPROM.

MOD_DEF(2), pin 4 on the transceiver, is connected to the SDA pin of the EEPROM.

The EEPROM WP pin is internally tied to ground with no external access, allowing write access to the customer-writable field (bytes 128-247 of address 1010001X). Note: address bytes 0-127 are not write protected and may cause diagnostic malfunctions if written over.

Decoding the Data

The information stored in the EEPROM including organization is defined in the SFP-MSA Pin Definitions and Host Board Layout document, dated 3/13/00, Section IV. The digital diagnostic information stored in the EEPROM is defined in the SFP document SFF-8472 draft rev 9.5, dated June 1, 2004.

Table 3. Data Field Descriptions

Address(1010000X)(A0h)		Address(1010001X)(A2h)	
0	Serial ID information; defined by SFP MSA	0	Alarm and warning limits
95		55	Reserved for external calibration constants
127		95	Real-time diagnostic information
	JDSU-specific information	119	JDSU-specific information
	Reserved for SFP MSA	127	Non-volatile, customer- writeable, fieldwriteable area
		247	
255		JDSU-specific information	
		255	

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Table 4. Serial ID Data and Map

Memory Address	Value	Comments
Address (1010000X)(A0h)		
0	03	SFP transceiver
1	04	SFP with serial ID
2	07	LC connector
3–10	0000000120400C05	850 nm, multimode, 1.062/2.125 FC, intermediate distance and 1000Base-SX
11	01	8B10B encoding mechanism
12	15	Nominal bit rate of 2.125 Gbps
13	00	Reserved
14	00	Single mode fiber not supported
15	00	Single mode fiber not supported
16	1E	300 meters of 50/125 μm fiber
17	0F	150 meters of 62.5/125 μm fiber
18	00	Copper not supported
19	00	Reserved
20–35	JDSU	Vendor name (ASCII)
36	00	Reserved
37–39	00019C	IEEE company ID (ASCII)
40–55	PLRXPL-VI-S24-22	Part number (ASCII, no hyphens included)
56–59		Rev of part number (ASCII)
60–61	0352	Wavelength of laser in nm; 850
62		Reserved
63		Check code; lower 8 bits of sum from byte 0 through 62
64	00	Reserved
65	1A	No Rate Select, Tx_Disable, Tx Fault, Loss of Signal implemented
66	00	Bit rate max of 2.2Gbps
67	00	Bit rate min of 1.0 Gbps
68–83		Serial number (ASCII)
84–91		Date code (ASCII)
92	68	Diagnostics monitoring type
93	F0	Digital diagnostics
94	2	Compliance SFF-8472 Rev 9.4
95		Check code; lower 8 bits of sum from byte 64 through 94

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Table 5. Diagnostics Data Map

Memory Address	Value	Comments
Address (1010001X)(A2h)		
00-01	Temp high alarm	MSB at low address
02-03	Temp low alarm	MSB at low address
04-05	Temp high warning	MSB at low address
06-07	Temp low warning	MSB at low address
08-09	Voltage high alarm	MSB at low address
10-11	Voltage low alarm	MSB at low address
12-13	Voltage high warning	MSB at low address
14-15	Voltage low warning	MSB at low address
16-17	Bias high alarm	MSB at low address
18-19	Bias low alarm	MSB at low address
20-21	Bias high warning	MSB at low address
22-23	Bias low warning	MSB at low address
24-25	TX power high alarm	MSB at low address
26-27	TX power low alarm	MSB at low address
28-29	TX power high warning	MSB at low address
30-31	Tx power Low warning	MSB at low address
32-33	RX power high alarm	MSB at low address
34-35	RX power low alarm	MSB at low address
36-37	RX power high warning	MSB at low address
38-39	RX power low warning	MSB at low address
40-55	Reserved	For future monitoring quantities
56-59	RP4	External calibration constant
60-63	RP3	External calibration constant
64-67	RP2	External calibration constant
68-71	RP1	External calibration constant
72-75	RP0	External calibration constant
76-77	Islope	External calibration constant
78-79	Ioffset	External calibration constant
80-81	TPslope	External calibration constant
82-83	TPoffset	External calibration constant
84-85	Tslope	External calibration constant
86-87	Toffset	External calibration constant
88-89	Vslope	External calibration constant
90-91	External calibration constant	Refer to SFF-8472 rev 9.5
92-94	Reserved	Reserved
95	Checksum	Low order 8 bits of sum from 0-94
96	Temperature MSB	Internal temperature AD values
97	Temperature LSB	
98	Vcc MSB	Internally measured supply voltage AD values
99	Vcc LSB	
100	TX bias MSB	TX bias current AD values

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Table 5. Diagnostics Data Map

(continued)

Memory Address	Value	Comments
Address (1010001X)(A2h)		
101	TX bias LSB	
102	TX power MSB	Measured TX output power AD values
103	TX power LSB	
104	RX power MSB	Measured RX input power AD values
105	RX power LSB	
106	Reserved MSB	For 1st future definition of digitized analog input
107	Reserved LSB	
108	Reserved MSB	For 2nd future definition of digitized analog input
109	Reserved LSB	
110-7	Tx disable state	Digital state of Tx disable pin
110-6	Soft Tx disable control	Writing 1 disables laser, this is OR'd with Tx_Disable pin
110-5	Reserved	
110-4	Rate select state	
110-3	Soft rate select control	
110-2	Tx fault state	Digital state
110-1	LOS state	Digital state
110-0	Data ready state	Digital state; 1 until transceiver is ready
111	Reserved	Reserved
112-119	Optional alarm and warning flag bits	Refer to SFF-8472 rev 9.5
120-127	Vendor specific	Vendor specific
128-247	User/customer EEPROM	Field writeable EEPROM
248-255	Vendor specific	Vendor specific

3.2 Package and Handling Instructions

Process Plug

The PLRXPL-VI-S24-22 is supplied with a dust cover. This plug protects the transceiver's optics during standard manufacturing processes by preventing contamination from air borne particles.

Note: it is recommended that the dust cover remain in the transceiver whenever an optical fiber connector is not inserted.

Recommended Cleaning and De-greasing Chemicals

JDSU recommends the use of methyl, isopropyl, and isobutyl alcohols for cleaning.

Do not use halogenated hydrocarbons (for example, trichloroethane, ketones such as acetone, chloroform, ethyl acetate, MEK, methylene chloride, methylene dichloride, phenol, N-methylpyrrolidone).

Flammability

The PLRXPL-VI-S24-22 housing is made of cast zinc and sheet metal.

3.3 Electrostatic Discharge (ESD)

Handling

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD-protected environment utilizing standard grounded benches, floor mats, and wrist straps.

Test and Operation

In most applications, the optical connector will protrude through the system chassis and be subjected to the same ESD environment as the system. Once properly installed in the system, this transceiver should meet and exceed common ESD testing practices and fulfill system ESD requirements.

Typical of optical transceivers, this module's receiver contains a highly sensitive optical detector and amplifier which may become temporarily saturated during an ESD strike. This could result in a short burst of bit errors. Such an event might require that the application re-acquire synchronization at the higher layers (for example, a serializer/deserializer chip).

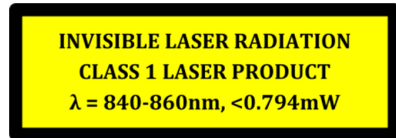
3.4 Eye Safety

The PLRXPL-VI-S24-22 is an international Class 1 laser product per IEC 825, and per CDRH, 21 CFR 1040 Laser Safety Requirements. The PLRXPL-VI-S24-22 is an eye safe device when operated within the limits of this specification.

Operating this product in a manner inconsistent with intended usage and specification may result in hazardous radiation exposure.

Laser Safety

The transceiver is certified as a Class 1 laser product per international standard IEC 60825-1:2007 2nd edition and is considered non-hazardous when operated within the limits of this specification.


Caution

Operating this product in a manner inconsistent with intended usage and specifications may result in hazardous radiation exposure. Use of controls or adjustments or performance of procedures other than these specified in this product datasheet may result in hazardous radiation exposure. Tampering with this laser product or operating this product outside the limits of this specification may be considered an 'act of manufacturing' and may require recertification of the modified product.

This device complies with 21 CFR 1040.10 except for deviations pursuant to Laser Notice No. 50 dated June 24, 2007.

Ordering Information

For more information on this or other products and their availability, please contact your local JDSU account manager or JDSU directly at 1-800-498-JDSU (5378) in North America and +800-5378-JDSU worldwide or via e-mail at customer.service@jdsu.com.

Sample: PLRXPL-VI-S24-22

Part Number	Temp. Range	Power Supply Tolerance	Dual Rate Fiber Channel	1000Base-SX	Digital Diagnostics	PCI Compliant
PLRXPL-VI-S24-22	-40 to 85°C	±10%	X	X	X	X

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