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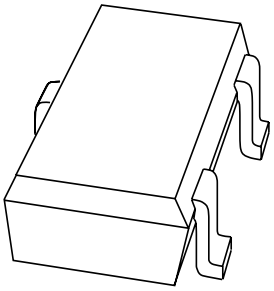
DATA SHEET



PMST3904
NPN switching transistor

Product data sheet
Supersedes data of 1999 Apr 22

2004 Jan 21

NPN switching transistor PMST3904

FEATURES

- Collector current capability I_C = 200 mA
- Collector-emitter voltage V_{CEO} = 40 V.

APPLICATIONS

- General amplification and switching.

DESCRIPTION

NPN switching transistor in a SOT323 plastic package.
PNP complement: PMST3906.

MARKING

TYPE NUMBER	MARKING CODE(1)
PMST3904	∗1A

Note

1. ∗ = p: Made in Hong Kong.
   ∗ = t: Made in Malaysia.
   ∗ = W: Made in China.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	40	V
I_C	collector current (DC)	200	mA

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector

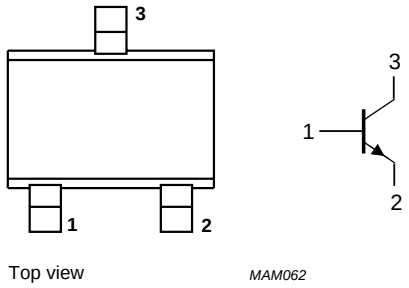


Fig.1 Simplified outline (SOT323) and symbol.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PMST3904	–	plastic surface mounted package; 3 leads	SOT323

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	40	V
V_{EBO}	emitter-base voltage	open collector	–	6	V
I_C	collector current (DC)		–	200	mA
I_{CM}	peak collector current		–	200	mA
I_{BM}	peak base current		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	200	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		−65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1	625	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

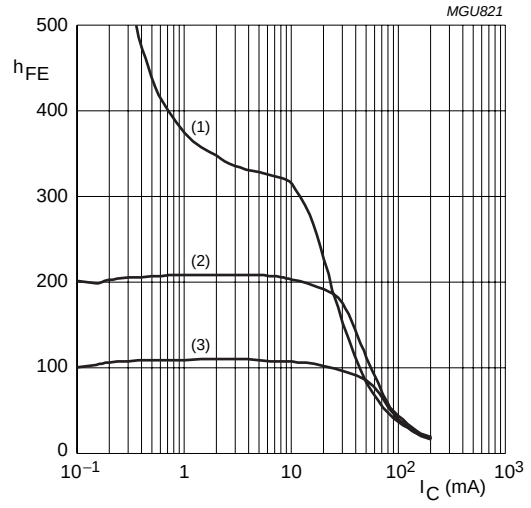
CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	I_E = 0; V_{CB} = 30 V	–	50	nA
I_{EBO}	emitter cut-off current	I_C = 0; V_{EB} = 6 V	–	50	nA
h_{FE}	DC current gain	V_{CE} = 1 V; see Fig.2; note 1			
		I_C = 0.1 mA	60	–	
		I_C = 1 mA	80	–	
		I_C = 10 mA	100	300	
		I_C = 50 mA	60	–	
		I_C = 100 mA	30	–	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 1 mA	–	200	mV
		I_C = 50 mA; I_B = 5 mA	–	300	mV
V_{BEsat}	base-emitter saturation voltage	I_C = 10 mA; I_B = 1 mA	650	850	mV
		I_C = 50 mA; I_B = 5 mA	–	950	mV
C_c	collector capacitance	$I_E = I_e$ = 0; V_{CB} = 5 V; f = 1 MHz	–	4	pF
C_e	emitter capacitance	$I_C = I_c$ = 0; V_{BE} = 500 mV; f = 1 MHz	–	8	pF
f_T	transition frequency	I_C = 10 mA; V_{CE} = 20 V; f = 100 MHz	300	–	MHz
F	noise figure	I_C = 100 μA; V_{CE} = 5 V; R_S = 1 kΩ; f = 10 Hz to 15.7 kHz	–	5	dB
Switching times (between 10% and 90% levels); see Fig.7					
t_d	delay time	I_{Con} = 10 mA; I_{Bon} = 1 mA; I_{Boff} = −1 mA	–	35	ns
t_r	rise time		–	35	ns
t_s	storage time		–	200	ns
t_f	fall time		–	50	ns

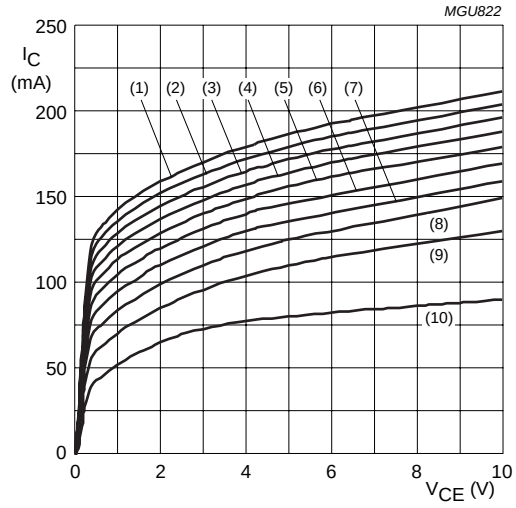
Note

1. Pulse test: $t_p \leq 300$ μs; $\delta \leq 0.02$.



V_{CE} = 1 V.
(1) T_{amb} = 150 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = −55 °C.

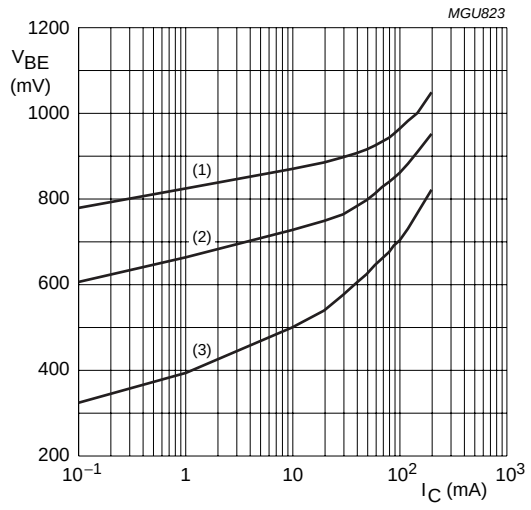
Fig.2 DC current gain; typical values.



T_{amb} = 25 °C.

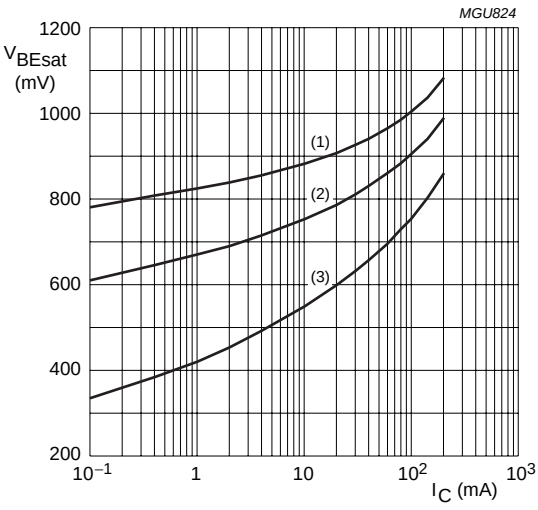
(1) I_B = 5 mA.
(2) I_B = 4.5 mA.
(3) I_B = 4 mA.
(4) I_B = 3.5 mA.
(5) I_B = 3 mA.
(6) I_B = 2.5 mA.
(7) I_B = 2 mA.
(8) I_B = 1.5 mA.
(9) I_B = 1 mA.
(10) I_B = 0.5 mA.

Fig.3 Collector current as a function of collector-emitter voltage.



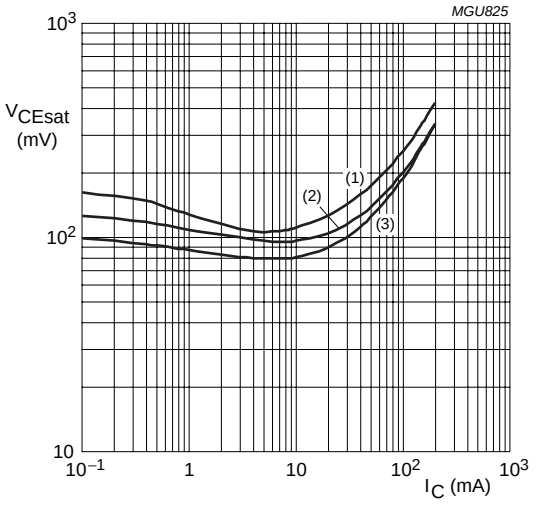
V_{CE} = 1 V.
(1) T_{amb} = −55 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = 150 °C.

Fig.4 Base-emitter voltage as a function of collector current.



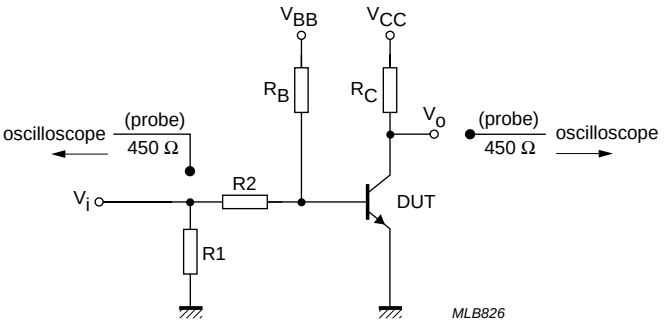
I_C/I_B = 10.
(1) T_{amb} = −55 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = 150 °C.

Fig.5 Base-emitter saturation voltage as a function of collector current.



$I_C/I_B = 10$.
(1) $T_{amb} = 150$ °C.
(2) $T_{amb} = 25$ °C.
(3) $T_{amb} = -55$ °C.

Fig.6 Collector-emitter saturation voltage as a function of collector current.

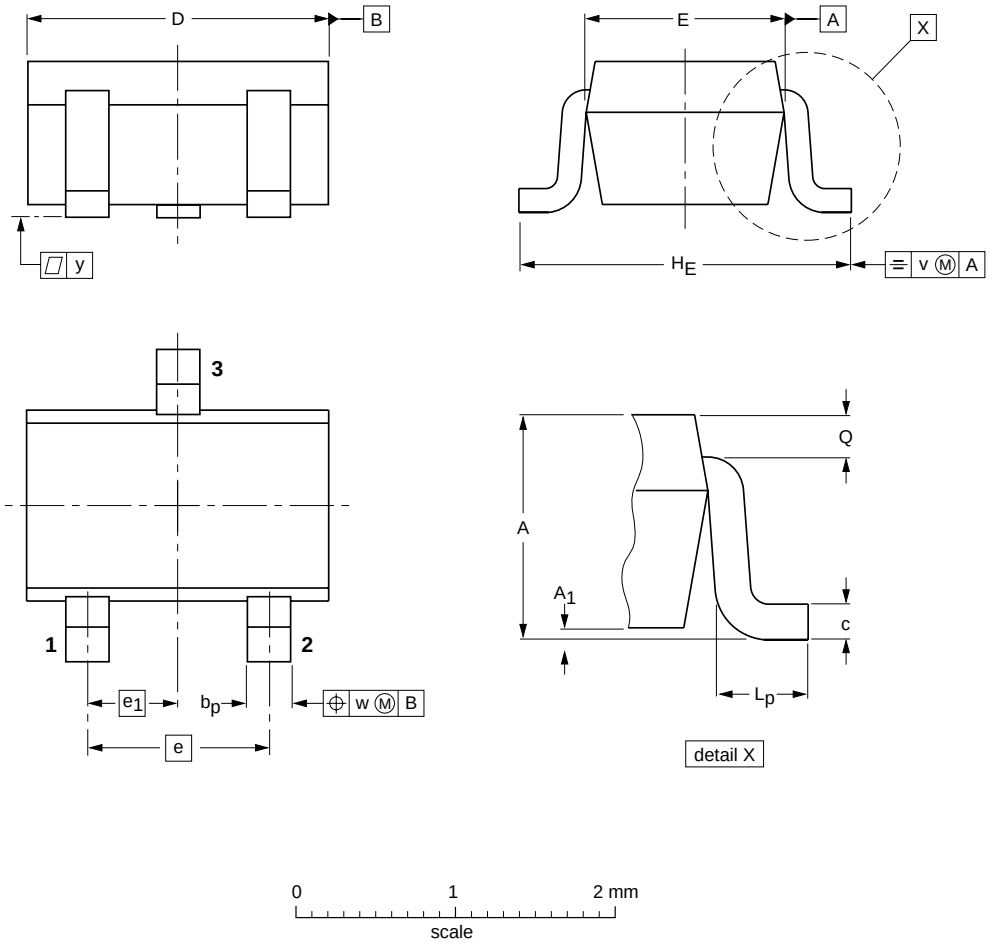


$V_i = 5$ V; T = 500 μs; $t_p = 10$ μs; $t_r = t_f \leq 3$ ns.
R1 = 56 Ω; R2 = 2.5 kΩ; $R_B = 3.9$ kΩ; $R_C = 270$ Ω.
$V_{BB} = -1.9$ V; $V_{CC} = 3$ V.
Oscilloscope: input impedance $Z_i = 50$ Ω.

Fig.7 Test circuit for switching times.

PACKAGE OUTLINE

Plastic surface-mounted package; 3 leads **SOT323**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT323			SC-70			~~04-11-04~~ 06-03-16

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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NXP Semiconductors

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This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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