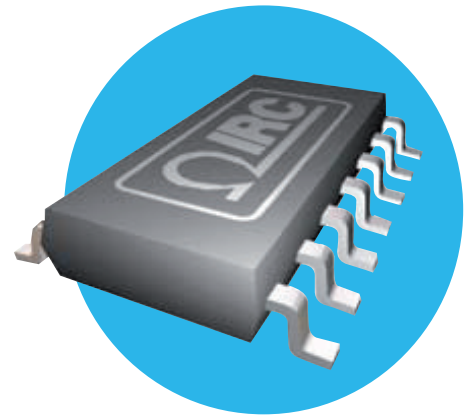


## Surface Mount SOIC Resistor Networks

### SOIC Series

- Tested for COTS applications
- Both narrow and wide body versions available
- Standard JEDEC 8, 14, 16, and 20 pin packages
- Ultra-stable TaNSil® resistors on silicon substrates
- Standard Sn/Pb and Pb-free terminations available



 All Pb-free parts comply with EU Directive 2011/65/EU (RoHS2)

IRC's TaNSil® SOIC resistor networks are the perfect solution for high volume applications that demand a small wiring board footprint. The .050" lead spacing provides higher lead density, increased component count, lower resistor cost, and high reliability.

The tantalum nitride film system on silicon provides precision tolerance, exceptional TCR tracking, low cost and miniature package. Excellent performance in harsh, humid environments is a trademark of IRC's self-passivating TaNSil® resistor film.

The SOIC series is ideally suited for the latest surface mount assembly techniques and each lead can be 100% visually inspected. The compliant gull wing leads relieve thermal expansion and contraction stresses created by soldering and temperature excursions.

For applications requiring high performance resistor networks in a low cost, surface mount package, specify IRC SOIC resistor networks.

### Electrical Data

Resistance Range	10R to 250K
Absolute Tolerance	To ±0.1%
Ratio Tolerance to R1	To ±0.05%
Absolute TCR	To ±25ppm/°C
Tracking TCR	To ±5ppm/°C
Element Power Rating @ 70°C Isolated Schematic Bussed Schematic	100mW 50mW
Power Rating @ 70°C SOIC-N Package	8-Pin 400mW 14-Pin 700mW 16-Pin 800mW
Power Rating @ 70°C SOIC-W Package	16-Pin 1.2W 20-Pin 1.5W
Rated Operating Voltage (not to exceed $\sqrt{\text{Power} \times \text{Resistance}}$ )	100 Volts
Operating Temperature	-55°C to +125°C
Noise	<-30dB

### Environmental Data

Test Per MIL-PRF-83401	Typical Delta R	Max Delta R
Thermal Shock	±0.02%	±0.1%
Power Conditioning	±0.03%	±0.1%
High Temperature Exposure	±0.03%	±0.05%
Short-time Overload	±0.02%	±0.05%
Low Temperature Storage	±0.03%	±0.05%
Life	±0.05%	±0.1%

#### General Note

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SOIC Series

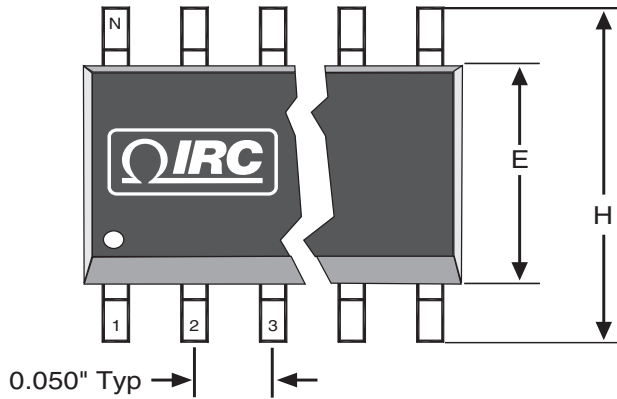
## Manufacturing Capability Data

Absolute TCR (ppm/°C)	ISOLATED SCHEMATIC A				BUSSED SCHEMATIC B			
	Ohmic Range (Ω)	Available Tolerances	Available Ratio Tolerances	Best Tracking (±ppm/°C)	Ohmic Range (Ω)	Available Tolerances	Available Ratio Tolerances	Best Tracking (±ppm/°C)
250	10-25	F G J	F G	50	10-25	F G J	F G	200
	26-50	D F G J	C D F G	10	26-50	F G J	D F G	100
	51-200	C D F G J	C D F G	5	51-100	D F G J	C D F G	50
	201-250K	B C D F G J	A B C D F G	5	101-200	D F G J	B C D F G	25
					201-500	B C D F G J	B C D F G	20
					501-100K	B C D F G J	A B C D F G	5
100	26-50	D F G J	C D F G	10	26-50	F G J	D F G	100
	51-200	C D F G J	C D F G	5	51-100	D F G J	C D F G	50
	201-250K	B C D F G J	A B F G	5	101-200	D F G J	B C D F G	25
					201-500	B C D F G J	B C D F G	20
					501-100K	B C D F G J	A B C D F G	5
50	26-50	D F G J	C D F G	10	51-100	D F G J	C D F G	50
	51-200	C D F G J	C D F G	5	101-200	D F G J	B C D F G	25
	201-250K	B C D F G J	A B F G	5	201-500	B C D F G J	B C D F G	20
					501-100K	B C D F G J	A B C D F G	5
25	51-200	C D F G J	C D F G	5	201-500	B C D F G J	B C D F G	20
	201-250K	B C D F G J	A B F G	5	501-100K	B C D F G J	A B C D F G	5

**General Note**

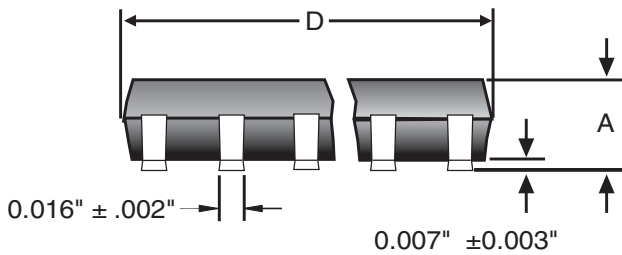
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## Physical and Schematic Data

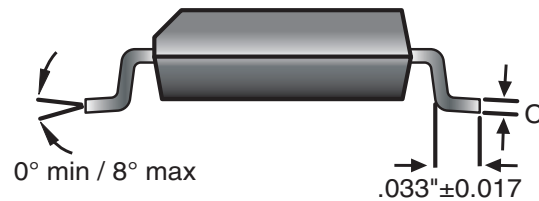


	SOIC-N			SOIC-W	
	8-Pin	14-Pin	16-Pin	16-Pin	20-Pin
D	0.193"±0.004 (4.902 ± 0.102)	0.341"±0.004 (8.661 ± 0.102)	0.390"±0.004 (9.906 ± 0.102)	0.402"±0.004 (10.211 ± 0.102)	0.502"±0.004 (12.751 ± 0.102)
H	0.236"±0.008 (5.994 ± 0.203)			0.406"±0.008 (10.312 ± 0.203)	
E	0.153"±0.004 (3.886 ± 0.102)			0.295"±0.004 (7.493 ± 0.102)	
A	0.064"±0.004 (1.626 ± 0.102)			0.100"±0.004 (2.540 ± 0.102)	
C	0.0075" - 0.010" (0.191 ± 0.254)			0.011"±0.002 (0.279 ± 0.051)	

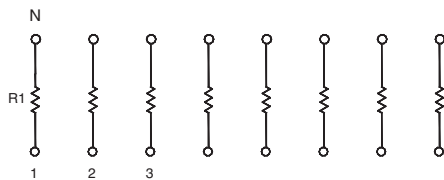
Note: N = number of pins (8, 14, 16)



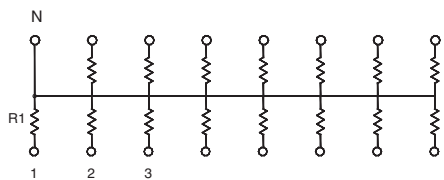
Note: All dimensions exclude mold flash and end flash which shall not exceed 0.006" per side.



Note: Lead Coplanarity 0.004" Max.

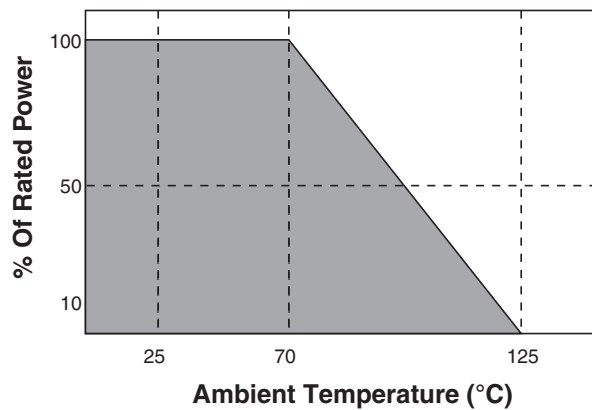


Schematic A  
Isolated



Schematic B  
Bussed

## Power Derating Curve



For additional information or to discuss your specific requirements, please contact our Applications Team using the contact details below.

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## Ordering Data

### Prefix

(Inclusion of Prefix is preferred but, historically, it may have been omitted.)

GUS - SS4A - 01 - 1002 - F B

### Style, Schematic and Termination

SS4A = 8-pin SOIC-N, 4 Isolated Resistors; Sn/Pb terminations  
 SS4ALF = 8-pin SOIC-N, 4 Isolated Resistors; 100% tin (Pb-free) terminations  
 SS4B = 8-pin SOIC-N, 7 Bussed Resistors; Sn/Pb terminations  
 SS4BLF = 8-pin SOIC-N, 7 Bussed Resistors; 100% tin (Pb-free) terminations

SS7A = 14-pin SOIC-N, 7 Isolated Resistors; Sn/Pb terminations  
 SS7ALF = 14-pin SOIC-N, 7 Isolated Resistors; 100% tin (Pb-free) terminations  
 SS7B = 14-pin SOIC-N, 13 Bussed Resistors; Sn/Pb terminations  
 SS7BLF = 14-pin SOIC-N, 13 Bussed Resistors; 100% tin (Pb-free) terminations

SS8A = 16-pin SOIC-N, 8 Isolated Resistors; Sn/Pb terminations  
 SS8ALF = 16-pin SOIC-N, 8 Isolated Resistors; 100% tin (Pb-free) terminations  
 SS8B = 16-pin SOIC-N, 15 Bussed Resistors; Sn/Pb terminations  
 SS8BLF = 16-pin SOIC-N, 15 Bussed Resistors; 100% tin (Pb-free) terminations

SL8A = 16-pin SOIC-W, 8 Isolated Resistors; Sn/Pb terminations  
 SL8ALF = 16-pin SOIC-W, 8 Isolated Resistors; 100% tin (Pb-free) terminations  
 SL8B = 16-pin SOIC-W, 15 Bussed Resistors; Sn/Pb terminations  
 SL8BLF = 16-pin SOIC-W, 15 Bussed Resistors; 100% tin (Pb-free) terminations

SL0A = 20-pin SOIC-W, 10 Isolated Resistors; Sn/Pb terminations  
 SL0ALF = 20-pin SOIC-W, 10 Isolated Resistors; 100% tin (Pb-free) terminations  
 SL0B = 20-pin SOIC-W, 19 Bussed Resistors; Sn/Pb terminations  
 SL0BLF = 20-pin SOIC-W, 19 Bussed Resistors; 100% tin (Pb-free) terminations

### Absolute TCR Code

00 =  $\pm 250$ ppm/ $^{\circ}$ C; 01 =  $\pm 100$ ppm/ $^{\circ}$ C  
 02 =  $\pm 50$ ppm/ $^{\circ}$ C; 03 =  $\pm 25$ ppm/ $^{\circ}$ C

### Resistance Code

4-Digit Resistance Code  
 Ex: 1002 = 10K $\Omega$ , 50R1 = 50.1 $\Omega$   
 (The USA style coding shown is preferred, but, historically, European style coding (e.g. 10K) may have been used.)

### Absolute Tolerance Code

J =  $\pm 5\%$ ; G =  $\pm 2\%$ ; F =  $\pm 1\%$ ; D =  $\pm 0.5\%$   
 C =  $\pm 0.25\%$ ; B =  $\pm 0.1\%$

### Optional Ratio Tolerance Code

G =  $\pm 2\%$ ; F =  $\pm 1\%$ ; D =  $\pm 0.5\%$ ;  
 C =  $\pm 0.25\%$ ; B =  $\pm 0.1\%$ ; A =  $\pm 0.05\%$

### Packaging

Specify tubes or tape & reel.  
 Tape and reel packaging is compliant with EIA-481-D: 8 mm through 200 mm Embossed Carrier Taping and 8 mm and 12 mm Punched Carrier Taping of Surface Mount Components for Automatic Handling.  
 Tube packaging drawing detail available upon request.

### General Note

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