

RoHS Compliant

Features

- High stability and high reliability
- 2.7 to 5.5V drive available
- Clipped sine wave or CMOS level output
- Low phase noise
- Disable Function (KT7050A)

Applications

- Femtocell, Stratum3
- SONET/ SDH/ Ethernet

How to Order

For Femtocell (Standard Spec.)

Freq. Temp. Chrst. : $\pm 0.1 \times 10^{-6} / -10^\circ\text{C}$ to 70°C

KT7050 A 20000 A G T 33 T xx
 ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨

For Stratum3 (Standard Spec.)

Freq. Temp. Chrst. : $\pm 0.28 \times 10^{-6} / -40^\circ\text{C}$ to 85°C

KT7050 A 20000 K A W 33 T xx
 ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨

① Series	⑥ Upper Operating Temp.
② Land Type	T +70°C
A 10Pads	W +85°C
B 4Pads	⑦ Supply Voltage
③ Output Frequency	33 3.3V
④ Freq. Temp. Chrst.	⑦ Voltage Control Function
A $+0.1 \times 10^{-6}$	T TCXO
K $\pm 0.28 \times 10^{-6}$	Other* VCTCXO
⑤ Lower Operating Temp.	* Customer Spec.
A -40°C	⑨ Option Code
G -10°C	
J 0°C	

Packaging (Tape & Reel 1000 pcs./ reel)

- Compliant to the GR1244-Core & GR253-Core
- Recommended in Microsemi's ZLAN-68 app. note for Stratum3 applications based on tests performed by Kyocera.

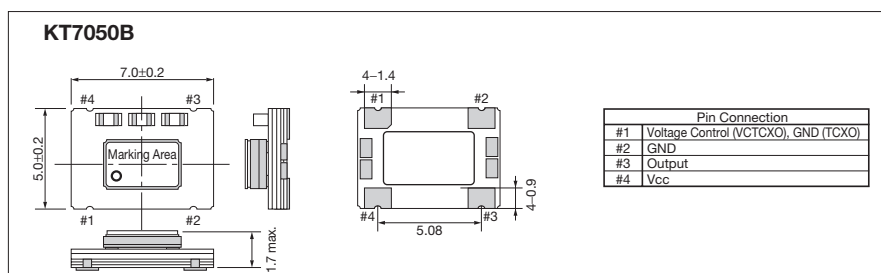
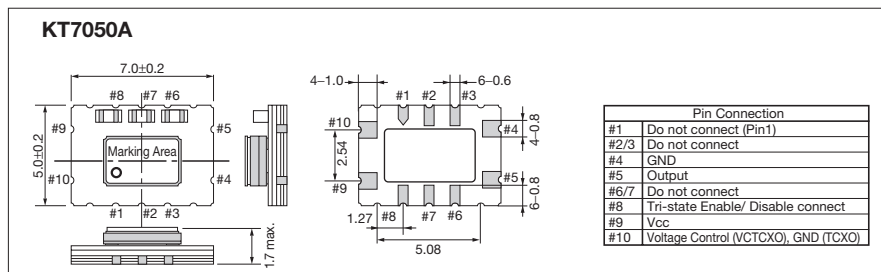
Specifications

Item	Symbol	Conditions	Min.	Max.	Units
Output Frequency Range	fo	Standard Frequency: 10, 19.2, 20, 24.576, 26, 30.72, 38.88, 40	10	40	MHz
Frequency Tolerance	f _{tol}	vs Temperature (-10 to +70°C) $[\pm(f_{\text{max}}-f_{\text{min}})/2f_0]$	-0.1	+0.1	$\times 10^{-6}$
		vs Temperature (-40 to +85°C) $[\pm(f_{\text{max}}-f_{\text{min}})/2f_0]$	-0.28	+0.28	
Supply Voltage	V _{CC}		+2.7	+5.5	V
Current Consumption	I _{CC}	CMOS output	—	6	mA
Frequency Aging	f _{age}	20years aging @40°C Including temp characteristics, initial tolerance, rated power supply voltage change and load change.	-4.6	+4.6	$\times 10^{-6}$
Voltage Control Range	f _{cont}	Positive *100k ohm min	± 5	± 20	$\times 10^{-6}$
Output Level	V _{pp}	Clipped Sine, Load: 10k ohm // 10pF	0.8	—	Vp-p
Low Level Output Voltage	V _{OL}	CMOS, Load: 15pF I _{OL} =4mA	—	10% V _{CC}	V
High Level Output Voltage	V _{OH}	CMOS, Load: 15pF I _{OH} =-4mA	90% V _{CC}	—	V
Rise / Fall Time (10% V _{CC} to 90% V _{CC})	tr/ tf	CMOS, Load: 15pF	—	8	ns
Symmetry	SYM	50% V _{CC}	45	55	%
Phase Noise @20MHz	—	- 90 (@10Hz offset) - 120 (@100Hz offset) - 140 (@1kHz offset) - 150 (@10kHz offset) - 150 (@100kHz offset)			dBc/ Hz

* Please contact us for other specifications.

Dimensions

(Unit: mm)



Recommended Land Pattern

(Unit: mm)

