19-3473; Rev 1; 8/11

-48V Hot-Swap Controllers with External RSENSE

General Description

The MAX5948A/MAX5948B are hot-swap controllers that allow a circuit card to be safely hot plugged into a live backplane. The MAX5948A/MAX5948B operate from -20V to -80V and are well-suited for -48V power systems. The MAX5948A is pin- and function-compatible with both the LT1640AL and LT1640L. The MAX5948B is pin- and function-compatible with both the LT1640AH and LT1640H.

The MAX5948A/MAX5948B provide a controlled turn-on to circuit cards preventing glitches on the power-supply rail and damage to board connectors and components. The MAX5948A/MAX5948B provide undervoltage, overvoltage, and overcurrent protection. These devices ensure the input voltage is stable and within tolerance before applying power to the load.

Both the MAX5948A and MAX5948B protect a system against overcurrent and short-circuit conditions by turning off the external MOSFET in the event of a fault condition.

Both devices feature an open-drain power-good status output, $\overline{PWRGD}$ for MAX5948A or PWRGD for MAX5948B, that can be used to enable downstream converters.

The MAX5948A/MAX5948B are available in an 8-pin SO package. Both devices are specified for the extended -40°C to +85°C temperature range.

Applications

Central-Office Switching

Network Switches/Routers

Server Line Cards

Base-Station Line Cards

Typical Operating Circuit appears at end of data sheet.

Features

- **Allow Safe Board Insertion and Removal from a Live -48V Backplane**
- **Pin- and Function-Compatible with LT1640AL/LT1640L (MAX5948A)**
- **Pin- and Function-Compatible with LT1640AH/LT1640H (MAX5948B)**
- **Withstand -100V Input Transients with No External Components**
- **Operate from -20V to -80V**
- **Programmable Inrush and Short-Circuit Current Limits**
- **Programmable Overvoltage Protection**
- **Programmable Undervoltage Lockout**
- **Power Up into a Shorted Load**
- **Power-Good Control Output**

Ordering Information

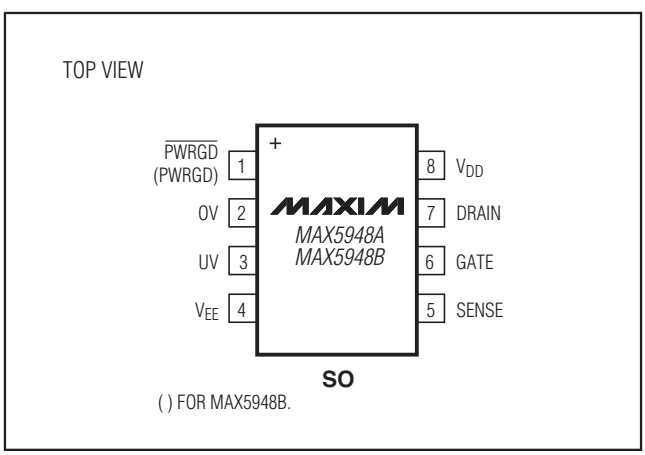
PART	TEMP RANGE	PIN-PACKAGE
MAX5948AESA+	-40°C to +85°C	8 SO
MAX5948BESA+	-40°C to +85°C	8 SO

+Denotes a lead(Pb)-free/RoHS-compliant package.

Selector Guide

PART	PWRGD POLARITY
MAX5948AESA	Active Low ($\overline{PWRGD}$)
MAX5948BESA	Active High (PWRGD)

Pin Configuration



-48V Hot-Swap Controllers with External RSENSE

ABSOLUTE MAXIMUM RATINGS

(All voltages are referenced to V_{EE}, unless otherwise noted.)
Supply Voltage (V_{DD} - V_{EE}) .....-0.3V to +100V
PWRGD, $\overline{PWRGD}$ .....-0.3V to +100V
DRAIN (Note 1).....-2V to +100V
SENSE .....-0.3V to +20V
GATE (internally clamped) .....-0.3V to +18V
UV and OV.....-0.3V to +60V
Current through SENSE .....±20mA
Current into GATE.....±300mA
Current into Any Other Pin.....±20mA
Current into Drain.....-100mA to +20mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.9mW/°C above +70°C).....471mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Test condition per Figure 1. DRAIN current must be limited to the specified 100mA maximum.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = 0V, V_{DD} = 48V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Operating Input Voltage Range	V_{DD}		20		80	V
Supply Current	I_{DD}	V_{UV} = 3V, OV = V_{EE}, SENSE = V_{EE}		0.7	2	mA
GATE DRIVER AND CLAMPING CIRCUITS						
Gate Pin Pullup Current	I_{PU}	GATE drive on, V_{GATE} = V_{EE}	-30	-45	-60	µA
Gate Pin Pulldown Current	I_{PD}	Any fault condition, V_{GATE} = 2V	24	50	70	mA
External Gate Drive	ΔV_{GATE}	V_{GATE} - V_{EE}, 20V ≤ V_{DD} ≤ 80V	10	13.5	18	V
GATE to V_{EE} Clamp Voltage	V_{GSCLMP}	V_{GATE} - V_{EE}, current into GATE = 30mA	15	16.4	18	V
CIRCUIT BREAKER						
Current-Limit Trip Voltage	V_{CB}	V_{CB} = V_{SENSE} - V_{EE}	40	50	60	mV
SENSE Input Bias Current	I_{SENSE}	V_{SENSE} = 50mV	0	-0.03	-1	µA
UV PIN						
UV High Threshold	V_{UVH}	UV low to high transition	1.213	1.243	1.272	V
UV Low Threshold	V_{UVL}	UV high to low transition	1.198	1.223	1.247	V
UV Hysteresis	V_{UVHY}			20		mV
UV Input Bias Current	I_{INUV}	V_{UV} = V_{EE}	0		-0.5	µA
OV PIN						
OV High Threshold	V_{OVH}	OV low to high transition	1.198	1.223	1.247	V
OV Low Threshold	V_{OVL}	OV high to low transition	1.165	1.203	1.232	V
OV Hysteresis	V_{OVHY}			20		mV
OV Input Bias Current	I_{INOV}	V_{OV} = V_{EE}	0		-0.5	µA
PWRGD OUTPUT SIGNAL REFERENCED TO DRAIN						
DRAIN Input Bias Current	I_{DRAIN}	V_{DRAIN} = 48V	10	80	250	µA
Power-Good Threshold	V_{PG}	V_{DRAIN} - V_{EE}, high to low transition	1.1	1.4	2.0	V
Power-Good Threshold Hysteresis	V_{PGHY}			0.4		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = 0V, V_{DD} = 48V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWRGD, $\overline{PWRGD}$ Output Leakage	I_{OH}	$V_{\overline{PWRGD}}$ (MAX5948A) = 80V, V_{DRAIN} = 48V, V_{PWRGD} (MAX5948B) = 80V, V_{DRAIN} = 0V			10	µA
Power-Good Output Impedance (PWRGD to DRAIN)	R_{OUT}	V_{PWRGD} (MAX5948B) (V_{DRAIN} - V_{EE}) < V_{PG}		500 x 10^3		MΩ
$\overline{PWRGD}$ Output Low Voltage	V_{OL}	$V_{\overline{PWRGD}}$ - V_{EE}; V_{DRAIN} - V_{EE} < V_{PG}, I_{OUT} = 1mA (MAX5948A)		0.11	0.4	V
PWRGD Output Low Voltage	V_{OL}	V_{PWRGD} - V_{DRAIN}; V_{DRAIN} = 5V, I_{OUT} = 1mA (MAX5948B)		0.11	0.4	V
AC PARAMETERS						
OV High to GATE Low	t_{PHLOV}	Figures 2, 3		0.5		µs
UV Low to GATE Low	t_{PHLUV}	Figures 2, 4		0.4		µs
OV Low to GATE High	t_{PLHOV}	Figures 2, 3		3.3		µs
UV High to GATE High	t_{PLHVL}	Figures 2, 4		3.4		µs
SENSE High to GATE Low	$t_{PHLSENSE}$	Figures 2, 5	2	3	4	µs
DRAIN Low to $\overline{PWRGD}$ Low DRAIN Low to (PWRGD - DRAIN) High	t_{PHLPG}	MAX5948A, Figures 2, 6		0.5		µs
		MAX5948B, Figures 2, 6		0.5		
DRAIN High to $\overline{PWRGD}$ High DRAIN High to (PWRGD - DRAIN) Low	t_{PLHPG}	MAX5948A, Figures 2, 6		0.5		µs
		MAX5948B, Figures 2, 6		0.5		

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to V_{EE}, unless otherwise specified.

Note 3: Limits are 100% tested at T_A = +25°C and +85°C. Limits at -40°C are guaranteed by design.

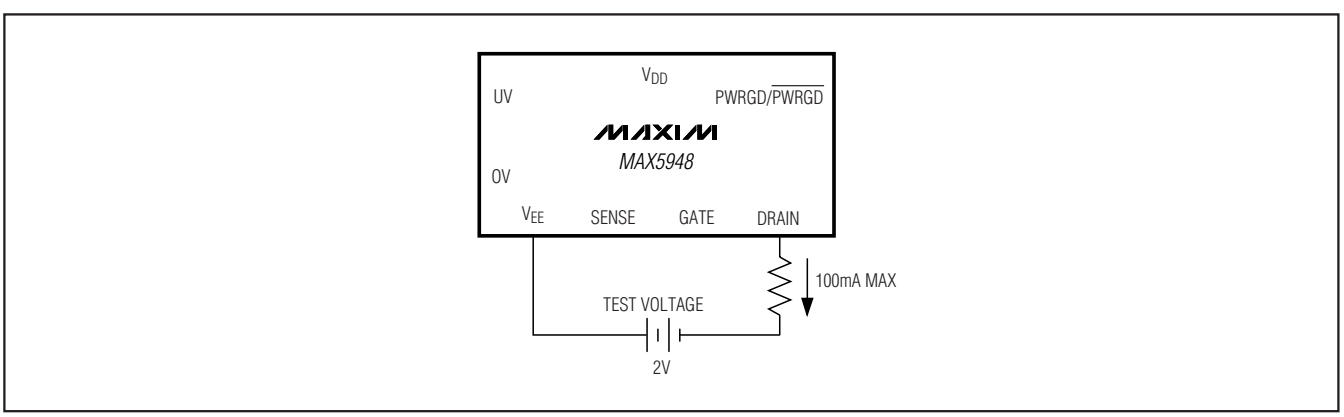


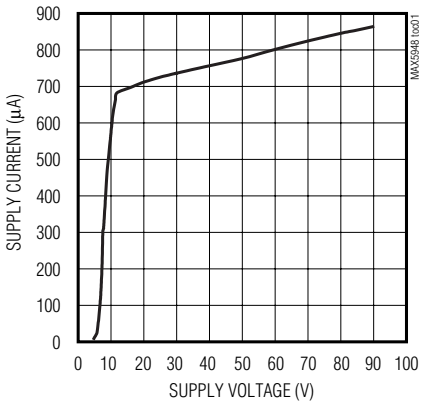
Figure 1. -2V DRAIN Voltage Test Circuit

-48V Hot-Swap Controllers with External RSENSE

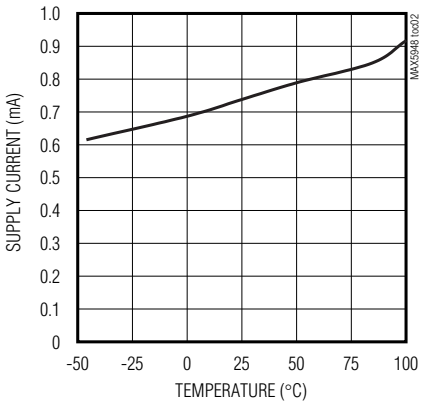
Typical Operating Characteristics

(V_{DD} = 48V, V_{EE} = 0V, T_A = +25°C, unless otherwise noted.)

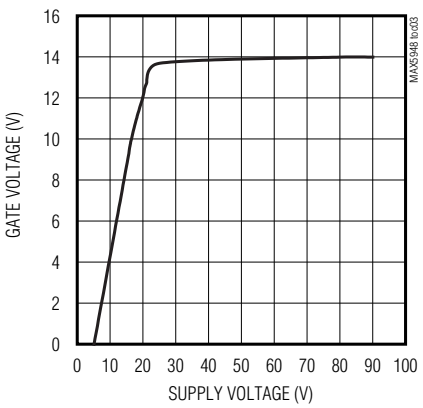
SUPPLY CURRENT vs. SUPPLY VOLTAGE



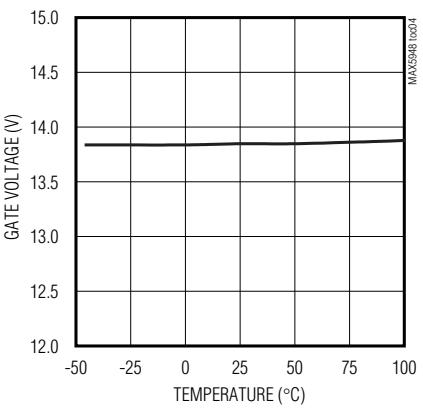
SUPPLY CURRENT vs. TEMPERATURE



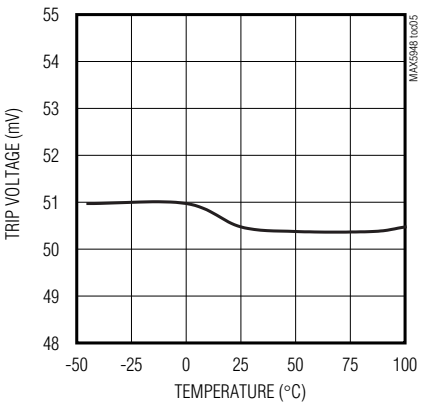
GATE VOLTAGE vs. SUPPLY VOLTAGE



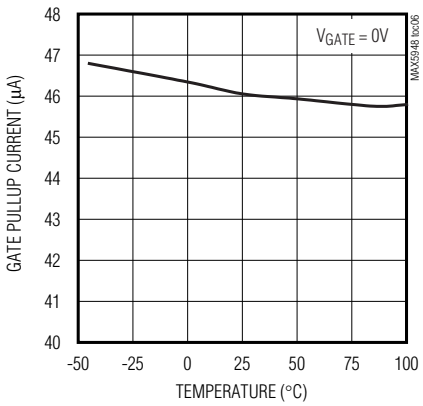
GATE VOLTAGE vs. TEMPERATURE



CIRCUIT-BREAKER TRIP VOLTAGE vs. TEMPERATURE



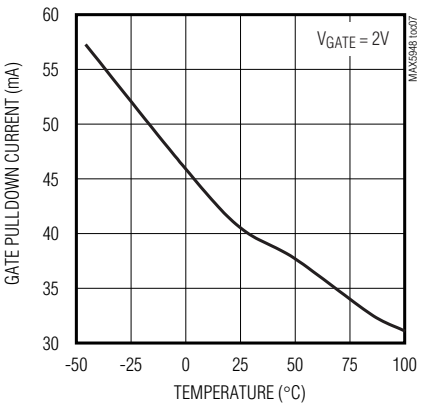
GATE PULLUP CURRENT vs. TEMPERATURE



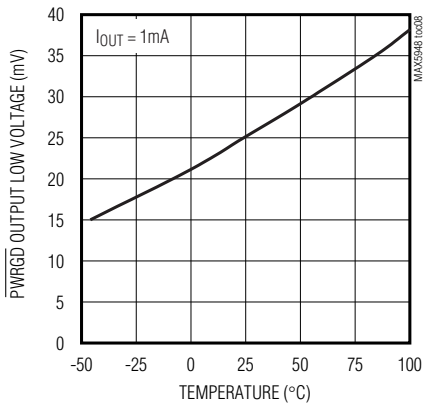
Typical Operating Characteristics (continued)

(V_{DD} = 48V, V_{EE} = 0V, T_A = +25°C, unless otherwise noted.)

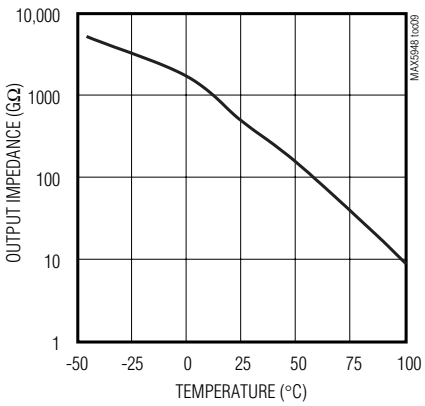
GATE PULLDOWN CURRENT vs. TEMPERATURE



PWRGD OUTPUT LOW VOLTAGE vs. TEMPERATURE (MAX5948A)



PWRGD OUTPUT IMPEDANCE vs. TEMPERATURE (MAX5948B)



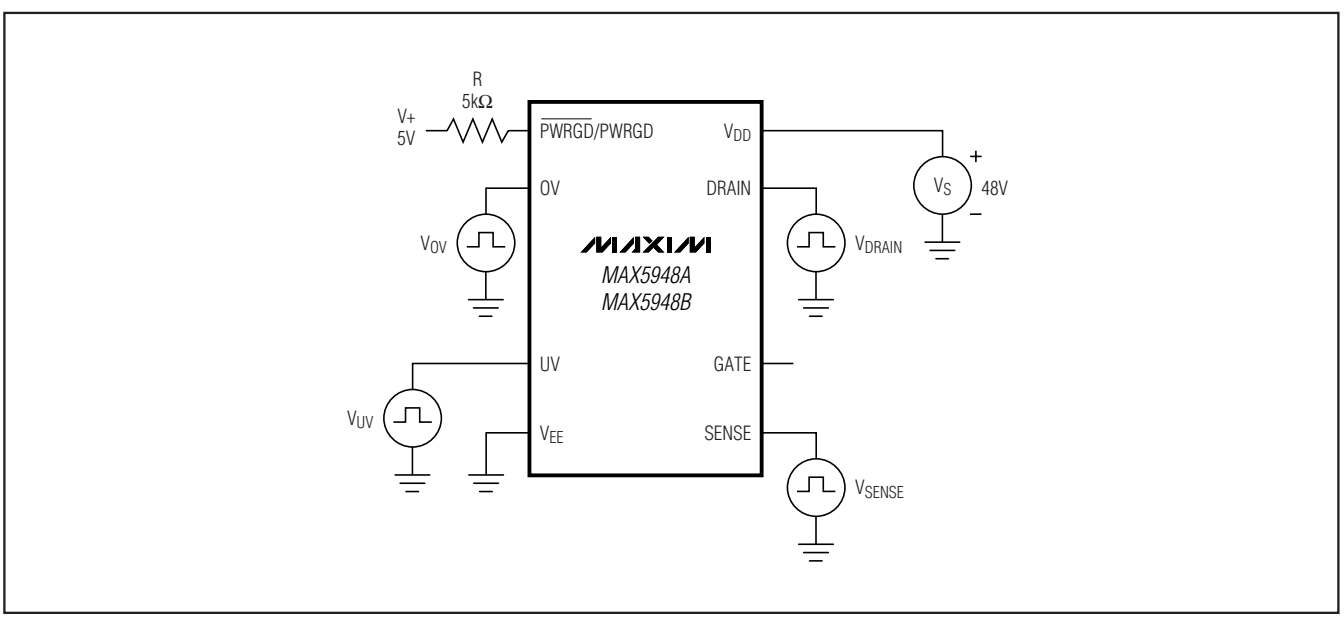


Figure 2. Test Circuit 1

Timing Diagrams

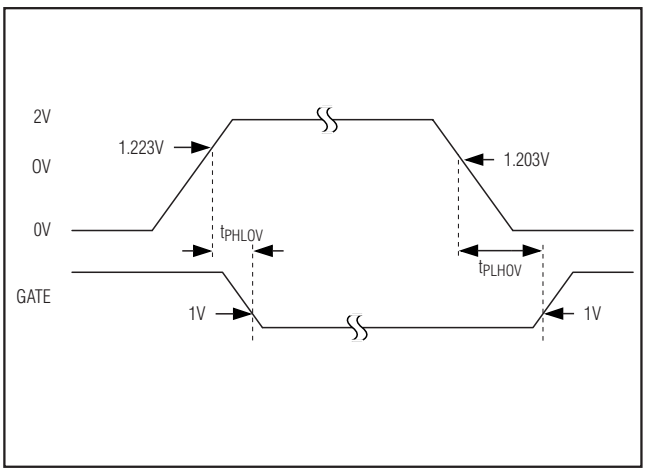


Figure 3. OV to GATE Timing

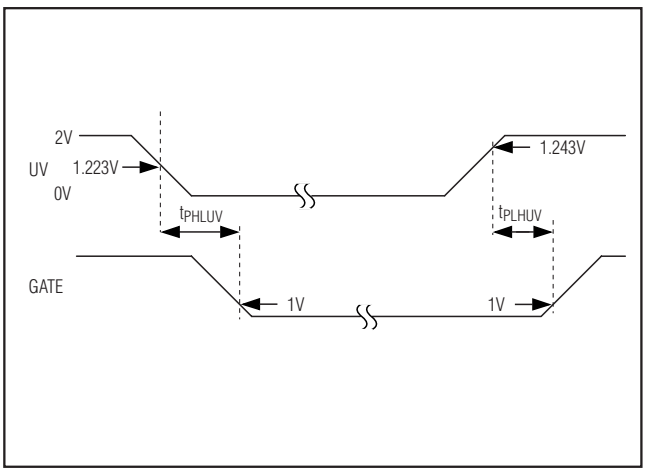


Figure 4. UV to GATE Timing

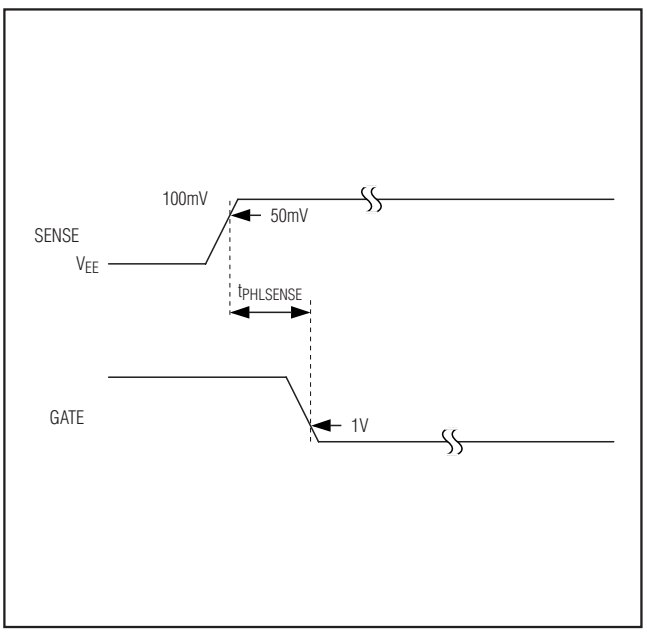


Figure 5. SENSE to GATE Timing

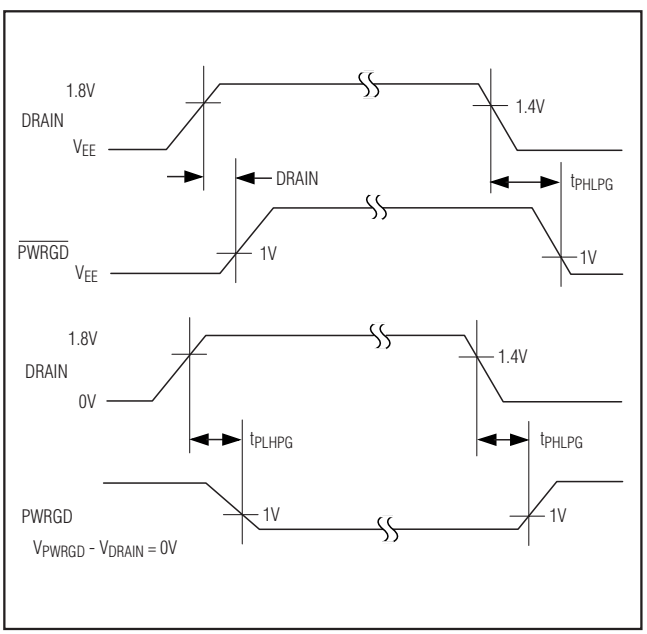


Figure 6. DRAIN to $\overline{PWRGD}$/PWRGD Timing

Pin Description

PIN		NAME	FUNCTION
MAX5948A	MAX5948B		
1	—	$\overline{PWRGD}$	Power-Good Signal Output. $\overline{PWRGD}$ is an active-low open-drain status output referenced to V_{EE}. $\overline{PWRGD}$ is low when $V_{DRAIN} - V_{EE} \le V_{PG}$, indicating a power-good condition. $\overline{PWRGD}$ is open drain otherwise.
—	1	PWRGD	Power-Good Signal Output. PWRGD is an active-high open-drain status output referenced to DRAIN. PWRGD is in a high-impedance state when $V_{DRAIN} - V_{EE} \le V_{PG}$, indicating a power-good condition. PWRGD is pulled low to DRAIN otherwise.
2	2	OV	Input Pin for Overvoltage Detection. OV is referenced to V_{EE}. When OV is pulled above V_{OVH} voltage, the GATE pin is immediately pulled low. The GATE pin remains low until the OV pin voltage reduces to V_{OVL}.
3	3	UV	Input Pin for Undervoltage Detection. UV is referenced to V_{EE}. When UV is pulled above V_{UVH} voltage, the GATE is enabled. When UV is pulled below V_{UVL}, GATE is pulled low. UV is also used to reset the circuit breaker after a fault condition. To reset the circuit breaker, pull UV below V_{UVL}.
4	4	V_{EE}	Device Negative Power-Supply Input. Connect to the negative power-supply rail.
5	5	SENSE	Current-Sense Voltage Input. Connect to an external sense resistor and the external MOSFET source. The voltage drop across the external sense resistor is monitored to detect overcurrent or short-circuit fault conditions. Connect SENSE to V_{EE} to disable the circuit-breaker feature.
6	6	GATE	Gate-Drive Output. Connect to gate of the external n-channel MOSFET.
7	7	DRAIN	Output-Voltage Sense Input. Connect to the output-voltage node (drain of external n-channel MOSFET).
8	8	V_{DD}	Positive Power-Supply Rail Input. This is the power ground in the negative-supply voltage system. Connect to the most positive potential of the power-supply inputs.

Detailed Description

The MAX5948A/MAX5948B are integrated hot-swap controllers for -48V power systems. They allow circuit boards to be safely hot plugged into a live backplane without causing a glitch on the power-supply rail. When circuit boards are inserted into a live backplane, the bypass capacitors at the input of the board's power module or switching power supply can draw large inrush currents as they charge. The inrush currents can cause glitches on the system power-supply rail and damage components on the board.

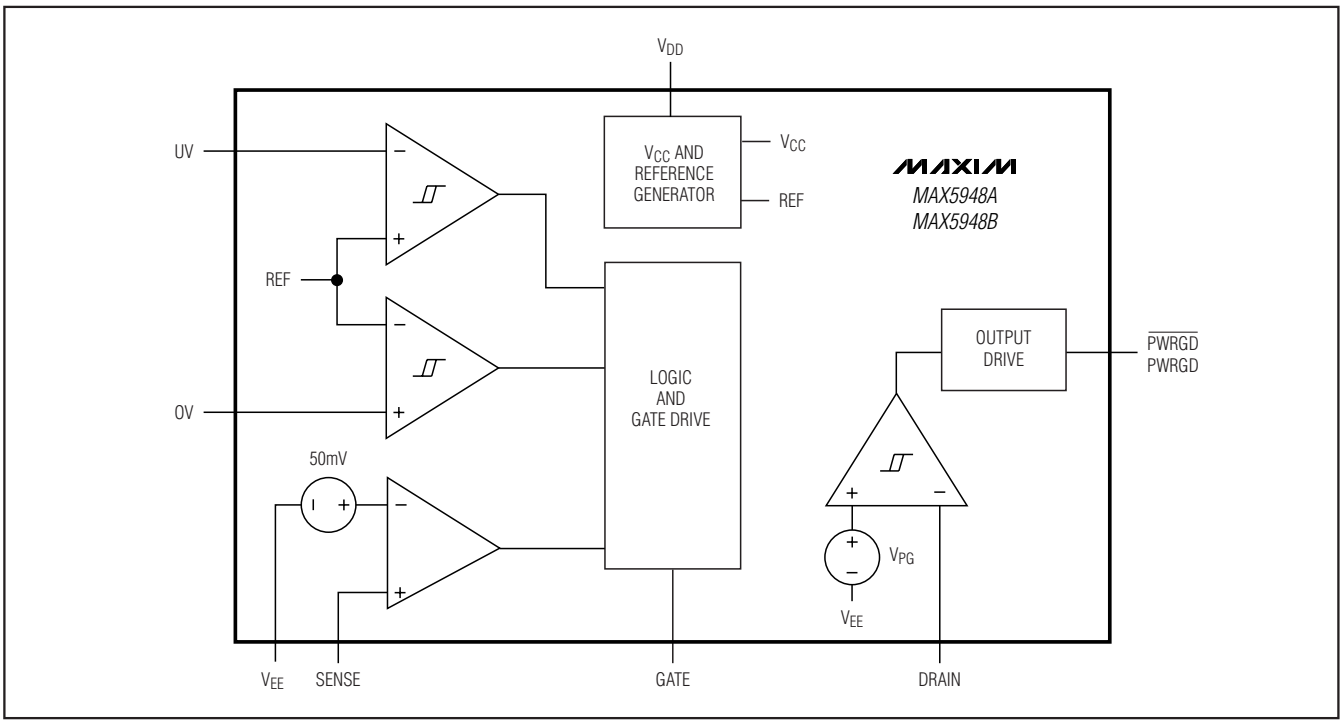
The MAX5948A/MAX5948B provide a controlled turn-on to circuit cards preventing glitches on the power-supply rail and damage to board connectors and components. Both the MAX5948A and MAX5948B provide undervoltage, overvoltage, and overcurrent protection. The MAX5948A/MAX5948B ensure the input voltage is stable and within tolerance before applying power to the load.

Board Insertion

Figure 6a shows a typical hot-swap circuit for -48V systems. When the circuit board first makes contact with the backplane, the DRAIN to GATE capacitance (C_{gd}) of Q1 pulls up the GATE voltage to roughly $I(V_{EE} \times C_{gd}) / (C_{gd} + C_{gs})I$. The MAX5948_ features an internal dynamic clamp between GATE and V_{EE} to keep the gate-to-source voltage of Q1 low during hot insertion, preventing Q1 from passing an uncontrolled current to the load. For most applications, the internal clamp between GATE and V_{EE} of the MAX5948A/MAX5948B eliminates the need for an external gate-to-source capacitor. Resistor R3 limits the current into the clamp circuitry during card insertion.

-48V Hot-Swap Controllers with External RSENSE

Block Diagram



Power-Supply Ramping

The MAX5948A/MAX5948B can reside either on the backplane or the removable circuit board (Figure 6a). Power is delivered to the load by placing an external n-channel MOSFET pass transistor in the power-supply path.

After the circuit board is inserted into the backplane and the supply voltage at V_{EE} is stable and within the undervoltage and overvoltage tolerance, the MAX5948A/MAX5948B turn on Q1. The MAX5948A/MAX5948B gradually turn on the external MOSFET by charging the gate of Q1 with a 45µA current source. Capacitor C2 provides a feedback signal to accurately limit the inrush current. The inrush current can be calculated:

$$I_{INRUSH} = (I_{PU} \times C_L)/C2$$

where C_L is the total load capacitance, C3 + C4, and I_{PU} is the MAX5948_ gate pullup current.

Figure 6b shows the inrush current waveform. The current through C2 controls the GATE voltage. At the end of the DRAIN ramp, the GATE voltage is charged to its final value. The GATE-to-SENSE clamp limits the maximum V_{GS} to about 18V under any condition.

Board Removal

If the card is removed from a live backplane, the output capacitor on the card may not be immediately discharged. While the output capacitor is discharging, the MAX5948_ continues to operate as if the input supply were still connected because the output capacitor temporarily supplies operating current to the IC. If the circuit is connected as in Figure 7a, the voltage at the UV pin falls below the UVLO detect threshold, and the MAX5948_ turns off the external MOSFET. If R4 in the circuit is connected directly to the -48V return, the external MOSFET remains on until the capacitor is discharged sufficiently to drop the UV pin voltage to the UVLO detect threshold.

In either case, when the MOSFET is turned off, the output capacitor continues to discharge by the IC supply current I_{DD}. The I_{DD} flows into the IC at the V_{DD} terminal, out at the V_{EE} terminal, and back to the capacitor through the substrate diode of the external MOSFET. There is also a parallel current path between the V_{EE} and DRAIN terminals through multiple internal ESD-protection diodes. The protection circuit built into the IC allows the DRAIN terminal voltage to drop below that of the V_{EE} terminal so long as the absolute maximum allowed DRAIN terminal current (-100mA) is not exceeded. As I_{DD} is only 2mA maximum, this limiting current will not even be approached.

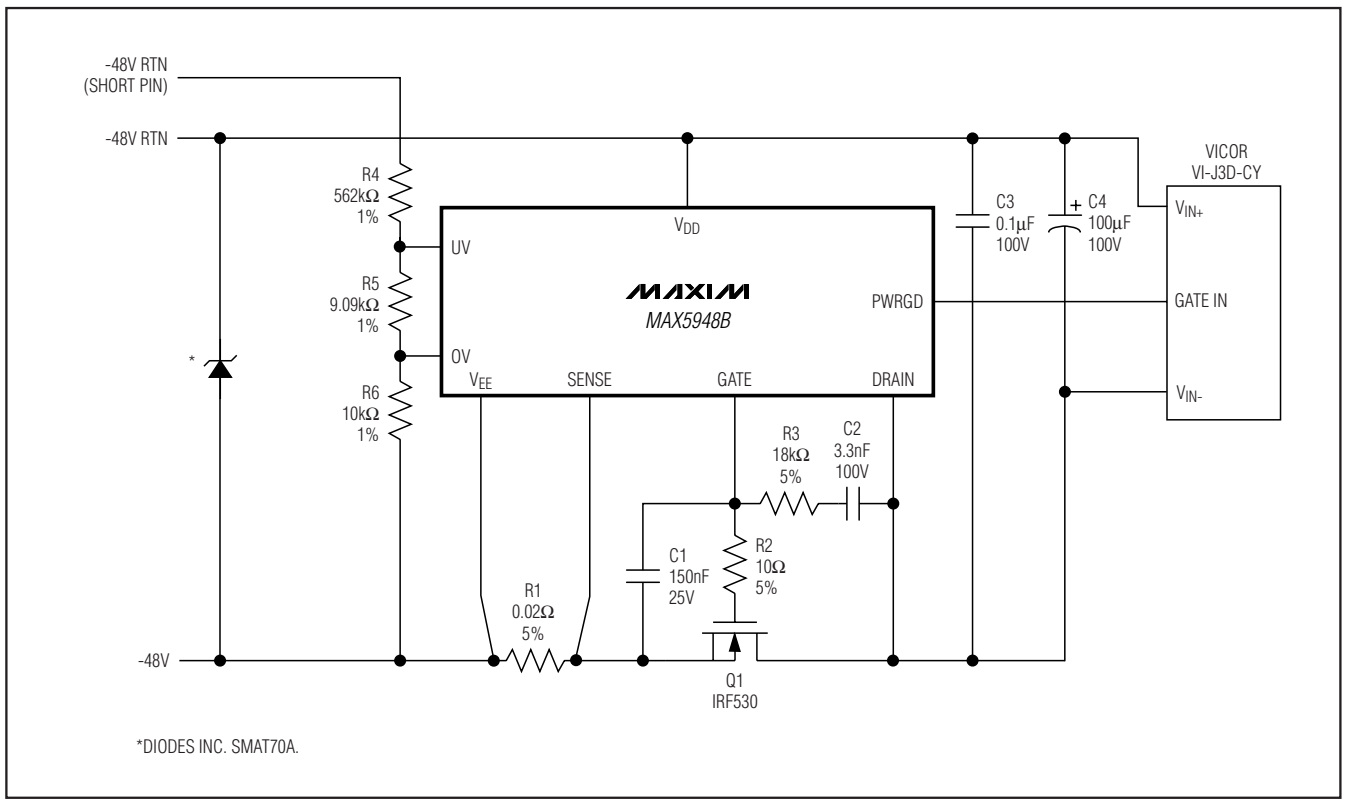


Figure 7a. Inrush Control Circuitry

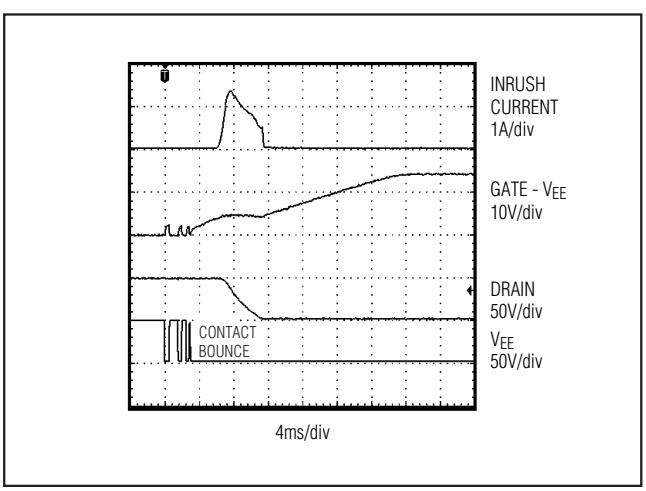


Figure 7b. Input Inrush Current

Electronic Circuit Breaker

The MAX5948 provides a circuit-breaker feature that protects against excessive load current and short-circuit conditions. The load current is monitored by sensing the voltage across an external sense resistor connected between V_{EE} and SENSE.

If the voltage between V_{EE} and SENSE exceeds the current-limit trip voltage (V_{CB}) for a period of $t_{PHLSENSE}$, the electronic circuit breaker will trip, causing the MAX5948A/MAX5948B to turn off the external MOSFET as shown in Figure 8.

After an overcurrent fault condition, the circuit breaker can be reset by pulling the UV pin low and then pulling UV high or by cycling power to the MAX5948A/MAX5948B.

-48V Hot-Swap Controllers with External RSENSE

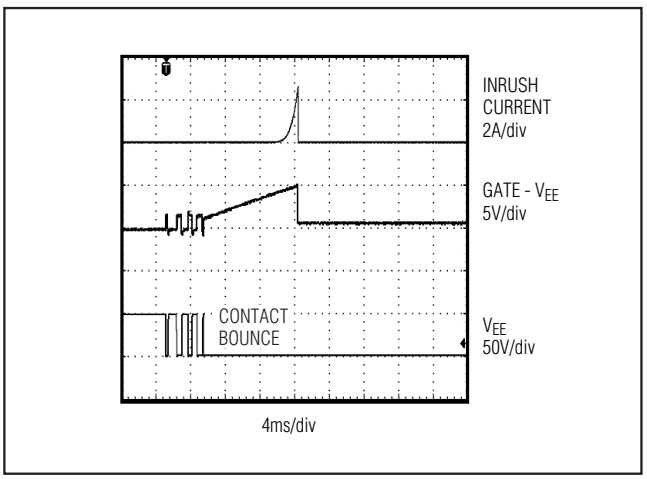


Figure 8. Startup Into a Short Circuit

If more than 3µs (typ) deglitch time ($t_{PHLSENSE}$) is needed to prevent spurious shutdown due to load current spikes or noise, a simple lowpass filter can be used between the SENSE and V_{EE} pins as shown in Figure 9. Resistor R7 and capacitor C3 slow down the response of the circuit breaker to filter momentary glitches in the SENSE voltage. The additional delay time can be estimated with the following equation:

$$t_{cbdly} = R7 \times C3 \times \ln\left(\frac{V_f - V_I}{V_f - V_{CB}}\right)$$

$$= R7 \times C3 \times \ln\left(\frac{I_f - I_I}{I_f - I_{CB}}\right)$$

where I_f is the current in fault condition, I_I is the initial current before the fault, and I_{CB} is the circuit-breaker trip current ($I_{CB} = V_{CB}/R1$). Alternatively, the corresponding voltages across the sense resistor (V_f, V_I, and V_{CB}) may be used in the equation as shown. The SENSE pin of the MAX5948A/MAX5948B sources very little current (0.02µA typ), so the addition of resistor R7 will introduce very little error in the circuit-breaker trip voltage. For example, a 10kΩ resistor for R7 will only cause a 200µV offset.

Example: A system has a 1A nominal load current and a 20mΩ sense resistor. The circuit-breaker delay needs to be increased to 50µs in response to a load current step to 5A. The circuit-breaker trip current is 50mV/20mΩ = 2.5A. Solving for R7 x C3 in the equation above yields a desired time constant of 100µs. This can be achieved with R7 = 100Ω and C3 = 1µF.

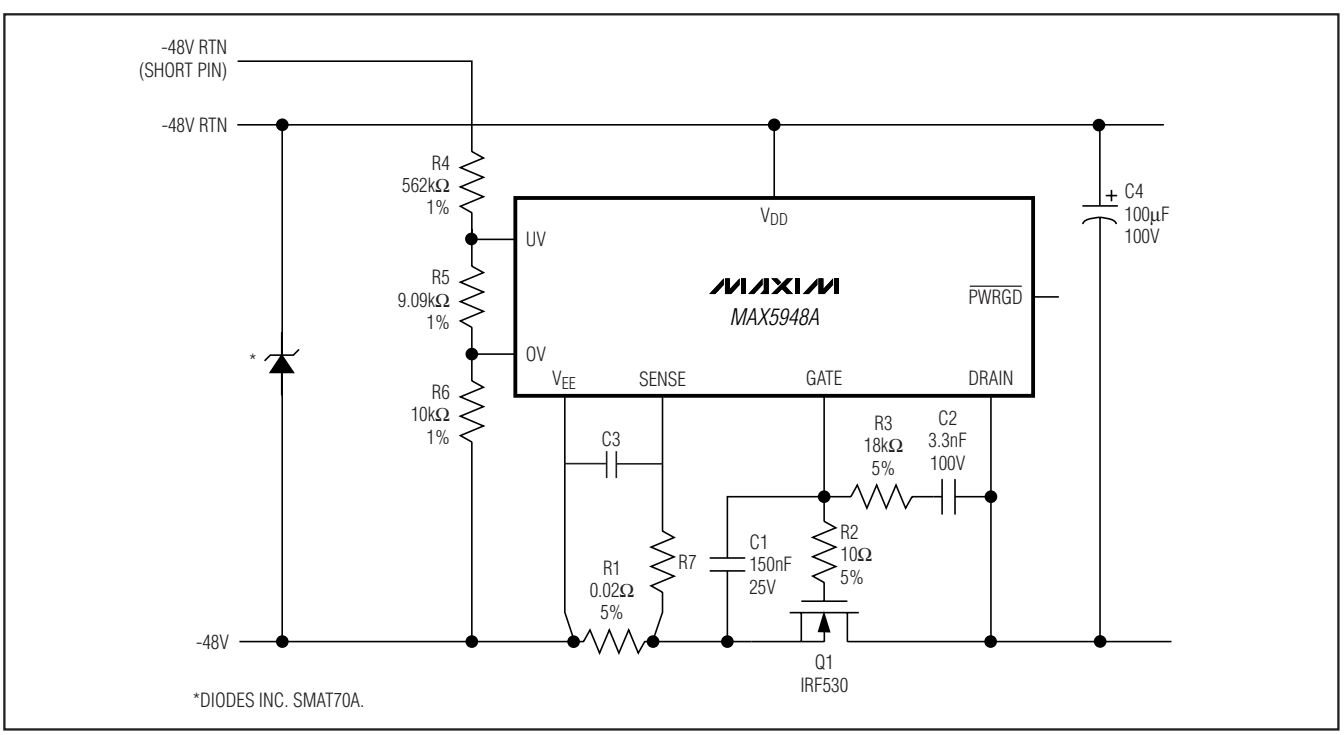


Figure 9. Extending the Short-Circuit Protection Delay

In the event of a short circuit at the output, the input supply may dip below the UV threshold, resetting the circuit breaker. The MAX5948 cycles ON and OFF until the short is removed, which can be minimized by creating a deglitching delay at the UV pin with a capacitor from UV to V_{EE}. This allows the input supply to recover before the UV pin resets the circuit breaker.

Figure 10 shows a circuit that automatically resets the circuit breaker after a current fault. Transistors Q2 and Q3 along with C4, D1, R7, and R8 form a programmable one-shot circuit. In normal operation, the GATE pin is pulled high and Q3 is turned on, pulling node 2 to V_{EE}. Resistor R8 turns off Q2. When a short occurs, the GATE pin is pulled low and Q3 turns off. Node 2 starts to charge C4 and Q2 turns on, pulling the UV pin low and resetting the circuit breaker. The instant C4 is fully charged, R8 turns off Q2, UV goes high and the GATE starts to ramp up. Q3 turns back on and pulls node 2 back to V_{EE}. Diode D1 clamps node 3 at one diode drop below V_{EE}. The duty cycle is set to 10% to prevent Q1 from overheating.

Undervoltage and Overvoltage Protection

The UV and OV pins can be used to detect undervoltage and overvoltage conditions. The UV and OV pins are internally connected to analog comparators with 20mV of hysteresis. When the UV voltage falls below its threshold or the OV voltage rises above its threshold, the GATE pin is immediately pulled low. The GATE pin is held low until UV goes high and OV is low indicating that the input supply voltage is within specification.

The UV pin is also used to reset the circuit breaker after a fault condition has occurred. The UV pin can be pulled below V_{UVL} to reset the circuit breaker.

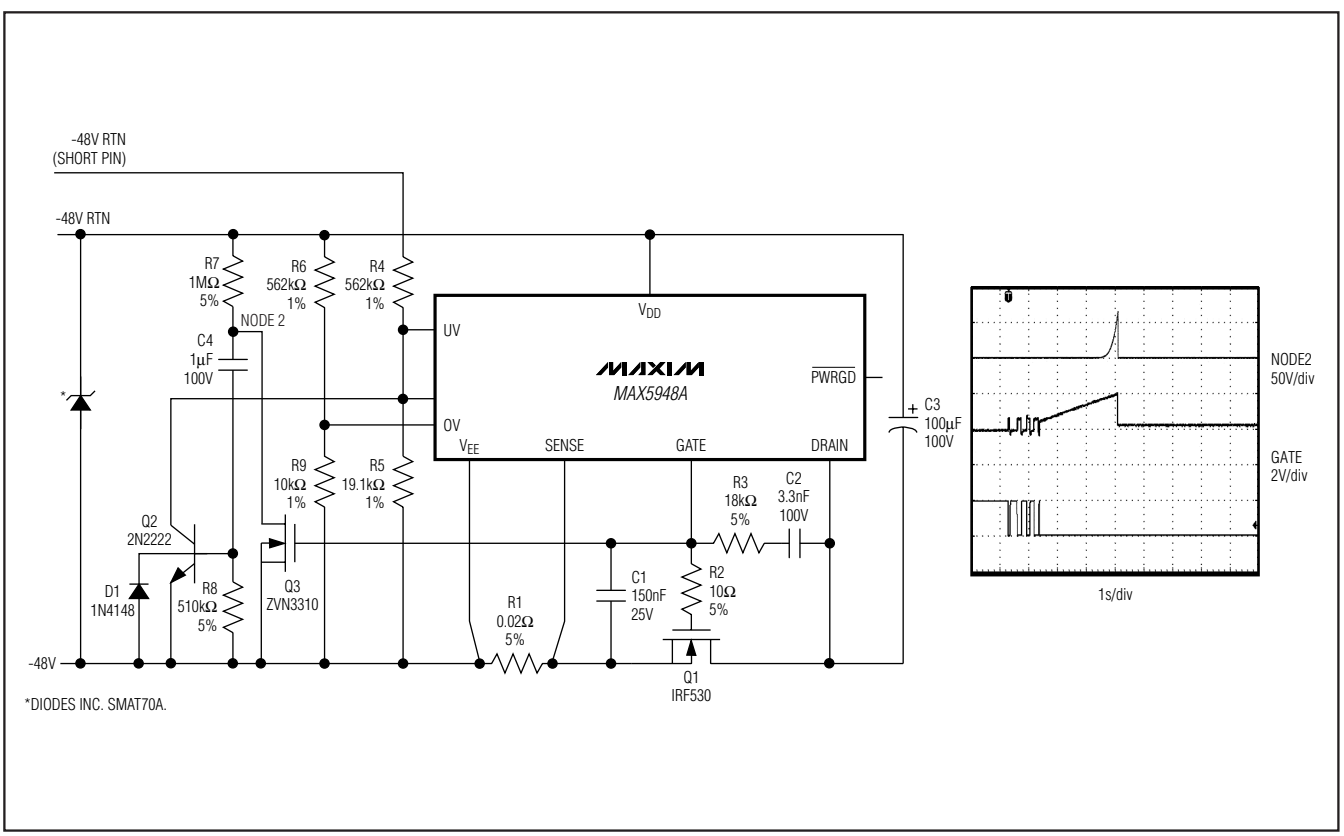


Figure 10. Automatic Restart After Current Fault

-48V Hot-Swap Controllers with External RSENSE

Figure 11a shows how to program the undervoltage and overvoltage trip thresholds using three resistors. With R4 = 562kΩ, R5 = 9.09kΩ, and R6 = 10kΩ, the undervoltage threshold is set to 37.2V (with a 37.8V release from undervoltage) and the overvoltage is set to 71.1V (with a 69.9V release from overvoltage).

More hysteresis can be added to the undervoltage lockout with the circuit shown in Figure 11b. Resistor R3 connected between GATE and UV lowers the supply undervoltage lockout threshold (supply voltage decreasing) to:

$$V_{UV,HL} = V_{UVL}\left(\frac{R2\times R3 + R1\times R3 + R1\times R2}{R2\times R3}\right) - \left(\Delta V_{GATE}\times\frac{R1}{R3}\right)$$

where V_{UVL} is typically 1.223V. The supply voltage to release from undervoltage lockout (supply voltage increasing) is:

$$V_{UV,LH} = V_{UVH}\left(\frac{R2\times R3 + R1\times R3 + R1\times R2}{R2\times R3}\right)$$

where V_{UVH} is typically 1.243V. The supply undervoltage lockout hysteresis is the difference, or:

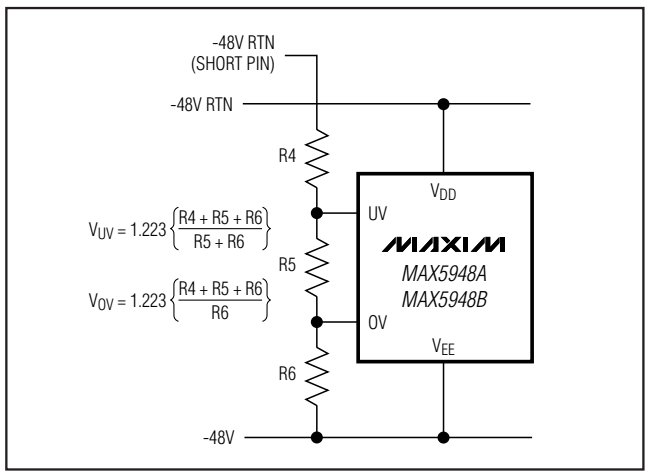


Figure 11a. Undervoltage and Overvoltage Sensing

$$V_{UV,HYS} = V_{UVHY}\left(\frac{R2\times R3 + R1\times R3 + R1\times R2}{R2\times R3}\right) + \left(\Delta V_{GATE}\times\frac{R1}{R3}\right)$$

where V_{UVHY} is typically 20mV.

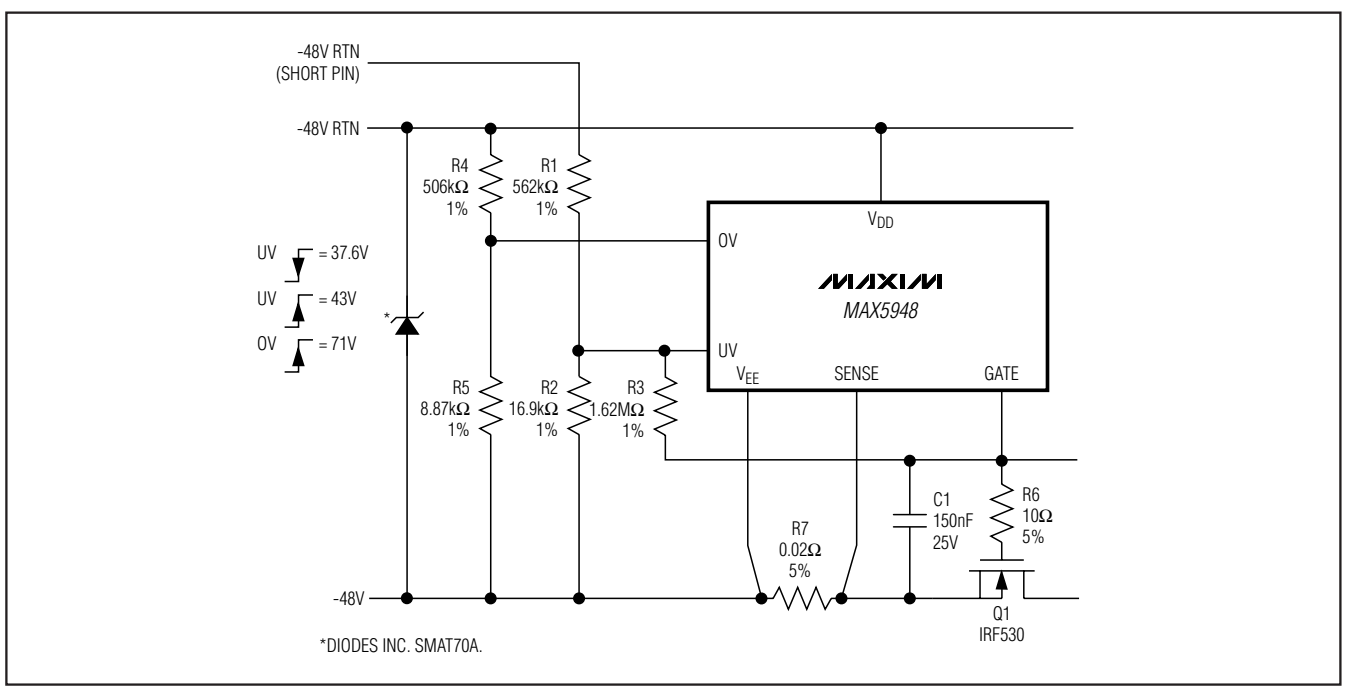


Figure 11b. Programmable Hysteresis For Undervoltage

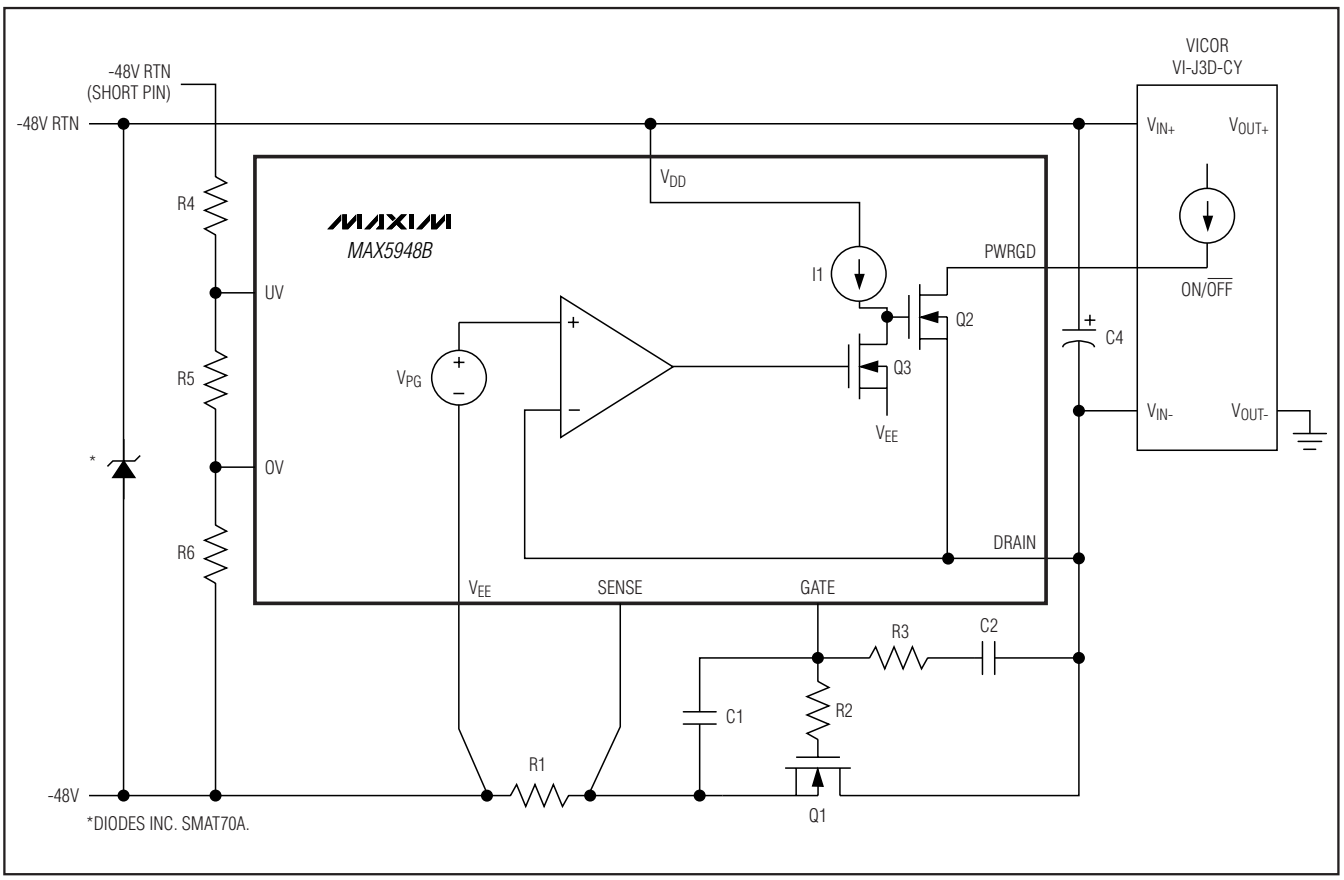


Figure 12. Active-High Enable Module

A separate resistor-divider must be used for the overvoltage lockout setting. The supply overvoltage lockout threshold is:

$$V_{OV} = V_{OVH}\left(\frac{R4+R5}{R5}\right)$$

where V_{OVH} is typically 1.223V.

Using R1 = 562kΩ, R2 = 16.9kΩ, R3 = 1.62MΩ, R4 = 506kΩ, R5 = 8.87kΩ, and the typical value of V_{GATE} = 13.5V results in the following thresholds:

$$V_{UV,HL} = 37.6V$$

$$V_{UV,LH} = 43V$$

(with hysteresis now increased to 5.4V), and V_{OV} = 71V (with 1.2V hysteresis).

$\overline{PWRGD}$/PWRGD Output

The $\overline{PWRGD}$ (PWRGD) output can be used directly to enable a power module after hot insertion. The MAX5948A ($\overline{PWRGD}$) can be used to enable modules with an active-low enable input (Figure 13), while the MAX5948B (PWRGD) is used to enable modules with an active-high enable input (Figure 12).

The PWRGD signal is referenced to the DRAIN terminal, which is the negative supply of the power module. The $\overline{PWRGD}$ signal is referenced to V_{EE}.

When the DRAIN voltage of the MAX5948A is high with respect to V_{EE}, the internal pulldown MOSFET Q2 is off and the $\overline{PWRGD}$ pin is in a high-impedance state (Figure 13). $\overline{PWRGD}$ is pulled high by the module's internal pullup current source, turning the module off. When the DRAIN voltage drops below V_{PG}, Q2 turns on and $\overline{PWRGD}$ pulls low, enabling the module.

The $\overline{PWRGD}$ signal can also be used to turn on an LED or optoisolator to indicate that the power is good (Figure 13) (see the *Component Selection Procedure* section).

-48V Hot-Swap Controllers with External RSENSE

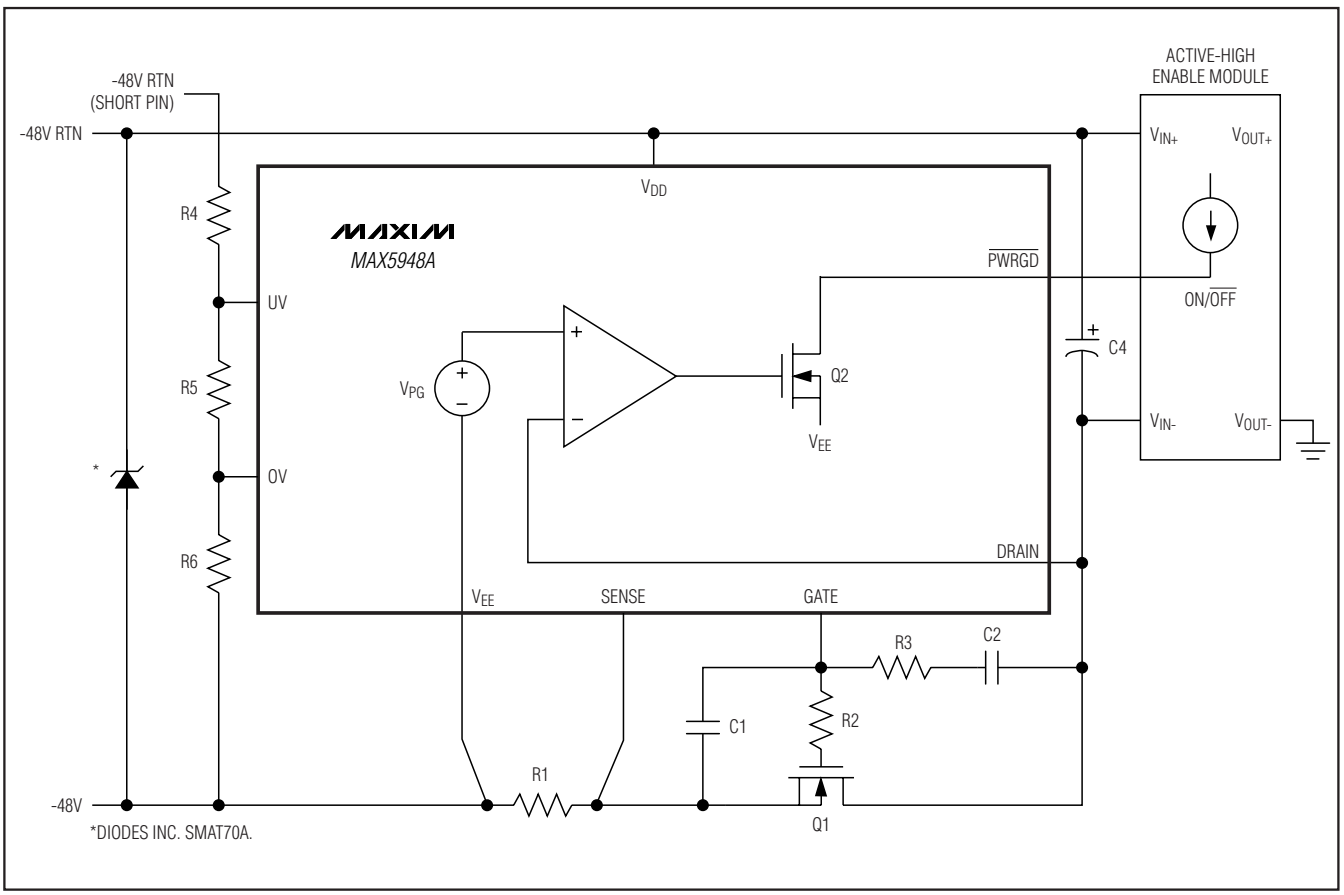


Figure 13. Active-Low Enable Module

When the DRAIN voltage of the MAX5948B is high with respect to V_{EE} (Figure 12), the internal MOSFET Q3 is turned off so that I1 and the internal MOSFET Q2 clamp the PWRGD pin to the DRAIN pin. MOSFET Q2 sinks the module's pullup current, and the module turns off.

When the DRAIN voltage drops below V_{PG}, MOSFET Q3 turns on, shorting I1 to V_{EE} and turning Q2 off. The pullup current in the module pulls PWRGD high, enabling the module.

GATE Voltage Regulation

GATE goes high when the following startup conditions are met: UV is high, OV is low, the supply voltage is above $V_{UV,LH}$, and (V_{SENSE} - V_{EE}) is less than 50mV. GATE is pulled up with a 45µA current source and is regulated at 13.5V above V_{EE}. The MAX5948A/MAX5948B include an internal clamp that ensures the GATE voltage of the external MOSFET never exceeds 18V. During a fast-rising V_{DD}, the clamp also keeps the GATE and SENSE potentials as close as possible to prevent the FET from accidentally turning on. When a fault condition is detected, GATE is pulled low with a 50mA current.

DRAIN Pin Protection

The MAX5948's DRAIN pin withstands negative voltages (referenced to V_{EE}); no external diode is required. When the -48V backplane shorts to ground and V_{EE} becomes 0V, the DRAIN pin is held at less than 1.5V (sum of Q1's body diode and voltage drop across R1) below V_{EE} due to the storage capacitor C3 (Figure 13). The -1.5V results in a 50mA reverse DRAIN current, which is within the capability of the MAX5948. A design with R1 larger than 0.1Ω may require a resistor in series with the DRAIN pin to avoid exceeding the 50mA drain current maximum.

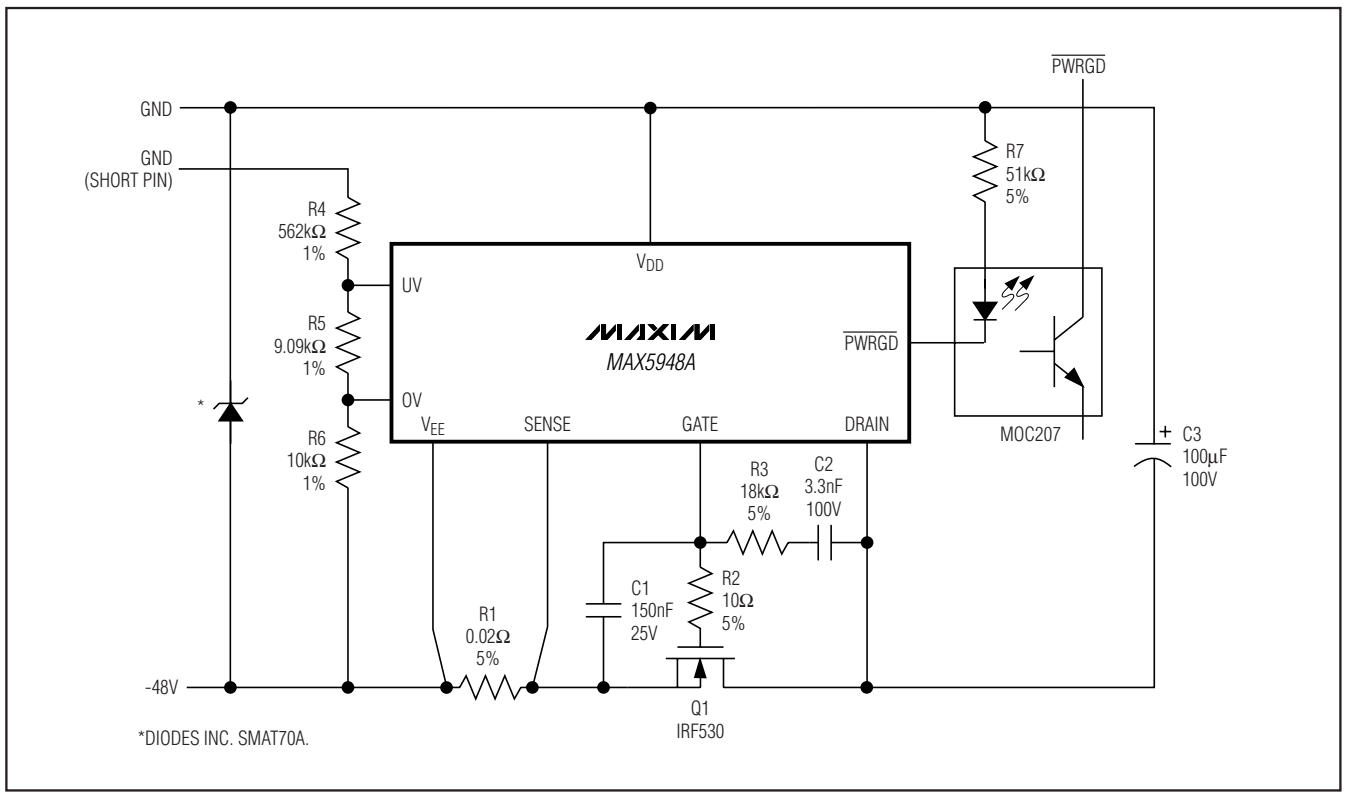


Figure 14. Using $\overline{PWRGD}$ to Drive an Optoisolator

Applications Information

(Refer to the *Typical Operating Circuit.*)

Sense Resistor

The circuit-breaker threshold is set to 50mV (typically). Select a sense resistor that causes a drop equal to or above the current-limit threshold at a current level above the maximum normal operating current. Typically, set the overload current to 1.5 to 2.0 times the nominal load current plus the load-capacitance charging current during startup. Choose the sense resistor power rating to be greater than $(V_{CB})^2 / R_{SENSE}$.

Component Selection Procedure

- Determine load capacitance:

  C_L = C3 + C4 + module input capacitance
- Determine load current, I_{LOAD}.
- Select circuit-breaker current, for example:

  $$I_{CB} = 2 \times I_{LOAD}$$
- Calculate R_{SENSE}:

  $$R_{SENSE} = \frac{50mV}{I_{CB}}$$

  Realize that I_{CB} varies ±20% due to trip-voltage tolerance.
- Set allowable inrush current:

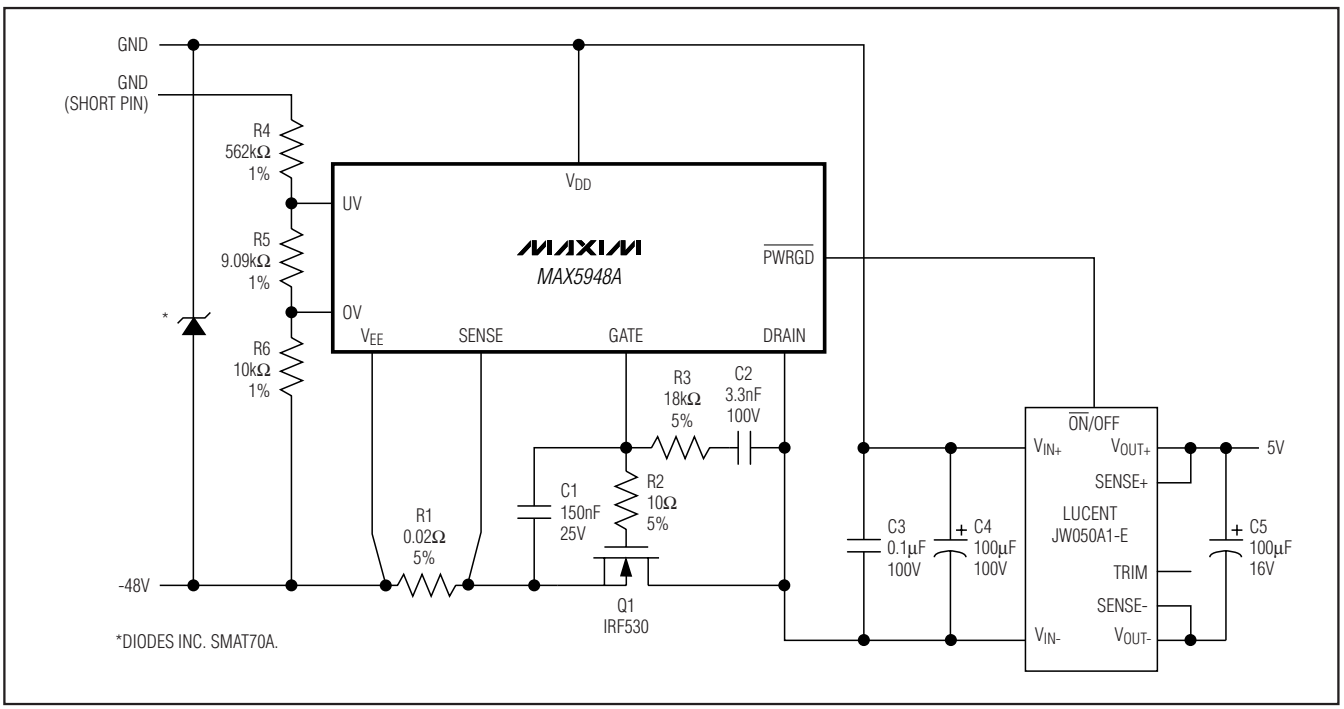
  $$I_{INRUSH} \le 0.8 \times \frac{40mV}{R_{SENSE}} - I_{LOAD} \text{ or}$$
  $$I_{INRUSH} + I_{LOAD} \le 0.8 \times I_{CB(MIN)}$$
- Determine value of C2:

  $$C_2 = \frac{45\mu A \times C_L}{I_{INRUSH}}$$
- Calculate value of C1:

  $$C_1 = (C_2 + C_{gd}) \times \left(\frac{V_{IN(MAX)} - V_{GS(TH)}}{V_{GS(TH)}} \right)$$

-48V Hot-Swap Controllers with External RSENSE

Typical Operating Circuit



- Determine value of R3:

$$R_3 \le \frac{150\mu s}{C_2}$$

- Set R2 = 10Ω.
- If an optocoupler is utilized as in Figure 14, determine the LED series resistor:

$$R_7 = \frac{V_{IN(NOMINAL)} - 2V}{3mA \le I_{LED} \le 5mA}$$

Although the suggested optocoupler is not specified for operation below 5mA, its performance is adequate for 36V temporary low-line voltage where LED current would then be ≈2.2mA to 3.7mA. If R7 is set as high as 51kΩ, optocoupler operation should be verified over the expected temperature and input voltage range to ensure suitable operation when LED current ≈0.9mA for 48V input and ≈0.7mA for 36V input.

If input transients are expected to momentarily raise the input voltage to >100V, select an input transient-voltage-suppression diode (TVS) to limit maximum voltage on the MAX5948 to less than 100V. A suitable device is the Diodes Inc. SMAT70A telecom-specific TVS.

Select Q1 to meet supply voltage, load current, efficiency, and Q1 package power-dissipation requirements:

$$BV_{DSS} \ge 100V$$

$$I_{D(ON)} \ge 3 \times I_{LOAD}$$

DPAK, D2PAK, or TO-220AB

Choose the lowest practical $R_{DS(ON)}$ within budget constraints. MOSFETs with values from 14mΩ to 540mΩ are available at 100V breakdown.

Ensure that the temperature rise of Q1 junction is not excessive at normal load current for the package selected. Ensure that I_{CB} current during voltage transients does not exceed allowable transient-safe operating-area limitations. This is determined from the SOA and transient-thermal-resistance curves in the Q1 manufacturer's data sheet.

Example 1:

I_{LOAD} = 2.5A, efficiency = 98%, then V_{DS} = 0.96V is acceptable, or $R_{DS(ON)} \le 384m\Omega$ at operating temperature is acceptable. An IRL520NS 100V nMOS with $R_{DS(ON)} \le 180m\Omega$ and $I_{D(ON)}$ = 10A is available in D2PAK. (A Vishay Siliconix SUD40N10-25 100V nMOS with $R_{DS(ON)} \le 25m\Omega$ and $I_{D(ON)}$ = 40A is available in DPAK, but may be more costly because of a larger die size).

Using the IRL520NS, V_{DS} ≤ 0.625V even at +80°C so efficiency ≥ 98.6% at 80°C. P_D ≤ 1.56W and junction temperature rise above case temperature would be 5°C due to the package θ_{JC} = 3.1°C/W thermal resistance. Of course, using the SUD40N10-25 would yield an efficiency greater than 99.8% to compensate for the increased cost.

If I_{CB} is set to twice I_{LOAD}, or 5A, V_{DS} momentarily doubles to ≤ 1.25V. If C_{OUT} = 4000µF, transient-line input voltage is Δ36V, the 5A charging-current pulse is:

$$t = \frac{4000\mu F \times 1.25V}{5A} = 1ms$$

Entering the data sheet transient-thermal-resistance curves at 1ms provides a θJC = 0.9°C/W. P_D = 6.25W, so Δt_{JC} = 5.6°C. Clearly, this is not a problem.

Example 2:

I_{LOAD} = 10A, efficiency = 98%, allowing V_{DS} = 0.96V but $R_{DS(ON)}$ ≤ 96mΩ. An IRF530 in a D^2PAK exhibits $R_{DS(ON)}$ ≤ 90mΩ at +25°C and ≤ 135mΩ at +80°C. Power dissipation is 9.6W at +25°C or 14.4W at +80°C. Junction-to-case thermal resistance is 1.9W/°C, so the junction temperature rise would be approximately 5°C above the +25°C case temperature. For higher efficiency, consider IRL540NS with $R_{DS(ON)}$ ≤ 44mΩ. This allows η = 99%, P_D ≤ 4.4W, and T_{JC} = +4°C (θ_{JC} = 1.1°C/W) at +25°C.

Thermal calculations for the transient condition yield I_{CB} = 20A, V_{DS} = 1.8V, t = 0.5ms, transient θ_{JC} = 0.12°C/W, P_D = 36W and Δt_{JC} = 4.3°C.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SO	S8+5	21-0041	90-0096

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/04	Initial release	—
1	8/11	Updated *Ordering Information*, *Absolute Maximum Ratings*, *Electrical Characteristics*, and *Package Information*.	1, 2, 3, 17