



**austriamicrosystems AG**

**is now**

**ams AG**

The technical content of this austriamicrosystems datasheet is still valid.

**Contact information:**

**Headquarters:**

ams AG  
Tobelbaderstrasse 30  
8141 Unterpremstaetten, Austria  
Tel: +43 (0) 3136 500 0  
e-Mail: [ams\\_sales@ams.com](mailto:ams_sales@ams.com)

Please visit our website at [www.ams.com](http://www.ams.com)

## AS3711

### Quad Buck High Current PMIC with Charger

#### 1 General Description

The AS3711 is a compact System PMU with integrated battery charger and back light driver.

The device offers advanced power management functions. All necessary ICs and peripherals in a battery powered mobile device are supplied by the AS3711. It features 3 DCDC buck converters as well as 8 low noise LDOs. The different regulated supply voltages are programmable via the serial control interface. 4MHz operation with 1uH coils are reducing cost and PCB space.

AS3711 further features a DCDC buck controller which is ideal to support processor core currents up to 3A.

The two step-up converter generate voltages for e.g.the backlight, classD amplifier, USB host support or LCD display supply. Both constant voltage (for e.g. OLED supply) as well as constant current (white LED backlight) operations with three current sinks are possible. An internal voltage protection is limiting the output voltage in the case of external component failures.

AS3711 contains a linear or switching mode Li-Ion battery charger with constant current and constant voltage. The maximum charging current is 1.5A. An integrated battery switch and an optional external switch are separating the battery during charging or whenever an external power supply is present. With this switch it is also possible to operate with no or deeply discharged batteries. A programmable current limit (100mA - 2.5A) can be used to control the maximum current used from a USB supply or charger input. Additional features are a 30V OV protection and battery temperature supervision.

The single supply voltage may vary from 2.7V to 5.5V.

#### 2 Key Features

##### Voltage Generation

- 3 DCDC step down regulators (2-4MHz)
  - DVM (0.6V-3.3V; 1x 1.2-1.5A, 2x 0.7-1A)
  - 60µA quiescent current
  - 2A with combined DCDC 2 & 3
- DCDC step down controller
  - DVM (0.6V-3.3V; 2-3A)
- 2 analog low noise LDOs, 6 digital LDOs
  - 2x 1.2-3-3V, 6x 0.9-3.3V; 150-300mA
  - 30µA quiescent current (low power mode)
- 1 ultra low power always on LDO 2.5V, 10mA
- Power supply supervision
- 4sec and 8sec emergency shut-down
- Stand-by function with voltage selection

##### HV Backlight Driver

- 2x step up with external transistor
  - e.g. 0.5-1A@5V; 40mA@50V
- Voltage control mode and over-voltage protection
- 3 programmable current sinks (max. 40mA)
- Possible external PWM dimming input (DLS, CABC)

##### Battery Charger

- Programmable trickle charging (25-220mA)
- Programmable constant current charging (up to 1500mA)
- Programmable constant voltage charging (3.9V-4.25V)
- Charger time-out and temperature supervision
- Selectable current limitation for USB mode
- Integrated battery switch & ideal diode (linear mode)
- External battery switch control (switching mode)
- External 30V OV protection

##### Supervisor

- Automatic battery monitoring with interrupt generation and selectable warning level
- Automatic temperature monitoring with interrupt generation and selectable warning and shutdown levels

##### Real Time Clock

- Ultra low power 32kHz oscillator
- Sec and minute counter, auto wake-up
- Programmable alarm
- Repeating alarm (seconds, minutes, 2 minutes, or 8 minutes)
- 32kHz clock output to peripheral
- <1µA total power consumption

##### General Purpose IOs

- 10-bit general purpose ADC input
- Wake-up/sleep and DVM input
- PWM (DLS, CABC) dimming input
- Status output for: charger, low battery, power good and step-up over-current
- Q32k clock output
- Interrupt output
- PWM output
- Step-up feedback input

### OTP programmable BOOT Sequence

- Programmable regulator default voltages
- Programmable start-up sequence

### General Purpose ADC

- 10-bit resolution
- Several internal / external sources
  - VUSB, VSUP, CHGIN, VBAT
  - GPIOx, CURRx
  - XOUT32k, SENSEN\_SU1, LX\_SD4
  - Chip temperature

### Control Interface

- I2C control lines, including watchdog
- ON input
- Bidirectional reset, with selectable delay
- Ultra low power standby mode

### Power-On Reset Circuit

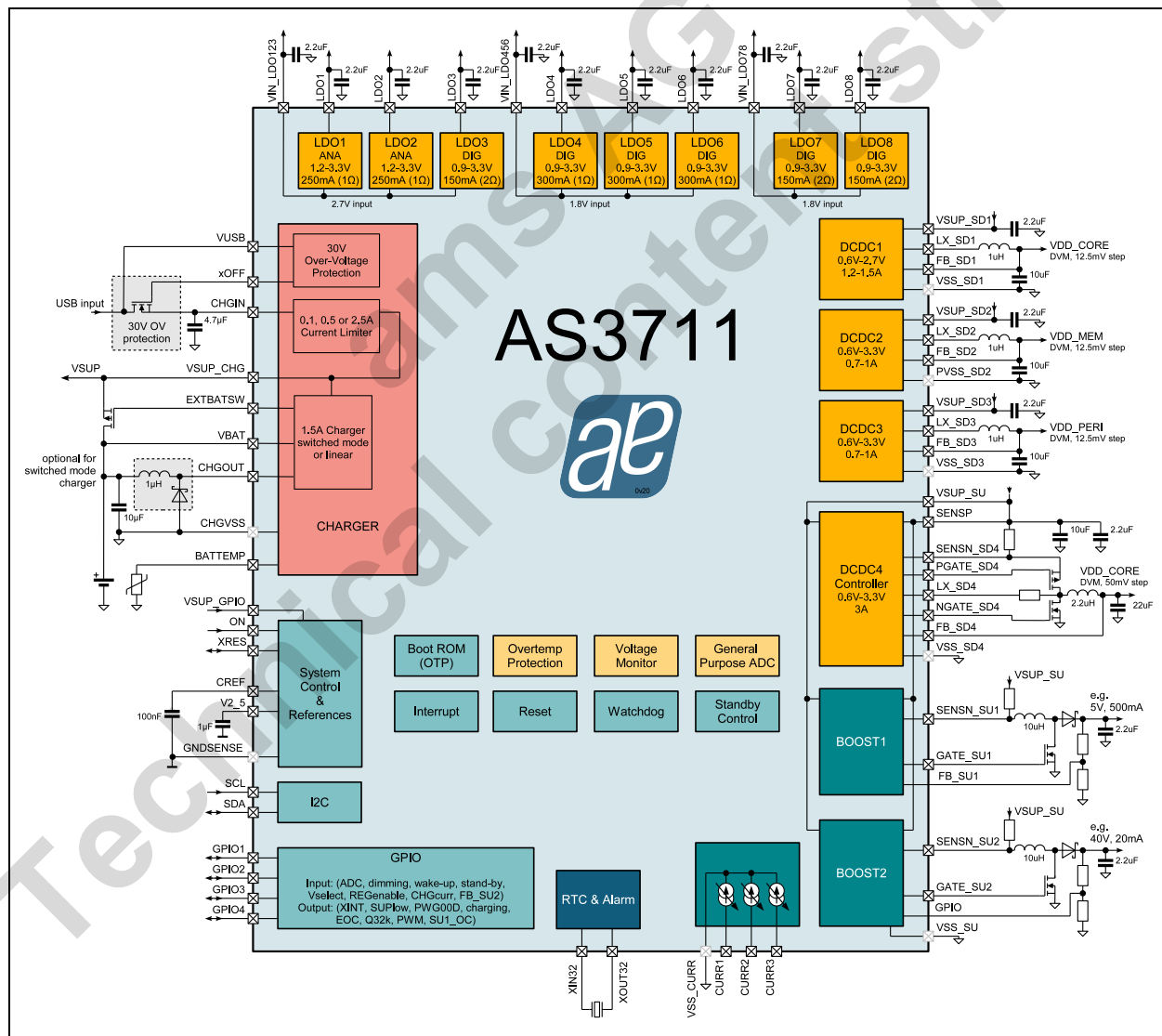
### Packaging

QFN56 7x7mm 0.4mm pitch

## 3 Application

The device is suitable for Portable Media Players, Portable Navigation Devices, E-Books, Mobile Internet Devices, and Tablet PCs.

Figure 1. AS3711 Block Diagram

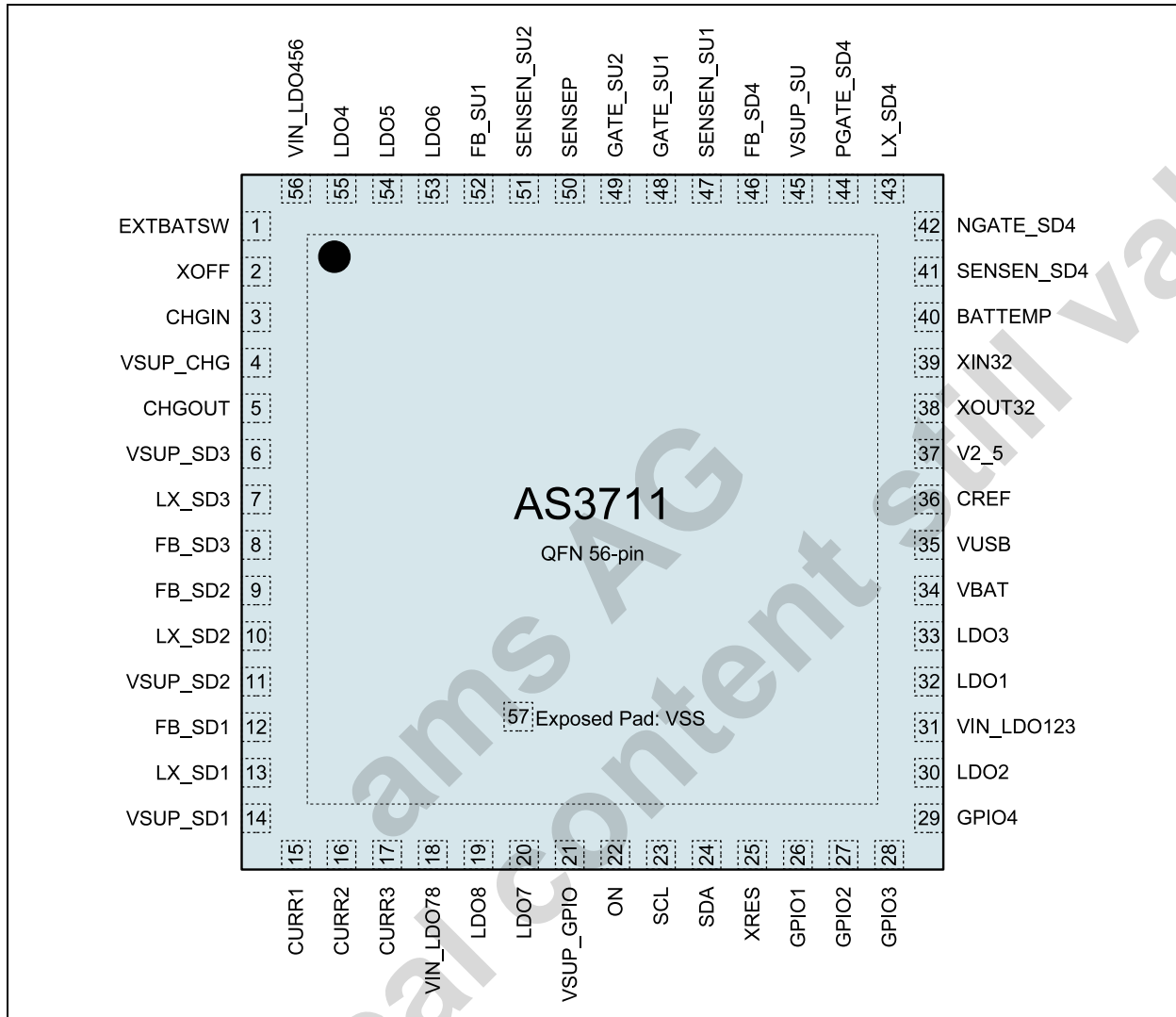


## Contents

|      |   |     |
|------|---|-----|
| 1    | General Description                               | 1   |
| 2    | Key Features                                      | 1   |
| 3    | Application                                       | 2   |
| 4    | Pin Assignments                                   | 4   |
| 4.1  | Pin Descriptions                                  | 4   |
| 5    | Absolute Maximum Ratings                          | 7   |
| 6    | Electrical Characteristics                        | 8   |
| 7    | Typical Operating Characteristics                 | 9   |
| 8    | Detailed Description - Power Management Functions | 10  |
| 8.1  | DCDC Step-Down Converter                          | 10  |
| 8.2  | DCDC Step-Down Controller                         | 16  |
| 8.3  | Analog LDO Regulators                             | 19  |
| 8.4  | Digital LDO Regulators                            | 21  |
| 8.5  | Low power LDO V2_5 Regulators                     | 23  |
| 8.6  | DCDC Step-Up Converter                            | 24  |
| 8.7  | Current Sinks                                     | 30  |
| 8.8  | Charger   | 31  |
| 9    | Detailed Description - System Functions           | 39  |
| 9.1  | Start-up  | 39  |
| 9.2  | Reset   | 41  |
| 9.3  | Stand-by  | 43  |
| 9.4  | Internal References                               | 44  |
| 9.5  | GPIO Pins   | 45  |
| 9.6  | Supervisor  | 48  |
| 9.7  | Watchdog  | 49  |
| 9.8  | Interrupt Generation                              | 50  |
| 9.9  | 10-Bit ADC  | 51  |
| 9.10 | Real Time Clock                                   | 53  |
| 9.11 | 2-Wire-Serial Control Interface                   | 54  |
| 10   | Register Overview                                 | 56  |
| 11   | Application Information                           | 95  |
| 12   | Package Drawings and Markings                     | 98  |
| 13   | Ordering Information                              | 101 |

## 4 Pin Assignments

Figure 2. Pin Assignments (Top View)



## 4.1 Pin Descriptions

Table 1. Pin Descriptions

| Pin Number | Pin Name<br>AS3711 | Pin Type | Description  | if not used   |
|------------|--------------------|----------|--|---------------|
| 1          | EXTBATSW           | ANA OUT  | External Battery Switch Gate Driver Output                 | open          |
| 2          | XOFF               | ANA OUT  | External OV NMOS Gate Driver Output                        | open          |
| 3          | CHGIN              | SUP IN   | Wall adapter or USB Bus Power Input (after protection)     | open          |
| 4          | VSUP_CHG           | SUP IO   | Current Limiter Output, Charger Input, connect to VSUPx    | always needed |
| 5          | CHGOUT             | ANA OUT  | Linear and DCDC Charger output                             | open          |
| 6          | VSUP_SD3           | SUP IN   | DCDC Step Down 3 Pos. Supply Terminal                      | always needed |
| 7          | LX_SD3             | DIG OUT  | DCDC Step Down 3 Switch Output to Coil                     | open          |
| 8          | FB_SD3             | ANA IN   | DCDC Step Down 3 Feedback Pin                              | open          |
| 9          | FB_SD2             | ANA IN   | DCDC Step Down 2 Feedback Pin                              | open          |
| 10         | LX_SD2             | DIG OUT  | DCDC Step Down 2 Switch Output to Coil                     | open          |
| 11         | VSUP_SD2           | SUP IN   | DCDC Step Down 2 Pos. Supply Terminal                      | always needed |
| 12         | FB_SD1             | ANA IN   | DCDC Step Down 1 Feedback Pin                              | open          |
| 13         | LX_SD1             | DIG OUT  | DCDC Step Down 1 Switch Output to Coil                     | open          |
| 14         | VSUP_SD1           | SUP IN   | DCDC Step Down 1 Pos. Supply Terminal                      | always needed |
| 15         | CURR1              | ANA IO   | Load Current Sink 1 Terminal                               | open          |
| 16         | CURR2              | ANA IO   | Load Current Sink 2 Terminal                               | open          |
| 17         | CURR3              | ANA IO   | Load Current Sink 3 Terminal                               | open          |
| 18         | VINLDO78           | SUP IN   | LDO 7 & 8 Positive Supply Terminal, connect to VSUP_CHG    | always needed |
| 19         | LDO8               | ANA OUT  | LDO8 Output  | open          |
| 20         | LDO7               | ANA OUT  | LDO7 Output  | open          |
| 21         | VSUP_GPIO          | SUP IN   | GPIO Positive Supply Terminal, connect to VSUP_CHG         | always needed |
| 22         | ON                 | DIG IN   | Power Up Input   | open          |
| 23         | SCL                | DIG IN   | 2-wire Serial IF Clock Input                               | open          |
| 24         | SDA                | DIG IO   | 2-wire Serial IF Data I/O                                  | open          |
| 25         | XRES               | DIG IO   | Reset IO   | open          |
| 26         | GPIO1              | ANA IO   | General Purpose IO 1                                       | open          |
| 27         | GPIO2              | ANA IO   | General Purpose IO 2                                       | open          |
| 28         | GPIO3              | ANA IO   | General Purpose IO 3                                       | open          |
| 29         | GPIO4              | ANA IO   | General Purpose IO 4                                       | open          |
| 30         | LDO2               | ANA OUT  | LDO2 Output  | open          |
| 31         | VINLDO123          | SUP IN   | LDO 1, 2 & 3 Positive Supply Terminal, connect to VSUP_CHG | always needed |
| 32         | LDO1               | ANA OUT  | LDO1 Output  | open          |
| 33         | LDO3               | ANA OUT  | LDO3 Output  | open          |
| 34         | VBAT               | SUP IO   | Li-Ion Battery Terminal                                    | open          |
| 35         | VUSB               | SUP IN   | Wall adapter or USB Bus Power Input (before protection)    | open          |
| 36         | CREF               | ANA IO   | Reference Bypass Capacitor Terminal                        | always needed |

Table 1. Pin Descriptions

| Pin Number | Pin Name<br>AS3711 | Pin Type | Description  | if not used   |
|------------|--------------------|----------|--|---------------|
| 37         | V2_5               | ANA OUT  | Internal 2.5V Regulator Supply Output                          | always needed |
| 38         | XOUT32             | ANA OUT  | RTC 32kHz Crystal Drive Terminal                               | open          |
| 39         | XIN32              | ANA IN   | RTC 32kHz Crystal Feedback Terminal                            | open          |
| 40         | BATTEMP            | ANA IO   | Li-Ion Battery Charger Temperature Sensor Input                | open          |
| 41         | SENSEN_SD4         | ANA IN   | DCDC Step Down 4 Negative Sense Resistor Input                 | open          |
| 42         | NGATE_SD4          | ANA OUT  | DCDC Step Down 4 ext. NMOS Gate Driver Output                  | open          |
| 43         | LX_SD4             | ANAIN    | DCDC Step Down 4 Sense Input                                   | open          |
| 44         | PGATE_SD4          | ANA OUT  | DCDC Step Down 4 ext. PMOS Gate Driver Output                  | open          |
| 45         | VSUP_SU            | SUP IN   | DCDC Step Down 4 Positive Supply Terminal, connect to VSUP_CHG | always needed |
| 46         | FB_SD4             | ANA IN   | DCDC Step Down 4 Feedback Pin                                  | open          |
| 47         | SENSEN_SU1         | ANA IN   | DCDC Step Up 1 Negative Sense Resistor Input                   | open          |
| 48         | GATE_SU1           | ANA OUT  | DCDC Step Up 1 ext. NMOS Gate Driver Output                    | open          |
| 49         | GATE_SU2           | ANA OUT  | DCDC Step Up 2 ext. NMOS Gate Driver Output                    | open          |
| 50         | SENSEP             | ANA IN   | DCDC Step Up 1, 2 & Step Down 4 Positive Sense Resistor Input  | open          |
| 51         | SENSEN_SU2         | ANA IN   | DCDC Step Up 2 Negative Sense Resistor Input                   | open          |
| 52         | FB_SU1             | ANA IN   | DCDC Step Up 1 Feedback Pin                                    | open          |
| 53         | LDO6               | ANA OUT  | LDO6 Output  | open          |
| 54         | LDO5               | ANA OUT  | LDO5 Output  | open          |
| 55         | LDO4               | ANA OUT  | LDO4 Output  | open          |
| 56         | LDO456             | SUP IN   | LDO 4, 5 & 6 Positive Supply Terminal, connect to VSUP_CHG     | always needed |

## 5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Electrical Characteristics on page 8](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

| Symbol  | Parameter                         | Min  | Max  | Unit | Comments   |
|---|-----------------------------------|------|------|------|--|
| <b>Electrical Parameters</b>                                |                                   |      |      |      |  |
|   | 5V pins                           | -0.5 | 7.0  | V    | Applicable for pins VSUP_CHG, VSUP_SD1/2/3, VSUP_SU, VSUP_GPIO, VIN_LDO123/456/78, GPIO1/2/3/4, GATE_SU1/2, NGATE_SD4, PGATE_SD4, FB_SU1, SENSEP, SENSEN_SU1/2, SENSEN_SD4, VBAT, LDO1/2/3/4/5/6/7/8, FB_SD1/2/3/4, LX_SD1/2/3/4, XRES, SCL, SDA |
|   | 3V pins                           | -0.5 | 5.0  | V    | Applicable for pins V2_5, CREF, ON, BATTEMP, XIN32, XOUT32   |
|   | 30V pins                          | -0.5 | 32   | V    | Applicable for pin VUSB, XOFF, CURR1/2/3   |
|   | Input Current (latch-up immunity) | -100 | 100  | mA   | Norm: JEDEC JESD78   |
| <b>Continuous Power Dissipation (T<sub>A</sub> = +70°C)</b> |                                   |      |      |      |  |
| P <sub>T</sub>  | Continuous power dissipation      |      | 1.8  | W    | P <sub>T</sub> <sup>1</sup> for QFN56 package (R <sub>TH</sub> ~ 30K/W)  |
| <b>Electrostatic Discharge</b>                              |                                   |      |      |      |  |
|   | Electrostatic Discharge HBM       |      | ±1.5 | kV   | Norm: JEDEC JESD22-A114F   |
| <b>Temperature Ranges and Storage Conditions</b>            |                                   |      |      |      |  |
| T <sub>AMB</sub>  | Operating Temperature             | -40  | +85  | °C   |  |
| T <sub>J</sub>  | Junction Temperature              |      | +125 | °C   |  |
|   | Storage Temperature Range         | -55  | +150 | °C   |  |
|   | Humidity non-condensing           | 5    | 85   | %    |  |
| <b>Temperature (soldering)</b>                              |                                   |      |      |      |  |
| T <sub>BODY</sub>   | Package Body Temperature          |      | 260  | °C   | Norm IPC/JEDEC J-STD-020 <sup>2</sup><br>The lead finish for Pb-free leaded packages is matte tin (100% Sn)  |
|   | Moisture Sensitive Level          |      | 3    |      | Represents a max. floor life time of 168h  |

1. Depending on actual PCB layout and PCB used
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices"



## 6 Electrical Characteristics

VSUPx=+2.7V...+5.5V, T<sub>A</sub>=-40°C...+85°C. Typical values are at VSUPx=+3.6V, T<sub>A</sub>=+25°C, unless otherwise specified.

The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 3. Electrical Characteristics

| Symbol                 | Parameter                       | Condition                     | Min | Typ | Max | Unit |
|------------------------|---------------------------------|-------------------------------|-----|-----|-----|------|
| VUSB                   | Charger HV Input                |                               | 0   | 5   | 30  | V    |
| CHGIN                  | Charger LV Input                |                               | 0   | 5   | 5.5 | V    |
| VSUPx                  | Supply Voltage<br>VSUP_x        |                               | 2.7 | 3.6 | 5.5 | V    |
| VINLDO123              | Supply Voltage for LDO 1, 2 & 3 |                               | 2.7 | 3.6 | 5.5 | V    |
| VINLDO456              | Supply Voltage for LDO 4, 5 & 6 |                               | 1.8 | 3.6 | 5.5 | V    |
| VINLDO78               | Supply Voltage for LDO 7 & 8    |                               | 1.8 | 3.6 | 5.5 | V    |
| V2_5                   | Voltage on Pin V2_5             |                               | 2.4 | 2.5 | 2.6 | V    |
| I <sub>low_power</sub> | Low Power current               | @ VSUPx = 4.2V                |     | 220 |     | μA   |
| I <sub>power_off</sub> | Power-Off current               | All regulators off<br>V2_5 on |     | 10  |     | μA   |

## 7 Typical Operating Characteristics

please see operating characteristics in the block description chapters.

ams AG  
Technical content still valid

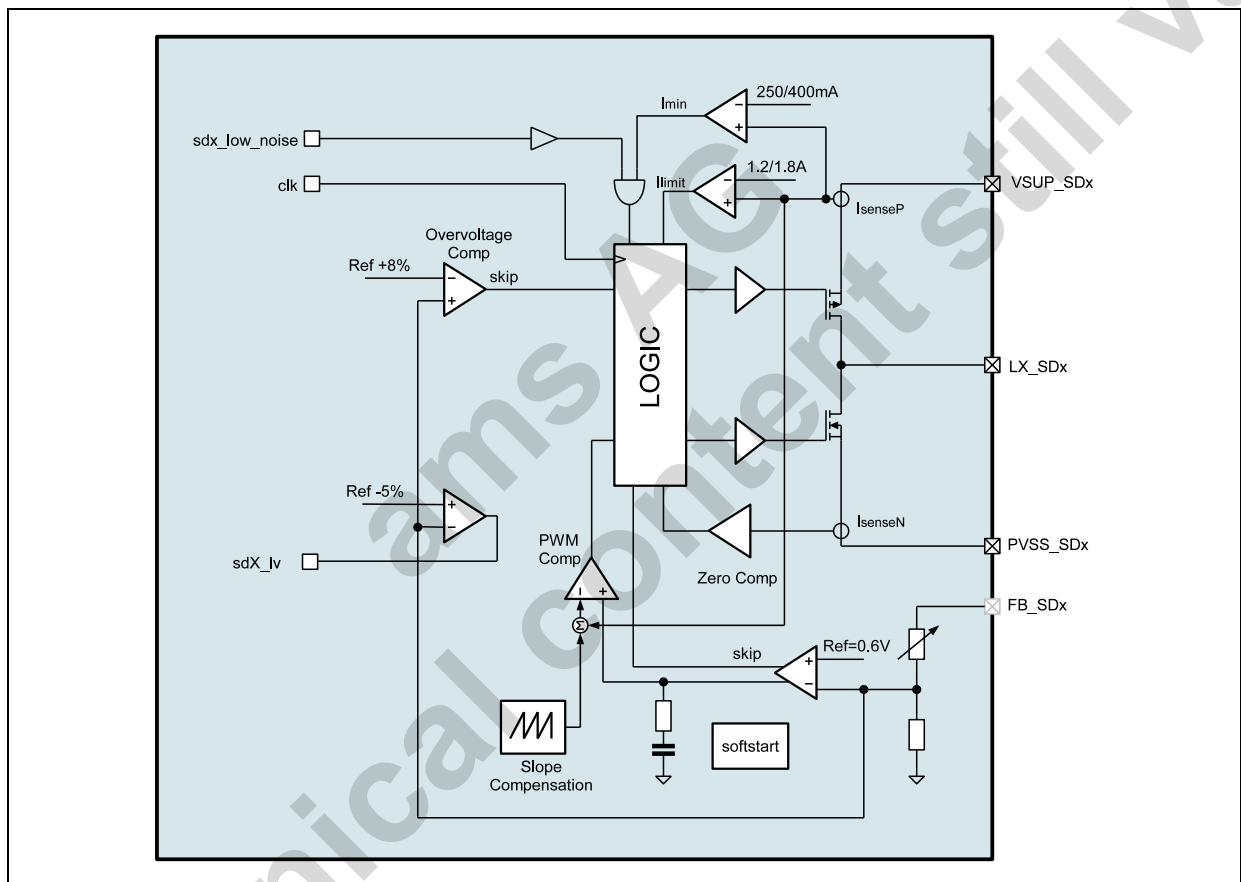
## 8 Detailed Description - Power Management Functions

### 8.1 DCDC Step-Down Converter

#### 8.1.1 General Description

The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 1A (SD2, SD3) and 1.5A for SD1, with an output capacitor of only 10 $\mu$ F. The implemented current limitation protects the DCDC and the coil during overload condition.

Figure 3. Step Down DC/DC Converter Block diagram



#### 8.1.2 Mode Settings

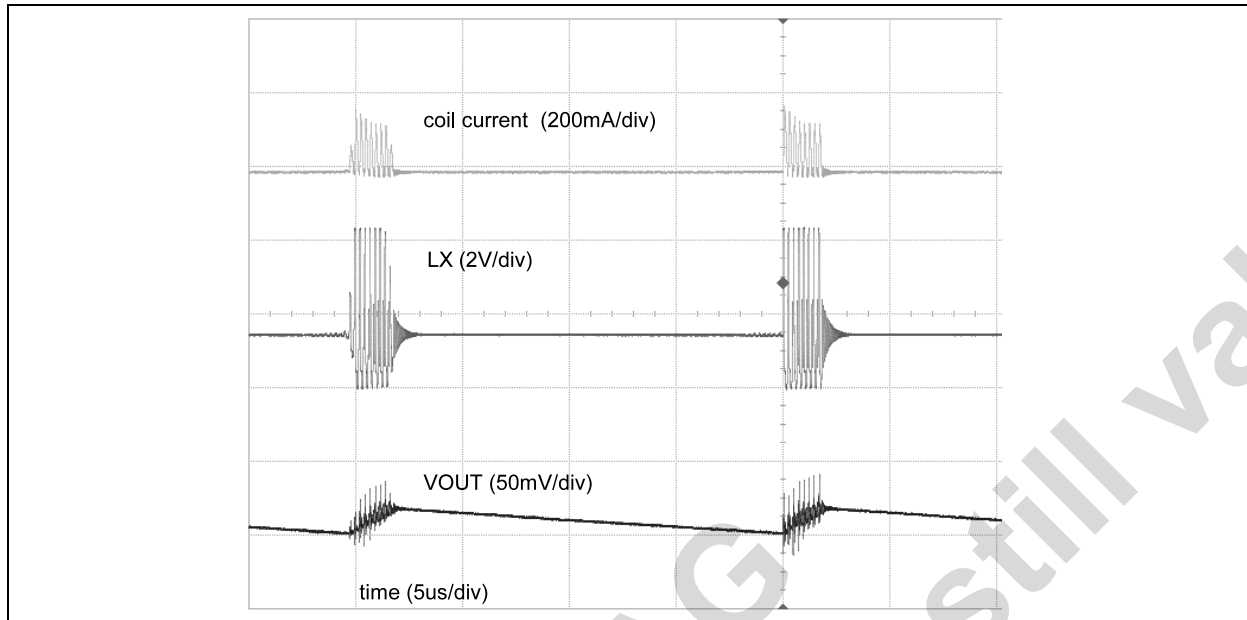
*Low ripple, low noise operation:*

Bit settings: sdx\_low\_noise=1

In this mode there is no minimum coil current necessary before switching off the PMOS. As long as the load current is superior to the ripple current the device operates in continuous mode. When the load current gets lower, the discontinuous mode is triggered. As result, the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to  $t_{min\_on}$  to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences.

Only in the case the load current gets so small that less than the minimum on-time of the PMOS would be needed to keep the loop in regulation the regulator will enter low power mode operation. The crossover point is about 15mA for  $V_{in}=3V$ ,  $V_{out}=1.2V$ , 1 $\mu$ H, 4MHz.

Figure 4. DCDC Buck with enabled low noise mode

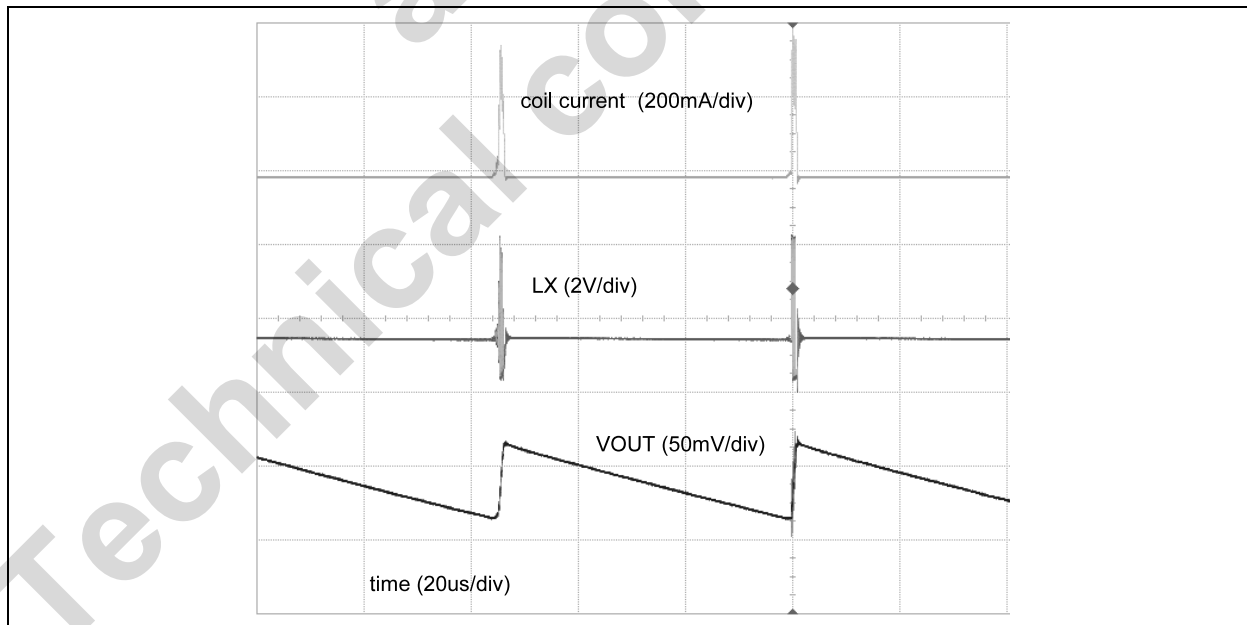
*High efficiency operation (default setting):*

Bit settings: sdX\_low\_noise=0

In this mode there is a minimum coil current necessary before switching off the PMOS. As a result there are less pulses necessary at low output loads, and therefore the efficiency at low output load is increased. As drawback this mode increases the ripple up to a higher output currents.

The crossover point to low power mode is already reached at reasonable high output currents. (e.g. @110mA for  $V_{in}=3V$ ,  $V_{out}=1.2V$ ,  $1\mu H$ ,  $4MHz$ )

Figure 5. DCDC Buck with disabled low noise mode



It's possible to switch between these two modes during operation:

### Low power mode operation (automatically controlled):

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two addition guard bands, based on comparators, are set at +/-5% of the target value to react quickly on large over/undershoots by immediately turning on the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

### DVM (Dynamic Voltage Management)

To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

DVM can be selected for all step-down converters, but only for one at a time. (see `sd_dvm_select` and `dvm_time` description)

### Fast Regulation Mode

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs an 22uF output capacitor instead the 10uF one to guarantee the stability of the regulator. the mode is enabled by setting `sdX_fast = 1`.

### Selectable Frequency Operation

Especially for very low load conditions, e.g. during a sleep mode of a processor, the switching frequency can be reduced to achieve a higher efficiency. The frequency for SD1, SD2 and SD3 can be set to 2, 3 or 4MHz. This mode is selected by setting `sdX_freq` and `sdX_fsel` to the appropriate values.

### 100% PMOS ON Mode for Low Dropout Regulation

For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is then in LDO mode.

## 8.1.3 Step-Down Converter Configuration Modes

The step down DCDC converters have two configuration modes to deliver different output currents for the applications. The operating mode is selected by setting the bit `sd3_slave` (the default is set by the Boot-OTP).

Figure 6. DC/DC step-down SD1, SD2, SD3 Normal Operating Mode; `sd3_slave = 0`

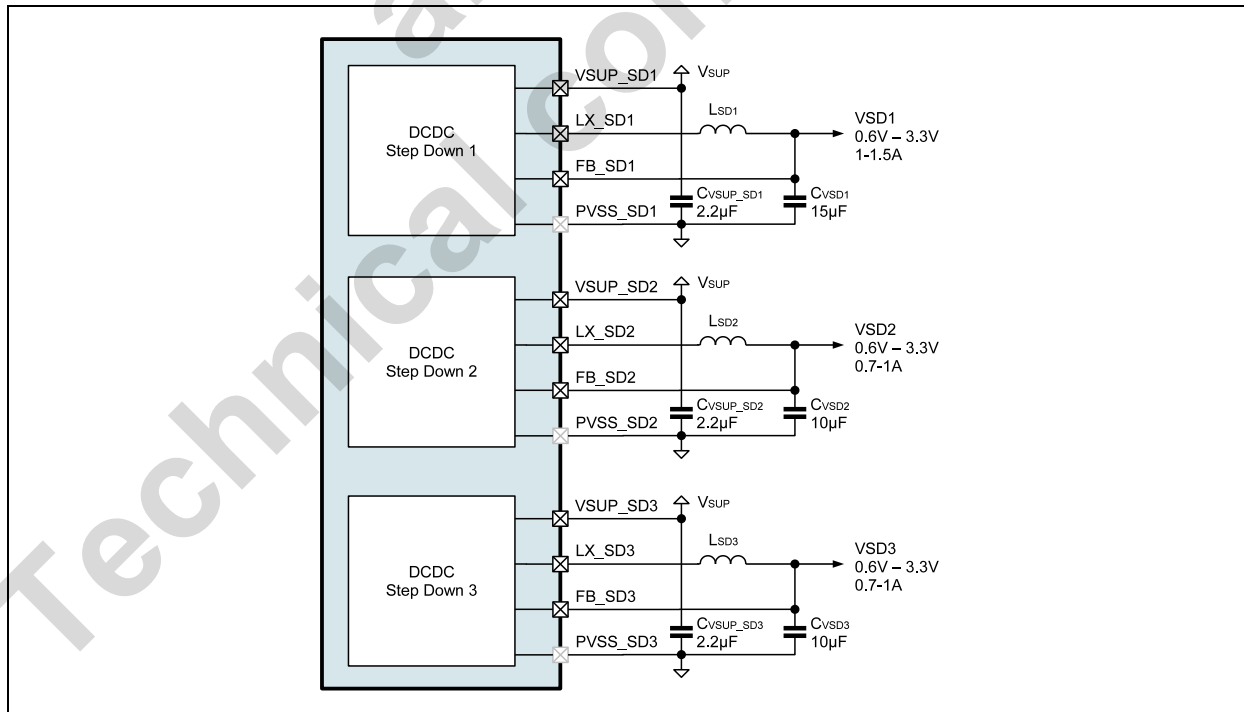
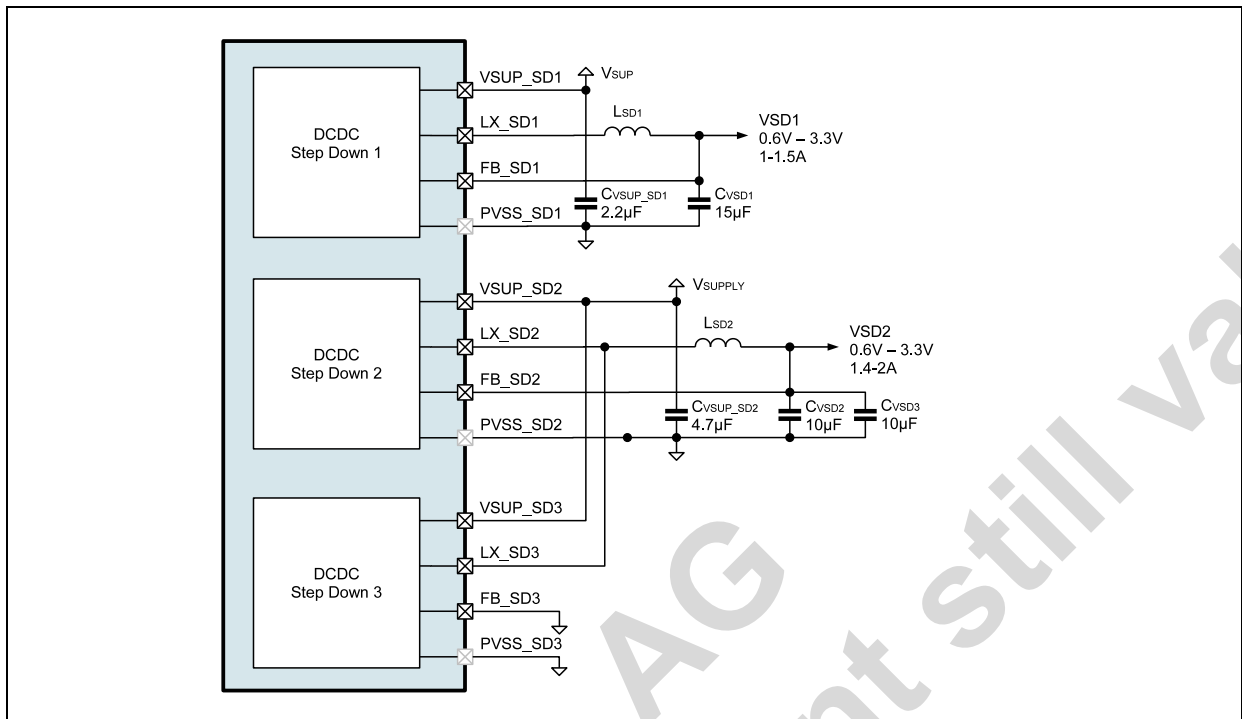


Figure 7. DC/DC step-down SD1, SD2, SD3 2A Operating Mode; *sd3\_slave* = 1

### 8.1.4 Parameter

Table 4. Step Down DC/DC Converter Parameters

| Symbol   | Parameter                | Note                                    | Min    | Typ  | Max  | Unit |
|----------|--------------------------|---|--------|------|------|------|
| VIN      | Input voltage            | Pin VSUP_SDx                            | 2.7    |      | 5.5  | V    |
| VOUT     | Regulated output voltage |   | 0.6125 |      | 3.35 | V    |
| VOUT_tol | Output voltage tolerance | min. 40mV                               | -3     |      | +3   | %    |
| ILIMIT   | Current limit            | SD1                                     |        | 1.8  |      | A    |
|          |                          | SD2, SD3                                |        | 1.2  |      | A    |
| RPSW     | P-Switch ON resistance   | SD1; VSUP_SDx=3.0V                      |        | 0.17 | 0.4  | Ω    |
|          |                          | SD2, SD3; VSUP_SDx=3.0V                 |        | 0.25 | 0.5  | Ω    |
| RNSW     | N-Switch ON resistance   | SD1; VSUP_SDx=3.0V                      |        | 0.17 | 0.4  | Ω    |
|          |                          | SD2, SD3; VSUP_SDx=3.0V                 |        | 0.25 | 0.5  | Ω    |
| Iload    | Load current             | SD1                                     | 0      |      | 1.5  | A    |
|          |                          | SD2, SD3                                | 0      |      | 1    | A    |
| fsw      | Switching frequency      | sdX_frequ=1, sdX_fsel=1; fclk_int =4MHz |        | 4    |      | MHz  |
|          |                          | sdX_frequ=1, sdX_fsel=0; fclk_int =4MHz |        | 3    |      | MHz  |
|          |                          | sdX_frequ=0, sdX_fsel=0; fclk_int =4MHz |        | 2    |      | MHz  |
| tmin_on  | minimum on time          |   |        | 40   |      | ns   |
| ηeff     | Efficiency               | Iout=300mA, Vout=2V, VSUP=3.5V          |        | 92   |      | %    |
| IVDD     | Current consumption      | Operating current without load          |        | 60   |      | µA   |
|          |                          | Shutdown current                        |        | 0.1  |      |      |

Table 5. Step Down DC/DC External Components

| Symbol      | Parameter        | Note                            | Min  | Typ | Max | Unit |
|-------------|------------------|---------------------------------|------|-----|-----|------|
| CFB_SD1     | Output capacitor | Ceramic X5R or X7R              | 10.0 | 15  |     | μF   |
|             |                  | Ceramic X5R or X7R, fast mode=1 | 20.0 | 30  |     | μF   |
| CFB_SD2-3   | Output capacitor | Ceramic X5R or X7R              | 8.0  | 10  |     | μF   |
|             |                  | Ceramic X5R or X7R, fast mode=1 | 16.0 | 20  |     | μF   |
| CVSUP_SD1-3 | Input capacitor  | Ceramic X5R or X7R              |      | 2.2 |     | μF   |
| LSD1-SD3    | Inductor         | 4MHz operation                  |      | 1   |     | μH   |
|             |                  | 3MHz operation                  |      | 1   |     |      |
|             |                  | 2MHz operation                  |      | 2.2 |     |      |

All measurements were done with 55mΩ chip coils (Murata LQM2HPN1R0MG0). Using coils with lower on-resistance will increase the efficiency especially at higher output currents.

Figure 8. Step Down DC/DC SD1 Efficiency vs. Output Current;  $V_{SUP} = 3.0V$ , 3MHz operation,  $T_A = +25^\circ C$

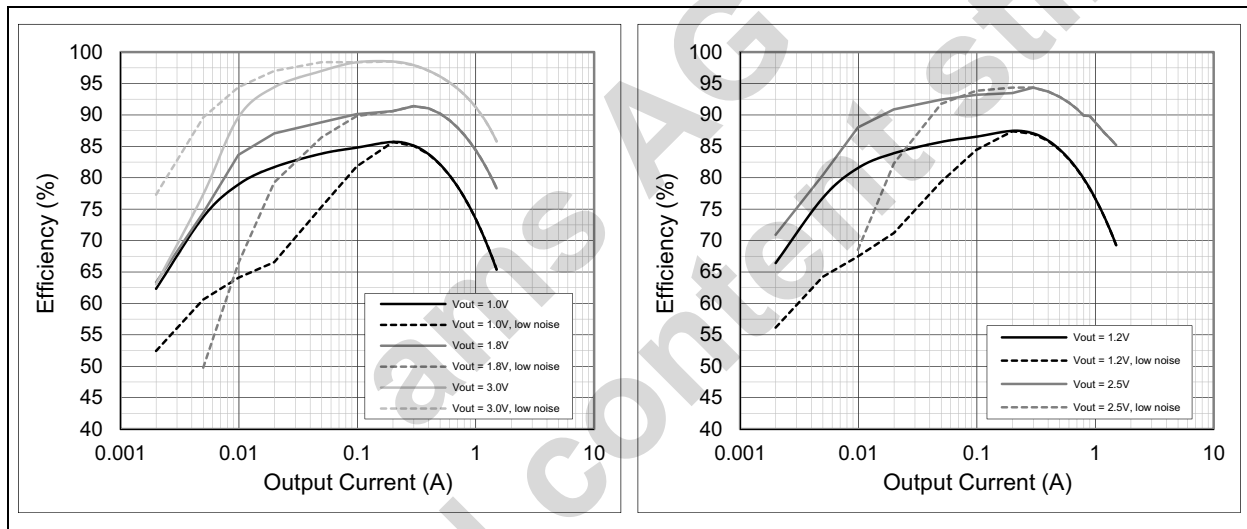


Figure 9. Step Down DC/DC SD1 Efficiency vs. Output Current;  $V_{SUP} = 3.8V$ , 3MHz operation,  $T_A = +25^\circ C$

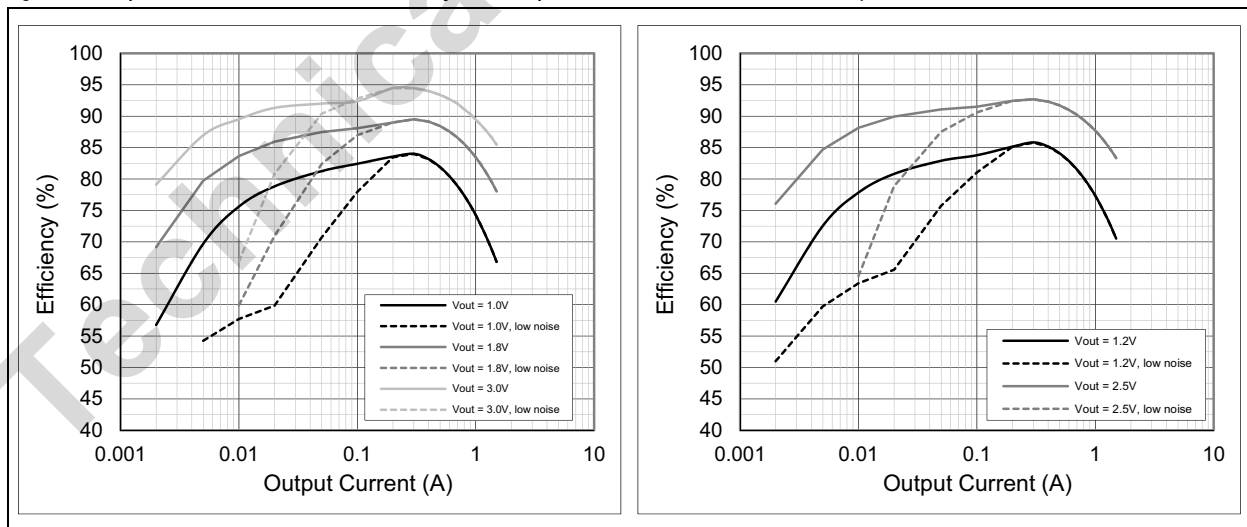


Figure 10. Step Down DC/DC SD2 & SD3 Efficiency vs. Output Current;  $V_{SUP} = 3.0V$ , 3MHz operation,  $T_A = +25^\circ C$

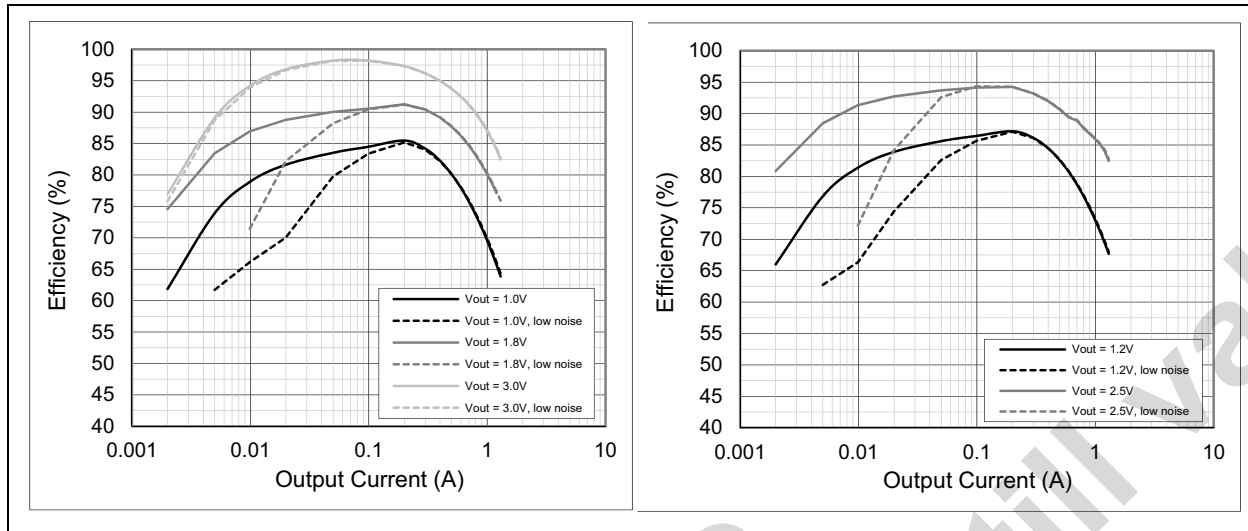
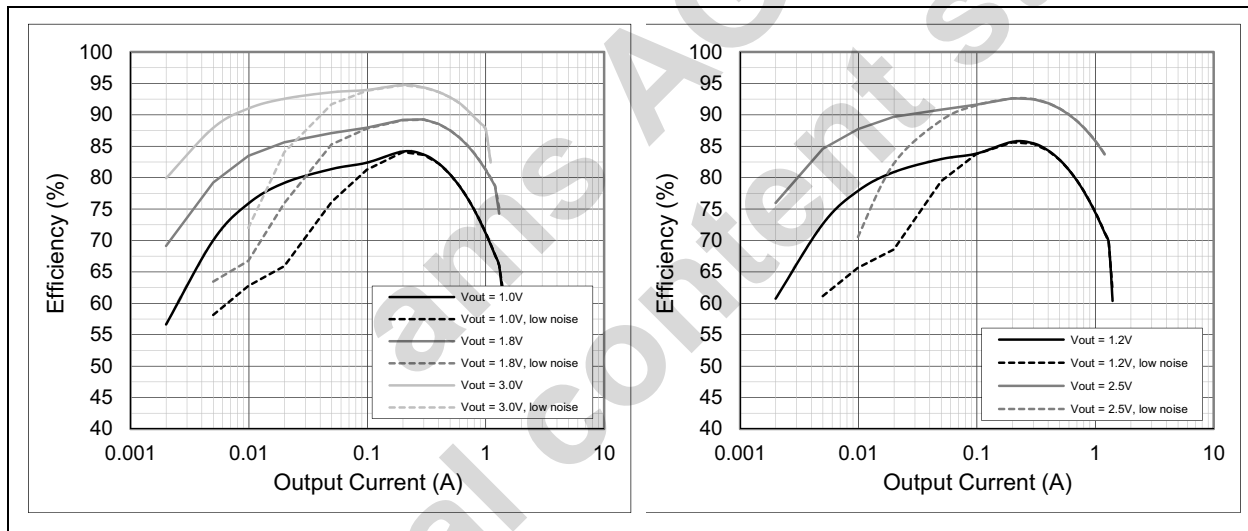


Figure 11. Step Down DC/DC SD2 & SD3 Efficiency vs. Output Current;  $V_{SUP} = 3.8V$ , 3MHz operation,  $T_A = +25^\circ C$



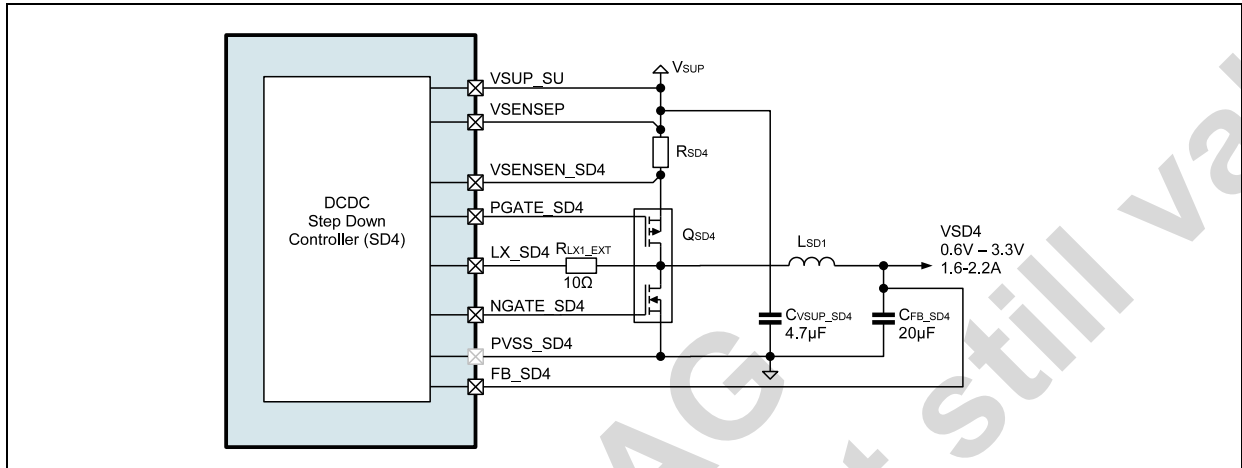


## 8.2 DCDC Step-Down Controller

### 8.2.1 General Description

The Step-Down controller SD4 uses a paired external NMOS, PMOS to achieve higher output currents. the maximum output current is determined by the external transistor and shunt used.

Figure 12. DC/DC step-down Controller



### 8.2.2 Parameter

Table 6. Step Down DC/DC Controller Parameters

| Symbol                  | Parameter                                   | Note                                 | Min    | Typ | Max | Unit |
|-------------------------|---|--------------------------------------|--------|-----|-----|------|
| VIN                     | Input voltage                               | Pin VSUP_SDx                         | 2.7    |     | 5.5 | V    |
| VOUT                    | Regulated output voltage                    |                                      | 0.6125 |     | 3.3 | V    |
| VOUT_tol                | Output voltage tolerance                    | min. 40mV                            | -3     |     | +3  | %    |
| V <sub>rsense_max</sub> | Current limit voltage at R <sub>sense</sub> | E.g.: 2.6A for 0.033Ω sense resistor |        | 100 |     | mV   |
| f <sub>sw</sub>         | Switching frequency                         | fclk_int = 4MHz                      |        | 1   |     | MHz  |

Table 7. Step Down DC/DC Controller External Components

| Symbol                          | Parameter        | Note                            | Min  | Typ | Max | Unit   |
|---------------------------------|------------------|---------------------------------|------|-----|-----|--|
| <b>External Components 1.6A</b> |                  |                                 |      |     |     |  |
| QSD4                            | paired NMOS-PMOS | FDC6327C                        |      |     |     | PMOS: Ron=250mOhm, 1.6A<br>NMOS: Ron=120mOhm, 2.7A |
| RSD4                            | shunt            | 0.15W; +/- 1%                   |      | 50  |     | mΩ   |
| CFB_SD4                         | Output capacitor | Ceramic X5R or X7R              | 16.0 | 20  |     | μF   |
|                                 |                  | Ceramic X5R or X7R, fast mode=1 | 32.0 | 40  |     | μF   |
| CVSUP_SD4                       | Input capacitor  | Ceramic X5R or X7R              |      | 10  |     | μF   |
| LSD4                            | Inductor         | 2A rated, 1MHz operation        |      | 2.2 |     | μH   |
| <b>External Components 2.2A</b> |                  |                                 |      |     |     |  |
| QSD4                            | paired NMOS-PMOS | FDC6420C                        |      |     |     | PMOS: Ron=190mOhm, 2.2A<br>NMOS: Ron=95mOhm, 3A    |
| RSD4                            | shunt            | 0.2W; +/- 1%                    |      | 33  |     | mΩ   |

Table 7. Step Down DC/DC Controller External Components

| Symbol                        | Parameter        | Note                             | Min  | Typ | Max | Unit   |
|-------------------------------|------------------|----------------------------------|------|-----|-----|--|
| CFB_SD4                       | Output capacitor | Ceramic X5R or X7R               | 24.0 | 30  |     | $\mu\text{F}$                                    |
|                               |                  | Ceramic X5R or X7R, fast mode=1  | 48.0 | 60  |     | $\mu\text{F}$                                    |
| CVSUP_SU                      | Input capacitor  | Ceramic X5R or X7R               |      | 10  |     | $\mu\text{F}$                                    |
| LSD4                          | Inductor         | 2.5A rated, 1MHz operation       |      | 1.5 |     | $\mu\text{H}$                                    |
| <b>External Components 3A</b> |                  |                                  |      |     |     |  |
| QSD4                          | paired NMOS-PMOS | NTHD3102C                        |      |     |     | PMOS: Ron=83mOhm, 4.2A<br>NMOS: Ron=37mOhm, 5.5A |
| RSD4                          | shunt            | 0.3W; +/- 1%                     |      | 25  |     | m $\Omega$                                       |
| CFB_SD4                       | Output capacitor | Ceramic X5R or X7R               | 32.0 | 40  |     | $\mu\text{F}$                                    |
|                               |                  | Ceramic X5R or X7R, fast mode =1 | 64.0 | 80  |     | $\mu\text{F}$                                    |
| CVSUP_SU                      | Input capacitor  | Ceramic X5R or X7R               |      | 10  |     | $\mu\text{F}$                                    |
| LSD4                          | Inductor         | 3A rated, 1MHz operation         |      | 1   |     | $\mu\text{H}$                                    |

All measurements were done with the 2.2A transistors (Fairchild FDC6420C) and 70m $\Omega$  chip coils (Murata LQM2HPN1R0MG0). Using coils with lower on-resistance will increase the efficiency especially at higher output currents.

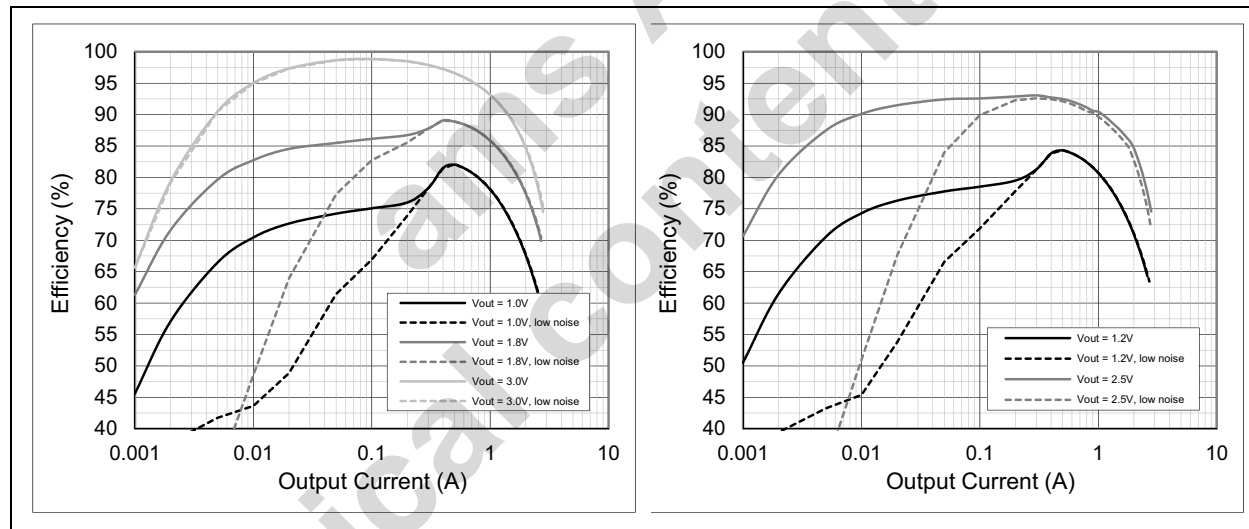
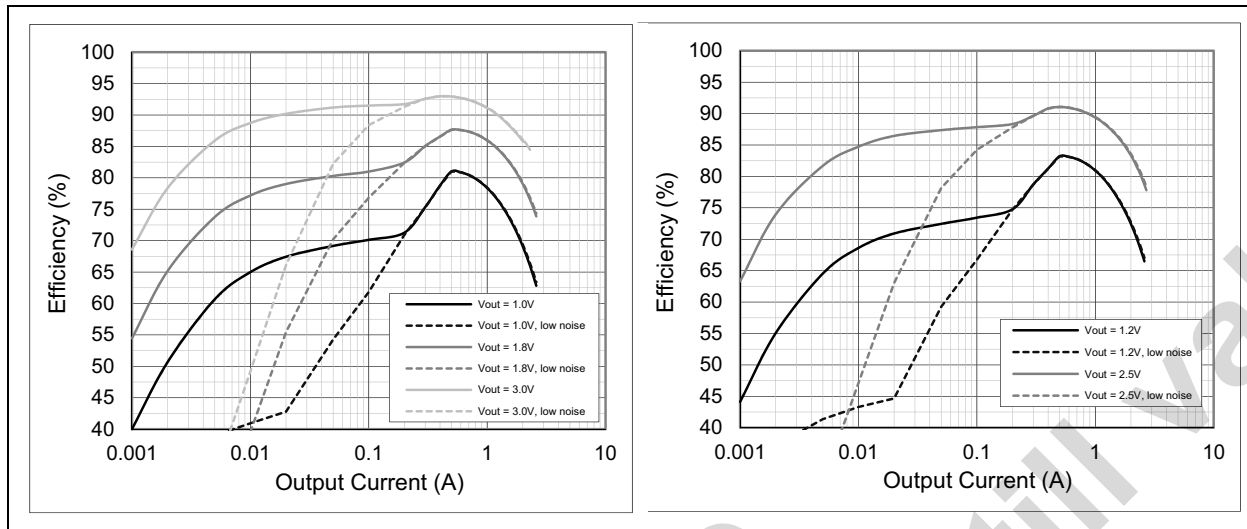
Figure 13. Step-Down DC/DC SD4 Controller Efficiency vs. Output Current;  $V_{SUP} = 3.0V$ ,  $T_A = +25^\circ\text{C}$ 

Figure 14. Step-Down DC/DC SD4 Controller Efficiency vs. Output Current;  $V_{SUP} = 3.8V$ ,  $T_A = +25^\circ C$



## 8.3 Analog LDO Regulators

### 8.3.1 General description

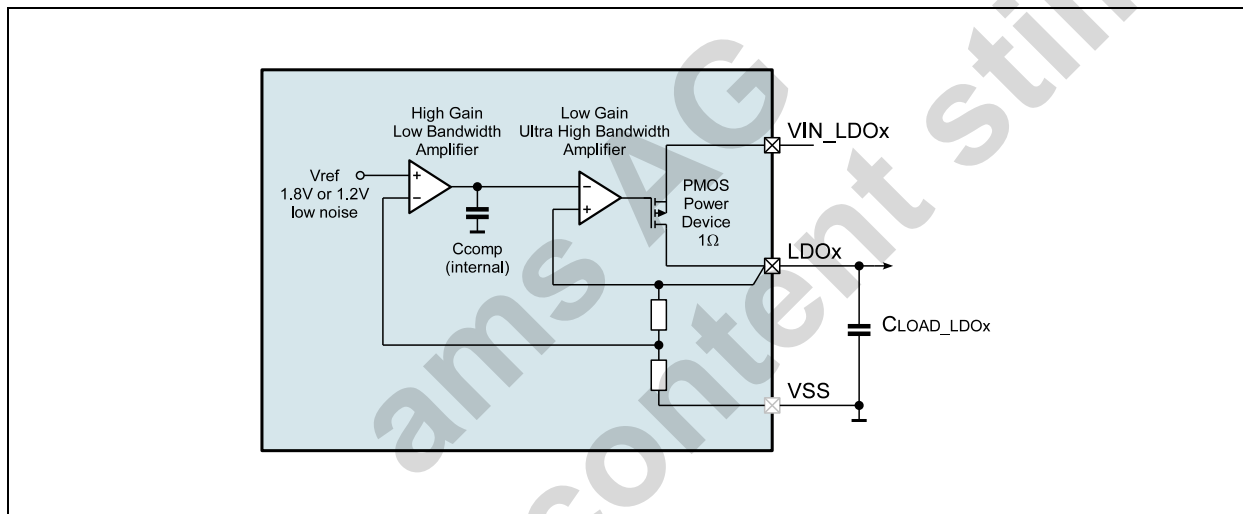
LDO1 and LDO2 are designed to supply sensitive analogue circuits like LNA's, Transceivers, VCO's and other critical RF components of cellular radios. Another application is the supply of audio devices or as a reference for AD and DA converters. The design is optimized to deliver the best compromise between quiescent current and regulator performance for battery powered devices.

Stability is guaranteed with ceramic output capacitors of  $1\mu\text{F} \pm 20\%$  (X5R) or  $2.2\mu\text{F} +100/-50\%$  (Z5U). The low ESR of these caps ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress the PA-ripple on the battery in TDMA systems at the output. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power device enables the device to deliver up to IOUT current even at nearly discharged batteries without any decrease of performance.

The default guaranteed operating current during start-up is 150mA, but can be set to 250mA with `IdoX_ilimit = 1`.

To save power in low-power states where the full performance is not needed the bias current can be reduce by setting `reg_low_bias_mode=1`.

Figure 15. Analog LDO Block diagram



### 8.3.2 Parameter

Table 8. Analog LDO (LDO1, LDO2) Characteristics

$V_{LDO123\_IN}=3.7\text{V}$ ;  $I_{LOAD}=150\text{mA}$ ;  $T_{amb}=25^\circ\text{C}$ ;  $C_{LOAD}=2.2\mu\text{F}$  (Ceramic); unless otherwise specified

| Symbol             | Parameter                    | Note   | Min | Typ | Max | Unit              |
|--------------------|------------------------------|--|-----|-----|-----|-------------------|
| VLDO123_IN         | Supply voltage range         |  | 2.7 |     | 5.5 | V                 |
| IOUT               | Output current <sup>1</sup>  | I <sub>doX</sub> _ilimit = 0                   | 0   |     | 150 | mA                |
|                    |                              | I <sub>doX</sub> _ilimit = 1                   | 0   |     | 250 |                   |
| R <sub>ON</sub>    | On resistance                | LDO1, LDO2                                     |     |     | 1   | Ω                 |
| PSRR               | Power supply rejection ratio | f=1kHz   | 70  |     |     | dB                |
|                    |                              | f=100kHz                                       | 40  |     |     |                   |
| I <sub>OFF</sub>   | Shut down current            |  |     |     | 100 | nA                |
| I <sub>VDD</sub>   | Supply current               | without load                                   |     | 50  |     | μA                |
|                    |                              | without load, <code>reg_low_bias_mode=1</code> |     | 30  |     | μA                |
| Noise              | Output noise                 | 10Hz < f < 100kHz                              |     |     | 50  | μV <sub>rms</sub> |
| t <sub>start</sub> | Startup time                 | low current limit used during start-up         |     |     | 200 | μs                |

Table 8. Analog LDO (LDO1, LDO2) Characteristics

$V_{LDO123\_IN}=3.7V$ ;  $I_{LOAD}=150mA$ ;  $T_{amb}=25^{\circ}C$ ;  $C_{LOAD}=2.2\mu F$  (Ceramic); unless otherwise specified

| Symbol                 | Parameter                | Note                               | Min | Typ | Max | Unit    |
|------------------------|--------------------------|------------------------------------|-----|-----|-----|---------|
| $V_{out}$              | Output voltage           |                                    | 1.2 |     | 3.3 | V       |
| $V_{out\_tol}$         | Output voltage tolerance | min. 40mV                          | -3  |     | 3   | %       |
| $V_{LineReg}$          | Line regulation          | Static                             | -1  |     | 1   | mV      |
|                        |                          | Transient; Slope: $t_r=10\mu s$    | -10 |     | 10  |         |
| $V_{LoadReg}$          | Load regulation          | Static                             | -1  |     | 1   | mV      |
|                        |                          | Transient; Slope: $t_r=10\mu s$    | -10 |     | 10  |         |
| $I_{LIMIT\_LDO1,2\_L}$ | low current limit        | $I_{doX\_ilimit} = 0$              |     | 300 |     | mA      |
| $I_{LIMIT\_LDO1,2\_H}$ | high current limit       | $I_{doX\_ilimit} = 1$              |     | 500 |     | mA      |
| $C_{LOAD\_LDO1,2\_L}$  | Ceramic load capacitor   | LDO1 / LDO2; $I_{doX\_ilimit} = 0$ | 1   |     | 5   | $\mu F$ |
| $C_{LOAD\_LDO1,2\_H}$  | Ceramic load capacitor   | LDO1 / LDO2; $I_{doX\_ilimit} = 1$ | 2   |     | 5   | $\mu F$ |

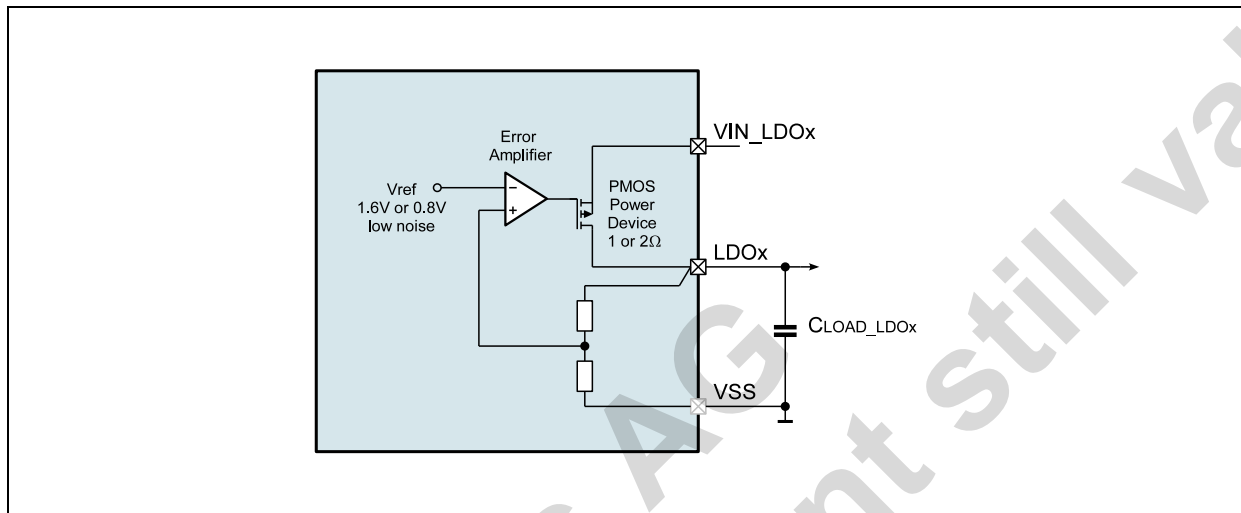
1. Guaranteed by design and verified by laboratory evaluation and characterization; not production tested.

## 8.4 Digital LDO Regulators

### 8.4.1 General Description

Digital LDOs offer a wide input (1.8V to 5.5V) as well as a wide output (0.9 to 3.3V) voltage range to be used for general purpose peripheral supply. Up to 300mA possible output currents are offered with good noise and regulation performance and very low quiescent current even suitable for stand-by power supply.

Figure 16. Digital LDO Block diagram



### 8.4.2 Parameter

Table 9. Digital LDO (LDO3, LDO4, LDO5, LDO6, LDO7, LDO8) Characteristics  
 VLDOx\_IN=3.7V; ILOAD=150mA; Tamb=25°C; CLOAD =1μF (Ceramic); unless otherwise specified

| Symbol     | Parameter                    | Note  | Min  | Typ   | Max | Unit |
|------------|------------------------------|---|------|-------|-----|------|
| VLDO123_IN | Supply voltage range         |   | 2.7  |       | 5.5 | V    |
| VLDO456_IN | Supply voltage range         |   | 1.75 |       | 5.5 | V    |
| VLDO78_IN  | Supply voltage range         |   | 1.75 |       | 5.5 | V    |
| IOUT       | Output current <sup>1</sup>  | I <sub>doX_ilimit</sub> = 0   | 0    |       | 150 | mA   |
|            |                              | I <sub>doX_ilimit</sub> = 1   | 0    |       | 300 | mA   |
| RON        | On resistance                | LDO4, LDO5, LDO6  |      |       | 1   | Ω    |
|            |                              | LDO3, LDO7, LDO8  |      |       | 2   | Ω    |
| PSRR       | Power supply rejection ratio | f=1kHz  | 60   |       |     | dB   |
|            |                              | f=100kHz  | 30   |       |     |      |
| IOFF       | Shut down current            |   |      | 100   |     | nA   |
| IVDD       | Supply current               | without load  |      | 30    | 43  | μA   |
| tstart     | Startup time                 | low current used during start-up  |      |       | 200 | μs   |
| Vout       | Output voltage               | V <sub>supply</sub> >3.0V, V <sub>CP</sub> =5.2V, I <sub>out</sub> <200mA | 0.9  |       | 3.3 | V    |
| Vout_tol   | Output voltage tolerance     | min. 40mV   | -3   |       | 3   | %    |
| VLineReg   | Line regulation              | Static  |      | 0.07  |     | %/V  |
|            |                              | Transient; Slope: tr=15μs; delta 1V                                       |      | 20    |     | mV   |
| VLoadReg   | Load regulation              | Static  |      | 0.014 |     | %/mA |
|            |                              | Transient; Slope: tr=15μs; 1mA->300mA                                     |      | 30    |     | mV   |

Table 9. Digital LDO (LDO3, LDO4, LDO5, LDO6, LDO7, LDO8) Characteristics  
*VLD0x\_IN=3.7V; ILOAD=150mA; Tamb=25°C; CLOAD =1μF (Ceramic); unless otherwise specified*

| Symbol          | Parameter          | Note            | Min | Typ | Max | Unit |
|-----------------|--------------------|-----------------|-----|-----|-----|------|
| ILIMIT_LDO3-8_L | low current limit  | ldoX_ilimit = 0 |     | 300 |     | mA   |
| ILIMIT_LDO3-8_H | high current limit | ldoX_ilimit = 1 |     | 500 |     | mA   |

1. Guaranteed by design and verified by laboratory evaluation and characterization; not production tested

## 8.5 Low power LDO V2\_5 Regulators

### 8.5.1 General Description

The low power LDO V2\_5 is needed to supply the chip core (analog and digital) of the device. It is designed to get the lowest possible power consumption, and still offering reasonable regulation characteristics. The regulator has two supply inputs selecting automatically the higher one. This gives the possibility to supply the chip core either with the battery or with the charger depending on the conditions. Bulk switch comparators are used to avoid any parasitic current flow. To ensure high PSRR and stability, a low-ESR ceramic capacitor of min. 1 $\mu$ F must be connected to the output.

### 8.5.2 Parameter

Table 10. Low power LDO (V2\_5) Characteristics, V<sub>BAT</sub>=3.7V; I<sub>LOAD\_ext</sub>=0; T<sub>amb</sub>=25°C; C<sub>LOAD</sub> = 1  $\mu$ F (Ceramic); unless otherwise specified

| Symbol             | Parameter            | Note   | Min | Typ | Max | Unit     |
|--------------------|----------------------|--|-----|-----|-----|----------|
| V <sub>BAT</sub>   | Supply voltage range |  | 2.7 |     | 5.5 | V        |
| V <sub>USB</sub>   |                      |  | 4.2 |     | 5.5 |          |
| R <sub>ON</sub>    | On resistance        | Guaranteed per design  |     | 50  |     | $\Omega$ |
| I <sub>OFF</sub>   | Shut down current    |  |     | 100 |     | nA       |
| I <sub>VDD</sub>   | Supply current       | Guaranteed per design, consider chip internal load for measurements. |     | 3   |     | $\mu$ A  |
| t <sub>start</sub> | Startup time         |  |     | 200 |     | $\mu$ s  |
| V <sub>out</sub>   | Output voltage       |  | 2.4 | 2.5 | 2.6 | V        |



## 8.6 DCDC Step-Up Converter

### 8.6.1 General Description

The DC/DC Step Up converter is a high efficiency current mode PWM regulator, which provides an output voltage dependent on the maximum VDS voltage of the external transistor, and maximum load current selectable by the external shunt resistor.

For Example:

- 5V, 0.5-1A @ 1MHz
- 25V, 50mA @ 1MHz
- 40V, 20mA @ 500kHz

A constant switching frequency results in a low noise on supply and output voltage.

Figure 17. DC/DC step-up Converter 1

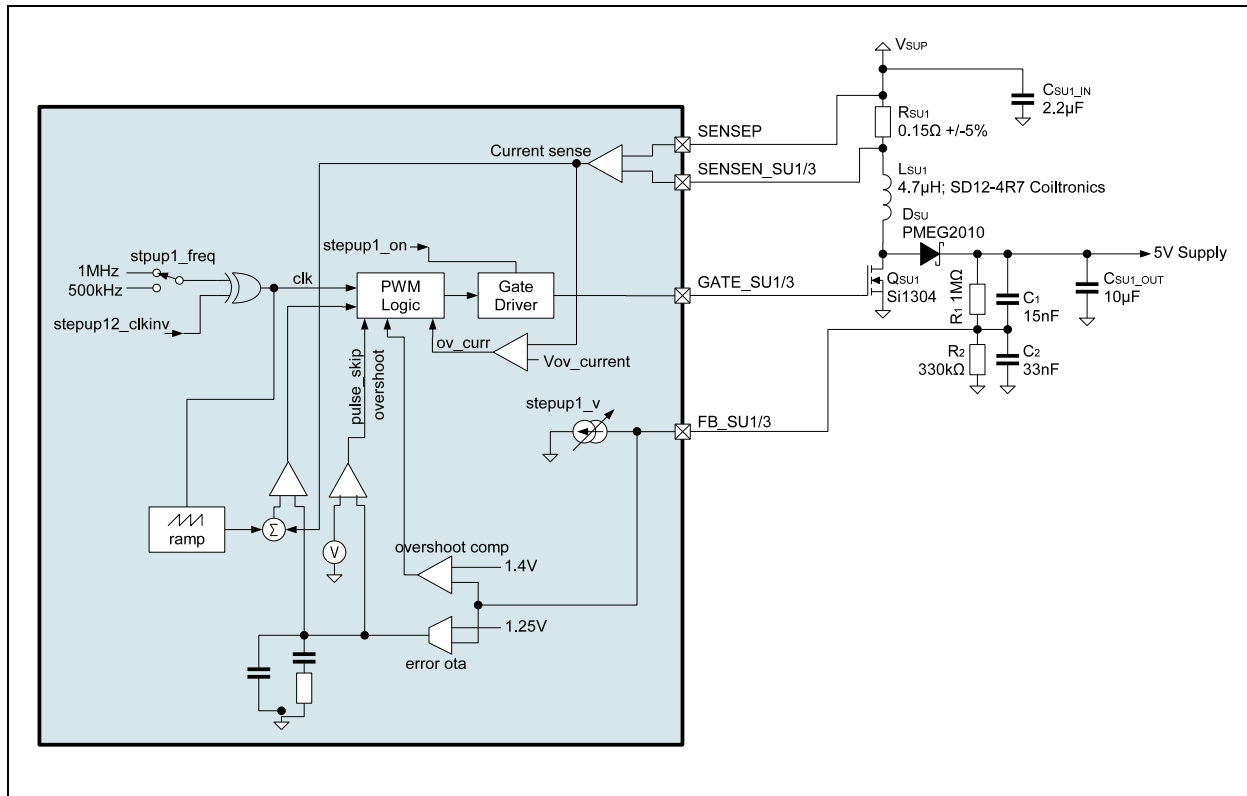
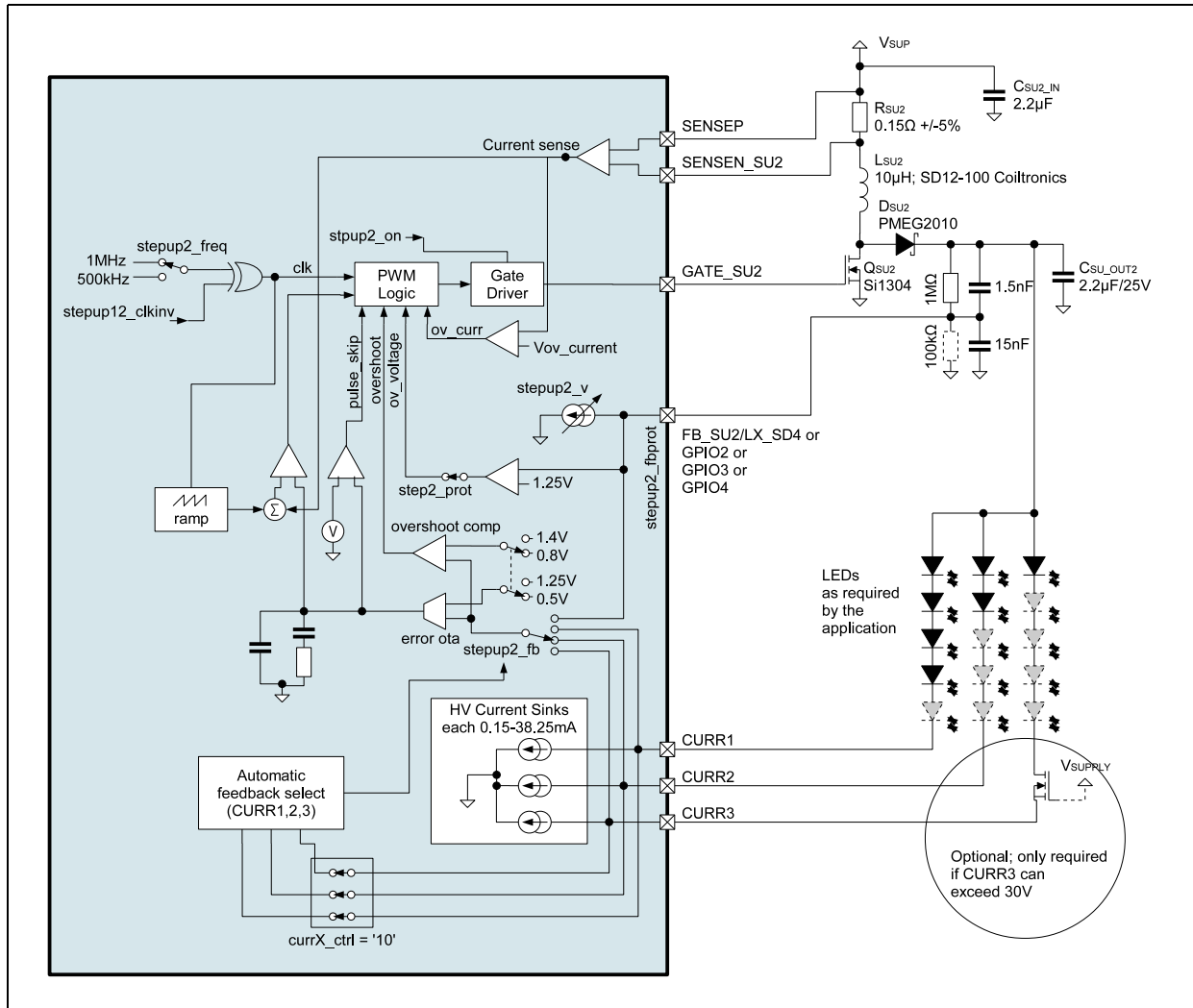


Figure 18. DC/DC step-up Converter 2



### 8.6.2 Feedback selection SU1

For step up SU1, the feedback is always FB\_SU1.

### 8.6.3 Feedback Selection SU2

For step up SU2 following feedback selections are possible (selected by setup2\_fb): (see Figure 18)

#### Current Feedback

CURRE1, CURRE2 or CURRE3 can be selected by **stepup2\_fb** as a current feedback pin.

The step-up converter is regulated such that the required current at the feedback path can be supported. **stepup2\_fbprot** selects the over-voltage protection feedback pin (LX\_SD4, GPIO2, GPIO3 or GPIO4). In this mode the output voltage will be limited by limiting the voltage on the selected feedback pin to 1.25V (select the external resistor network and **stepup2\_v** to adjust this limitation voltage).

**stepup2\_prot\_dis** has to be set to 0, otherwise the protection is disabled.

Always choose the path with the higher voltage drop as feedback to guarantee adequate supply for the other, unregulated path.

#### Current Feedback with Automatic Feedback Selection

Same as above, but when currX\_ctrl = 10b for the used current sinks, the chip automatically selects the highest string (CURRE1, CURRE2 or CURRE3) as feedback input.

### Voltage Feedback

**stepup2\_fb** = 00b. LX\_SD4, GPIO2, GPIO3 or GPIO4 can be selected by **stepup2\_fbprot** as a voltage feedback input.

The step-up converter output voltage is regulated by regulating the selected feedback pin voltage to 1.25V.

### Calculating Resistors for Voltage Feedback or Over-Voltage Protection

Bit **stepupX\_res** should be set to 1 in voltage feedback mode using two resistors.

The output voltage is regulated to a constant value, given by:

$$V_{SU} = \frac{R_1 + R_2}{R_2} \times 1,25 + I_{FB} \times R_1$$

If R2 is not used, the output voltage is:

$$V_{SU} = 1,25 + I_{FB} \times R_1$$

V<sub>SU</sub>: Step up regulator output voltage

R<sub>1</sub> Feedback resistor R1

R<sub>2</sub> Feedback resistor R2

I<sub>FB</sub>: Tuning current on DCDC\_FB pin: stepupX\_v (0..31µA (1µA steps))

Example:

Table 11. Step Up Output Voltage (Voltage mode or protection voltage)

| IFB (stepupX_v) | Vsu                 | Vsu                |
|-----------------|---------------------|--------------------|
| µA              | R1=1M Ω,R2 not used | R1=500k Ω,R2=64k Ω |
| 0               | -                   | 11                 |
| 1               | -                   | 11.5               |
| 2               | -                   | 12                 |
| 3               | -                   | 12.5               |
| 4               | -                   | 13                 |
| 5               | 6.25                | 13.5               |
| 6               | 7.25                | 14                 |
| 7               | 8.25                | 14.5               |
| 8               | 9.25                | 15                 |
| 9               | 10.25               | 15.5               |
| 10              | 11.25               | 16                 |
| 11              | 12.25               | 16.5               |
| 12              | 13.25               | 17                 |
| 13              | 14.25               | 17.5               |
| 14              | 15.25               | 18                 |
| 15              | 16.25               | 18.5               |

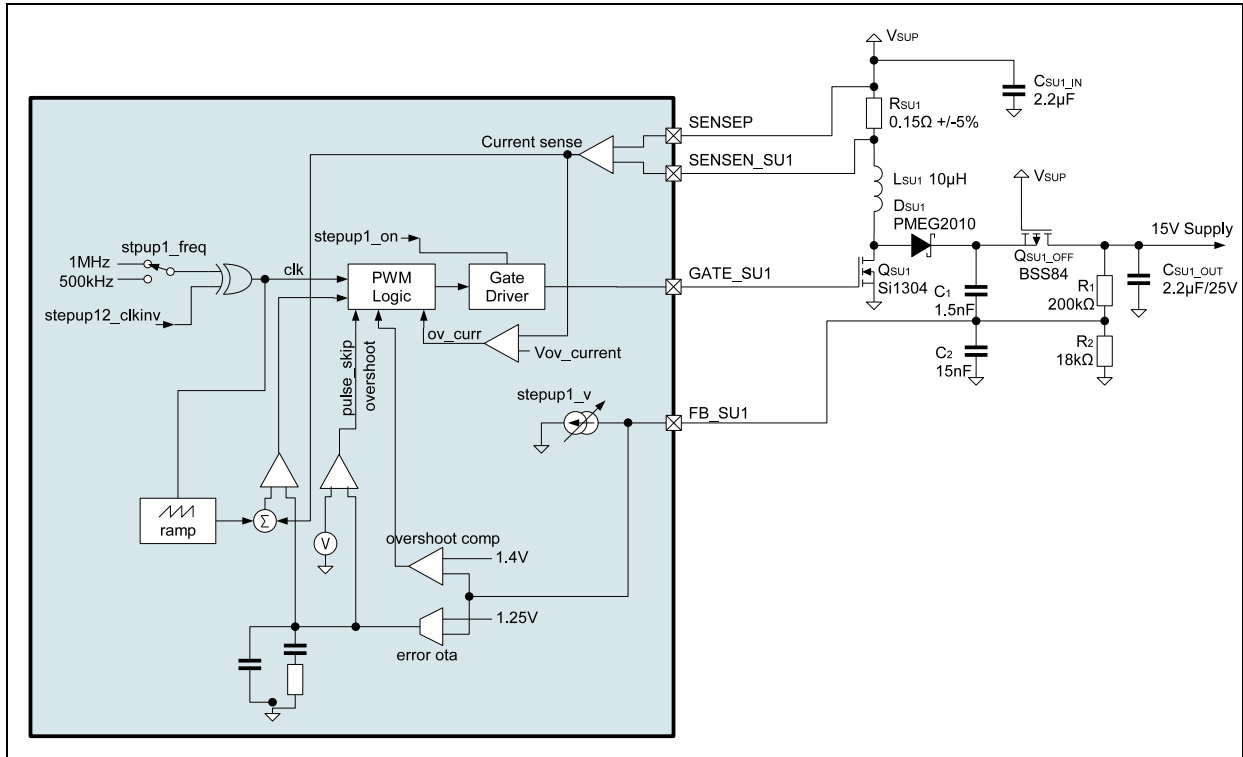
**Note:** The voltage on pin CURR1, CURR2 and CURR3 must never exceed 30V.

### 8.6.4 Output disconnect

As the output voltage is always on, an additional output transistor can be added to reduce shutdown current through R1, R2 and the connected output circuit.

**Note:** A similar circuit can be used for step up converter 2.

Figure 19. StepUp 1 with regulated output voltage (15V), and switch off function of output voltage, to reduce shutdown current



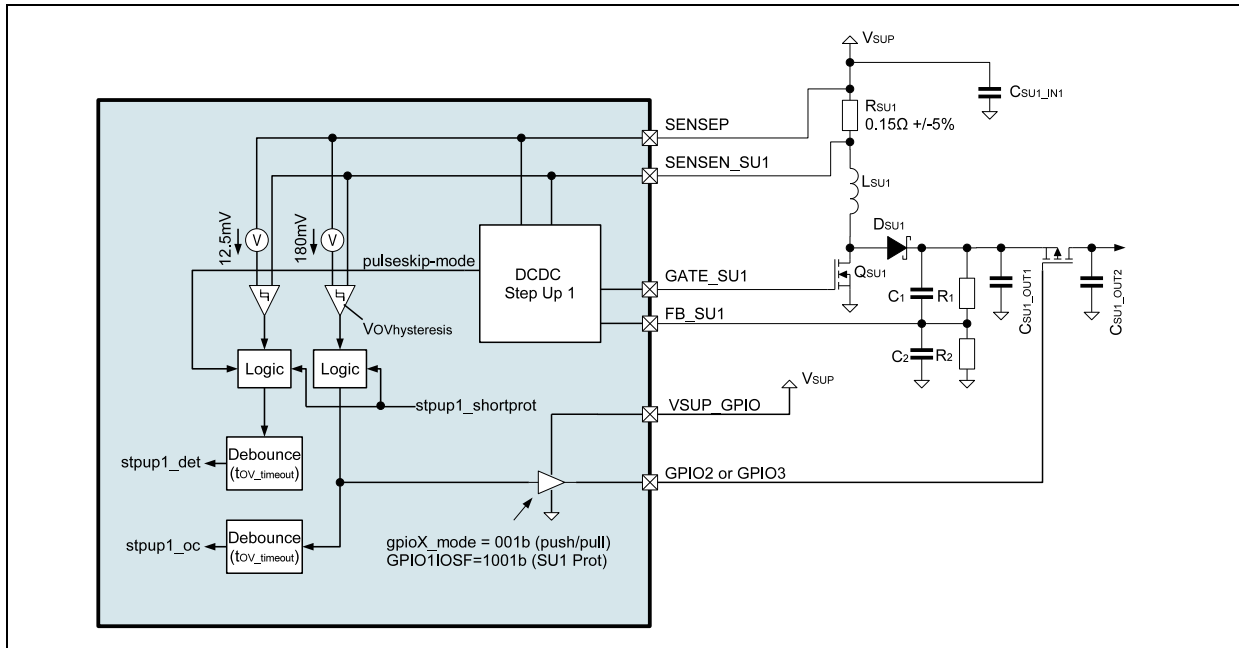
### 8.6.5 StepUp1 Load Detection and Over-current Protection Circuit

This circuit protects the DCDC step up1 converter during short circuit and startup, by regulation of the output current.

An additional feature is the detection of a minimum output load of the Step-up converter. It is also possible to use this circuit without the DCDC step up converter, by using the sense resistor only:

- Detection circuit: If the voltage on  $R_{sense}$  exceeds  $V_{DETECT}$  for more than 1ms, or the DCDC Step up converter is not in pulse-skip for more than 1ms, the `stepup1_det` bit will be set.
- Over-current protection: If the Over-current voltage  $V_{OVCURRENT}$  has been exceeded by more than 5ms the bit `stpup1_oc` will be set and can only reset, by switching off and on the Protection circuit by writing `stpup1_shortprot 0 - 1`. If `stpup1_oc` is set the load will be disconnected, if `stpup1_oc_timeout=1`

Figure 20. StepUp 1 Load Detection and Over-current Protection Application Circuit



### 8.6.6 Parameter

Table 12. DC/DC Step-up Controller Parameters

| Symbol                  | Parameter                                       | Note   | Min  | Typ                     | Max  | Unit |
|-------------------------|---|--|------|-------------------------|------|------|
| I <sub>VDD</sub>        | Quiescent Current                               | Pulse skipping mode                            |      | 140                     |      | μA   |
| V <sub>FB1</sub>        | Feedback voltage for external resistor divider: | for constant voltage control                   | 1.20 | 1.25                    | 1.30 | V    |
| V <sub>FB2</sub>        | Feedback voltage for current sink regulation    | CURR1, CURR2 or CURR3                          |      | 0.6                     |      | V    |
| I <sub>DCDC_FB</sub>    | Additional tuning current at FB_SUX             | adjustable by software in 1 μA steps           | 0    |                         | 31   | μA   |
|                         | Accuracy of feedback current                    | @ full scale                                   | -7   |                         | 7    | %    |
| V <sub>rsense_max</sub> | Current limit voltage at Rsense                 | E.g.: 0.65A for 0.15Ω sense resistor           |      | 100                     |      | mV   |
| R <sub>SW</sub>         | switch resistance                               | ON-resistance of external switching transistor |      |                         | 1    | Ω    |
| I <sub>load</sub>       | Load current                                    | at 25V output voltage                          | 0    |                         | 50   | mA   |
| f <sub>IN</sub>         | Switching frequency                             | internal CLK frequency/4, default 1MHz         |      | f <sub>clk_int</sub> /4 |      | MHz  |
| t <sub>MIN_ON</sub>     | Minimum on time                                 |  |      | 130                     |      | ns   |
| MDC                     | Maximum duty cycle                              | @ 1MHz   |      | 91                      |      | %    |

Table 13. StepUp1 protection/detection circuit parameters

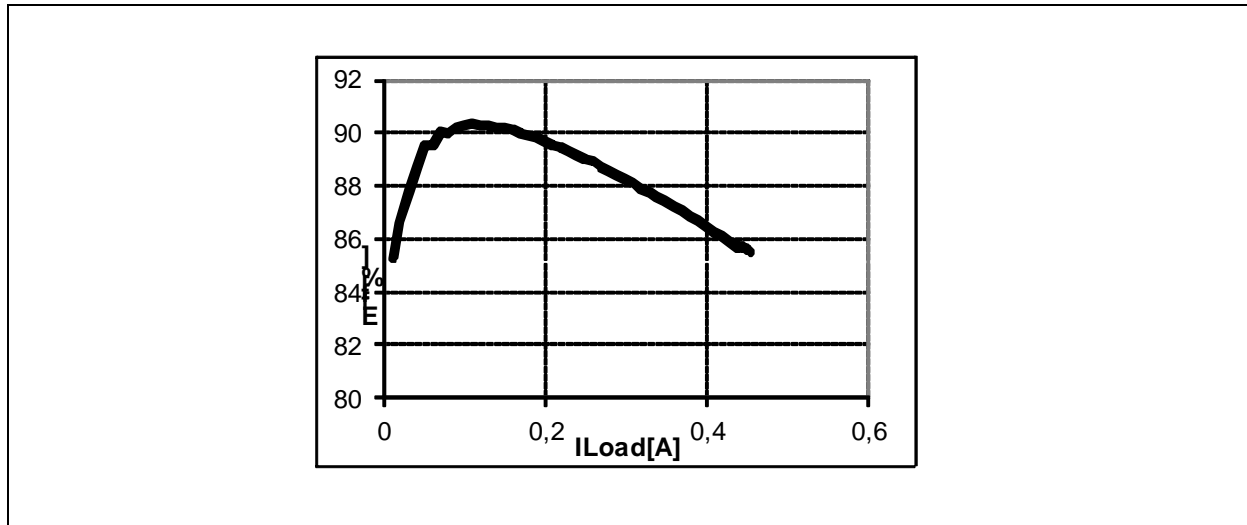
| Symbol              | Parameter                     | Note                           | Min | Typ  | Max | Unit |
|---------------------|-------------------------------|--------------------------------|-----|------|-----|------|
| V <sub>DETECT</sub> | Detection Threshold           | For Rsense=0.150Ω => 83mA typ. | 2   | 12.5 | 25  | mV   |
| VOVCURRENT          | Over-current Threshold rising | For Rsense=0.150Ω => 1.2A typ. | 150 | 180  | 215 | mV   |

Table 13. StepUp1 protection/detection circuit parameters

| Symbol        | Parameter                | Note   | Min | Typ | Max | Unit |
|---------------|--------------------------|--|-----|-----|-----|------|
| VOVhysteresis | Over-current Hysteresis  |  |     | 50  |     | mV   |
| tOV_timeout   | Over-current timeout     | Interrupt and/or external PMOS switching off after timeout<br>$f_{clk\_int} = 2.2\text{MHz}$ |     | 5   |     | ms   |
| tdetect       | Detection de-bounce time | $f_{clk\_int} = 2.2\text{MHz}$   |     | 1   |     | ms   |

Table 14. DC/DC Step-up Controller External Components

| Symbol                          | Parameter                | Note  | Min                       | Typ  | Max                             | Unit          |
|---------------------------------|--------------------------|---|---------------------------|------|---------------------------------|---------------|
| C <sub>out</sub>                | Output capacitor         | ceramic, $\pm 20\%$   |                           | 2.2  |                                 | $\mu\text{F}$ |
| L <sub>SU</sub>                 | Inductor                 | Use inductors with small C <sub>parasitic</sub> (<100pF) to get high efficiency; V <sub>out</sub> >8V   |                           | 10   |                                 | $\mu\text{H}$ |
|                                 |                          | Use inductors with small C <sub>parasitic</sub> (<100pF) to get high efficiency; V <sub>out</sub> <8V   |                           | 4.7  |                                 | $\mu\text{H}$ |
| Q <sub>SU</sub>                 | Transistor               | V <sub>GS(TH)</sub> threshold voltage   |                           | 1.3  | 1.5                             | V             |
|                                 |                          | V <sub>DS</sub> max drain to source voltage   | V <sub>out_max</sub> +20% |      |                                 | V             |
|                                 |                          | R <sub>DS(ON)</sub> drain - source on resistance  |                           | 0.35 |                                 | $\Omega$      |
|                                 |                          | Q <sub>GS</sub> total gate charge @ V <sub>GS</sub> =4.5V   |                           | 3    | 5                               | nC            |
| C <sub>1</sub> / C <sub>2</sub> | Feedback capacitor ratio | ratio should be smaller than the feedback resistor ratio (inverted) to avoid overshoots during start-up |                           |      | R <sub>2</sub> / R <sub>1</sub> | $\mu\text{F}$ |

8.6.7 Step-Up DC/DC Controller Efficiency vs. Output Current; V<sub>SUP</sub> = 3.8V, T<sub>A</sub> = +25°C

## 8.7 Current Sinks

### 8.7.1 General Description

These are general-purpose current sinks intended to control the backlight(s), buzzer and vibrator.

CURR1 and CURR2, CURR3 are high voltage (30V) current sinks, e.g. for series of white LEDs.

Current sinks CURR1, CURR2 and CURR3 can be controlled individually. The step-up DCDC converter (SU2) may supply them with voltages up to 30V. For an automatic feedback selection the used current sinks can be assigned to the SU2 booster.

If not used as a current sink, CURR3 can be used to output several status signals. In this mode the CURR3 output acts like an open-drain output and needs an external pull-up resistor for generating logic high levels.

### 8.7.2 Parameter

Table 15. Current Sinks Characteristics

| Symbol              | Parameter                       | Note   | Min | Typ | Max | Unit    |
|---------------------|---------------------------------|--|-----|-----|-----|---------|
| $I_{CURR1,2,3}$     | CURR1,2 & 3 current, 00h-3Fh    | For $V(DCDC\_CURRx) > 0.5V$<br>resolution = 0.157mA              | 0   |     | 40  | mA      |
| $I_{DCDC\_protect}$ | Current sink protection Current | Protection Current if $stpup2\_on=1$<br>and $currx\_current=00h$ |     | 2   |     | $\mu A$ |
| $\Delta$            | absolute Accuracy               | All Current sinks  | -8  |     | +8  | %       |
| $V_{CURR1,2,3}$     | Voltage compliance              | during normal operation  | 0.5 |     | 30  | V       |

## 8.8 Charger

### 8.8.1 General Description

The AS3711 device serves as a standalone battery charge controller supporting rechargeable lithium ion (Li+) and batteries. Requiring only a few external components, a full-featured battery charger with a high degree of flexibility can easily be realized. The main features of the controller are:

- Charge adapter detection
- PowerPath management & internal voltage regulator (V2\_5), for dead battery startup
- Low current (soft) charging
- Low current (trickle) charging
- Constant current charging
- Constant voltage charging
- 30V Overvoltage protection
- Battery presence indication
- Operation without battery
- Input current limitation
- Input voltage drop regulation
- Programmable linear or switched mode operation
- Bypass mode for high input current application (up to 6A)

Figure 21. Charger Application Block Diagram, Step Down charger mode

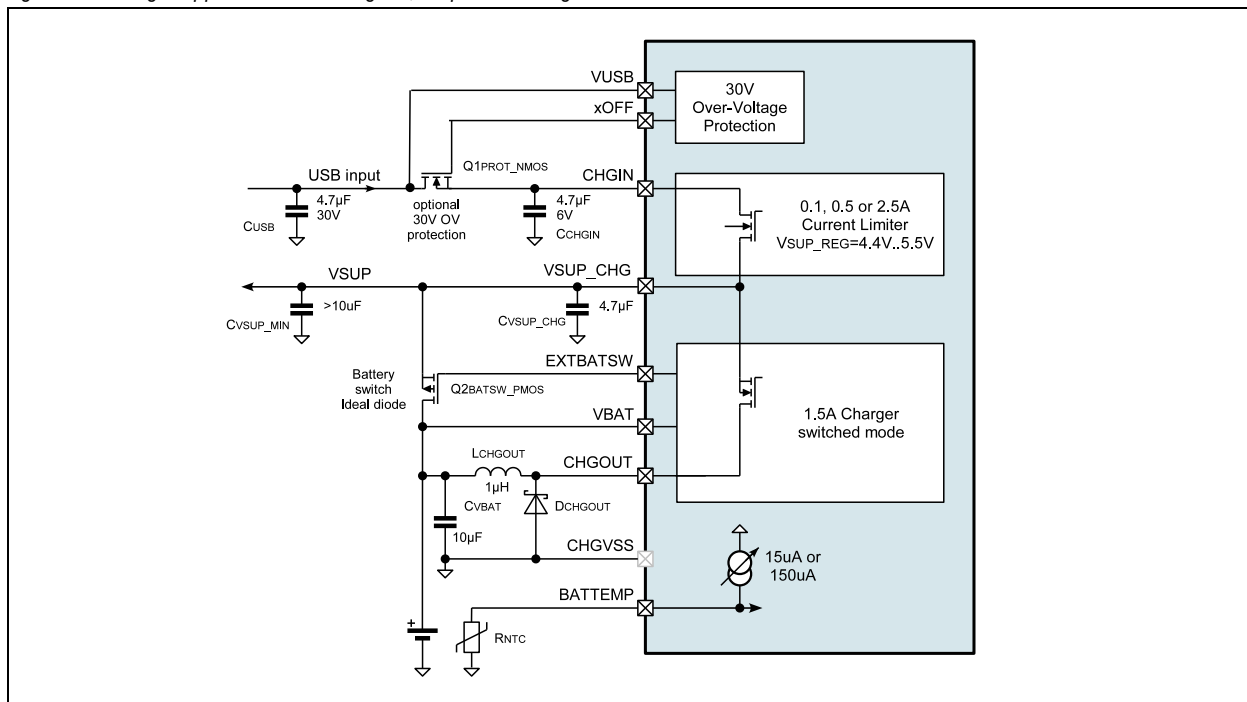
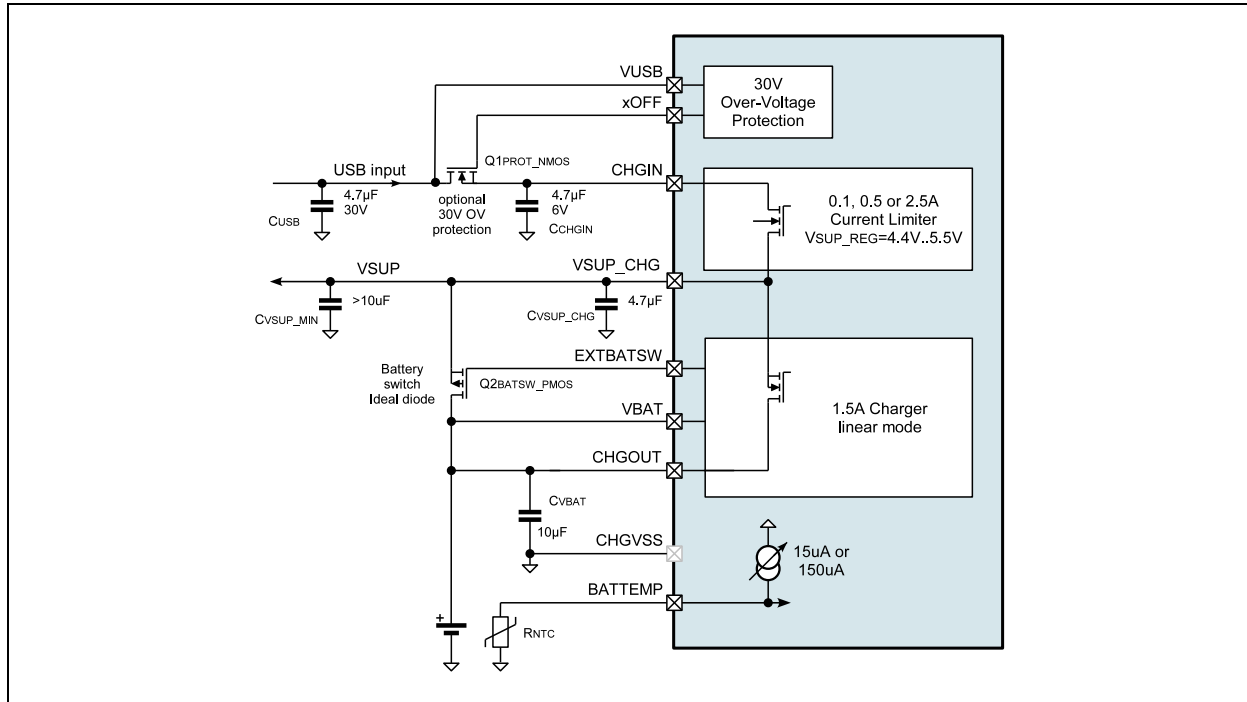




Figure 22. Charger Application Block Diagram, Linear charger mode



## 8.8.2 Charging Cycle Description

### Charge adapter detection

The charge controller uses an integrated detection circuit to determine if an external charge adapter has been applied to the VUSB pin. If the adapter voltage exceeds the battery voltage at pin VBAT by  $V_{CHDET}$  the *ChDet* bit in the *ChargerStatus* register will be set. The detection circuit will reset the charge controller (bit **ChDet** is cleared) as soon as the voltage at the VUSB pin drops to only  $V_{CHMIN}$  above the battery voltage. In case the AS3710AS3711 device is reset the charge controller will also be reset, even if a charge adapter is applied to the VUSB pin.

### Soft charging

Soft charge mode is started when an external charge adapter has been detected, the *bat\_charging\_enable* is set and the battery voltage at pin VBAT is below the  $V_{SOFT}$  threshold.

### Low current (trickle) charging

Trickle charge mode is started when an external charge adapter has been detected *bat\_charging\_enable* is set and the battery voltage at pin VBAT is below the  $V_{TRICKLE}$  threshold and above  $V_{SOFT}$  threshold; bits **ChDet** and **Trickle** will be set in the *ChargerStatus* register. In this mode the charge current will be limited to **TrickleCurrent** (set in the *ChargerCurrent* register) to prevent undue stress in case of deeply discharged batteries. Once  $V_{TRICKLE}$  has been exceeded, the charger will change over to constant current charging (**Trickle** is cleared).

### Constant current charging

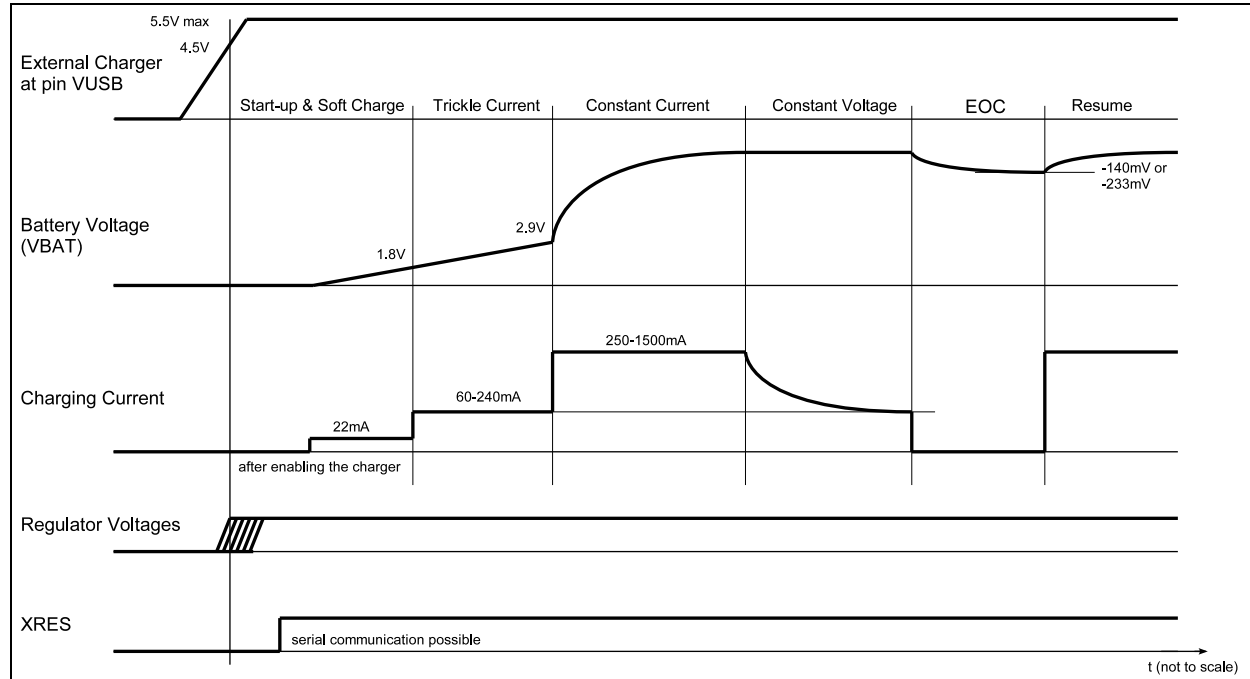
Constant current charging is initiated when *bat\_charging\_enable* is set and the battery voltage at pin VBAT is above the  $V_{TRICKLE}$  and below  $V_{CHOFF}$ . The **CCM** bit is set when the charger has started, and the charge current will be limited to **ConstantCurrent** by the battery charge controller. When the battery approaches full charge, its voltage will reach the charge termination threshold  $V_{CHOFF}$ .  $V_{CHOFF}$  depends on the **ChVolEoc** bits settings. Top-off charge will be started (**CVM** will be set).

### Constant voltage charging

Constant voltage charge mode is initiated and the **CVM** bit will be set when the  $V_{CHOFF}$  threshold has been reached.

The charge current is monitored during constant voltage charging. It will be decreasing from its initial value during constant current charging and eventually drop below the value set by **TrickleCurrent**. If the measured charge current is less than or equal to **TrickleCurrent**, the charging cycle is terminated and **EOC** is set.

### 8.8.3 Charger States



### 8.8.4 Stop charging conditions

There are multiple safety features implemented that trigger a stop\_charging condition:

These are the following:

- Battery temperature too high. If  $ntc\_on=1$  and voltage at pin NTC is below  $V_{BATTEMP}$
- Timeout timer expired (If  $ch\_timeout>0$  and charging time has been exceeded. (Can be reset by unplugging the charger, setting  $chg\_on=0$  or writing  $charging\_tmax=0$ )
- VUSB over-voltage detected
- Die temp  $>140deg$  ( $ov\_temp\_140$  set)

### 8.8.5 Battery presence indication and operation without battery

After EOC state is reached a timer for NOBAT detection is started. If there is no battery present, the VBAT voltage will drop to  $V_{RESUME}$ . Depending on the load on VBAT and the capacitor on VBAT this might take some milliseconds to 1 second. If the RESUME mode is enabled (Bit  $auto\_resume=1$ ), the charger will restart charging (ConstantCurrent charging) after 100msec delay.

The 100msec dead time is necessary to get a battery oscillation frequency below 10Hz, if there is no battery present.

If the NOBAT detection timer is below 2 seconds after reaching EOC state, and this happens 2 times in serial, the **Nobat** bit in ChargerStatus register is set. If an battery is inserted the bit will be reset after the timer exceeds the 2 seconds.

In addition, if the **nobat\_ntc\_det** bit is set the looping will be stopped and a NTC detection is started.

A pull up current of 0.5uA is applied to BATTEMP. If the BATTEMP voltage is above 1.8V, the state machine stays in the no bat state. If the BATTEMP voltage is below 1.8V, a charging cycle is initiated.

### 8.8.6 Charger overvoltage protection

This blocks checks if the charger voltage VUSB is above  $V_{CHOVH}$ . If the VUSB voltage is above  $V_{CHOVH}$ , the pin XOFF is pulled to GND immediately, to protect the pin VCHG\_IN, and the charger is set into off state. If the VUSB voltage is below  $V_{CHOVH}$  the XOFF pin is charged up to  $V_{XOFF\_REG}$  with an integrated charge pump. If the pin exceeds  $V_{XOFF\_MIN}$  the **usb\_prot\_ready** bit is set and the charger is started.

### 8.8.7 NTC supervision

This charger block also features a supply for an external NTC resistor to measure the battery temperature while charging. If the temperature is too high (voltage on BATTEMP pin is below  $V_{BATTEMP\_ON}$ ) the charger will stop operation. If needed an interrupt can be generated based on this event. When the battery temperature drops the charger the voltage on BATTEMP pin will rise above  $V_{BATTEMP\_OFF}$  and the charger will start charging again. This is forming a temperature hysteresis of about 3 to 5°C to avoid an oscillation of the charger.

The levels for switching off the charger (**ntc\_temp**: 45°C or 55°C) as well as the type of NTC (**ntc\_10k**: 10k or 100k) can be selected via register settings. The battery temperature supervision via the NTC can be switched off (**ntc\_on** = 0).

The supply for the NTC will be only on when a charger is detected and **ntc\_on** bit is set.

### 8.8.8 Charger Modes

Figure 23. Linear Charger Modes

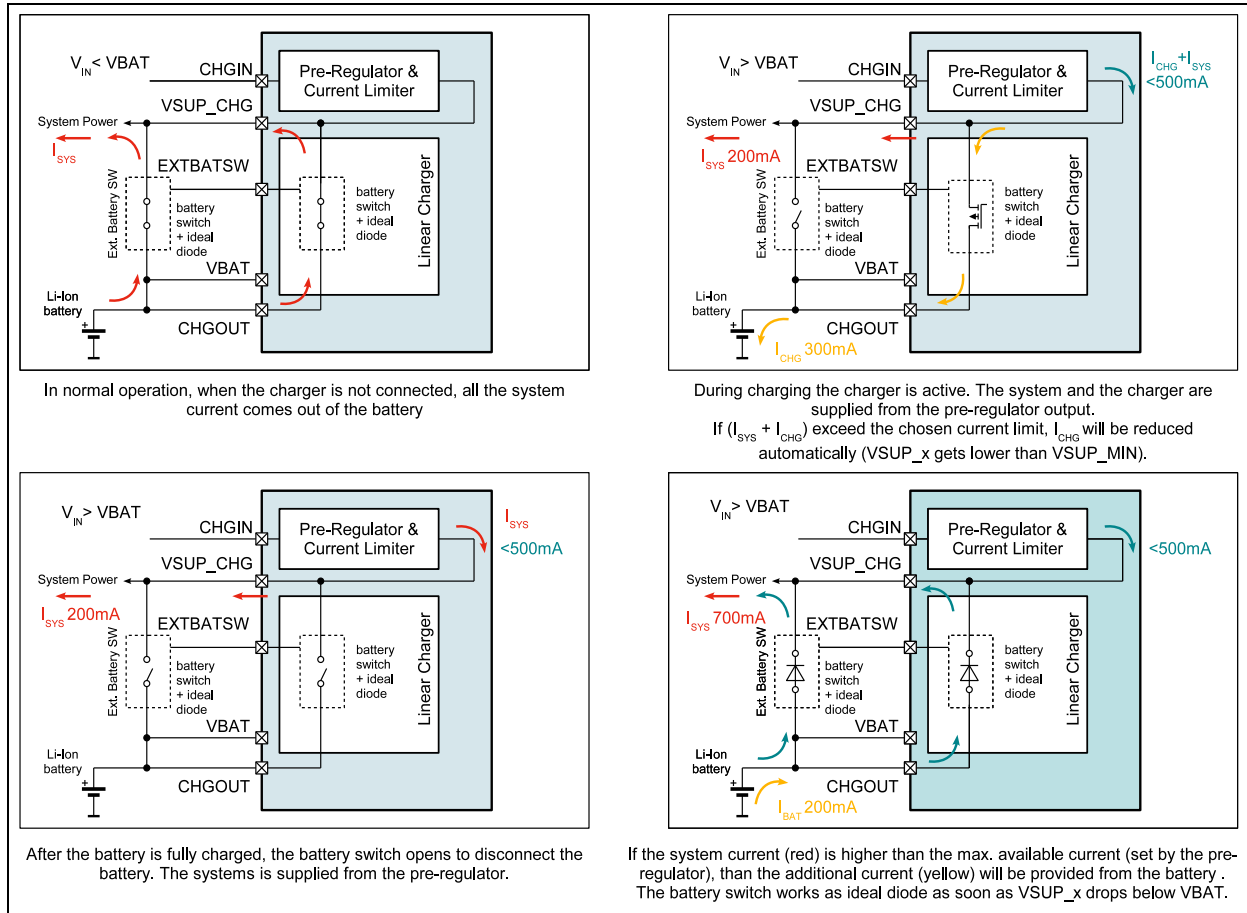
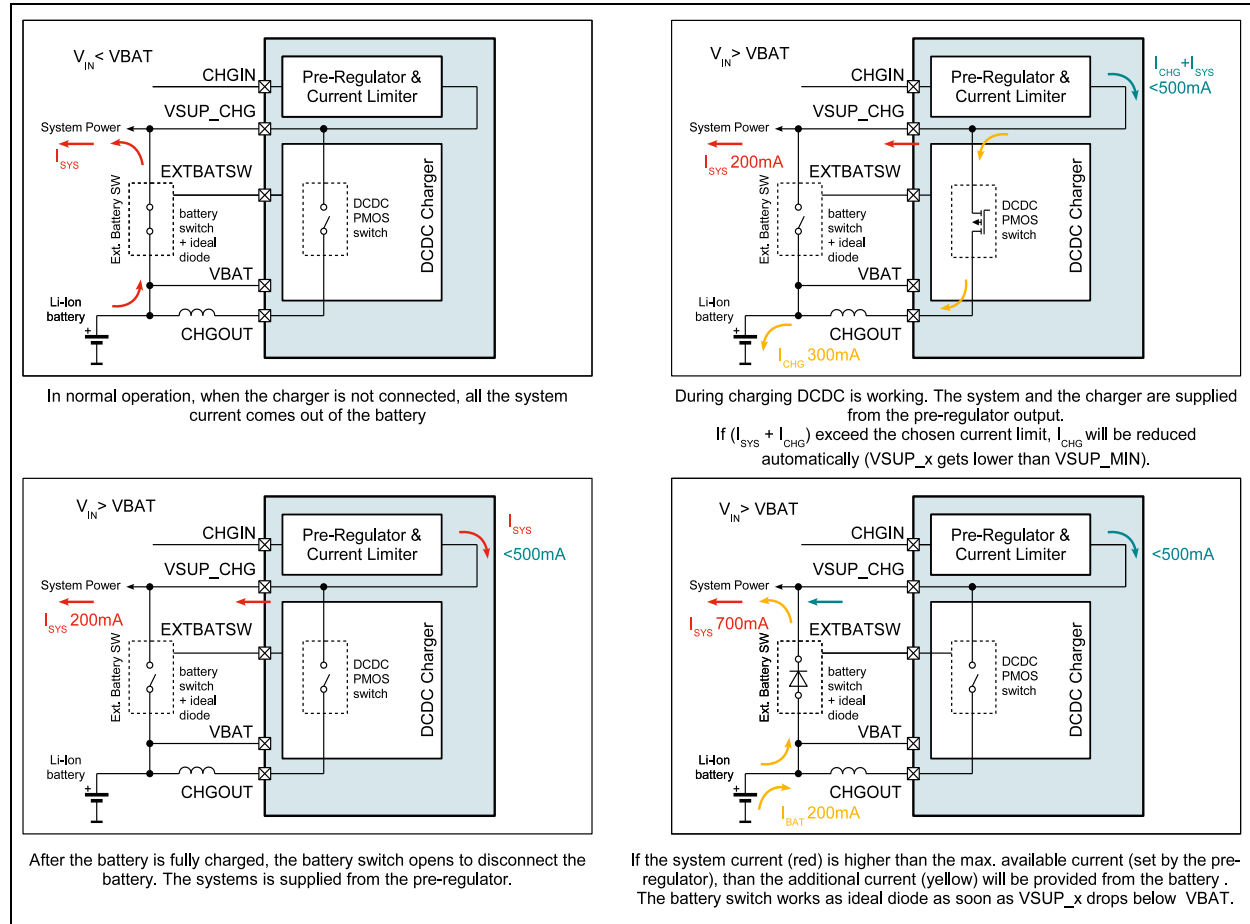
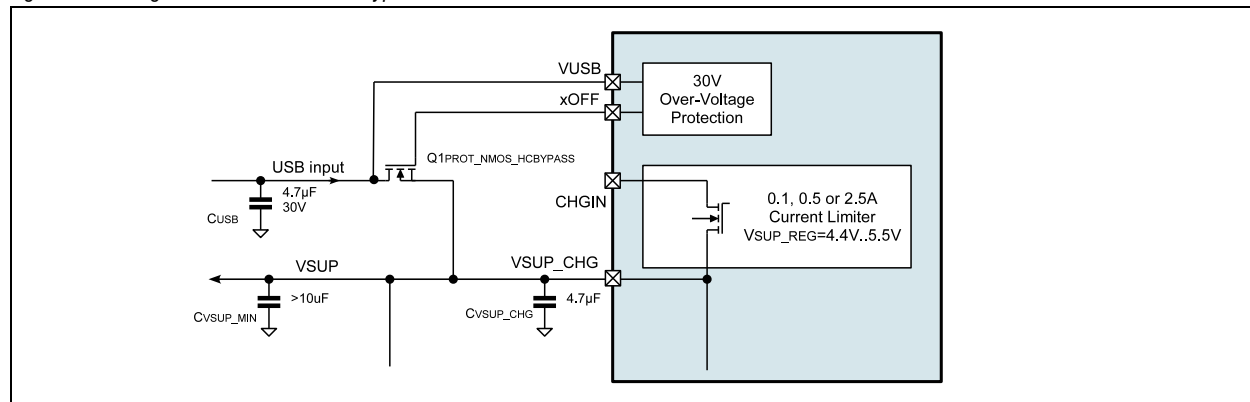


Figure 24. DCDC Charger Modes



### 8.8.9 Alternative Charger Input Configurations

Figure 25. Charger with Current Limiter Bypass



### 8.8.10 Parameter

$T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 16. Charger Parameter

| Symbol                             | Parameter   | Condition   | Min  | Typ           | Max   | Unit          |
|------------------------------------|---|---|------|---------------|-------|---------------|
| $V_{CHDET}$                        | Charger Detection threshold   | VUSB-VBAT<br>Hysteresis is > 40mV   | 50   | 75            | 105   | mV            |
| $V_{CHMIN}$                        |   |   | 0    | 20            | 35    | mV            |
| $V_{SOFT}$                         | Apply $I_{SOFT}$ charging current below that VBAT voltage                             |   |      | 1.8           |       | V             |
| $I_{SOFT}$                         | Charging current if VBAT is below $V_{SOFT}$  |   |      | 22            |       | mA            |
| $V_{TRICKLE}$                      | Trickle to CC current threshold   | $V_{BAT}$ rising  |      | 2.9           |       | V             |
| $I_{TRICKLE}$                      | Trickle/EOC current limit   | Programmable in 60mA steps  |      | 60..<br>240   |       | mA            |
| $V_{CHOFF}$                        | Charge termination threshold  | programmable in 20mV steps between 3.5 and 4.44V  |      | 3.5..<br>4.44 |       | V             |
|                                    |   | @ <b>ChVoltEOC</b> =35 (4.2V)   | 4.15 | 4.20          | 4.242 | V             |
| $I_{CC}$                           | CC current limit  | Programmable in 50mA steps  |      | 250..<br>1500 |       | mA            |
|                                    |   | linear charging mode  | -10% |               | +10%  | mA            |
| $I_{USB\_limit}$                   | USB input current limit   | @ 470mA   | -7%  | 470           | +6%   | mA            |
| $V_{RESUME}$                       | Resume voltage limit to start charger   | VBAT falling threshold (depending on <b>ChVoltResume</b> )  |      | 140/233       |       | mV            |
| $V_{SUP\_min}$                     | VSUP level for charging current regulation (reduction), to avoid voltage drop on VSUP | Trickle current (or constant current in linear mode) will be regulated down, if VSUP drops below this level | -6%  | 3.9           | 3%    | V             |
|                                    |   |   |      | 4.2           |       |               |
|                                    |   |   |      | 4.5           |       |               |
|                                    |   |   |      | 4.7           |       |               |
| $I_{REV\_OFF}$                     | Reverse current shut down   | $V_{SUP\_CHG} = 5V$ , VUSB open   |      | 5             |       | $\mu\text{A}$ |
| $V_{Diode}$                        | Ideal Diode start voltage   |   |      | 50            |       | mV            |
| $R_{ON\_BATSW}$                    | Battery Switch On-resistance  |   |      | 0.10          |       | $\Omega$      |
| <b>Temp Supervision</b>            |   |   |      |               |       |               |
| $V_{BATTEMP\_ON}$                  | Battery Temp. high level (50 or 55°C)   | $V_{SUP} > 3V$<br>$NTC_{\beta=4200}$  |      | 500 or<br>400 |       | mV            |
| $V_{BATTEMP\_OFF}$                 | Battery Temp. low level (45 or 50°C)  | $V_{SUP} > 3V$<br>$NTC_{\beta=4200}$  |      | 600 or<br>500 |       | mV            |
| $I_{BATTEMP}$                      | NTC Bias Current  | 100k $\Omega$ NTC<br>10k $\Omega$ NTC   | -15% | 15<br>150     | +15%  | $\mu\text{A}$ |
| <b>XOFF overvoltage protection</b> |   |   |      |               |       |               |
| $V_{CHOVH}$                        | VUSB Overvoltage Detection  | monitor voltage on VUSB, disable charging beyond this voltage (200mV hysteresis)                            |      | 6.2           | +3%   | V             |
|                                    |   |   | -3%  | 6.0           |       |               |
| $V_{XOFF\_min}$                    | Minimum XOFF voltage for charger startup  |   |      | 7.5           |       | V             |
| $V_{XOFF\_REG}$                    | Regulation voltage for XOFF pin   |   |      | 10            |       | V             |
| $I_{XOFF}$                         | External pull down current on XOFF pin  | Connect XOFF pin to MOSFET gates only   |      |               | 100   | nA            |

Table 17. External Components

| Symbol                            | Description                  | Condition                                  | Min | Typ | Max | Unit |
|-----------------------------------|------------------------------|--|-----|-----|-----|------|
| Q1 <sub>PROT_NMOS</sub>           | FDN337N                      | V <sub>ds</sub> =30V, 2.2A                 |     | 65  |     | mΩ   |
|                                   | FDN339AN                     | V <sub>ds</sub> =20V, 3A                   |     | 35  |     | mΩ   |
|                                   | FDN327N                      | V <sub>ds</sub> =20V, 2A                   |     | 70  |     | mΩ   |
|                                   | FDG311N                      | V <sub>ds</sub> =20V, 1.9A                 |     | 115 |     | mΩ   |
|                                   | Si1472DH                     |  |     | 82  |     | mΩ   |
| Q1 <sub>PROT_NMOS_HC BYPASS</sub> | FDC637AN                     | V <sub>ds</sub> =20V, 6.2A                 |     | 24  |     | mΩ   |
|                                   | FDT439N                      | V <sub>ds</sub> =30V, 6.3A                 |     | 45  |     | mΩ   |
| Q2 <sub>BATSW_NMOS</sub>          | FDN306P                      | @ 4.5V                                     |     | 40  |     | mΩ   |
|                                   | FDC602                       | @ 4.5V                                     |     | 33  |     | mΩ   |
|                                   | FDC642                       | @ 4.5V                                     |     | 65  |     | mΩ   |
| C <sub>USB</sub>                  | Bypass capacitor on VUSB pin | ± 20%, X5R or X7R dielectric / 25V         |     | 4.7 |     | μF   |
| C <sub>VSUP_CHG</sub>             | Bypass capacitor on VSUP_CHG | X5R or X7R dielectric near to pin VSUP_CHG |     | 4.7 |     | μF   |
| C <sub>VSUP_MIN</sub>             | Bypass capacitor on VSUP     | X5R or X7R dielectric, total value         | 10  |     |     | μF   |
| C <sub>VBAT</sub>                 | Bypass capacitor on VBAT     | X5R or X7R dielectric                      |     | 10  |     | μF   |
| L <sub>CHGOUT</sub>               | LQM2HPN1R0MJ0 (MURATA)       | R <sub>on</sub> =90mΩ / 1.5A rated current |     | 1   |     | μH   |
|                                   | MLP2520S1R0M (TDK)           | R <sub>on</sub> =85mΩ / 1.5A rated current |     | 1   |     | μH   |
| D <sub>CHGOUT</sub>               | PMEG2010 (NXP)               |  |     | 1A  |     |      |
|                                   | NSR10F20NXT5G (ONSEMI)       |  |     | 1A  |     |      |

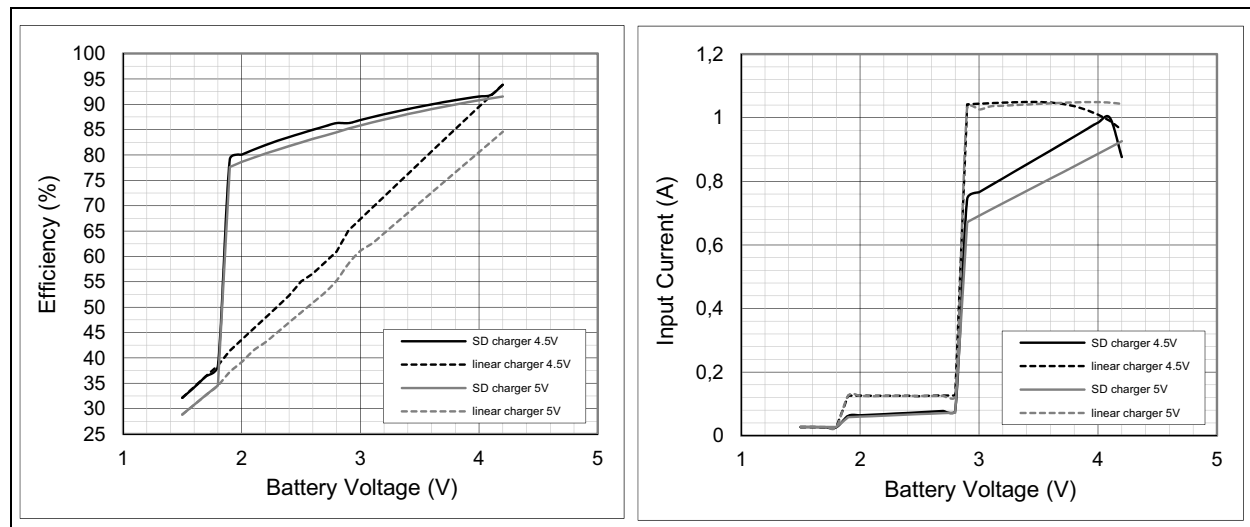
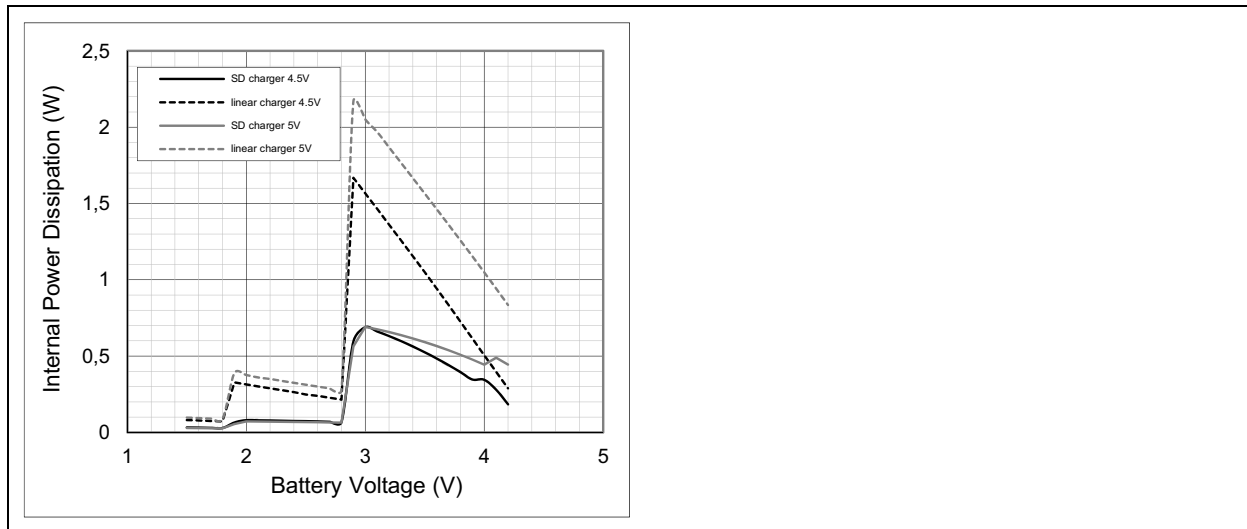
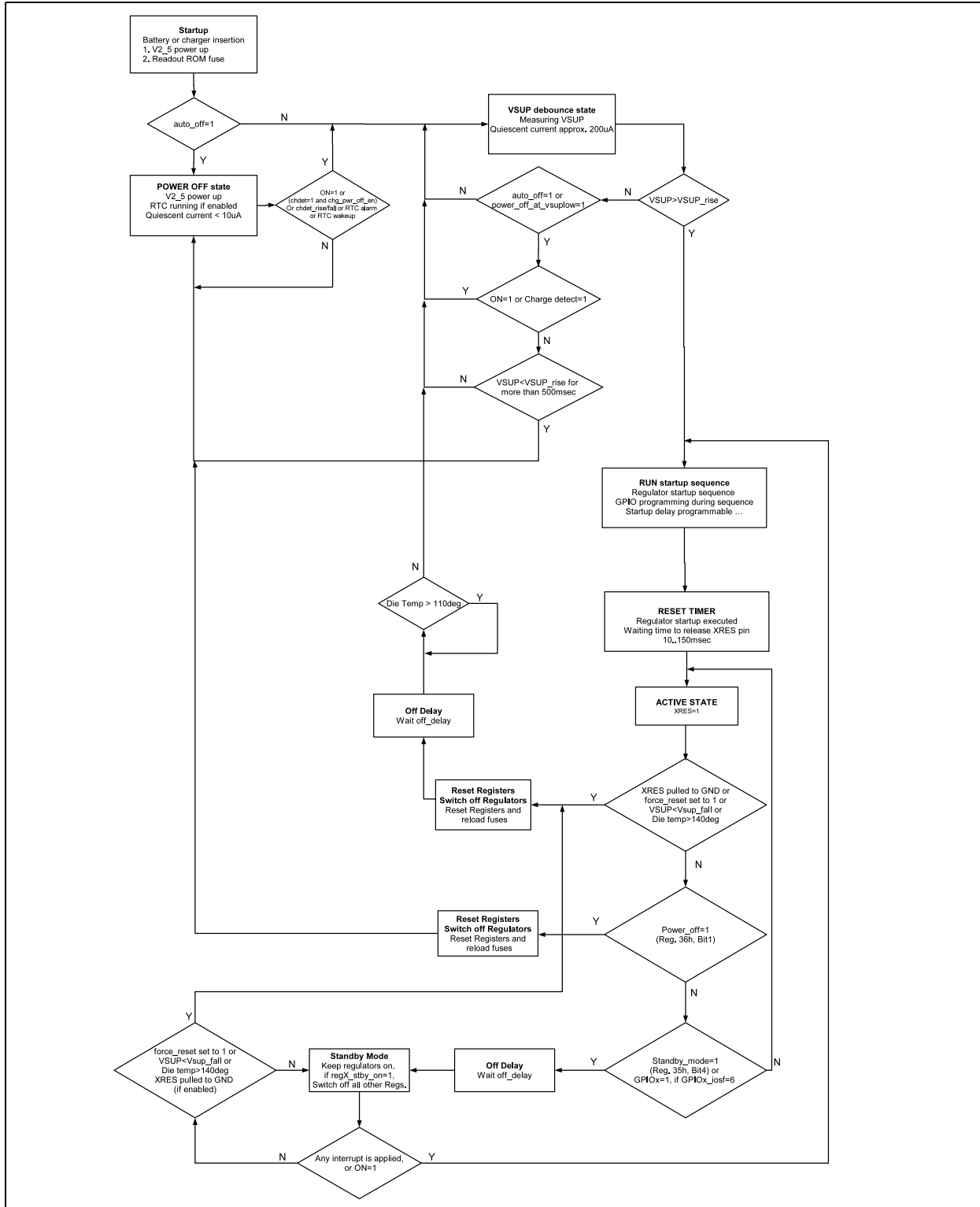
Figure 26. Step-Down vs Linear Charger; V<sub>SUP</sub> = 4.5/5.0V, T<sub>A</sub> = +25°C

Figure 27. Step-Down vs Linear Charger;  $V_{SUP} = 4.5/5.0V$ ,  $T_A = +25^\circ C$ 

# 9 Detailed Description - System Functions

## 9.1 Start-up

Figure 28. Startup flow chart





### 9.1.1 Normal Startup

During a normal reset cycle (e.g. after the battery or a charger is inserted), after V2\_5 is above  $V_{POR}$  and VSUP is above ResVoltRise a normal startup happens:

- The external capacitor on CREF is charged to 1.8V.
- Configuration of Charger (DCDC or linear) and SD2/SD3 (combined mode or separated) is read from the Boot-OTP.
- Startup State machine reads out the internal Boot-OTP. The start-up sequence of Step-Down Converter, LDO's and GPIOs are controlled by the Boot-OTP.
- Reset-Timer is set by the Boot-OTP
- The reset is released when the Reset Timer expires (external pin XRES)

### 9.1.2 Startup from Charger

If the voltage on pin VUSB is within VSTARTCHARGER, the AS3711 is started (even with VBAT = 0V). This allows the battery to be charged (even from deeply discharged batteries) and finally a normal startup to happen.

### 9.1.3 Parameter

Table 18. Charger and ON-input Startup Conditions

| Symbol             | Parameter                           | Note        | Min  | Typ | Max                    | unit |
|--------------------|-------------------------------------|-------------|------|-----|------------------------|------|
| VSTARTCHARGER      | Voltage on VUSB for system to start | on Pin VUSB | 4.2  | 5.0 | 30                     | V    |
| V <sub>ON_IL</sub> | ON Low Level input voltage          |             | -0.3 |     | 0.4                    |      |
| V <sub>ON_IH</sub> | ON High Level input                 |             | 1.4  |     | V <sub>VSUP_GPIO</sub> |      |
| I <sub>ON_PD</sub> | ON Pull down current                |             | 4    | 12  |                        | μA   |

## 9.2 Reset

### 9.2.1 General Description

XRES is a low active bi-directional pin. An external pull-up to the periphery supply has to be added.

During each reset cycle the following states are controlled by the AS3711:

- pin XRES is forced to GND
- normal startup with programmable power-on sequence and regulator voltages (see Start-up on page 39)
- reset is active until the programmable reset timer (set by register bits *res\_timer<2:0>*) expires
- all registers are set to their default values after power-on, except the reset control- and status-registers.
- XRES is pulled high by the external resistor and the whole system is leaving the reset state

**Note:** Programming is controlled by the internal Boot-OTP

### 9.2.2 Parameter

Table 19. XRES-input Characteristics

| Symbol               | Parameter                     | Note | Min  | Typ | Max           | Unit |
|----------------------|-------------------------------|------|------|-----|---------------|------|
| V <sub>XRES_IL</sub> | XRES Low Level input voltage  |      | -0.3 |     | 0.4           | V    |
| V <sub>XRES_IH</sub> | XRES High Level input voltage |      | 1.4  |     | VSUP_G<br>PIO | V    |

### 9.2.3 Reset Conditions

Reset can be activated from 7 different sources:

- Power on (battery or charger insertion)
- Low Battery
- Software forced reset
- Power off mode
- External triggered through the pin XRES
- Over-temperature
- Watchdog
- On-key long press

*Voltage detection:*

There are two types of voltage dependent resets: V<sub>POR</sub> and V<sub>XRES</sub>. V<sub>POR</sub> monitors the voltage on V2\_5 and V<sub>XRES</sub> monitors the voltage on VSUP. The linear regulator for V2\_5 is always on and uses the voltage CHGIN or VBAT VSUP as its source.

The pin XRES is only released if V2\_5 is above V<sub>POR</sub> and VSUP is above ResVotlRise.

Table 20. Reset Levels

| Symbol                   | Parameter   | Note   | Min | Typ                       | Max | Unit |
|--------------------------|---|--|-----|---------------------------|-----|------|
| V <sub>POR</sub>         | Overall power on reset  | Monitor voltage on V2_5; power on reset for all internal functions | 1.5 | 2.0                       | 2.3 | V    |
| VXRES <sub>RISE</sub>    | Reset level for V <sub>supply</sub> rising  | Monitor voltage on VSUP; rising level                              |     | ResVolt Rise <sup>1</sup> |     | V    |
| VXRES <sub>FALLING</sub> | Reset level for V <sub>supply</sub> falling   | Monitor voltage on VSUP; falling level                             |     | 2.7                       |     | V    |
|                          |   | if <b>SupResEn</b> =1 only   |     | ResVoltFall               |     | V    |
| VXRES <sub>MASK</sub>    | Mask time for VXRES <sub>FALLING</sub> .<br>Duration for VBAT<ResVoltFall until a reset cycle is started <sup>2</sup> | <b>FastResEn</b> = 0   |     | 3                         |     | ms   |
|                          |   | <b>FastResEn</b> = 1   |     | 4                         |     | us   |

1. It's recommended to set the ResVoltRise level 200mV above the ResVolt Fall level to have a hysteresis.
2. XRES signal is de-bounced with the specified mask time for rising- and falling slope of VBAT.

**Note:** VXRES<sub>FALLING</sub> is only accepted if the reset condition is longer than VXRES<sub>MASK</sub>. This guard time is used to avoid a complete reset of the system in case of short drops of VBAT.

#### Power off:

To put the chip into ultra low power mode, write '1' into *power\_off*. The chip stays in power off mode until the external pin ON is pulled high, the charger is inserted or the level V<sub>POR</sub> is touched to start a complete reset cycle. The bit *power\_off* is automatically cleared by this reset cycle. During *power\_off* state all circuits are shut-off except the Low Power LDO (V2\_5). Thus the current consumption of AS3711 is reduced to less than 15 µA. The digital part is supplied by V2\_5, all other circuits are turned off in this mode, including references and oscillator. Except the reset control registers all other registers are set to their default value after power-on.

#### Software forced reset

Writing '1' into the register bit *force\_reset* immediately starts a reset cycle. The bit *force\_reset* is automatically cleared by this reset.

#### External triggered reset:

If the pin XRES is pulled from high to low by an external source (e.g. microprocessor or button) a reset cycle is started as well.

#### Over-temperature reset:

The reset cycle can be started by over-temperature conditions. (see Supervisor on page 48)

#### Watchdog reset:

If the watchdog is armed (register bit **wtdg\_on** = 1 and **wtdg\_res\_on** = 1) and the timer expires it causes a reset. (see Watchdog on page 49).

#### Long ON-key press:

When applying a high level on the ON input pin for 4s/8s (depending on **on\_reset\_delay**) a reset is initiated. This is thought as a safety feature when the SW hangs up and no watchdog is used.

## 9.3 Stand-by

### 9.3.1 General Description

Stand-by allows shutting down a part or the complete system. Stand-by can be terminated by every possible interrupt or GPIO of the PMU. The interrupt has to be enabled and GPIO has to be configured before going to hibernation.

Table 21. Hibernation

| State          | Description  |
|----------------|--|
| Enter via GPIO | <p>To enter stand-by mode the following settings have to be done:</p> <ul style="list-style-type: none"> <li>- Enable just these IRQ sources which should lead to leave hibernation mode.</li> <li>- Make sure that IRQ is inactive (IRQ flags get cleared by register reading)</li> <li>- Set the GPIO to input (gpioX_mode = 0)</li> <li>- Set the GPIO for stand-by control (gpioX_iosf = 6)</li> <li>- Set regX_select and regX_voltage if an other voltage is needing during stand-by for up to 3 regulators</li> <li>- Define which regulators should be kept powered during stand-by (sdX_stby_on, ldoX_stby_on)</li> <li>- set <b>chg_pwr_off_en</b> to 1</li> <li>- Activate the selected GPIO</li> </ul> |
| Enter via SW   | <p>To enter stand-by mode the following settings have to be done:</p> <ul style="list-style-type: none"> <li>- Enable just these IRQ sources which should lead to leave hibernation mode.</li> <li>- Make sure that IRQ is inactive (IRQ flags get cleared by register reading)</li> <li>- Set the delay for going into stand-by after the SW command (<b>off_delay</b>)</li> <li>- Define which regulators should be kept powered during stand-by (sdX_stby_on, ldoX_stby_on)</li> <li>- set <b>chg_pwr_off_en</b> to 1</li> <li>- set <b>standby_mode_on</b> to 1</li> </ul>   |
| Hibernation    | <p>V2_5 chip supply is kept ON<br/>           All other regulators are switched OFF dependent on the stby_on bits<br/>           XRES goes active (can be disabled in the boot ROM) and pwr_good goes inactive</p>   |
| Leave          | <p>The chip will come out of stand-by with</p> <ul style="list-style-type: none"> <li>- IRQ activation or</li> <li>- GPIO control (if entered via GPIO or interrupt)</li> </ul> <p>Start-Up sequence is provided defined by the boot ROM.</p>  |

## 9.4 Internal References

The internal reference circuits needs the following external components:

Table 22. Reference External Components

| Symbol | Parameter                 | Note   | Min  | Typ | Max  | Unit |
|--------|---------------------------|--|------|-----|------|------|
| CEXT   | External filter capacitor | Ceramic low-ESR capacitor between CREF and VSS | -10% | 100 | +10% | nF   |

### 9.4.1 Low Power Mode

Use bit *low\_power\_on* to activate the Low Power Mode. In this mode the on-chip voltage reference and the temperature supervision comparators are operating in pulsed mode. This reduces the quiescent current of the AS3711 by 45uA (typ.). Because of the pulsed function some specifications are not fulfilled in this mode (e.g. increased noise), but still the full functionality is available.

**Note:** Low power mode can be controlled by the serial interface.

### 9.4.2 Parameter

Table 23. References Parameters

| Symbol | Parameter                            | Note  | #Min | Typ  | Max | Unit |
|--------|--------------------------------------|---|------|------|-----|------|
| VCEXT  | Reference Voltage                    | Low noise trimmed voltage reference – connected to Pad CREF; <b>do not load</b> | -1%  | 1.8  | +1% | V    |
| fCLK   | Accuracy of Internal reference clock | Adjustable by serial interface register clk_int                                 | -12  | fCLK | +12 | %    |



The regulator effected by this mode is selected by regX\_select. While GPIO3 & GPIO4 always control all regulators selected by regX\_select, GPIO1 and GPIO2 may be used to control two regulators separately.:

Table 24. GPIO Vselect modes

| gpio1_iosf = | gpio2_iosf = | Vselect mode   |
|--------------|--------------|--|
| <> 5         | <> 5         | no voltage select by GPIO for regulator  |
| <> 5         | 5            | GPIO2 controls regulator selected by <b>reg1_select</b> , <b>reg2_select</b> and <b>reg3_select</b>  |
| 5            | <> 5         | GPIO1 controls regulator selected by <b>reg1_select</b> , <b>reg2_select</b> and <b>reg3_select</b>  |
| 5            | 5            | GPIO1 controls regulator selected by reg1_select<br>GPIO2 controls regulator selected by reg2_select |

#### Stand-by and Vselect input

This mode is very similar to the Vselct mode described in the previous paragraph. In addition to switch between 2 register settings of 2 regulators the chip is set into stand-by mode when the GPIOx pin goes low and wakes up again when the pin is pulled high. The gpioX\_mode should be set to input.

While GPIO3 & GPIO4 always control all regulators selected by regX\_select, GPIO1 & GPIO2 may be used to control two regulators separately.:

Table 25. GPIO Stand-by plus Vselect modes

| gpio1_iosf = | gpio2_iosf = | Vselect mode   | stand-by control |
|--------------|--------------|--|------------------|
| <> 6         | <> 6         | no voltage select by GPIO for regulator  | no               |
| <> 6         | 6            | GPIO2 controls regulator selected by <b>reg1_select</b> , <b>reg2_select</b> and <b>reg3_select</b>  | yes              |
| 6            | <> 6         | GPIO1 controls regulator selected by <b>reg1_select</b> , <b>reg2_select</b> and <b>reg3_select</b>  | yes              |
| 6            | 6            | GPIO1 controls regulator selected by reg1_select<br>GPIO2 controls regulator selected by reg2_select | yes              |

#### PWRGOOD output

This signal will go high at the end of the start-up sequence. This can be used as a second reset signal to the processor to e.g. start oscillators. The gpioX\_mode should be set to output.

#### Q32k output

When selected the GPIOx will provide the 32kHz RTC crystal frequency. If the oscillator is not enabled or not assembled a internal RC oscillator based clock will be used for the output. The gpioX\_mode should be set to output.

#### Watchdog input

When pulling the GPIO high the watchdog will be triggered to avoid a reset cycle initiated ba the watchdog. The gpioX\_mode should be set to input.

#### SU1 OC output

This output signal can be used to control an external disconnect transistor if SU1 detects an over current condition. The gpioX\_mode should be set to output.

#### Charger active output

When selected, the GPIOx will go high if the charger is active. The gpioX\_mode should be set to output.

#### EOC output

When selected, the GPIOx will go high if the charger has reached the EOC state. The gpioX\_mode should be set to output.

#### 100/500mA charger input

Whith this function the charger input current limiter can be set to 100 or 500mA (low power or high power USB limit). The gpioX\_mode should be set to input.

#### 500/2.5A charger input

Whith this function the charger input current limiter can be set to 500 or 2.5A (high power USB limit or full current enabled). The gpioX\_mode should be set to input.

### Charging enable input

When pulling the GPIO to high the charger is being enabled and vice versa. This is to enable the charger without I2C communication. The gpioX\_mode should be set to input.

### PWM output

The gpio block includes an internal programmable PWM generator (can be connected to any of the GPIO outputs). Its timing is defined by pwm\_h\_time, pwm\_l\_time and pwm\_div. The gpioX\_mode should be set to output.

## 9.5.3 Parameter

Table 26. GPIO Pin Characteristics

$V_{SUP}=2.7$  to  $5.5V$ ;  $T_{amb}=-20$  to  $+70^{\circ}C$ ; unless otherwise specified

| Symbol           | Parameter                         | Note   | Min                       | Typ | Max                   | Unit      |
|------------------|-----------------------------------|--|---------------------------|-----|-----------------------|-----------|
| $V_{GPIO_{MAX}}$ | Maximum voltage on GPIO1...4 pins | Pin VSUP_GPIO is used as supply for the GPIO pins  |                           |     | $V_{SUP\_GPIO} + 0.3$ | V         |
| $V_{OL}$         | Low level output voltage          | $I_{OL}=+1mA$ ; digital output                     | -0.3                      |     | +0.4                  | V         |
| $V_{OH}$         | High level output voltage         | $I_{OH}=-1mA$ ; digital push-pull output           | $0.8 \cdot V_{SUP\_GPIO}$ |     | $V_{SUP\_GPIO}$       | V         |
| $V_{IL}$         | Low level input voltage           | digital input                                      | -0.3                      |     | 0.4                   | V         |
| $V_{IH}$         | High level input voltage          | digital input                                      | 1.4                       |     | $V_{SUP\_GPIO}$       | V         |
| $I_{LEAKAGE}$    | Leakage current                   | high impedance                                     |                           |     | 10                    | $\mu A$   |
| $R_{pull-up}$    | Pull-up resistance                | if enabled,<br>$V_{SUP\_GPIO}=3.6V$                |                           | 300 |                       | $k\Omega$ |
| $R_{pull-down}$  | Pull-down resistance              | digital input; if enabled;<br>$V_{SUP\_GPIO}=3.6V$ |                           | 300 |                       | $k\Omega$ |



## 9.6 Supervisor

All LDO's, the DCDC step ups and DCDC step downs have an integrated over-current protection.

An overtemperature protection of the chip is also integrated which can be switched on with the serial interface signal `temp_pmc_on` (enabled by default; it is not recommended to disable the over-temperature protection).

### 9.6.1 General Description

The chip has two signals for the serial interface: `ov_temp_110` and `ov_temp_140`. The flag `ov_temp_110` is automatically reset if the overtemperature condition is removed, whereas `ov_temp_140` has to be reset by the serial interface with the signal `rst_ov_temp_140`.

If the flag `ov_temp_140` is set, an automatic reset of the complete chip is initiated. The chip will only start-up when the temperature falls below the  $T_{110}$  level (including hysteresis). The flag `ov_temp_140` is not affected by this reset cycle allowing the software to detect the reason for this unexpected shutdown.

Table 27. Over-temperature Detection

| Symbol     | Parameter                              | Note | Min | Typ | Max | Unit |
|------------|--|------|-----|-----|-----|------|
| $T_{110}$  | ov_temp_110 rising threshold           |      | 95  | 110 | 125 | °C   |
| $T_{140}$  | ov_temp_140 rising threshold           |      | 125 | 140 | 155 | °C   |
| $T_{hyst}$ | ov_temp_110 and ov_temp_140 hysteresis |      |     | 5   |     | °C   |

## 9.7 Watchdog

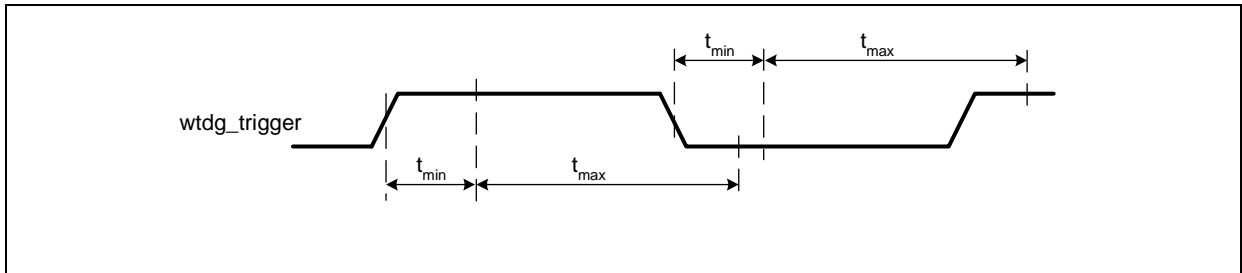
### 9.7.1 General Description

The purpose of the watchdog is to detect a deadlock of the software. If the watchdog is active, it must receive a continuous trigger signal within a programmable time window. If there is no signal anymore for a certain time period from a defined pad or special serial interface bit, it starts either a complete reset cycle or changes the state of an output pin, which can be used e.g. as an interrupt to the processor.

- The watchdog is highly configurable by the following register bits:
- The complete block can be switched on by `wtdg_on = 1` and off by `wtdg_on = 0`.
- The watchdog time window is defined by the register `wtdg_min_timer` and `wtdg_max_timer`.
- The trigger signal can be configured by register `wtdg_sw_sig` and `gpio1_iosf` or `gpio4_iosf`.
- If the watchdog expires, the system can start automatically a reset cycle if `wtdg_reset_on = 1`.

### 9.7.2 Parameter

Figure 30. Watchdog timing diagram



## 9.8 Interrupt Generation

### 9.8.1 General Description

The interrupt controller generates an interrupt request for the host controller as soon as one or more of the bits in the *Interrupt 1...3* register are set by pulling high pin INT (INT has to be selected as a GPIO output function). The output polarity can be changed to active low (XINT) by using the `gpioX_invert` bit of the selected GPIO. All the interrupt sources can be enabled in the Interrupt Mask 1...3 register. The Interrupt 1...3 registers are cleared automatically after the host controller has read them. To prevent the AS3711 device from losing an interrupt event, the register that is read is captured before it is transmitted to the host controller via the serial interface. As soon as the transmission of the captured value is complete a logical AND operation with the bit wise inverted captured value is applied to the register to clear all interrupt bits that have already been transmitted. Clearing the read interrupt bits takes 2 clock cycles, a read access to the same register before the clearing process has completed will yield a value of '0'. Note that an interrupt that has been present at the previous read access will be cleared as well in case it occurs again before the clearing process has completed.

During a read access to one of the interrupt registers the INT pin will be released. As soon as the transferred bits of the interrupt register have been cleared the INT pin will be pulled high in case a new interrupt has occurred in the meantime. By doing so the interrupt controller will work correctly with host controllers that are edge- and level-sensitive on their interrupt request input. Multiple byte read access is recommended to avoid reading the *Interrupt 1* register over and over again in response to a new interrupt that has occurred in the same register (and thus pulling high pin INT) before the Interrupt 2,3 register has been read.

## 9.9 10-Bit ADC

This general purpose ADC can be used for measuring several voltages and currents to perform functions like battery monitor, temperature supervision, button press detection, etc.

### 9.9.1 Input Sources

Table 28. ADC10 Input Sources

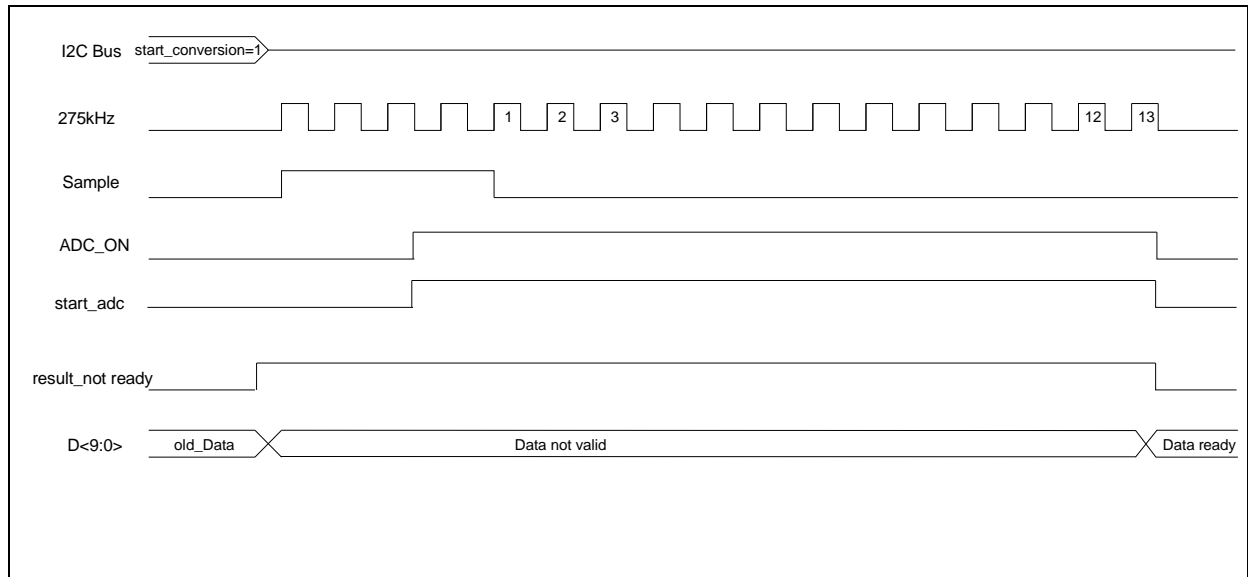
| # | Source          | Range       | LSB           | Mode      | Description                        |
|---|-----------------|-------------|---------------|-----------|------------------------------------|
| 0 | BATTEMP         | 1.8V        | 1.76mV        | 1:1       | check battery charging temperature |
| 1 | DIE temperature | 1.8V        | 1.76mV        | 1:1       | $T_j = (0.866 * ADC10<9:0>) - 274$ |
| 2 | XOUT32X         | 1.8V        | 1.76mV        | 1:1       |                                    |
| 3 | CURR1           | 1.0V        | 1.76mV        | 1:1       |                                    |
| 4 | CURR2           | 1.0V        | 1.76mV        | 1:1       |                                    |
| 5 | CURR3           | 1.0V        | 1.76mV        | 1:1       |                                    |
| 6 | VUSB            | 15V         | 26.4mV        | 15:1      | check USB charger HV input         |
| 7 | CHGIN           | 5.5V        | 7.03mV        | 4:1       | check USB charger LV input         |
| 8 | VBAT            | 5.5V        | 7.03mV        | 4:1       | check Li-Ion battery voltage       |
| 9 | VSUP            | 5.5V        | 7.03mV        | 4:1       | check main system supply voltage   |
| A | SENSEN_SU1      | 1.8V / 5.5V | 1.76 / 7.03mV | 1:1 / 4:1 |                                    |
| B | LX_SD4          | 1.8V / 5.5V | 1.76 / 7.03mV | 1:1 / 4:1 |                                    |
| C | GPIO2           | 1.8V / 5.5V | 1.76 / 7.03mV | 1:1 / 4:1 |                                    |
| D | GPIO3           | 1.8V / 5.5V | 1.76 / 7.03mV | 1:1 / 4:1 |                                    |
| E | GPIO4           | 1.8V / 5.5V | 1.76 / 7.03mV | 1:1 / 4:1 |                                    |
| F |                 |             |               |           | reserved                           |

### 9.9.2 Parameter

Table 29. ADC Characteristics

| Symbol                             | Parameter       | Note  | Min | Typ                     | Max | Unit |
|------------------------------------|-----------------|---|-----|-------------------------|-----|------|
| Resolution                         |                 |   | 10  |                         |     | Bit  |
| Input Voltage Range                | V <sub>in</sub> | for 1:1 mode  | 0   |                         | 1.8 | V    |
| Differential Nonlinearity          | DNL             | 1LSB 1.76mV for 1:1 (depending on selected channel) |     | ± 0.25                  |     | LSB  |
| Integral Nonlinearity              | INL             |   |     | ± 0.5                   |     | LSB  |
| Input Offset Voltage               | V <sub>os</sub> |   |     | 2                       |     | LSB  |
| Input Impedance                    | R <sub>in</sub> |   | 100 |                         |     | MΩ   |
| Input Capacitance                  | C <sub>in</sub> |   |     |                         | 9   | pF   |
| Power Supply Current               | I <sub>dd</sub> | during conversion only                              |     | 500                     |     | μA   |
| Power Down Current                 | I <sub>dd</sub> |   |     | 100                     |     | nA   |
| <b>Transient Parameters (25°C)</b> |                 |   |     |                         |     |      |
| Conversion Time                    | T <sub>c</sub>  |   |     | 40                      |     | μs   |
| Clock Frequency                    | f <sub>c</sub>  | internal CLK frequency/8                            |     | f <sub>clk_int</sub> /8 |     | kHz  |
| Settling time of S&H               | t <sub>s</sub>  |   | 1   |                         |     | μs   |

Figure 31. ADC Timing-diagram



## 9.10 Real Time Clock

### 9.10.1 General Description

The RTC module provides time information to the system. It is implemented as a 6-bit counter that is incremented every second - with the 32kHz oscillator delivering the necessary accurate time base – and is reset to 0 each time the counter value is 60. An additional 24-bit minute counter is incremented each time the 6-bit counter is reset to 0. Both counters are set to 0 at a power-on-reset. The host controller can set the counter to any value by setting the RTC 1...4 registers.

To prevent ambiguous time information because of the 30-bit value being incremented before all of the 4 registers have been read or written, a 30-bit parallel shadow register is implemented. Every time a write/read access via the serial interface occurs the parallel shadow register is updated with the current value of the 30-bit counter. Any write access to the RTCSecond register will disable the update of the parallel register and set the value of the appropriate byte of the parallel register. Any subsequent write access to the RTCMinute3 register will transfer the current value of the 30-bit parallel register to the RTCSecond/Minute1..3 registers and the update of the parallel register is enabled again. Similarly, any read access to the RTCSecond register will freeze the current value of the parallel register and submit the appropriate byte to the host controller via the serial interface. Any subsequent read access to the RTCMinute3 register will enable the update of the parallel register again. This mechanism makes sure that the maximum error of the value that is written to or read from the registers is 1 second.

To start the RTC, rtc\_on bit has to be set to 1.

The RTC stops automatically at its highest value (3F,FF,FF,FF) to prevent overrun.

### 9.10.2 Alarm

The RTC module includes an alarm function. When the content of the RTCAlarm registers equals the content of the RTC registers bit rtc\_alarm will be set in the interrupt register. Furthermore the RTC module can generate a repeating interrupt every second, every minute, every 2 minutes or every 8 minutes.

To avoid ambiguous behavior during write access to the RTCAlarm registers any write access to the RTCAlarmSecond register will disable the alarm function; any subsequent write access to the RTCAlarmMinute3 will enable the alarm function again.

## 9.11 2-Wire-Serial Control Interface

### 9.11.1 Feature List

- Fast-mode capability (max. SCL-frequency is 400 kHz)
- 7+1-bit addressing mode
- 60h x 8-bit data registers (word address 0x00 - 0x60)
- Write formats: Single-Byte-Write, Page-Write
- Read formats: Current-Address-Read, Random-Read, Sequential-Read
- SDA input delay and SCL spike filtering by integrated RC-components

### 9.11.2 Protocol

Table 30. 2-Wire Serial Symbol Definition

| Symbol   | Definition                        | RW | Note               |
|----------|-----------------------------------|----|--------------------|
| S        | Start condition after stop        | R  | 1 bit              |
| Sr       | Repeated start                    | R  | 1 bit              |
| DW       | Device address for write          | R  | 1000 0000b (80h)   |
| DR       | Device address for read           | R  | 1000 0001b (81h)   |
| WA       | Word address                      | R  | 8 bit              |
| A        | Acknowledge                       | W  | 1 bit              |
| N        | No Acknowledge                    | R  | 1 bit              |
| reg_data | Register data/write               | R  | 8 bit              |
| data (n) | Register data/read                | W  | 8 bit              |
| P        | Stop condition                    | R  | 1 bit              |
| WA++     | Increment word address internally | R  | during acknowledge |

Figure 32. Byte Write

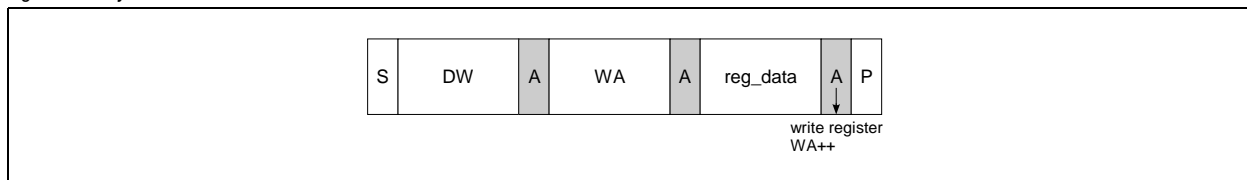
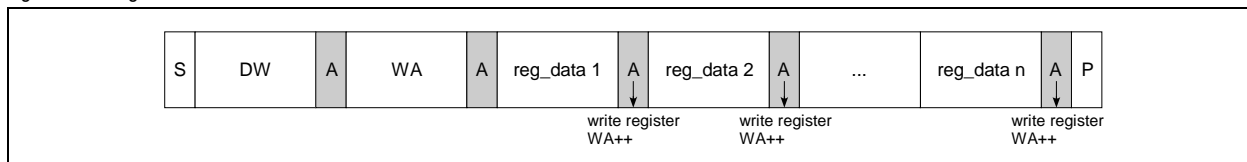


Figure 33. Page Write

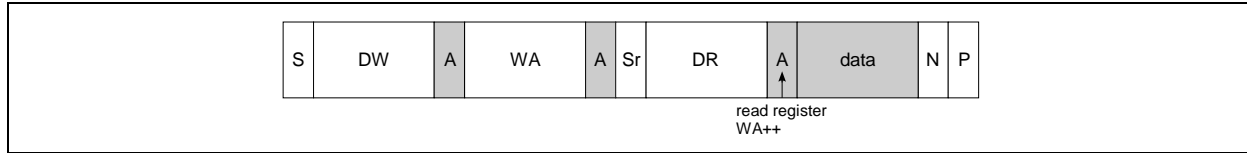


Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 34. Random Read

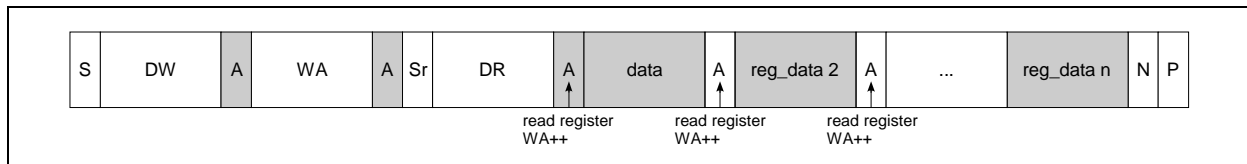


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

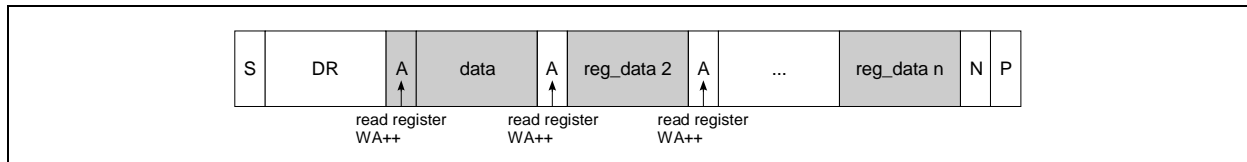
In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure 35. Sequential Read



Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 36. Current Address Read



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

### 9.11.3 Parameter

Table 31. I2C SDA,SCL Characteristics

| Symbol          | Parameter                        | Note | Min  | Typ | Max           | Unit |
|-----------------|----------------------------------|------|------|-----|---------------|------|
| V <sub>IL</sub> | SCL,SDA Low Level input voltage  |      | -0.3 |     | 0.4           | V    |
| V <sub>IH</sub> | SCL,SDA High Level input voltage |      | 1.4  |     | VSUP_G<br>PIO | V    |

The AS3711 is compatible to the NXP two wire specification [http://www.nxp.com/acrobat\\_download2/literature/9398/39340011.pdf](http://www.nxp.com/acrobat_download2/literature/9398/39340011.pdf) Version 2.1 January 2000 for standard and fast mode (no high speed mode).



## 10 Register Overview

Table 32. Register Overview

| Addr | Name           | <D7>                | <D6>            | <D5>                | <D4>           | <D3>                | <D2>       | <D1>                | <D0> |  |
|------|----------------|---------------------|-----------------|---------------------|----------------|---------------------|------------|---------------------|------|--|
| 00h  | SD1Voltage     | sd1_frequ           | sd1_vsel<6:0>   |                     |                |                     |            |                     |      |  |
| 01h  | SD2Voltage     | sd2_frequ           | sd2_vsel<6:0>   |                     |                |                     |            |                     |      |  |
| 02h  | SD3Voltage     | sd3_frequ           | sd3_vsel<6:0>   |                     |                |                     |            |                     |      |  |
| 03h  | SD4Voltage     |                     | sd4_vsel<6:0>   |                     |                |                     |            |                     |      |  |
| 04h  | LDO1Voltage    | ldo1_on             | ldo1_ilimit     | -                   | ldo1_vsel<4:0> |                     |            |                     |      |  |
| 05h  | LDO2Voltage    | ldo2_on             | ldo2_ilimit     | -                   | ldo2_vsel<4:0> |                     |            |                     |      |  |
| 06h  | LDO3Voltage    | ldo3_on             | ldo3_ilimit     | ldo3_vsel<5:0>      |                |                     |            |                     |      |  |
| 07h  | LDO4Voltage    | ldo4_on             | ldo4_ilimit     | ldo4_vsel<5:0>      |                |                     |            |                     |      |  |
| 08h  | LDO5Voltage    | ldo5_on             | ldo5_ilimit     | ldo5_vsel<5:0>      |                |                     |            |                     |      |  |
| 09h  | LDO6Voltage    | ldo6_on             | ldo6_ilimit     | ldo6_vsel<5:0>      |                |                     |            |                     |      |  |
| 0ah  | LDO7Voltage    | ldo7_on             | ldo7_ilimit     | ldo7_vsel<5:0>      |                |                     |            |                     |      |  |
| 0bh  | LDO8Voltage    | ldo8_on             | ldo8_ilimit     | ldo8_vsel<5:0>      |                |                     |            |                     |      |  |
| 0ch  | GPIO1control   | gpio1_invert        | gpio1_iosf<6:3> |                     |                | gpio1_mode<2:0>     |            |                     |      |  |
| 0dh  | GPIO2control   | gpio2_invert        | gpio2_iosf<6:3> |                     |                | gpio2_mode<2:0>     |            |                     |      |  |
| 0eh  | GPIO3control   | gpio3_invert        | gpio3_iosf<6:3> |                     |                | gpio3_mode<2:0>     |            |                     |      |  |
| 0fh  | GPIO4control   | gpio4_invert        | gpio4_iosf<6:3> |                     |                | gpio4_mode<2:0>     |            |                     |      |  |
| 10h  | SD_control     |                     | -               | sd4_enable          |                | sd3_enable          | sd2_enable | sd1_enable          |      |  |
| 20h  | GPIOsignal_out |                     | -               | gpio4_out           |                | gpio3_out           | gpio2_out  | gpio1_out           |      |  |
| 21h  | GPIOsignal_in  |                     | -               | gpio4_in            |                | gpio3_in            | gpio2_in   | gpio1_in            |      |  |
| 22h  | Reg1_Voltage   | reg1_voltage<7:0>   |                 |                     |                |                     |            |                     |      |  |
| 23h  | Reg2_Voltage   | reg2_voltage<7:0>   |                 |                     |                |                     |            |                     |      |  |
| 24h  | Reg_control    | reg2_select<7:4>    |                 |                     |                | reg1_select<3:0>    |            |                     |      |  |
| 25h  | GPIOctrl_sd    | gpio_ctrl_sd4<7:6>  |                 | gpio_ctrl_sd3<5:4>  |                | gpio_ctrl_sd2<3:2>  |            | gpio_ctrl_sd1<1:0>  |      |  |
| 26h  | GPIOctrl_ldo1  | gpio_ctrl_ldo4<7:6> |                 | gpio_ctrl_ldo3<5:4> |                | gpio_ctrl_ldo2<3:2> |            | gpio_ctrl_ldo1<1:0> |      |  |
| 27h  | GPIOctrl_ldo2  | gpio_ctrl_ldo8<7:6> |                 | gpio_ctrl_ldo7<5:4> |                | gpio_ctrl_ldo6<3:2> |            | gpio_ctrl_ldo5<1:0> |      |  |
| 2bh  | Reg3_Voltage   | reg3_voltage<7:0>   |                 |                     |                |                     |            |                     |      |  |

Table 32. Register Overview

| Addr | Name                    | <D7>                | <D6>               | <D5>              | <D4>             | <D3>              | <D2>             | <D1>                | <D0>           |                       |
|------|-------------------------|---------------------|--------------------|-------------------|------------------|-------------------|------------------|---------------------|----------------|-----------------------|
| 2ch  | Reg_control3            | -                   |                    |                   |                  | reg3_select<3:0>  |                  |                     |                |                       |
| 30h  | SD_control1             | sd4_low_noise       | sd3_low_noise      | sd2_low_noise     | sd1_low_noise    | sd4_fast          | sd3_fast         | sd2_fast            | sd1_fast       |                       |
| 31h  | SD_control2             | sd_dvm_select<7:6>  |                    | dvm_time<5:4>     |                  | sd3_slave         | sd3_fsel         | sd2_fsel            | sd1_fsel       |                       |
| 32h  | Battery_voltage_monitor | FastResEn           | SupResEn           | ResVoltFall<5:3>  |                  |                   | ResVoltRise<2:0> |                     |                |                       |
| 33h  | Startup_Control         | -                   |                    |                   |                  |                   |                  |                     | chg_pwr_off_en | power_off_at_vsup_low |
| 34h  | ResetTimer              | -                   | stby_reset_disable | auto_off          | off_delay<4:3>   |                   | -                | res_timer<1:0>      |                |                       |
| 35h  | ReferenceControl        | on_reset_delay      | reg_low_bias_mode  | clk_div2          | standby_mode_on  | clk_int<3:1>      |                  |                     | low_power_on   |                       |
| 36h  | ResetControl            | onkey_reset         | reset_reason<6:3>  |                   |                  |                   | on_input         | power_off           | force_reset    |                       |
| 37h  | OvertemperatureControl  |                     |                    |                   |                  | rst_ov_temp_140   | ov_temp_140      | ov_temp_110         | temp_pmc_on    |                       |
| 38h  | WatchdogControl         | -                   |                    |                   |                  |                   |                  |                     | wtdg_res_on    | wtdg_on               |
| 39h  | Reg_standby_mod1        | disable_regpd       | -                  |                   |                  | sd4_stby_on       | sd3_stby_on      | sd2_stby_on         | sd1_stby_on    |                       |
| 3ah  | Reg_standby_mod2        | ldo8_stby_on        | ldo7_stby_on       | ldo6_stby_on      | ldo5_stby_on     | ldo4_stby_on      | ldo3_stby_on     | ldo2_stby_on        | ldo1_stby_on   |                       |
| 40h  | curr_control            | curr3_ctrl<7:4>     |                    |                   |                  | curr2_ctrl<3:2>   |                  | curr1_ctrl<1:0>     |                |                       |
| 41h  | pwm_control_l           | pwm_l_time<7:0>     |                    |                   |                  |                   |                  |                     |                |                       |
| 42h  | pwm_control_h           | pwm_h_time<7:0>     |                    |                   |                  |                   |                  |                     |                |                       |
| 43h  | curr1_value             | curr1_current<7:0>  |                    |                   |                  |                   |                  |                     |                |                       |
| 44h  | curr2_value             | curr2_current<7:0>  |                    |                   |                  |                   |                  |                     |                |                       |
| 45h  | curr3_value             | curr3_current<7:0>  |                    |                   |                  |                   |                  |                     |                |                       |
| 46h  | Watchdog_min_timer      | wtdg_min_timer<7:0> |                    |                   |                  |                   |                  |                     |                |                       |
| 47h  | Watchdog_max_timer      | wtdg_max_timer<7:0> |                    |                   |                  |                   |                  |                     |                |                       |
| 48h  | WatchdogSoftwareSignal  | pwm_div<7:6>        |                    | -                 |                  |                   |                  |                     | wtdg_sw_sig    |                       |
| 50h  | Stepup_control1         | stepup1_v<7:3>      |                    |                   |                  |                   | stepup1_res      | stepup1_freq        | stepup1_on     |                       |
| 51h  | Stepup_control2         | stepup2_v<7:3>      |                    |                   |                  |                   | stepup2_res      | stepup2_freq        | stepup2_on     |                       |
| 53h  | Stepup_control4         | stpup1_det          | stpup1_oc          | stpup1_oc_timeout | stpup1_shortprot | stpup2_pwm_lowf   | stepup2_prot_dis | stepup2_fb<1:0>     |                |                       |
| 54h  | Stepup_control5         | -                   |                    |                   |                  | stepup2_pwm_mod_e | stepup12_clkinv  | stepup2_fbprot<1:0> |                |                       |

Table 32. Register Overview

| Addr | Name                  | <D7>              | <D6>             | <D5>                 | <D4>              | <D3>            | <D2>               | <D1>                | <D0>              |  |
|------|-----------------------|-------------------|------------------|----------------------|-------------------|-----------------|--------------------|---------------------|-------------------|--|
| 60h  | RTCcontrol            | -                 |                  |                      | rtc_irq_mode<4:3> |                 | rtc_on             | rtc_alarm_wakeup_en | rtc_rep_wakeup_en |  |
| 61h  | RTCSecond             | second<7:0>       |                  |                      |                   |                 |                    |                     |                   |  |
| 62h  | RTCMinute1            | minute0<7:0>      |                  |                      |                   |                 |                    |                     |                   |  |
| 63h  | RTCMinute2            | minute1<7:0>      |                  |                      |                   |                 |                    |                     |                   |  |
| 64h  | RTCMinute3            | minute2<7:0>      |                  |                      |                   |                 |                    |                     |                   |  |
| 65h  | RTCAlarmSecond        | alarmsecond<7:0>  |                  |                      |                   |                 |                    |                     |                   |  |
| 66h  | RTCAlarmMinute1       | alarmminute0<7:0> |                  |                      |                   |                 |                    |                     |                   |  |
| 67h  | RTCAlarmMinute2       | alarmminute1<7:0> |                  |                      |                   |                 |                    |                     |                   |  |
| 68h  | RTCAlarmMinute3       | alarmminute2<7:0> |                  |                      |                   |                 |                    |                     |                   |  |
| 69h  | SRAM                  | SRAM<7:0>         |                  |                      |                   |                 |                    |                     |                   |  |
| 70h  | ADC_control           | start_conversion  | adc_on           | adc_slow             | gpio_lv           | adc_select<3:0> |                    |                     |                   |  |
| 71h  | ADC_MSB_result        | result_not_ready  | D9_3<6:0>        |                      |                   |                 |                    |                     |                   |  |
| 72h  | ADC_LSB_result        | -                 |                  |                      |                   |                 | D2_0<2:0>          |                     |                   |  |
| 73h  | RegStatus             | curr3_lv          | curr2_lv         | curr1_lv             | -                 | sd4_lv          | sd3_lv             | sd2_lv              | sd1_lv            |  |
| 74h  | InterruptMask1        | LowBat_int_m      | ovtmp_int_m      | onkey_int_m          | chdet_int_m       | eoc_int_m       | resume_int_m       | nobat_int_m         | trickle_int_m     |  |
| 75h  | InterruptMask2        | rtc_rep_int_m     | stpup1_det_m     | stpup1_oc_m          | bat_temp_m        | sd4_lv_int_m    | sd3_lv_int_m       | sd2_lv_int_m        | sd1_lv_int_m      |  |
| 76h  | InterruptMask3        | -                 |                  |                      |                   |                 | gpio_restart_int_m | gpio_int_m          | rtc_alarm_int_m   |  |
| 77h  | InterruptStatus1      | LowBat_int_i      | ovtmp_int_i      | onkey_int_i          | chdet_int_i       | eoc_int_i       | resume_int_i       | nobat_int_i         | trickle_int_i     |  |
| 78h  | InterruptStatus2      | rtc_rep_int_i     | stpup1_det_i     | stpup1_oc_i          | bat_temp_i        | sd4_lv_int_i    | sd3_lv_int_i       | sd2_lv_int_i        | sd1_lv_int_i      |  |
| 79h  | InterruptStatus3      | -                 |                  |                      |                   |                 | gpio_restart_int_i | gpio_int_i          | rtc_alarm_int_i   |  |
| 80h  | ChargerControl1       | nobat_ntc_det     | auto_resume      | bat_charging_enable  | usb_current<4:1>  |                 |                    |                     | usb_chgEn         |  |
| 81h  | ChargerVoltageControl | vsup_min<7:6>     |                  |                      | ChVoltEOC<5:0>    |                 |                    |                     |                   |  |
| 82h  | ChargerCurrentControl | eoc_current       | cc_lowlimit      | ConstantCurrent<5:2> |                   |                 |                    | TrickleCurrent<1:0> |                   |  |
| 83h  | Chargerconfig         | -                 | Charging_1Hz_clk | ChVoltResume         | temp_sel<4:3>     |                 | vsup_voltage<2:0>  |                     |                   |  |
| 84h  | NTCsupervision        | -                 |                  |                      |                   |                 | ntc_temp           | ntc_10k             | ntc_on            |  |
| 85h  | Chargersupervision    | -                 | ovprot_dis       | dcdc_chmode          | charging_tmax     | ch_timeout<3:0> |                    |                     |                   |  |

Table 32. Register Overview

| Addr | Name           | <D7>     | <D6>       | <D5> | <D4> | <D3>          | <D2>           | <D1>          | <D0>       |  |
|------|----------------|----------|------------|------|------|---------------|----------------|---------------|------------|--|
| 86h  | ChargerStatus1 | Nobat    | Battemp_hi | EOC  | CVM  | Trickle       | Resume         | CCM           | ChDet      |  |
| 87h  | ChargerStatus2 | -        |            |      |      |               | usb_prot_ready | batsw_on      | batsw_mode |  |
| 8eh  | LockRegister   | -        |            |      |      |               | charger_lock   | reg_lock<1:0> |            |  |
| 90h  | ASIC_ID1       | ID1<7:0> |            |      |      |               |                |               |            |  |
| 91h  | ASIC_ID2       | -        |            |      |      | revision<3:0> |                |               |            |  |

**SD1Voltage Register (Address 00h).**

| Addr: 00h |           | SD1Voltage |        |   |
|-----------|-----------|------------|--------|---|
| Bit       | Bit Name  | Default    | Access | Bit Description   |
| 7         | sd1_frequ | 0          | RW     | Selects between high and low frequency dependent on sd1_fsel<br><b>0</b> : 2MHz if <b>sd1_fsel=0</b> , 3MHz if <b>sd1_fsel=1</b><br><b>1</b> : 3MHz if <b>sd1_fsel=0</b> , 4MHz if <b>sd1_fsel=1</b>  |
| 6:0       | sd1_vsel  | 'b0000000  | RW     | The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down.<br><b>00h</b> : DC/DC powered down<br><b>01h-40h</b> : $V_{SD1}=0.6V+sd1\_vsel*12.5mV$<br><b>41h-70h</b> : $V_{SD1}=1.4V+(sd1\_vsel-40h)*25mV$<br><b>71h-7Fh</b> : $V_{SD1}=2.6V+(sd1\_vsel-70h)*50mV$ |

**SD2Voltage Register (Address 01h).**

| Addr: 01h |           | SD2Voltage |        |   |
|-----------|-----------|------------|--------|---|
| Bit       | Bit Name  | Default    | Access | Bit Description   |
| 7         | sd2_frequ | 0          | RW     | Selects between high and low frequency dependent on sd2_fsel<br><b>0</b> : 2MHz if <b>sd2_fsel=0</b> , 3MHz if <b>sd2_fsel=1</b><br><b>1</b> : 3MHz if <b>sd2_fsel=0</b> , 4MHz if <b>sd2_fsel=1</b>  |
| 6:0       | sd2_vsel  | 'b000 0000 | RW     | The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down.<br><b>00h</b> : DC/DC powered down<br><b>01h-40h</b> : $V_{SD2}=0.6V+sd2\_vsel*12.5mV$<br><b>41h-70h</b> : $V_{SD2}=1.4V+(sd2\_vsel-40h)*25mV$<br><b>71h-7Fh</b> : $V_{SD2}=2.6V+(sd2\_vsel-70h)*50mV$ |

**SD3Voltage Register (Address 02h).**

| Addr: 02h |           | SD3Voltage |        |   |
|-----------|-----------|------------|--------|---|
| Bit       | Bit Name  | Default    | Access | Bit Description   |
| 7         | sd3_frequ | 0          | RW     | Selects between high and low frequency dependent on sd3_fsel<br><b>0</b> : 2MHz if <b>sd3_fsel=0</b> , 3MHz if <b>sd3_fsel=1</b><br><b>1</b> : 3MHz if <b>sd3_fsel=0</b> , 4MHz if <b>sd3_fsel=1</b>  |
| 6:0       | sd3_vsel  | 'b000 0000 | RW     | The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down.<br><b>00h</b> : DC/DC powered down<br><b>01h-40h</b> : $V_{SD3}=0.6V+sd3\_vsel*12.5mV$<br><b>41h-70h</b> : $V_{SD3}=1.4V+(sd3\_vsel-40h)*25mV$<br><b>71h-7Fh</b> : $V_{SD3}=2.6V+(sd3\_vsel-70h)*50mV$ |

**SD4Voltage Register (Address 03h).**

| Addr: 03h |          | SD4Voltage |        |   |
|-----------|----------|------------|--------|---|
| Bit       | Bit Name | Default    | Access | Bit Description   |
| 7         | -        | 0          | RW     | -   |
| 6:0       | sd4_vsel | 'b000 0000 | RW     | The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down.<br><b>00h</b> : DC/DC powered down<br><b>01h-40h</b> : $V_{SD4}=0.6V+sd4\_vsel*12.5mV$<br><b>41h-70h</b> : $V_{SD4}=1.4V+(sd4\_vsel-40h)*25mV$<br><b>71h-7Fh</b> : $V_{SD4}=2.6V+(sd4\_vsel-70h)*50mV$ |

**LDO1Voltage Register (Address 04h).**

| Addr: 04h |             | LDO1Voltage |        |   |
|-----------|-------------|-------------|--------|---|
| Bit       | Bit Name    | Default     | Access | Bit Description   |
| 7         | ldo1_on     | 0           | RW     | Switch on of LDO1<br><b>0</b> : LDO off<br><b>1</b> : LDO on  |
| 6         | ldo1_ilimit | 0           | RW     | Sets limit of LDO1<br><b>0</b> : 150mA limit<br><b>1</b> : 250mA limit  |
| 4:0       | ldo1_vsel   | 'b0 0000    | RW     | The voltage select bits set the LDO output voltage<br><b>0h-0Fh</b> : $1.2V + ldo1\_vsel*50mV$<br><b>10h-1Fh</b> : $1.8V + (ldo1\_vsel-16)*100mV$ |

**LDO2Voltage Register (Address 05h).**

| Addr: 05h |             | LDO2Voltage |        |   |
|-----------|-------------|-------------|--------|---|
| Bit       | Bit Name    | Default     | Access | Bit Description   |
| 7         | ldo2_on     | 0           | RW     | Switch on of LDO2<br><b>0</b> : LDO off<br><b>1</b> : LDO on  |
| 6         | ldo2_ilimit | 0           | RW     | Sets limit of LDO2<br><b>0</b> : 150mA limit<br><b>1</b> : 250mA limit  |
| 4:0       | ldo2_vsel   | 'b0 0000    | RW     | The voltage select bits set the LDO output voltage<br><b>0h-0Fh</b> : $1.2V + ldo2\_vsel*50mV$<br><b>10h-1Fh</b> : $1.8V + (ldo2\_vsel-16)*100mV$ |

**LDO3Voltage Register (Address 06h).**

| Addr: 06h |             | LDO3Voltage |        |   |
|-----------|-------------|-------------|--------|---|
| Bit       | Bit Name    | Default     | Access | Bit Description   |
| 7         | ldo3_on     | 0           | RW     | Switch on of LDO3<br>0 : LDO off<br>1 : LDO on  |
| 6         | ldo3_ilimit | 0           | RW     | Sets limit of LDO3<br>0 : 150mA operating range<br>1 : 300mA operating range  |
| 5:0       | ldo3_vsel   | 'b00 0000   | RW     | The voltage select bits set the LDO output voltage<br>00h-10h : $V\_LDO3=0.9V+ldo3\_vsel*50mV$<br>11h-1fh : do not use<br>20h-3Fh : $V\_LDO3=1.75V+(ldo3\_vsel-20h)*50mV$ |

**LDO4Voltage Register (Address 07h).**

| Addr: 07h |             | LDO4Voltage |        |   |
|-----------|-------------|-------------|--------|---|
| Bit       | Bit Name    | Default     | Access | Bit Description   |
| 7         | ldo4_on     | 0           | RW     | Switch on of LDO4<br>0 : LDO off<br>1 : LDO on  |
| 6         | ldo4_ilimit | 0           | RW     | Sets limit of LDO4<br>0 : 150mA operating range<br>1 : 300mA operating range  |
| 5:0       | ldo4_vsel   | 'b00 0000   | RW     | The voltage select bits set the LDO output voltage<br>00h-10h : $V\_LDO4=0.9V+ldo4\_vsel*50mV$<br>11h-1fh : Do not use<br>20h-3Fh : $V\_LDO4=1.75V+(ldo4\_vsel-20h)*50mV$ |

**LDO5Voltage Register (Address 08h).**

| Addr: 08h |             | LDO5Voltage |        |   |
|-----------|-------------|-------------|--------|---|
| Bit       | Bit Name    | Default     | Access | Bit Description   |
| 7         | ldo5_on     | 0           | RW     | Switch on of LDO5<br>0 : LDO off<br>1 : LDO on  |
| 6         | ldo5_ilimit | 0           | RW     | Sets limit of LDO5<br>0 : 150mA operating range<br>1 : 300mA operating range  |
| 5:0       | ldo5_vsel   | 'b00 0000   | RW     | The voltage select bits set the LDO output voltage<br>00h-10h : $V\_LDO5=0.9V+ldo5\_vsel*50mV$<br>11h-1fh : Do not use<br>20h-3Fh : $V\_LDO5=1.75V+(ldo5\_vsel-20h)*50mV$ |

**LDO6Voltage Register (Address 09h).**

| Addr: 09h |             | LDO6Voltage |        |   |
|-----------|-------------|-------------|--------|---|
| Bit       | Bit Name    | Default     | Access | Bit Description   |
| 7         | ldo6_on     | 0           | RW     | Switch on of LDO6<br>0 : LDO off<br>1 : LDO on  |
| 6         | ldo6_ilimit | 0           | RW     | Sets limit of LDO6<br>0 : 150mA operating range<br>1 : 300mA operating range  |
| 5:0       | ldo6_vsel   | 'b00 0000   | RW     | The voltage select bits set the LDO output voltage<br>00h-10h : $V_{LDO6}=0.9V+ldo6\_vsel*50mV$<br>11h-1fh : Do not use<br>20h-3Fh : $V_{LDO6}=1.75V+(ldo6\_vsel-20h)*50mV$ |

**LDO7Voltage Register (Address 0ah).**

| Addr: 0ah |             | LDO7Voltage |        |   |
|-----------|-------------|-------------|--------|---|
| Bit       | Bit Name    | Default     | Access | Bit Description   |
| 7         | ldo7_on     | 0           | RW     | Switch on of LDO7<br>0 : LDO off<br>1 : LDO on  |
| 6         | ldo7_ilimit | 0           | RW     | Sets limit of LDO7<br>0 : 150mA operating range<br>1 : 300mA operating range  |
| 5:0       | ldo7_vsel   | 'b00 0000   | RW     | The voltage select bits set the LDO output voltage<br>00h-10h : $V_{LDO7}=0.9V+ldo7\_vsel*50mV$<br>11h-1fh : Do not use<br>20h-3Fh : $V_{LDO7}=1.75V+(ldo7\_vsel-20h)*50mV$ |

**LDO8Voltage Register (Address 0bh).**

| Addr: 0bh |             | LDO8Voltage |        |   |
|-----------|-------------|-------------|--------|---|
| Bit       | Bit Name    | Default     | Access | Bit Description   |
| 7         | ldo8_on     | 0           | RW     | Switch on of LDO8<br>0 : LDO off<br>1 : LDO on  |
| 6         | ldo8_ilimit | 0           | RW     | Sets limit of LDO8<br>0 : 150mA operating range<br>1 : 300mA operating range  |
| 5:0       | ldo8_vsel   | 'b00 0000   | RW     | The voltage select bits set the LDO output voltage<br>00h-10h : $V_{LDO8}=0.9V+ldo8\_vsel*50mV$<br>11h-1fh : Do not use<br>20h-3Fh : $V_{LDO8}=1.75V+(ldo8\_vsel-20h)*50mV$ |



**GPIO1control Register (Address 0ch).**

| Addr: 0ch |              | GPIO1control |        |   |
|-----------|--------------|--------------|--------|---|
| Bit       | Bit Name     | Default      | Access | Bit Description   |
| 7         | gpio1_invert | 0            | RW     | Invert GPIO input/output<br><b>0</b> : Normal mode<br><b>1</b> : Invert input or output   |
| 6:3       | gpio1_iosf   | 'b0000       | RW     | Select the GPIO special function<br><b>0</b> : Normal I/O operation<br><b>1</b> : Interrupt output<br><b>2</b> : VSUP_low output<br><b>3</b> : GPIO interrupt input<br><b>4</b> : Current sink PWM input<br><b>5</b> : Vselect input, (apply on <b>reg1_select</b> , <b>reg2_select</b> and <b>reg3_select</b> , if <b>gpio2_iosf</b> =5 then apply on <b>reg1_select</b> only)<br><b>6</b> : standby + Vselect + restart interrupt input<br><b>7</b> : pwr_good output<br><b>8</b> : Q32k output (if <b>osc_pd</b> =1 then internal RC oscillator with 32kHz divider is used)<br><b>9</b> : Watchdog input<br><b>10</b> : Charger active output<br><b>11</b> : EOC output<br><b>12</b> : 100/500mA charger input<br><b>13</b> : 500mA/2.5A charger input<br><b>14</b> : PWM output<br><b>15</b> : Charger enable input |
| 2:0       | gpio1_mode   | 'b011        | RW     | Selects the GPIO mode (I, I/O, Tri, Pulls)<br><b>0</b> : Input<br><b>1</b> : Output (push and pull)<br><b>2</b> : IO (open drain, only NMOS is active)<br><b>3</b> : Tristate<br><b>4</b> : Input with pullup<br><b>5</b> : Input with pulldown<br><b>6</b> : IO (open drain (NMOS) with pullup)<br><b>7</b> : n/a  |

**GPIO2control Register (Address 0dh).**

| Addr: 0dh |              | GPIO2control |        |   |
|-----------|--------------|--------------|--------|---|
| Bit       | Bit Name     | Default      | Access | Bit Description   |
| 7         | gpio2_invert | 0            | RW     | Invert GPIO input/output<br><b>0</b> : Normal mode<br><b>1</b> : Invert input or output   |
| 6:3       | gpio2_iosf   | 'b0000       | RW     | Select the GPIO special function<br><b>0</b> : Normal i/o operation<br><b>1</b> : Interrupt output<br><b>2</b> : VSUP_low output<br><b>3</b> : GPIO interrupt input<br><b>4</b> : Current sink PWM input<br><b>5</b> : Vselect input, (apply on <b>reg1_select</b> , <b>reg2_select</b> and <b>reg3_select</b> , if <b>gpio1_iosf</b> =5 then apply on <b>reg2_select</b> and <b>reg3_select</b> only)<br><b>6</b> : standby + Vselect + restart interrupt input<br><b>7</b> : pwr_good output<br><b>8</b> : Q32k output (if <b>osc_pd</b> =1 then internal RC oscillator with 32kHz divider is used)<br><b>9</b> : Stepup1 over-current output<br><b>10</b> : Charger active output<br><b>11</b> : EOC output<br><b>12</b> : 100/500mA charger input<br><b>13</b> : 500mA/2.5A charger input<br><b>14</b> : PWM output<br><b>15</b> : Charger enable input |
| 2:0       | gpio2_mode   | 'b011        | RW     | Selects the GPIO mode (I, I/O, Tri, Pulls)<br><b>0</b> : Input<br><b>1</b> : Output (push and pull)<br><b>2</b> : IO (open drain, only NMOS is active)<br><b>3</b> : ADC input (tristate)<br><b>4</b> : Input with pullup<br><b>5</b> : Input with pulldown<br><b>6</b> : IO (open drain (NMOS) with pullup)<br><b>7</b> : ADC input with pulldown  |

**GPIO3control Register (Address 0eh).**

| Addr: 0eh |              | GPIO3control |        |  |
|-----------|--------------|--------------|--------|--|
| Bit       | Bit Name     | Default      | Access | Bit Description  |
| 7         | gpio3_invert | 0            | RW     | Invert GPIO input/output<br><b>0</b> : Normal mode<br><b>1</b> : Invert input or output  |
| 6:3       | gpio3_iosf   | 'b0000       | RW     | Select the GPIO special function<br><b>0</b> : Normal i/o operation<br><b>1</b> : Interrupt output<br><b>2</b> : VSUP_low output<br><b>3</b> : GPIO interrupt input<br><b>4</b> : Currentsink PWM input<br><b>5</b> : Vselect input, (apply on <b>reg1_select</b> , <b>reg2_select</b> and <b>reg3_select</b> )<br><b>6</b> : standby + Vselect + restart interrupt input<br><b>7</b> : pwr_good output<br><b>8</b> : Q32k output (if osc_pd=1 then internal RC oscillator with 32kHz divider is used)<br><b>9</b> : Stepup1 over-current output<br><b>10</b> : Charger active output<br><b>11</b> : EOC output<br><b>12</b> : 100/500mA charger input<br><b>13</b> : 500mA/2.5A charger input<br><b>14</b> : PWM output<br><b>15</b> : Charger enable input |
| 2:0       | gpio3_mode   | 'b011        | RW     | Selects the GPIO mode (I, I/O, Tri, Pulls)<br><b>0</b> : Input<br><b>1</b> : Output (push and pull)<br><b>2</b> : IO (open drain, only NMOS is active)<br><b>3</b> : ADC input (tristate)<br><b>4</b> : Input with pullup<br><b>5</b> : Input with pulldown<br><b>6</b> : IO (open drain (NMOS) with pullup)<br><b>7</b> : ADC input with pulldown   |

**GPIO4control Register (Address 0fh).**

| Addr: 0fh |              | GPIO4control |        |   |
|-----------|--------------|--------------|--------|---|
| Bit       | Bit Name     | Default      | Access | Bit Description   |
| 7         | gpio4_invert | 0            | RW     | Invert GPIO input/output<br>0 : Normal mode<br>1 : Invert input or output   |
| 6:3       | gpio4_iosf   | 'b0000       | RW     | Select the GPIO special function<br>0 : Normal i/o operation<br>1 : Interrupt output<br>2 : VSUP_low output<br>3 : GPIO interrupt input<br>4 : Currentsink PWM input<br>5 : Vselect input, (apply on <b>reg1_select</b> , <b>reg2_select</b> and <b>reg3_select</b> )<br>6 : standby + Vselect + restart interrupt input<br>7 : pwr_good output<br>8 : Q32k output (if osc_pd=1 then internal RC oscillator with 32kHz divider is used)<br>9 : Watchdog input<br>10 : Charger active output<br>11 : EOC output<br>12 : 100/500mA charger input<br>13 : 500mA/2.5A charger input<br>14 : PWM output<br>15 : Charger enable input |
| 2:0       | gpio4_mode   | 'b011        | RW     | Selects the GPIO mode (I, I/O, Tri, Pulls)<br>0 : Input<br>1 : Output (push and pull)<br>2 : IO (open drain, only NMOS is active)<br>3 : ADC input (tristate)<br>4 : Input with pullup<br>5 : Input with pulldown<br>6 : IO (open drain (NMOS) with pullup)<br>7 : ADC input with pulldown  |

**SD\_control Register (Address 10h).**

| Addr: 10h |            | SD_control |        |  |
|-----------|------------|------------|--------|--|
| Bit       | Bit Name   | Default    | Access | Bit Description                                      |
| 7:4       | -          | 'b0000     | n/a    | do not use   |
| 3         | sd4_enable | 'b1        | RW     | Global stepdown4 enable<br>0 : SD4 off<br>1 : SD4 on |
| 2         | sd3_enable | 'b1        | RW     | Global stepdown3 enable<br>0 : SD3 off<br>1 : SD3 on |
| 1         | sd2_enable | 'b1        | RW     | Global stepdown2 enable<br>0 : SD2 off<br>1 : SD2 on |
| 0         | sd1_enable | 'b1        | RW     | Global stepdown1 enable<br>0 : SD1 off<br>1 : SD1 on |

**GPIOsignal\_out Register (Address 20h).**

| Addr: 20h |           | GPIOsignal_out |        |  |
|-----------|-----------|----------------|--------|--|
| Bit       | Bit Name  | Default        | Access | Bit Description  |
| 7:4       | -         | 'b0000         | n/a    | do not use   |
| 3         | gpio4_out | 0              | RW     | This bit determines the output signal of the GPIO4 pin when selected as output source. |
| 2         | gpio3_out | 0              | RW     | This bit determines the output signal of the GPIO3 pin when selected as output source. |
| 1         | gpio2_out | 0              | RW     | This bit determines the output signal of the GPIO2 pin when selected as output source. |
| 0         | gpio1_out | 0              | RW     | This bit determines the output signal of the GPIO1 pin when selected as output source. |

**GPIOsignal\_in Register (Address 21h).**

| Addr: 21h |          | GPIOsignal_in |        |  |
|-----------|----------|---------------|--------|--|
| Bit       | Bit Name | Default       | Access | Bit Description  |
| 7:4       | -        | 'b0000        | n/a    | do not use   |
| 3         | gpio4_in | 0             | RO     | This bit reflects the logic level of the GPIO4 pin when configured as digital input pin. |
| 2         | gpio3_in | 0             | RO     | This bit reflects the logic level of the GPIO3 pin when configured as digital input pin. |
| 1         | gpio2_in | 0             | RO     | This bit reflects the logic level of the GPIO2 pin when configured as digital input pin. |
| 0         | gpio1_in | 0             | RO     | This bit reflects the logic level of the GPIO1 pin when configured as digital input pin. |

**Reg1\_Voltage Register (Address 22h).**

| Addr: 22h |              | Reg1_Voltage |        |   |
|-----------|--------------|--------------|--------|---|
| Bit       | Bit Name     | Default      | Access | Bit Description   |
| 7:0       | reg1_voltage | 'b0000 0000  | RW     | This register is mapped to the register address 0h+Reg1_select , if gioX_iosf = 5 or 6 (Vselect input), and the GPIOx input = 1. This feature allows voltage switching of a predefined regulator with just one GPIO input.<br><b>0 ..FFh</b> : Selects voltage, ilimit, on or frequency bits of LDO or DCDC |

**Reg2\_Voltage Register (Address 23h).**

| Addr: 23h |              | Reg2_Voltage |        |  |
|-----------|--------------|--------------|--------|--|
| Bit       | Bit Name     | Default      | Access | Bit Description  |
| 7:0       | reg2_voltage | 'b0000 0000  | RW     | This register is mapped to the register address 0h+Reg3_select , if gioX_iosf=5 or 6 (Vselect input), and GPIOx input = 1, This feature allows voltage switching of a predefined regulator with just one GPIO input<br><b>0 ..FFh</b> : Selects voltage, ilimit, on or frequency bits of LDO or DCDC |

**Reg\_control Register (Address 24h).**

| Addr: 24h |             | Reg_control |        |  |
|-----------|-------------|-------------|--------|--|
| Bit       | Bit Name    | Default     | Access | Bit Description  |
| 7:4       | reg2_select | 'b1111      | RW     | Selects regulator for mapping feature; if reg_select2 ≥ 0Ch, then feature is disabled. |
| 3:0       | reg1_select | 'b1111      | RW     | Selects regulator for mapping feature; if reg_select1 ≥ 0Ch, then feature is disabled. |

**GPIOctrl\_sd Register (Address 25h).**

| Addr: 25h |               | GPIOctrl_sd |        |   |
|-----------|---------------|-------------|--------|---|
| Bit       | Bit Name      | Default     | Access | Bit Description   |
| 7:6       | gpio_ctrl_sd4 | 'b00        | RW     | Enable GPIO control of DCDC SD4. GPIO ctrl only enabled, if <b>sd4_vsel</b> > 0<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : Controlled by GPIO3 |
| 5:4       | gpio_ctrl_sd3 | 'b00        | RW     | Enable GPIO control of DCDC SD3. GPIO ctrl only enabled, if <b>sd3_vsel</b> > 0<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : Controlled by GPIO3 |
| 3:2       | gpio_ctrl_sd2 | 'b00        | RW     | Enable GPIO control of DCDC SD2. GPIO ctrl only enabled, if <b>sd2_vsel</b> > 0<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : Controlled by GPIO3 |
| 1:0       | gpio_ctrl_sd1 | 'b00        | RW     | Enable GPIO control of DCDC SD1. GPIO ctrl only enabled, if <b>sd1_vsel</b> > 0<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : Controlled by GPIO3 |

**GPIOctrl\_Ido1 Register (Address 26h).**

| Addr: 26h |                | GPIOctrl_Ido1 |        |  |
|-----------|----------------|---------------|--------|--|
| Bit       | Bit Name       | Default       | Access | Bit Description  |
| 7:6       | gpio_ctrl_ido4 | 'b00          | RW     | Enable GPIO control of LDO4. GPIO ctrl only enabled, if <b>Ido4_on</b> = 1<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : Controlled by GPIO3 |
| 5:4       | gpio_ctrl_ido3 | 'b00          | RW     | Enable GPIO control of LDO3. GPIO ctrl only enabled, if <b>Ido3_on</b> = 1<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : Controlled by GPIO3 |
| 3:2       | gpio_ctrl_ido2 | 'b00          | RW     | Enable GPIO control of LDO2. GPIO ctrl only enabled, if <b>Ido2_on</b> = 1<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : Controlled by GPIO3 |
| 1:0       | gpio_ctrl_ido1 | 'b00          | RW     | Enable GPIO control of LDO1. GPIO ctrl only enabled, if <b>Ido1_on</b> = 1<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : Controlled by GPIO3 |

**GPIOctrl\_Ido2 Register (Address 27h).**

| Addr: 27h |                | GPIOctrl_Ido2 |        |  |
|-----------|----------------|---------------|--------|--|
| Bit       | Bit Name       | Default       | Access | Bit Description  |
| 7:6       | gpio_ctrl_ido8 | 'b00          | RW     | Enable GPIO control of LDO8. GPIO ctrl only enabled, if <b>Ido8_on</b> = 1<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : Controlled by GPIO3 |
| 5:4       | gpio_ctrl_ido7 | 'b00          | RW     | Enable GPIO control of LDO7. GPIO ctrl only enabled, if <b>Ido7_on</b> = 1<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : Controlled by GPIO3 |
| 3:2       | gpio_ctrl_ido6 | 'b00          | RW     | Enable GPIO control of LDO6. GPIO ctrl only enabled, if <b>Ido6_on</b> = 1<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : Controlled by GPIO3 |
| 1:0       | gpio_ctrl_ido5 | 'b00          | RW     | Enable GPIO control of LDO5. GPIO ctrl only enabled, if <b>Ido5_on</b> = 1<br><b>0</b> : No GPIO control<br><b>1</b> : Controlled by GPIO1<br><b>2</b> : Controlled by GPIO2<br><b>3</b> : Controlled by GPIO3 |

**Reg3\_Voltage Register (Address 2bh).**

| Addr: 2bh |              | Reg3_Voltage |        |  |
|-----------|--------------|--------------|--------|--|
| Bit       | Bit Name     | Default      | Access | Bit Description  |
| 7:0       | reg3_voltage | 'b0000 0000  | RW     | This register is mapped to the register address 0h+Reg3_select , if gioX_josf=5 or 6 (Vselect input), and GPIOx input = 1, This feature allows voltage switching of a predefined regulator with just one GPIO input<br><b>0 ..FFh</b> : Selects voltage, ilimit, on or frequency bits of LDO or DCDC |

**Reg\_control3 Register (Address 2ch).**

| Addr: 2ch |             | Reg_control3 |        |  |
|-----------|-------------|--------------|--------|--|
| Bit       | Bit Name    | Default      | Access | Bit Description  |
| 7:4       | -           | 'b0000       | n/a    | do not use   |
| 3:0       | reg3_select | 'b1111       | RW     | Selects regulator for mapping feature; if reg_select3 ≥ 0Ch, then feature is disabled. |



**SD\_control1 Register (Address 30h).**

| Addr: 30h |               | SD_control1 |        |  |
|-----------|---------------|-------------|--------|--|
| Bit       | Bit Name      | Default     | Access | Bit Description  |
| 7         | sd4_low_noise | 0           | RW     | Enables low noise mode of SD4. If enabled, smaller current pulses and output ripple is activated.<br><b>0</b> : Normal mode. Minimum current pulses of >100mA applied in skip mode.<br><b>1</b> : Low noise mode. Only minimum on time applied in skip mode. |
| 6         | sd3_low_noise | 0           | RW     | Enables low noise mode of SD3. If enabled, smaller current pulses and output ripple is activated.<br><b>0</b> : Normal mode. Minimum current pulses of >100mA applied in skip mode.<br><b>1</b> : Low noise mode. Only minimum on time applied in skip mode. |
| 5         | sd2_low_noise | 0           | RW     | Enables low noise mode of SD2. If enabled, smaller current pulses and output ripple is activated.<br><b>0</b> : Normal mode. Minimum current pulses of >100mA applied in skip mode.<br><b>1</b> : Low noise mode. Only minimum on time applied in skip mode. |
| 4         | sd1_low_noise | 0           | RW     | Enables low noise mode of SD1. If enabled, smaller current pulses and output ripple is activated.<br><b>0</b> : Normal mode. Minimum current pulses of >100mA applied in skip mode.<br><b>1</b> : Low noise mode. Only minimum on time applied in skip mode. |
| 3         | sd4_fast      | 0           | RW     | Selects a faster regulation mode for SD4 suitable for larger load changes.<br><b>0</b> : normal mode<br><b>1</b> : fast mode, double Cext required (see external components)   |
| 2         | sd3_fast      | 0           | RW     | Selects a faster regulation mode for SD3 suitable for larger load changes.<br><b>0</b> : normal mode<br><b>1</b> : fast mode, double Cext required (see external components)   |
| 1         | sd2_fast      | 0           | RW     | Selects a faster regulation mode for SD2 suitable for larger load changes.<br><b>0</b> : normal mode<br><b>1</b> : fast mode, double Cext required (see external components)   |
| 0         | sd1_fast      | 0           | RW     | Selects a faster regulation mode for SD1 suitable for larger load changes.<br><b>0</b> : normal mode<br><b>1</b> : fast mode, double Cext required (see external components)   |

**SD\_control2 Register (Address 31h).**

| Addr: 31h |               | SD_control2 |        |  |
|-----------|---------------|-------------|--------|--|
| Bit       | Bit Name      | Default     | Access | Bit Description  |
| 7:6       | sd_dvm_select | 'b00        | RW     | Apply DVM counter to the following DCDC converter:<br><b>0</b> : Select SD1 for DVM<br><b>1</b> : Select SD2 for DVM<br><b>2</b> : Select SD3 for DVM<br><b>3</b> : Select SD4 for DVM   |
| 5:4       | dvm_time      | 'b00        | RW     | Time steps of DVM voltage change of selected step down, if voltage of step Down is changed during operation (sd <sub>x</sub> _vsel) voltage is decreased/increased by single steps 12.5mV<br><b>0</b> : 0 µsec, immediate change (no DVM)<br><b>1</b> : 4 µsec time delay between steps<br><b>2</b> : 8 µsec time delay between steps<br><b>3</b> : 16 µsec time delay between steps |
| 3         | sd3_slave     | 0           | RW     | Enables slave mode of SD3<br><b>0</b> : Normal mode of SD3<br><b>1</b> : SD3 is slave of SD2   |
| 2         | sd3_fsel      | 0           | RW     | Selects between high and low frequency range<br><b>0</b> : 2 or 3MHz frequency (selectable by <b>sd3_frequ</b> )<br><b>1</b> : 3 or 4MHz frequency (selectable by <b>sd3_frequ</b> )   |
| 1         | sd2_fsel      | 0           | RW     | Selects between high and low frequency range<br><b>0</b> : 2 or 3MHz frequency (selectable by <b>sd2_frequ</b> )<br><b>1</b> : 3 or 4MHz frequency (selectable by <b>sd2_frequ</b> )   |
| 0         | sd1_fsel      | 0           | RW     | Selects between high and low frequency range<br><b>0</b> : 2 or 3MHz frequency (selectable by <b>sd1_frequ</b> )<br><b>1</b> : 3 or 4MHz frequency (selectable by <b>sd1_frequ</b> )   |

**Battery\_voltage\_monitor Register (Address 32h).**

| Addr: 32h |             | Battery_voltage_monitor |          |   |
|-----------|-------------|-------------------------|----------|---|
| Bit       | Bit Name    | Default                 | Access   | Bit Description   |
| 7         | FastResEn   | 0                       | RW       | <b>0</b> : ResVoltFall debounce time = 3msec<br><b>1</b> : ResVoltFall debounce time = 4µsec  |
| 6         | SupResEn    | 0                       | RW       | <b>0</b> : A reset is generated if VSUP falls below 2.7V **<br><b>1</b> : A reset is generated if VSUP falls below ResVoltFall<br>** If VBAT falls below ResVoltFall only an interrupt is generated (if enabled) and the µProcessor can shut down the system)   |
| 5:3       | ResVoltFall | 'b000                   | RW       | This value determines the reset level ResVoltFall for falling VBAT. It is recommended to set this value at least 200mV lower than ResVoltRise<br><b>0</b> : 2.7V<br><b>1</b> : 2.9V<br><b>2</b> : 3.1V<br><b>3</b> : 3.2V<br><b>4</b> : 3.3V<br><b>5</b> : 3.4V<br><b>6</b> : 3.5V<br><b>7</b> : 3.6V |
| 2:0       | ResVoltRise | 'b000                   | RO (OTP) | This value determines the reset level ResVoltRise for rising VBAT. It is recommended to set this value at least 200mV higher than ResVoltFall<br><b>0</b> : 2.7V<br><b>1</b> : 2.9V<br><b>2</b> : 3.1V<br><b>3</b> : 3.2V<br><b>4</b> : 3.3V<br><b>5</b> : 3.4V<br><b>6</b> : 3.5V<br><b>7</b> : 3.6V |

**Startup\_Control Register (Address 33h).**

| Addr: 33h |                      | Startup_Control |          |   |
|-----------|----------------------|-----------------|----------|---|
| Bit       | Bit Name             | Default         | Access   | Bit Description   |
| 7:2       | -                    | 'b00 0000       | n/a      | do not use  |
| 1         | chg_pwr_off_en       | 0               | RO (OTP) | Select charger detection in power off mode Read only (OTP setting)<br><b>0</b> : Exit of Power Off mode, if charger is detected (level detection)<br><b>1</b> : Exit of Power Off mode, if charger insertion is detected (rising edge detection) .  |
| 0         | power_off_at_vsuplow | 0               | RW       | Switch on Power off mode if low VSUP is detected during active or standby mode (Pin ON= low and bit auto_off=0)<br><b>0</b> : If low battery is detected, battery voltage is continuously monitored and chip startup initiated if battery voltage is above ResVoltRise<br><b>1</b> : If low battery is detected, enter power off mode |

**ResetTimer Register (Address 34h).**

| Addr: 34h |                    | ResetTimer |        |   |
|-----------|--------------------|------------|--------|---|
| Bit       | Bit Name           | Default    | Access | Bit Description   |
| 7         | -                  | 'b0        | n/a    | do not use  |
| 6         | stby_reset_disable | 0          | RW     | Disable Reset output signal (pin XRES) in standby mode.<br>0 : Normal mode, reset is active in standby mode<br>1 : No reset in standby mode and during exit of standby mode         |
| 5         | auto_off           | 0          | RO     | Defines startup behavior at first battery insertion<br>0 : Startup of chip if VBAT>ResVoltRise<br>1 : Enter power off mode (Startup with ON key or charger insertion)               |
| 4:3       | off_delay          | 'b01       | RW     | Set Delay between I2C command, GPIO or Reset signal for power_off, standby mode or reset and execution of that command.<br>0 : No delay<br>1 : 8 msec<br>2 : 16 msec<br>3 : 32 msec |
| 2         | -                  | 'b0        | n/a    | do not use  |
| 1:0       | res_timer          | 'b00       | RW     | Set RESTime, after the last regulator has started<br>0 : RESTIME = 10ms<br>1 : RESTIME = 50ms<br>2 : RESTIME = 100ms<br>3 : RESTIME = 150ms   |

**ReferenceControl Register (Address 35h).**

| Addr: 35h |                   | ReferenceControl |        |   |
|-----------|-------------------|------------------|--------|---|
| Bit       | Bit Name          | Default          | Access | Bit Description   |
| 7         | on_reset_delay    | 0                | RW     | Sets the on reset delay time<br><b>0</b> : 8 sec (if <b>onkey_reset=1</b> )<br><b>1</b> : 4 sec (if <b>onkey_reset=1</b> )  |
| 6         | reg_low_bias_mode | 0                | RW     | Sets the on reset delay time<br><b>0</b> : normal operation<br><b>1</b> : reduces the bias for the analog LDO1 and LDO2   |
| 5         | clk_div2          | 0                | RW     | Divide internal clock oscillator by 2 to reduce quiescent current for low power operation<br><b>0</b> : Normal mode<br><b>1</b> : Internal clock frequency divided by two. All timings are increased by two. Switching frequency of all DCDC converters are divided by two. Reduced transient performance of DCDC converters.   |
| 4         | standby_mode_on   | 0                | RW     | Setting to 1 sets the PMU into standby mode. All regulators are disabled except those regulators enabled by register Reg standby mode. XRES will be pulled to low. A normal startup of all regulators will be done with any interrupt (has to be enabled before entering standby mode). During this startup, regulators defined by Reg standby mode register are continuously on. |
| 3:1       | clk_int           | 'b000            | RW     | Sets the internal CLK frequency $f_{CLK}$ used for DCDCs, PWM, ...<br><b>0</b> : 4 MHz (default)<br><b>1</b> : 3.8 MHz<br><b>2</b> : 3.6 MHz<br><b>3</b> : 3.4 MHz<br><b>4</b> : 3.2 MHz<br><b>5</b> : 3.0 MHz<br><b>6</b> : 2.8 MHz<br><b>7</b> : 2.6 MHz<br>All frequencies, timings and delays in this datasheet are based on 4MHz <b>clk_int</b>                              |
| 0         | low_power_on      | 0                | RW     | Enable low power mode of internal reference.<br><b>0</b> : Standard mode<br><b>1</b> : Low power mode - all specification except noise parameters are still valid. Iq reduced by approx. 30 $\mu$ A   |

**ResetControl Register (Address 36h).**

| Addr: 36h |              | ResetControl |        |  |
|-----------|--------------|--------------|--------|--|
| Bit       | Bit Name     | Default      | Access | Bit Description  |
| 7         | onkey_reset  | 0            | RW     | 0 : Reset after 4/8 seconds ON pressed disabled<br>1 : Reset after 4/8 seconds ON pressed enabled  |
| 6:3       | reset_reason | 'b0000       | RW     | Flags to indicate to the software the reason for the last reset<br>0 : V <sub>POR</sub> has been reached (battery or charger insertion from scratch)<br>1 : <b>ResVoltFall</b> was reached (battery voltage drop below 2.75V)<br>2 : Software forced by <b>force_reset</b><br>3 : Software forced by <b>power_off</b> and ON was pulled high<br>4 : Software forced by <b>power_off</b> and charger was detected<br>5 : External triggered through the pin XRES<br>6 : Reset caused by overtemperature T140<br>7 : Reset caused by watchdog<br>8 : Reset caused by 4/8 seconds ON press<br>9 : NA<br>10 : Reset caused by RTC repeated wakeup or alarm wakeup<br>11 : Reset caused by interrupt in standby mode<br>12 : Reset caused by ON pulled high in standby mode |
| 2         | on_input     | 0            | R_PUSH | <b>Read:</b> This flag represents the state of the ON pad directly<br><b>Write:</b> Setting to 1 resets the 4/8 sec. <b>onkey_reset</b> timer  |
| 1         | power_off    | 0            | RW     | Setting to 1 starts a reset cycle, but waits after the Reg_off state for a rising edge on the pin ON or until the charger is detected.   |
| 0         | force_reset  | 0            | RW     | Setting to 1 starts a complete reset cycle   |

**OvertemperatureControl Register (Address 37h).**

| Addr: 37h |                 | OvertemperatureControl |        |  |
|-----------|-----------------|------------------------|--------|--|
| Bit       | Bit Name        | Default                | Access | Bit Description  |
| 7:4       | -               | 'b0000                 | n/a    | do not use   |
| 3         | rst_ov_temp_140 | 0                      | RW     | If the over-temperature threshold 2 has been reached, the flag <b>ov_temp_140</b> is set and a reset cycle is started. <b>ov_temp_140</b> should be reset by writing 1 and afterward 0 to <b>rst_ov_temp_140</b> . |
| 2         | ov_temp_140     | 0                      | RO     | Flag that the over-temperature threshold 2 (T140) has been reached - this flag is not reset by a over-temperature caused reset and has to be reset by <b>rst_ov_temp_140</b> .                                     |
| 1         | ov_temp_110     | 0                      | RO     | Flag that the over-temperature threshold 1 (T110) has been reached   |
| 0         | temp_pmc_on     | 1                      | RO     | Switch on / off of temperature supervision; default: on - all other bits are only valid if set to 1. Leave at 1, do not disable  |

**WatchdogControl Register (Address 38h).**

| Addr: 38h |             | WatchdogControl |        |   |
|-----------|-------------|-----------------|--------|---|
| Bit       | Bit Name    | Default         | Access | Bit Description   |
| 7:2       | -           | 'b00 0000       | n/a    | do not use  |
| 1         | wtdg_res_on | 0               | RW     | If the watchdog expires and wtdg_res_on = 1 a reset cycle will be started     |
| 0         | wtdg_on     | 0               | RW     | Switches on the complete watchdog<br>0 : Watchdog off<br>1 : Watchdog enabled |

**Reg\_standby\_mod1 Register (Address 39h).**

| Addr: 39h |               | Reg_standby_mod1 |        |   |
|-----------|---------------|------------------|--------|---|
| Bit       | Bit Name      | Default          | Access | Bit Description   |
| 7         | disable_regpd | 0                | RW     | This bit disables the pulldown of all regulators<br>0 : Normal operation approx. 1k $\Omega$ pulldown of all regulators<br>1 : Pulldown disabled >100k $\Omega$ of all regulators |
| 6:4       | -             | b000             | n/a    | do not use  |
| 3         | sd4_stby_on   | 0                | RW     | Enable Step down 4 in standby mode  |
| 2         | sd3_stby_on   | 0                | RW     | Enable Step down 3 in standby mode  |
| 1         | sd2_stby_on   | 0                | RW     | Enable Step down 2 in standby mode  |
| 0         | sd1_stby_on   | 0                | RW     | Enable Step down 1 in standby mode  |

**Reg\_standby\_mod2 Register (Address 3ah).**

| Addr: 3ah |              | Reg_standby_mod2 |        |                             |
|-----------|--------------|------------------|--------|-----------------------------|
| Bit       | Bit Name     | Default          | Access | Bit Description             |
| 7         | ldo8_stby_on | 0                | RW     | Enable LDO8 in standby mode |
| 6         | ldo7_stby_on | 0                | RW     | Enable LDO7 in standby mode |
| 5         | ldo6_stby_on | 0                | RW     | Enable LDO6 in standby mode |
| 4         | ldo5_stby_on | 0                | RW     | Enable LDO5 in standby mode |
| 3         | ldo4_stby_on | 0                | RW     | Enable LDO4 in standby mode |
| 2         | ldo3_stby_on | 0                | RW     | Enable LDO3 in standby mode |
| 1         | ldo2_stby_on | 0                | RW     | Enable LDO2 in standby mode |
| 0         | ldo1_stby_on | 0                | RW     | Enable LDO1 in standby mode |

**curr\_control Register (Address 40h).**

| Addr: 40h |            | curr_control |        |   |
|-----------|------------|--------------|--------|---|
| Bit       | Bit Name   | Default      | Access | Bit Description   |
| 7:4       | curr3_ctrl | 'b0000       | RW     | On/Off control of the pad CURRE3<br><b>0</b> : Current sink is turned off<br><b>1</b> : Current sink is active<br><b>2</b> : Current sink is active and LED string connected to SU2. Required for automatic feedback selection.<br><b>3</b> : Controlled by internal PWM generator, or external, if gpioX_iosf=4<br><b>4</b> : XINT output (active low interrupt output)<br><b>5</b> : VSUP_low output<br><b>6</b> : Charger active output<br><b>7</b> : EOC output<br><b>8</b> : Inverted signal of ON pin as output<br><b>9</b> : Signal of ON pin as output<br><b>10</b> : Q32k output (if osc_pd=1 then internal RC oscillator with 32kHz divider is used)<br><b>11</b> : PWM output<br><b>12</b> : PWRGOOD output<br><b>13-15</b> : NA |
| 3:2       | curr2_ctrl | 'b00         | RW     | On/Off control of the pad CURRE2<br><b>0</b> : Current sink is turned off<br><b>1</b> : Current sink is active<br><b>2</b> : Current sink is active and LED string connected to SU2. Required for automatic feedback selection.<br><b>3</b> : Controlled by internal PWM generator, or external, if gpioX_iosf=4  |
| 1:0       | curr1_ctrl | 'b00         | RW     | On/Off control of the pad CURRE1<br><b>0</b> : Current sink is turned off<br><b>1</b> : Current sink is active<br><b>2</b> : Current sink is active and LED string connected to SU2. Required for automatic feedback selection.<br><b>3</b> : Controlled by internal PWM generator, or external, if gpioX_iosf=4  |

**pwm\_control\_l Register (Address 41h).**

| Addr: 41h |            | pwm_control_l |        |  |
|-----------|------------|---------------|--------|--|
| Bit       | Bit Name   | Default       | Access | Bit Description  |
| 7:0       | pwm_l_time | 'b00000000    | RW     | This bit defines the low time of the PWM generator in 1MHz units.<br><b>0</b> : $\text{pwm\_div} * 1\mu\text{sec}$<br><b>1</b> : $\text{pwm\_div} * 2\mu\text{sec}$<br><b>2</b> : $\text{pwm\_div} * 3\mu\text{sec}$<br>... : ...<br><b>255</b> : $\text{pwm\_div} * 256\mu\text{sec}$ |



**pwm\_control\_h Register (Address 42h).**

| Addr: 42h |            | pwm_control_h |        |   |
|-----------|------------|---------------|--------|---|
| Bit       | Bit Name   | Default       | Access | Bit Description   |
| 7:0       | pwm_h_time | 'b00000000    | RW     | This bit defines the high time of the PWM generator in 1MHz units.<br><b>0</b> : pwm_div * 1µsec<br><b>1</b> : pwm_div * 2µsec<br><b>2</b> : pwm_div * 3µsec<br>... : ...<br><b>255</b> : pwm_div * 256µsec |

**curr1\_value Register (Address 43h).**

| Addr: 43h |               | curr1_value |        |   |
|-----------|---------------|-------------|--------|---|
| Bit       | Bit Name      | Default     | Access | Bit Description   |
| 7:0       | curr1_current | 'b00000000  | RW     | Defines the current into CURR1, if enabled by curr1_ctrl<br><b>0</b> : Power down (default state)<br><b>1</b> : 0.15mA (LSB)<br>... : ...<br><b>255</b> : 38.25mA |

**curr2\_value Register (Address 44h).**

| Addr: 44h |               | curr2_value |        |   |
|-----------|---------------|-------------|--------|---|
| Bit       | Bit Name      | Default     | Access | Bit Description   |
| 7:0       | curr2_current | 'b00000000  | RW     | Defines the current into CURR2, if enabled by curr2_ctrl<br><b>0</b> : Power down (default state)<br><b>1</b> : 0.15mA (LSB)<br>... : ...<br><b>255</b> : 38.25mA |

**curr3\_value Register (Address 45h).**

| Addr: 45h |               | curr3_value |        |   |
|-----------|---------------|-------------|--------|---|
| Bit       | Bit Name      | Default     | Access | Bit Description   |
| 7:0       | curr3_current | 'b00000000  | RW     | Defines the current into CURR3, if enabled by curr3_ctrl<br><b>0</b> : Power down (default state)<br><b>1</b> : 0.15mA (LSB)<br>... : ...<br><b>255</b> : 38.25mA |

**Watchdog\_min\_timer Register (Address 46h).**

| Addr: 46h |                | Watchdog_min_timer |        |  |
|-----------|----------------|--------------------|--------|--|
| Bit       | Bit Name       | Default            | Access | Bit Description  |
| 7:0       | wtdg_min_timer | 'b00000000         | RW     | Defines the minimum watchdog trigger time (LSB=7.5ms, range: 0 - 1.9s) |

**Watchdog\_max\_timer Register (Address 47h).**

| Addr: 47h |                | Watchdog_max_timer |        |   |
|-----------|----------------|--------------------|--------|---|
| Bit       | Bit Name       | Default            | Access | Bit Description   |
| 7:0       | wtdg_max_timer | 'b11111111         | RW     | Defines the maximum watchdog trigger time (LSB=7.5ms, range: 7.5ms - 1.9s), do not set to (00)h |

**WatchdogSoftwareSignal Register (Address 48h).**

| Addr: 48h |             | WatchdogSoftwareSignal |        |   |
|-----------|-------------|------------------------|--------|---|
| Bit       | Bit Name    | Default                | Access | Bit Description   |
| 7:6       | pwm_div     | 'b00                   | RW     | This bit defines the divider ratio of the prescaler for the PWM generator.<br><b>0</b> : Divide by 1<br><b>1</b> : Divide by 2<br><b>2</b> : Divide by 4<br><b>3</b> : Divide by 16 |
| 0         | wtdg_sw_sig | 0                      | PUSH   | Trigger input by the serial interface if gpioX_josf<>9  |

**Stepup\_control1 Register (Address 50h).**

| Addr: 50h |              | Stepup_control1 |        |  |
|-----------|--------------|-----------------|--------|--|
| Bit       | Bit Name     | Default         | Access | Bit Description  |
| 7:3       | stepup1_v    | 'b0000          | RW     | Defines the tuning current at FB_SU1 pin;<br><b>0</b> : 0 $\mu$ A<br><b>1</b> : 1 $\mu$ A<br>... : ...<br><b>31</b> : 31 $\mu$ A   |
| 2         | stepup1_res  | 0               | RW     | Gain selection for DCDC SU1<br><b>0</b> : If FB_SU1 is used with current feedback only (Only R1,C1 connected)<br><b>1</b> : If FB_SU1 is used with external resistor divider (2 resistors) |
| 1         | stepup1_freq | 0               | RW     | Selects SU1 frequency<br><b>0</b> : 1 MHz<br><b>1</b> : 0.5 MHz  |
| 0         | stepup1_on   | 0               | RW     | On/Off control of SU1<br><b>0</b> : SU1 off<br><b>1</b> : SU1 on   |

**Stepup\_control2 Register (Address 51h).**

| Addr: 51h |              | Stepup_control2 |        |   |
|-----------|--------------|-----------------|--------|---|
| Bit       | Bit Name     | Default         | Access | Bit Description   |
| 7:3       | stepup2_v    | 'b00000         | RW     | Defines the tuning current at FB_SU2 pin<br><b>0</b> : 0 $\mu$ A<br><b>1</b> : 1 $\mu$ A<br>... : ...<br><b>31</b> : 31 $\mu$ A   |
| 2         | stepup2_res  | 0               | RW     | Gain selection for DCDC SU2<br><b>0</b> : If DCDC is used with current feedback (CURR1,CURR2,CURR3) or if FB_SU2 is used with current feedback only (Only R1,C1 connected)<br><b>1</b> : If FB_SU2 is used with external resistor divider (2 resistors) |
| 1         | stepup2_freq | 0               | RW     | Selects SU3 frequency<br><b>0</b> : 1 MHz<br><b>1</b> : 0.5 MHz   |
| 0         | stepup2_on   | 0               | RW     | On/Off control of SU2<br><b>0</b> : SU2 off<br><b>1</b> : SU2 on  |

**Stepup\_control4 Register (Address 53h).**

| Addr: 53h |                   | Stepup_control4 |        |   |
|-----------|-------------------|-----------------|--------|---|
| Bit       | Bit Name          | Default         | Access | Bit Description   |
| 7         | stpup1_det        | 0               | RO     | SU1 detection status register<br><b>0</b> : VRsense < V <sub>DETECT</sub> for more than 1ms, and DCDC SU1 converter is in pulseskip for more than 1ms.<br><b>1</b> : VRsense > V <sub>DETECT</sub> for more than 1ms, or the DCDC SU1 converter is not in pulseskip for more than 1ms.  |
| 6         | stpup1_oc         | 0               | RO     | SU1 overcurrent status bit<br><b>0</b> : VRsense < V <sub>OVCURRENT</sub><br><b>1</b> : VRsense > V <sub>OVCURRENT</sub> for more than 5ms (latched state)  |
| 5         | stpup1_oc_timeout | 0               | RW     | Controls GPIOx switch-off, after overcurrent timeout (5ms) for DCDC SU1<br><b>0</b> : Disabled<br><b>1</b> : Enabled  |
| 4         | stpup1_shortprot  | 0               | RW     | Enables Protection and Detection circuit for DCDC SU1<br><b>0</b> : No protection and load detection<br><b>1</b> : Short protection and load detection enabled  |
| 3         | stpup2_pwm_lowf   | 0               | RW     | Selects PWM operation of SU2<br><b>0</b> : High frequency operation PWM>20kHz**<br><b>1</b> : Low frequency PWM operation: <b>stepup2_on</b> and curr1...3_on (if PWM enabled) switched off during PWM low time<br>** Step_up switched on all the time. (current sinks are not switched off (currX_on=1 all the time), but currX_current masked to 00h during PWM low time.). During PWM off-time then feedback voltage is sampled. |
| 2         | stepup2_prot_dis  | 0               | RW     | DCDC SU2 overvoltage protection to prevent damage of external NFET, if CURR1, CURR2 or CURR3 feedback selected, and no LED string connected.<br><b>0</b> : Switch off DCDC SU2 if the voltage on FB_SU2 exceeds 1.25V<br><b>1</b> : Overvoltage protection disabled   |
| 1:0       | stepup2_fb        | 'b00            | RW     | Controls the feedback source<br><b>0</b> : voltage feedback (external resistor divider) selected by <b>stepup2_fbprot</b><br><b>1</b> : CURR1 feedback enabled (feedback through white LEDs)<br><b>2</b> : CURR2 feedback enabled (feedback through white LEDs)<br><b>3</b> : CURR3 feedback enabled (feedback through white LEDs)  |

**Stepup\_control5 Register (Address 54h).**

| Addr: 54h |                  | Stepup_control5 |        |  |
|-----------|------------------|-----------------|--------|--|
| Bit       | Bit Name         | Default         | Access | Bit Description  |
| 7:4       | -                | 'b0000          | n/a    | do not use   |
| 3         | stepup2_pwm_mode | 0               | RW     | Enable PWM mode<br>0 : Normal operation<br>1 : PWM mode operation. Feedback is sampled during PWM off-time, if stpup2_lowf=0.  |
| 2         | stepup12_clkinv  | 0               | RW     | Invert input clock of SU1 and SU2 converter<br>0 : Use positive edge of internal clk<br>1 : Use negative edge of internal clk  |
| 1:0       | stepup2_fbprot   | 'b00            | RW     | Controls the feedback protection of SU2 with external resistor divider (regulated to 0.8V).<br>0 : LX_SD4 enabled as input (If SD4 not used)<br>1 : GPIO2 enabled as input<br>2 : GPIO3 enabled as input<br>3 : GPIO4 enabled as input |

**RTCcontrol Register (Address 60h).**

| Addr: 60h |                     | RTCcontrol |        |  |
|-----------|---------------------|------------|--------|--|
| Bit       | Bit Name            | Default    | Access | Bit Description  |
| 7:5       | -                   | 'b000      | n/a    | do not use   |
| 4:3       | rtc_irq_mode        | 'b00       | RW     | 0 : Generates an interrupt every second<br>1 : Generates an interrupt every minute<br>2 : Generates an interrupt every 2 minute<br>3 : Generates an interrupt every 8 minute |
| 2         | rtc_on              | 0          | RW     | Switch on the 32kHz RTC oscillator<br>0 : 32kHz oscillator disabled<br>1 : 32kHz oscillator enabled  |
| 1         | rtc_alarm_wakeup_en | 0          | RW     | 0 : Disables RTC alarm wake-up in power off mode<br>1 : Enable RTC alarm wake-up in power off mode   |
| 0         | rtc_rep_wakeup_en   | 0          | RW     | 0 : Disables RTC repeated wake-up in power off mode<br>1 : Enable RTC repeated wake-up in power off mode   |

**RTCSecond Register (Address 61h).**

| Addr: 61h |          | RTCSecond |        |                 |
|-----------|----------|-----------|--------|-----------------|
| Bit       | Bit Name | Default   | Access | Bit Description |
| 7:0       | second   | 00h       | RW     | -               |

**RTCMinute1 Register (Address 62h).**

| Addr: 62h |          | RTCMinute1 |        |                 |
|-----------|----------|------------|--------|-----------------|
| Bit       | Bit Name | Default    | Access | Bit Description |
| 7:0       | minute0  | 00h        | RW     | -               |

**RTCMinute2 Register (Address 63h).**

| Addr: 63h |          | RTCMinute2 |        |                 |
|-----------|----------|------------|--------|-----------------|
| Bit       | Bit Name | Default    | Access | Bit Description |
| 7:0       | minute1  | 00h        | RW     | -               |

**RTCMinute3 Register (Address 64h).**

| Addr: 64h |          | RTCMinute3 |        |                 |
|-----------|----------|------------|--------|-----------------|
| Bit       | Bit Name | Default    | Access | Bit Description |
| 7:0       | minute2  | 00h        | RW     | -               |

**RTCAlarmSecond Register (Address 65h).**

| Addr: 65h |             | RTCAlarmSecond |        |  |
|-----------|-------------|----------------|--------|--|
| Bit       | Bit Name    | Default        | Access | Bit Description  |
| 7:0       | alarmsecond | 3Fh            | RW     | AlarmMinute2 has to be written to latch the whole alarm register |

**RTCAlarmMinute Register (Address 66h).**

| Addr: 66h |              | RTCAlarmMinute |        |  |
|-----------|--------------|----------------|--------|--|
| Bit       | Bit Name     | Default        | Access | Bit Description  |
| 7:0       | alarmminute0 | FFh            | RW     | AlarmMinute2 has to be written to latch the whole alarm register |

**RTCAlarmMinute2 Register (Address 67h).**

| Addr: 67h |              | RTCAlarmMinute2 |        |  |
|-----------|--------------|-----------------|--------|--|
| Bit       | Bit Name     | Default         | Access | Bit Description  |
| 7:0       | alarmminute1 | FFh             | RW     | AlarmMinute2 has to be written to latch the whole alarm register |

**RTCAlarmMinute3 Register (Address 68h).**

| Addr: 68h |              | RTCAlarmMinute3 |        |                 |
|-----------|--------------|-----------------|--------|-----------------|
| Bit       | Bit Name     | Default         | Access | Bit Description |
| 7:0       | alarmminute2 | FFh             | RW     | -               |

**SRAM Register (Address 69h).**

| Addr: 69h |          | SRAM    |        |                 |
|-----------|----------|---------|--------|-----------------|
| Bit       | Bit Name | Default | Access | Bit Description |
| 7:0       | SRAM     | 00h     | RW     | -               |

**ADC\_control Register (Address 70h).**

| Addr: 70h |                  | ADC_control |        |  |
|-----------|------------------|-------------|--------|--|
| Bit       | Bit Name         | Default     | Access | Bit Description  |
| 7         | start_conversion | 0           | RW     | Writing a 1 into this bit starts one ADC conversion  |
| 6         | adc_on           | 0           | RW     | Writing a 1 into this bit continuously activates the ADC S/H and the input multiplexer. The ADC and the MUX are also activated for a conversion period when <b>start_conversion</b> is set to 1. Useful for high impedance input sources on ADC inputs   |
| 5         | adc_slow         | 0           | RW     | Select ADC sampling frequency<br><b>0</b> : 250kHz (conversion time: approx. 60µs)<br><b>1</b> : 62.5kHz (conversion time: approx. 240µs)  |
| 4         | gpio_lv          | 0           | RW     | <b>0</b> : High voltage range of GPIO1...4/SENSEN_SU1 (4:1 divider active)<br><b>1</b> : Low voltage range of GPIO1...4/SENSEN_SU1 (1:1 divider, 1.8V max)   |
| 3:0       | adc_select       | 'b0000      | RW     | Selects an ADC channel<br><b>0</b> : BATTEMP NTCADCIN (1:1)<br><b>1</b> : Temperature sensor: DIE temperature [C] = adc_result * 0.866 - 274 (1:1)<br><b>2</b> : XOUT32K (1:1, 1.8Vmax)<br><b>3</b> : CURR1 (1:1, 1V max)<br><b>4</b> : CURR2 (1:1, 1V max)<br><b>5</b> : CURR3 (1:1, 1V max)<br><b>6</b> : VUSB(15:1, 15V max)<br><b>7</b> : CHGIN (4:1)<br><b>8</b> : VBAT (4:1)<br><b>9</b> : VSUP (4:1)<br><b>10</b> : SENSEN_SU1 (4:1 or 1:1 )<br><b>11</b> : LX_SD4 (4:1 or 1:1 )<br><b>12</b> : GPIO2 (4:1 or 1:1 )<br><b>13</b> : GPIO3 (4:1 or 1:1 )<br><b>14</b> : GPIO4 (4:1 or 1:1 )<br><b>15</b> : NA |

**ADC\_MSB\_result Register (Address 71h).**

| Addr: 71h |                  | ADC_MSB_result |        |   |
|-----------|------------------|----------------|--------|---|
| Bit       | Bit Name         | Default        | Access | Bit Description   |
| 7         | result_not_ready | 0              | RO     | Indicates end of conversion 0 result is ready 1 conversion is running |
| 6:0       | D9_3             | 'b000 0000     | RO     | ADC result register Bit9..Bit3  |

**ADC\_LSB\_result Register (Address 72h).**

| Addr: 72h |          | ADC_LSB_result |        |                                 |
|-----------|----------|----------------|--------|---------------------------------|
| Bit       | Bit Name | Default        | Access | Bit Description                 |
| 7:3       | -        | 'b0000 0       | n/a    | do not use                      |
| 2:0       | D2_0     | 'b000          | RO     | ADC result register Bit2...Bit0 |

**RegStatus Register (Address 73h).**

| Addr: 73h |          | RegStatus |        |   |
|-----------|----------|-----------|--------|---|
| Bit       | Bit Name | Default   | Access | Bit Description   |
| 7         | curr3_lv | 0         | RO     | Bit is set when voltage of current sink CURR3 drops below low voltage threshold (1ms debounce time default) |
| 6         | curr2_lv | 0         | RO     | Bit is set when voltage of current sink CURR2 drops below low voltage threshold (1ms debounce time default) |
| 5         | curr1_lv | 0         | RO     | Bit is set when voltage of current sink CURR1 drops below low voltage threshold (1ms debounce time default) |
| 4         | -        | 0         | n/a    | do not use  |
| 3         | sd4_lv   | 0         | RO     | Bit is set when voltage of SD4 drops below low voltage threshold (-5%) (1ms debounce time default)          |
| 2         | sd3_lv   | 0         | RO     | Bit is set when voltage of SD3 drops below low voltage threshold (-5%) (1ms debounce time default)          |
| 1         | sd2_lv   | 0         | RO     | Bit is set when voltage of SD2 drops below low voltage threshold (-5%) (1ms debounce time default)          |
| 0         | sd1_lv   | 0         | RO     | Bit is set when voltage of SD1 drops below low voltage threshold (-5%) (1ms debounce time default)          |

**InterruptMask1 Register (Address 74h).**

| Addr: 74h |               | InterruptMask1 |        |  |
|-----------|---------------|----------------|--------|--|
| Bit       | Bit Name      | Default        | Access | Bit Description  |
| 7         | LowBat_int_m  | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 6         | ovtmp_int_m   | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 5         | onkey_int_m   | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 4         | chdet_int_m   | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 3         | eoc_int_m     | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 2         | resume_int_m  | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 1         | nobat_int_m   | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 0         | trickle_int_m | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |



**InterruptMask2 Register (Address 75h).**

| Addr: 75h |               | InterruptMask2 |        |  |
|-----------|---------------|----------------|--------|--|
| Bit       | Bit Name      | Default        | Access | Bit Description  |
| 7         | rtc_rep_int_m | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 6         | stpup1_det_m  | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 5         | stpup1_oc_m   | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 4         | bat_temp_m    | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 3         | sd4_lv_int_m  | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 2         | sd3_lv_int_m  | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 1         | sd2_lv_int_m  | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 0         | sd1_lv_int_m  | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |

**InterruptMask3 Register (Address 76h).**

| Addr: 76h |                    | InterruptMask3 |        |  |
|-----------|--------------------|----------------|--------|--|
| Bit       | Bit Name           | Default        | Access | Bit Description  |
| 7:3       | -                  | 'b0000 0       | n/a    | do not use   |
| 2         | gpio_restart_int_m | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 1         | gpio_int_m         | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |
| 0         | rtc_alarm_int_m    | 1              | RW     | 0 : interrupt enabled<br>1 : interrupt masked (disabled) |

**InterruptStatus1 Register (Address 77h).**

| Addr: 77h |               | InterruptStatus1 |        |   |
|-----------|---------------|------------------|--------|---|
| Bit       | Bit Name      | Default          | Access | Bit Description                                     |
| 7         | LowBat_int_i  | 0                | POP    | Bit is set when VsUP drops below <b>ResVoltFall</b> |
| 6         | ovtmp_int_i   | 0                | POP    | Bit is set when 110deg is exceeded                  |
| 5         | onkey_int_i   | 0                | POP    | Rising and falling edge                             |
| 4         | chdet_int_i   | 0                | POP    | Rising and falling edge                             |
| 3         | eoc_int_i     | 0                | POP    | Rising and falling edge                             |
| 2         | resume_int_i  | 0                | POP    | Rising and falling edge                             |
| 1         | nobat_int_i   | 0                | POP    | Rising and falling edge                             |
| 0         | trickle_int_i | 0                | POP    | Rising and falling edge                             |

**InterruptStatus2 Register (Address 78h).**

| Addr: 78h |               | InterruptStatus2 |        |                         |
|-----------|---------------|------------------|--------|-------------------------|
| Bit       | Bit Name      | Default          | Access | Bit Description         |
| 7         | rtc_rep_int_i | 0                | POP    | Rising edge only        |
| 6         | stpup1_det_i  | 0                | POP    | Rising edge only        |
| 5         | stpup1_oc_i   | 0                | POP    | Rising edge only        |
| 4         | bat_temp_i    | 0                | POP    | Rising and falling edge |
| 3         | sd4_lv_int_i  | 0                | POP    | Rising edge only        |
| 2         | sd3_lv_int_i  | 0                | POP    | Rising edge only        |
| 1         | sd2_lv_int_i  | 0                | POP    | Rising edge only        |
| 0         | sd1_lv_int_i  | 0                | POP    | Rising edge only        |

**InterruptStatus3 Register (Address 79h).**

| Addr: 79h |                    | InterruptStatus3 |        |                         |
|-----------|--------------------|------------------|--------|-------------------------|
| Bit       | Bit Name           | Default          | Access | Bit Description         |
| 7:3       | -                  | 'b0000 0         | n/a    | do not use              |
| 2         | gpio_restart_int_i | 0                | POP    | Falling edge            |
| 1         | gpio_int_i         | 0                | POP    | Rising and falling edge |
| 0         | rtc_alarm_int_i    | 0                | POP    | Rising edge only        |

**ChargerControl1 Register (Address 80h).**

| Addr: 80h |                     | ChargerControl1 |        |  |
|-----------|---------------------|-----------------|--------|--|
| Bit       | Bit Name            | Default         | Access | Bit Description  |
| 7         | nobat_ntc_det       | 1               | RW     | Enables nobat_det feature with NTC, ntc_nobat debounce time=100ms  |
| 6         | auto_resume         | 1               | RW     | <b>0</b> : charger will stay in EOC even when the battery voltage drops<br><b>1</b> : charger will start charging when the battery voltage hits the resume level   |
| 5         | bat_charging_enable | 0               | RW     | <b>0</b> : USB is supplying VsUP, but battery switch is open. USB charger regulates to Vsup_voltage<br><b>1</b> : Normal battery charger operation form USB charger  |
| 4:1       | usb_current         | 'b1000          | RW     | Sets the USB input current limit, if not GPIO controlled<br><b>0</b> : 94mA (USB low current, also if gpiox_iosf=12 and gpiox=0)<br><b>1</b> : 141mA<br><b>2</b> : 189mA<br><b>3</b> : 237mA<br><b>4</b> : 285mA<br><b>5</b> : 332mA<br><b>6</b> : 380mA<br><b>7</b> : 428mA<br><b>8</b> : 470mA (USB high current, also if gpiox_iosf=12 and gpiox=1)<br><b>9</b> : 517mA<br><b>10</b> : 754A<br><b>11</b> : 1.29A<br><b>12</b> : 1.7A<br><b>13</b> : 2.53A<br><b>14</b> : 2.53A<br><b>15</b> : 2.53A |
| 0         | usb_chgEn           | 1               | RW     | ON/OFF control of USB charger input current limiter<br><b>0</b> : input current limiter disabled<br><b>1</b> : input current limiter enabled   |

**ChargerVoltageControl Register (Address 81h).**

| Addr: 81h |           | ChargerVoltageControl |        |  |
|-----------|-----------|-----------------------|--------|--|
| Bit       | Bit Name  | Default               | Access | Bit Description  |
| 7:6       | vsup_min  | 'b01                  | RW     | Regulate down battery charging current on that level of VsUP during trickle charging and constant current charging, to prevent voltage drop on VsUP.<br><b>0</b> : 3.9V<br><b>1</b> : 4.2V<br><b>2</b> : 4.50V<br><b>3</b> : 4.70V |
| 5:0       | ChVoltEOC | 'b10 0011             | RW     | Sets the end-of-charge voltage level V <sub>CHOFF</sub> (20mV steps)<br><b>0</b> : 3.5V<br><b>1</b> : 3.52V<br>... : ...<br><b>35</b> : 4.2V<br>... : ...<br><b>47-63</b> : 4.44V  |

**ChargerCurrentControl Register (Address 82h).**

| Addr: 82h |                 | ChargerCurrentControl |        |  |
|-----------|-----------------|-----------------------|--------|--|
| Bit       | Bit Name        | Default               | Access | Bit Description  |
| 7         | eoc_current     | 0                     | RW     | Sets eoc_current<br><b>0</b> : eoc current = <b>TrickleCurrent</b><br><b>1</b> : eoc current = <b>TrickleCurrent</b> / 2   |
| 6         | cc_lowlimit     | 1                     | RW     | Sets the range of the charging current limit in constant current mode.<br><b>0</b> : Normal mode<br><b>1</b> : Low current mode Current= <b>ConstantCurrent</b> - 500mA  |
| 5:2       | ConstantCurrent | 'b0000                | RW     | Sets the charging current limit in constant current mode.<br><b>0</b> : 750mA<br><b>1</b> : 800mA<br><b>2</b> : 850mA<br><b>3</b> : 900mA<br><b>4</b> : 950mA<br><b>5</b> : 1000mA<br><b>6</b> : 1050mA<br><b>7</b> : 1100mA<br><b>8</b> : 1150mA<br><b>9</b> : 1200mA<br><b>10</b> : 1250mA<br><b>11</b> : 1300mA<br><b>12</b> : 1350mA<br><b>13</b> : 1400mA<br><b>14</b> : 1450mA<br><b>15</b> : 1500mA |
| 1:0       | TrickleCurrent  | 'b01                  | RW     | Sets the charging current limit in trickle current mode.<br><b>0</b> : 60mA<br><b>1</b> : 120mA<br><b>2</b> : 180mA<br><b>3</b> : 240mA  |

**ChargerConfig Register (Address 83h).**

| Addr: 83h |                  | ChargerConfig |        |   |
|-----------|------------------|---------------|--------|---|
| Bit       | Bit Name         | Default       | Access | Bit Description   |
| 7         | -                | 0             | n/a    | do not use  |
| 6         | Charging_1Hz_clk | 0             | RW     | Sets the mode for the charging output status (gpioX_iosf=10)<br><b>0</b> : Normal operation: charging=1, not charging=0<br><b>1</b> : 1Hz blinking operation: charging=1Hz, not charging=0                      |
| 5         | ChVoltResume     | 0             | RW     | Sets the resume voltage level $V_{CHRES}$ .<br><b>0</b> : 120mV<br><b>1</b> : 240mV   |
| 4:3       | temp_sel         | 'b00          | RW     | Selects temperature regulation of charging current (die temperature)<br><b>0</b> : 110°C<br><b>1</b> : 90°C<br><b>2</b> : 120°C<br><b>3</b> : 130°C   |
| 2:0       | vsup_voltage     | 'b101         | RW     | Voltage regulation of VSUP of the input current limiter<br><b>0</b> : 4.4V<br><b>1</b> : 4.5V<br><b>2</b> : 4.6V<br><b>3</b> : 4.7V<br><b>4</b> : 4.8V<br><b>5</b> : 4.9V<br><b>6</b> : 5.0V<br><b>7</b> : 5.5V |

**NTCSupervision Register (Address 84h).**

| Addr: 84h |          | NTCSupervision |        |   |
|-----------|----------|----------------|--------|---|
| Bit       | Bit Name | Default        | Access | Bit Description   |
| 7:3       | -        | 'b0000 0       | n/a    | do not use  |
| 2         | ntc_temp | 0              | RW     | Select NTC mode<br><b>0</b> : 50deg temperature limit<br><b>1</b> : 45deg temperature limit |
| 1         | ntc_10k  | 0              | RW     | Select NTC resistor type<br><b>0</b> : 100kΩ<br><b>1</b> : 10kΩ                             |
| 0         | ntc_on   | 0              | RW     | ON/OFF control of battery NTC supervision<br><b>0</b> : Disabled<br><b>1</b> : Enabled      |

**Chargersupervision Register (Address 85h).**

| Addr: 85h |               | Chargersupervision |        |  |
|-----------|---------------|--------------------|--------|--|
| Bit       | Bit Name      | Default            | Access | Bit Description  |
| 7         | -             | 0                  | n/a    | do not use   |
| 6         | ovprot_dis    | 1                  | RW     | Disables external overvoltage protection, function of XOFF pin<br>0 : Overvoltage protection enabled<br>1 : Overvoltage protection disabled  |
| 5         | dcdc_chmode   | 1                  | RW     | Enables DCDC charger mode<br>0 : Linear charger mode enabled<br>1 : Step down charger enabled  |
| 4         | charging_tmax | 1                  | RW     | 0 : Read: no time-out reached, Write: reset charger time-out counter<br>1 : <b>ch_timeout</b> reached and charging stopped   |
| 3:0       | ch_timeout    | 'b0000             | RW     | Sets the charger time-out timer<br>0 : Off<br>1 : 0.5 hour<br>2 : 1 hour<br>3 : 1.5 hour<br>4 : 2 hour<br>5 : 2.5 hour<br>6 : 3 hour<br>7 : 3.5 hour<br>8 : 4 hour<br>9 : 4.5 hour<br>10 : 5 hour<br>11 : 5.5 hour<br>12 : 6 hour<br>13 : 6.5 hour<br>14 : 7 hour<br>15 : 7.5 hour |

**ChargerStatus1 Register (Address 86h).**

| Addr: 86h |            | ChargerStatus1 |        |   |
|-----------|------------|----------------|--------|---|
| Bit       | Bit Name   | Default        | Access | Bit Description   |
| 7         | Nobat      | 0              | RO     | Bit is set, if no battery has been detected (after EOC measured on NTC)               |
| 6         | Battemp_hi | 0              | RO     | Bit is set, if high battery temperature has been detected                             |
| 5         | EOC        | 0              | RO     | Bit is set, if End of charge state has been reached                                   |
| 4         | CVM        | 0              | RO     | Bit is set, if charger is operating in constant voltage mode                          |
| 3         | Trickle    | 0              | RO     | Bit is set, if charger is operating in trickle current. V <sub>BAT</sub> < 2.9V       |
| 2         | Resume     | 0              | RO     | Bit is set, if Battery voltage is below resume level                                  |
| 1         | CCM        | 0              | RO     | Bit is set, if charger is operating in constant current mode                          |
| 0         | ChDet      | 0              | RO     | Bit is set when external charge adapter has been detected on pin V <sub>CHARGER</sub> |

**ChargerStatus2 Register (Address 87h).**

| Addr: 87h |                | ChargerStatus2 |        |  |
|-----------|----------------|----------------|--------|--|
| Bit       | Bit Name       | Default        | Access | Bit Description  |
| 7:3       | -              | 'b0000 0       | n/a    | do not use   |
| 2         | usb_prot_ready | 0              | RO     | Bit indicates, that the USB input voltage protection pin X <sub>OFF</sub> is precharged to a voltage > 7.5V X <sub>OFF</sub> is pull to GND if an overvoltage on V <sub>USB</sub> is detected. |
| 1         | batsw_on       | 0              | RO     | Bits indicates the status of the battery switch  |
| 0         | batsw_mode     | 0              | RO     | <b>00</b> : Battery switch closed<br><b>01</b> : Battery switch open with ideal diode<br><b>10</b> : Charging mode<br><b>11</b> : Battery switch closed  |

**Lock Register (Address 8eh).**

| Addr: 8eh |              | Lock     |        |  |
|-----------|--------------|----------|--------|--|
| Bit       | Bit Name     | Default  | Access | Bit Description  |
| 7:3       | -            | 'b0000 0 | n/a    | do not use   |
| 2         | charger_lock | 0        | RW     | Enables lock of the following charger registers: 81h, 82h, 83h, Chargervoltagecontrol, Chargercurrentcontrol, Chargerconfig. Bits can only be set. Reset only with full reset cycle  |
| 1:0       | reg_lock     | 'b00     | RW     | Enables lock of Regulator voltages Bits can only be set. Reset only with full reset cycle<br><b>0</b> : No lock<br><b>1</b> : Lock of voltage of LDOs (LDO1..8_vsel) (all bits) and voltage of StepDownBits(sd1..4_vsel) [5:6] only<br><b>2</b> : Lock voltage of StepDownbits 5:6 only (no LDOs)<br><b>3</b> : Lock voltage of StepDowns (all bits) and LDOs (all bits).<br><b>Note:</b> Setting sdx_vsel to 0 is possible all the time to allow switching off the regulator. Writing a non-zero value after that will restore the old value. |

**ASIC\_ID1 Register (Address 90h).**

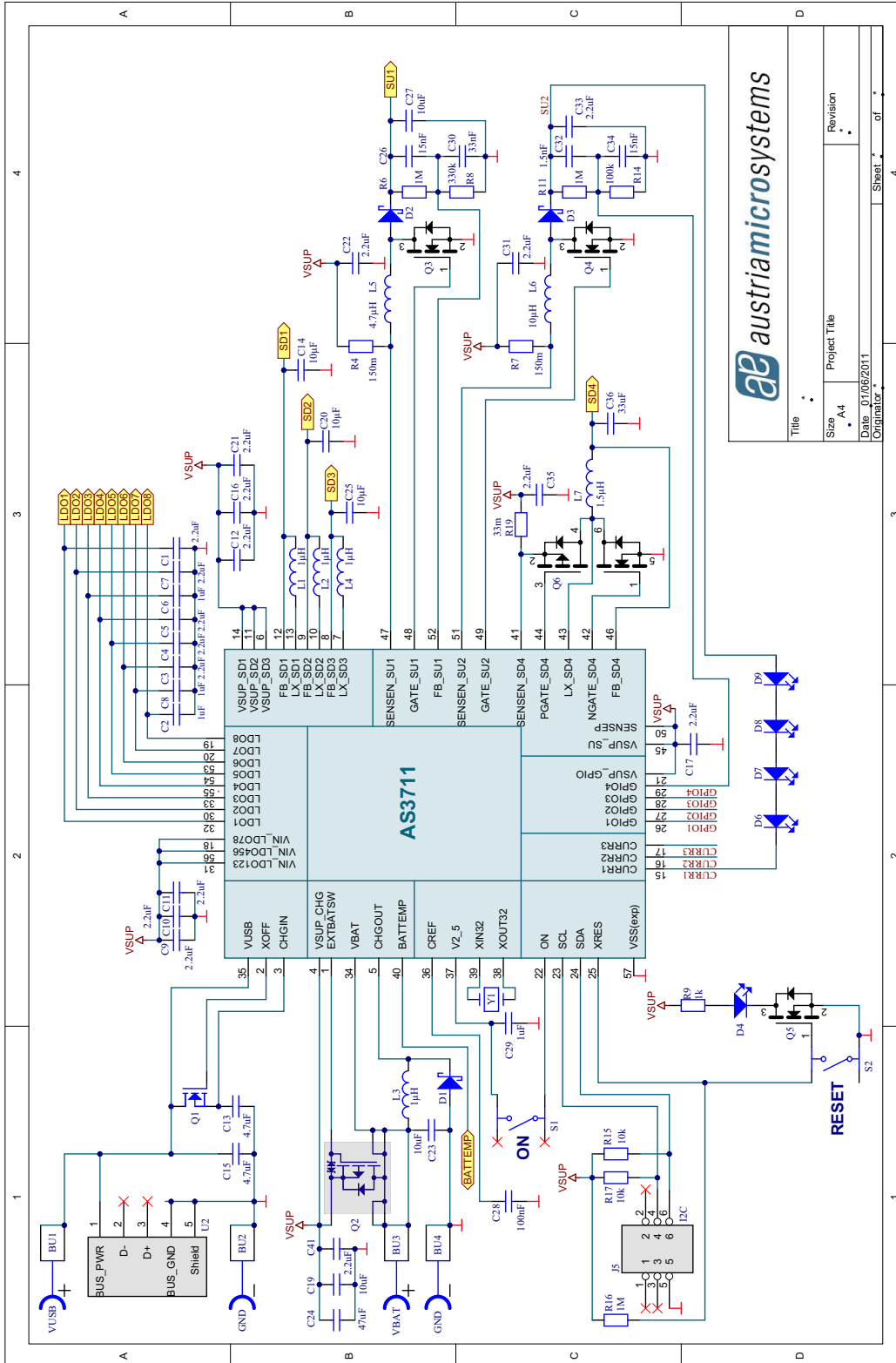
| Addr: 90h |          | ASIC_ID1 |        |                 |
|-----------|----------|----------|--------|-----------------|
| Bit       | Bit Name | Default  | Access | Bit Description |
| 7:0       | ID1      | 8Bh      | RO     | -               |

**ASIC\_ID2 Register (Address 91h).**

| Addr: 91h |          | ASIC_ID2 |        |                            |
|-----------|----------|----------|--------|----------------------------|
| Bit       | Bit Name | Default  | Access | Bit Description            |
| 3:0       | revision | 'b0000   | RO     | <b>Note:</b> Metal fuse!!! |

# 11 Application Information

Figure 37. AS3711 Application Schematic



**austriamicrosystems**

|           |               |
|-----------|---------------|
| Title     |               |
| Size      | Project Title |
| Date      | Revision      |
| Character |               |



Figure 38. PCB Layout Recommendation for SD1, SD2, SD3 and Switched Mode Charger

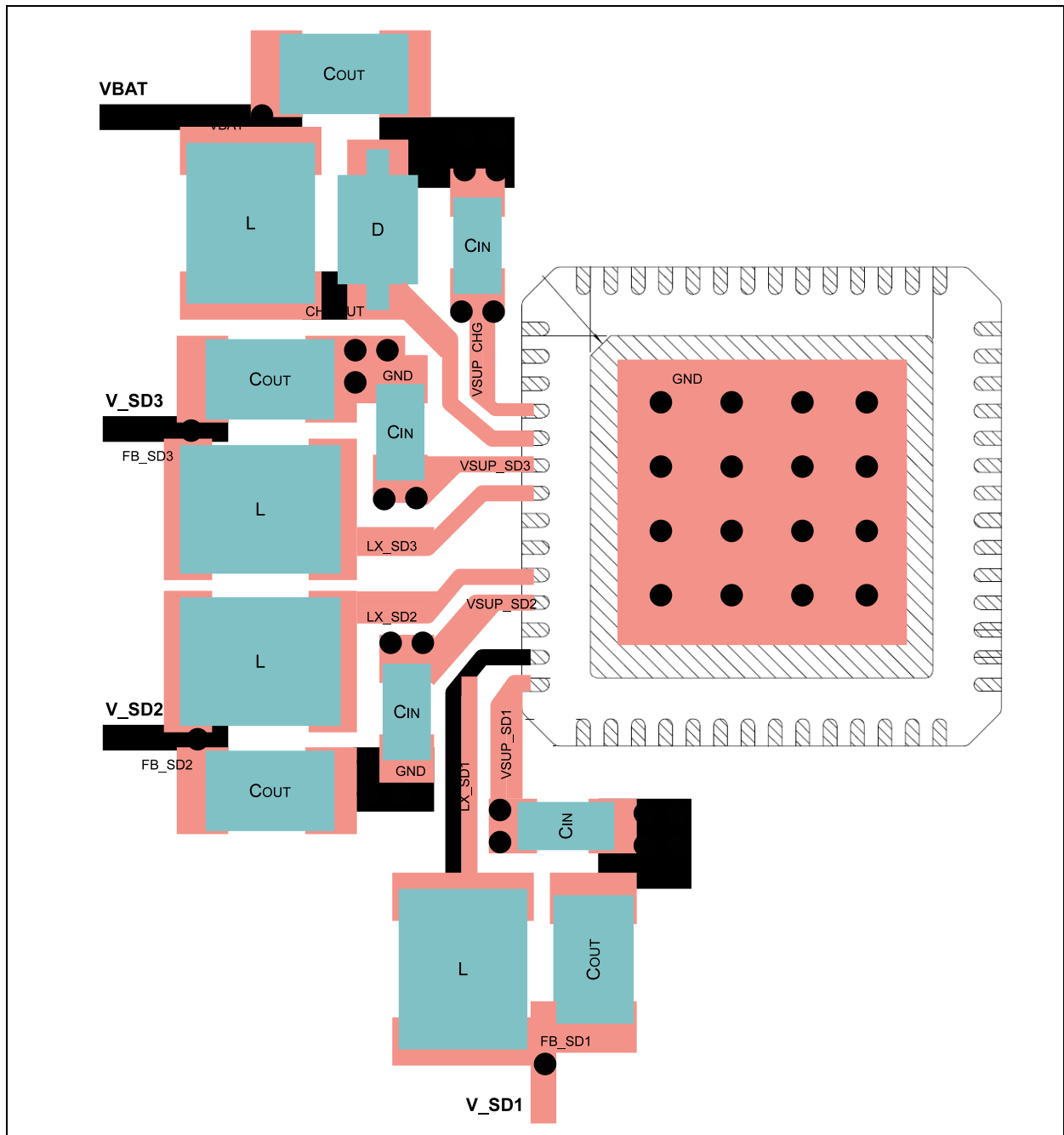
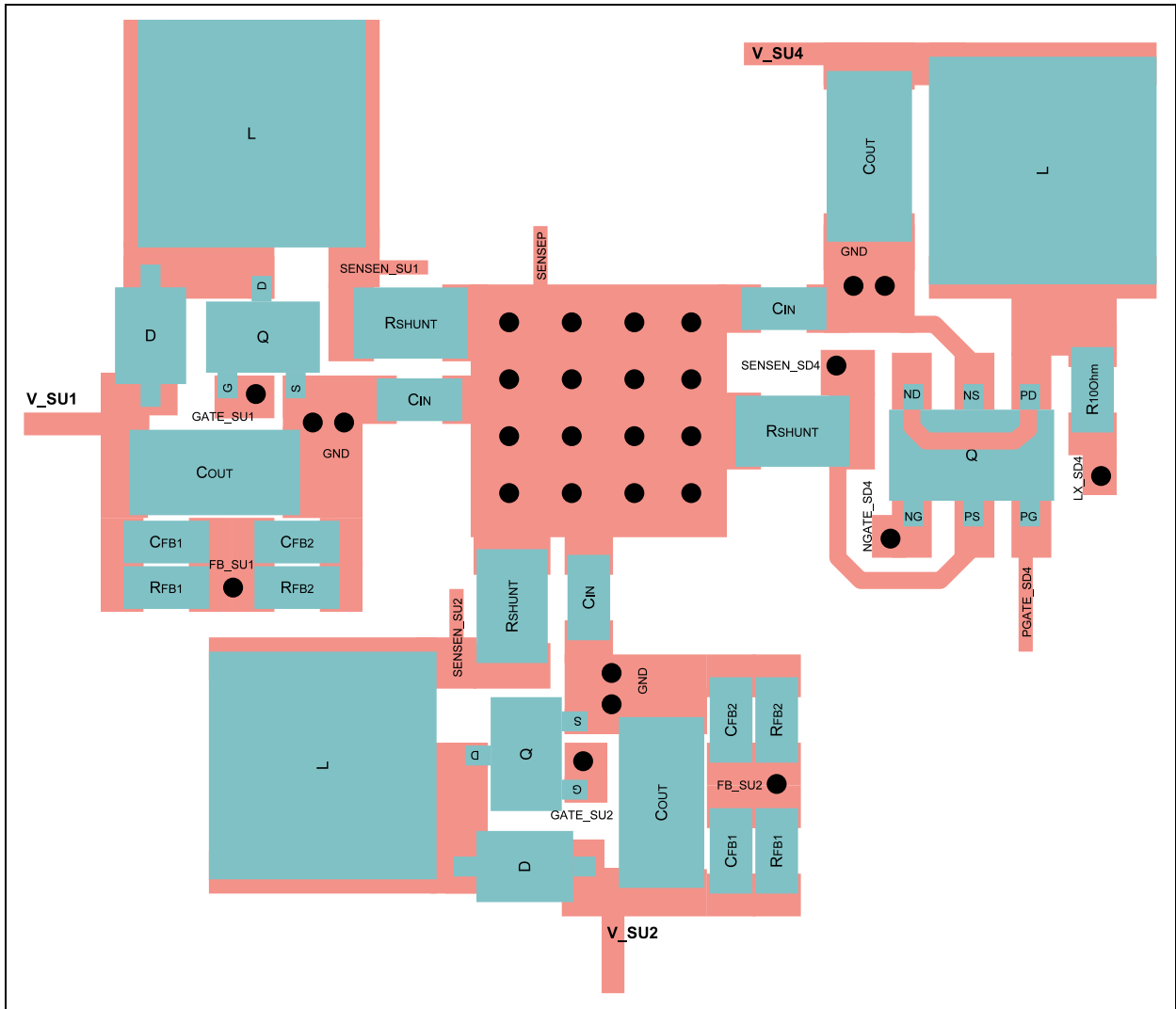


Figure 39. PCB Layout Recommendation for SU1, SU2, SD4



# 12 Package Drawings and Markings

Figure 40. Package Drawings and Dimensions

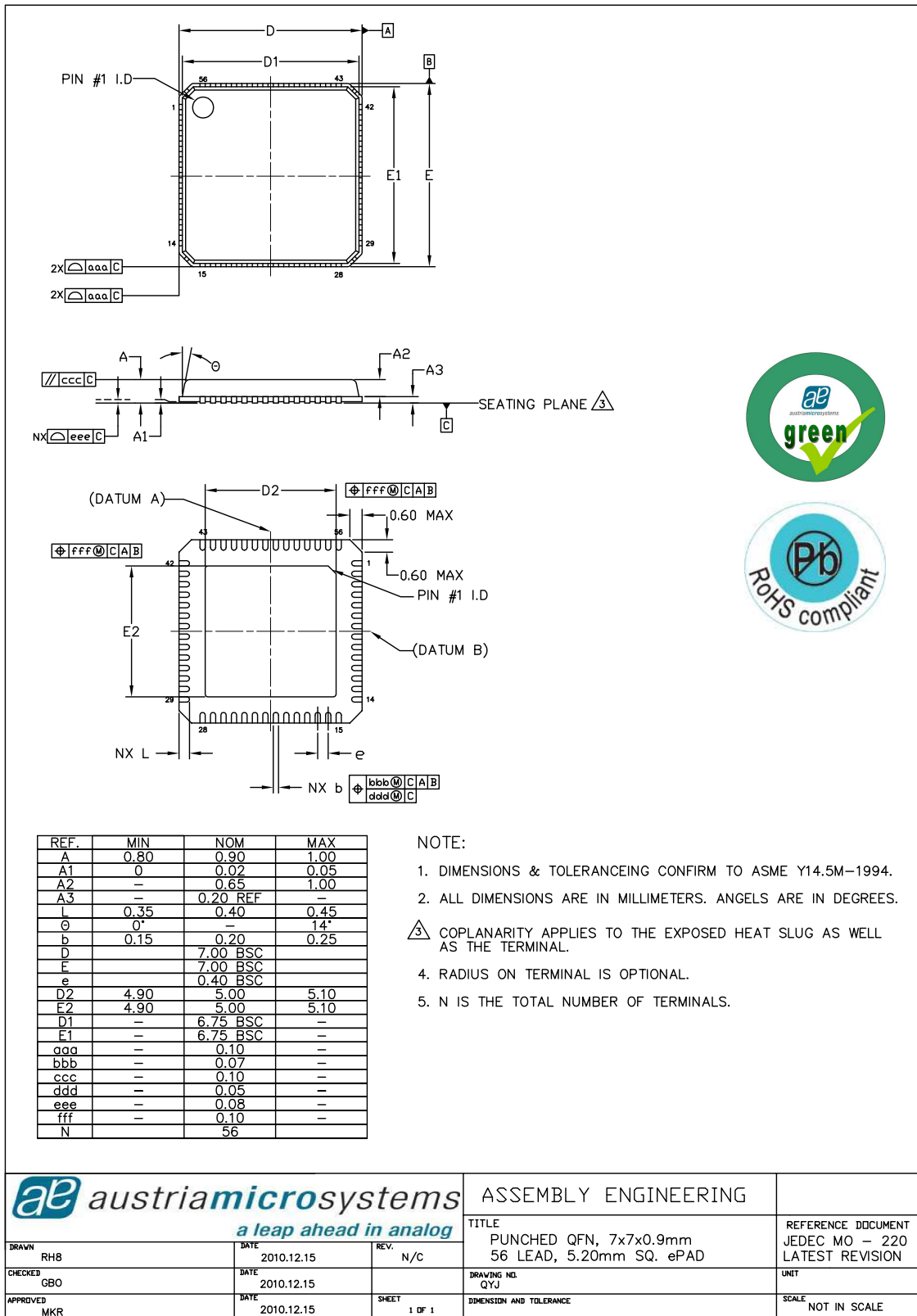


Figure 41. QFN Marking

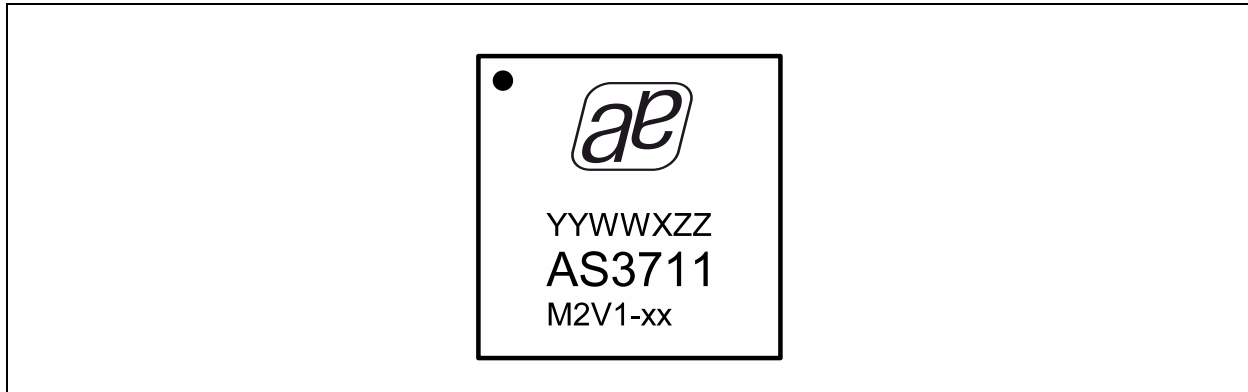


Table 33. Package Code YWWZZZ

| YY   | WW                                | X                | ZZ          |
|------|-----------------------------------|------------------|-------------|
| year | working week assembly / packaging | plant identifier | free choice |

Table 34. Start-up Revision Code

| xx | Sequence  |
|----|---|
| FF | engineering samples, no sequence programmed or sequence programmed on request |
| 00 | default sequence (no sequence programmed)                                     |
| xx | customer specified sequence programmed during production test                 |

## Revision History

| Revision | Date    | Owner    | Description  |
|----------|---------|----------|--|
| 0.10     | 3.2011  | pkm      | Initial draft  |
| 0.20     | 10.2011 | pkm, cwo | typo corrections;<br>updated block diagrams, PCB layout recommendations, charger mode diagrams, application schematics, DCDC performance characteristics<br>added register 2bh and 2ch for chip version 2v1. |
| 1.0      | 10.2011 | pkm      | first official release   |
| 1.1      | 12.2011 | pkm      | corrected ntc_on bit description, adjusted max die temperature, updated dc dc mode description   |
| 1.2      | 5.2012  | pkm      | corrected "enter standby mode", GPIO1 input mode description, GPIO block diagram, GPIO IOSF, interrupt signal polarity<br>added switching charger graphs, added step-up external components, ASIC ID         |
|          |         |          |  |

**Note:** Typos may not be explicitly mentioned under revision history.

## 13 Ordering Information

The devices are available as the standard products shown below.

Table 35. Ordering Information

| Ordering Code  | Marking | Sequence                         | Description                              | Delivery Form        | Package               |
|----------------|---------|----------------------------------|--|----------------------|-----------------------|
| AS3711-BQFR-FF | M2V1-FF | sequence programmable on request | Quad Buck High Current PMIC with Charger | Tray                 | QFN56 7x7 0.4mm pitch |
| AS3711-BQFP-00 | M2V1-00 | default sequence                 | Quad Buck High Current PMIC with Charger | Tape & Reel dry pack | QFN56 7x7 0.4mm pitch |
| AS3711-BQFP-xx | M2V1-xx | customer specified               | Quad Buck High Current PMIC with Charger | Tape & Reel dry pack | QFN56 7x7 0.4mm pitch |

**Note:** All products are RoHS compliant and austriamicrosystems green.

Buy our products or get free samples online at ICdirect: <http://www.austriamicrosystems.com/ICdirect>

Technical Support is available at <http://www.austriamicrosystems.com/Technical-Support>

For further information and requests, please contact us [mailto: sales@austriamicrosystems.com](mailto:sales@austriamicrosystems.com) or find your local distributor at <http://www.austriamicrosystems.com/distributor>

## Copyrights

Copyright © 1997-2012, austriamicrosystems AG, Tobelbaderstrasse 30, 8141 Unterpremstaetten, Austria-Europe. Trademarks Registered ®. All rights reserved. The material herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner.

All products and companies mentioned are trademarks or registered trademarks of their respective companies.

## Disclaimer

Devices sold by austriamicrosystems AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application. For shipments of less than 100 parts the manufacturing flow might show deviations from the standard production flow, such as test flow or test location.

The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.



## Contact Information

### Headquarters

austriamicrosystems AG  
Tobelbaderstrasse 30  
A-8141 Unterpremstaetten, Austria

Tel: +43 (0) 3136 500 0  
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

<http://www.austriamicrosystems.com/contact>