AT24C64B

I²C-Compatible (2-Wire) Serial EEPROM
64K (8192 x 8)

DATASHEET

Features

- Low-voltage and Standard-voltage Operation
  - 2.7V (V_{CC} = 2.7V to 5.5V)
  - 1.8V (V_{CC} = 1.8V to 5.5V)
- Low-power Devices (I_{SB} = 6µA at 5.5V) Available
- Internally Organized 8192 x 8
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bi-directional Data Transfer Protocol
- 400kHz Clock Rate
- Write Protect Pin for Hardware Data Protection
- 32-byte Page Write Mode (Partial Page Writes Allowed)
- Self-Timed Write Cycle (5ms max)
- High Reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- Lead-free/Halogen-free Devices Available
- 8-lead JEDEC SOIC and TSSOP Packages
- Die Sales: Wafer Form, Waffle Pack, and Bumped Wafers

Description

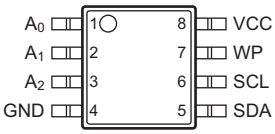
The Atmel® AT24C64B provides 65,536 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 8,192 words of 8 bits each. The device's cascadable feature allows up to eight devices to share a common 2-Wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT24C64B is available in space saving 8-lead JEDEC SOIC and 8-lead TSSOP packages and is accessed via a 2-Wire serial interface. In addition, the entire family is available in 2.7V (2.7 to 5.5V) and 1.8V (1.8 to 5.5V) versions.

1. Pin Configurations

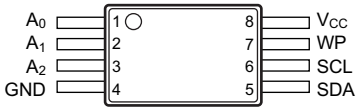
Table 1-1. Pin Configurations

Pin Name	Function
$A_0 – A_2$	Address Inputs
GND	Ground
SCL	Serial Clock Input
SDA	Serial Data
WP	Write Protect
V_{CC}	Power Supply

8-lead SOIC
(Top View)



8-lead TSSOP
(Top View)

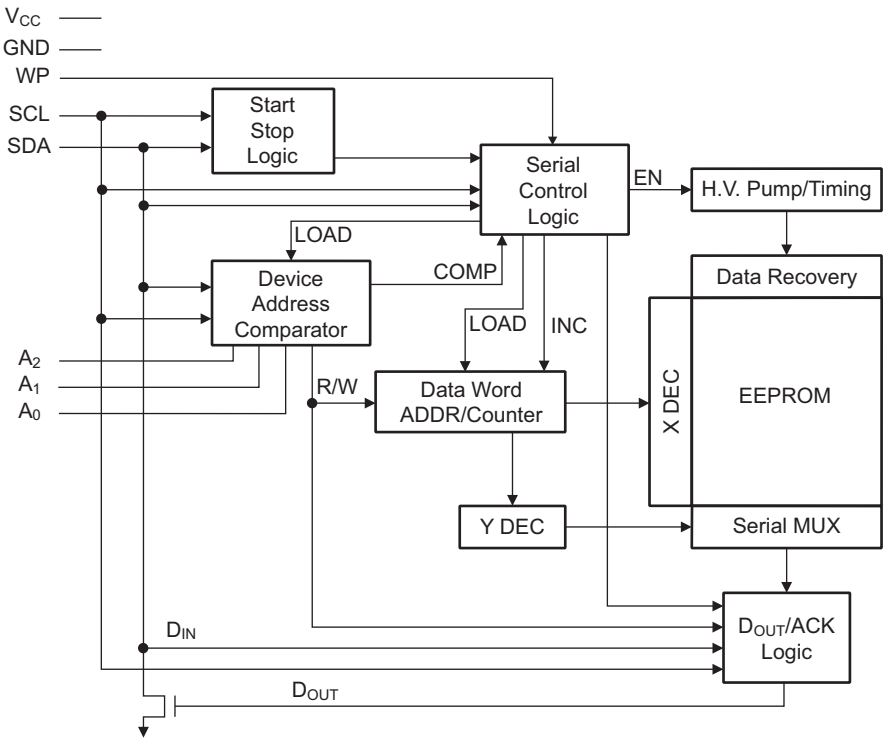


2. Absolute Maximum Ratings*

Operating Temperature	-55 to +125°C
Storage Temperature	-65 to +150°C
Voltage on Any Pin with Respect to Ground	-1V to +7V
Maximum Operating Voltage	6.25V
DC Output Current	5mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Block Diagram



4. Pin Description

Serial Clock (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

Device Addresses (A2, A1, A0): The A_2, A_1, and A_0 pins are Device Address inputs which are hardwired or left not connected for hardware compatibility with other AT24Cxxxx devices. When the pins are hardwired, as many as eight 64Kb devices may be addressed on a single bus system (see Section 7., “Device Addressing”). If the pins are left floating, the A_2, A_1, and A_0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3pF. If coupling is >3pF, Atmel recommends connecting the address pins to GND.

Write Protect (WP): The Write Protect input, when connected to GND, allows normal Write operations. When WP is connected high to V_{CC}, all Write operations to the upper quandrant (16Kb) of memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3pF. If coupling is >3pF, Atmel recommends connecting the pin to GND.

5. Memory Organization

AT24C64B, 64K Serial EEPROM: The 64K is internally organized as 256 pages of 32 bytes each. Random word addressing requires a 13 bit data word address.

5.1 Pin Capacitance [1]

Applicable over recommended operating range from T_A = 25°C, f = 1MHz, V_{CC} = +5.0V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

5.2 DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40 to +85°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V	Read at 400kHz		0.4	1.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V	Write at 400kHz		2.0	3.0	mA
I_{SB1}	Standby Current (1.8V Option)	V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}			1.0	µA
I_{SB2}	Standby Current (2.7V Option)	V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}			2.0	µA
I_{SB3}	Standby Current (5.0V Option)	V_{CC} = 4.5 - 5.5V	V_{IN} = V_{CC} or V_{SS}			6.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}			0.05	3.0	µA
V_{IL}	Input Low Level[1]			-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level	V_{CC} = 3.0V	I_{OL} = 2.10mA			0.4	V
V_{OL1}	Output Low Level	V_{CC} = 1.8V	I_{OL} = 0.15mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

5.3 AC Characteristics

Applicable over recommended operating range from T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100pF (unless otherwise noted). Test conditions are listed in Note 2.

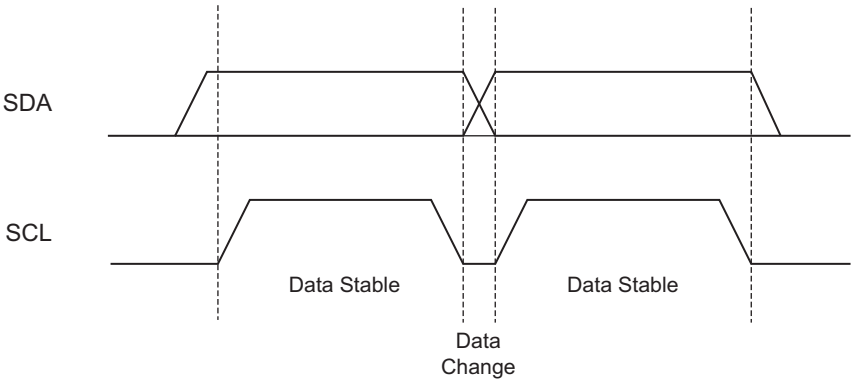
Symbol	Parameter	1.8V to 3.6V		5V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		400	kHz
t_{LOW}	Clock Pulse Width Low	1.3		1.2		µs
t_{HIGH}	Clock Pulse Width High	0.6		0.6		µs
t_I	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.2	0.9	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1.3		1.2		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.6		µs
$t_{SU.STA}$	Start Set-up Time	0.6		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		100		ns
t_R	Inputs Rise Time(1)		0.3		0.3	µs
t_F	Inputs Fall Time(1)		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		0.6		µs
t_{DH}	Data Out Hold Time	200		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance(1)	25°C, Page Mode, 5.0V	1,000,000				Write Cycles

Notes:
1. This parameter is characterized and is not 100% tested (T_A = 25°C).
2. AC measurement conditions:
   - R_L (connects to V_{CC}): 1.3kΩ (2.5V, 5.5V), 10kΩ (1.7V)
   - Input pulse voltages: 0.3V_{CC} to 0.7V_{CC}
   - Input rise and fall times: ≤50ns
   - Input and output timing reference voltages: 0.5 x V_{CC}

6. Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

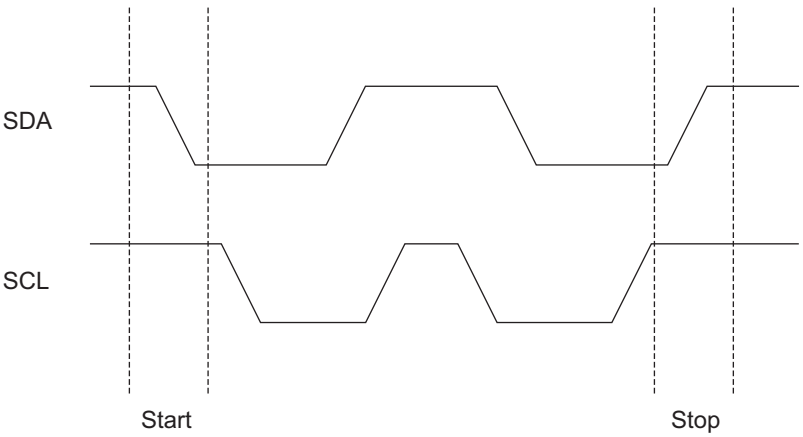
Figure 6-1. Data Validity



Start Condition: A high-to-low transition of SDA with SCL high is a Start condition which must precede any other command.

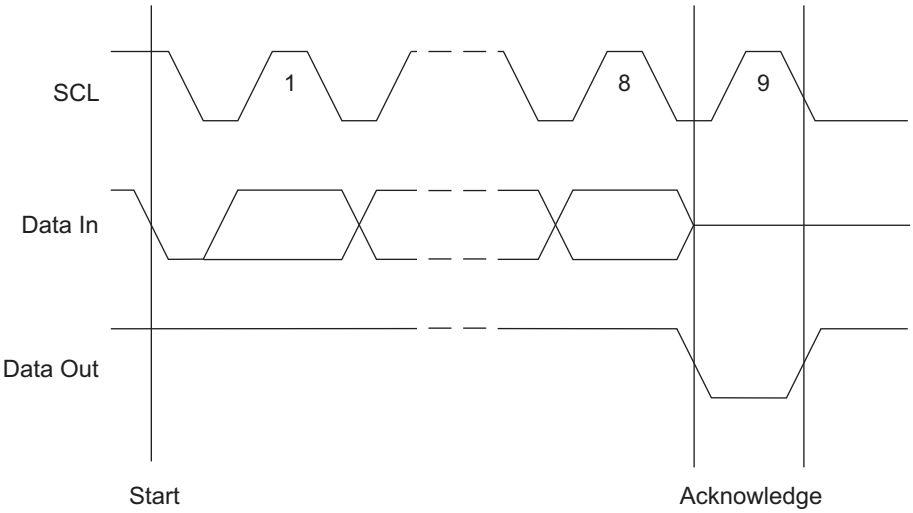
Stop Condition: A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the Stop command will place the EEPROM in a standby power mode.

Figure 6-2. Start and Stop Definition



Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

Figure 6-3. Output Acknowledge



Standby Mode: The AT24C64B features a low-power standby mode which is enabled:

- Upon power-up,
- After the receipt of the Stop bit, and
- Completion of any internal operations.

Memory Reset: After an interruption in protocol, power loss or system reset, any 2-Wire part can be reset by following these steps:

1. Clock up to nine cycles,
2. Look for SDA high in each cycle while SCL is high,
3. Create a Start condition as SDA is high.

The device is ready for the next communication after the above steps have been completed.

Figure 6-4. Software Reset

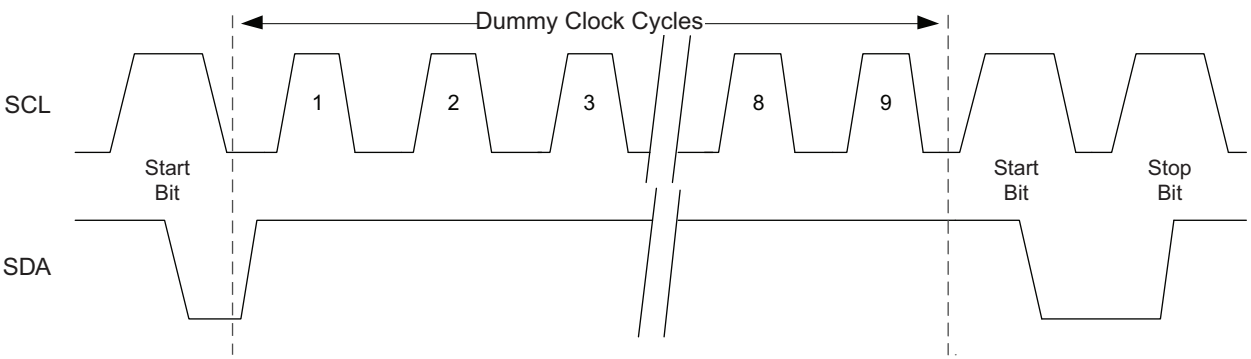


Figure 6-5. Bus Timing — SCL: Serial Clock, SDA: Serial Data I/O

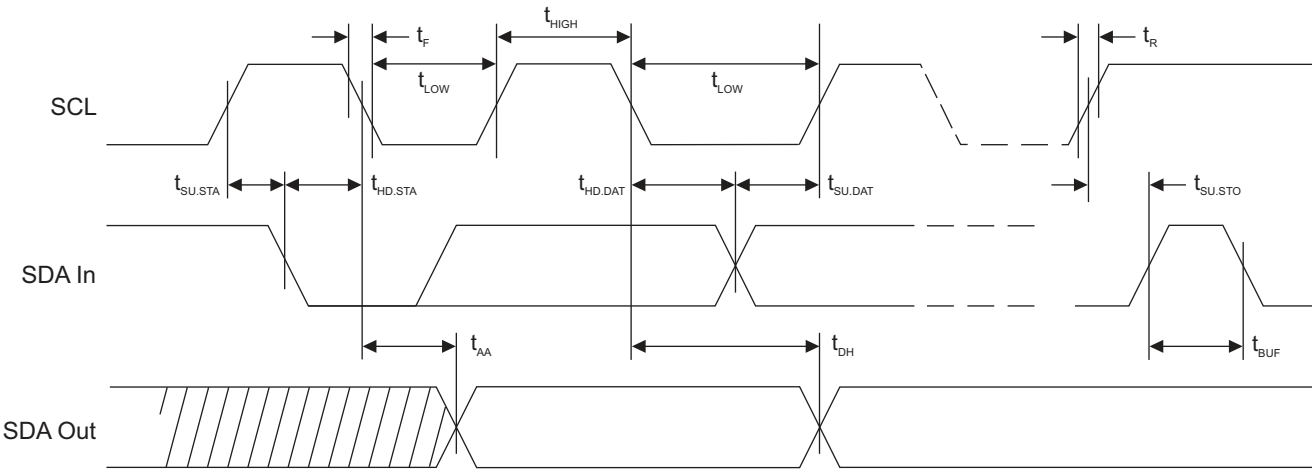
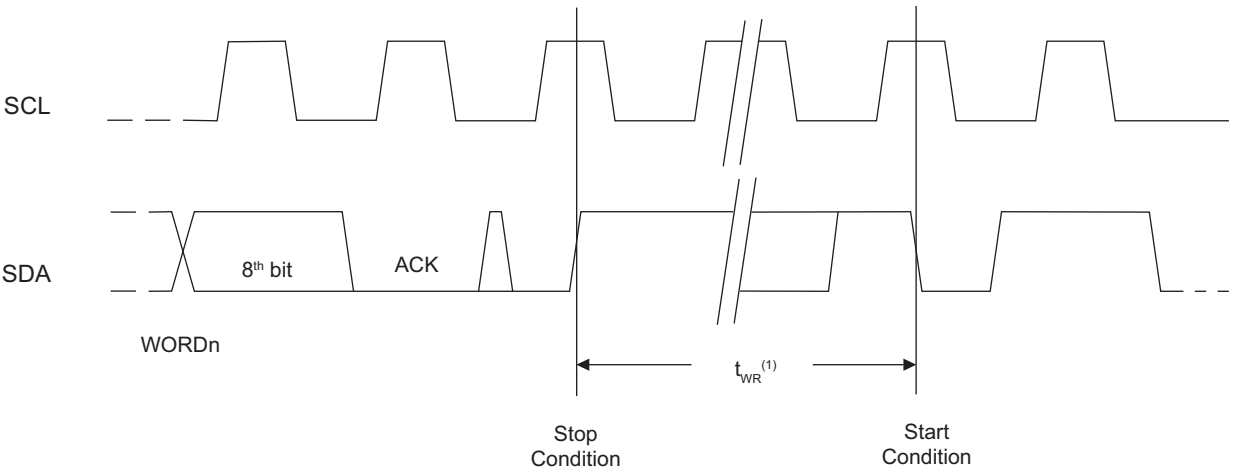


Figure 6-6. Write Cycle Timing — SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid Stop condition of a Write Sequence to the end of the internal clear/write cycle.

7. Device Addressing

The 64Kb EEPROM requires an 8-bit device address word following a Start condition to enable the device for a Read or Write operation. The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown below. This is common to all 2-Wire EEPROM devices.

Figure 7-1. Device Address

1	0	1	0	A2	A1	A0	R/W

MSB LSB

The 64Kb uses the three Device Address bits A2, A1, and A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A_2, A_1, and A_0 pins use an internal proprietary circuit that biases them to a Logic Low condition if the pins are allowed to float.

The eighth bit of the Device Address is the Read/Write operation select bit. A Read operation is initiated if this bit is high, and a Write operation is initiated if this bit is low.

Upon a compare of the Device Address, the EEPROM will output a zero. If a compare is not made, the device will return to standby state.

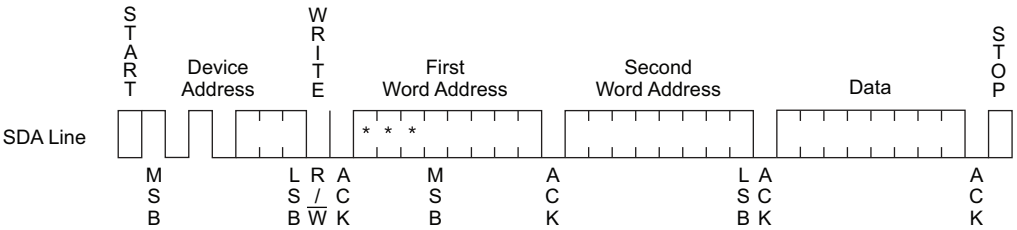
Noise Protection: Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device. A low-V_{CC} detector resets the device to prevent data corruption in a noisy environment.

Data Security: The AT24C64B has a hardware data protection scheme which allows the user to write protect the upper quadrant (16Kb) of memory when the WP pin is at V_{CC}.

8. Write Operations

Byte Write: A Write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, i.e. microcontroller, must terminate the write sequence with a Stop condition. At this time, the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete.

Figure 8-1. Byte Write

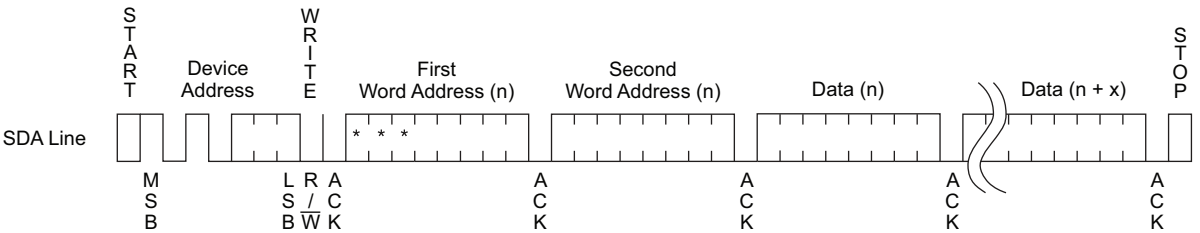


Note: * = Don't Care bits

Page Write: The 64K EEPROM is capable of 32-byte Page Writes.

A Page Write is initiated the same way as a Byte Write, but the microcontroller does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the Page Write sequence with a Stop condition.

Figure 8-2. Page Write



Note: * = Don't Care bits

The data word address' lower five bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will roll-over and the previous data will be overwritten.

Acknowledge Polling: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, Acknowledge Polling can be initiated. This involves sending a Start condition followed by the device address word. The Read/Write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the Read or Write Sequence to continue.

9. Read Operations

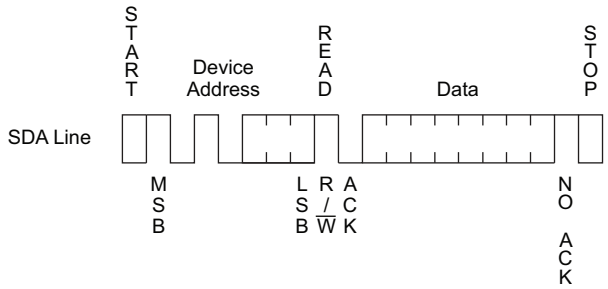
Read operations are initiated the same way as Write operations with the exception the Read/Write Select bit in the device address word is set to one. There are three read operations:

- Current Address Read
- Random Address Read
- Sequential Read

Current Address Read: The internal data word address counter maintains the last address accessed during the last Read or Write operation, incremented by one. This address stays valid between operations as long as the device power is maintained. The address roll-over during Read is from the last byte of the last memory page to the first byte of the first page. The address roll-over during Write is from the last byte of the current page to the first byte of the same page.

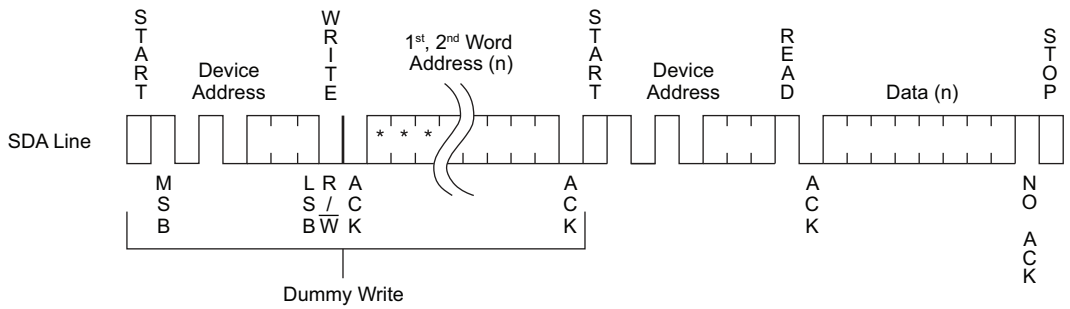
Once the Device Address with the Read/Write Select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following Stop condition.

Figure 9-1. Current Address Read



Random Read: A Random Read requires a dummy Byte Write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another Start condition. The microcontroller now initiates a Current Address Read by sending a Device Address with the Read/Write Select bit high. The EEPROM acknowledges the Device Address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following Stop condition.

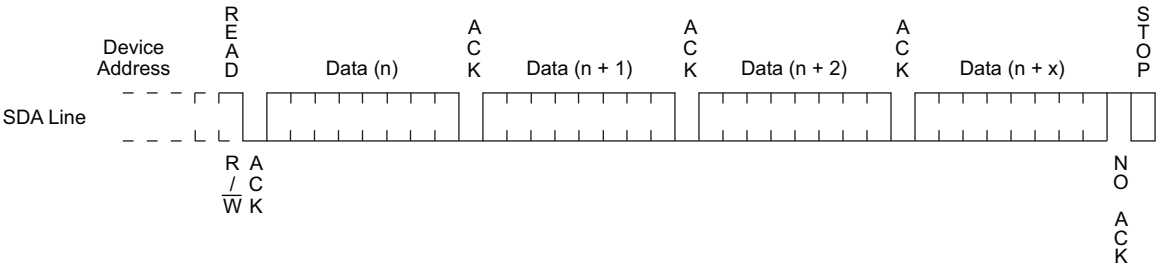
Figure 9-2. Random Read



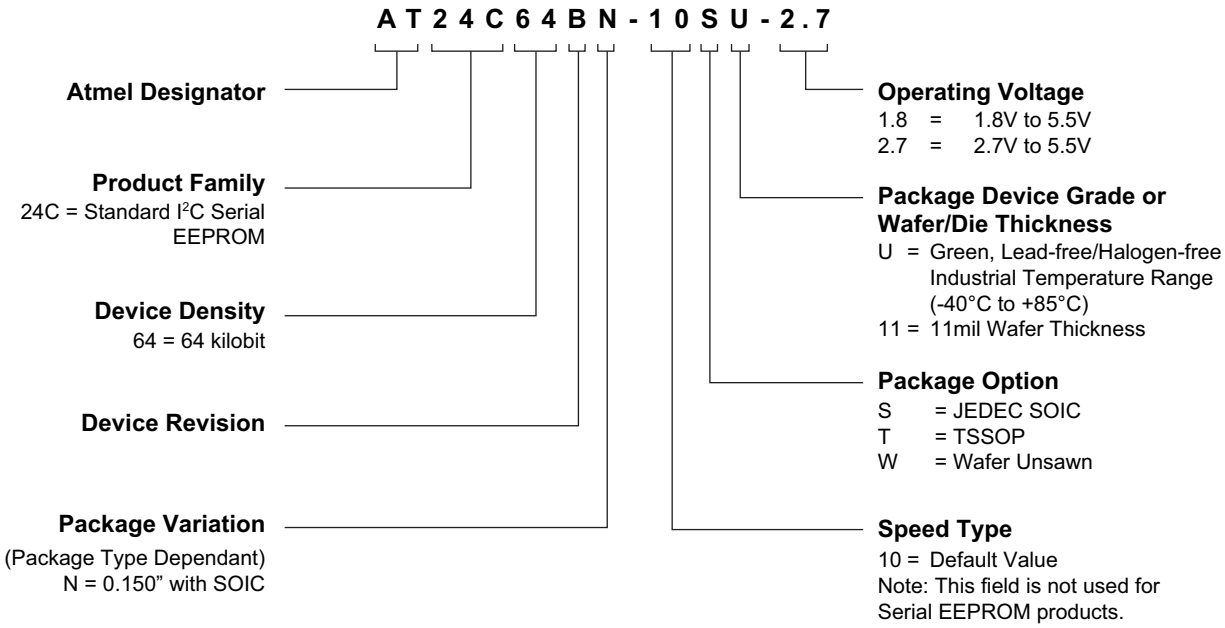
Note: 1. * = Don't Care bits

Sequential Read: Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a zero but does generate a following Stop condition.

Figure 9-3. Sequential Read

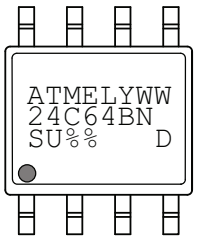
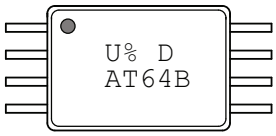


10. Ordering Code Detail



11. Part Markings

AT24C64B: Package Marking Information

8-lead SOIC(3)	8-lead TSSOP(4)
	

Note 1: ● designates pin 1
Note 2: Package drawings are not to scale
Note 3: Back side marking will include Assembly Location and lot Number
Note 4: Back side marking will include Date Code, Assembly Location and Lot Number

Date Codes				**Voltages**
Y = Year		M = Month	WW = Work Week of Assembly	%% = Minimum Voltage
9: 2009	3: 2013	A: January	02: Week 2	18 or 1: 1.8V min
0: 2010	4: 2014	B: February	04: Week 4	27 or 3: 2.7V min
1: 2011	5: 2015	...	...	
2: 2012	6: 2016	L: December	52: Week 52	

Country of Assembly	**Lot Number**	**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number	U: Industrial/Matte Tin/SnAguCu

Trace Code	**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ	AT: Atmel ATM: Atmel ATML: Atmel

1/31/14

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	**TITLE** **24C64BSM**, AT24C64B Package Marking Information	**DRAWING NO.** 24C64BSM	**REV.** A

12. Ordering Information

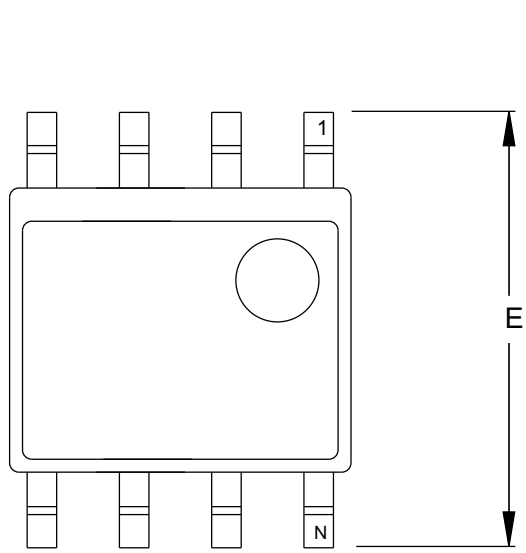
Ordering Code	Lead Finish	Package	Voltage	Operation Range
AT24C64BN-10SU-2.7(2)	Lead-free/Halogen-free	8S1	1.8V to 5.5V	Industrial Temperature (-40°C to 85°C)
AT24C64BN-10SU-1.8(2)				
AT24C64B-10TU-2.7(2)		8X		
AT24C64B-10TU-1.8(2)				
AT24C64B-W1.8-11(3)	—	Die Sale		

Notes:
1. For 2.7V devices used in the 4.5V to 5.5V range, see Section 5.2, “DC Characteristics” and Section 5.3, “AC Characteristics”.
2. U = Green Package and RoHS compliant.
3. Available in waffle pack and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Marketing.

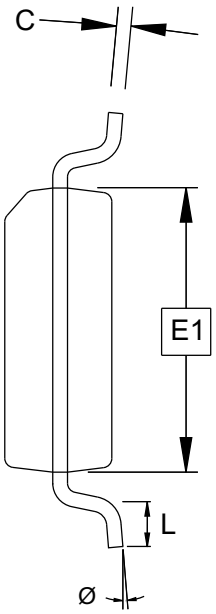
Package Type	
8S1	8-lead 0.150” wide body, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead 4.4mm body, Plastic Thin Shrink Small Outline Package (TSSOP)

13. Packaging Information

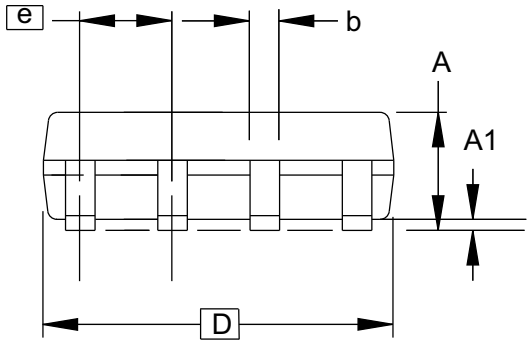
13.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

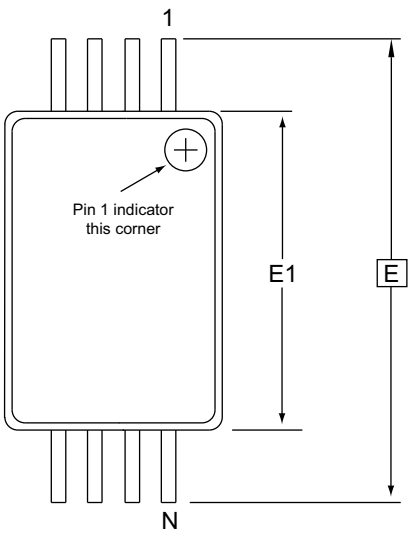
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

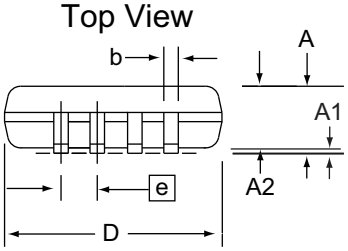
6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** G

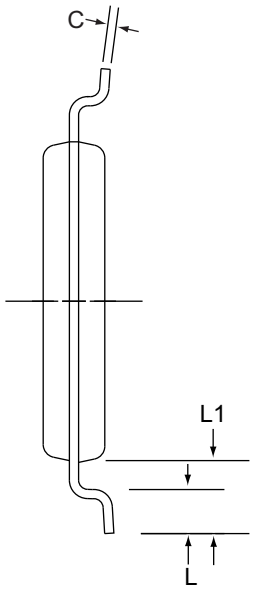
13.2 8X — 8-lead TSSOP



Top View



Side View



End View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	0.25	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

2/27/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	**GPC** TNR	**DRAWING NO.** 8X	**REV.** E

14. Revision History

Doc. Rev.	Date	Comments
3350F	05/2014	Add ordering code detail and part markings. Update the 8X package drawing, template, logos, and disclaimer page. (No change in functional specification.)
3350E	09/2007	Update template; implemented revision history.

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