Features

- High-performance Fully CMOS, Electrically-erasable Complex Programmable Logic Device
  - 64 Macrocells
  - 5.0 ns Pin-to-pin Propagation Delay
  - Registered Operation up to 333 MHz
  - Enhanced Routing Resources
  - Optimized for 1.8V Operation
  - 2 I/O Banks to Facilitate Multi-voltage I/O Operation: 1.5V, 1.8V, 2.5V, 3.3V
  - SSTL2 and SSTL3 I/O Standards
- In-System Programming (ISP) Supported
  - ISP Using IEEE 1532 (JTAG) Interface
  - IEEE 1149.1 JTAG Boundary Scan Test
- Flexible Logic Macrocell
  - D/T/Latch Configurable Flip-flops
  - 5 Product Terms per Macrocell, Expandable up to 40
  - Global and Individual Register Control Signals
  - Global and Individual Output Enable
  - Programmable Output Slew Rate with Low Output Drive
  - Programmable Open Collector Output Option
  - Maximum Logic Utilization by Burying a Register with a Combinatorial Output and Vice Versa
- Fully Green (RoHS Compliant)
- 10 µA Standby Current
- Power Saving Option During Operation Using PD1 and PD2 Pins
- Programmable Pin-keeper Option on Inputs and I/Os
- Programmable Schmitt Trigger Option on Input and I/O Pins
- Programmable Input and I/O Pull-up Option
- Unused I/O Pins Can Be Configured as Ground (Optional)
- Available in Commercial and Industrial Temperature Ranges
- Available in 44-lead and 100-lead TQFP
- Advanced Digital CMOS Technology
  - 100% Tested
  - Completely Reprogrammable
  - 10,000 Program/Erase Cycles
  - 20-year Data Retention
  - 2000V ESD Protection
  - 200 mA Latch-up Immunity
- Security Fuse Feature
- Hot-Socketing Supported

High-performance CPLD

ATF1504BE

3637B–PLD–1/08

Enhanced Features

- **Improved Connectivity (Additional Feedback Routing, Alternate Input Routing)**
- **Output Enable Product Terms**
- **Outputs Can Be Configured for High or Low Drive**
- **Combinatorial Output with Registered Feedback and Vice Versa within each Macrocell**
- **Three Global Clock Pins**
- **Fast Registered Input from Product Term**
- **Pull-up Option on TMS and TDI JTAG Pins**
- **OTF (On-the-Fly) Reconfiguration Mode**
- **DRA (Direct Reconfiguration Access)**

1. Description

The ATF1504BE is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable memory technology. With 64 logic macrocells and up to 68 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1504BE's enhanced routing switch matrices increase usable gate count and the odds of successful pin-locked design modifications.

The ATF1504BE has up to 64 bi-directional I/O pins and four dedicated input pins. Each dedicated input pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell. Figures 1-1 and 1-2 show the pin assignments for the 100-lead and 44-lead TQFP packages respectively.

Figure 1-1. 100-lead TQFP Top View

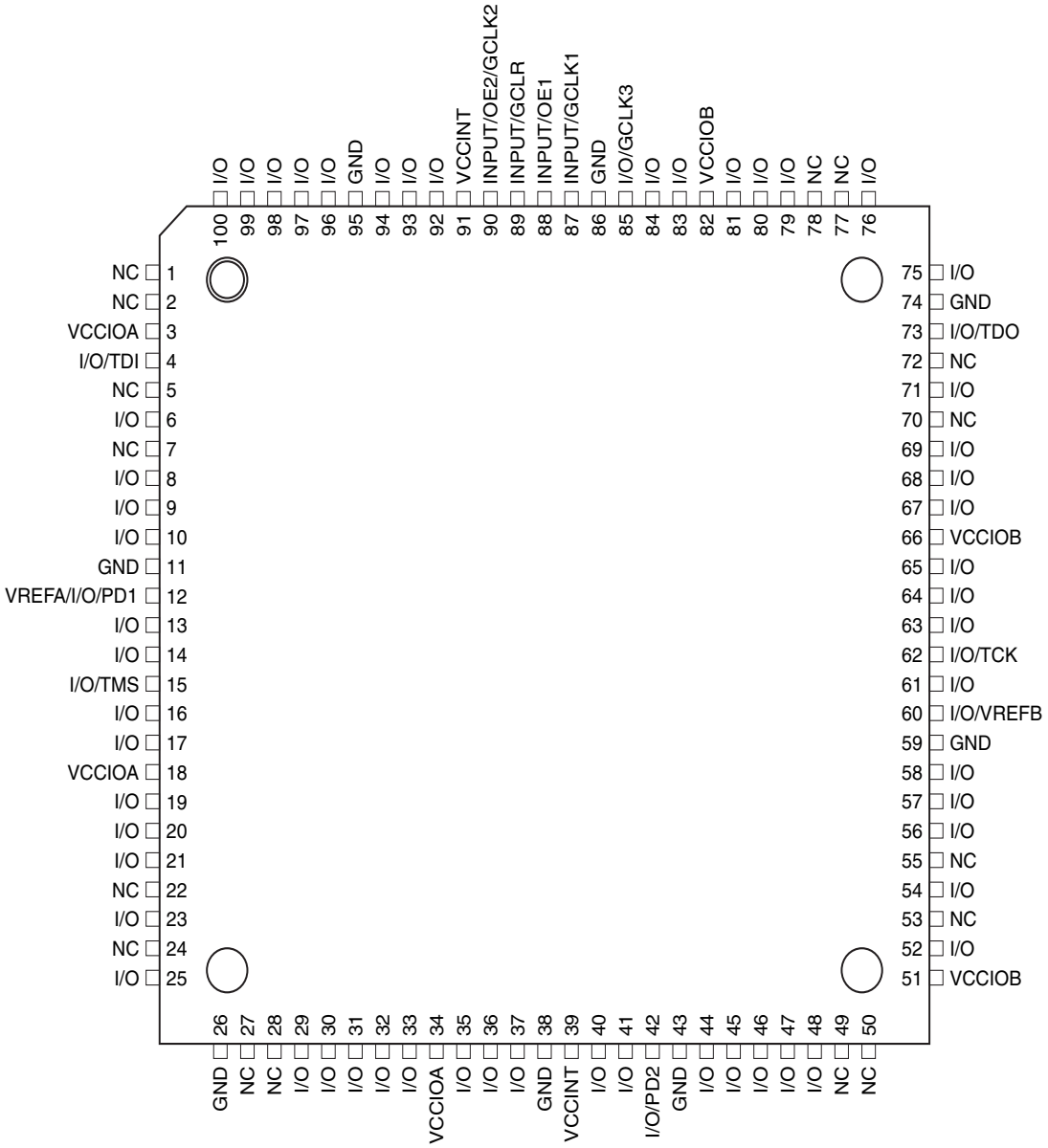


Figure 1-2. 44-lead TQFP Top View

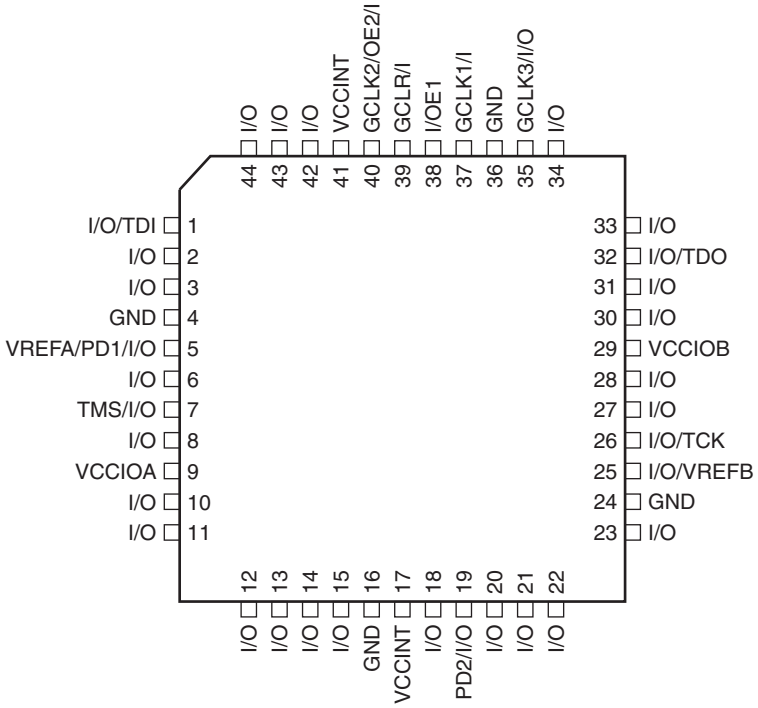
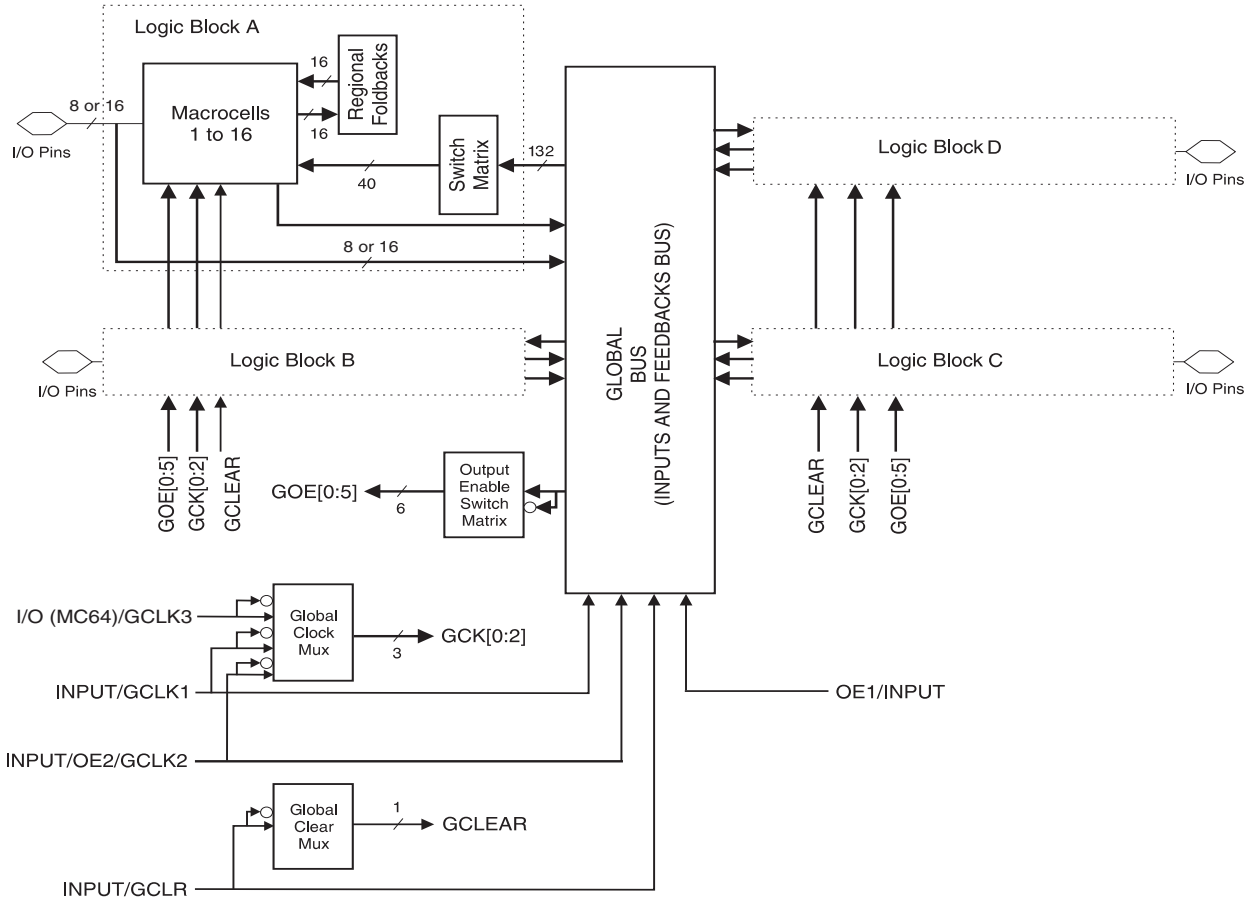


Figure 1-3. Block Diagram



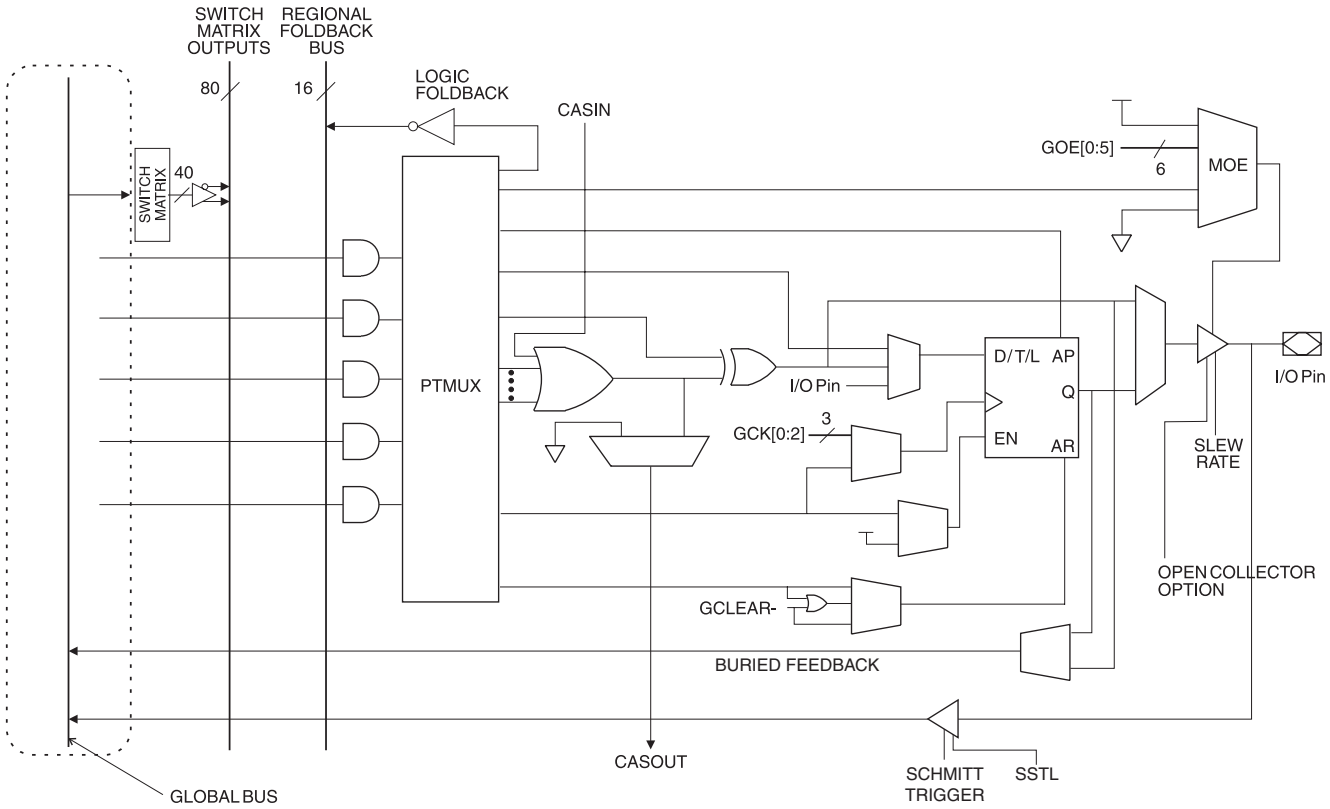
Each of the 64 macrocells generates a buried feedback signal that goes to the global bus (see Figure 1-3). Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1504BE allows fast, efficient generation of complex logic functions. The ATF1504BE contains eight such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1504BE macrocell, shown in Figure 1-4, is highly flexible and capable of supporting complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer, OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

A security fuse, when programmed, protects the contents of the ATF1504BE. Two bytes (16 bits) of User Electronic Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Electronic Signature is accessible regardless of the state of the security fuse.

The ATF1504BE device supports In-System Programming (ISP) via the industry-standard 4-pin JTAG interface (IEEE 1532 standard), and is fully compliant with IEEE 1149.1 for Boundary Scan Test. ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

Figure 1-4. ATF1504BE Macrocell



1.1 Product Terms and Select Mux

Each ATF1504BE macrocell has five product terms. Each product term receives as its inputs all signals from the switch matrix and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX configuration is determined by the design compiler, which selects the optimum macrocell configuration.

1.2 OR/XOR/CASCADE Logic

The ATF1504BE's logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with minimal additional delay.

The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high or low level. For combinatorial outputs, the fixed level input allows polarity selection. For registered functions, the fixed levels allow DeMorgan minimization of product terms.

1.3 Flip-flop

The ATF1504BE's flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK and SR operation, the flip-flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can be any one of the Global CLK signals (GCK[0 : 2]) or an individual product term. The flip-flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

1.4 Extra Feedback

The ATF1504BE macrocell output can be selected as registered or combinatorial. The extra buried feedback signal can be either combinatorial or a registered signal regardless of whether the output is combinatorial or registered. (This enhancement function is automatically implemented by the fitter software.) Feedback of a buried combinatorial output allows the creation of a second latch within a macrocell.

1.5 I/O Control

The output enable multiplexer (MOE) controls the output enable signal. Each I/O can be individually configured as an input, output or bi-directional pin. The output enable for each macrocell can be selected from the true or complement of the two output enable pins, a subset of the I/O pins, or a subset of the I/O macrocells. This selection is automatically done by the fitter software when the I/O is configured as an input or bi-directional pin.

1.6 Global Bus/Switch Matrix

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 64 macrocells. The switch matrix in each logic block receives as its inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.

1.7 Foldback Bus

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to all 16 macrocells within the logic block. The foldback is an inverse polarity of one of the macrocell's product terms. The 16 foldback terms in each logic block allow generation of high fan-in sum terms or other complex logic functions with little additional delay.

2. Input and I/O Pins

2.1 Programmable Pin-keeper Option for Inputs and I/Os

The ATF1504BE offers the option of individually programming each of its input or I/O pin so that pin-keeper circuit can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level. This circuitry prevents undriven input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Figure 2-1 shows the pin-keeper circuit for an Input Pin and Figure 2-2 shows the same for an I/O pin. The pin-keeper circuit is a weak feedback latch and has an effective resistance that is approximately 50 kΩ

Figure 2-1. Input with Programmable Pin-keeper

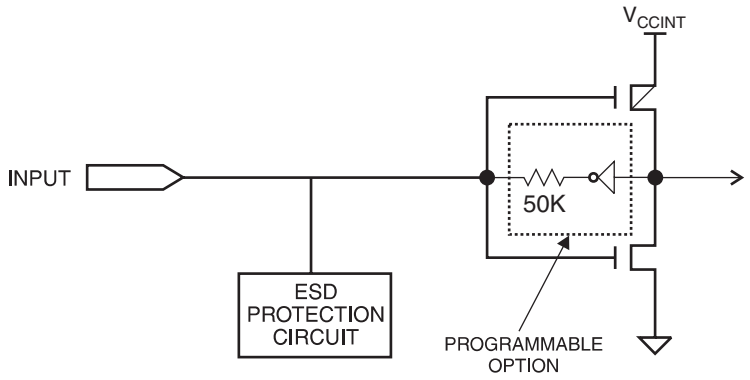
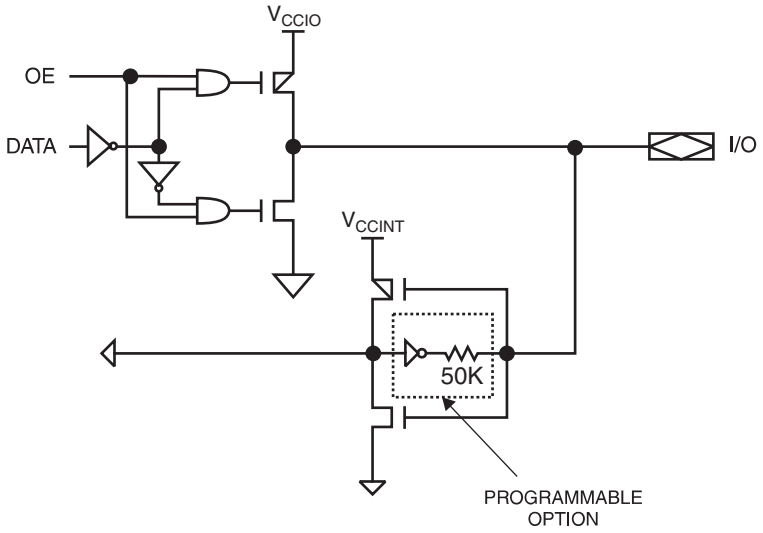


Figure 2-2. I/O with Programmable Pin-keeper



2.2 Schmitt Trigger

The Input Buffer of each input and I/O pin has an optional schmitt trigger setting. The schmitt trigger option can be used to buffer inputs with slow rise times.

2.3 Output Drive Capability

Each output has a high/low drive option. The low drive option (slow slew rate) can be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed or drive strength. Outputs default to high drive strength by Atmel software and can be set to low drive strength through the slew rate option.

2.4 I/O Bank

The I/O pins of the ATF1504BE are grouped into two banks, Bank A and Bank B. Bank A comprises of I/O pins for macrocells 1 to 32 (Logic Block A and B), and it is powered by V_{CCIOA}. Bank B comprises of I/O pins for macrocells 33 to 64 (Logic Block C and D), and it is powered by V_{CCIOB}.

2.5 I/O Standard

The ATF1504BE supports a wide range of I/O standards which include LVTTL, LVCMOS33, LVCMOS25, LVCMOS18 and LVCMOS15. The I/O pins of the ATF1504BE can also be individually configured to support SSTL-2 (Class I) and SSTL-3 (Class I) advanced I/O standards.

This and the two I/O banks, together, allow the ATF1504BE to be used for voltage level translation.

3. Power Management

Unlike conventional CPLDs with sense amplifiers, the ATF1504BE is designed using low-power full CMOS design techniques. This enables the ATF1504BE to achieve extremely low power consumption over the full operating frequency spectrum.

The ATF1504BE also has an optional power-down mode. In this mode, current drops to below 100 µA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. When enabled, the device goes into power-down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins.

4. Security Feature

A fuse is provided to prevent unauthorized copying of the ATF1504BE fuse patterns. Once enabled, fuse reading or verification is inhibited. However, the 16-bit User Electronic Signature remains accessible. To reset this feature, the entire memory array in the device must be erased.

5. Programming Methods

The ATF1504BE devices are In-System Programmable (ISP) or In-System Configurable (ISC) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

When using the ISP hardware or software to program the ATF1504BE devices, four I/O pins must be reserved for the JTAG interface. However, the logic features that the macrocells have associated with these I/O pins are still available to the design for buried logic functions.

To facilitate ISP programming by the Automated Test Equipment (ATE) vendors, Serial Vector Format (SVF) files can be created by Atmel-provided software utilities. ATF1504BE devices can also be programmed using standard third-party programmers. With a third-party programmer, the JTAG ISP port can be disabled, thereby allowing four additional I/O pins to be used for logic.

The AT1504BE device supports several configuration modes which gives designers several unique options for programming.

The different modes of programming are:

- ISC – In-System Configuration
- OTF – On-the-Fly Reconfiguration
- DRA – Direct Reconfiguration Access

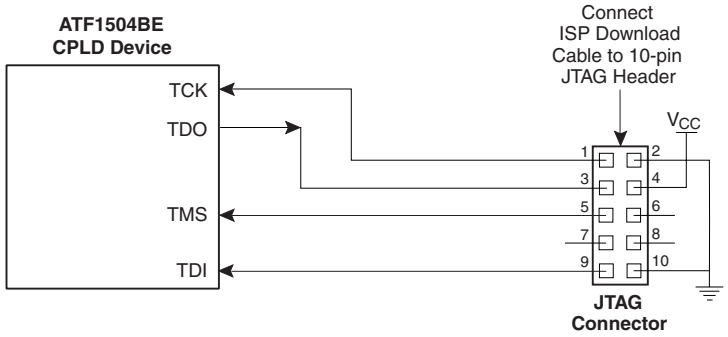
5.1 In-System Configuration – ISC (Also Referred to as ISP)

This mode is the de-facto standard used to program the CPLD when it is attached to a PCB. The term ISC can also be used interchangeably with ISP (In-system Programming). ISC or ISP eliminates the need for an external device programmer, and the devices can be soldered to a PCB without being preprogrammed.

In the ISC mode, the logic operation of the ATF1504BE is halted and the embedded configuration memory is programmed. The device is programmed by first erasing the configuration memory in the CPLD and then loading the new configuration data into the memory, which in-turn configures the PLD for functional mode. When the device is in the ISC programming mode, all user I/Os are held in the high impedance state.

The ISC mode is best suited for working with the ATF1504BE device in a design development or production environment. Configuration of the ATF1504BE device done via a Download Cable (see Figure 5-1 on page 11) is the default mode used to program the device in the ISC mode. In this mode, the PC is typically the controlling device that communicates with the CPLD.

Figure 5-1. Configuration of ATF1504BE Device Using a Download Cable



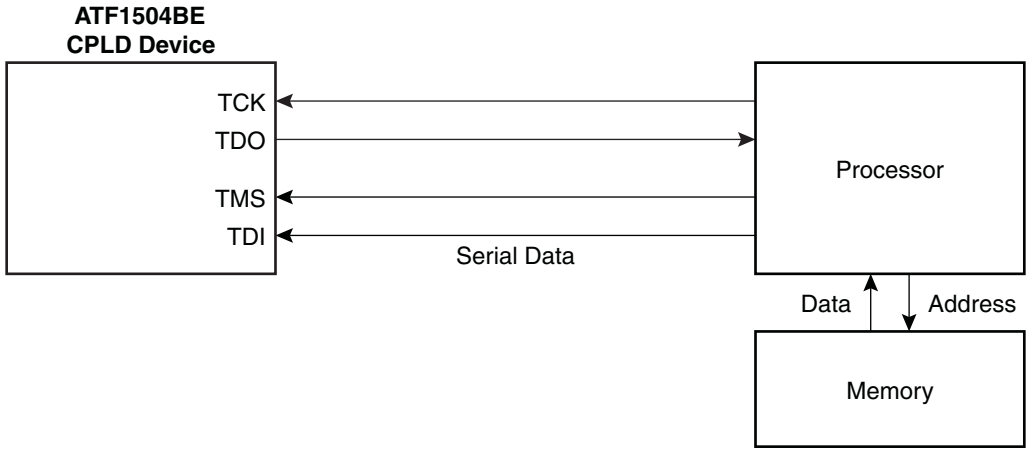
5.2 On-the-Fly Reconfiguration – OTF

In this mode, the CPLD design pattern stored in the internal configuration memory can be modified while the previously-programmed design pattern is operating with minimal disturbance to the programming operation of the new design. The new configuration will take affect after the OTF programming process is completed and the OTF mode is exited.

The configuration data for any design is stored in the internal configuration memory. Once the configuration data is transferred to the internal static registers of the CPLD, the CPLD operates with the design pattern and the configuration memory is free to be re-loaded with a new set of configuration data. The design pattern due to the new configuration content is activated through an initialization cycle that occurs on exiting the OTF mode or after the next power up sequence.

Figure 5-2 shows the electrical interface for configuration of the ATF1504BE device in the OTF mode. The processor is the controlling device that communicates with the CPLD and uses configuration data stored in the external memory to configure the CPLD.

Figure 5-2. Configuration of ATF1504BE Device Using a Processor and Memory



5.3 Direct Reconfiguration Access – DRA

This reconfiguration mode allows the user to directly modify the internal static registers of the CPLD without affecting the configuration data stored in the embedded memory. It is more useful in cases where immediate and temporary context change in the function of the hardware is desired.

The embedded configuration memory in the ATF1504BE does not change when a new set of configuration data is passed to the ATF1504BE using the DRA mode. Instead, the internal static registers of the CPLD are directly written with the data entering the device via the JTAG port. In other words, it's a temporary change in the function performed by the CPLD since a power sequence results in the device being configured again by the data stored in the embedded memory.

5.4 ISP Programming Protection

The ATF1504BE has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The I/O pins default to high-Z state during such a condition.

All ATF1504BE devices are initially shipped in the erased state, thereby making them ready to use for ISP.

6. JTAG-BST/ISP Overview

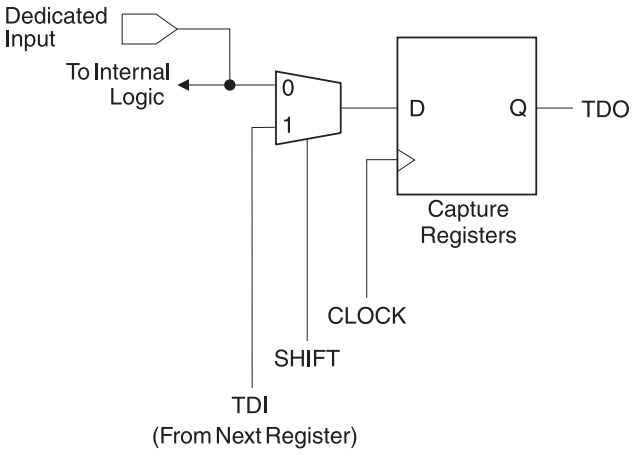
The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1504BE. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing methods. Each input pin and I/O pin has its own boundary-scan cell (BSC) to support boundary-scan testing. The TAP controller is automatically reset at power-up. The five JTAG modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE and HIGHZ. The ATF1504BE's BSC can be fully described using a BSDL file as described in IEEE 1149.1 standard. This allows ATF1504BE testing to be described and implemented using any one of the third-party development tools supporting this standard.

The ATF1504BE also has the option of using the four JTAG-standard I/O pins for ISP. The ATF1504BE is programmable through the four JTAG pins using the IEEE standard JTAG programming protocol established by IEEE 1532 standard using 1.8V/2.5V/3.3V LVCMOS level programming signals from the ISP interface for in-system programming. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

6.1 JTAG Boundary-scan Cell (BSC) Testing

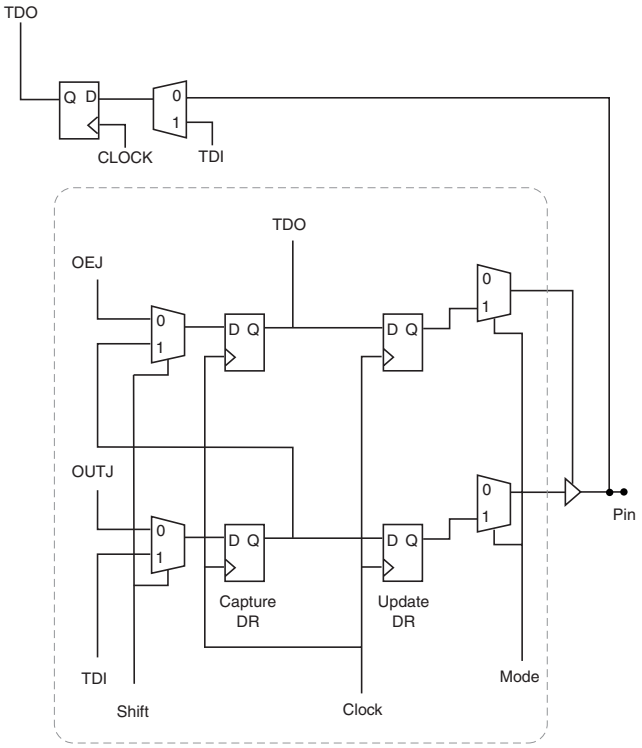
The ATF1504BE contains 64 I/O pins and four dedicated input pins. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing as described in detail by IEEE 1532 standard. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells is shown below.

Figure 6-1. BSC Configuration for Input and I/O Pins (Except JTAG TAP Pins)



Note: The ATF1504BE has a pull-up option on TMS and TDI pins. This feature is selected as a design option.

Figure 6-2. BSC Configuration for Macrocell



7. Design Software Support

ATF1504BE designs are supported by several third-party tools. Automated fitters allow logic synthesis using a variety of high-level description languages such as VHDL® and Verilog®. Third party synthesis and simulation tools from Mentor Graphics® are integrated into Atmel's software tools.

8. Electrical Specifications

Table 8-1. Absolute Maximum Ratings*

Operating Temperature	-40° C to +85° C
Storage Temperature	-65° C to +150° C
Supply Voltage (V_{CCINT})	-0.5V to +2.5V
Supply Voltage for Output Drivers (V_{CCIO})	-0.5V to +4.5V
Junction Temperature	-55° C to +155° C

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8-2. Operating Temperature Range

	Commercial	Industrial
Operating Temperature (Ambient)	0° C - 70° C	-40° C - 85° C

Table 8-3. Pin Capacitance[1]

	Typ	Max	Units	Conditions
C_{IN}	8	10	pF	V_{IN} = 0V; f = 1.0 MHz
$C_{I/O}$	8	10	pF	V_{OUT} = 0V; f = 1.0 MHz

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Table 8-4. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CCINT}	Supply Voltage for internal logic and input buffers		1.7	1.8	1.9	V
V_{CCIO}	Supply Voltage for output drivers at 3.3V		3.0	3.3	3.6	V
V_{CCIO}	Supply Voltage for output drivers at 2.5V		2.3	2.5	2.7	V
V_{CCIO}	Supply Voltage for output drivers at 1.8V		1.7	1.8	1.9	V
V_{CCIO}	Supply Voltage for Output Drivers at 1.5V		1.4	1.5	1.6	V
$I_{CC\_INT(HD)}$	Operating Current[1] for V_{CCINT} (supply voltage)	V_{CCINT} = 1.8V, V_{CCIO} = 3.3V, f = 1 MHz		150		µA
$I_{CC\_IO(HD)}$	Operating Current[1] for V_{CCIO} (supply voltage for output drivers), per LAB	V_{CCINT} = 1.8V, V_{CCIO} = 3.3V, f = 1 MHz		165		µA
$I_{CC\_INT(LD)}$	Operating Current[1] for V_{CCINT} (low drive)	V_{CCINT} = 1.8V, V_{CCIO} = 3.3V, f = 1 MHz		145		µA
$I_{CC\_IO(LD)}$	Operating Current[1] for V_{CCIO} (supply voltage for output drivers), per LAB	V_{CCINT} = 1.8V, V_{CCIO} = 3.3V, f = 1 MHz		60		µA
I_{SB}	Standby Current[1]	V_{CCINT} = 1.9V, V_{CCIO} = 3.6V		10		µA
I_{IL}, I_{IH}	Input Leakage	V_{CCINT} = 1.8V, V_{IN} = 0V or V_{CCINT}			±1	µA
I_{OZH}, I_{OH}	Output or IO Leakage	V_{CCINT} = 1.8V, V_{CCIO} = 3.6V, V_{IN} = 0V or V_{CCIO}			±1	µA
LVCMOS 3.3V & LVTTL (HD: High Drive, LD: Low Drive)						
V_{IL}	Input Low-voltage		-0.3		0.8	V
V_{IH}	Input High-voltage		2		3.9	V
V_{OL}	Output Low-voltage	HD: I_{OL} = 8 mA, V_{CCIO} = 3V			0.4	V
		LD: I_{OL} = 1 mA, V_{CCIO} = 3V			0.4	V
V_{OH}	Output High-voltage	HD: I_{OH} = -8 mA, V_{CCIO} = 3V	V_{CCIO} - 0.4			V
		LD: I_{OH} = -1 mA, V_{CCIO} = 3V	V_{CCIO} - 0.4			V
LVCMOS 2.5V						
V_{IL}	Input Low-voltage		-0.3		0.7	V
V_{IH}	Input High-voltage		1.7		3.9	V
V_{OL}	Output Low-voltage	HD: I_{OL} = 8 mA, V_{CCIO} = 2.3V			0.4	V
		LD: I_{OL} = 1 mA, V_{CCIO} = 2.3V			0.4	V
V_{OH}	Output High-voltage	HD: I_{OH} = -8 mA, V_{CCIO} = 2.3V	V_{CCIO} - 0.4			V
		LD: I_{OH} = -1 mA, V_{CCIO} = 2.3V	V_{CCIO} - 0.4			V
LVCMOS 1.8V						
V_{IL}	Input Low-voltage		-0.3		0.35 x V_{CCIO}	V

Table 8-4. DC Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High-voltage		1.2		3.9	V
V_{OL}	Output Low-voltage	HD: I_{OL} = 2 mA, V_{CCIO} = 1.7V			0.45	V
		LD: I_{OL} = 1 mA, V_{CCIO} = 1.7V			0.2	V
V_{OH}	Output High-voltage	HD: I_{OH} = -2 mA, V_{CCIO} = 1.7V	V_{CCIO} - 0.45			V
		LD: I_{OH} = -1 mA, V_{CCIO} = 1.7V	V_{CCIO} - 0.45			V
LVCMOS 1.5V						
V_{IL}	Input Low-voltage		-0.3		0.35 x V_{CCIO}	V
V_{IH}	Input High-voltage		1.2		3.9	V
V_{OL}	Output Low-voltage	HD: I_{OL} = 2 mA, V_{CCIO} = 1.4V			0.45	V
		LD: I_{OL} = 1 mA, V_{CCIO} = 1.4V			0.2	V
V_{OH}	Output High-voltage	HD: I_{OH} = -2 mA, V_{CCIO} = 1.4V	V_{CCIO} - 0.45			V
		LD: I_{OH} = -1 mA, V_{CCIO} = 1.4V	V_{CCIO} - 0.45			V

Note: 1. 16-bit up/down counter used in each LAB.

Table 8-5. Schmitt Trigger Input Threshold Voltage

	V_{THL}		V_{TLH}	
V_{CCINT}	Min	Max	Min	Max
1.70	0.68	0.73	1.05	1.08
1.95	0.81	0.88	1.18	1.22

Table 8-6. SSTL2-1 DC Voltage Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CCIO}	Input Source Voltage		2.3	2.5	2.7	V
V_{REF} (1)	Input Reference Voltage		1.15	1.25	1.35	V
V_{TT} (2)	Termination Voltage		V_{REF} - 0.05	1.25	V_{REF} + 0.04	V
V_{IH}	Input High Voltage		V_{REF} + 0.45		3.9	V
V_{IL}	Input Low Voltage		-0.3		V_{REF} - 0.6	V
V_{OH}	Output High Voltage	I_{OH} = -8 mA, V_{CCIO} = 2.3V	V_{CCIO} - 0.6			V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA, V_{CCIO} = 2.3V			0.54	V
$V_{IH(DC)}$	Input High Voltage		V_{REF} + 0.15		V_{CCIO} + 0.3	V
$V_{IL(DC)}$	Input Low Voltage		-0.3		V_{REF} - 0.15	V

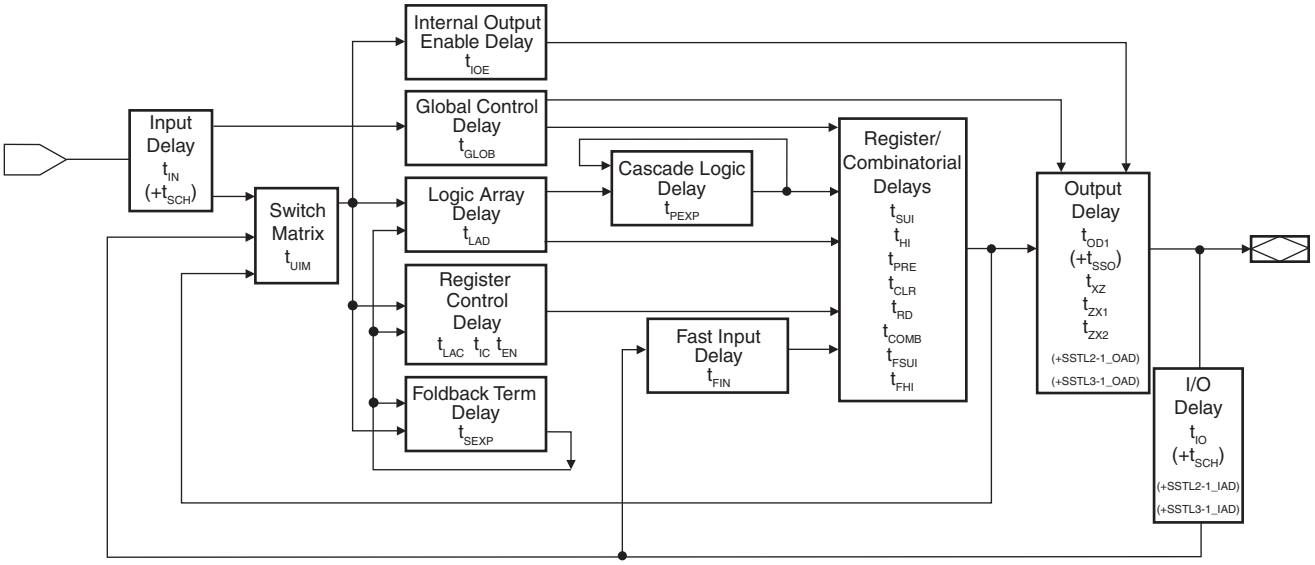
Notes: 1. Peak-to-peak noise on V_{REF} may not exceed ±2% V_{REF}, V_{REF} should track the variations in V_{CCIO}.
2. V_{TT} of transmitting device must track V_{REF} of receiving devices.

Table 8-7. SSTL3-1 DC Voltage Specifications

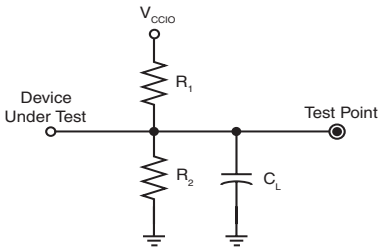
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CCIO}	Input Source Voltage		3.0	3.3	3.6	V
V_{REF} (1)	Input Reference Voltage		1.3	1.5	1.7	V
V_{TT} (2)	Termination Voltage		V_{REF} - 0.05	1.5	V_{REF} + 0.05	V
V_{IH}	Input High Voltage		V_{REF} + 0.4		V_{CCIO} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		V_{REF} - 0.6	V
V_{OH}	Output High Voltage	I_{OH} = -8 mA, V_{CCIO} = 3V	V_{CCIO} - 1.1			V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA, V_{CCIO} = 2.3V			0.7	V
$V_{IH(DC)}$	Input High Voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
$V_{IL(DC)}$	Input Low Voltage		-0.3		V_{REF} - 0.18	V

Notes: 1. Peak-to-peak noise on V_{REF} may not exceed ±2% V_{REF}, V_{REF} should track the variations in V_{CCIO}.
2. V_{TT} of transmitting device must track V_{REF} of receiving devices.

9. Timing Model



10. Output AC Test Loads



	R1	R2	CL
LVTTL	350 Ohm	350 Ohm	35 pF
LVCMOS33	300 Ohm	300 Ohm	35 pF
LVCMOS25	200 Ohm	200 Ohm	35 pF
LVCMOS18	150 Ohm	150 Ohm	35 pF

Note: C_L includes test fixtures and probe capacitance.

11. AC Characteristics

Table 11-1. AC Characteristics [1]

Symbol	Parameter		-5		-7		Units
			Min	Max	Min	Max	
t_{PD1_INP}	Delay for Single Input to Non-registered Output			5.0		6	ns
t_{PD1}	Input or Feedback to Non-registered Output			7		7.5	ns
t_{PD2}	Input or Feedback to Non-registered Feedback			4.2		4.7	ns
t_{SU}	Global Clock Setup Time		2.2		2.8		ns
t_{H}	Global Clock Hold Time		0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input		1		2		ns
t_{FH}	Global Clock Hold Time of Fast Input		0.5		0.75		ns
t_{COP}	Global Clock to Output Delay			6		6.9	ns
t_{CH}	Global Clock High Time		1.25		2		ns
t_{CL}	Global Clock Low Time		1.25		2		ns
t_{ASU}	Array Clock Setup Time		1.7		2.2		ns
t_{AH}	Array Clock Hold Time		0.50		0.60		ns
t_{ACOP}	Array Clock to Output Delay			6.5		7.5	ns
t_{ACH}	Array Clock High Time		1.75		2.5		ns
t_{ACL}	Array Clock Low Time		1.75		2.5		ns
t_{CNT}	Minimum Global Clock Period			3		4.75	ns
f_{CNT}	Maximum Internal Global Clock Frequency		333		210		MHz
t_{ACNT}	Minimum Array Clock Period			4		5.5	ns
f_{ACNT}	Maximum Internal Array Clock Frequency		250		181		MHz
$f_{MAX\_EXT\_SYNC}$	Maximum External Frequency	V_{CCIO} = 3.3V		122		103	MHz
$f_{MAX\_EXT\_ASYNC}$	Maximum External Frequency	V_{CCIO} = 3.3V		122		103	MHz
t_{IN}	Input Pad and Buffer Delay		0.7			0.9	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.7			0.9	ns
t_{FIN}	Fast Input Delay			1		1	ns
t_{SEXP}	Foldback Term Delay			2		3	ns
t_{PEXP}	Cascade Logic Delay			0.5		1.0	ns
t_{LAD}	Logic Array Delay			1.8		1.8	ns
t_{LAC}	Logic Control Delay			1.5		2	ns
t_{IOE}	Internal Output Enable Delay			2		2	ns
t_{OD1}	Output Buffer Delay (HD) (High Drive; C_L = 35 pF)	V_{CCIO} = 1.5V V_{CCIO} = 1.8V V_{CCIO} = 2.5V V_{CCIO} = 3.3V		4.5 4.0 3.5 2.8		4.5 4.0 3.5 2.8	ns

Table 11-1. AC Characteristics (Continued)[1]

Symbol	Parameter		-5 Min	-5 Max	-7 Min	-7 Max	Units
t_{ZX1}	Output Buffer Enable Delay (High Drive; C_L = 35 pF)	V_{CCIO} = 1.5V V_{CCIO} = 1.8V V_{CCIO} = 2.5V V_{CCIO} = 3.3V		5.0 4.5 3.5 3.0		6.0 5.5 4.5 4.0	ns
t_{ZX2}	Output Buffer Enable Delay (Low Drive; C_L = 35 pF)	V_{CCIO} = 1.5V V_{CCIO} = 1.8V V_{CCIO} = 2.5V V_{CCIO} = 3.3V		6.0 5.5 4.5 4.0		7.0 6.5 5.5 5.0	ns
t_{XZ}	Output Buffer Disable Delay (C_L = 5 pF)			4		4	ns
t_{SUI}	Register Setup Time		1.7		2.2		ns
t_{HI}	Register Hold Time		0.5		0.6		ns
t_{FSUI}	Register Setup Time of Fast Input		0.5		0.6		ns
t_{FHI}	Register Hold Time of Fast Input		0.5		0.6		ns
t_{RD}	Register Delay			0.7		1.2	ns
t_{COMB}	Combinatorial Delay			1.2		1.2	ns
t_{IC}	Array Clock Delay			1.8		1.8	ns
t_{EN}	Register Enable Time			2.5		3	ns
t_{GLOB}	Global Control Delay			1.8		2	ns
t_{PRE}	Register Preset Time			1.75		2	ns
t_{CLR}	Register Clear Time			1.75		2	ns
t_{UIM}	Switch Matrix Delay			0.5		0.8	ns
t_{SCH}	Schmitt Trigger Added Delay			1.5		2	ns
t_{SSO}	Output Added Delay for V_{CCIO} Level (LD)	V_{CCIO} = 1.5V V_{CCIO} = 1.8V V_{CCIO} = 2.5V V_{CCIO} = 3.3V		6.5 5.5 5.25 5		8.5 7.5 7.25 7	ns
SSTL2-1_IAD[2] SSTL3-1_IAD[2]	SSTL Input Delay Adder (HD)	V_{CCIO} = 2.5V V_{CCIO} = 3.3V		1.5 1.5		1.5 1.5	ns
SSTL2-1_OAD[2] SSTL3-1_OAD[2]	SSTL Output Delay Adder (HD)	V_{CCIO} = 2.5V V_{CCIO} = 3.3V		1 1		1 1	ns

Note: 1. See ordering information for valid part numbers.
2. SSTL is not supported for low drive output (LD).

12. Power-down Mode

The ATF1504BE includes an optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD pin is high, the device supply current is reduced to less than 100 µA. During power-down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down pin feature is enabled in the logic design file or through Atmel software. Designs using the power-down pin may not use the PD pin logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

Table 12-1. Power-down AC Characteristics[1][2]

Symbol	Parameter	-5/-7		Units
		Min	Max	
t_{IVDH}	Valid I, I/O before PD High	10		ns
t_{GVDH}	Valid OE[2] before PD High	10		ns
t_{CVDH}	Valid Clock[2] before PD High	10		ns
t_{DHIX}	I, I/O Don't Care after PD High		5	ns
t_{DHGX}	OE[2] Don't Care after PD High		5	ns
t_{DHCX}	Clock[2] Don't Care after PD High		5	ns
t_{DLIV}	PD Low to Valid I, I/O		2	µs
t_{DLGV}	PD Low to Valid OE (Pin or Term)		2	µs
t_{DLCV}	PD Low to Valid Clock (Pin or Term)		2	µs
t_{DLOV}	PD Low to Valid Output		2	µs

Notes: 1. For low-drive outputs, add t_{SSO}.
2. Pin or product term.

13. ATF1504BE Dedicated Pinouts

Table 13-1. ATF1504BE Dedicated Pinouts

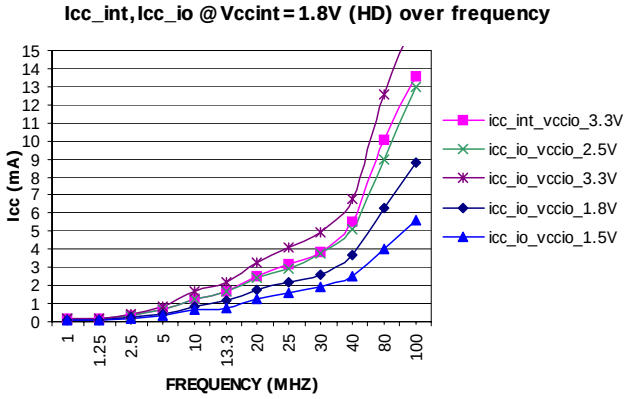
Dedicated Pin	44-lead TQFP	100-lead TQFP
INPUT / OE2 / GCLK2	40	90
INPUT / GCLR	39	89
INPUT / OE1	38	88
INPUT / GCLK1	37	87
I/O / GCLK3	35	85
I/O / PD1 / V_{REFA}	5	12
I/O / PD2	19	42
I/O / V_{REFB}	25	60
I/O / TDI (JTAG)	1	4
I/O / TMS (JTAG)	7	15
I/O / TCK (JTAG)	26	62
I/O / TDO (JTAG)	32	73
GND	4, 16, 24, 36	11, 26, 38, 43, 59, 74, 86, 95
V_{CCINT}	17, 41	39, 91
V_{CCIOA}	9	3, 18, 34
V_{CCIOB}	29	51, 66, 82
N/C	-	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78
# of Signal Pins	36	68
# User I/O Pins	32	64

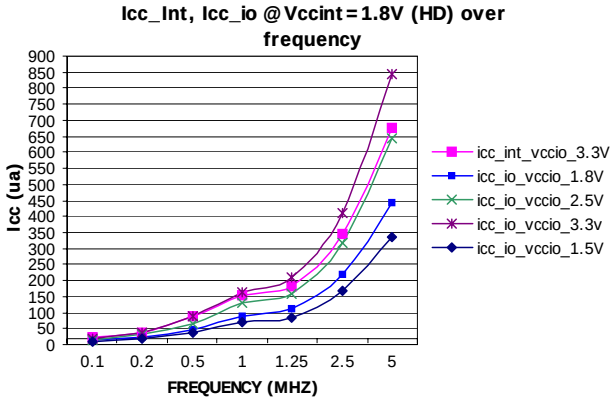
OE (1, 2)	Global OE pins
GCLR	Global Clear pin
GCLK (1, 2, 3)	Global Clock pins
PD (1, 2)	Power-down pins
TDI, TMS, TCK, TDO	JTAG pins used for boundary-scan testing or in-system programming
GND	Ground pins
V_{CCINT}	V_{CC} pins for the device (+1.8V)
V_{CCIOA}	LAB A and B – V_{CC} supply pins for I/Os (1.5V, 1.8V, 2.5V, or 3.3V)
V_{CCIOB}	LAB C and D – V_{CC} supply pins for I/Os (1.5V, 1.8V, 2.5V, or 3.3V)
V_{REFA}	Reference voltage pin for SSTL inputs in banks A and B
V_{REFB}	Reference voltage pin for SSTL inputs in banks C and D

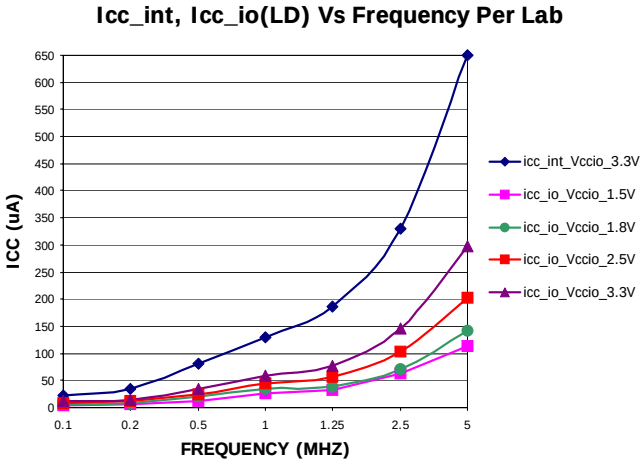
Table 13-2. ATF1504BE I/O Pinouts

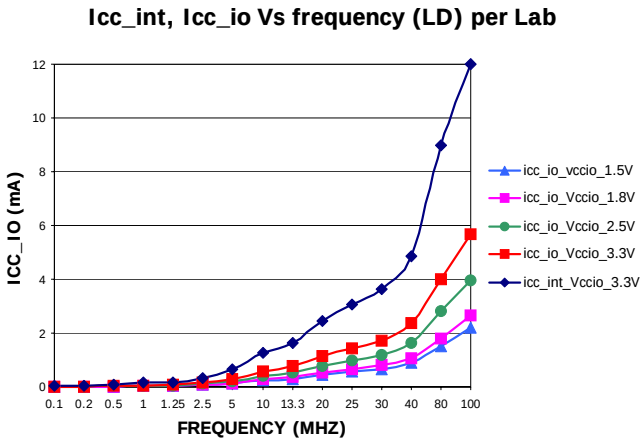
MC	Logic Block	44-lead TQFP	100-lead TQFP	MC	Logic Block	44-lead TQFP	100-lead TQFP
1	A	6	14	33	C	18	40
2	A	-	13	34	C	-	41
3/ **PD1/ VREFA**	A	5	12	35/ **PD2**	C	19	42
4	A	3	10	36	C	20	44
5	A	2	9	37	C	21	45
6	A	-	8	38	C	-	46
7	A	-	6	39	C	-	47
8/ **TDI**	A	1	4	40	C	22	48
9	A	-	100	41	C	23	52
10	A	-	99	42	C	-	54
11	A	44	98	43	C	-	56
12	A	-	97	44	C	-	57
13	A	-	96	45	C	-	58
14	A	43	94	46/ **VREFB**	C	25	60
15	A	-	93	47	C	-	61
16	A	42	92	48/ **TCK**	C	26	62
17	B	15	37	49	D	27	63
18	B	-	36	50	D	-	64
19	B	14	35	51	D	28	65
20	B	13	33	52	D	30	67
21	B	12	32	53	D	31	68
22	B	-	31	54	D	-	69
23	B	-	30	55	D	-	71
24	B	11	29	56/ **TDO**	D	32	73
25	B	10	25	57	D	33	75
26	B	-	23	58	D	-	76
27	B	-	21	59	D	-	79
28	B	-	20	60	D	-	80
29	B	-	19	61	D	-	81
30	B	8	17	62	D	34	83
31	B	-	16	63	D	-	84
32/ **TMS**	B	7	15	64/ **GCLK3**	D	35	85

14. Typical DC and AC Characteristic Graphs

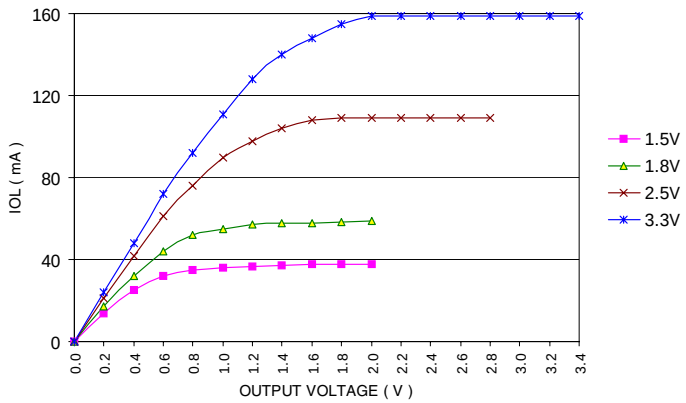




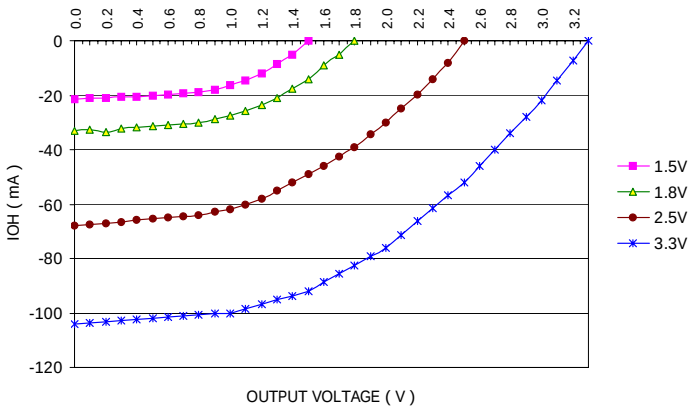




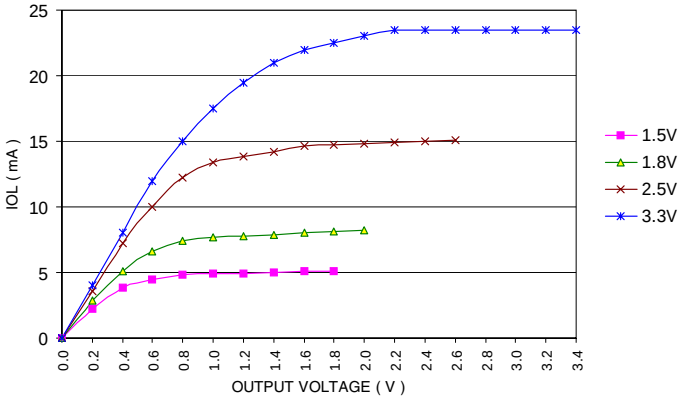
OUTPUT SINK CURRENT(IOL) VS. OUTPUT VOLTAGE
(VCCINT = 1.8V, VCCIO = 1.5-3.3V, TA = 25C), High Drive



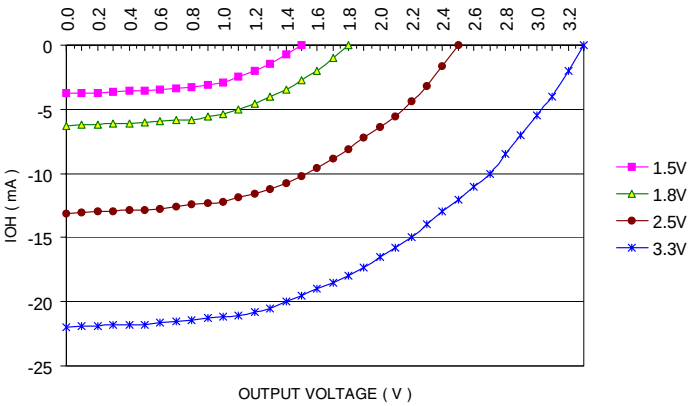
OUTPUT SOURCE CURRENT(IOH) VS. OUTPUT VOLTAGE
(VCCINT = 1.8V, VCCIO = 1.5-3.3V, TA = 25C), High Drive



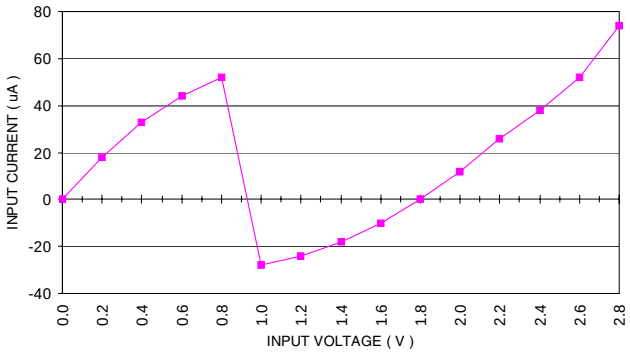
OUTPUT SINK CURRENT(IOL) VS. OUTPUT VOLTAGE
(VCCINT = 1.8V, VCCIO = 1.5-3.3V, TA = 25C), Low Drive



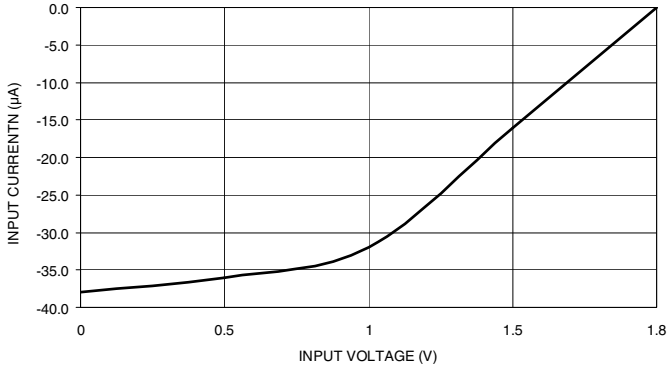
OUTPUT SOURCE CURRENT(IOH) VS. OUTPUT VOLTAGE
(VCCINT = 1.8V, VCCIO =1.5-3.3V, TA = 25C), Low Drive



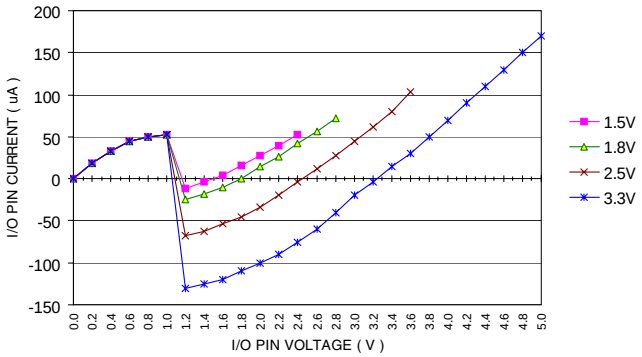
INPUT CURRENT VS. INPUT VOLTAGE
INPUT PIN (VCCINT = 1.8V, TA = 25C)
(PIN-KEEPER ON)



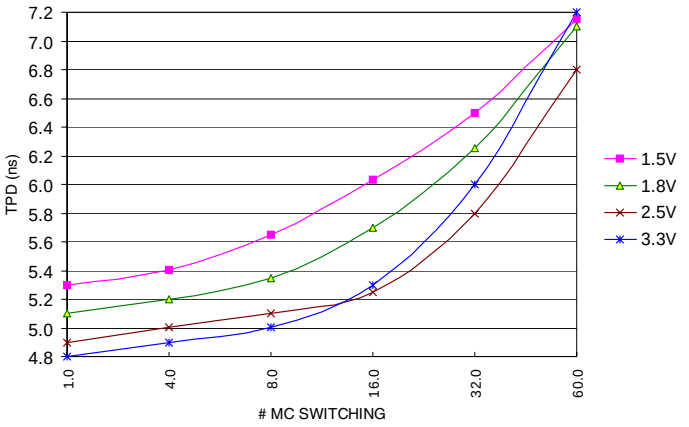
INPUT & I/O CURRENT VS. INPUT VOLTAGE
V_{CCINT} = 1.8V, V_{CCIO} = 1.8V (T_A = 25°C)
(Pull-Up On)



I/O PIN CURRENT VS. I/O PIN VOLTAGE
I/O PIN (VCCINT = 1.8V, VCCIO = 1.5V-3.3V, TA = 25C)
(PIN KEEPER ON)



TPD VS. # MC SWITCHING
(VCCINT = 1.8V, VCCIO = 1.5-3.3V, TA = 25C)



15. Ordering Information

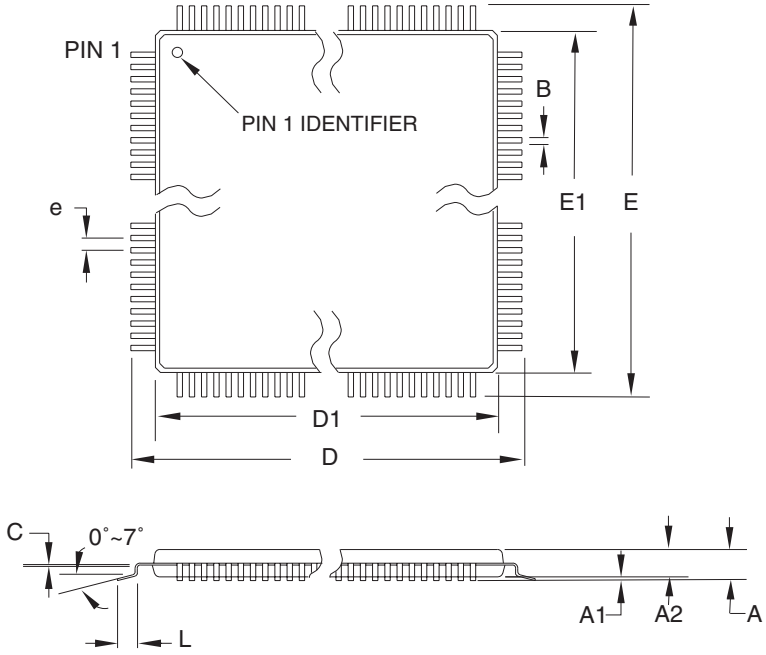
15.1 Lead-free Package Options (RoHS Compliant)

t_{PD} (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
5	6	ATF1504BE-5AX100	100A	Commercial (0° C to +70° C)
7	6.5	ATF1504BE-7AU100	100A	Industrial (-40° C to +85° C)
5	6	ATF1504BE-5AX44	44A	Commercial (0° C to +70° C)
7	6.5	ATF1504BE-7AU44	44A	Industrial (-40° C to +85° C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
100A	100-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)

16. Packaging Information

16.1 44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

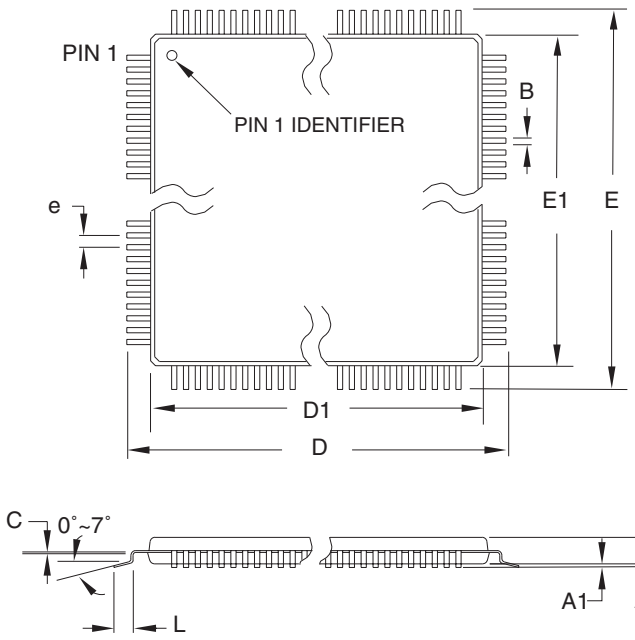
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

16.2 100A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100A,** 100-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	100A	C

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