HSMP-386x
Surface Mount PIN Diodes

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

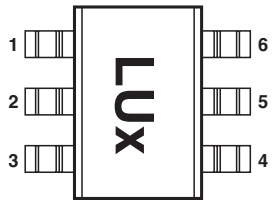
Description/Applications

The HSMP-386x series of general purpose PIN diodes are designed for two classes of applications. The first is attenuators where current consumption is the most important design consideration. The second application for this series of diodes is in switches where low capacitance is the driving issue for the designer.

The HSMP-386x series Total Capacitance (C_T) and Total Resistance (R_T) are typical specifications. For applications that require guaranteed performance, the general purpose HSMP-383x series is recommended.

A SPICE model is not available for PIN diodes as SPICE does not provide for a key PIN diode characteristic, carrier lifetime.

Pin Connections and Package Marking, SOT-363



Notes:

1. Package marking provides orientation, identification, and date code.
2. See "Electrical Specifications" for appropriate package marking.

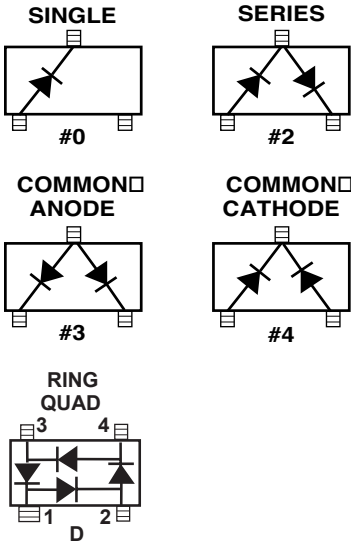
Features

- Unique Configurations in Surface Mount Packages
  - Add Flexibility
  - Save Board Space
  - Reduce Cost
- Switching
  - Low Distortion Switching
  - Low Capacitance
- Attenuating
  - Low Current Attenuating for Less Power Consumption
- Matched Diodes for Consistent Performance
- Better Thermal Conductivity for Higher Power Dissipation
- Low Failure in Time (FIT) Rate[1]
- Lead-free

Note:

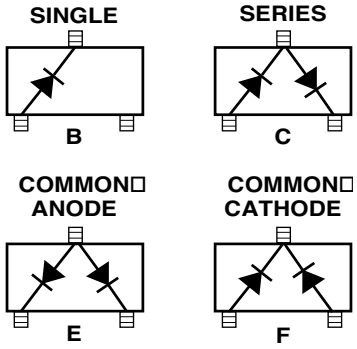
1. For more information see the Surface Mount PIN Reliability Data Sheet.

Package Lead Code Identification, SOT-23, SOT-143 (Top View)

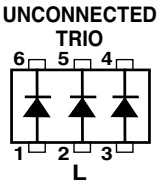


See separate data sheet HSMP-386D

Package Lead Code Identification, SOT-323 (Top View)



Package Lead Code Identification, SOT-363 (Top View)



Absolute Maximum Ratings[1] T_C = +25°C

Symbol	Parameter	Unit	SOT-23	SOT-323
I_f	Forward Current (1 µs Pulse)	Amp	1	1
P_{IV}	Peak Inverse Voltage	V	50	50
T_j	Junction Temperature	°C	150	150
T_{stg}	Storage Temperature	°C	-65 to 150	-65 to 150
θ_{jc}	Thermal Resistance[2]	°C/W	500	150

ESD WARNING:
Handling Precautions Should Be Taken To Avoid Static Discharge.

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_C = +25°C, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

Electrical Specifications T_C = 25°C, each diode

PIN General Purpose Diodes, Typical Specifications T_A = 25°C

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Typical Series Resistance R_S (Ω)	Typical Total Capacitance C_T (pF)
3860	L0	0	Single	50	3.0/1.5*	0.20
3862	L2	2	Series			
3863	L3	3	Common Anode			
3864	L4	4	Common Cathode			
386B	L0	B	Single			
386C	L2	C	Series			
386E	L3	E	Common Anode			
386F	L4	F	Common Cathode			
386L	LL	L	Unconnected Trio			
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10$ µA	I_F = 10 mA f = 100 MHz I_F = 100 mA*	V_R = 50 V f = 1 MHz

HSMP-386x Typical Parameters at $T_C = 25°C$

Part Number HSMP-	Total Resistance R_T (Ω)	Carrier Lifetime t (ns)	Reverse Recovery Time T_{rr} (ns)	Total Capacitance C_T (pF)
386x	22	500	80	0.20
Test Conditions	I_F = 1 mA f = 100 MHz	I_F = 50 mA T_R = 250 mA	V_R = 10 V I_F = 20 mA 90% Recovery	V_R = 50 V f = 1 MHz

Typical Performance, $T_C = 25°C$, each diode

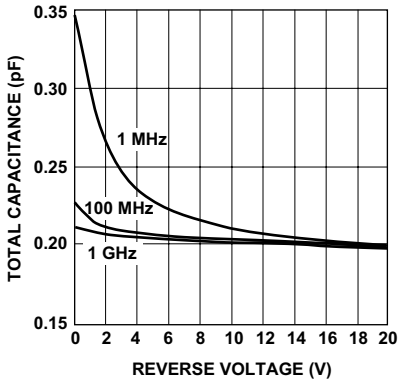


Figure 1. RF Capacitance vs. Reverse Bias.

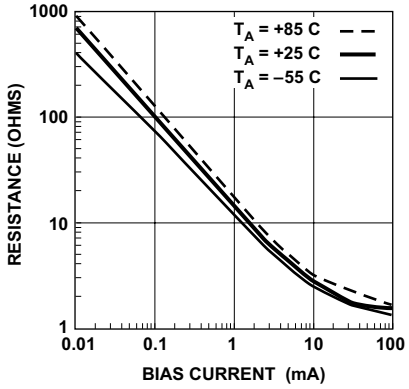


Figure 2. Typical RF Resistance vs. Forward Bias Current.

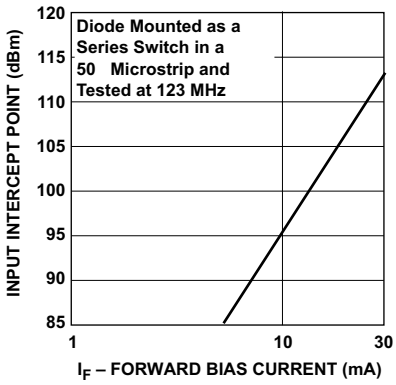


Figure 3. 2nd Harmonic Input Intercept Point vs. Forward Bias Current for Switch Diodes.

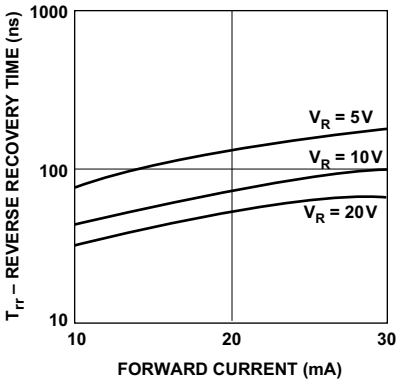


Figure 4. Reverse Recovery Time vs. Forward Current for Various Reverse Voltages.

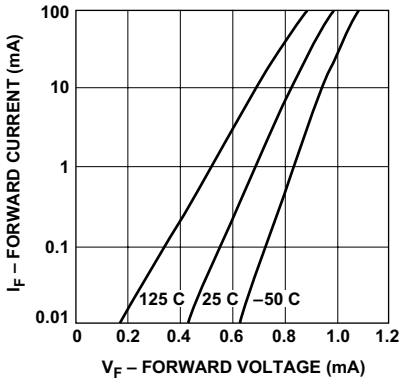
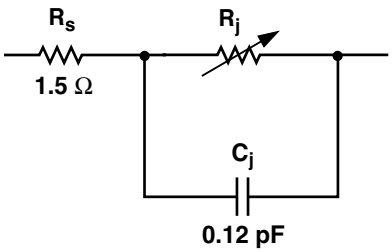


Figure 5. Forward Current vs. Forward Voltage.

Equivalent Circuit Model

HSMP-386x Chip*



$R_T = 1.5 + R_j$

$C_T = C_P + C_j$

$R_j = \frac{12}{I^{0.9}} \Omega$

I = Forward Bias Current in mA

* See AN1124 for package models

Typical Applications for Multiple Diode Products

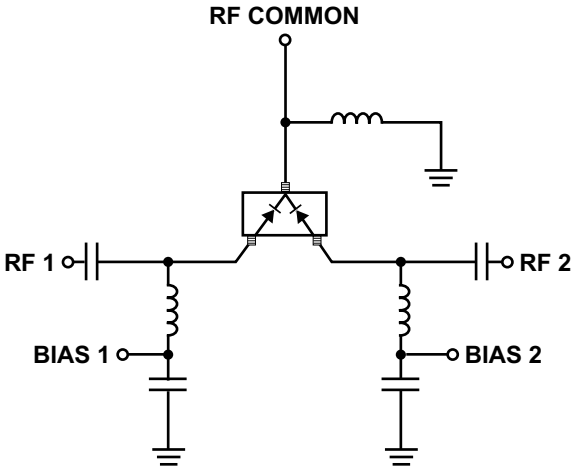


Figure 6. Simple SPDT Switch, Using Only Positive Current.

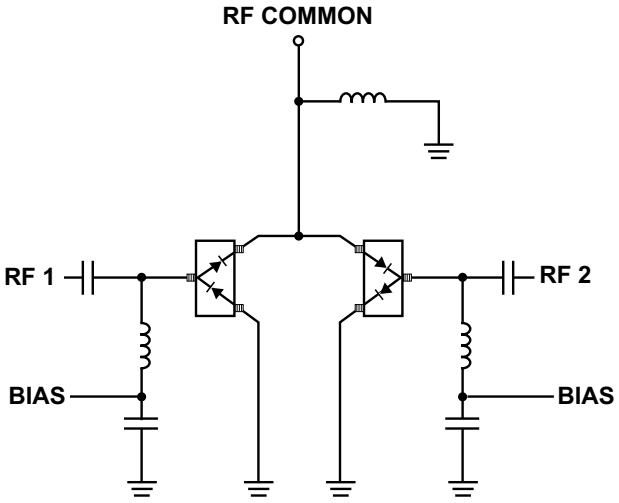


Figure 7. High Isolation SPDT Switch, Dual Bias.

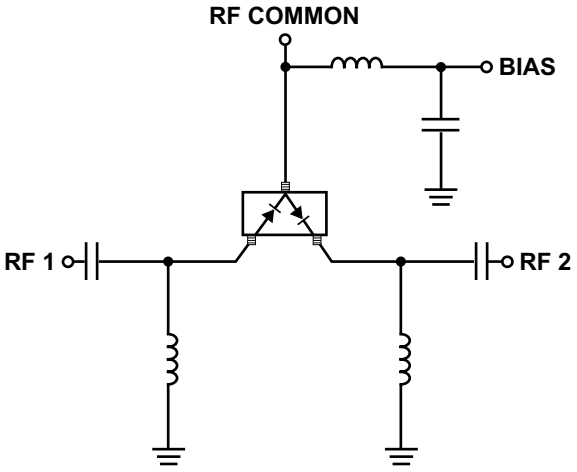


Figure 8. Switch Using Both Positive and Negative Current.

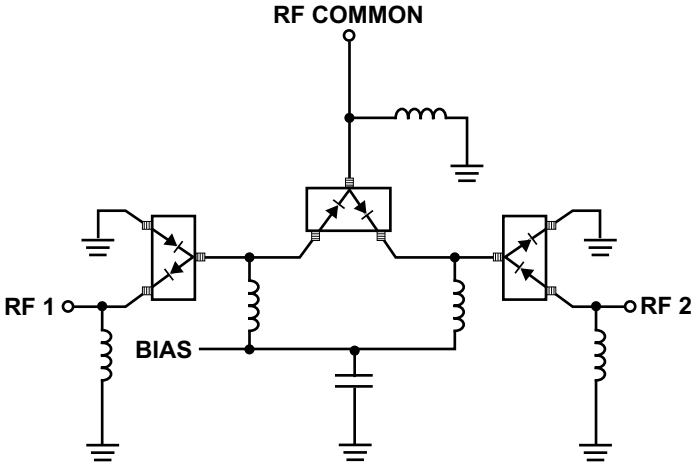


Figure 9. Very High Isolation SPDT Switch, Dual Bias.

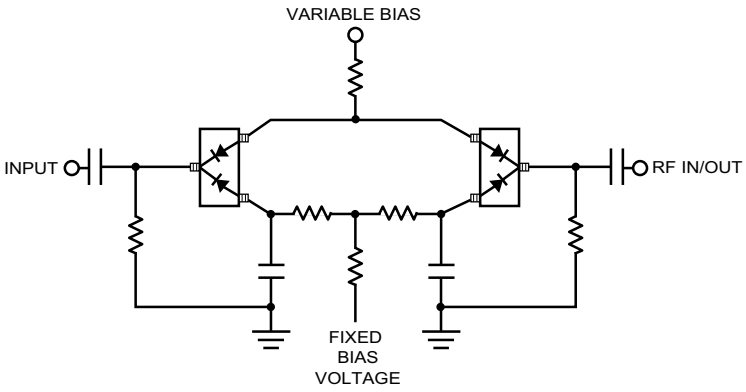


Figure 10. Four Diode π Attenuator. See AN1048 for details.

Typical Applications for Multiple Diode Products (continued)

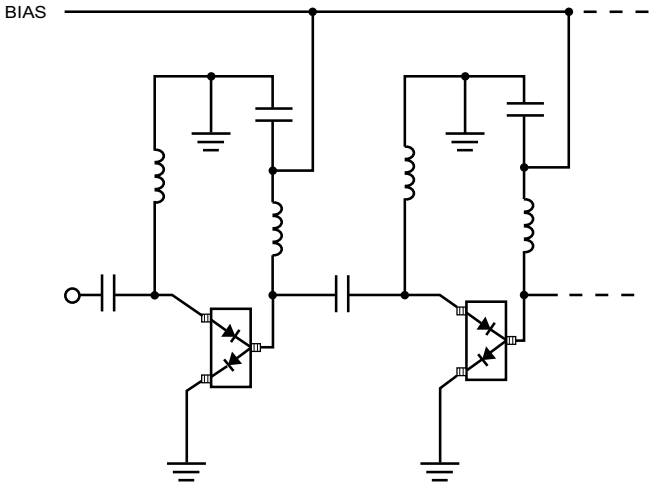
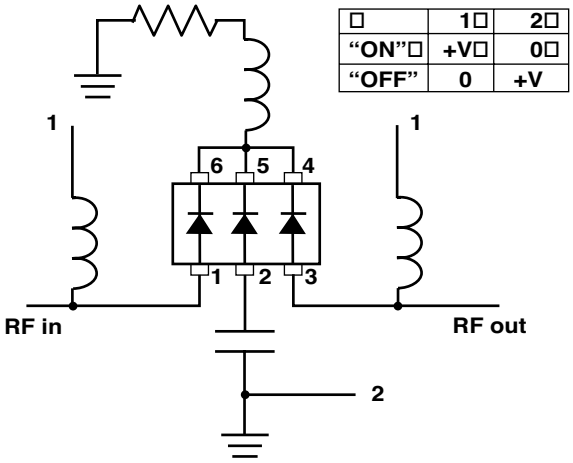


Figure 11. High Isolation SPST Switch (Repeat Cells as Required).



	1	2
"ON"	+V	0
"OFF"	0	+V

Figure 12. HSMP-386L Unconnected Trio used in a Positive Voltage, High Isolation Switch.

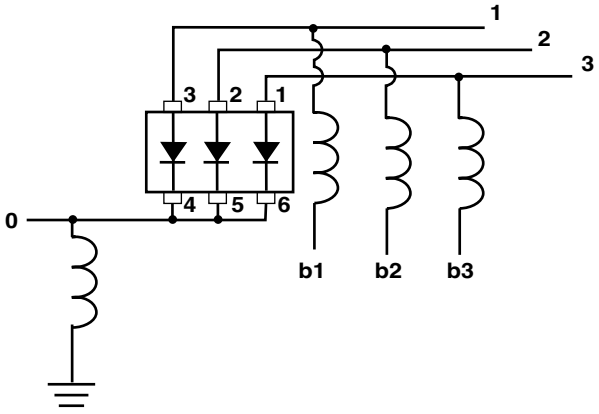
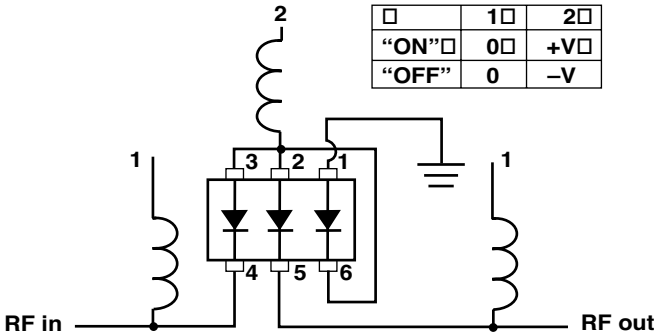


Figure 13. HSMP-386L used in a SP3T Switch.

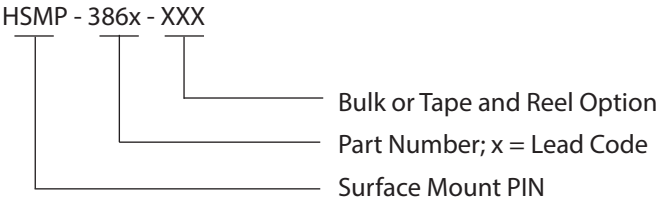


	1	2
"ON"	0	+V
"OFF"	0	–V

Figure 14. HSMP-386L Unconnected Trio used in a Dual Voltage, High Isolation Switch.

Ordering Information

Specify part number followed by option. For example:



Option Descriptions

-BLKG = Bulk, 100 pcs. per antistatic bag
-TR1G = Tape and Reel, 3000 devices per 7" reel
-TR2G = Tape and Reel, 10,000 devices per 13" reel

Tape and Reeling conforms to Electronic Industries RS-481, "Taping of Surface Mounted Components for Automated Placement."

Assembly Information

SOT-323 PCB Footprint

Recommended PCB pad layouts for the miniature SOT packages are shown in Figures 15, 16, 17. These layouts provide ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the performance.

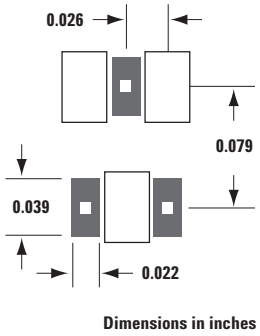


Figure 15. Recommended PCB Pad Layout for Avago's SC70 3L/SOT-323 Products.

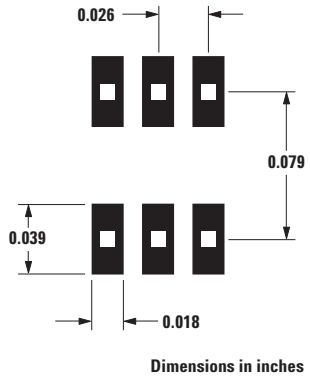


Figure 16. Recommended PCB Pad Layout for Avago's SC70 6L/SOT-363 Products.

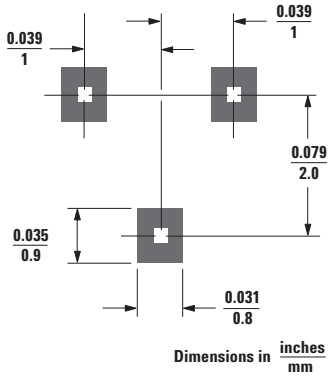


Figure 17. Recommended PCB Pad Layout for Avago's SOT-23 Products.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT package, will reach solder reflow temperatures faster than those with a greater mass.

Avago's diodes have been qualified to the time-temperature profile shown in Figure 18. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 260°C.

These parameters are typical for a surface mount assembly process for Avago diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

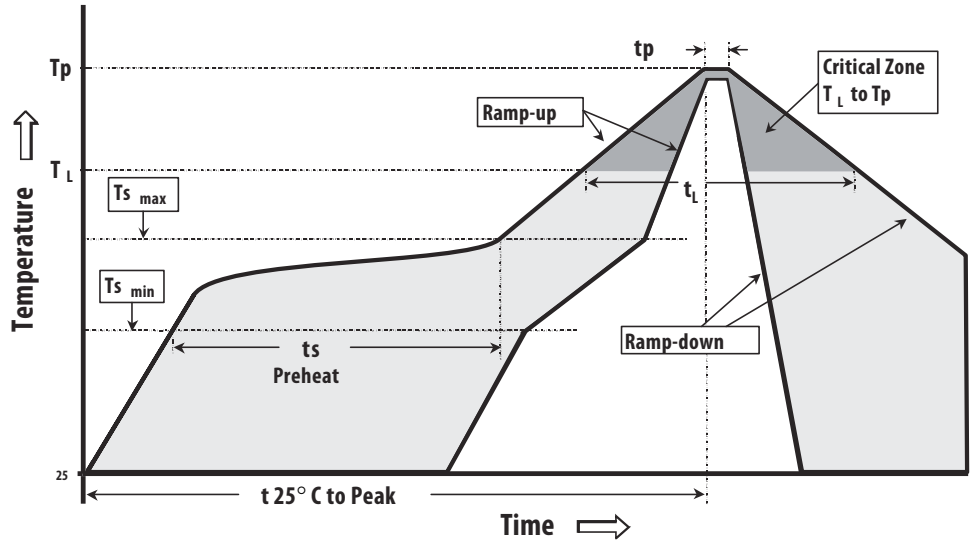


Figure 18. Surface Mount Assembly Profile.

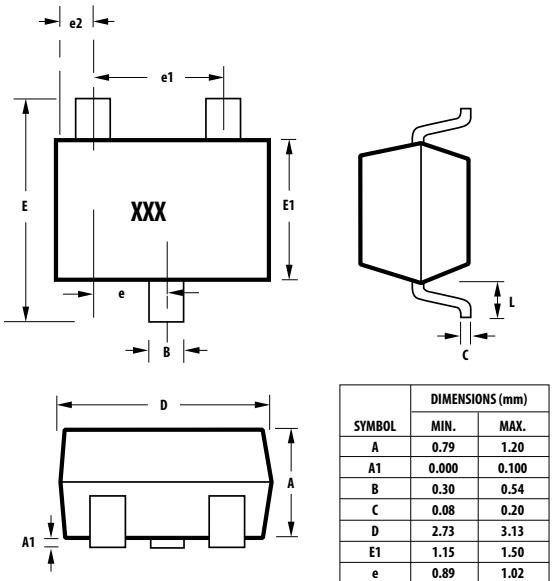
Lead-Free Reflow Profile Recommendation (IPC/JEDEC J-STD-020C)

Reflow Parameter		Lead-Free Assembly
Average ramp-up rate (Liquidus Temperature ($T_{S(max)}$ to Peak)		3°C/ second max
Preheat	Temperature Min ($T_{S(min)}$)	150°C
	Temperature Max ($T_{S(max)}$)	200°C
	Time (min to max) (t_S)	60-180 seconds
Ts(max) to TL Ramp-up Rate		3°C/second max
Time maintained above:	Temperature (T_L)	217°C
	Time (t_L)	60-150 seconds
Peak Temperature (T_p)		260 +0/-5°C
Time within 5 °C of actual Peak temperature (t_p)		20-40 seconds
Ramp-down Rate		6°C/second max
Time 25 °C to Peak Temperature		8 minutes max

Note 1: All temperatures refer to topside of the package, measured on the package body surface

Package Dimensions

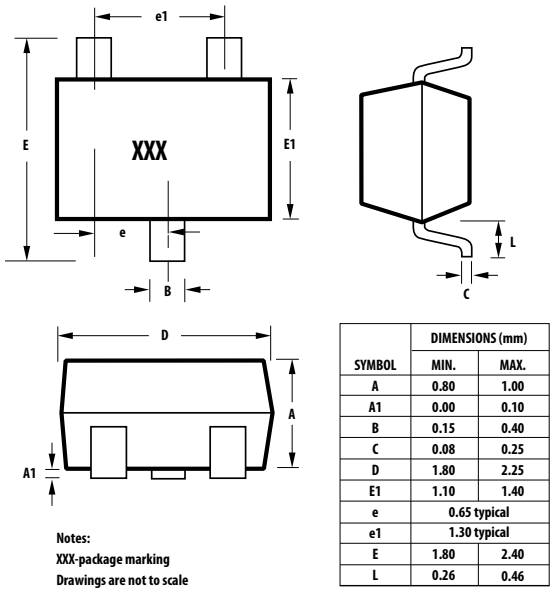
Outline 23 (SOT-23)



SYMBOL	DIMENSIONS (mm)	
	MIN.	MAX.
A	0.79	1.20
A1	0.000	0.100
B	0.30	0.54
C	0.08	0.20
D	2.73	3.13
E1	1.15	1.50
e	0.89	1.02
e1	1.78	2.04
e2	0.45	0.60
E	2.10	2.70
L	0.45	0.69

Notes:
XXX-package marking
Drawings are not to scale

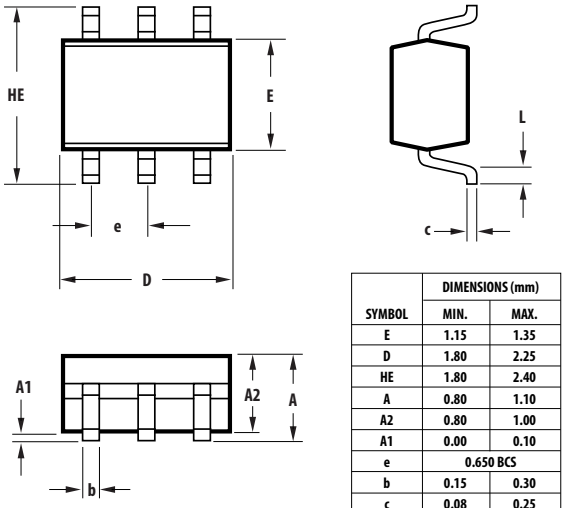
Outline SOT-323 (SC-70, 3 Lead)



SYMBOL	DIMENSIONS (mm)	
	MIN.	MAX.
A	0.80	1.00
A1	0.00	0.10
B	0.15	0.40
C	0.08	0.25
D	1.80	2.25
E1	1.10	1.40
e	0.65 typical	
e1	1.30 typical	
E	1.80	2.40
L	0.26	0.46

Notes:
XXX-package marking
Drawings are not to scale

Outline 363 (SC-70, 6 Lead)

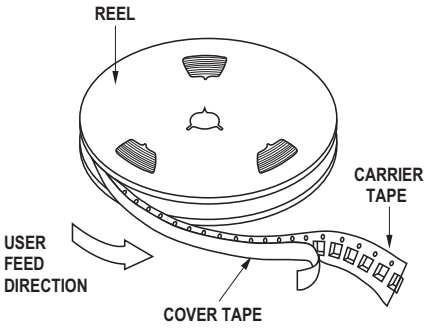


SYMBOL	DIMENSIONS (mm)	
	MIN.	MAX.
E	1.15	1.35
D	1.80	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
e	0.650 BCS	
b	0.15	0.30
c	0.08	0.25
L	0.10	0.46

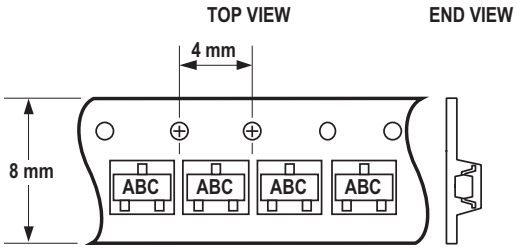
Package Characteristics

Lead Material ..... Copper (SOT-323/363); Alloy 42 (SOT-23)
Lead Finish ..... Tin 100% (Lead-free option)
Maximum Soldering Temperature ..... 260°C for 5 seconds
Minimum Lead Strength ..... 2 pounds pull
Typical Package Inductance ..... 2 nH
Typical Package Capacitance ..... 0.08 pF (opposite leads)

Device Orientation

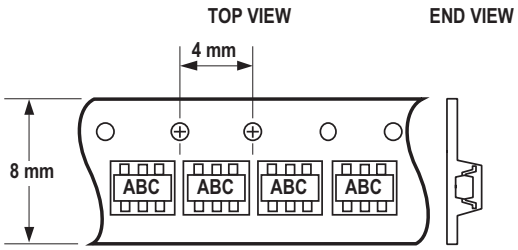


For Outlines SOT-23, -323



Note: "AB" represents package marking code.
"C" represents date code.

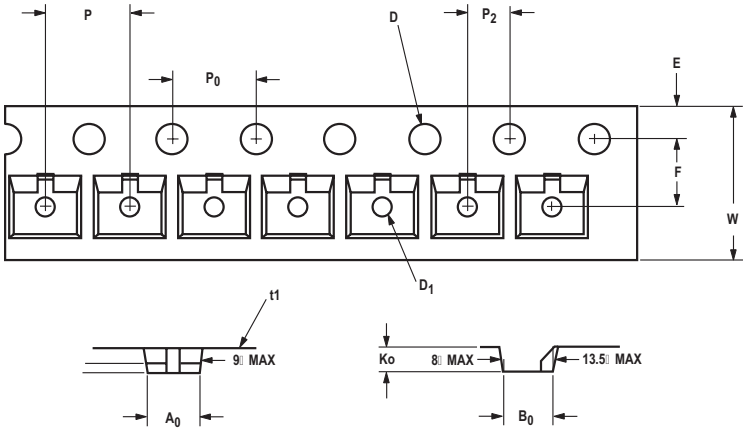
For Outline SOT-363



Note: "AB" represents package marking code.
"C" represents date code.

Tape Dimensions and Product Orientation

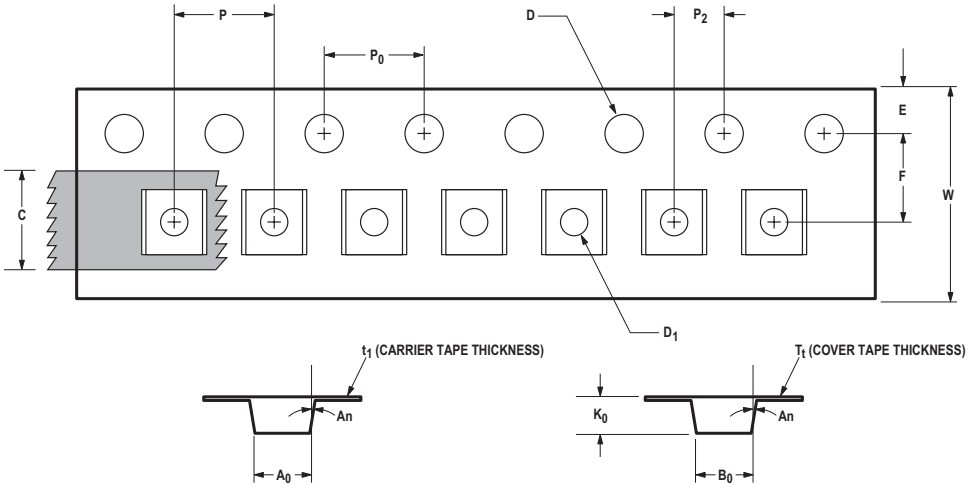
For Outline SOT-23



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.15 ± 0.10	0.124 ± 0.004
	WIDTH	B_0	2.77 ± 0.10	0.109 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.05	0.039 ± 0.002
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 + 0.30 - 0.10	0.315 + 0.012 - 0.004
	THICKNESS	t1	0.229 ± 0.013	0.009 ± 0.0005
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

Tape Dimensions and Product Orientation

For Outlines SOT-323, -363



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.40 ± 0.10	0.0□4 ± 0.004
	WIDTH	B_0	2.40 ± 0.10	0.0□4 ± 0.004
	DEPTH	K_0	1.20 ± 0.10	0.04□ ± 0.004
	PITCH	P	4.00 ± 0.10	0.15□ ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.0□ + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.0□1 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.15□ ± 0.004
	POSITION	E	1.□5 ± 0.10	0.0□ ± 0.004
CARRIER TAPE	WIDTH	W	□.00 ± 0.□0	0.□15 ± 0.012
	THICKNESS	t_1	0.254 ± 0.02	0.0100 ± 0.000□
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.0□2 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	□.50 ± 0.05	0.1□ ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.0□ ± 0.002
ANGLE	FOR SOT□2□ (SC□0□ LEAD)	An	□ °C MA□	
	FOR SOT□□□ (SC□0□ LEAD)		10°C MA□	

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-0293EN - October 21, 2013