

4-Mbit (256 K × 16) Static RAM

Features

- Temperature ranges
 - Industrial: -40 °C to 85 °C
- Pin and function compatible with CY7C1041CV33
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 90 \text{ mA}$
- Low CMOS standby power
 - $I_{SB2} = 10 \text{ mA}$
- 2.0 V data retention
- Automatic power-down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Available in Pb-free 48-ball VFPGA, 44-pin (400-mil) molded SOJ, and 44-pin TSOP II Packages

Functional Description

The CY7C1041DV33 is a high performance CMOS Static RAM organized as 256 K words by 16-bits. To write to the device, take chip enable (\overline{CE}) and write enable (\overline{WE}) inputs LOW. If byte low enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₀ to I/O₇) is written into the location specified on the address pins (A₀ to A₁₇). If byte high enable (\overline{BHE}) is LOW, then data from I/O pins (I/O₈ to I/O₁₅) is written into the location specified on the address pins (A₀ to A₁₇).

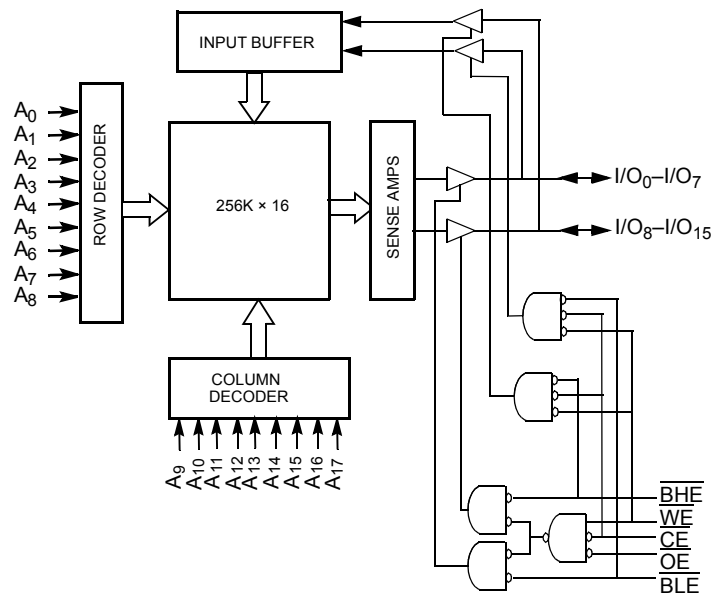
To read from the device, take chip enable (\overline{CE}) and output enable (\overline{OE}) LOW while forcing the write enable (\overline{WE}) HIGH. If \overline{BLE} is LOW, then data from the memory location specified by the address pins appears on I/O₀ to I/O₇. If \overline{BHE} is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the Truth Table on page 11 for a complete description of read and write modes.

The input and output pins (I/O₀ to I/O₁₅) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), outputs are disabled (\overline{OE} HIGH), \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW and \overline{WE} LOW).

The CY7C1041DV33 is available in a standard 44-pin 400-mil wide SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout and a 48-ball FBGA package.

For a complete list of related documentation, [click here](#).

Logic Block Diagram



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Selection Guide

Description	-10 (Industrial)	Unit
Maximum access time	10	ns
Maximum operating current	90	mA
Maximum CMOS standby current	10	mA

Pin Configuration

Figure 1. 48-ball VFBGA (Pinout 1) [1, 2]

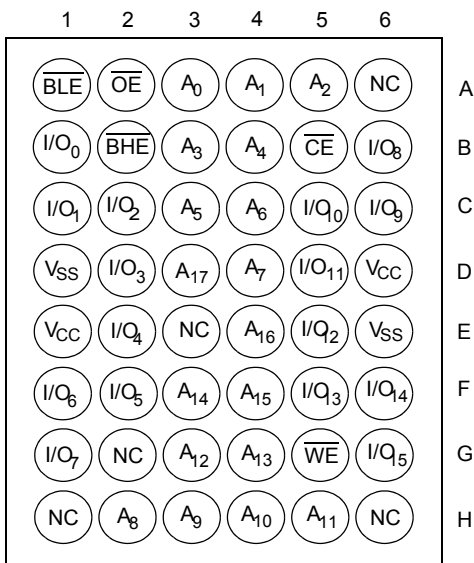


Figure 2. 48-ball VFBGA (Pinout 2) [1, 2]

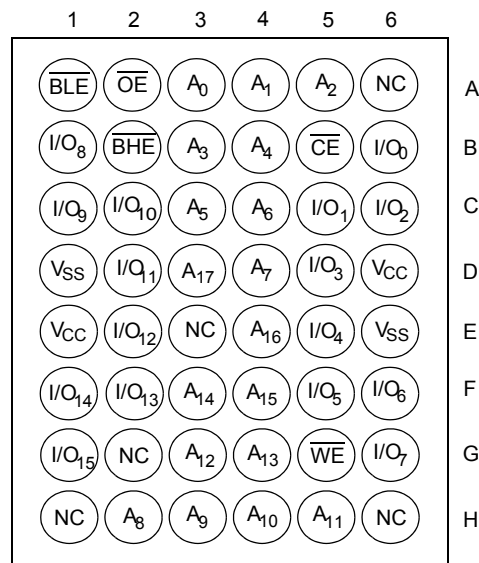
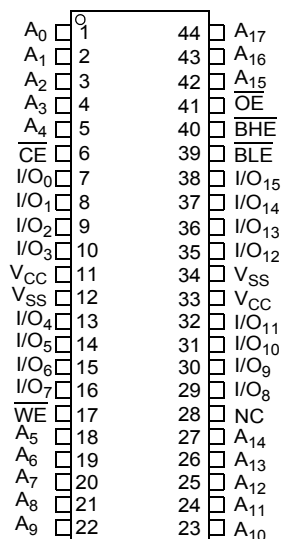


Figure 3. 44-pin SOJ/TSOP II pinout



Notes

1. NC pins are not connected on the die.
2. Pinout 1 is compliant with CY7C1041CV33 and pinout 2 is JEDEC compliant. The difference between the two is that the higher and lower byte I/Os (I/O_[7:0] and I/O_[15:8] balls) are swapped.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C
 Ambient temperature with power applied -55 °C to +125 °C
 Supply voltage on V_{CC} relative to GND ^[3] ... -0.3 V to +4.6 V
 DC voltage applied to outputs in high Z State ^[3] -0.3 V to $V_{CC} + 0.3$ V

DC input voltage ^[3] -0.3 V to $V_{CC} + 0.3$ V
 Current into outputs (LOW) 20 mA
 Static discharge voltage (MIL-STD-883, method 3015) > 2001 V
 Latch up current > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	-40 °C to +85 °C	3.3 V ± 0.3 V	10 ns

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10 (Industrial)		Unit	
			Min	Max		
V_{OH}	Output HIGH voltage	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	-	V	
V_{OL}	Output LOW voltage	$V_{CC} = \text{Min}, I_{OL} = 8.0 \text{ mA}$	-	0.4	V	
$V_{IH}^{[3]}$	Input HIGH voltage		2.0	$V_{CC} + 0.3$	V	
$V_{IL}^{[3]}$	Input LOW voltage		-0.3	0.8	V	
I_{IX}	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	+1	μA	
I_{OZ}	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$, output disabled	-1	+1	μA	
I_{CC}	V_{CC} operating supply current	$V_{CC} = \text{Max}, f = f_{MAX} = 1/t_{RC}$	100 MHz	-	90	mA
			83 MHz	-	80	mA
			66 MHz	-	70	mA
			40 MHz	-	60	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	Max V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	-	20	mA	
I_{SB2}	Automatic CE power-down current – CMOS inputs	Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$, $V_{IN} \geq V_{CC} - 0.3 \text{ V}$ or $V_{IN} \leq 0.3 \text{ V}$, $f = 0$	-	10	mA	

Note

3. Minimum voltage is -2.0 V and $V_{IH}(\text{max}) = V_{CC} + 2 \text{ V}$ for pulse durations of less than 20 ns.

Capacitance

Parameter ^[4]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 3.3 V	8	pF
C _{OUT}	I/O capacitance		8	pF

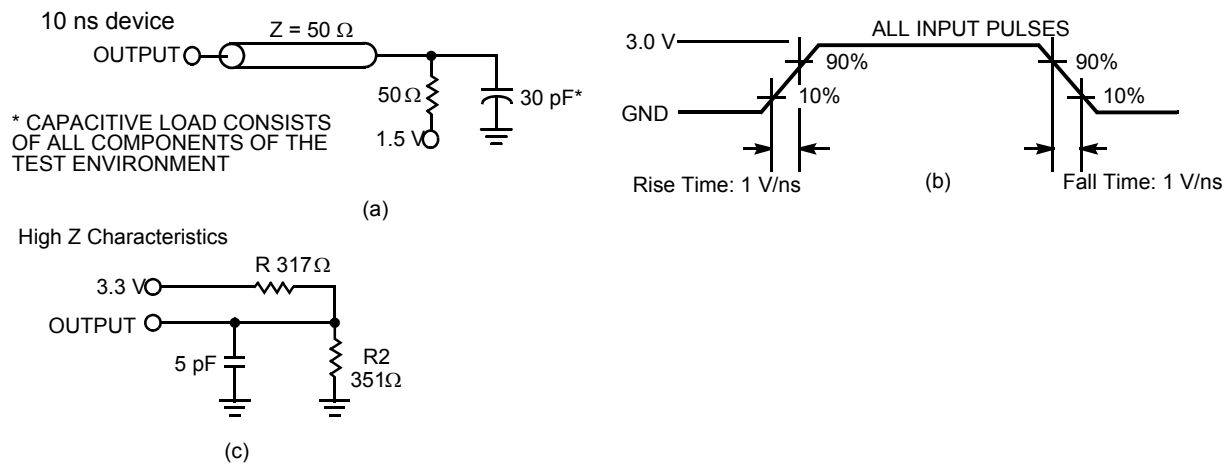
Thermal Resistance

Parameter ^[4]	Description	Test Conditions	48-ball FBGA Package	44-pin SOJ Package	44-pin TSOP II Package	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four layer printed circuit board	27.89	57.91	50.66	°C/W
Θ _{JC}	Thermal resistance (junction to case)		14.74	36.73	17.17	°C/W

AC Test Loads and Waveforms

The AC test loads and waveform diagram follows.

Figure 4. AC Test Loads and Waveforms ^[5]



Notes

- 4. Tested initially and after any design or process changes that may affect these parameters.
- 5. AC characteristics (except high Z) are tested using the load conditions shown in Figure 4 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 4 (c).

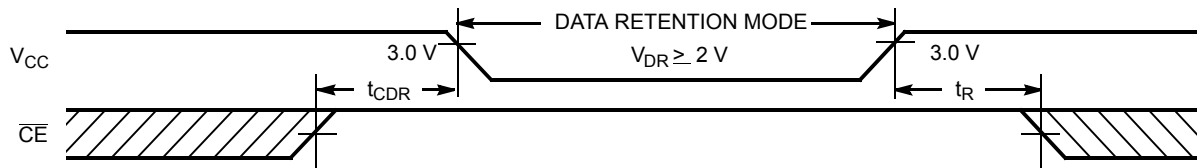
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions ^[6]	Min	Max	Unit
V_{DR}	V_{CC} for data retention		2.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR} = 2.0\text{ V}$, $\overline{CE} \geq V_{CC} - 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	10	mA
t_{CDR} ^[7]	Chip deselect to data retention time		0	–	ns
t_R ^[8]	Operation recovery time		t_{RC}	–	ns

Data Retention Waveform

Figure 5. Data Retention Waveform



Notes

6. No input may exceed $V_{CC} + 0.3\text{ V}$.
7. Tested initially and after any design or process changes that may affect these parameters.
8. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50\ \mu\text{s}$ or stable at $V_{CC(min.)} \geq 50\ \mu\text{s}$.

AC Switching Characteristics

Over the Operating Range

Parameter ^[9]	Description	-10 (Industrial)		Unit
		Min	Max	
Read Cycle				
$t_{power}^{[10]}$	V_{CC} (Typical) to the first access	100	–	μ s
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	\overline{CE} LOW to data valid	–	10	ns
t_{DOE}	\overline{OE} LOW to data valid	–	5	ns
t_{LZOE}	\overline{OE} LOW to low Z ^[11]	0	–	ns
t_{HZOE}	\overline{OE} HIGH to high Z ^[11, 12]	–	5	ns
t_{LZCE}	\overline{CE} LOW to low Z ^[11]	3	–	ns
t_{HZCE}	\overline{CE} HIGH to high Z ^[11, 12]	–	5	ns
t_{PU}	\overline{CE} LOW to power-up	0	–	ns
t_{PD}	\overline{CE} HIGH to power-down	–	10	ns
t_{DBE}	Byte enable to data valid	–	5	ns
t_{LZBE}	Byte enable to low Z	0	–	ns
t_{HZBE}	Byte disable to high Z	–	6	ns
Write Cycle ^[13, 14]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	\overline{CE} LOW to write end	7	–	ns
t_{AW}	Address setup to write end	7	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	\overline{WE} pulse width	7	–	ns
t_{SD}	Data setup to write end	5	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	\overline{WE} HIGH to low Z ^[11]	3	–	ns
t_{HZWE}	\overline{WE} LOW to high Z ^[11, 12]	–	5	ns
t_{BW}	Byte enable to end of write	7	–	ns

Notes

9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
10. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access is performed.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , t_{HZBE} is less than t_{LZBE} , and t_{HZWE} is less than t_{LZWE} for any given device.
12. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of Figure 4. Transition is measured when the outputs enter a high impedance state.
13. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and BHE or BLE, and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one signal can go inactive to terminate the write.
14. The minimum write cycle time for Write Cycle No. 4 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 6. Read Cycle No. 1 [15, 16]

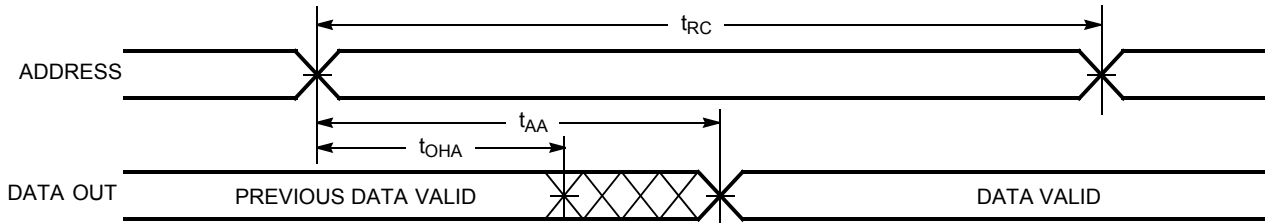
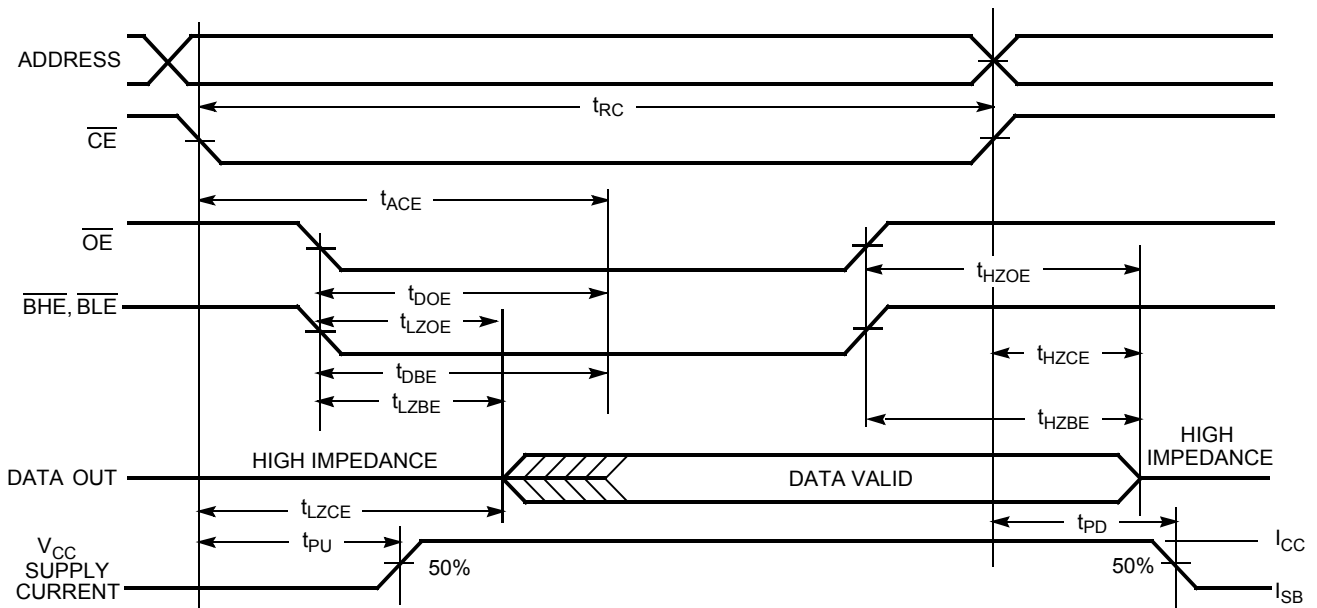


Figure 7. Read Cycle No. 2 (\overline{OE} Controlled) [16, 17]



Notes

- 15. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} , and \overline{BLE} = V_{IL} .
- 16. \overline{WE} is HIGH for read cycle.
- 17. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [18, 19]

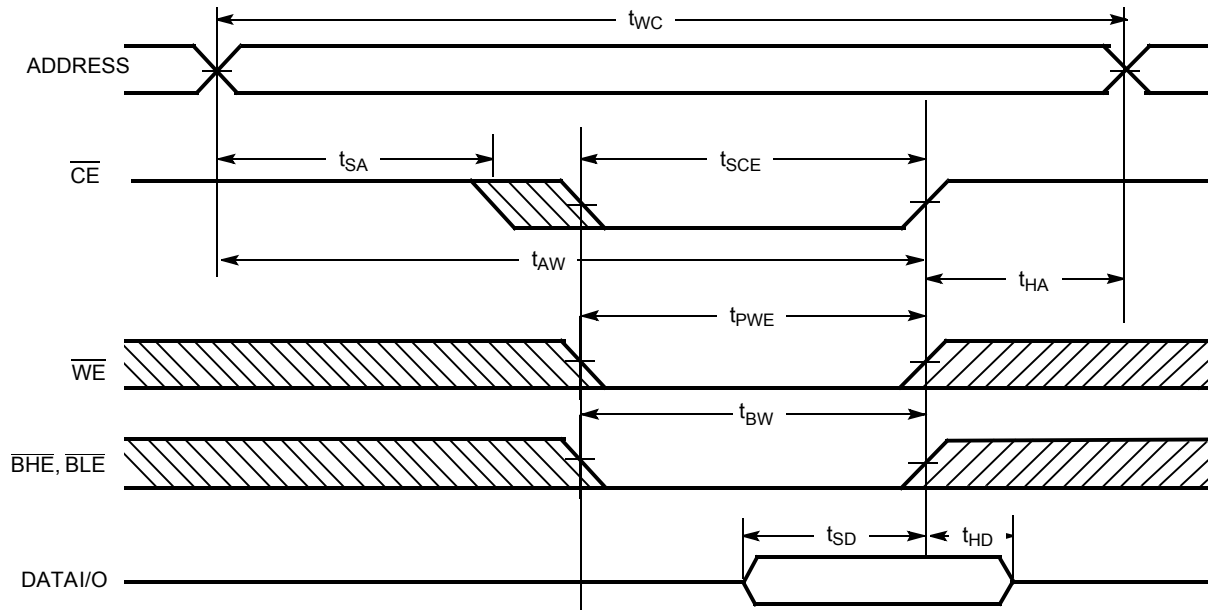
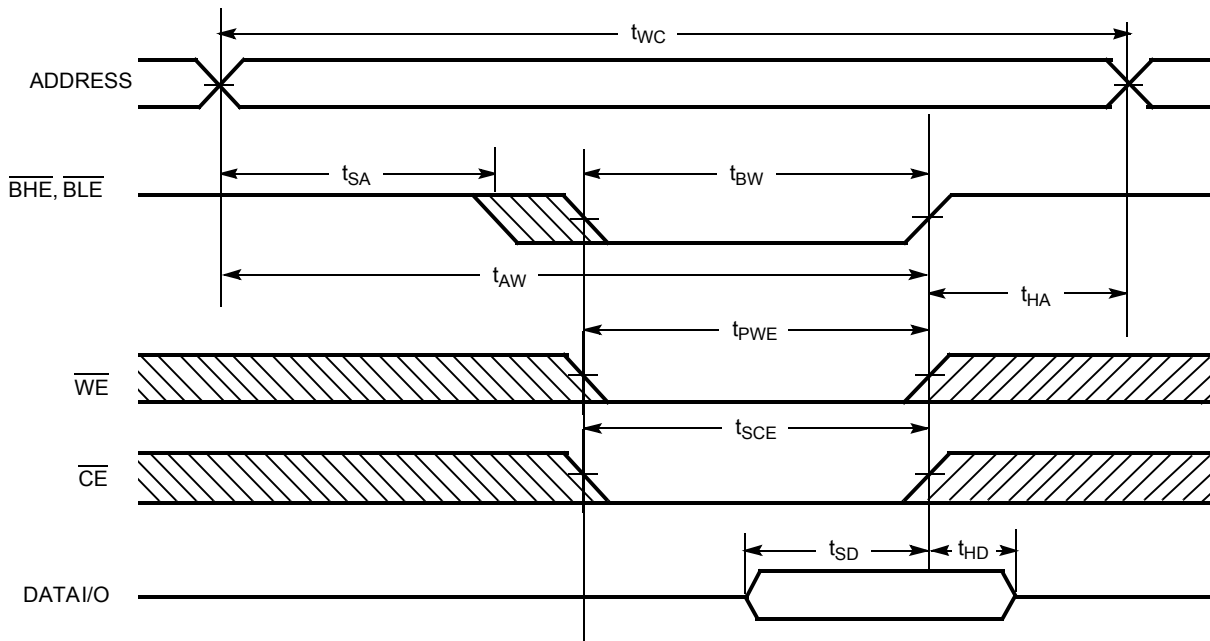


Figure 9. Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



Notes

- 18. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and $\overline{\text{BLE}} = V_{IH}$.
- 19. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} HIGH During Write) [20, 21]

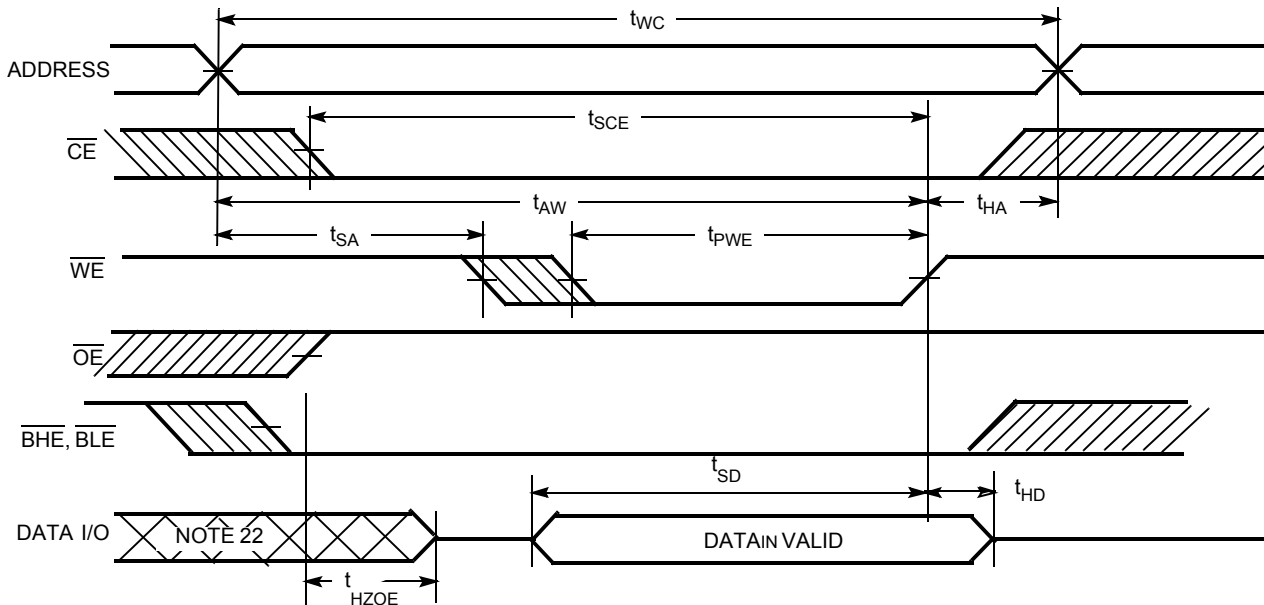
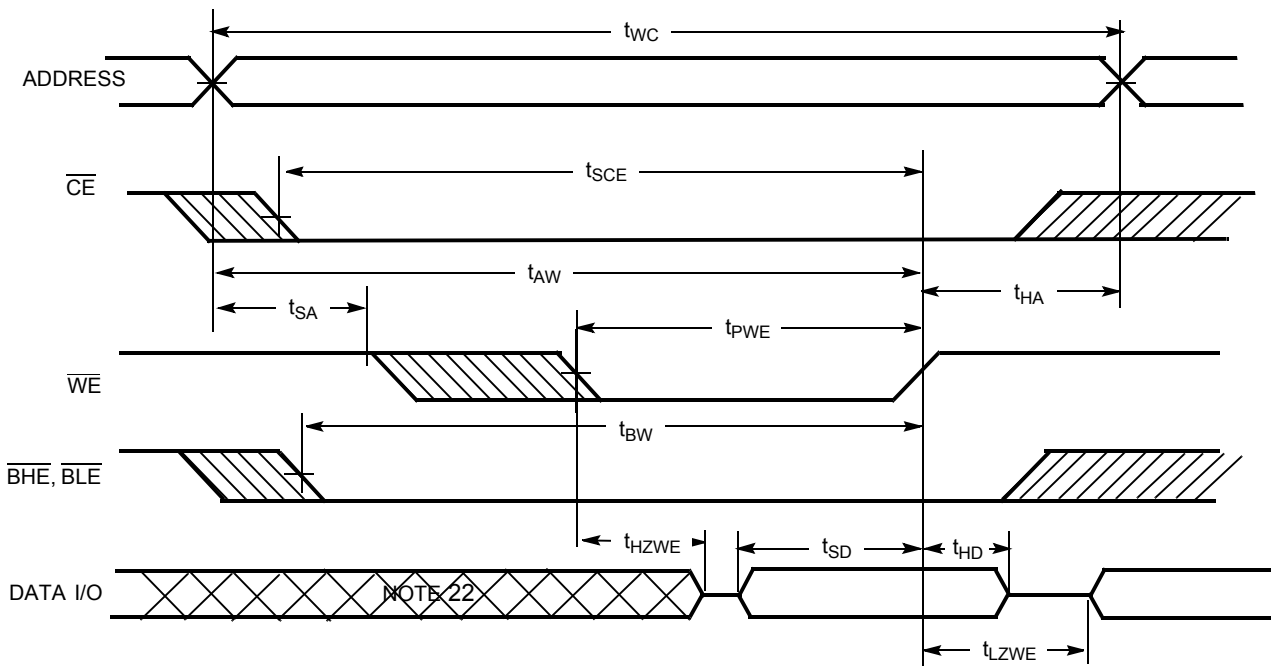


Figure 11. Write Cycle No. 4 (\overline{WE} Controlled, \overline{OE} LOW)



Notes

- 20. Data I/O is high impedance if \overline{OE} or \overline{BHE} and $\overline{BLE} = V_{IH}$.
- 21. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high impedance state.
- 22. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
H	X	X	X	X	High Z	High Z	Power down	Standby (I _{SB})
L	L	H	L	L	Data out	Data out	Read all bits	Active (I _{CC})
L	L	H	L	H	Data out	High Z	Read lower bits only	Active (I _{CC})
L	L	H	H	L	High Z	Data out	Read upper bits only	Active (I _{CC})
L	X	L	L	L	Data in	Data in	Write all bits	Active (I _{CC})
L	X	L	L	H	Data in	High Z	Write lower bits only	Active (I _{CC})
L	X	L	H	L	High Z	Data in	Write upper bits only	Active (I _{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I _{CC})
L	X	X	H	H	High Z	High Z	Selected, outputs disabled	Active (I _{CC})

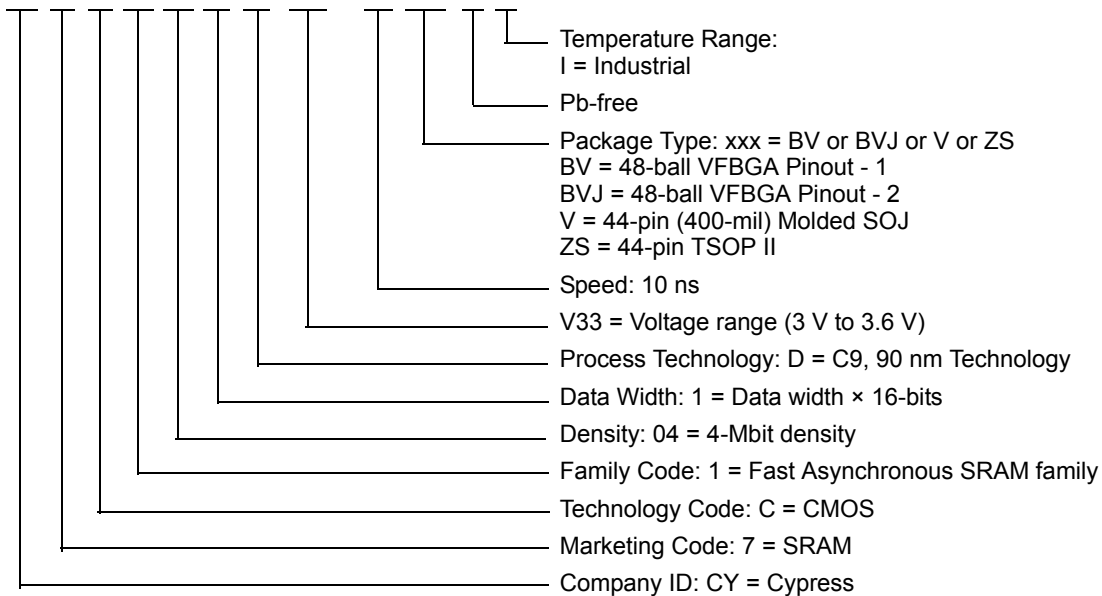
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1041DV33-10BVI	51-85150	48-ball VFBGA Pinout - 1 ^[23]	Industrial
	CY7C1041DV33-10BVXI		48-ball VFBGA (Pb-free) Pinout - 1 ^[23]	
	CY7C1041DV33-10BVJXI		48-ball VFBGA (Pb-free) Pinout - 2 ^[23]	
	CY7C1041DV33-10VXI	51-85082	44-pin (400-mil) Molded SOJ (Pb-free)	
	CY7C1041DV33-10ZSXI	51-85087	44-pin TSOP II (Pb-free)	

Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions

CY 7 C 1 04 1 D V33 - 10 XXX X I

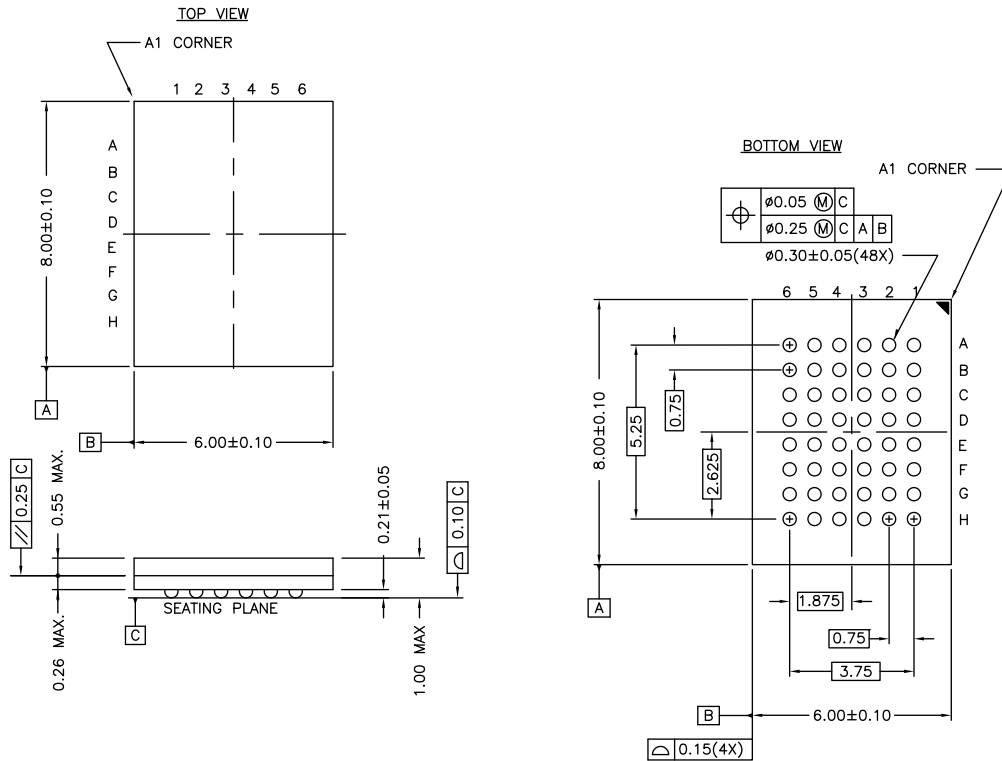


Note

23. Pinout 1 is compliant with CY7C1041CV33 and pinout 2 is JEDEC compliant. The difference between the two is that the higher and lower byte I/Os (I/O_[7:0] and I/O_[15:8] balls) are swapped.

Package Diagrams

Figure 12. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)
 posted on the Cypress web.

51-85150 *H

Package Diagrams (continued)

Figure 13. 44-pin Molded SOJ (400-mil) V44.4 Package Outline, 51-85082

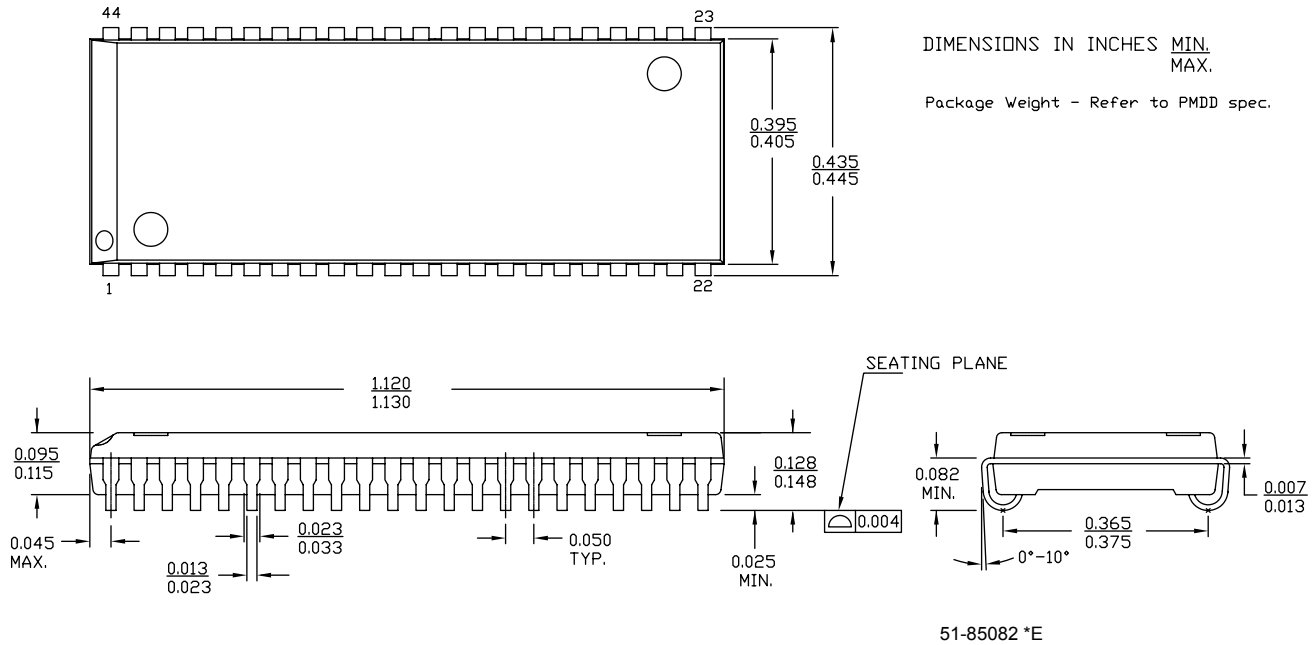
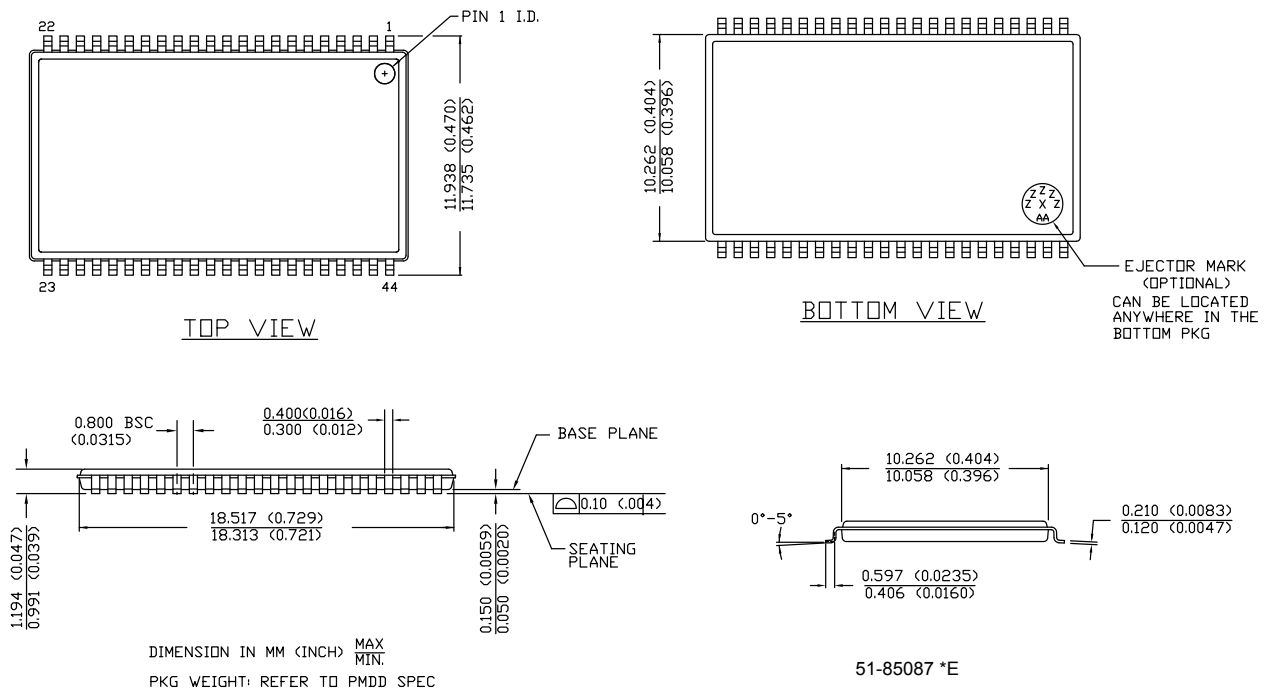


Figure 14. 44-pin TSOP Z44-II Package Outline, 51-85087



Acronyms

Acronym	Description
\overline{CE}	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
\overline{OE}	Output Enable
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
\overline{WE}	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1041DV33, 4-Mbit (256 K × 16) Static RAM				
Document Number: 38-05473				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	201560	SWI	See ECN	Advance Data sheet for C9 IPP
*A	233729	RKF	See ECN	1.AC, DC parameters are modified as per EROS(Spec # 01-2165) 2.Pb-free offering in the 'Ordering information'
*B	351117	PCI	See ECN	Changed from Advance to Preliminary Removed 15 and 20 ns Speed bin Corrected DC voltage (min) value in maximum ratings section from - 0.5 to - 0.3V Redefined I _{CC} values for Com'I and Ind'I temperature ranges I _{CC} (Com'I): Changed from 100, 80 and 67 mA to 90, 80 and 75 mA for 8, 10 and 12ns speed bins respectively I _{CC} (Ind'I): Changed from 80 and 67 mA to 90 and 85 mA for 10 and 12ns speed bins respectively Added Static Discharge Voltage and latch-up current spec Added V _{IH(max)} spec in Note# 2 Changed Note# 4 on AC Test Loads Changed reference voltage level for measurement of Hi-Z parameters from ±500 mV to ±200 mV Added Data Retention Characteristics/Waveform and footnote # 11, 12 Added Write Cycle (WE Controlled, OE HIGH During Write) Timing Diagram Changed Package Diagram name from 44-Pin TSOP II Z44 to 44-Pin TSOP II ZS44 and from 44-Pin (400-mil) Molded SOJ V34 to 44-Pin (400-mil) Molded SOJ V44 Changed part names from Z to ZS in the Ordering Information Table Added 8 ns Product Information Added Pin-Free Ordering Information Shaded Ordering Information Table
*C	446328	NXR	See ECN	Converted from Preliminary to Final Removed -8 speed bin Removed Commercial Operating Range product information Included Automotive Operating Range product information Updated Thermal Resistance table Updated footnote #8 on High-Z parameter measurement Updated the ordering information and replaced Package Name column with Package Diagram in the Ordering Information Table

Document History Page *(continued)*

Document Title: CY7C1041DV33, 4-Mbit (256 K × 16) Static RAM				
Document Number: 38-05473				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*D	480177	VKN	See ECN	Added -10BVI product ordering code in the Ordering Information table
*E	2541850	VKN / PYRS	07/22/08	Added -10BVJXI part
*F	2752971	VKN	08/18/2009	Added Automotive-A information For 12 ns speed, changed I _{SB1} spec from 25 mA to 15 mA For 12 ns speed, changed t _{DOE} and t _{DBE} specs from 6 ns to 7 ns Updated ordering information table
*G	3034079	PRAS	09/20/2010	Added Ordering Code Definitions . Added Acronyms and Units of Measure . Minor edits
*H	3082285	HRP	11/09/2010	Corrected typo in Note 20.
*I	3149096	AJU	01/24/2011	No technical updates.
*J	3182129	HRP	03/02/2011	No technical updates
*K	3271586	PRAS	06/01/2011	Updated Features (Dislodged automotive part information to 001-69789). Updated Functional Description (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines."). Updated Selection Guide (Dislodged automotive part information to 001-69789). Updated Operating Range (Dislodged automotive part information to 001-69789). Updated DC Electrical Characteristics (Dislodged automotive part information to 001-69789). Updated AC Switching Characteristics (Dislodged automotive part information to 001-69789). Updated Data Retention Characteristics (Dislodged automotive part information to 001-69789). Updated Truth Table . Updated Ordering Information (Dislodged automotive part information to 001-69789). Updated in new template.
*L	3438781	TAVA	11/15/2011	Updated package drawing specs to current revision.
*M	4170254	MEMJ	10/22/2013	Updated Package Diagrams : spec 51-85150 – Changed revision from *G to *H. spec 51-85082 – Changed revision from *D to *E. spec 51-85087 – Changed revision from *D to *E. Updated in new template.
*N	4578500	MEMJ	12/16/2014	Added related documentation hyperlink in page 1. Updated footnote 13.

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