

## General Description

The Cypress CYBLE-022001-00 is a fully certified and qualified module supporting Bluetooth® Low Energy (BLE) wireless communication. The CYBLE-022001-00 is a turnkey solution and includes onboard crystal oscillators, chip antenna, passive components, and Cypress PROc™ BLE.

The CYBLE-022001-00 supports a number of peripheral functions (ADC, timers, counters, PWM) and serial communication protocols (I<sup>2</sup>C, UART, SPI) through its programmable architecture. The CYBLE-022001-00 includes a royalty-free BLE stack compatible with Bluetooth 4.1 and provides up to 16 GPIOs in a small 10 × 10 × 1.80 mm package.

The CYBLE-022001-00 is a complete solution and an ideal fit for applications requiring BLE wireless connectivity.

### Module Description

- Module size: 10.0 mm × 10.0 mm × 1.80 mm (with shield)
- Bluetooth 4.1 single-mode module
- Industrial temperature range: –40 °C to +85 °C
- 32-bit processor (0.9 DMIPS/MHz) with single-cycle 32-bit multiply, operating at up to 48 MHz
- 128-KB flash memory
- 16-KB SRAM memory
- Watchdog timer with dedicated internal low-speed oscillator (ILO)
- Two-pin SWD for programming
- Up to 16 GPIOs configurable as open drain high/low, pull-up/pull-down, HI-Z analog, HI-Z digital, or strong output
- Certified to FCC, CE MIC, KC, and IC regulations
  - FCC ID: WAP2001
  - IC ID: 7922A-2001
  - MIC ID: 005-101007
  - KC ID: MSIP-CRM-Cyp-2001
- Bluetooth SIG 4.1 qualified
  - QDID: [67366](#)
  - Declaration ID: [D026297](#)

### Power Consumption

- TX output power: –18 dbm to +3 dbm
- Received signal strength indicator (RSSI) with 1-dB resolution
- TX current consumption of 15.6 mA (radio only, 0 dbm)
- RX current consumption of 16.4 mA (radio only)
- Low power mode support
  - Deep Sleep: 1.3 µA with watch crystal oscillator (WCO) on
  - Hibernate: 150 nA with SRAM retention
  - Stop: 60 nA with XRES wakeup

### Functional Capabilities

- Up to 15 capacitive sensors for buttons or sliders with best-in-class signal-to-noise ration (SNR) and liquid tolerance
- 12-bit, 1-Msps SAR ADC with internal reference, sample-and-hold (S/H), and channel sequencer
- Two serial communication blocks (SCBs) supporting I<sup>2</sup>C (master/slave), SPI (master/slave), or UART
- Four dedicated 16-bit timer, counter, or PWM blocks (TCPWMs)
- Programmable low voltage detect (LVD) from 1.8 V to 4.5 V
- I<sup>2</sup>S master interface
- Bluetooth Low Energy protocol stack supporting generic access profile (GAP) Central, Peripheral, Observer, or Broadcaster roles
- Switches between Central and Peripheral roles on-the-go
- Standard Bluetooth Low Energy profiles and services for interoperability
- Custom profile and service for specific use cases

### Benefits

The CYBLE-022001-00 module is provided as a turnkey solution, including all necessary hardware required to use BLE communication standards.

- Proven, qualified, and certified hardware design ready to use
- Small footprint (10 × 10 mm × 1.80 mm), perfect for space constrained applications
- Reprogrammable architecture
- Fully certified module eliminates the time needed for design, development and certification processes
- Bluetooth SIG qualified with QDID and Declaration ID
- Flexible communication protocol support
- PSoC Creator™ provides an easy-to-use integrated design environment (IDE) to configure, develop, program, and test a BLE application

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## Overview

### Module Description

The CYBLE-022001-00 module is a complete module designed to be soldered to the applications main board.

#### *Module Dimensions and Drawing*

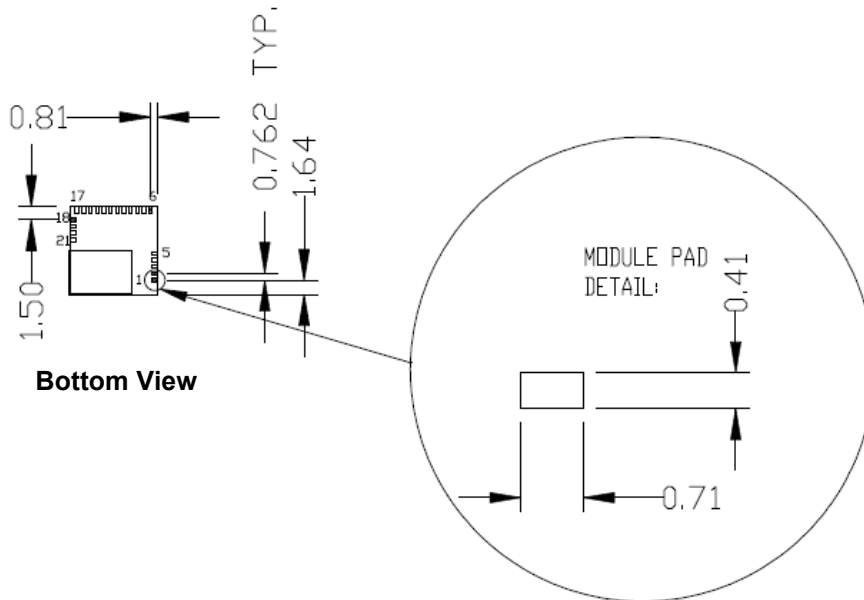
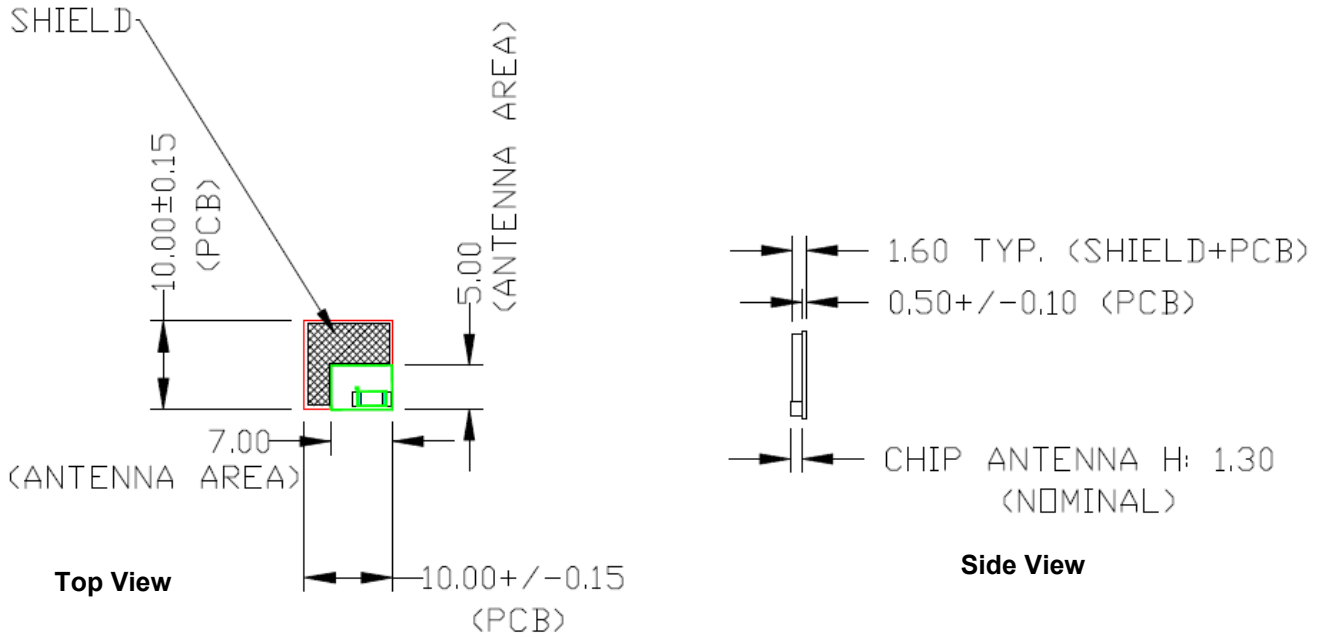
Cypress reserves the right to select components (including the appropriate BLE device) from various vendors to achieve the BLE module functionality. Such selections will still guarantee that all height restrictions of the component area are maintained. Designs should be held within the physical dimensions shown in the mechanical drawings in [Figure 1](#). All dimensions are in millimeters (mm).

**Table 1. Module Design Dimensions**

Dimension Item		Specification
Module dimensions	Length (X)	10.00 ± 0.15 mm
	Width (Y)	10.00 ± 0.15 mm
Antenna location dimensions	Length (X)	7.00 ± 0.15 mm
	Width (Y)	5.00 ± 0.15 mm
PCB thickness	Height (H)	0.50 ± 0.10 mm
Shield height	Height (H)	1.10 ± 0.10 mm
Maximum component height	Height (H)	1.30 mm typical (chip antenna)
Total module thickness (bottom of module to highest component)	Height (H)	1.80 mm typical

See [Figure 1](#) on page 4 for the mechanical reference drawing for CYBLE-022001-00.

Figure 1. Module Mechanical Drawing



- MODULE PAD ASSIGNMENT:
- PAD1:GND
  - PAD2:P4.1
  - PAD3:P5.1
  - PAD4:P5.0
  - PAD5:VDDR
  - PAD6:P1.6
  - PAD7:P0.7
  - PAD8:P0.4
  - PAD9:P0.5
  - PAD10:GND
  - PAD11:P0.6
  - PAD12:P1.7
  - PAD13:VDD
  - PAD14:XRES
  - PAD15:P3.5
  - PAD16:P3.4
  - PAD17:P3.7
  - PAD18:P1.4
  - PAD19:P1.5
  - PAD20:P3.6
  - PAD21:P1N4.0

**Note**

1. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see [Figure 3](#) and [Figure 4](#) on page 6.

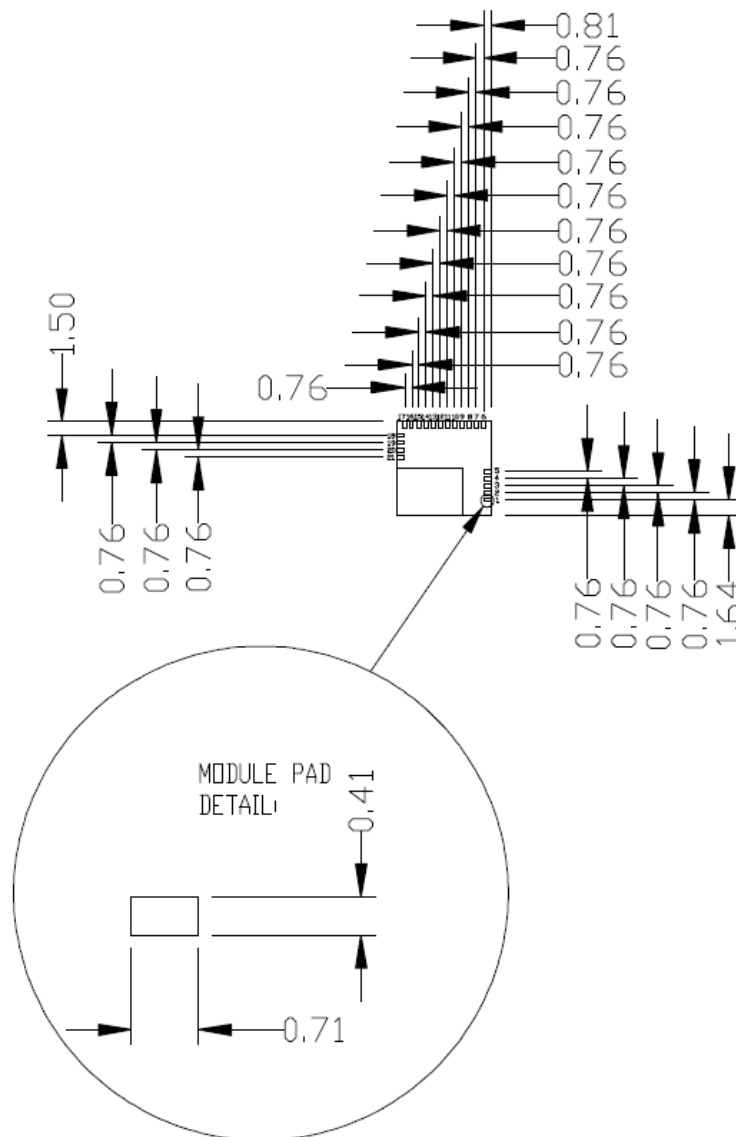
**Pad Connection Interface**

As shown in the bottom view of Figure 1 on page 4, the CYBLE-022001-00 connects to the host board via solder pads on the back of the module. Table 2 and Figure 2 detail the solder pad length, width, and pitch dimensions of the CYBLE-022001-00 module.

**Table 2. Solder Pad Connection Description**

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
SP	21	Solder Pads	0.71 mm	0.41 mm	0.76 mm

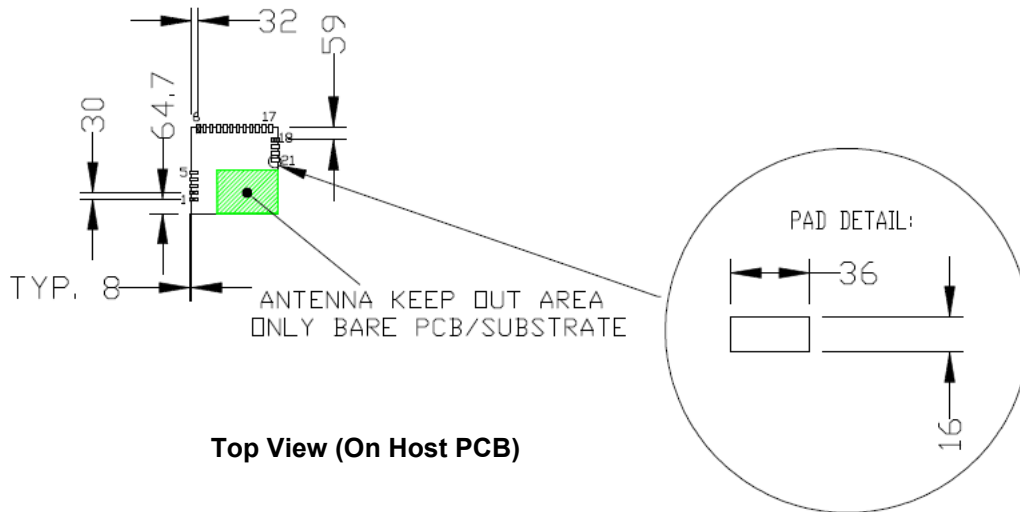
**Figure 2. Solder Pad Dimensions**



### Recommended Host PCB Layout

Figure 3 details the recommended PCB layout pattern for the host PCB. Dimensions are in mils.

Figure 3. Recommended PCB Layout Pattern for CYBLE-022001-00



To maximize RF performance, the host layout should follow these recommendations:

1. The ideal placement of the Cypress BLE module is in a corner of the host board with the chip antenna located at the far corner. This placement minimizes the additional recommended keep out area stated in item 2.
2. It is recommended that the area around the Cypress BLE module chip antenna should contain an additional keep out area, where no grounding or signal trace are contained. The keep out area applies to all layers of the host board. The recommended dimensions of the host PCB keep out area are shown in Figure 4 (dimensions are in mm).

Figure 4. Recommended Host PCB Keep Out Area Around the CYBLE-022001-00 Chip Antenna

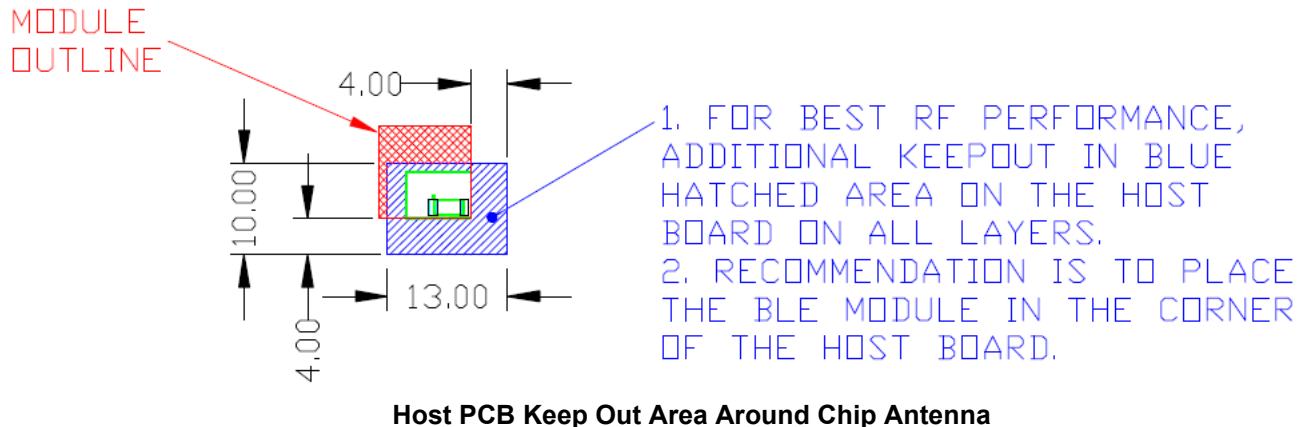


Table 3 details the solder pad pitch (center-to-center) for each of the neighboring connections.

**Table 3. Module Solder Pad Connection Dimensions**

Pad X	Pad Y	Pad Pitch (Pad X - Pad Y)	Comments
Bottom Right Corner	1	1.64 mm	Distance from bottom right corner to Pad 1 center
1	2	0.76 mm	Distance from Pad 1 center to Pad 2 center
2	3	0.76 mm	Distance from Pad 2 center to Pad 3 center
3	4	0.76 mm	Distance from Pad 3 center to Pad 4 center
4	5	0.76 mm	Distance from Pad 4 center to Pad 5 center
Top Right Corner	6	0.81 mm	Distance from top right corner to Pad 6 center
6	7	0.76 mm	Distance from Pad 6 center to Pad 7 center
7	8	0.76 mm	Distance from Pad 7 center to Pad 8 center
8	9	0.76 mm	Distance from Pad 8 center to Pad 9 center
9	10	0.76 mm	Distance from Pad 9 center to Pad 10 center
10	11	0.76 mm	Distance from Pad 10 center to Pad 11 center
11	12	0.76 mm	Distance from Pad 11 center to Pad 12 center
12	13	0.76 mm	Distance from Pad 12 center to Pad 13 center
13	14	0.76 mm	Distance from Pad 13 center to Pad 14 center
14	15	0.76 mm	Distance from Pad 14 center to Pad 15 center
15	16	0.76 mm	Distance from Pad 15 center to Pad 16 center
16	17	0.76 mm	Distance from Pad 16 center to Pad 17 center
Top Left Corner	18	1.50 mm	Distance from top left corner to Pad 18 center
18	19	0.76 mm	Distance from Pad 18 center to Pad 19 center
19	20	0.76 mm	Distance from Pad 19 center to Pad 20 center
20	21	0.76 mm	Distance from Pad 20 center to Pad 21 center

Table 4 details the solder pad connection definitions and available functions for each connection pad. Table 4 lists the solder pads on CYBLE-022001-00, the BLE device port-pin, and denotes whether the function shown is available for each solder pad. Each connection is configurable for a single option shown with a ✓.

**Table 4. Solder Pad Connection Definitions**

Solder Pad Number	Device Port Pin	UART	SPI	I <sup>2</sup> C	TCPWM <sup>[2]</sup>	CapSense	WCOOut	ECO_OUT	LCD	SWD	GPIO
1	GND <sup>[3]</sup>	Ground Connection									
2	P4.1 <sup>[4]</sup>	✓(CTS)	✓(MISO)		✓	✓(Sensor / C <sub>TANK</sub> )	–	–	✓	–	✓
3	P5.1	✓(TX)	✓(SCLK)	✓(SCL)	✓	✓(Sensor)	–	✓	✓	–	✓
4	P5.0	✓(RX)	✓(SS)	✓(SDA)	✓	✓(Sensor)	–	–	✓	–	✓
5	V <sub>DDR</sub>	Radio Power Supply (1.9V to 5.5V)									
6	P1.6	✓(RTS)	✓(SS)	–	✓	✓(Sensor)	–	–	✓	–	✓
7	P0.7	✓(CTS)	✓(SCLK)	–	✓	✓(Sensor)	–	–	✓	✓(SWDCLK)	✓
8	P0.4	✓(RX)	✓(MOSI)	✓(SDA)	✓	✓(Sensor)	–	✓	✓	–	✓
9	P0.5	✓(TX)	✓(MISO)	✓(SCL)	✓	✓(Sensor)	–	–	✓	–	✓
10	GND	Ground Connection									
11	P0.6	✓(RTS)	✓(SS)	–	✓	✓(Sensor)	–	–	✓	✓(SWDIO)	✓
12	P1.7	✓(CTS)	✓(SCLK)	–	✓	✓(Sensor)	–	–	✓	–	✓
13	V <sub>DD</sub>	Digital Power Supply Input (1.71 to 5.5V)									
14	XRES	External Reset Hardware Connection Input									
15	P3.5	✓(TX)	–	✓(SCL)	✓	✓(Sensor)	–	–	✓	–	✓
16	P3.4	✓(RX)	–	✓(SDA)	✓	✓(Sensor)	–	–	✓	–	✓
17	P3.7	✓(CTS)	✓(MISO)	–	–	✓(Sensor)	✓	–	✓	–	✓
18	P1.4	✓(RX)	✓(MOSI)	✓(SDA)	✓	✓(Sensor)	–	–	✓	–	✓
19	P1.5	✓(TX)	✓(MISO)	✓(SCL)	✓	✓(Sensor)	–	–	✓	–	✓
20	P3.6	✓(RTS)	–	–	✓	✓(Sensor)	–	–	✓	–	✓
21	P4.0 <sup>[5]</sup>	✓(RTS)	–	–	✓	✓(C <sub>MOD</sub> )	–	–	✓	–	✓

**Notes**

- TCPWM stands for timer, counter, and PWM. If supported, the pad can be configured to any of these peripheral functions.
- The main board needs to connect both GND connections (Pad 1 and Pad 10) on the module to the common ground of the system.
- When using the capacitive sensing functionality, Pad 2 (P4.1) can be connected to a C<sub>TANK</sub> capacitor (located off of Cypress BLE Module). C<sub>TANK</sub> should be used if implementing a shield layer on the capacitive sensor. If used, this capacitor should be placed as close to the module as possible.
- When using the capacitive sensing functionality, Pad 21 (P4.0) must be connected to a C<sub>MOD</sub> capacitor (located off of Cypress BLE Module). The value of this capacitor is 2.2 nF and should be placed as close to the module as possible.
- If the I<sup>2</sup>S feature is used in the design, the I<sup>2</sup>S pins shall be dynamically routed to the appropriate available GPIO by PSoC Creator.



## Power Supply Connections and Recommended External Components

### Power Connections

The CYBLE-022001-00 contains two power supply connections, VDD and VDDR. The VDD connection supplies power for both digital and analog device operation. The VDDR connection supplies power for the device radio.

VDD accepts a supply range of 1.8 V to 5.5 V. VDDR accepts a supply range of 1.9 V to 5.5 V. These specifications can be found in [Table 9](#). The maximum power supply ripple for both power connections on the module is 100 mV, as shown in [Table 7](#).

The power supply ramp rate of VDD must be equal to or greater than that of VDDR.

### Connection Options

Two connection options are available for any application:

1. Single supply: Connect VDD and VDDR to the same supply.
2. Independent supply: Power VDD and VDDR separately.

### External Component Recommendation

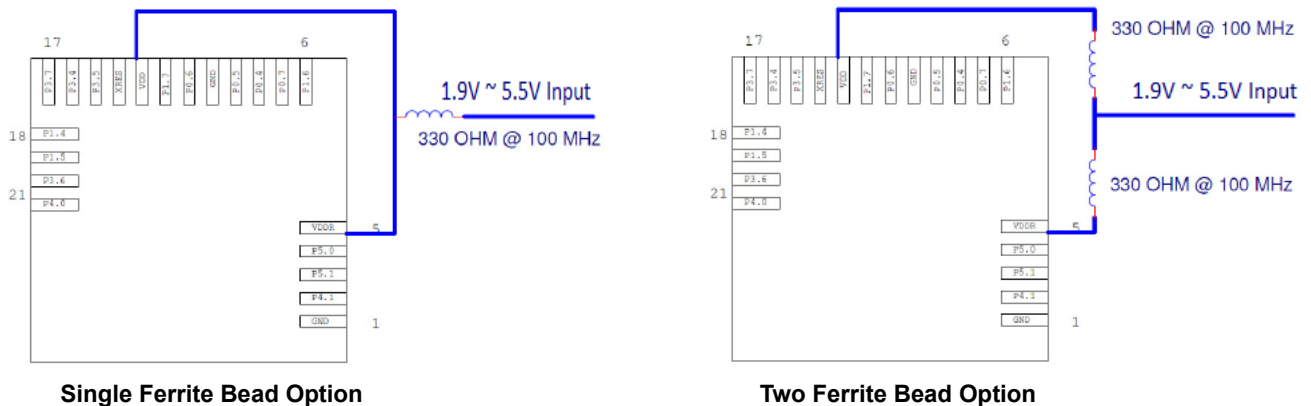
In either connection scenario, it is recommended to place an external ferrite bead between the supply and the module connection. The ferrite bead should be positioned as close as possible to the module pin connection.

[Figure 5](#) details the recommended host schematic options for a single supply scenario. The use of one or two ferrite beads will depend on the specific application and configuration of the CYBLE-022001-00.

[Figure 6](#) details the recommended host schematic for an independent supply scenario.

The recommended ferrite bead value is 330 Ω, 100 MHz. (Murata BLM21PG331SN1D).

**Figure 5. Recommended Host Schematic Options for a Single Supply Option**



**Figure 6. Recommended Host Schematic for Independent Supply Option**

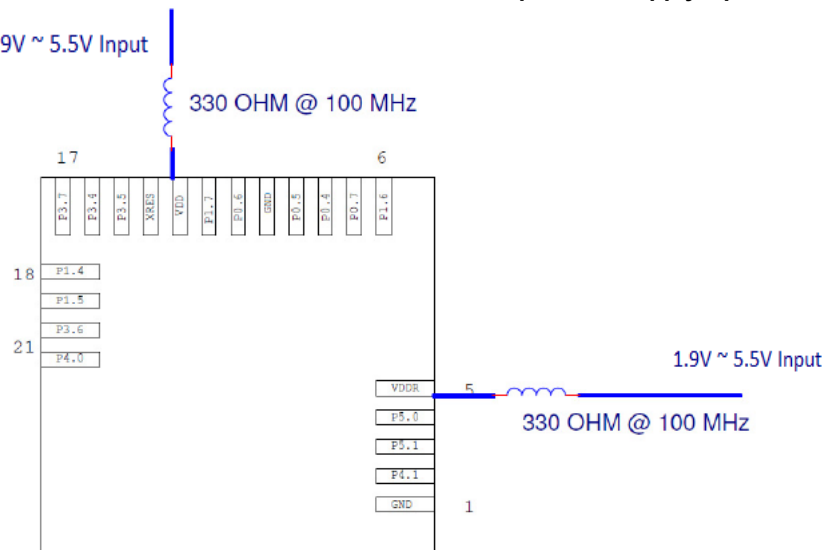
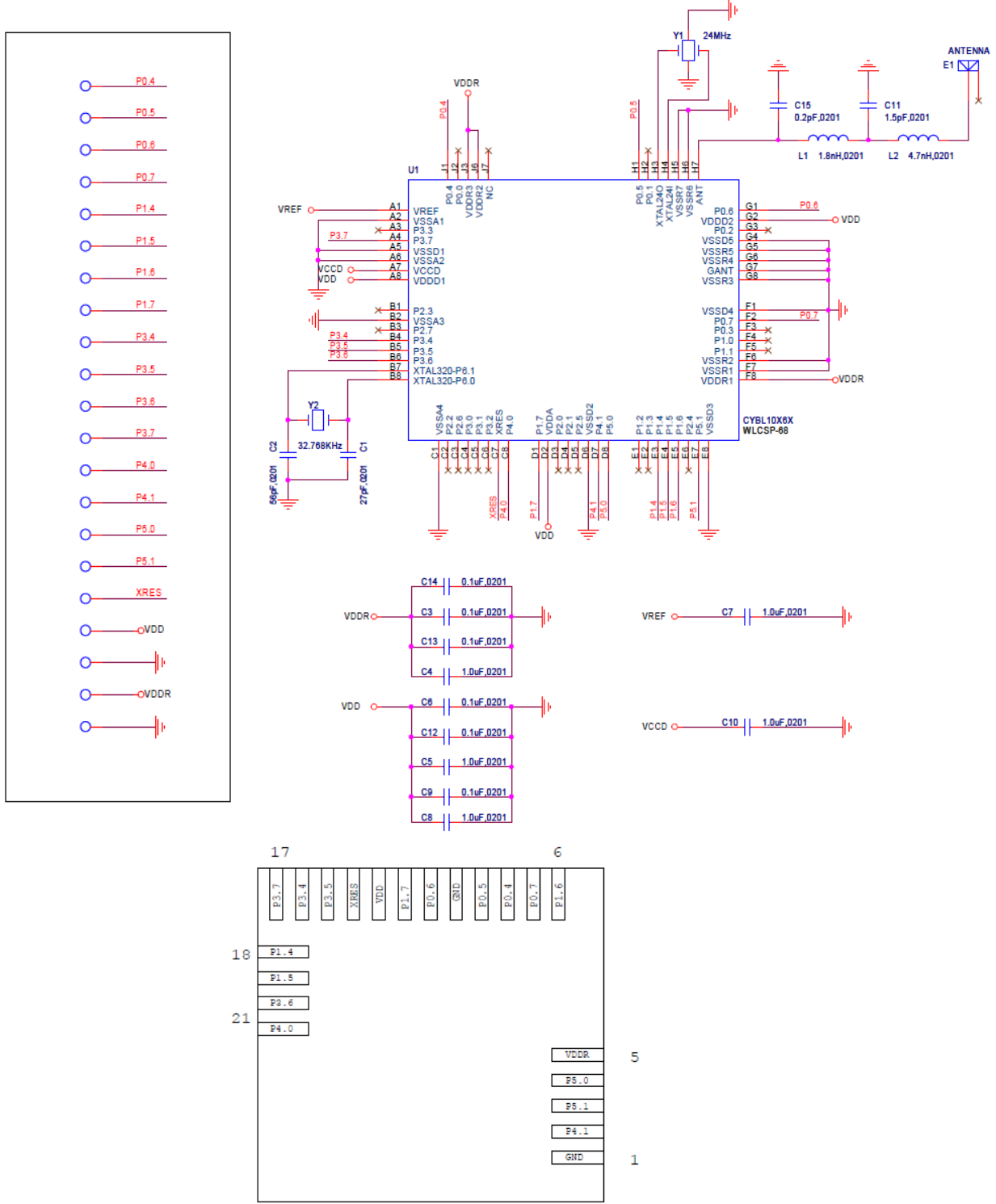


Figure 7 shows the CYBLE-022001-00 schematic.

Figure 7. CYBLE-022001-00 Schematic Diagram



## Critical Components List

Table 5 details the critical components used in the CYBLE-022001-00 module.

**Table 5. Critical Component List**

Component	Reference Designator	Description
Silicon	U1	68-pin WLCSP Programmable Radio-on-Chip (PRoC) with BLE
Crystal	Y1	24.000 MHz, 10PF
Crystal	Y2	32.768 kHz, 12.5PF
Antenna	E1	2.4 – 2.5 GHz chip antenna

## Antenna Design

Table 6 details the chip antenna used in the CYBLE-022001-00 module. The specifications listed are according to the vendor's datasheet. The Cypress module performance improves many of these characteristics. For more information, see Table 8.

**Table 6. Chip Antenna Specifications**

Item	Description
Chip Antenna Manufacturer	Johanson Technology Inc.
Chip Antenna Part Number	2450AT18B100
Frequency Range	2400 – 2500 MHz
Peak Gain	0.5 dBi typical
Average Gain	-0.5 dBi typical
Return Loss	9.5 dB minimum

## Electrical Specification

Table 7 details the absolute maximum electrical characteristics for the Cypress BLE module.

**Table 7. CYBLE-022001-00 Absolute Maximum Ratings**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>DDD_ABS</sub>	Analog, digital, or radio supply relative to V <sub>SS</sub> (V <sub>SSD</sub> = V <sub>SSA</sub> )	-0.5	-	6	V	Absolute maximum
V <sub>CCD_ABS</sub>	Direct digital core voltage input relative to V <sub>SSD</sub>	-0.5	-	1.95	V	Absolute maximum
V <sub>DDD_RIPPLE</sub>	Maximum power supply ripple for V <sub>DD</sub> and V <sub>DDR</sub> input voltage	-	-	100	mV	3.0V supply Ripple frequency of 100 kHz to 750 kHz
V <sub>GPIO_ABS</sub>	GPIO voltage	-0.5	-	V <sub>DD</sub> + 0.5	V	Absolute maximum
I <sub>GPIO_ABS</sub>	Maximum current per GPIO	-25	-	25	mA	Absolute maximum
I <sub>GPIO_injection</sub>	GPIO injection current: Maximum for V <sub>IH</sub> > V <sub>DD</sub> and minimum for V <sub>IL</sub> < V <sub>SS</sub>	-0.5	-	0.5	mA	Absolute maximum current injected per pin
LU	Pin current for latch up	-200	-	200	mA	-

Table 8 details the RF characteristics for the Cypress BLE module.

**Table 8. CYBLE-022001-00 RF Performance Characteristics**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
RF <sub>O</sub>	RF output power on ANT	-18	0	3	dBm	Configurable via register settings
RX <sub>S</sub>	RF receive sensitivity on ANT	-	-91	-	dBm	Guaranteed by design simulation; High Gain Mode
F <sub>R</sub>	Module frequency range	2400	-	2480	MHz	-
G <sub>P</sub>	Peak gain	-	0.5	-	dBi	-
G <sub>Avg</sub>	Average gain	-	-0.5	-	dBi	-
RL	Return loss	-	-10.5	-	dB	-

Table 9 through Table 37 list the module level electrical characteristics for the CYBLE-022001-00. All specifications are valid for -40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

**Table 9. CYBLE-022001-00 DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>DD1</sub>	Power supply input voltage	1.8	-	5.5	V	With regulator enabled
V <sub>DD2</sub>	Power supply input voltage unregulated	1.71	1.8	1.89	V	Internally unregulated supply
V <sub>DDR1</sub>	Radio supply voltage (radio on)	1.9	-	5.5	V	-
V <sub>DDR2</sub>	Radio supply voltage (radio off)	1.71	-	5.5	V	-
<b>Active Mode, V<sub>DD</sub> = 1.71 V to 5.5 V</b>						
I <sub>DD3</sub>	Execute from flash; CPU at 3 MHz	-	1.7	-	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD4</sub>	Execute from flash; CPU at 3 MHz	-	-	-	mA	T = -40 °C to 85 °C
I <sub>DD5</sub>	Execute from flash; CPU at 6 MHz	-	2.5	-	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD6</sub>	Execute from flash; CPU at 6 MHz	-	-	-	mA	T = -40 °C to 85 °C
I <sub>DD7</sub>	Execute from flash; CPU at 12 MHz	-	4	-	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V

**Table 9. CYBLE-022001-00 DC Specifications (continued)**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>DD8</sub>	Execute from flash; CPU at 12 MHz	–	–	–	mA	T = –40 °C to 85 °C
I <sub>DD9</sub>	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD10</sub>	Execute from flash; CPU at 24 MHz	–	–	–	mA	T = –40 °C to 85 °C
I <sub>DD11</sub>	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD12</sub>	Execute from flash; CPU at 48 MHz	–	–	–	mA	T = –40 °C to 85 °C
<b>Sleep Mode, V<sub>DD</sub> = 1.8 to 5.5 V</b>						
I <sub>DD13</sub>	IMO on	–	–	–	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V, SYSCLK = 3 MHz
<b>Sleep Mode, V<sub>DD</sub> and V<sub>DDR</sub> = 1.9 to 5.5 V</b>						
I <sub>DD14</sub>	ECO on	–	–	–	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V, SYSCLK = 3 MHz
<b>Deep-Sleep Mode, V<sub>DD</sub> = 1.8 to 3.6 V</b>						
I <sub>DD15</sub>	WDT with WCO on	–	1.5	–	μA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD16</sub>	WDT with WCO on	–	–	–	μA	T = –40 °C to 85 °C
I <sub>DD17</sub>	WDT with WCO on	–	–	–	μA	T = 25 °C, V <sub>DD</sub> = 5 V
I <sub>DD18</sub>	WDT with WCO on	–	–	–	μA	T = –40 °C to 85 °C
<b>Deep-Sleep Mode, V<sub>DD</sub> = 1.71 to 1.89 V (Regulator Bypassed)</b>						
I <sub>DD19</sub>	WDT with WCO on	–	–	–	μA	T = 25 °C
I <sub>DD20</sub>	WDT with WCO on	–	–	–	μA	T = –40 °C to 85 °C
<b>Hibernate Mode, V<sub>DD</sub> = 1.8 to 3.6 V</b>						
I <sub>DD27</sub>	GPIO and reset active	–	150	–	nA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD28</sub>	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
<b>Hibernate Mode, V<sub>DD</sub> = 3.6 to 5.5 V</b>						
I <sub>DD29</sub>	GPIO and reset active	–	–	–	nA	T = 25 °C, V <sub>DD</sub> = 5 V
I <sub>DD30</sub>	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
<b>Stop Mode, V<sub>DD</sub> = 1.8 to 3.6 V</b>						
I <sub>DD33</sub>	Stop-mode current (V <sub>DD</sub> )	–	20	–	nA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD34</sub>	Stop-mode current (V <sub>DDR</sub> )	–	40	–	nA	T = 25 °C, V <sub>DDR</sub> = 3.3 V
I <sub>DD35</sub>	Stop-mode current (V <sub>DD</sub> )	–	–	–	nA	T = –40 °C to 85 °C
I <sub>DD36</sub>	Stop-mode current (V <sub>DDR</sub> )	–	–	–	nA	T = –40 °C to 85 °C, V <sub>DDR</sub> = 1.9 V to 3.6 V
<b>Stop Mode, V<sub>DD</sub> = 3.6 to 5.5 V</b>						
I <sub>DD37</sub>	Stop-mode current (V <sub>DD</sub> )	–	–	–	nA	T = 25 °C, V <sub>DD</sub> = 5 V
I <sub>DD38</sub>	Stop-mode current (V <sub>DDR</sub> )	–	–	–	nA	T = 25 °C, V <sub>DDR</sub> = 5 V
I <sub>DD39</sub>	Stop-mode current (V <sub>DD</sub> )	–	–	–	nA	T = –40 °C to 85 °C
I <sub>DD40</sub>	Stop-mode current (V <sub>DDR</sub> )	–	–	–	nA	T = –40 °C to 85 °C

**Table 10. AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>CPU</sub>	CPU frequency	DC	–	48	MHz	1.71 V ≤ V <sub>DD</sub> ≤ 5.5 V
T <sub>SLEEP</sub>	Wakeup from Sleep mode	–	0	–	μs	Guaranteed by characterization
T <sub>DEEPSLEEP</sub>	Wakeup from Deep-Sleep mode	–	–	25	μs	24-MHz IMO. Guaranteed by characterization
T <sub>HIBERNATE</sub>	Wakeup from Hibernate mode	–	–	2	ms	Guaranteed by characterization
T <sub>STOP</sub>	Wakeup from Stop mode	–	–	2	ms	XRES wakeup

**GPIO**
**Table 11. GPIO DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>IH</sub> <sup>[7]</sup>	Input voltage HIGH threshold	0.7 × V <sub>DD</sub>	–	–	V	CMOS input
	LVTTL input, V <sub>DD</sub> < 2.7 V	0.7 × V <sub>DD</sub>	–	–	V	–
	LVTTL input, V <sub>DD</sub> ≥ 2.7 V	2.0	–	–	V	–
V <sub>IL</sub>	Input voltage LOW threshold	–	–	0.3 × V <sub>DD</sub>	V	CMOS input
	LVTTL input, V <sub>DD</sub> < 2.7 V	–	–	0.3 × V <sub>DD</sub>	V	–
	LVTTL input, V <sub>DD</sub> ≥ 2.7 V	–	–	0.8	V	–
V <sub>OH</sub>	Output voltage HIGH level	V <sub>DD</sub> – 0.6	–	–	V	I <sub>OH</sub> = 4 mA at 3.3-V V <sub>DD</sub>
	Output voltage HIGH level	V <sub>DD</sub> – 0.5	–	–	V	I <sub>OH</sub> = 1 mA at 1.8-V V <sub>DD</sub>
V <sub>OL</sub>	Output voltage LOW level	–	–	0.6	V	I <sub>OL</sub> = 8 mA at 3.3-V V <sub>DD</sub>
	Output voltage LOW level	–	–	0.6	V	I <sub>OL</sub> = 4 mA at 1.8-V V <sub>DD</sub>
	Output voltage LOW level	–	–	0.4	V	I <sub>OL</sub> = 3 mA at 3.3-V V <sub>DD</sub>
R <sub>PULLUP</sub>	Pull-up resistor	3.5	5.6	8.5	kΩ	–
R <sub>PULLDOWN</sub>	Pull-down resistor	3.5	5.6	8.5	kΩ	–
I <sub>IL</sub>	Input leakage current (absolute value)	–	–	2	nA	25 °C, V <sub>DD</sub> = 3.3 V
I <sub>IL_CTBM</sub>	Input leakage on CTBm input pins	–	–	4	nA	–
C <sub>IN</sub>	Input capacitance	–	–	7	pF	–
V <sub>HYSTTL</sub>	Input hysteresis LVTTL	25	40	–	mV	V <sub>DD</sub> > 2.7 V
V <sub>HYSMOS</sub>	Input hysteresis CMOS	0.05 × V <sub>DD</sub>	–	–	1	–
I <sub>DIODE</sub>	Current through protection diode to V <sub>DD</sub> /V <sub>SS</sub>	–	–	100	μA	–
I <sub>TOT_GPIO</sub>	Maximum total source or sink chip current	–	–	200	mA	–

**Note**

 7. V<sub>IH</sub> must not exceed V<sub>DD</sub> + 0.2 V.

**Table 12. GPIO AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>RISEF</sub>	Rise time in Fast-Strong mode	2	–	12	ns	3.3-V V <sub>DD</sub> , C <sub>LOAD</sub> = 25 pF
T <sub>FALLF</sub>	Fall time in Fast-Strong mode	2	–	12	ns	3.3-V V <sub>DD</sub> , C <sub>LOAD</sub> = 25 pF
T <sub>RISES</sub>	Rise time in Slow-Strong mode	10	–	60	ns	3.3-V V <sub>DD</sub> , C <sub>LOAD</sub> = 25 pF
T <sub>FALLS</sub>	Fall time in Slow-Strong mode	10	–	60	ns	3.3-V V <sub>DD</sub> , C <sub>LOAD</sub> = 25 pF
F <sub>GPIOOUT1</sub>	GPIO F <sub>OUT</sub> ; 3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V Fast-Strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
F <sub>GPIOOUT2</sub>	GPIO F <sub>OUT</sub> ; 1.7 V ≤ V <sub>DD</sub> ≤ 3.3 V Fast-Strong mode	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
F <sub>GPIOOUT3</sub>	GPIO F <sub>OUT</sub> ; 3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V Slow-Strong mode	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
F <sub>GPIOOUT4</sub>	GPIO F <sub>OUT</sub> ; 1.7 V ≤ V <sub>DD</sub> ≤ 3.3 V Slow-Strong mode	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
F <sub>GPIOIN</sub>	GPIO input operating frequency 1.71 V ≤ V <sub>DD</sub> ≤ 5.5 V	–	–	48	MHz	90/10% V <sub>IO</sub>

**Table 13. OVT GPIO DC Specifications (P5\_0 and P5\_1 Only)**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>IL</sub>	Input leakage (absolute value). V <sub>IH</sub> > V <sub>DD</sub>	–	–	10	μA	25°C, V <sub>DD</sub> = 0 V, V <sub>IH</sub> = 3.0 V
V <sub>OL</sub>	Output voltage LOW level	–	–	0.4	V	I <sub>OL</sub> = 20 mA, V <sub>DD</sub> > 2.9 V

**Table 14. OVT GPIO AC Specifications (P5\_0 and P5\_1 Only)**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>RISE_OVFS</sub>	Output rise time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V <sub>DD</sub> =3.3 V
T <sub>FALL_OVFS</sub>	Output fall time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V <sub>DD</sub> =3.3 V
T <sub>RISESS</sub>	Output rise time in Slow-Strong mode	10	–	60	ns	25 pF load, 10%-90%, V <sub>DD</sub> = 3.3 V
T <sub>FALLSS</sub>	Output fall time in Slow-Strong mode	10	–	60	ns	25 pF load, 10%-90%, V <sub>DD</sub> = 3.3 V
F <sub>GPIOOUT1</sub>	GPIO F <sub>OUT</sub> ; 3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V Fast-Strong mode	–	–	24	MHz	90/10%, 25 pF load, 60/40 duty cycle
F <sub>GPIOOUT2</sub>	GPIO F <sub>OUT</sub> ; 1.71 V ≤ V <sub>DD</sub> ≤ 3.3 V Fast-Strong mode	–	–	16	MHz	90/10%, 25 pF load, 60/40 duty cycle

## XRES

**Table 15. XRES DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>IH</sub>	Input voltage HIGH threshold	0.7 × V <sub>DD</sub>	–	–	V	CMOS input
V <sub>IL</sub>	Input voltage LOW threshold	–	–	0.3 × V <sub>DD</sub>	V	CMOS input
R <sub>PULLUP</sub>	Pull-up resistor	3.5	5.6	8.5	kΩ	–
C <sub>IN</sub>	Input capacitance	–	3	–	pF	–
V <sub>HYSXRES</sub>	Input voltage hysteresis	–	100	–	mV	–
I <sub>DIODE</sub>	Current through protection diode to V <sub>DD</sub> /V <sub>SS</sub>	–	–	100	μA	–

**Table 16. XRES AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>RESETWIDTH</sub>	Reset pulse width	1	–	–	μs	–

**Serial Communication**
**Table 17. I<sup>2</sup>C DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>I2C1</sub>	Block current consumption at 100 kHz	–	–	10.5	μA	–
I <sub>I2C2</sub>	Block current consumption at 400 kHz	–	–	135	μA	–
I <sub>I2C3</sub>	Block current consumption at 1 Mbps	–	–	310	μA	–
I <sub>I2C4</sub>	I <sup>2</sup> C enabled in Deep-Sleep mode	–	–	1.4	μA	–

**Table 18. Fixed I<sup>2</sup>C AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>I2C1</sub>	Bit rate	–	–	1	Mbps	Maximum is applicable to Port 5[0] and Port 5[1] only

**Table 19. Fixed UART DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>UART1</sub>	Block current consumption at 100 kbps	–	–	9	μA	–
I <sub>UART2</sub>	Block current consumption at 1000 kbps	–	–	312	μA	–

**Table 20. Fixed UART AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>UART</sub>	Bit rate	–	–	1	Mbps	–

**Table 21. Fixed SPI DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>SPI1</sub>	Block current consumption at 1 Mbps	–	–	360	μA	–
I <sub>SPI2</sub>	Block current consumption at 4 Mbps	–	–	560	μA	–
I <sub>SPI3</sub>	Block current consumption at 8 Mbps	–	–	600	μA	–

**Table 22. Fixed SPI AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>SPI</sub>	SPI operating frequency (master; 6x over sampling)	–	–	8	MHz	–

**Table 23. Fixed SPI Master Mode AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>DMO</sub>	MOSI valid after SCLK driving edge	–	–	18	ns	–
T <sub>DSI</sub>	MISO valid before SCLK capturing edge Full clock, late MISO sampling used	20	–	–	ns	Full clock, late MISO sampling
T <sub>HMO</sub>	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge



**Table 24. Fixed SPI Slave Mode AC Specifications**

Parameter	Description	Min	Typ	Max	Units
T <sub>DMI</sub>	MOSI valid before SCLK capturing edge	40	–	–	ns
T <sub>DSO</sub>	MISO valid after SCLK driving edge	–	–	42 + 3 × T <sub>CPU</sub>	ns
T <sub>DSO_ext</sub>	MISO Valid after SCLK driving edge in external clock mode. V <sub>DD</sub> < 3.0 V	–	–	50	ns
T <sub>HSO</sub>	Previous MISO data hold time	0	–	–	ns
T <sub>SSELSCK</sub>	SSEL valid to first SCK valid edge	100	–	–	ns

Refer to the CYBL10X6X datasheet at [www.cypress.com/?rID=99422](http://www.cypress.com/?rID=99422) for details on Analog (ADC, CapSense) and Digital (TCPWM) Peripherals DC and AC specifications.

## Memory

**Table 25. Flash DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>PE</sub>	Erase and program voltage	1.71	–	5.5	V	–
T <sub>WS48</sub>	Number of Wait states at 32–48 MHz	2	–	–		CPU execution from flash
T <sub>WS32</sub>	Number of Wait states at 16–32 MHz	1	–	–		CPU execution from flash
T <sub>WS16</sub>	Number of Wait states for 0–16 MHz	0	–	–		CPU execution from flash

**Table 26. Flash AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>ROWWRITE</sub> <sup>[8]</sup>	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
T <sub>ROWERASE</sub> <sup>[8]</sup>	Row erase time	–	–	13	ms	–
T <sub>ROWPROGRAM</sub> <sup>[8]</sup>	Row program time after erase	–	–	7	ms	–
T <sub>BULKERASE</sub> <sup>[8]</sup>	Bulk erase time (128 KB)	–	–	35	ms	–
T <sub>DEVPROG</sub> <sup>[8]</sup>	Total device program time	–	–	25	seconds	–
F <sub>END</sub>	Flash endurance	100 K	–	–	cycles	–
F <sub>RET</sub>	Flash retention. T <sub>A</sub> ≤ 55 °C, 100 K P/E cycles	20	–	–	years	–
F <sub>RET2</sub>	Flash retention. T <sub>A</sub> ≤ 85 °C, 10 K P/E cycles	10	–	–	years	–

## System Resources

### Power-on-Reset (POR)

**Table 27. POR DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>RISEIPOR</sub>	Rising trip voltage	0.80	–	1.45	V	–
V <sub>FALLIPOR</sub>	Falling trip voltage	0.75	–	1.40	V	–
V <sub>IPORHYST</sub>	Hysteresis	15	–	200	mV	–

**Table 28. POR AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>PPOR_TR</sub>	Precision power-on reset (PPOR) response time in Active and Sleep modes	–	–	1	μs	–

### Note

- It can take as much as 20 ms to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

**Table 29. Brown-Out Detect**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>FALLPPOR</sub>	BOD trip voltage in Active and Sleep modes	1.64	–	–	V	–
V <sub>FALLDPSLP</sub>	BOD trip voltage in Deep Sleep	1.4	–	–	V	–

**Table 30. Hibernate Reset**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>HBRTRIP</sub>	BOD trip voltage in Hibernate	1.1	–	–	V	–

*Voltage Monitors (LVD)*
**Table 31. Voltage Monitor DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>LVI1</sub>	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	–
V <sub>LVI2</sub>	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	–
V <sub>LVI3</sub>	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	–
V <sub>LVI4</sub>	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	–
V <sub>LVI5</sub>	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	–
V <sub>LVI6</sub>	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	–
V <sub>LVI7</sub>	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	–
V <sub>LVI8</sub>	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	–
V <sub>LVI9</sub>	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	–
V <sub>LVI10</sub>	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	–
V <sub>LVI11</sub>	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	–
V <sub>LVI12</sub>	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	–
V <sub>LVI13</sub>	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	–
V <sub>LVI14</sub>	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	–
V <sub>LVI15</sub>	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	–
V <sub>LVI16</sub>	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	–
LVI_IDD	Block current	–	–	100	μA	–

**Table 32. Voltage Monitor AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>MONTRIP</sub>	Voltage monitor trip time	–	–	1	μs	–

*SWD Interface*
**Table 33. SWD Interface Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>SWDCLK1</sub>	3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
F <sub>SWDCLK2</sub>	1.71 V ≤ V <sub>DD</sub> ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
T <sub>SWDI_SETUP</sub>	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
T <sub>SWDI_HOLD</sub>	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
T <sub>SWDO_VALID</sub>	T = 1/f SWDCLK	–	–	0.5 × T	ns	–
T <sub>SWDO_HOLD</sub>	T = 1/f SWDCLK	1	–	–	ns	–

*Internal Main Oscillator*
**Table 34. IMO DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>IMO1</sub>	IMO operating current at 48 MHz	–	–	1000	μA	–
I <sub>IMO2</sub>	IMO operating current at 24 MHz	–	–	325	μA	–
I <sub>IMO3</sub>	IMO operating current at 12 MHz	–	–	225	μA	–
I <sub>IMO4</sub>	IMO operating current at 6 MHz	–	–	180	μA	–
I <sub>IMO5</sub>	IMO operating current at 3 MHz	–	–	150	μA	–

**Table 35. IMO AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>IMOTOL3</sub>	Frequency variation from 3 to 48 MHz	–	–	±2	%	With API-called calibration
F <sub>IMOTOL3</sub>	IMO startup time	–	12	–	μs	–

*Internal Low-Speed Oscillator*
**Table 36. ILO DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>ILO2</sub>	ILO operating current at 32 kHz	–	0.3	1.05	μA	–

**Table 37. ILO AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>STARTILO1</sub>	ILO startup time	–	–	2	ms	–
F <sub>ILOTRIM1</sub>	32-kHz trimmed frequency	15	32	50	kHz	–

**Table 38. ECO Trim Value Specification**

Parameter	Description	Value	Details/Conditions
ECO <sub>TRIM</sub>	24-MHz trim value (firmware configuration)	0x00003FFA	Optimum trim value that needs to be loaded to register CY_SYS_XTAL_BLERD_BB_XO_CAPTRIM_REG

## Environmental Specifications

### Environmental Compliance

This Cypress BLE module is built in compliance with the Restriction of Hazardous Substances (RoHS) and Halogen Free (HF) directives. The Cypress module and components used to produce this module are RoHS and HF compliant.

### RF Certification

The CYBLE-022001-00 module is certified under the following RF certification standards:

- FCC: WAP2001
- CE
- IC: 7922A-2001
- MIC: 005-101007
- KC: MSIP-CRM-Cyp-2001

### Environmental Conditions

Table 39 describes the operating and storage conditions for the Cypress BLE module.

**Table 39. Environmental Conditions for CYBLE-022001-00**

Description	Minimum Specification	Maximum Specification
Operating temperature	-40 °C	85 °C
Operating humidity (relative, non-condensation)	5%	85%
Thermal ramp rate	-	3 °C/minute
Storage temperature	-40 °C	85 °C
Storage temperature and humidity	-	85 °C at 85%
ESD: Module integrated into system Components <sup>[9]</sup>	-	15 kV Air 2.2 kV Contact

### ESD and EMI Protection

Exposed components require special attention to ESD and electromagnetic interference (EMI).

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

**Device Handling:** Proper ESD protocol must be followed in manufacturing to ensure component reliability.

**Note**

9. This does not apply to the RF pins (ANT, XTALI, and XTALO). RF pins (ANT, XTALI, and XTALO) are tested for 500-V HBM.

## Regulatory Information

### FCC

#### FCC NOTICE:



The device CYBLE-022001-00, including the antenna 2450AT18B100 from Johanson Technology, complies with Part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407. transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

#### CAUTION:



The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Cypress Semiconductor may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions,ê may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

#### LABELING REQUIREMENTS:



The Original Equipment Manufacturer (OEM) must ensure that FCC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: WAP2001.

In any case the end product must be labeled exterior with "Contains FCC ID: WAP2001"

#### ANTENNA WARNING:



This device is tested with a standard SMA connector and with the antennas listed below. When integrated in the OEMs product, these fixed antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

#### RF EXPOSURE:



To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antennas in [Table 6](#) on page 11, to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYBLE-022001-00 with the chip antenna mounted (FCC ID: WAP2001) is far below the FCC radio frequency exposure limits. Nevertheless, use CYBLE-022001-00 in such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

### Industry Canada (IC) Certification

CYBLE-022001-00 is licensed to meet the regulatory requirements of Industry Canada (IC),

License: IC: 7922A-2001

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from [www.ic.gc.ca](http://www.ic.gc.ca).

This device has been designed to operate with the antennas listed in [Table 6](#) on page 11, having a maximum gain of 0.5 dBi. Antennas not included in this list or having a gain greater than 0.5 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

#### IC NOTICE:



The device CYBLE-022001-00 including the antenna 2450AT18B100 from Johanson technology, complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

#### LABELING REQUIREMENTS:



The Original Equipment Manufacturer (OEM) must ensure that IC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor IC identifier for this product as well as the IC Notice above. The IC identifier is 7922A-2001. In any case, the end product must be labeled in its exterior with "Contains IC: 7922A-2001"

### European R&TTE Declaration of Conformity

Hereby, Cypress Semiconductor declares that the Bluetooth module CYBLE-022001-00 complies with the essential requirements and other relevant provisions of Directive 1999/5/EC. As a result of the conformity assessment procedure described in Annex III of the Directive 1999/5/EC, the end-customer equipment should be labeled as follows:



All versions of the CYBLE-022001-00 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

**MIC Japan**

CYBLE-022001-00 is certified as a module with type certification number 005-101007. End products that integrate CYBLE-022001-00 do not need additional MIC Japan certification for the end product.

End product can display the certification label of the embedded module.

Model Name: EZ-BLE PRoC Module

Part Number: CYBLE-022001-00

Manufactured by Cypress Semiconductor.



**005-101007**

**KC Korea**

CYBLE-022001-00 is certified for use in Korea with certificate number MSIP-CRM-Cyp-2001.

한국 인증 세부정보:



1. 제품명(모델명): 특정소출력무선기기(무선데이터통신시스템용 무선기기), CYBLE-022001-00
2. 인증 번호: MSIP-CRM-Cyp-2001
3. 라이선스 소유자: Cypress Semiconductor Corporation
4. 제조일자: 2015.04
5. 제조업체/국가명: Cypress Semiconductor Corporation/ 중국

해당 무선설비는 전파혼신 가능성이 있으므로 인명안전과 관련된 서비스는 할 수 없습니다.

## Ordering Information

Table 40 lists the CYBLE-022001-00 part number and features.

**Table 40. Ordering Information**

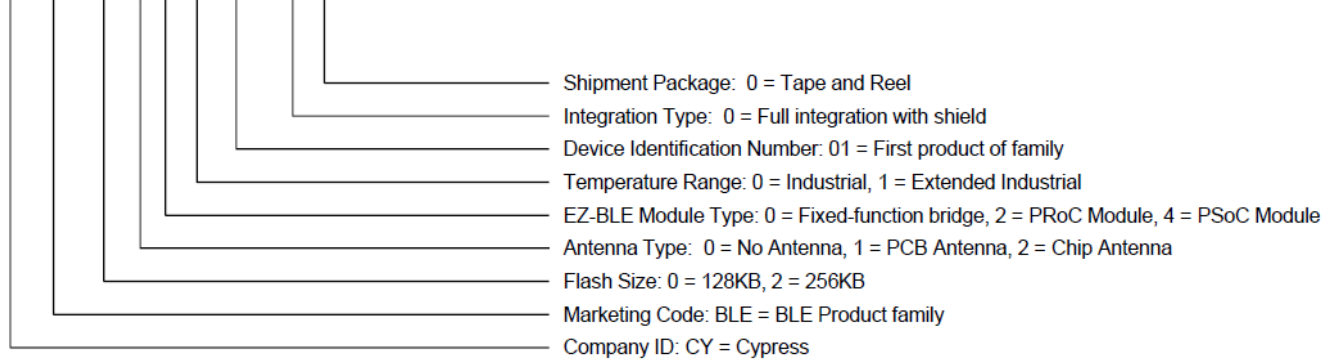
Part Number	CPU Speed (MHz)	Flash Size (KB)	CapSense	SCB	TCPWM	12-Bit SAR ADC	I <sup>2</sup> S	LCD	Package	Packaging
CYBLE-022001-00	48	128	Yes	2	4	1 Msps	Yes	Yes	21-SMT	Tape and Reel

## Ordering Code Definitions

The part numbers are of the form CYBLE-ABCDEF-GH where the fields are defined as follows.

Example

CY BLE - A B C D EF - G H



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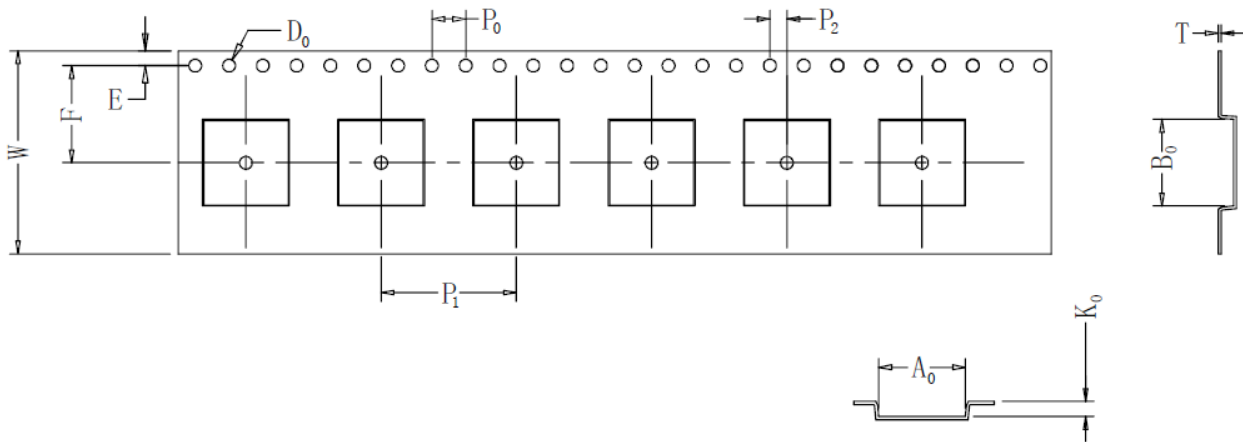


**Packaging**

The CYBLE-022001-00 is offered in tape and reel packaging. [Figure 8](#) details the tape dimensions used for the CYBLE-022001-00.

**Figure 8. CYBLE-022001-00 Tape Dimensions**

Item	W	A <sub>0</sub>	B <sub>0</sub>	K <sub>0</sub>	K <sub>1</sub>	P <sub>1</sub>	F	E	D <sub>0</sub>	D <sub>1</sub>	P <sub>0</sub>	P <sub>2</sub>	T
Measurement	24.0 <sup>+0.30</sup> <sub>-0.30</sub>	10.26 <sup>+0.10</sup> <sub>-0.10</sub>	10.26 <sup>+0.10</sup> <sub>-0.10</sub>	2.00 <sup>+0.10</sup> <sub>-0.10</sub>	<sup>+0.10</sup> <sub>-0.10</sub>	16.0 <sup>+0.10</sup> <sub>-0.10</sub>	11.5 <sup>+0.10</sup> <sub>-0.10</sub>	1.75 <sup>+0.10</sup> <sub>-0.10</sub>	1.50 <sup>+0.10</sup> <sub>-0.00</sub>	1.50 <sup>+0.10</sup> <sub>-0.10</sub>	4.00 <sup>+0.10</sup> <sub>-0.10</sub>	2.00 <sup>+0.10</sup> <sub>-0.10</sub>	0.30 <sup>+0.05</sup> <sub>-0.05</sub>



[Figure 9](#) details the orientation of the CYBLE-022001-00 in the tape as well as the direction for unreeling.

**Figure 9. Component Orientation in Tape and Unreeling Direction**

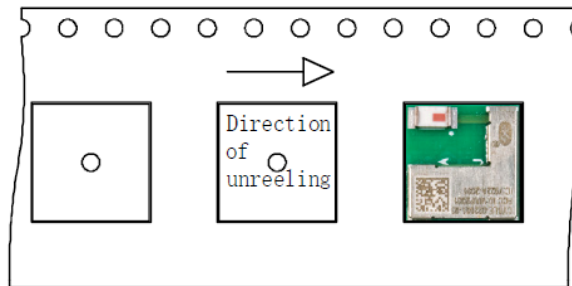
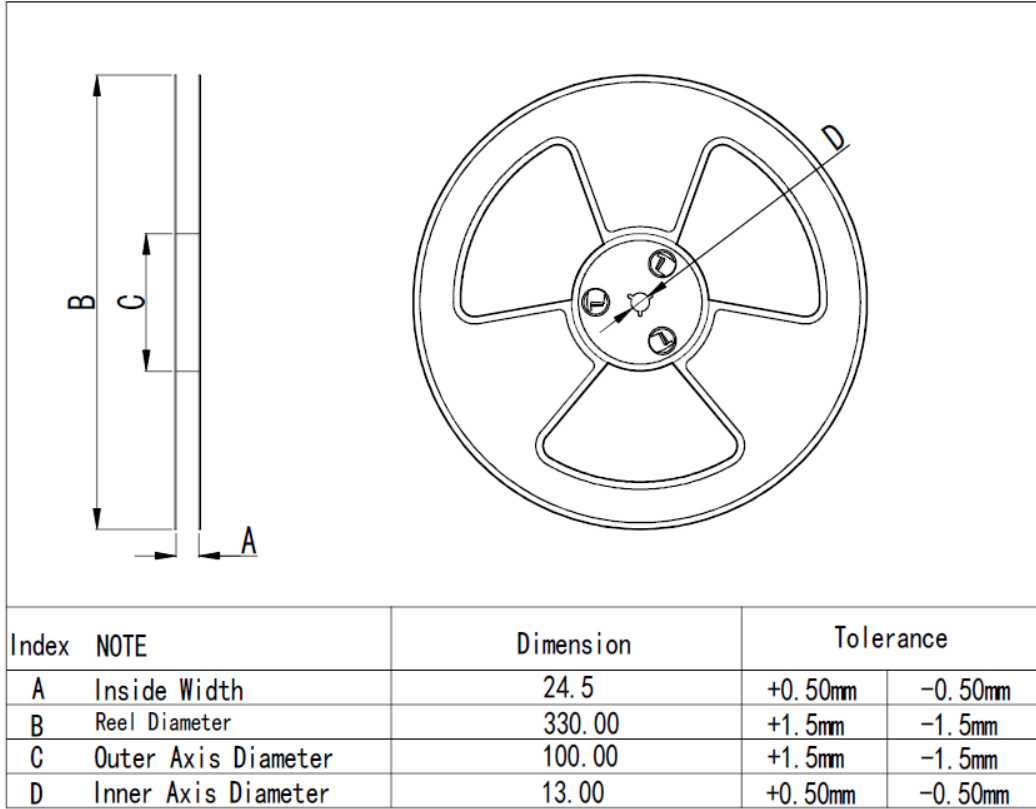


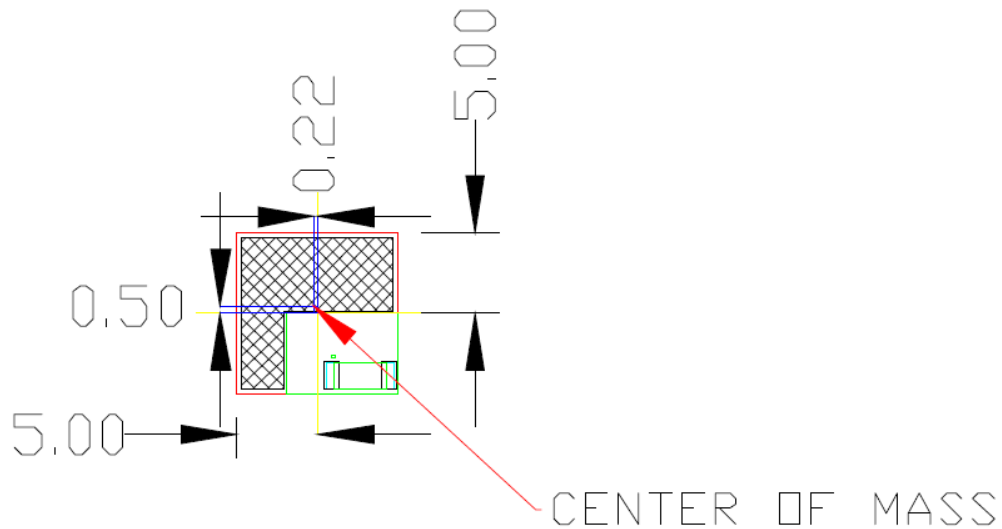
Figure 10 details reel dimensions used for the CYBLE-022001-00.

**Figure 10. Reel Dimensions**



The CYBLE-022001-00 is designed to be used with pick-and-place equipment in an SMT manufacturing environment. The center-of-mass for the CYBLE-022001-00 is detailed in Figure 11.

**Figure 11. CYBLE-022001-00 Center of Mass**



## Acronyms

Table 41. Acronyms Used in this Document

Acronym	Description
BLE	Bluetooth Low Energy
Bluetooth SIG	Bluetooth Special Interest Group
CE	European Conformity
CSA	Canadian Standards Association
EMI	electromagnetic interference
ESD	electrostatic discharge
FCC	Federal Communications Commission
GPIO	general-purpose input/output
IC	Industry Canada
IDE	integrated design environment
KC	Korea Certification
MIC	Ministry of Internal Affairs and Communications (Japan)
PCB	printed circuit board
RX	receive
QDID	qualification design ID
SMT	surface-mount technology; a method for producing electronic circuitry in which the components are placed directly onto the surface of PCBs
TCPWM	timer, counter, pulse width modulator (PWM)
TUV	Germany: Technischer Überwachungs-Verein (Technical Inspection Association)
TX	transmit

## Document Conventions

### Units of Measure

Table 42. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kV	kilovolt
mA	milliamperes
mm	millimeters
mV	millivolt
µA	microamperes
µm	micrometers
MHz	megahertz
GHz	gigahertz
V	volt

Document History Page

Document Title: CYBLE-022001-00 EZ-BLE™ PRoC™ Module Document Number: 001-95662				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4662055	DSO	02/18/2015	Preliminary datasheet for CYBLE-022001-00 module.
*A	4679323	DSO	03/09/2015	Updated Pad 10 on module pinout from NC to GND. Updated Module Pad Assignment in <a href="#">Figure 1</a> on page 4. Updated title of <a href="#">Table 3</a> to “Module Solder Pad Connection Dimensions”. Updated <a href="#">Table 4</a> to change Pad 10 from NC to GND. Updated <a href="#">Figure 5</a> , <a href="#">Figure 6</a> , and <a href="#">Figure 7</a> to update Pad 10 from NC to GND.
*B	4710754	DSO	04/01/2015	Updated Title Page heading to “EZ-BLE™ PRoC™ Module”. Updated <a href="#">Module Description</a> to correct GPIO number from “12” to “16”. Updated <a href="#">Module Description</a> to add QDID and Declaration ID under <a href="#">Bluetooth SIG 4.1 qualified</a> item. Updated <a href="#">Functional Capabilities</a> to correct number of capacitive sensors supported from nine to 13. Updated <a href="#">Power Consumption</a> Stop mode as “60 nA with XRES wakeup”. Updated terms “pre-certified” and “pre-qualified” to “certified” and “qualified” respectively. Updated <a href="#">Table 10</a> to change Details/Conditions to “XRES wakeup”. Updated <a href="#">Acronyms</a> to add “QDID”.
*C	4812402	DSO	06/26/2015	Changed document status from “Preliminary” to “Final”. Updated <a href="#">Functional Capabilities</a> to correct number of capacitive sensors supported from nine to 15. Updated <a href="#">Module Description</a> to add identification numbers for FCC, IC, KC, and MIC regulatory agencies. Updated <a href="#">Power Supply Connections and Recommended External Components</a> section to specify power supply ramp timing for VDD and VDDR. Updated <a href="#">Figure 7</a> to final design schematic. Update $IDD_{15}$ in <a href="#">Table 9</a> from 1.3 $\mu$ A to 1.5 $\mu$ A. Added <a href="#">Packaging</a> section. Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Acronyms</a> to add “SMT”.

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