

# 2.5 V or 3.3 V, 200-MHz, 1:10 Clock Distribution Buffer

#### **Features**

- 2.5 V or 3.3 V operation
- 200-MHz clock support
- Two LVCMOS-/LVTTL-compatible inputs
- Ten clock outputs: drive up to 20 clock lines
- 1× or 1/2× configurable outputs
- Output three-state control
- 250-ps max output-to-output skew
- Pin-compatible with MPC946, MPC9446
- Available in commercial and industrial temperature range
- 32-pin TQFP package

#### **Description**

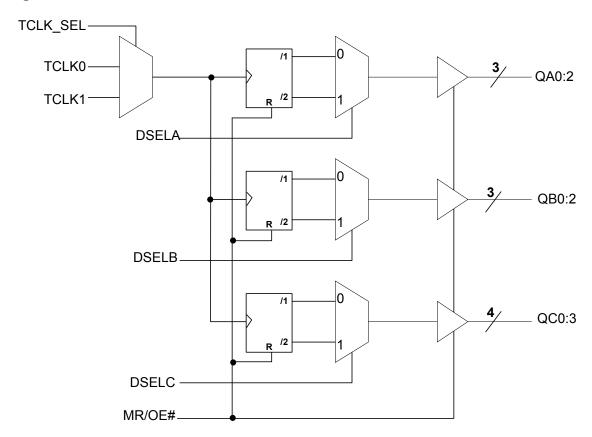
The CY29946 is a low-voltage 200-MHz clock distribution buffer with the capability to select one of two LVCMOS/LVTTL compatible input clocks. These clock sources can be used to provide for test clocks as well as the primary system clocks. All other control inputs are LVCMOS/LVTTL compatible. The 10 outputs are LVCMOS or LVTTL compatible and can drive 50  $\Omega$  series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:20.

The CY29946 is capable of generating 1× and 1/2× signals from a 1× source. These signals are generated and retimed internally to ensure minimal skew between the 1× and 1/2× signals. SEL(A:C) inputs allow flexibility in selecting the ratio of 1× to1/2× outputs.

The CY29946 outputs can also be three-stated via MR/OE# input. When MR/OE# is set HIGH, it resets the internal flip-flops and three-states the outputs.

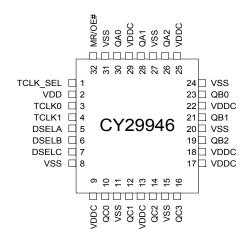
For a complete list of related documentation, click here.

### **Block Diagram**





# **Pin Configuration**



# Pin Description<sup>[1]</sup>

Pin	Name	PWR	I/O	Description
3, 4	TCLK(0,1)		I, PU	External Reference/Test Clock Input
26, 28, 30	QA(2:0)	VDDC	0	Clock Outputs
19, 21, 23	QB(2:0)	VDDC	0	Clock Outputs
10, 12, 14, 16	QC(0:3)	VDDC	0	Clock Outputs
5, 6, 7	DSEL(A:C)		I, PD	<b>Divider Select Inputs</b> . When HIGH, selects ÷2 input divider. When LOW, selects ÷1 input divider.
1	TCLK_SEL		I, PD	TCLK Select Input. When LOW, TCLK0 clock is selected and when HIGH TCLK1 is selected.
32	MR/OE#		I, PD	Output Enable Input. When asserted LOW, the outputs are enabled and when asserted HIGH, internal flip-flops are reset and the outputs are three-stated. If more than 1 Bank is being used in /2 Mode, a reset must be performed (MR/OE# Asserted High) after power-up to ensure all internal flip-flops are set to the same state.
9, 13, 17, 18, 22, 25, 29	VDDC			2.5 V or 3.3 V Power Supply for Output Clock Buffers
2	VDD			2.5 V or 3.3 V Power Supply
8, 11, 15, 20, 24, 27, 31	VSS			Common Ground

#### Note

<sup>1.</sup> PD = Internal pull-down. PU = Internal pull-up.



#### Absolute Maximum Conditions[2]

Maximum Input Voltage Relative to $V_{\mbox{\scriptsize SS}}$ .	V <sub>SS</sub> – 0.3 V
Maximum Input Voltage Relative to $V_{\mbox{\scriptsize DD}}.$	V <sub>DD</sub> + 0.3 V
Storage Temperature	–65 °C to +150 °C
Operating Temperature	–40 °C to +85 °C
Maximum ESD protection	2 kV
Maximum Power Supply	5.5 V
Maximum Input Current	±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$
.

Unused inputs must always be tied to an appropriate logic voltage level (either  $\rm V_{SS}$  or  $\rm V_{DD}).$ 

# **DC Electrical Specifications**

 $V_{DD}$  =  $V_{DDC}$  = 3.3 V ± 10% or 2.5 V ± 5%, over the specified temperature range

Parameter	Description	Conditions	Min	Тур	Max	Unit
$V_{IL}$	Input Low Voltage		V <sub>SS</sub>	_	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	_	$V_{DD}$	V
I <sub>IL</sub>	Input Low Current <sup>[3]</sup>			_	-100	μA
I <sub>IH</sub>	Input High Current <sup>[3]</sup>		1	_	100	μA
$V_{OL}$	Output Low Voltage <sup>[4]</sup>	I <sub>OL</sub> = 20 mA	1	_	0.4	V
V <sub>OH</sub>	Output High Voltage <sup>[4]</sup>	$I_{OH} = -20 \text{ mA}, V_{DD} = 3.3 \text{ V}$	2.5	_	-	V
		$I_{OH} = -20 \text{ mA}, V_{DD} = 2.5 \text{ V}$	1.8	_	_	
I <sub>DDQ</sub>	Quiescent Supply Current		1	5	7	mA
I <sub>DD</sub>	Dynamic Supply Current	V <sub>DD</sub> = 3.3 V, Outputs @ 100 MHz, CL = 30 pF	-	130	-	mA
		V <sub>DD</sub> = 3.3 V, Outputs @ 160 MHz, CL = 30 pF	1	225	_	
		V <sub>DD</sub> = 2.5 V, Outputs @ 100 MHz, CL = 30 pF	_	95	-	
		V <sub>DD</sub> = 2.5 V, Outputs @ 160 MHz, CL = 30 pF	_	160	-	
Z <sub>Out</sub>	Output Impedance	V <sub>DD</sub> = 3.3 V	12	15	18	W
		V <sub>DD</sub> = 2.5 V	14	18	22	
C <sub>in</sub>	Input Capacitance		-	4	_	pF

- Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.
   Inputs have pull-up/pull-down resistors that effect input current.
   Driving series or parallel terminated 50 Ω (or 50 Ω to V<sub>DD</sub>/2) transmission lines.



# **AC Electrical Specifications**

 $V_{DD}$  =  $V_{DDC}$  = 3.3 V ± 10% or 2.5 V ± 5%, over the specified temperature range<sup>[5]</sup>

Parameter	Description	Conditions	Min	Тур	Max	Unit
F <sub>max</sub>	Input Frequency <sup>[6]</sup>	V <sub>DD</sub> = 3.3 V	_	-	200	MHz
		V <sub>DD</sub> = 2.5 V	_	-	170	
T <sub>pd</sub>	TTL_CLK To Q Delay <sup>[6]</sup>		5.0	-	11.5	ns
F <sub>outDC</sub>	Output Duty Cycle <sup>[6, 7]</sup>	Measured at V <sub>DD</sub> /2	45	-	55	%
t <sub>pZL</sub> , t <sub>pZH</sub>	Output enable time (all outputs)		2	-	10	ns
t <sub>pLZ</sub> , t <sub>pHZ</sub>	Output disable time (all outputs)		2	_	10	ns
T <sub>skew</sub>	Output-to-Output Skew <sup>[6, 8]</sup>		_	150	250	ps
T <sub>skew(pp)</sub>	Part-to-Part Skew <sup>[9]</sup>		_	2.0	4.5	ns
$T_r/T_f$	Output Clocks Rise/Fall Time <sup>[8]</sup>	0.8 V to 2.0 V, V <sub>DD</sub> = 3.3 V	0.10	_	1.0	ns
		0.6 V to 1.8 V, V <sub>DD</sub> = 2.5 V	0.10	_	1.3	

- Notes
  Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
  Outputs driving 50Ω transmission lines.
  50% input duty cycle.
  See Figure 1 on page 5.
  Part-to-Part skew at a given temperature and voltage.



Figure 1. LVCMOS\_CLK CY29946 Test Reference for  $\rm V_{CC}$  = 3.3 V and  $\rm V_{CC}$  = 2.5 V

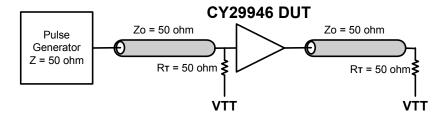


Figure 2. LVCMOS Propagation Delay (T<sub>PD</sub>) Test Reference

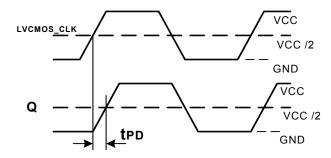


Figure 3. Output Duty Cycle (FoutDC)

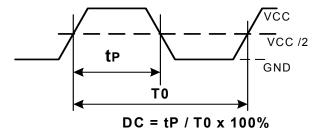
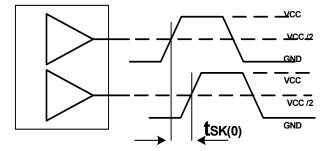


Figure 4. Output-to-Output Skew  $t_{sk(0)}$ 

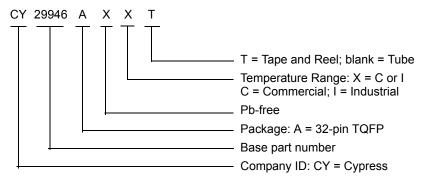




# **Ordering Information**

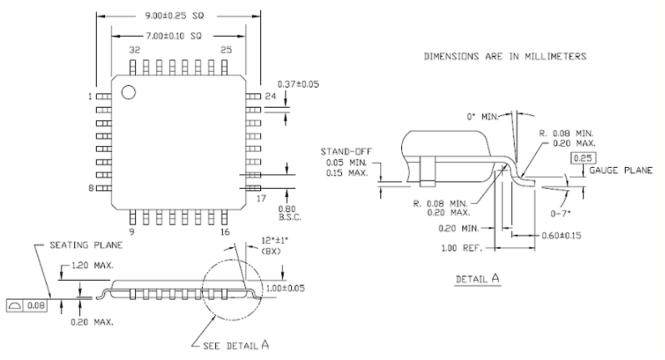
Part Number	Package Type	Production Flow
CY29946AXC	32-pin TQFP	Commercial, 0 °C to +70 °C
CY29946AXCT	32-pin TQFP – Tape and Reel	Commercial, 0 °C to +70 °C
CY29946AXI	32-pin TQFP	Industrial, –40 °C to +85 °C
CY29946AXIT	32-pin TQFP – Tape and Reel	Industrial, –40 °C to +85 °C

#### **Ordering Code Definitions**



# **Package Drawing and Dimensions**

Figure 5. 32-pin TQFP 7 × 7 × 1.0 mm A3210



51-85063 \*D



# Acronyms

Acronym	Description
ESD	electrostatic discharge
I/O	input/output
LVCMOS	low voltage complementary metal oxide semiconductor
LVTTL low-voltage transistor-transistor logic	
TQFP thin quad flat pack	

# **Document Conventions**

#### **Units of Measure**

Symbol	Unit of Measure			
°C	degree Celsius			
kV	kilo Volts			
MHz	Mega Hertz			
μA	micro Amperes			
mA	milli Amperes			
mm	milli meter			
mV	milli Volts			
ns	nano seconds			
Ω	ohms			
%	percent			
pF	pico Farad			
ps	pico seconds			
V	Volts			
W	Watts			



# **Document History Page**

Document Title: CY29946, 2.5 V or 3.3 V, 200-MHz, 1:10 Clock Distribution Buffer Document Number: 38-07286					
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change	
**	111097	02/07/02	BRK	New data sheet	
*A	116780	08/15/02	HWT	Added the commercial temperature range in the Ordering Information	
*B	122878	12/22/02	RBI	Added power-up requirements to Maximum Ratings	
*C	130007	10/15/03	RGL Fixed the block diagram. Fixed the MK/OE# description in the pin description table.		
*D	131375	11/21/03	RGL Updated document history page (revision *C) to reflect changes the not listed.		
*E	221587	See ECN	RGL	Minor Change: Moved up the word Block Diagram in the first page.	
*F	2899714	03/26/10	BRIJ/CXQ	Removed inactive parts from the ordering table. Updated package diagram	
*G	3254185	05/11/2011	CXQ	Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated in new template.	
*H	4389717	05/30/2014	XHT	Sunset Review. Changed package revision *C to *D	
*	4586288	12/03/2014	XHT	Added related documentation hyperlink in page 1.	



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