CY7C144E

8 K × 8 Dual-port Static RAM with SEM, INT, BUSY

Features

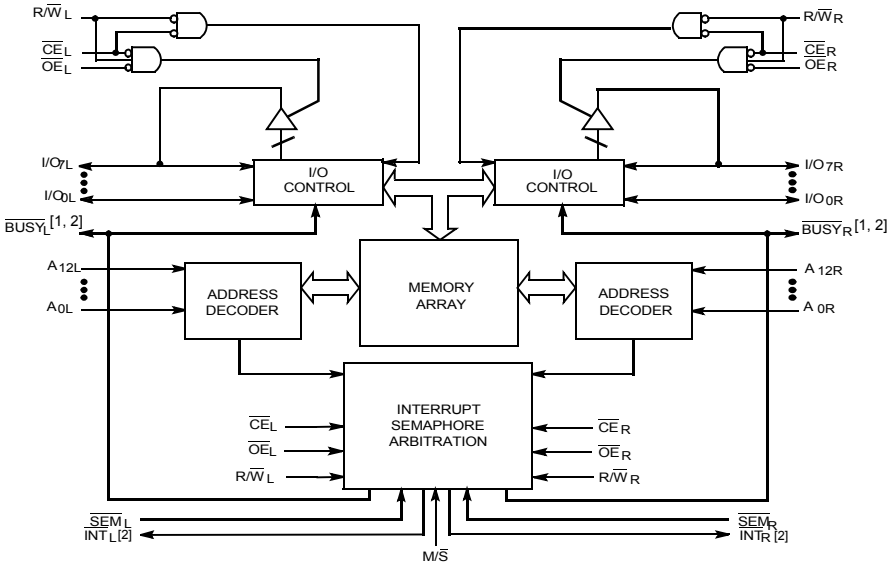
- True dual-ported memory cells that enable simultaneous reads of the same memory location
- 8 K × 8 organization (CY7C144E)
- 0.35-micron CMOS for optimum speed and power
- High-speed access: 15 ns
- Low operating power: I_{CC} = 180 mA (typical), standby ISB3 = 0.05 mA (typical)
- Fully asynchronous operation
- Automatic power-down
- TTL compatible
- Master / slave select pin enables bus width expansion to 16-bits or more
- Busy arbitration scheme provided
- Semaphores included to permit software handshaking between ports
- $\overline{INT}$ flag for port-to-port communication
- Available in 68-pin PLCC and 64-pin TQFP
- Pb-free packages available

Functional Description

The CY7C144E is a high speed CMOS 8 K × 8 dual port static RAM. Various arbitration schemes are included on the CY7C144E to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7C144E can be used as a standalone 64-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16-bit or wider master / slave dual-port static RAM. An M/S pin is provided for implementing 16-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor / multiprocessor designs, communications status buffering, and dual-port video / graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable (R/W), and output enable ($\overline{OE}$). Two flags, $\overline{BUSY}$ and $\overline{INT}$, are provided on each port. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin.
For a complete list of related documentation, click here.

Logic Block Diagram



Notes
1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.
2. Interrupt: push-pull output and requires no pull-up resistor.

Contents

Table 1. Selection Guide

Description	7C144E-15	7C144E-25	7C144E-55	Unit
Maximum access time	15	25	55	ns
Typical operating current	190	180	180	mA
Typical Standby Current for ISB1 (both ports TTL level)	50	45	45	mA
Typical Standby Current for ISB3 (both ports CMOS level)	0.05	0.05	0.05	mA

Pin Configuration

Figure 1. 68-pin PLCC (Top View)

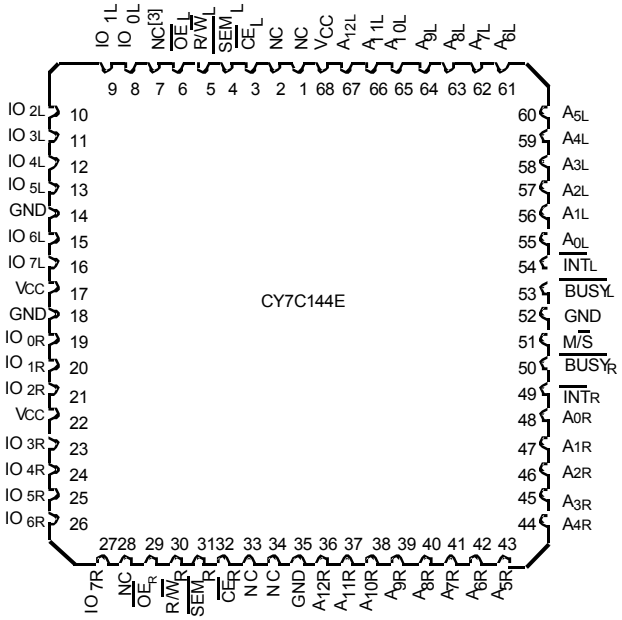


Figure 2. 64-pin TQFP (Top View)

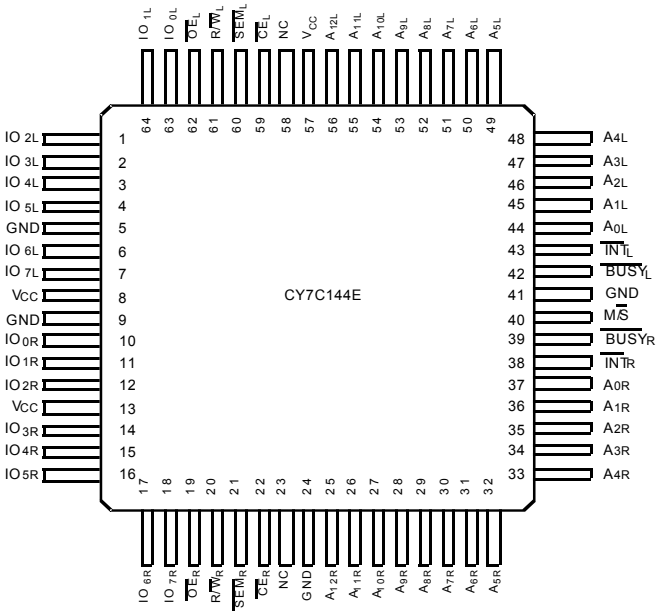


Table 2. Pin Definitions

Left Port	Right Port	Description
I/O_{0L-7L}	I/O_{0R-7R}	Data bus I/O
A_{0L-12L}	A_{0R-12R}	Address lines
CE_L	CE_R	Chip enable
OE_L	OE_R	Output enable
R/W_L	R/W_R	Read / write enable
SEM_L	SEM_R	Semaphore enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
INT_L	INT_R	Interrupt Flag. INT_L is set when right port writes location 1FFE and is cleared when left port reads location 1FFE. INT_R is set when left port writes location 1FFF[4] and is cleared when right port reads location 1FFF[4].
$BUSY_L$	$BUSY_R$	Busy flag
M/S		Master or slave select
V_{CC}		Power
GND		Ground

Architecture

The CY7C144E consists of a an array of 8 K words of 8 bits each of dual-port RAM cells, I/O, address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads / writes to any location in memory. To handle simultaneous writes or reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be used for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/S pin, the CY7C144E can function as a Master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7C144E has an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R / $\overline{W}$ to guarantee a valid write. A write operation is controlled by either the $\overline{OE}$ pin (see Figure 7 on page 12) or the R / $\overline{W}$ pin (see Figure 8 on page 12). Data can be written to the device t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R / $\overline{W}$. Required inputs for non-contention operations are summarized in Table 3 on page 5.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ are asserted. If the user of the CY7C144E wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin.

Interrupts

The interrupt flag ($\overline{INT}$) permits communications between ports.When the left port writes to location 1FFF, the right port's interrupt flag ($\overline{INT}_R$) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag ($\overline{INT}_L$) is accomplished when the right port writes to location 1FFE. This flag is cleared when the left port reads the specified location 1FFE. The message at 1FFF or 1FFE is user-defined. See Table 4 on page 6 for input requirements for $\overline{INT}$. $\overline{INT}_R$ and $\overline{INT}_L$ are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7C144E provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other the Busy logic determines which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. $\overline{BUSY}$ will be asserted t_{BLA}

Notes
3. This pin is NC.
4. 8K x 8 (CY7C144E): 1FFE(left port) and 1FFF(right port)

Master/Slave

An M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This enables the device to interface to a master device with no external components.Writing of slave devices must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation.When presented a HIGH input, the M/$\overline{S}$ pin allows the device to be used as a master and therefore the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C144E provides eight semaphore latches which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports.The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a 0 to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value is available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control over the shared resource, otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore.When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a 1 is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). $A_{0–2}$ represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access.When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a 1 appears at the same semaphore address on the right port. That semaphore can now only be modified by the side showing 0 (the left port in this case). If the left port now relinquishes control by writing a 1 to the semaphore, the semaphore will be set to 1 for both sides. However, if the right port had requested the semaphore (written a 0) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. Table 5 on page 6 shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore is definitely obtained by one side or the other, but there is no guarantee which side controls the semaphore. Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All Semaphores on both sides should have a one written into them at initialization from both sides to assure that they are free when needed.

Table 3. Non-Contending Read/Write

Inputs				Outputs	Operation
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	$I/O_{0–7}$	
H	X	X	H	High Z	Power-down
H	H	L	L	Data out	Read data in semaphore
X	X	H	X	High Z	I/O lines disabled
H	↑	X	L	Data in	Write to semaphore
L	H	L	H	Data out	Read
L	L	X	H	Data in	Write
L	X	X	L		Illegal condition

Table 4. Interrupt Operation Example (assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = HIGH)

Function	Left Port					Right Port				
	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0-12} (CY7C144E)	$\overline{INT}$	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0-12} (CY7C144E)	$\overline{INT}$
Set left $\overline{INT}$	X	X	X	X	L	L	L	X	1FFE	X
Reset left $\overline{INT}$	X	L	L	1FFE	H	X	L	L	X	X
Set right $\overline{INT}$	L	L	X	1FFF	X	X	X	X	X	L
Reset right $\overline{INT}$	X	X	X	X	X	X	L	L	1FFF	H

Table 5. Semaphore Operation Example

Function	I/O_{0-7} Left	I/O_{0-7} Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.[5]

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.3 V to +7.0 V

DC voltage applied to outputs in High Z state .....–0.5 V to +7.0 V

DC input voltage[6].....–0.5 V to +7.0 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... >2001 V (per MIL-STD-883, Method 3015)

Latch-up current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	–40 °C to +85 °C	5 V ± 10%

Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions		7C144E-15			7C144E-25			7C144E-55			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	–	2.4	–	–	2.4	–		V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 4.0 mA		–	–	0.4	–	–	0.4	–	–	0.4	V
V_{IH}	Input HIGH voltage			2.2	–	–	2.2	–	–	2.2	–		V
V_{IL}	Input LOW voltage			–	–	0.8	–	–	0.8	–	–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–10	–	+10	–10	–	+10	–10	–	+10	µA
I_{OZ}	Output leakage current	Outputs disabled, GND ≤ V_O ≤ V_{CC}		–10	–	+10	–10	–	+10	–10	–	+10	µA
I_{CC}	Operating current	V_{CC} = Max, I_{OUT} = 0 mA Outputs disabled	Com'l	–	190	280	–	180	275	–	180	275	mA
			Ind	–	215	305	–	215	305	–	215	305	
I_{SB1}	Standby current (Both ports TTL levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[7]	Com'l	–	50	70	–	45	65	–	45	65	mA
			Ind	–	65	95	–	65	95	–	65	95	
I_{SB2}	Standby current (One port TTL level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[7]	Com'l	–	120	180	–	110	160	–	110	160	mA
			Ind	–	135	205	–	135	205	–	135	205	
I_{SB3}	Standby current (Both ports CMOS levels)	Both ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0[7]	Com'l	–	0.05	0.5	–	0.05	0.5	–	0.05	0.5	mA
			Ind	–	0.05	0.5	–	0.05	0.5	–	0.05	0.5	
I_{SB4}	Standby current (One port CMOS level)	One port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, Active Port outputs, f = f_{MAX}[7]	Com'l	–	110	160	–	100	140	–	100	140	mA
			Ind	–	125	175	–	125	175	–	125	175	

Notes

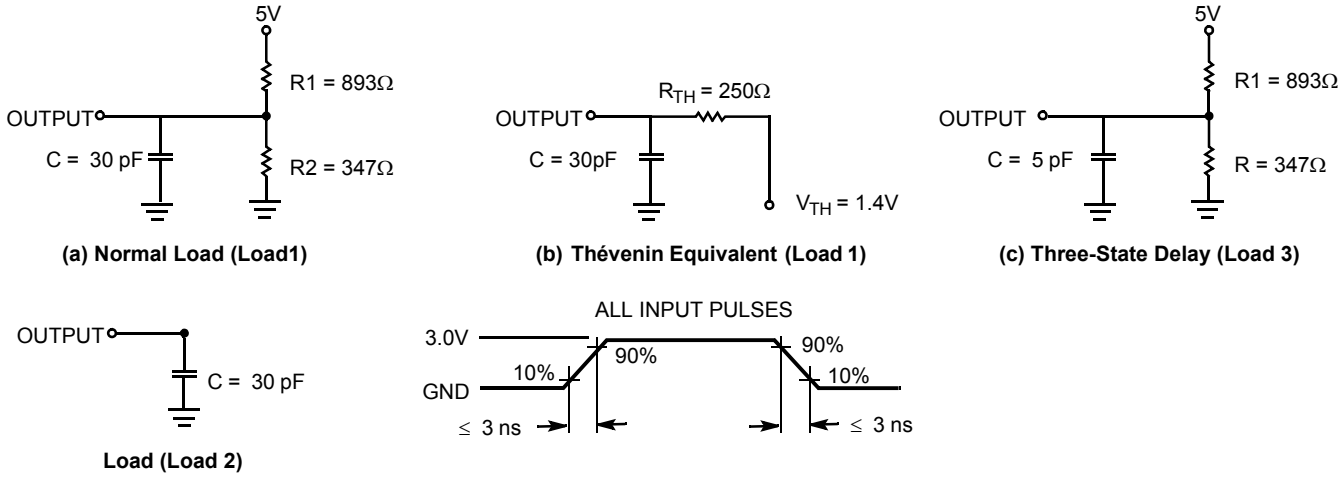
5. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
6. Pulse width < 20 ns.
7. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	10	pF
C_{OUT}	Output capacitance		10	pF

Figure 3. AC Test Loads and Waveforms



(a) Normal Load (Load1)

(b) Thévenin Equivalent (Load 1)

(c) Three-State Delay (Load 3)

Load (Load 2)

Switching Characteristics

Over the operating range[8]

Parameter	Description	7C144E-15		7C144E-25		7C144E-55		Unit
		Min	Max	Min	Max	Min	Max	
READ CYCLE								
t_{RC}	Read cycle time	15	–	25	–	55	–	ns
t_{AA}	Address to data valid	–	15	–	25	–	55	ns
t_{OHA}	Output hold from address change	3	–	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	15	–	25	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	10	–	15	–	25	ns
t_{LZOE}[9, 10]	$\overline{OE}$ Low to Low Z	3	–	3	–	3	–	ns
t_{HZOE}[9, 10]	$\overline{OE}$ HIGH to High Z	–	10	–	15	–	25	ns
t_{LZCE}[9, 10]	$\overline{CE}$ LOW to Low Z	3	–	3	–	3	–	ns
t_{HZCE}[9, 10]	$\overline{CE}$ HIGH to High Z	–	10	–	15	–	25	ns
t_{PU}[10]	$\overline{CE}$ LOW to power-up	0	–	0	–	0	–	ns
t_{PD}[10]	$\overline{CE}$ HIGH to power-down	–	15	–	25	–	55	ns
WRITE CYCLE								
t_{WC}	Write cycle time	15	–	25	–	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	12	–	20	–	45	–	ns
t_{AW}	Address setup to write end	12	–	20	–	45	–	ns
t_{HA}	Address hold from write end	0	–	2	–	2	–	ns
t_{SA}	Address setup to write start	0	–	0	–	0	–	ns
t_{PWE}	Write pulse width	12	–	20	–	40	–	ns
t_{SD}	Data setup to write end	10	–	15	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	0	–	ns
t_{HZWE}[10]	R/$\overline{W}$ LOW to High Z	–	10	–	15	–	25	ns
t_{LZWE}[10]	R/$\overline{W}$ HIGH to Low Z	3	–	3	–	3	–	ns
t_{WDD}[11]	Write pulse to data delay	–	30	–	50	–	70	ns
t_{DDD}[11]	Write data valid to read data valid	–	25	–	30	–	40	ns

Notes

8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OI}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
10. Test conditions used are Load 3. This parameter is guaranteed but not tested.
11. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.

Switching Characteristics (continued)

Over the operating range[8]

Parameter	Description	7C144E-15		7C144E-25		7C144E-55		Unit
		Min	Max	Min	Max	Min	Max	
BUSY TIMING[12]								
t_{BLA}	$\overline{BUSY}$ LOW from address match	–	15	–	20	–	30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from address mismatch	–	15	–	20	–	30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW	–	15	–	20	–	30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH	–	15	–	20	–	30	ns
t_{PS}	Port setup for priority	5	–	5	–	5	–	ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0	–	0	–	0	–	ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13	–	20	–	30	–	ns
t_{BDD}	$\overline{BUSY}$ HIGH to data valid[13]	–	15	–	25	–	55	ns
INTERRUPT TIMING[12]								
t_{INS}	$\overline{INT}$ Set time	–	15	–	25	–	35	ns
t_{INR}	$\overline{INT}$ Reset time	–	15	–	25	–	35	ns
SEMAPHORE TIMING								
t_{SOP}	$\overline{SEm}$ flag update pulse ($\overline{OE}$ or $\overline{SEM}$)	10	–	10	–	20	–	ns
t_{SWRD}	SEm flag write to read time	5	–	5	–	5	–	ns
t_{SPS}	SEm flag contention window	5	–	5	–	5	–	ns
t_{SAA}	SEM Address Access Time	–	15	–	20	–	20	

Note
12. Test conditions used are Load 2.
13. t_{BDD} is a calculated parameter and is the greater of $t_{WDD} – t_{PWE}$ (actual) or $t_{DDD} – t_{SD}$ (actual).

Switching Waveforms

Figure 4. Read Cycle No. 1 (Either Port Address Access)[14, 15]

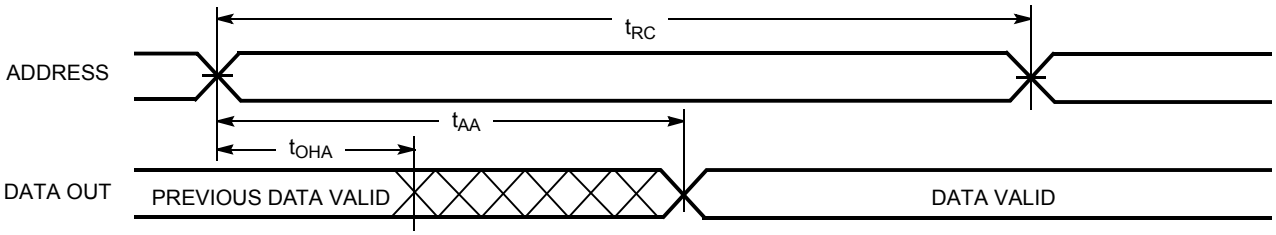


Figure 5. Read Cycle No. 2 (Either Port $\overline{CE}$/$\overline{OE}$ Access)[14, 16, 17]

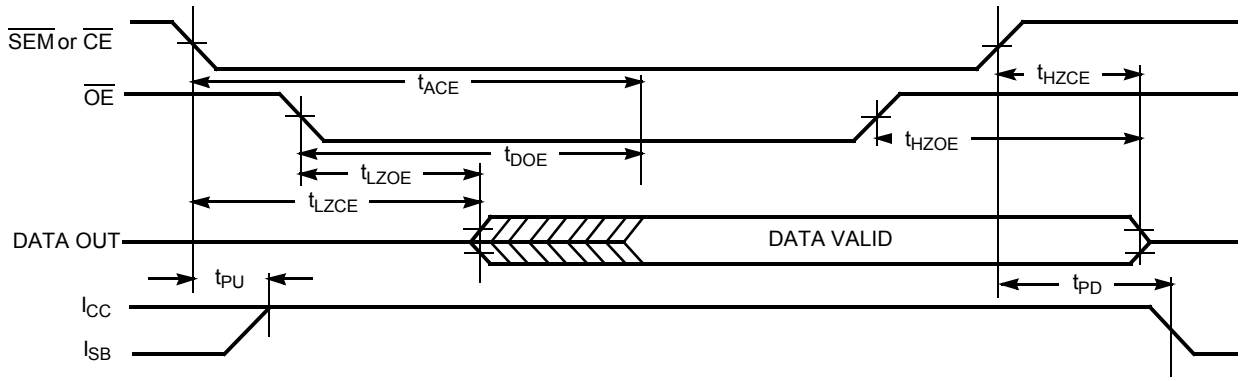
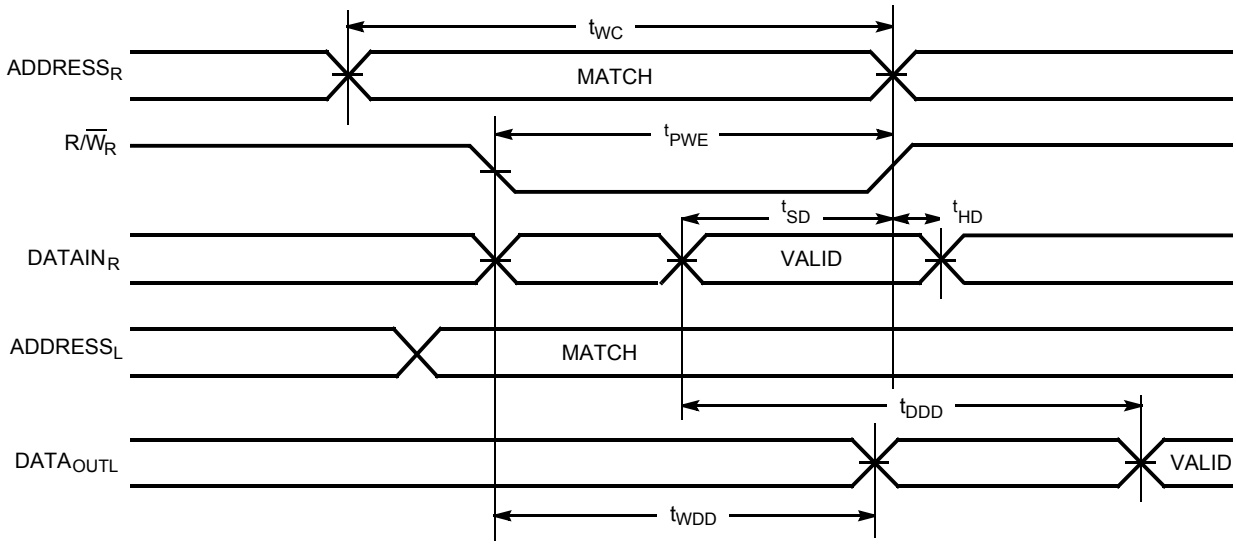


Figure 6. Read Timing with Port-to-port Delay (M/$\overline{S}$ = L)[18, 19]



Notes
14. R/$\overline{W}$ is HIGH for read cycle.
15. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
17. $\overline{CE}_L$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.
18. $\overline{BUSY}$ = HIGH for the writing port.
19. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1: $\overline{OE}$ Three-state Data I/Os (Either Port)[20, 21, 22]

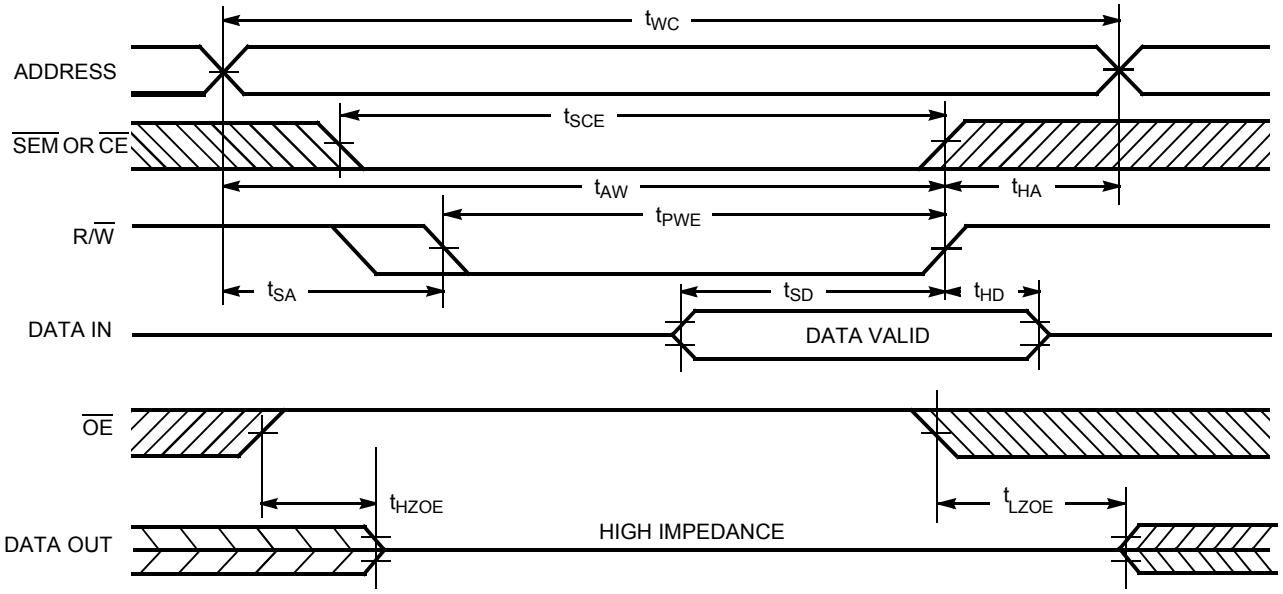
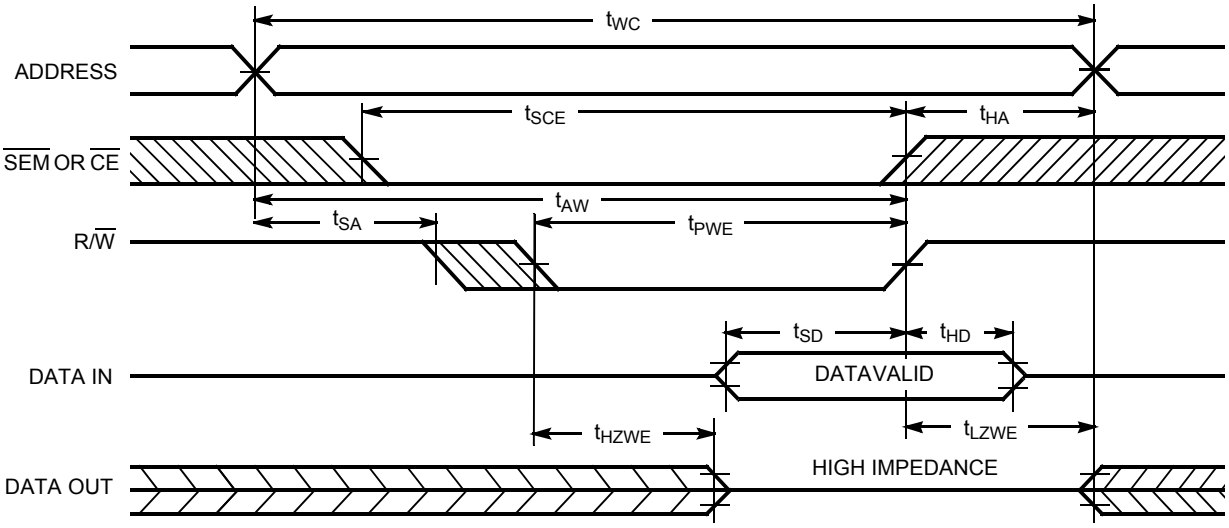


Figure 8. Write Cycle No. 2: R/$\overline{W}$ Three-state Data I/Os (Either Port)[20, 22, 23]



Notes

20. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
21. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
22. R/$\overline{W}$ must be HIGH during all address transitions.
23. Data I/O pins enter high impedance when $\overline{OE}$ is held LOW during write.

Switching Waveforms (continued)

Figure 9. Semaphore Read After Write Timing, Either Side[24]

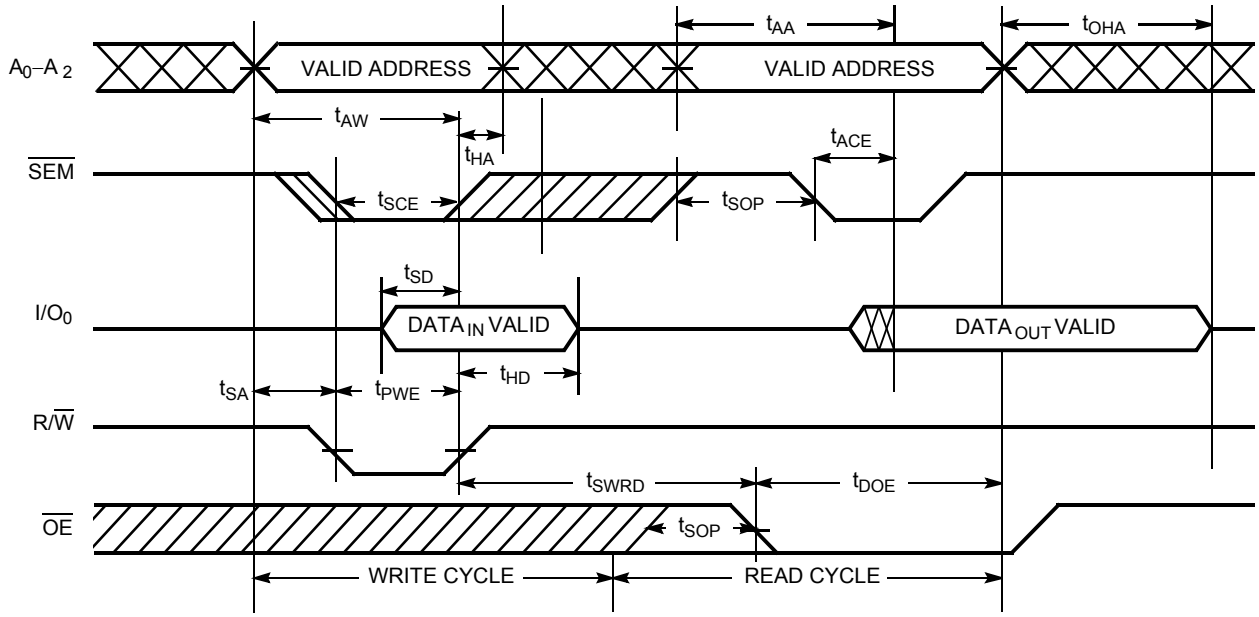
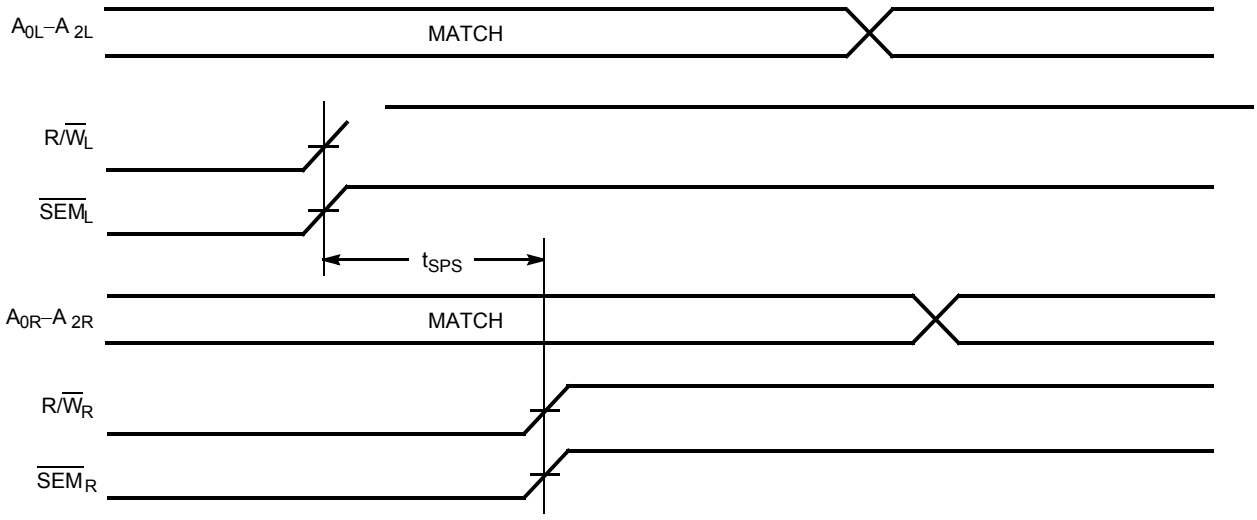


Figure 10. Semaphore Contention[25, 26, 27]



Notes
24. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
25. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
26. Semaphores are reset (available to both ports) at cycle start.
27. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)

Figure 11. Read with $\overline{BUSY}$ (M/S = HIGH)[19]

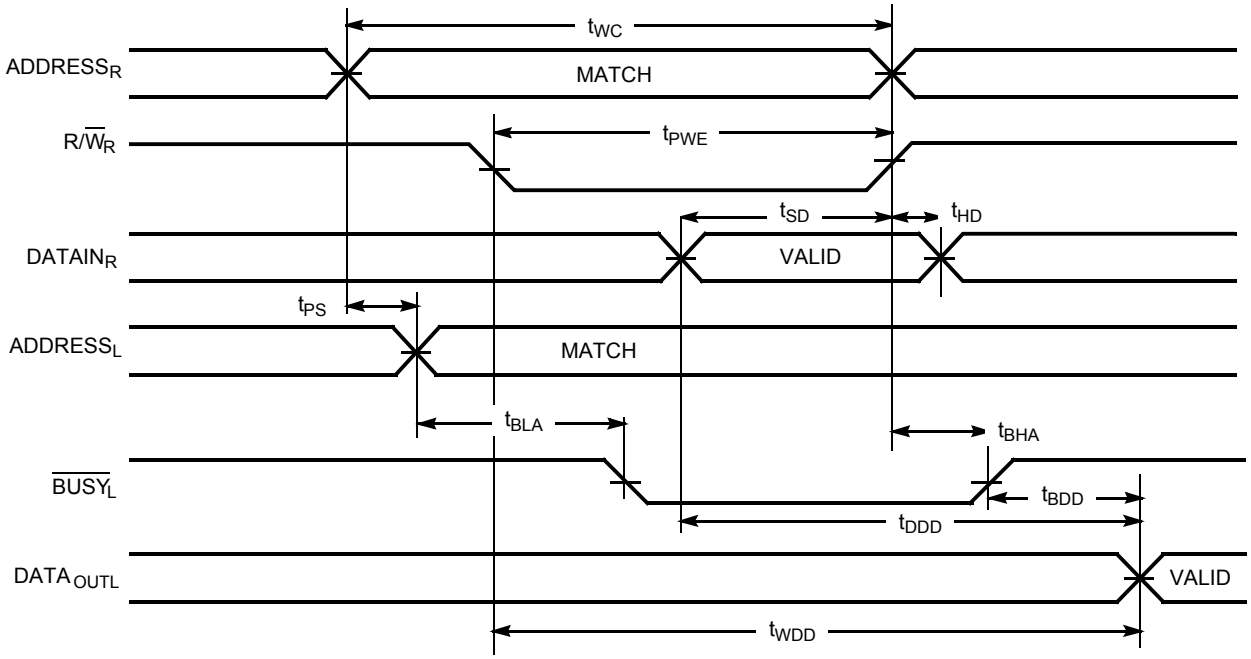
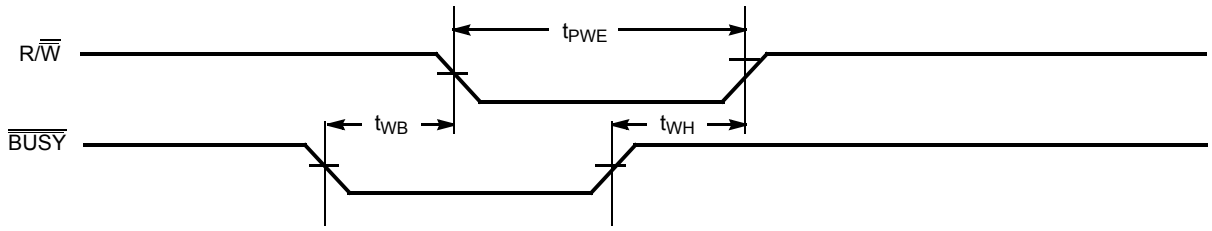


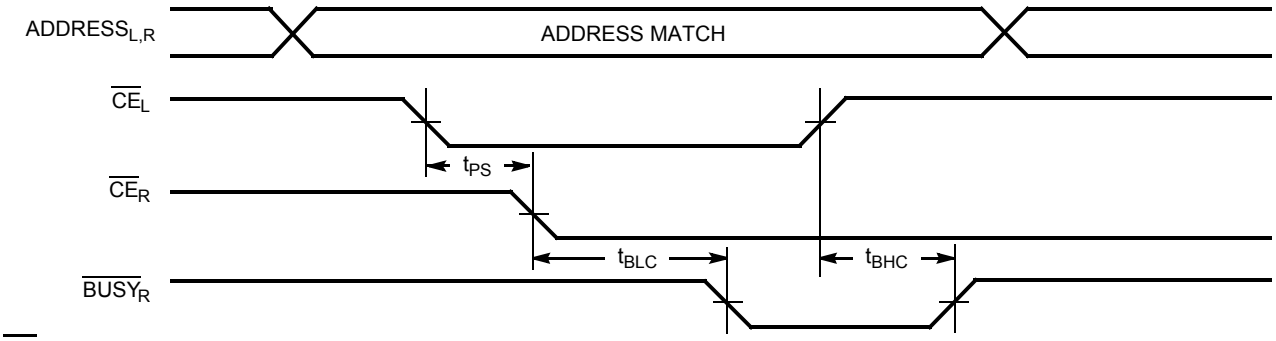
Figure 12. Write Timing with Busy Input (M/$\overline{S}$ = LOW)



Switching Waveforms (continued)

Figure 13. Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[28]

$\overline{CE}_L$ Valid First:



$\overline{CE}_R$ Valid First:

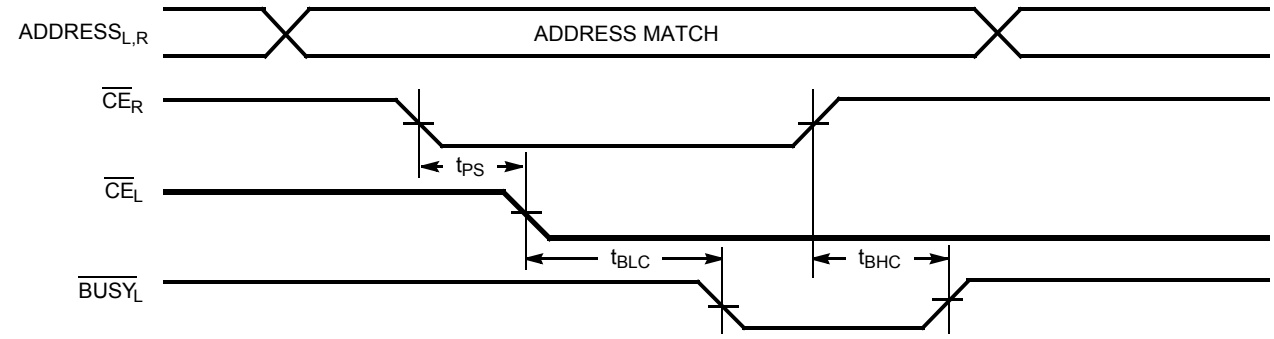
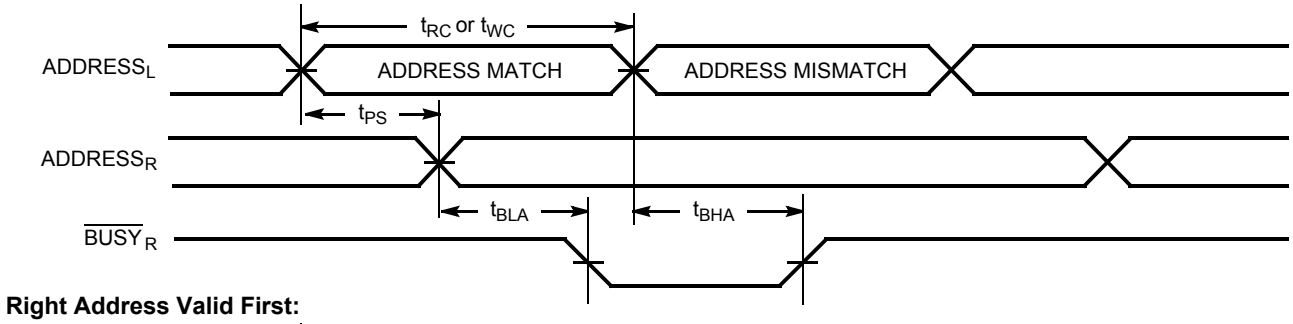
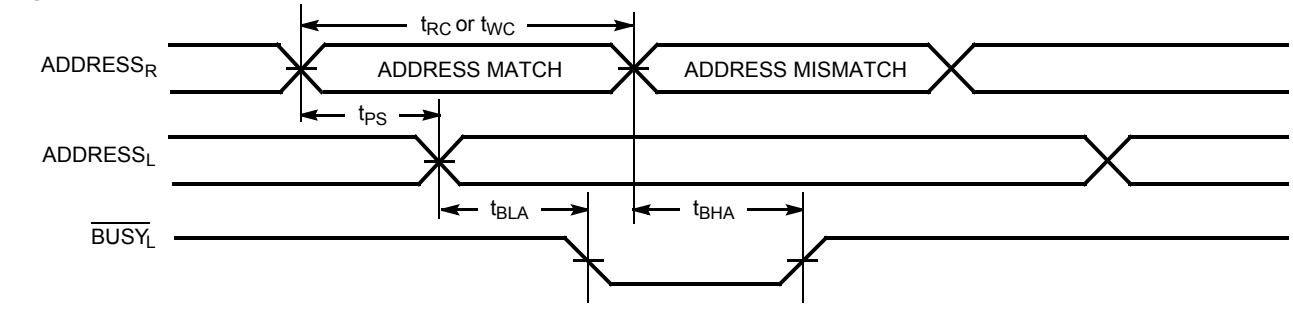


Figure 14. Busy Timing Diagram No. 2 (Address Arbitration)[28]

Left Address Valid First:



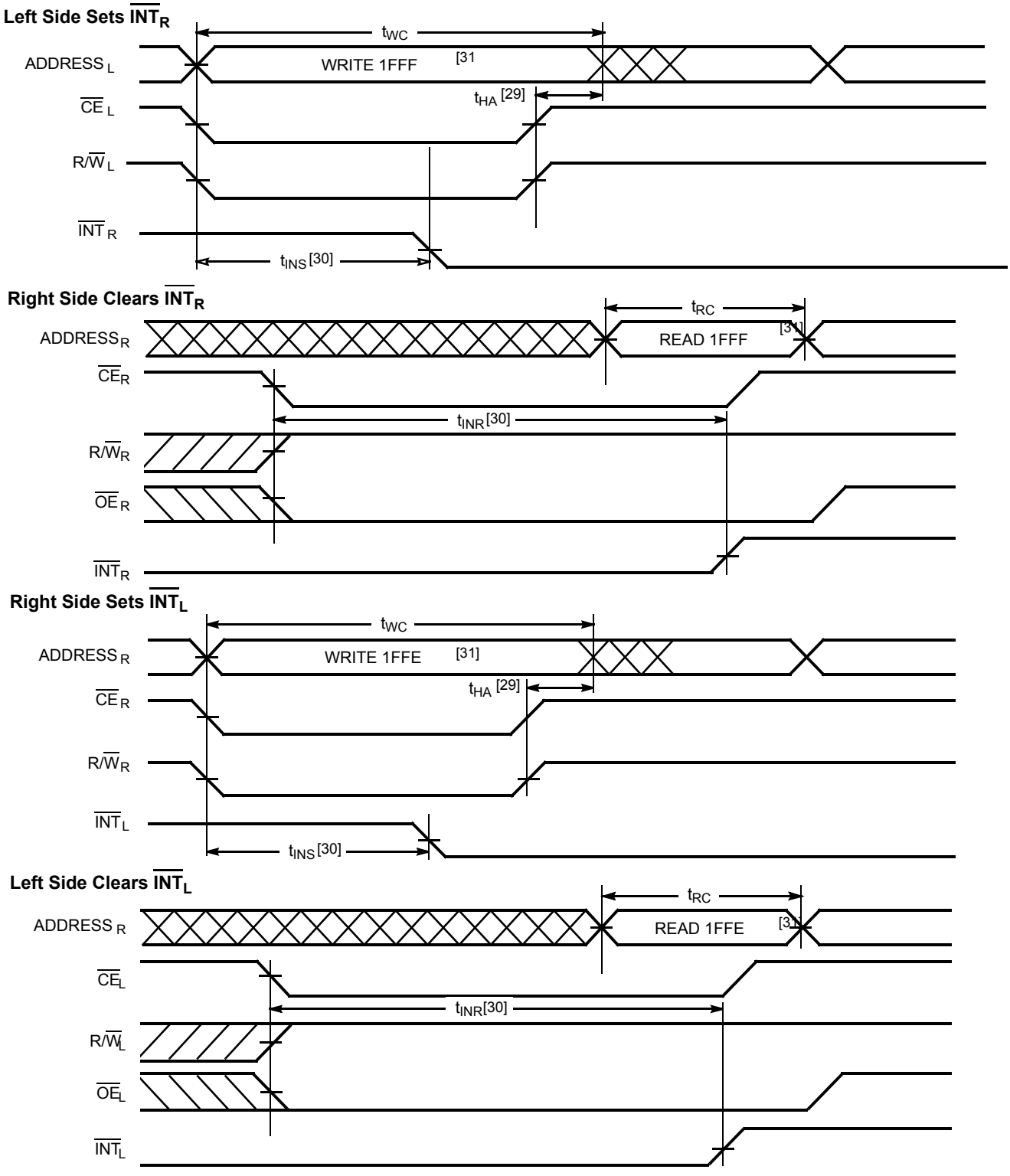
Right Address Valid First:



Note
28. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.

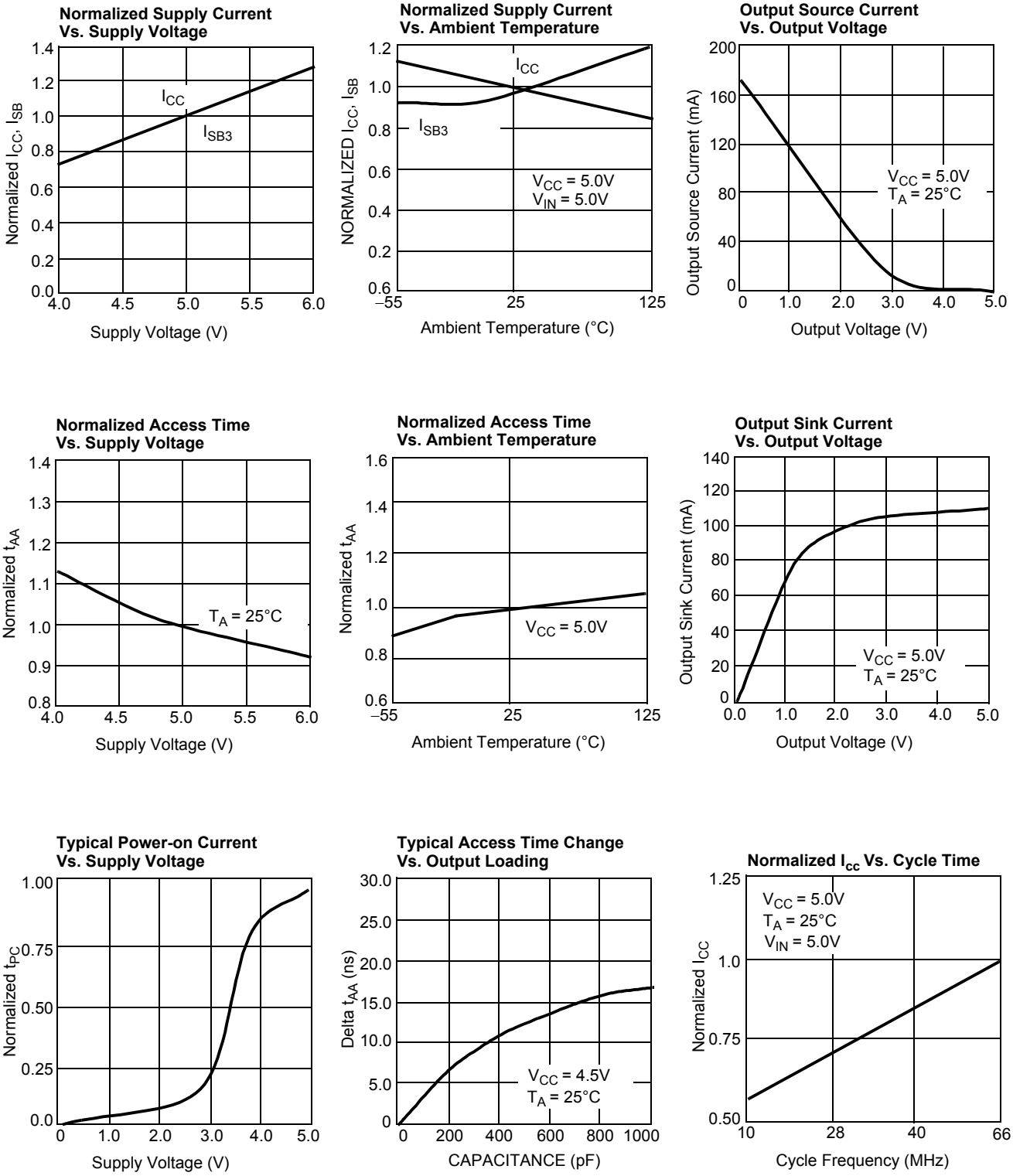
Switching Waveforms (continued)

Figure 15. Interrupt Timing Diagrams



Notes
29. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
30. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.
31. 8 K × 8 (CY7C144E): 1FFE(left port) and 1FFF(right port).

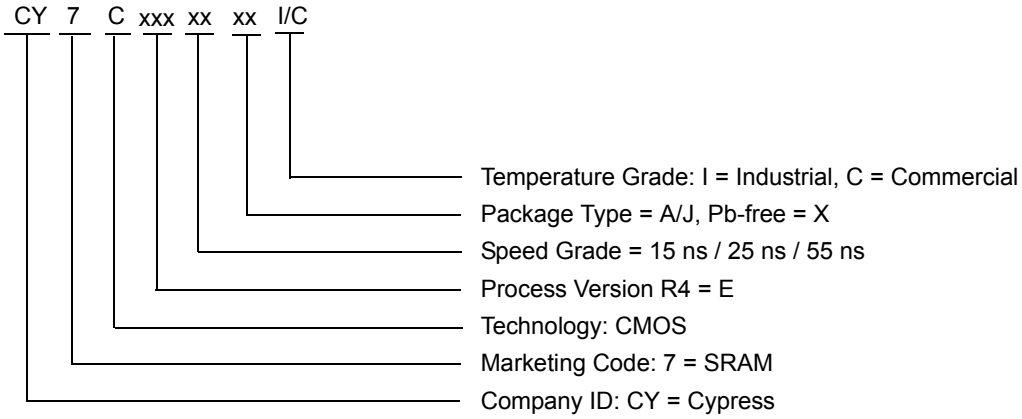
Figure 16. Typical DC and AC Characteristics



Ordering Information

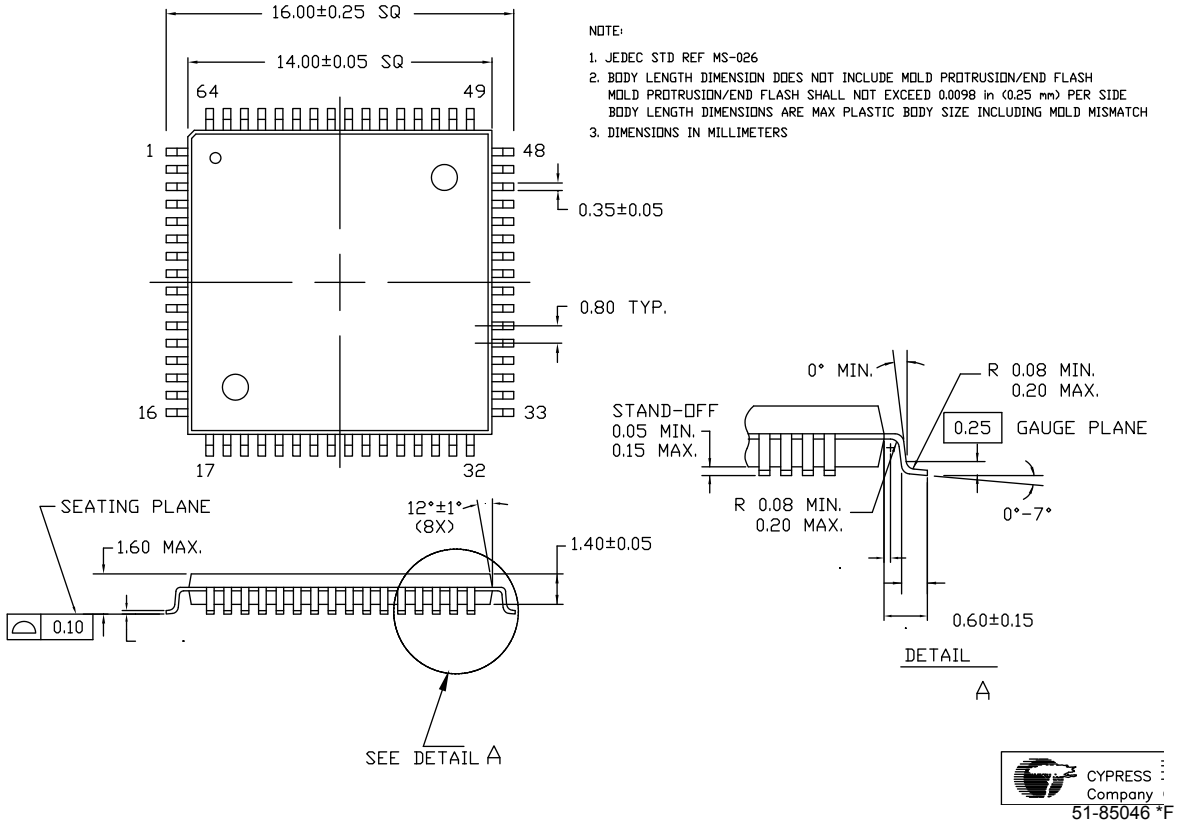
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C144E-15AXC	51-85046	64-pin TQFP (Pb-free)	Commercial
	CY7C144E-15JXI	51-85005	68-pin plastic leaded chip carrier (Pb-free)	Industrial
	CY7C144E-15AXI	51-85046	64-pin TQFP (Pb-free)	Industrial
25	CY7C144E-25AXC	51-85046	64-pin Thin Quad Flat Pack (Pb-free)	Commercial
55	CY7C144E-55AXC	51-85046	64-pin TQFP (Pb-free)	Commercial
	CY7C144E-55JXC	51-85005	68-pin plastic leaded chip carrier (Pb-free)	Commercial

Ordering Code Definitions



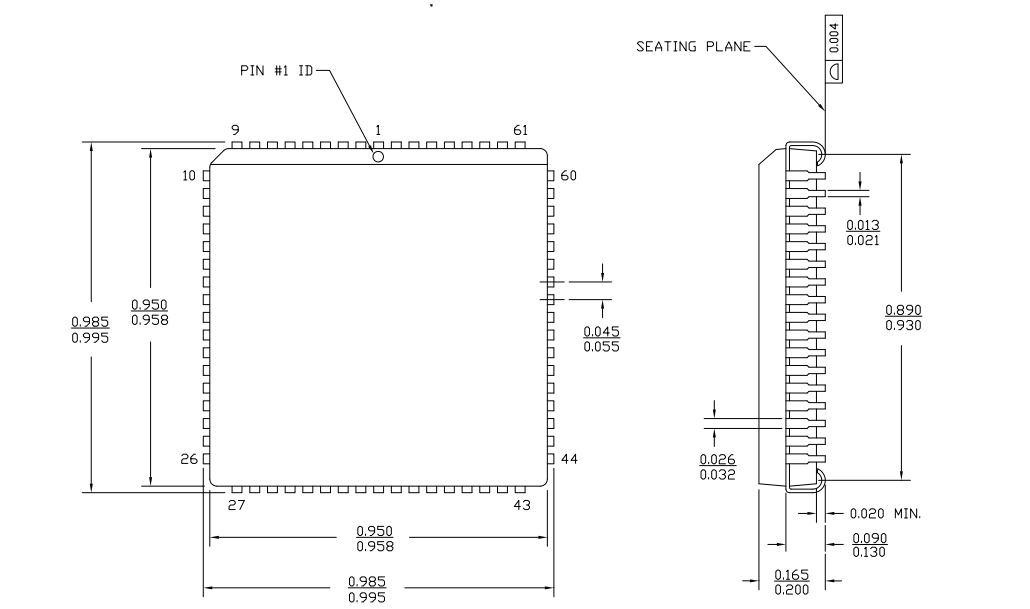
Package Diagrams

Figure 17. 64-pin Thin Plastic Quad Flat Pack (14 × 14 × 1.4 mm)



Package Diagrams (continued)

Figure 18. 68-pin Plastic Leaded Chip Carrier



DIMENSIONS IN INCHES MIN.
MAX.

51-85005 *C

Acronyms

Table 6. Acronyms Used

Acronym	Description
CMOS	complementary metal oxide semiconductor
$\overline{CE}$	chip enable
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
$\overline{WE}$	write enable

Reference Documents

CY7C144, CY7C145 8K × 8/9 Dual-Port Static RAM with SEM, INT, BUSY (38-06034)

Document Conventions

Units of Measure

Table 7. Units of Measure

Symbol	Unit of Measure
ns	nano second
V	volt
µA	micro ampere
mA	milli ampere
pF	pico Farad
°C	degree Celsius
W	watt

Document History Page

Document Title: CY7C144E 8 K × 8 Dual-port Static RAM with SEM, INT, BUSY Document Number: 001-63982				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3038037	ADMU	09/24/10	New data sheet
*A	3395887	ADMU	10/05/11	Changed status from Preliminary to Final. Removed CY7C138E and related information.
*B	3403147	ADMU	10/12/2011	No technical updates.
*C	4559526	ADMU	11/07/2014	Added documentation related hyperlink in page 1 Updated package diagram from 51-85046 *E to 51-85046 *F

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