

## Features

- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- High speed
  - $t_{AA} = 20 \text{ ns}$
- Low active power
  - 495 mW
- Low standby power
  - 110 mW
- TTL-compatible inputs and outputs
- $V_{IH}$  of 2.2 V
- Capable of withstanding greater than 2001 V electrostatic discharge

## Functional Description

The CY7C168A is a high-performance CMOS static RAM organized as 4096 by 4-bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and three-state drivers. The CY7C168A has an automatic power-down feature, reducing the power consumption by 77% when deselected.

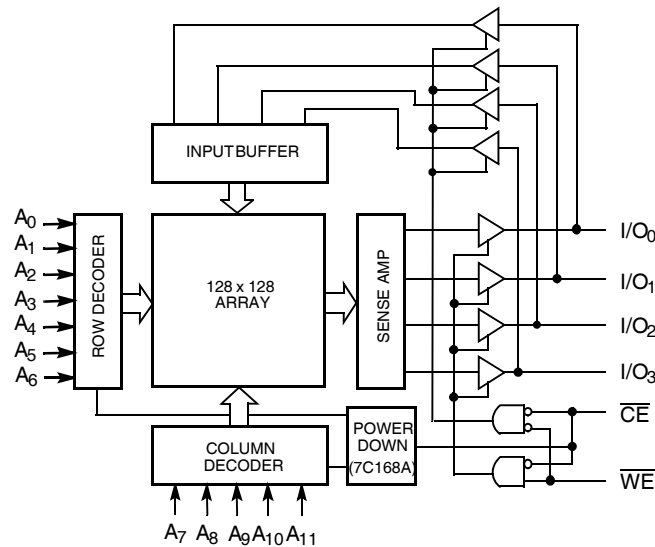
Writing to the device is accomplished when the chip select ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the four data input/output pins ( $I/O_0$  through  $I/O_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{11}$ ).

Reading the device is accomplished by taking the chip enable ( $\overline{CE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data input/output pins ( $I/O_0$  through  $I/O_3$ ).

The input/output pins remain in a high-impedance state when chip enable ( $\overline{CE}$ ) is HIGH or write enable ( $\overline{WE}$ ) is LOW.

A die coat is used to insure alpha immunity.

## Logic Block Diagram



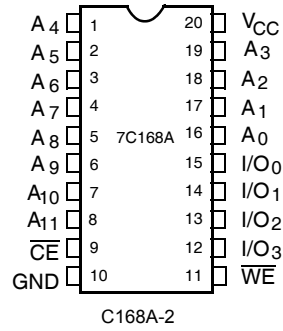
C168A-1

## Contents

<b>Pin Configuration</b> .....	<b>3</b>	<b>Ordering Information</b> .....	<b>9</b>
<b>Selection Guide</b> .....	<b>3</b>	Ordering Code Definitions .....	9
<b>Maximum Ratings</b> .....	<b>4</b>	<b>Package Diagram</b> .....	<b>9</b>
<b>Operating Range</b> .....	<b>4</b>	<b>Acronyms</b> .....	<b>10</b>
<b>Electrical Characteristics</b> .....	<b>4</b>	<b>Document Conventions</b> .....	<b>10</b>
<b>Capacitance</b> .....	<b>5</b>	Units of Measure .....	10
<b>AC Test Loads and Waveforms</b> .....	<b>5</b>	<b>Document History Page</b> .....	<b>11</b>
<b>Switching Characteristics</b> .....	<b>6</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>12</b>
<b>Switching Waveforms</b> .....	<b>6</b>	Worldwide Sales and Design Support .....	12
<b>Typical DC and AC Characteristics</b> .....	<b>8</b>	Products .....	12
		PSoC Solutions .....	12

**Pin Configuration**

**Figure 1. DIP Top View**



**Selection Guide**

		<b>7C168A-20</b>
Maximum access time (ns)		20
Maximum operating current (mA)	Commercial	90
	Military	100

**Maximum Ratings**

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

- Storage temperature ..... -65 °C to +150 °C
- Ambient temperature with power applied..... -55 °C to +125 °C
- Supply voltage to ground potential (pin 20 to pin 10)..... -0.5 V to +7.0 V
- DC voltage applied to outputs in high Z state..... -0.5 V to +7.0 V
- DC input voltage ..... -3.0 V to +7.0 V

- Output current into outputs (low) ..... 20 mA
- Static discharge voltage..... > 2001 V (per MIL-STD-883, method 3015)
- Latch-up current ..... > 200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0 °C to +70 °C	5 V ± 10%

**Electrical Characteristics**

Over the Operating Range

Parameter	Description	Test Conditions	7C168A-20		Unit
			Min	Max	
V <sub>OH</sub>	Output HIGH voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4	-	V
V <sub>OL</sub>	Output LOW voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA	-	0.4	V
V <sub>IH</sub>	Input HIGH voltage		2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW voltage <sup>[1]</sup>		-0.5	0.8	V
I <sub>IX</sub>	Input load current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	+10	µA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , output disabled	-10	+10	µA
I <sub>OS</sub>	Output short circuit current <sup>[2]</sup>	V <sub>CC</sub> = Max, V <sub>OUT</sub> = GND	-	-350	mA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA	-	90	mA
I <sub>SB1</sub>	Automatic $\overline{CE}$ power-down current	Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$	-	40	mA
I <sub>SB2</sub>	Automatic $\overline{CE}$ power-down current	Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3 V$	-	20	mA

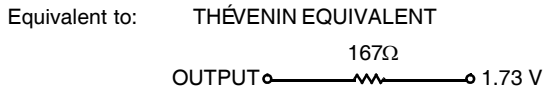
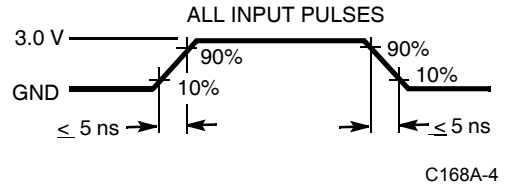
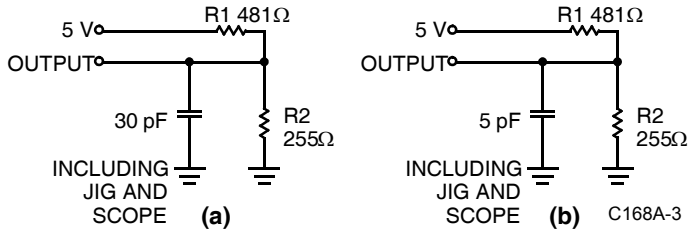
**Notes**

1. V<sub>IL</sub> min = -3.0 V for pulse durations less than 30 ns.
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Capacitance<sup>[3]</sup>

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 5.0 V	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

AC Test Loads and Waveforms



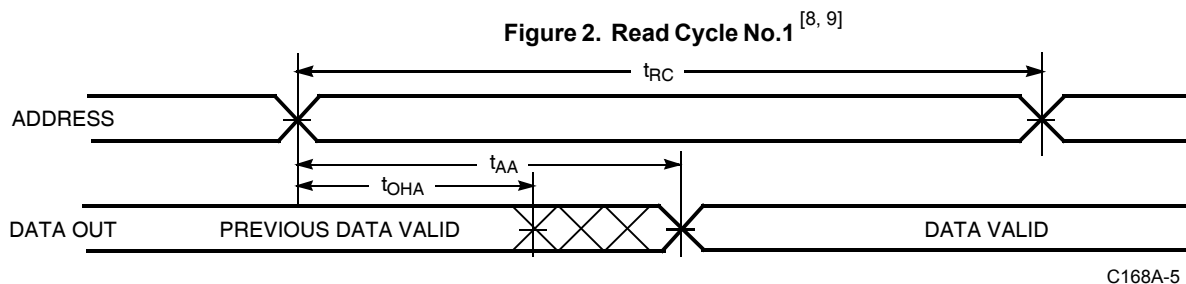
**Note**  
 3. Tested initially and after any design or process changes that may affect these parameters.

## Switching Characteristics

Over the Operating Range<sup>[4]</sup>

Parameter	Description	7C168A-20		Unit
		Min.	Max.	
<b>READ CYCLE</b>				
$t_{RC}$	Read cycle time	20	–	ns
$t_{AA}$	Address to data valid	–	20	ns
$t_{OHA}$	Output hold from address change	5	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	20	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low Z <sup>[5]</sup>	5	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to high Z <sup>[5, 6]</sup>	–	8	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down	–	20	ns
$t_{RCS}$	Read command set-up	0	–	ns
$t_{RCH}$	Read command hold	0	–	ns
<b>WRITE CYCLE<sup>[7]</sup></b>				
$t_{WC}$	Write cycle time	20	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	15	–	ns
$t_{AW}$	Address set-up to write end	15	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address set-up to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	15	–	ns
$t_{SD}$	Data set-up to write end	10	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[5]</sup>	7	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[5, 6]</sup>	5	–	ns

## Switching Waveforms



### Notes

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
- At any given temperature and voltage condition,  $t_{HZ}$  is less than  $t_{LZ}$  for all devices. Transition is measured  $\pm 500$  mV from steady state voltage with specified loading in part (b) of AC Test Loads and Waveforms.
- $t_{HZCE}$  and  $t_{HZWE}$  are tested with  $C_L = 5$  pF as in part (a) of Test Loads and Waveforms. Transition is measured  $\pm 500$  mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CE} = V_{IL}$ .

Switching Waveforms (continued)

Figure 3. Read Cycle<sup>[10, 11]</sup>

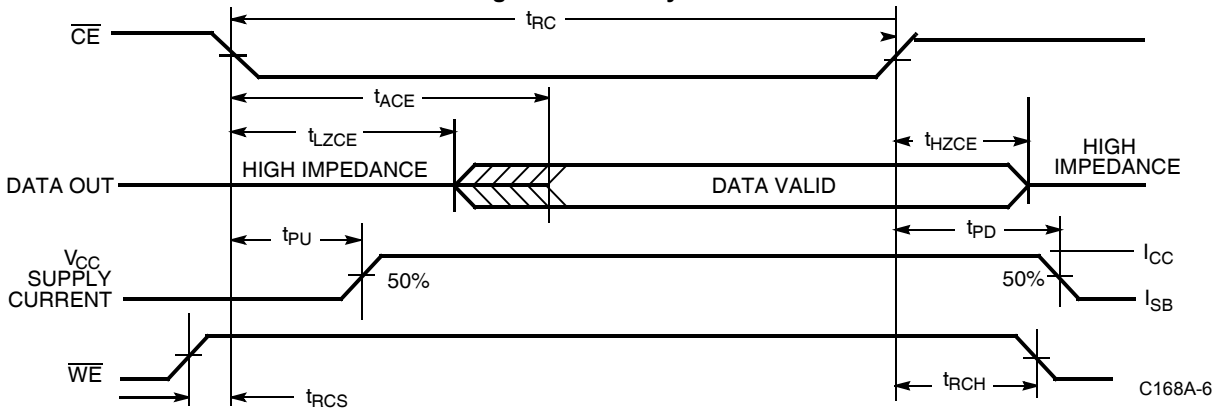


Figure 4. Write Cycle No.1 (WE Controlled)<sup>[12]</sup>

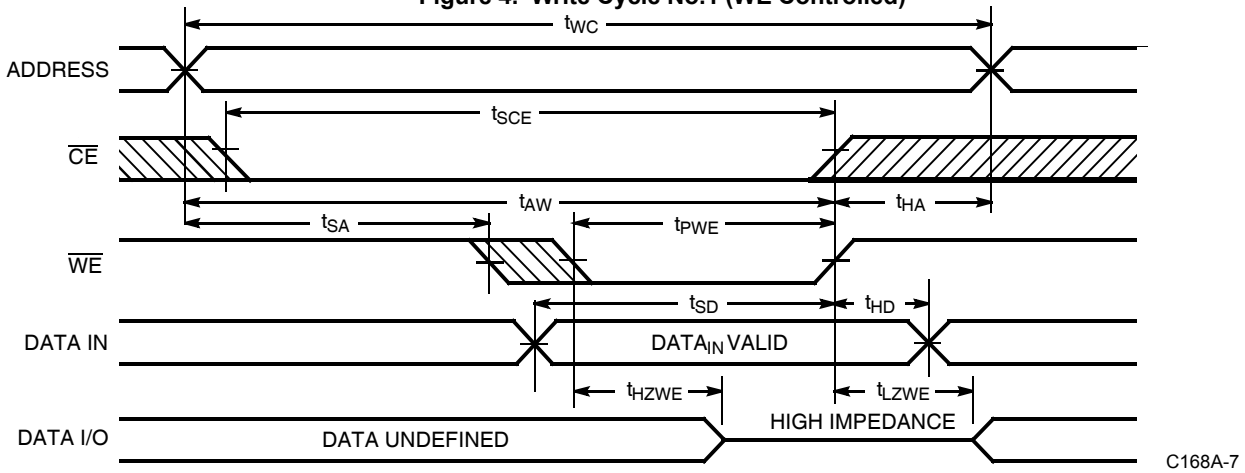
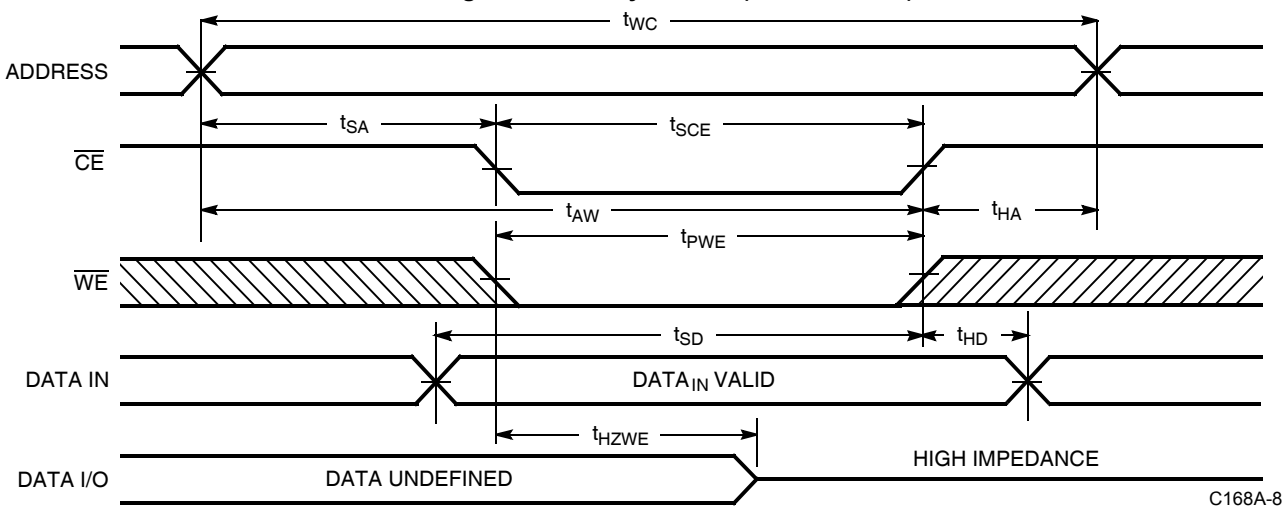


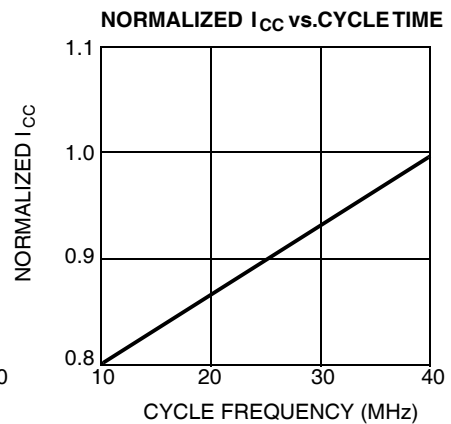
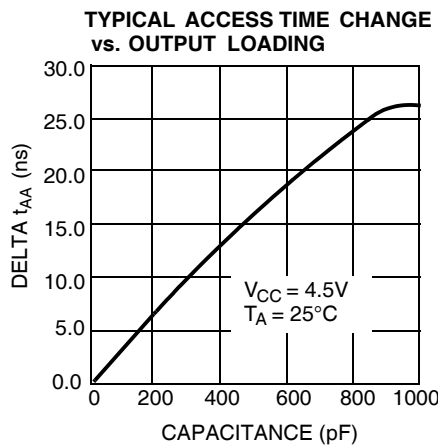
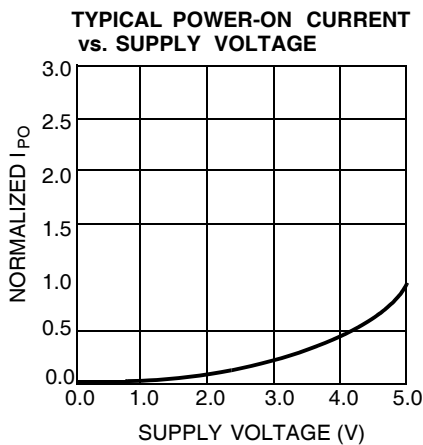
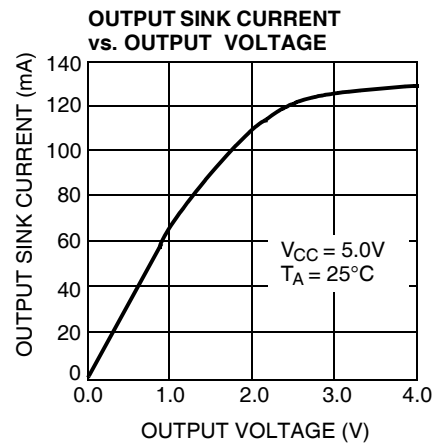
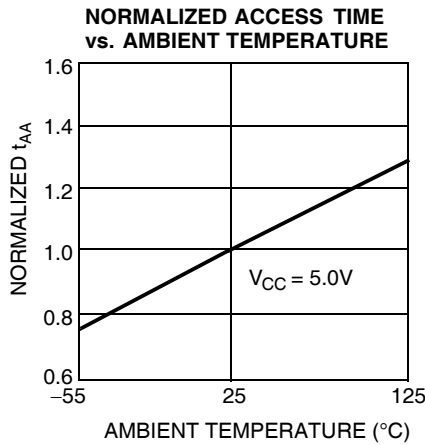
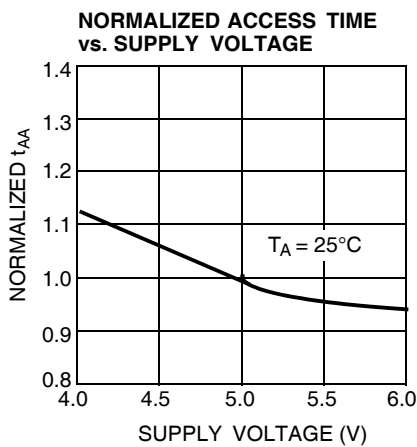
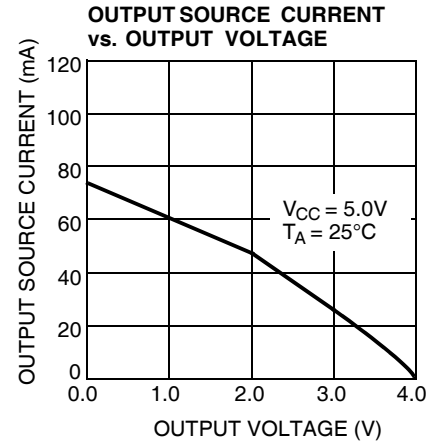
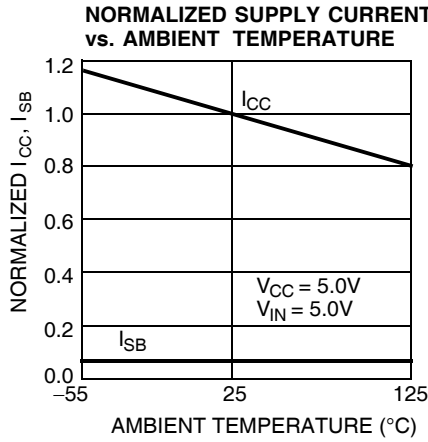
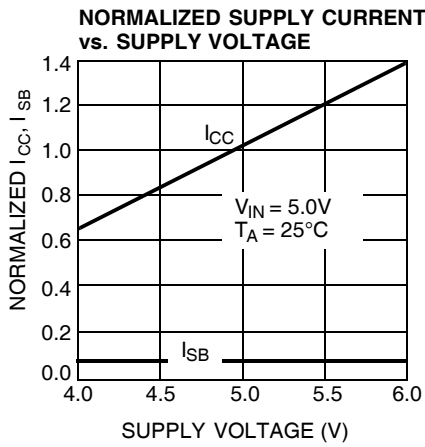
Figure 5. Write Cycle No. 2 (CS Controlled)<sup>[12, 13]</sup>



Notes

- 10. WE is HIGH for read cycle.
- 11. Address valid prior to or coincident with CE transition LOW.
- 12. The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- 13. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

### Typical DC and AC Characteristics

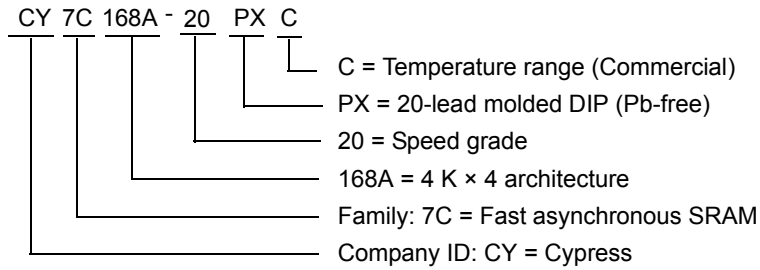




### Ordering Information

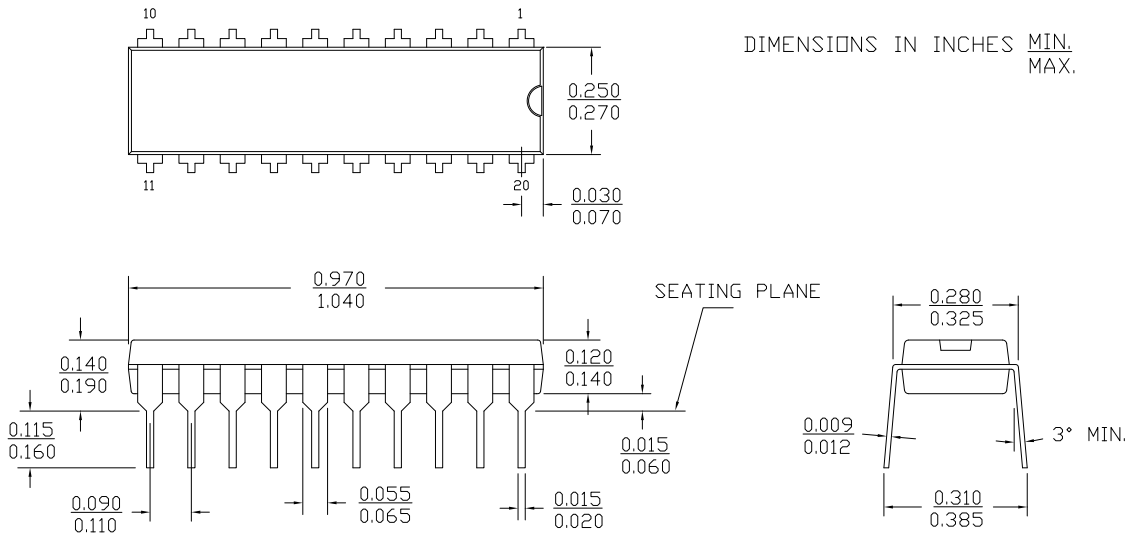
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C168A-20PXC	P5	20-Lead Molded DIP	Commercial

### Ordering Code Definitions



### Package Diagram

Figure 6. 20-Lead (300-Mil) Molded DIP P5



### Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
CE	chip enable
DIP	dual inline package
I/O	input/output
SRAM	static random access memory
TTL	transistor-transistor logic
WE	write enable

### Document Conventions

#### Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
μA	micro Amperes
mA	milli Amperes
mV	milli Volts
mW	milli Watts
pF	pico Farad
°C	degree Celcius
W	Watts
%	percent

Document History Page

Document Title: CY7C168A 4 K × 4 RAM Document Number: 38-05029				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106815	09/10/01	SZV	Change from Spec number: 38-00095 to 38-05029
*A	3008799	08/19/2010	AJU	Updated $t_{AA}$ to 20 ns under High Speed, 495 mW under Low active power in Features section Updated Figure caption to DIP Top View in Pin Configuration section Updated Selection Guide section with only 7C168A-20 values Updated Operating Range section with only Commercial temperature range Updated Electrical Characteristics section with only 7C168A-20 values Updated Switching Characteristics section with only 7C168A-20 values Updated Ordering Information section with only CY7C168A-20PXC Ordering Code Updated Package Diagram with only the latest revision of "20-Lead (300-Mil) Molded DIP P5" (Figure 6 in page 8) Minor edits and updated in new template
*B	3090588	11/19/2010	AJU	Post to external web.
*C	3097955	11/30/2010	PRAS	No technical updates. Sunset review.

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