CY7C1012AV33

512 K × 24 Static RAM

Features

- High speed
  - t_{AA} = 8 ns
- Low active power
  - 1080 mW (max)
- Operating voltages of 3.3 ± 0.3 V
- 2.0 V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with $\overline{CE}_0$, $\overline{CE}_1$ and $\overline{CE}_2$ features
- Available in non Pb-free 119 ball PBGA.

Functional Description

The CY7C1012AV33 is a high-performance CMOS static RAM organized as 512 K words by 24 bits. Each data byte is separately controlled by the individual chip selects ($\overline{CE}_0$, $\overline{CE}_1$, $\overline{CE}_2$). $\overline{CE}_0$ controls the data on the I/O_0–I/O_7, while $\overline{CE}_1$ controls the data on I/O_8–I/O_{15}, and $\overline{CE}_2$ controls the data on the data pins I/O_{16}–I/O_{23}. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

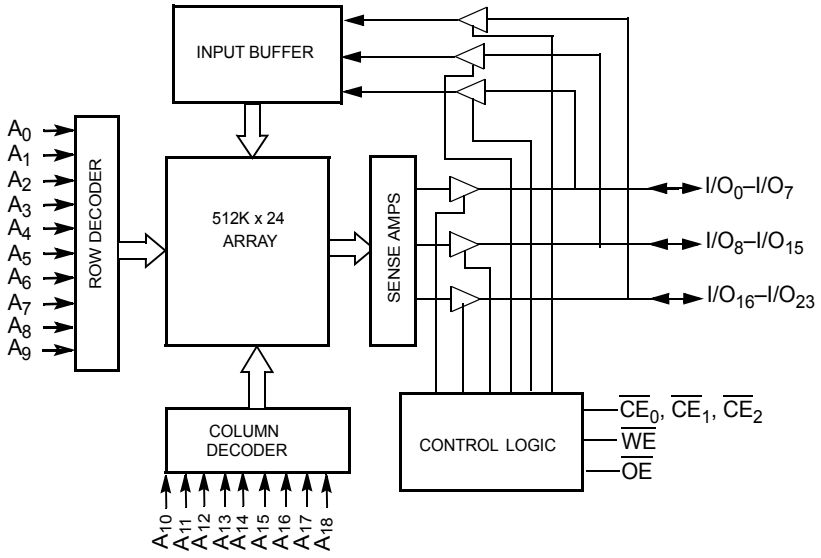
Writing the data bytes into the SRAM is accomplished when the chip select controlling that byte is LOW and the write enable input ($\overline{WE}$) input is LOW. Data on the respective input/output (I/O) pins is then written into the location specified on the address pins (A_0–A_{18}). Asserting all of the chip selects LOW and write enable LOW will write all 24 bits of data into the SRAM. Output enable ($\overline{OE}$) is ignored while in WRITE mode.

Data bytes can also be individually read from the device. Reading a byte is accomplished when the chip select controlling that byte is LOW and write enable ($\overline{WE}$) HIGH while output enable ($\overline{OE}$) remains LOW. Under these conditions, the contents of the memory location specified on the address pins will appear on the specified data input/output (I/O) pins. Asserting all the chip selects LOW will read all 24 bits of data from the SRAM.

The 24 I/O pins (I/O_0–I/O_{23}) are placed in a high-impedance state when all the chip selects are HIGH or when the output enable ($\overline{OE}$) is HIGH during a READ mode. For further details, refer to the truth table of this data sheet.

The CY7C1012AV33 is available in a standard 119-ball PBGA. For a complete list of related documentation, click here.

Functional Block Diagram



Contents

Selection Guide

Description		-8	Unit
Maximum Access Time		8	ns
Maximum Operating Current	Commercial	300	mA
	Industrial	300	
Maximum CMOS Standby Current	Commercial / Industrial	50	mA

Pin Configurations

Figure 1. 119-ball PBGA pinout (Top View) [1, 2]

	1	2	3	4	5	6	7
A	NC	A	A	A	A	A	NC
B	NC	A	A	$\overline{CE}_0$	A	A	NC
C	I/O_{12}	NC	$\overline{CE}_1$	NC	$\overline{CE}_2$	NC	I/O_0
D	I/O_{13}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_1
E	I/O_{14}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_2
F	I/O_{15}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_3
G	I/O_{16}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_4
H	I/O_{17}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_5
J	NC	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	DNU
K	I/O_{18}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_6
L	I/O_{19}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_7
M	I/O_{20}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_8
N	I/O_{21}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_9
P	I/O_{22}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{10}
R	I/O_{23}	A	NC	NC	NC	A	I/O_{11}
T	NC	A	A	$\overline{WE}$	A	A	NC
U	NC	A	A	$\overline{OE}$	A	A	NC

Notes
1. NC pins are not connected on the die.
2. DNU pins have to be left floating or tied to VSS to ensure proper application.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{CC} to Relative GND[3] .....–0.5 V to +4.6 V

DC Voltage Applied to Outputs in high Z State [3] .....–0.5 V to V_{CC} + 0.5 V

DC Input Voltage [3] .....–0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	3.3 V ± 0.3 V
Industrial	–40 °C to +85 °C	

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions [4]		-8		Unit
				Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA		–	0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	V
V_{IL} [3]	Input LOW Voltage			–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, $f = f_{MAX} = 1/t_{RC}$	Commercial	–	300	mA
			Industrial	–	300	mA
I_{SB1}	Automatic CE Power-down Current – TTL Inputs	Max V_{CC}, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}		–	100	mA
I_{SB2}	Automatic CE Power-down Current – CMOS Inputs	Max V_{CC}, $\overline{CE} \geq V_{CC}$ – 0.3 V, $V_{IN} \geq V_{CC}$ – 0.3 V, or $V_{IN} \leq$ 0.3 V, f = 0	Commercial / Industrial	–	50	mA

Notes

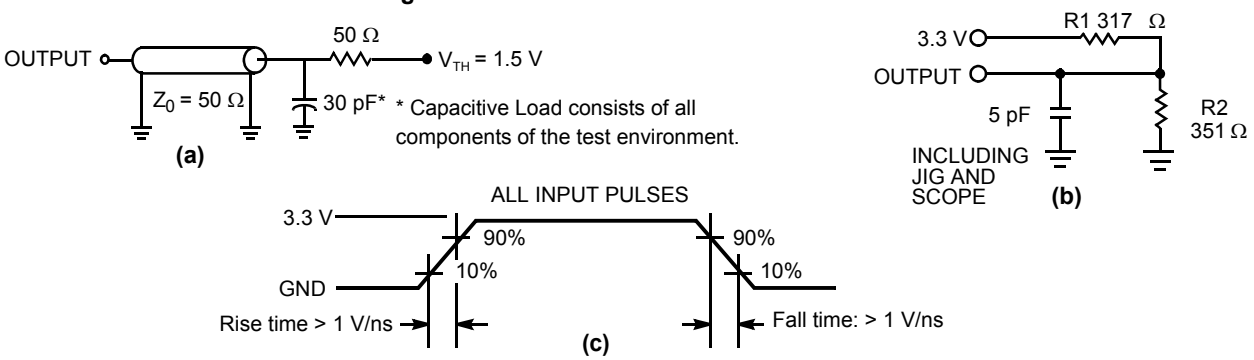
3. V_{IL} (min) = –2.0 V for pulse durations of less than 20 ns.
4. $\overline{CE}$ refers to a combination of $\overline{CE_0}$, $\overline{CE_1}$, and $\overline{CE_2}$. $\overline{CE}$ is active LOW when all three of these signals are active LOW at the same time.

Capacitance

Parameter [5]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	8	pF
C_{OUT}	I/O Capacitance		10	pF

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [6]



Notes

5. Tested initially and after any design or process changes that may affect these parameters.
6. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0 V). As soon as 1 ms (T_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0 V) voltage.

AC Switching Characteristics

Over the Operating Range

Parameter [7]	Description	-8		Unit
		Min	Max	
Read Cycle				
t_{power}[8]	V_{CC}(typical) to the first access	1	–	ms
t_{RC}	Read Cycle Time	8	–	ns
t_{AA}	Address to Data Valid	–	8	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	$\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW to Data Valid	–	8	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	5	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z[9]	1	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z[9]	–	5	ns
t_{LZCE}	$\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW to low Z[9]	3	–	ns
t_{HZCE}	$\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH to high Z[9]	–	5	ns
t_{PU}	$\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW to power-up[10]	0	–	ns
t_{PD}	$\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH to power-down[10]	–	8	ns
t_{DBE}	Byte Enable to Data Valid	–	5	ns
t_{LZBE}	Byte Enable to low Z[9]	1	–	ns
t_{HZBE}	Byte Disable to high Z[9]	–	5	ns
Write Cycle[11, 12]				
t_{WC}	Write Cycle Time	8	–	ns
t_{SCE}	$\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW to Write End	6	–	ns
t_{AW}	Address Set-up to Write End	6	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Set-up to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	6	–	ns
t_{SD}	Data Set-up to Write End	5	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z[13]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z[13]	–	5	ns
t_{BW}	Byte Enable to End of Write	6	–	ns

Notes

7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and transmission line loads. Test conditions for the read cycle use output loading as shown in part (a) of the Figure 2, unless specified otherwise.
8. This part has a voltage regulator which steps down the voltage from 3 V to 2 V internally. t_{power} time has to be provided initially before a read/write operation is started.
9. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, and t_{LZOE}, t_{LZCE}, t_{LZWE}, t_{LZBE} are specified with a load capacitance of 5 pF as in part (b) of Figure 2. Transition is measured ±200 mV from steady-state voltage.
10. These parameters are guaranteed by design and are not tested.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW and $\overline{WE}$ LOW. The chip enables must be active and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
12. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
13. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, and t_{LZOE}, t_{LZCE}, t_{LZWE}, t_{LZBE} are specified with a load capacitance of 5 pF as in part (b) of Figure 2 on page 5. Transition is measured ±200 mV from steady-state voltage.

Switching Waveforms

Figure 3. Read Cycle No. 1 [14, 15]

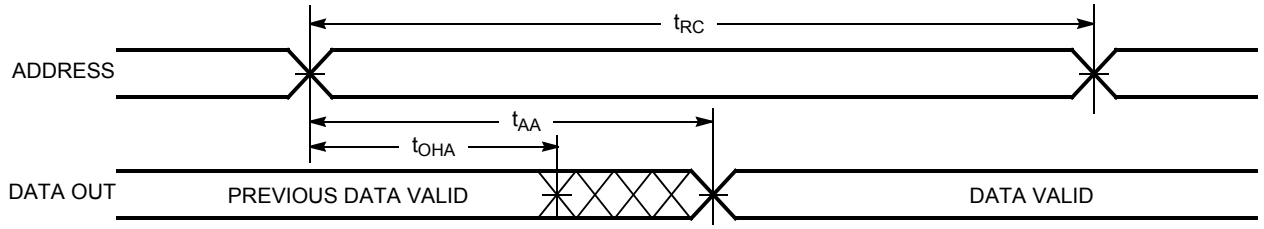


Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled) [15, 16, 17]

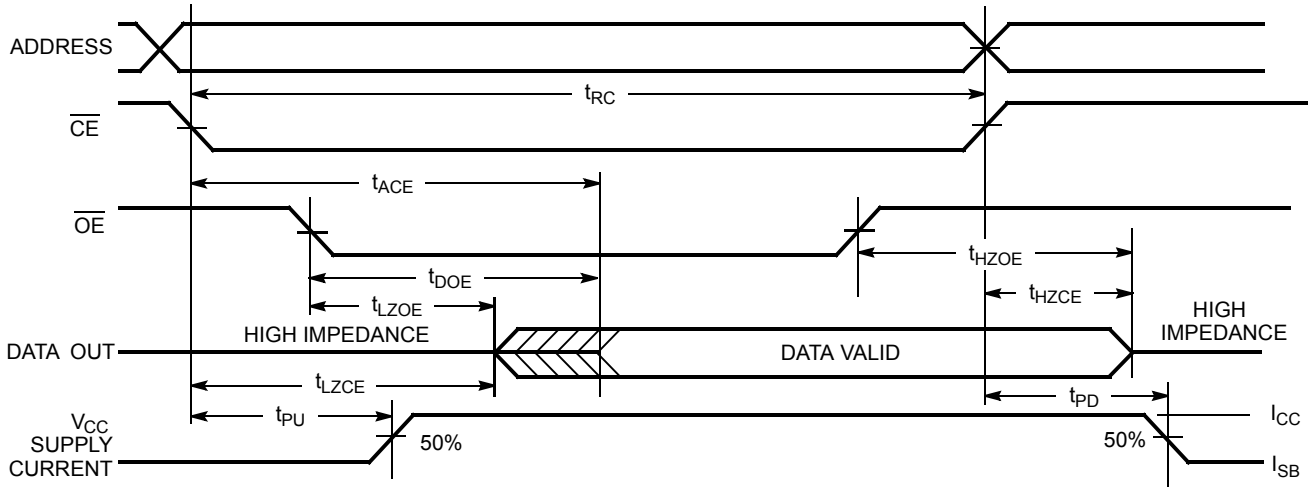
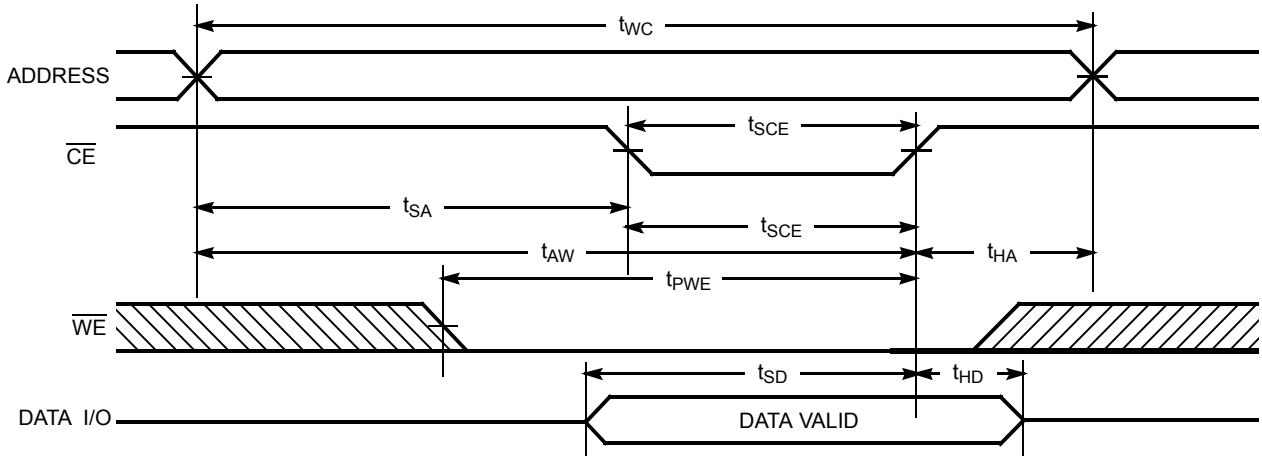


Figure 5. Write Cycle No. 1 ($\overline{CE}$ Controlled) [17, 18, 19]



Notes
14. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
15. $\overline{WE}$ is HIGH for read cycle.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
17. $\overline{CE}$ refers to a combination of $\overline{CE_0}$, $\overline{CE_1}$, and $\overline{CE_2}$. $\overline{CE}$ is active LOW when all three of these signals are active LOW at the same time.
18. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
19. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms *(continued)*

Figure 6. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [20, 21]

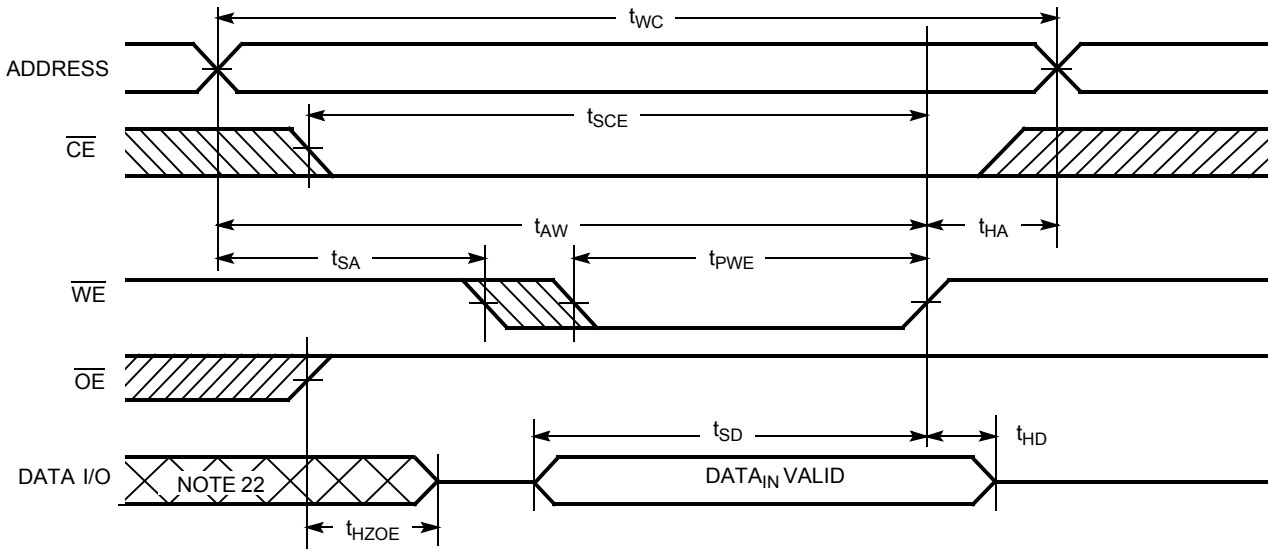
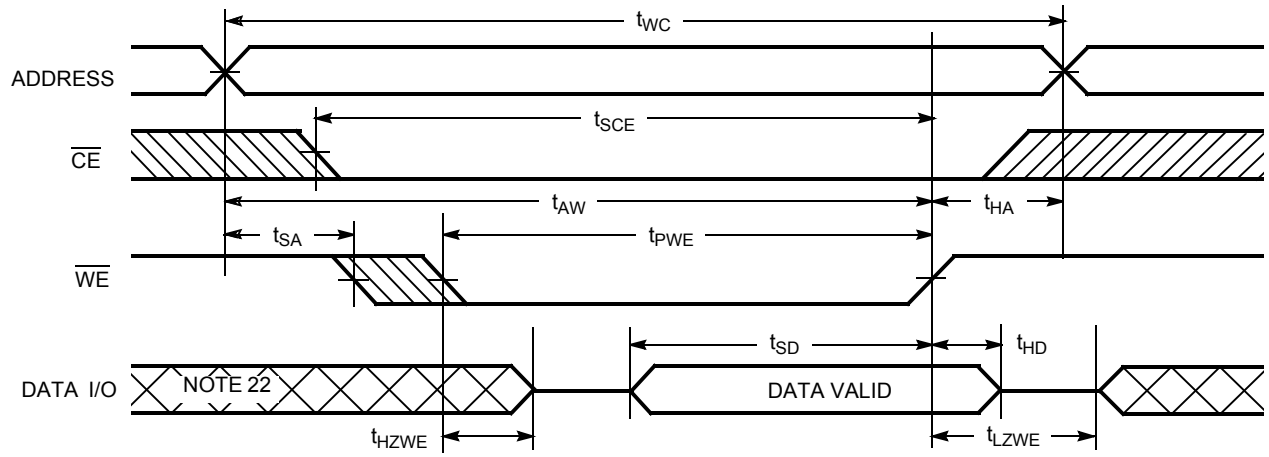


Figure 7. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [21, 23]



Notes
20. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
21. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
22. During this period the I/Os are in the output state and input signals should not be applied.
23. $\overline{CE}$ refers to a combination of $\overline{CE_0}$, CE_1, and CE_2. $\overline{CE}$ is active LOW when all three of these signals are active LOW at the same time.

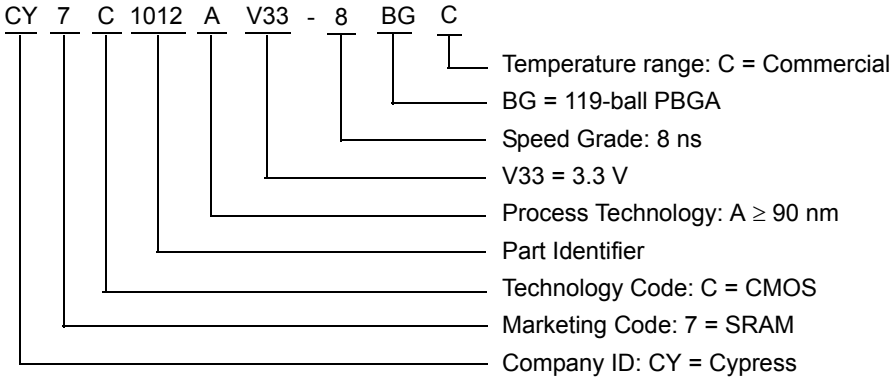
Truth Table

$\overline{CE_0}$	$\overline{CE_1}$	$\overline{CE_2}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_{23}	Mode	Power
H	H	H	X	X	High Z	Power-down	Standby (I_{SB})
L	H	H	L	H	I/O_0–I/O_7 Data Out	Read	Active (I_{CC})
H	L	H	L	H	I/O_8–I/O_{15} Data Out	Read	Active (I_{CC})
H	H	L	L	H	I/O_{16}–I/O_{23} Data Out	Read	Active (I_{CC})
L	L	L	L	H	Full Data Out	Read	Active (I_{CC})
L	H	H	X	L	I/O_0–I/O_7 Data In	Write	Active (I_{CC})
H	L	H	X	L	I/O_8–I/O_{15} Data In	Write	Active (I_{CC})
H	H	L	X	L	I/O_{16}–I/O_{23} Data In	Write	Active (I_{CC})
L	L	L	X	L	Full Data In	Write	Active (I_{CC})
L	L	L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

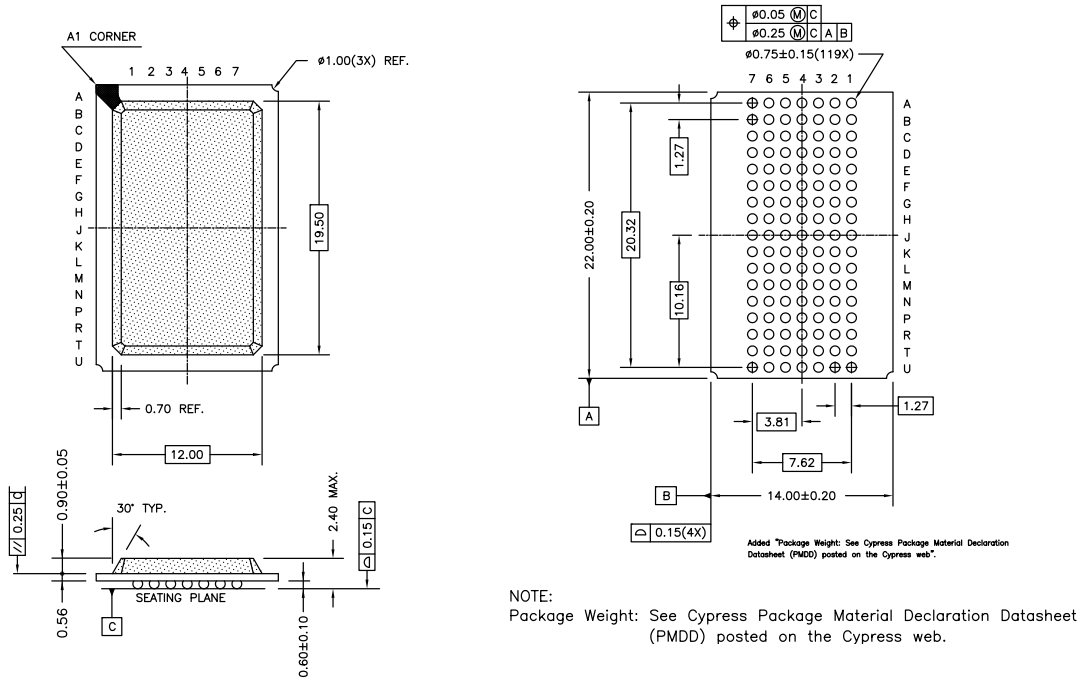
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
8	CY7C1012AV33-8BGC	51-85115	119-ball (14 × 22 × 2.4 mm) PBGA	Commercial

Ordering Code Definitions



Package Diagram

Figure 8. 119-ball PBGA (14 × 22 × 2.4 mm) BG119 Package Outline, 51-85115



NOTE:
Package Weight: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85115 *D

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
I/O	Input/Output
$\overline{OE}$	Output Enable
PBGA	Plastic Ball Grid Array
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
mW	milliwatt
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1012AV33, 512 K × 24 Static RAM Document Number: 38-05254				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	113711	03/11/02	NSL	New data sheet.
*A	117057	07/31/02	DFP	Removed 15-ns bin
*B	117988	09/03/02	DFP	Added 8-ns bin
*C	118992	09/19/02	DFP	Change Cin (input capacitance) from 6 pF to 8 pF Change Cout (output capacitance) from 8 pF to 10 pF
*D	120382	11/15/02	DFP	Final data sheet. Added note 4 to “AC Test Loads and Waveforms”
*E	492137	See ECN	NXR	Removed 12 ns speed bin from product offering Included note #1 and 2 on page #2 Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated Ordering Information Table
*F	2896044	03/19/2010	AJU	Updated Ordering Information Table Updated Package Diagram Added Sales, Solutions, and Legal Information
*G	3097955	11/30/2010	PRAS	Added Ordering Code Definitions. Added Acronyms and Units of Measure. Minor edits.
*H	3086499	06/07/2011	AJU	Updated Selection Guide (Removed -10 column). Updated DC Electrical Characteristics (Removed -10 column). Updated AC Switching Characteristics (Removed -10 column). Updated in new template.
*I	4212876	12/06/2013	VINI	Updated Package Diagram: spec 51-85115 – Changed revision from *C to *D. Updated in new template. Completing Sunset Review.
*J	4573215	11/18/2014	VINI	Added related documentation hyperlink in page 1.

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