

Features

- Pin- and function-compatible with CY7C1046B
- High speed
 - $t_{AA} = 10 \text{ ns}$
- CMOS for optimum speed and power
- Low active power
 - $I_{CC} = 90 \text{ mA}$ at 10 ns
- Low CMOS standby power
 - $I_{SB2} = 10 \text{ mA}$
- Data retention at 2.0 V
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Available in lead-free 400-mil-wide 32-pin SOJ package

Functional Description

The CY7C1046D is a high-performance CMOS static RAM organized as 1M words by 4 bits. Easy memory expansion is

provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and tri-state drivers. Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the four I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{19}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

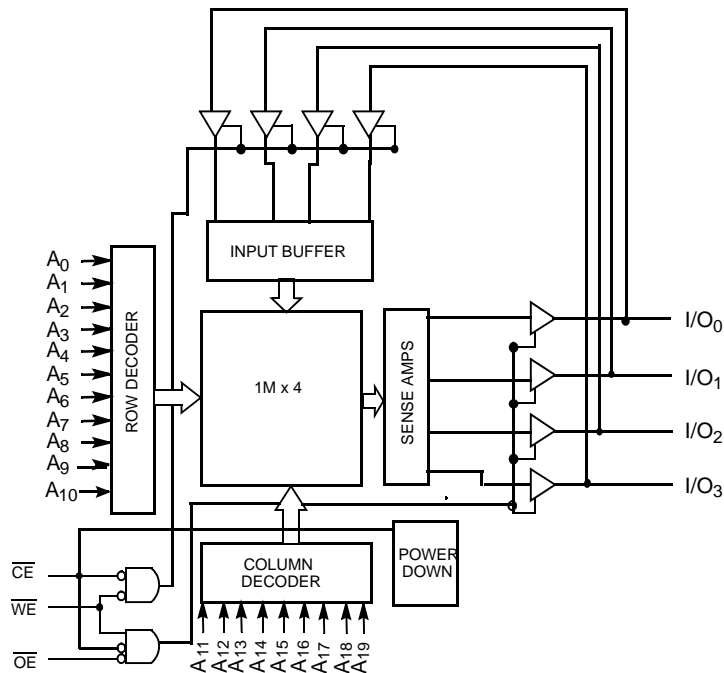
The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1046D is available in a standard 400-mil-wide 32-pin SOJ package with center power and ground (revolutionary) pinout.

The CY7C1046D device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see [Electrical Characteristics on page 4](#) for more details and suggested alternatives.

For a complete list of related documentation, [click here](#).

Logic Block Diagram



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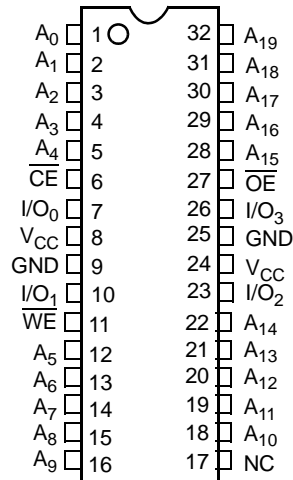
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Selection Guide

Description	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	90	mA
Maximum CMOS Standby Current (mA)	10	mA

Pin Configuration

Figure 1. 32-pin SOJ pinout (Top View)



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to +150 °C
 Ambient temperature with power applied -55 °C to +125 °C
 Supply voltage on V_{CC} to relative GND ^[1] -0.5 V to +6.0 V
 DC voltage applied to outputs in high Z state ^[1] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage ^[1] -0.5 V to $V_{CC} + 0.5$ V
 Current into outputs (LOW) 20 mA
 Static discharge voltage (per MIL-STD-883, method 3015) > 2001 V
 Latch up current > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	-40 °C to +85 °C	4.5 V–5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit	
			Min	Max		
V_{OH}	Output HIGH voltage	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	–	V	
		$V_{CC} = \text{Max}, I_{OH} = -0.1 \text{ mA}$	–	3.4 ^[2]		
V_{OL}	Output LOW voltage	$V_{CC} = \text{Min}, I_{OL} = 8.0 \text{ mA}$	–	0.4	V	
V_{IH}	Input HIGH voltage		2.0	$V_{CC} + 0.5$	V	
V_{IL}	Input LOW voltage ^[1]		-0.5	0.8	V	
I_{IX}	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-1	+1	μA	
I_{OZ}	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$, output disabled	-1	+1	μA	
I_{CC}	V_{CC} operating supply current	$V_{CC} = \text{Max}, f = f_{\text{MAX}} = 1/t_{RC}$	100 MHz	–	90	mA
			83 MHz	–	80	
			66 MHz	–	70	
			40 MHz	–	60	
I_{SB1}	Automatic CE Power-Down Current – TTL inputs	Max V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{\text{MAX}}$	–	20	mA	
I_{SB2}	Automatic CE Power-Down Current – CMOS inputs	Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$, $V_{IN} \geq V_{CC} - 0.3 \text{ V}$, or $V_{IN} \leq 0.3 \text{ V}$, $f = 0$	–	10	mA	

Notes

- $V_{IL}(\text{min}) = -2.0 \text{ V}$ and $V_{IH}(\text{max}) = V_{CC} + 2 \text{ V}$ for pulse durations of less than 20 ns.
- Please note that the maximum V_{OH} limit does not exceed minimum CMOS V_{IH} of 3.5V. If you are interfacing this SRAM with 5V legacy processors that require a minimum V_{IH} of 3.5V, please refer to Application Note [AN6081](#) for technical details and options you may consider.

Capacitance

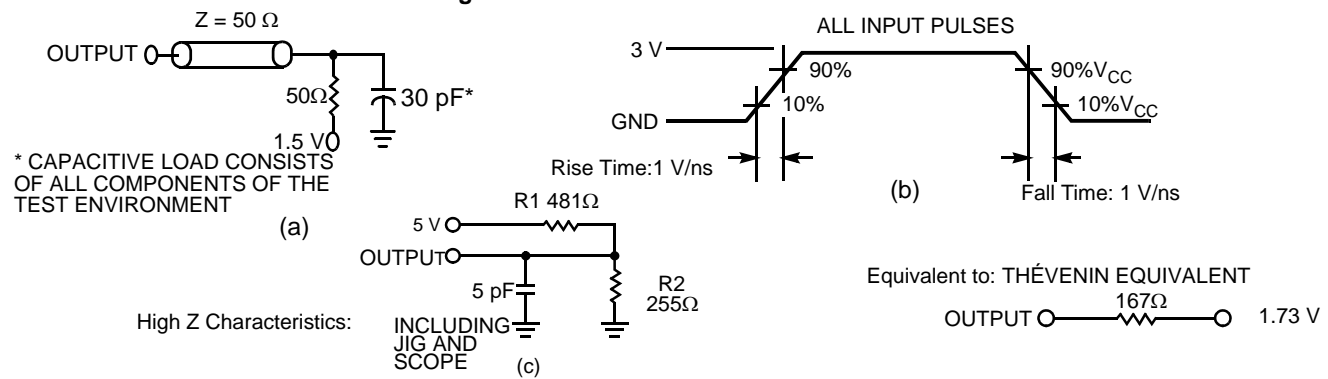
Parameter ^[3]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 5.0 V	8	pF
C _{OUT}	I/O capacitance		8	pF

Thermal Resistance

Parameter ^[3]	Description	Test Conditions	SOJ Package	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	53.44	°C/W
Θ _{JC}	Thermal resistance (junction to case)		38.25	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[4]



Notes

- 3. Tested initially and after any design or process changes that may affect these parameters.
- 4. AC characteristics (except high Z) are tested using the load conditions shown in (a). High Z characteristics are tested for all speeds using the test load shown in (c).

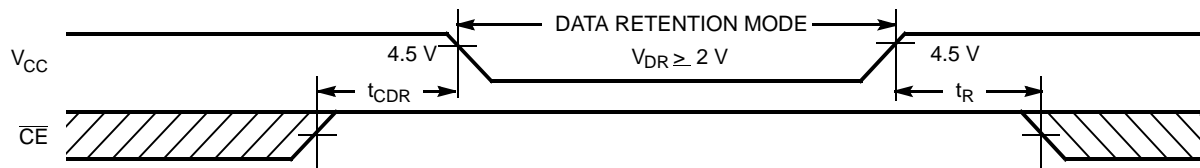
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions ^[5]	Min	Max	Unit
V_{DR}	V_{CC} for data retention		2.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR} = 2.0\text{ V}$, $CE \geq V_{CC} - 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	10	mA
$t_{CDR}^{[6]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[7]}$	Operation recovery time		t_{RC}	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

- No inputs may exceed $V_{CC} + 0.3\text{ V}$.
- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\min)} \geq 50\ \mu\text{s}$ or stable at $V_{CC(\min)} \geq 50\ \mu\text{s}$.

Switching Characteristics

Over the Operating Range

Parameter ^[8]	Description	7C1046D-10		Unit
		Min	Max	
Read Cycle				
t_{power}	V_{CC} (typical) to the first access ^[9]	100	–	μ s
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	\overline{CE} LOW to data valid	–	10	ns
t_{DOE}	\overline{OE} LOW to data valid	–	5	ns
t_{LZOE}	\overline{OE} LOW to low Z ^[11]	0	–	ns
t_{HZOE}	\overline{OE} HIGH to high Z ^[10, 11]	–	5	ns
t_{LZCE}	CE LOW to low Z ^[11]	3	–	ns
t_{HZCE}	\overline{CE} HIGH to high Z ^[10, 11]	–	5	ns
t_{PU}	\overline{CE} LOW to power-up	0	–	ns
t_{PD}	CE HIGH to power-down	–	10	ns
Write Cycle^[12, 13]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	\overline{CE} LOW to write end	7	–	ns
t_{AW}	Address set-up to write end	7	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	\overline{WE} pulse width	7	–	ns
t_{SD}	Data set-up to write end	6	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	\overline{WE} HIGH to low Z ^[11]	3	–	ns
t_{HZWE}	\overline{WE} LOW to high Z ^[10, 11]	–	5	ns

Notes

8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
9. t_{POWER} gives the minimum amount of time that the power supply should be at stable, typical V_{CC} values until the first memory access can be performed.
10. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
12. The internal write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
13. The minimum write cycle time for Write Cycle no. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 4. Read Cycle No. 1 [14, 15]

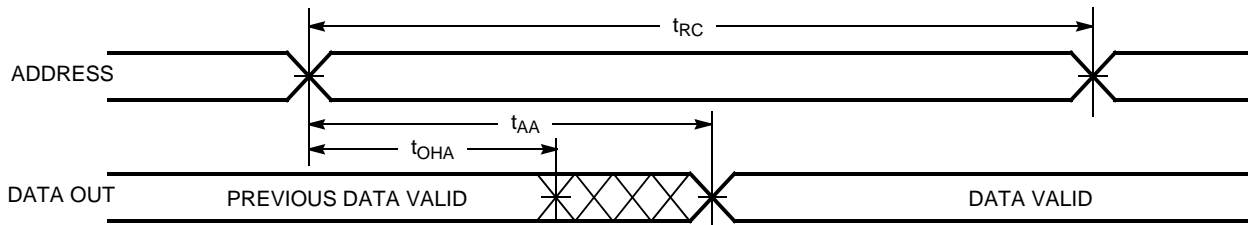
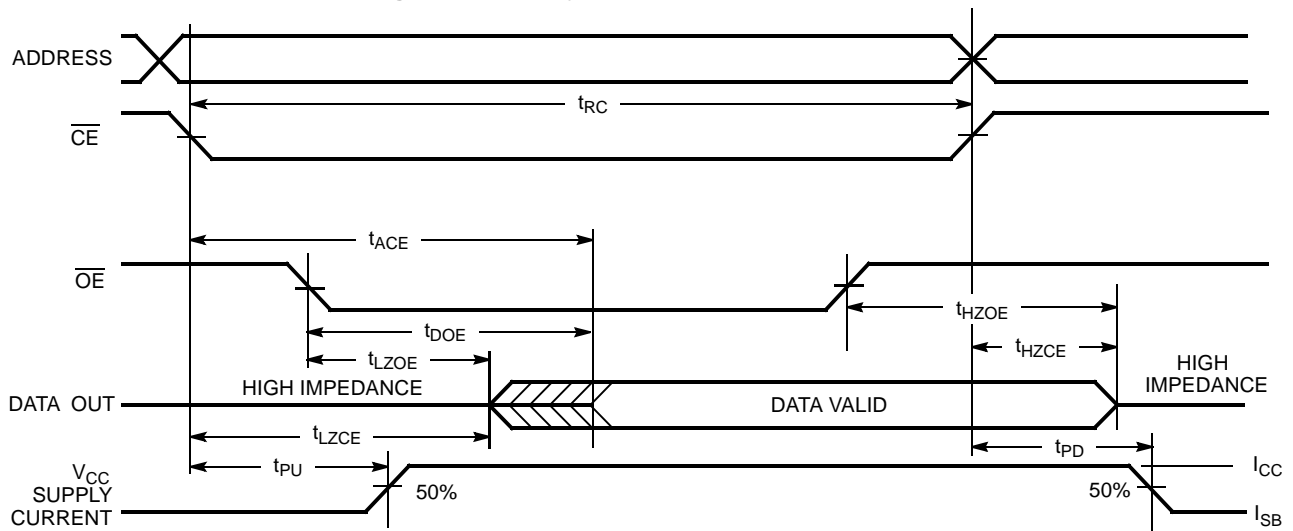


Figure 5. Read Cycle No. 2 (\overline{OE} Controlled) [15, 16]



Notes

- 14. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
- 15. WE is HIGH for read cycle.
- 16. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [17, 18]

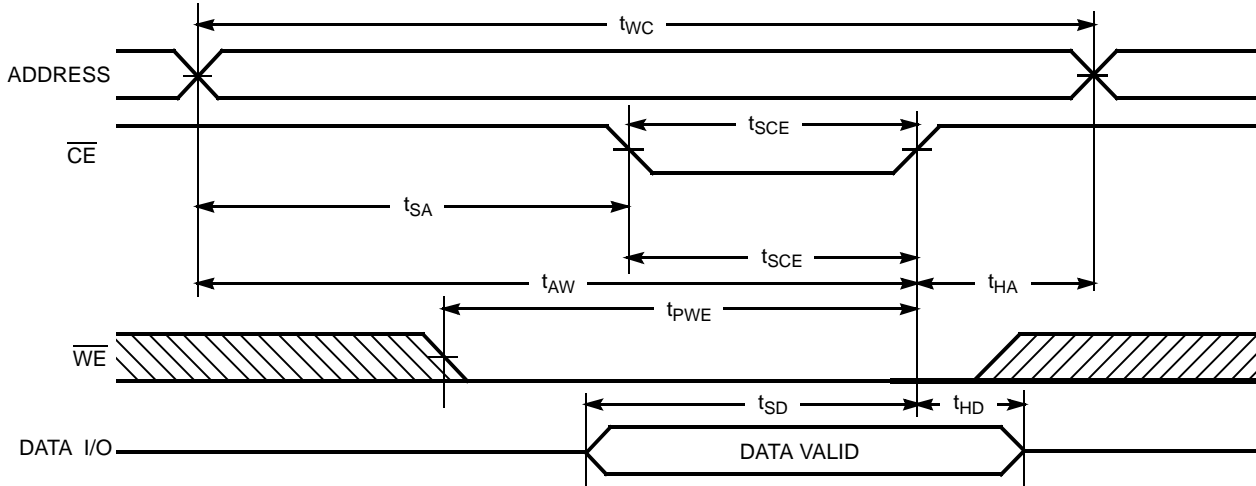
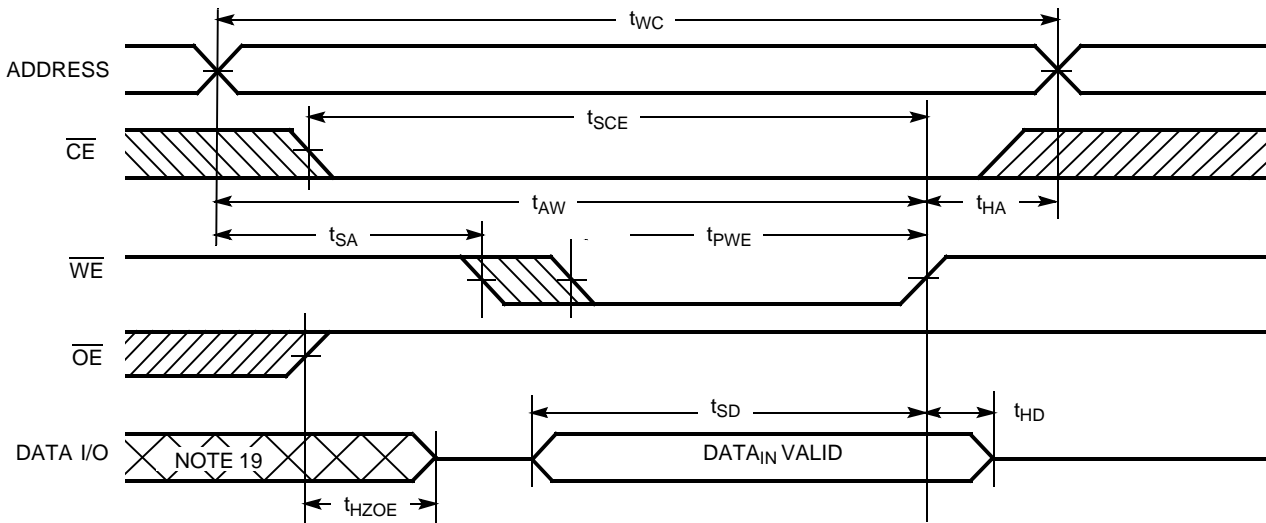


Figure 7. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write) [17, 18]

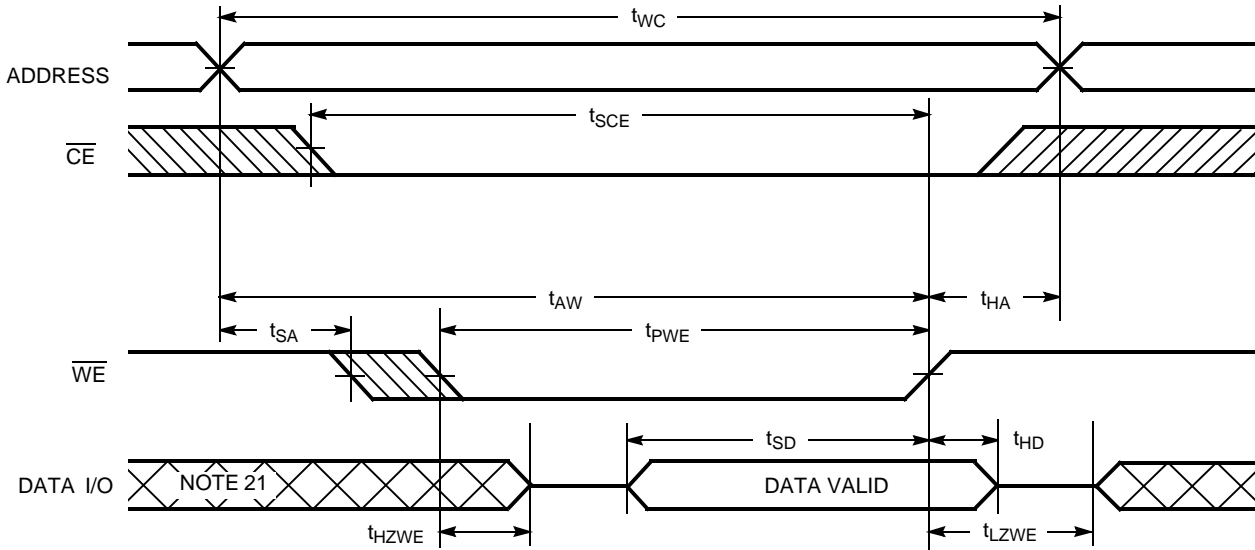


Notes

- 17. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.
- 18. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.
- 19. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [20]



Notes

- 20. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
- 21. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

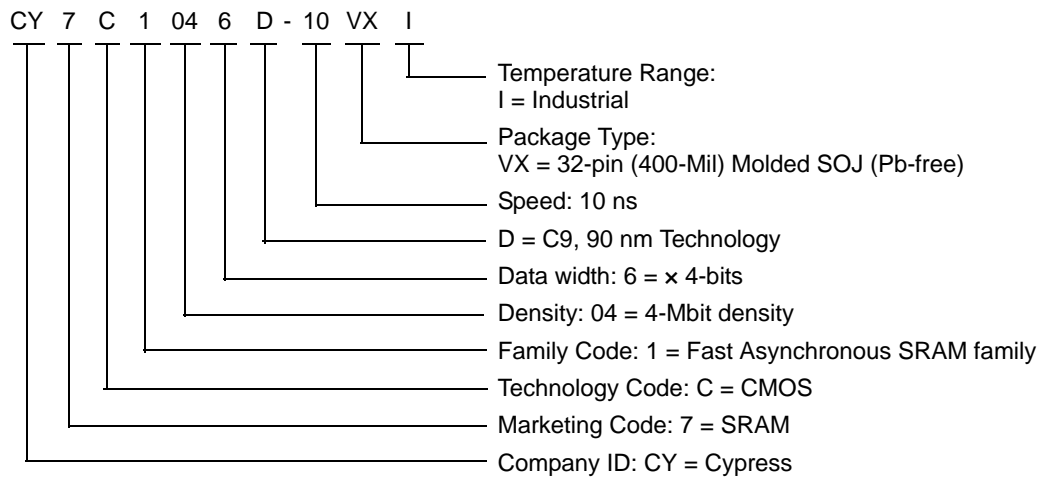
$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O ₀ –I/O ₃	Mode	Power
H	X	X	High Z	Power-down	Standby (I _{SB})
L	L	H	Data Out	Read	Active (I _{CC})
L	X	L	Data In	Write	Active (I _{CC})
L	H	H	High Z	Selected, outputs disabled	Active (I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1046D-10VXI	51-85033	32-pin (400-Mil) Molded SOJ (Pb-free)	Industrial

Please contact your local Cypress sales representative for availability of these parts.

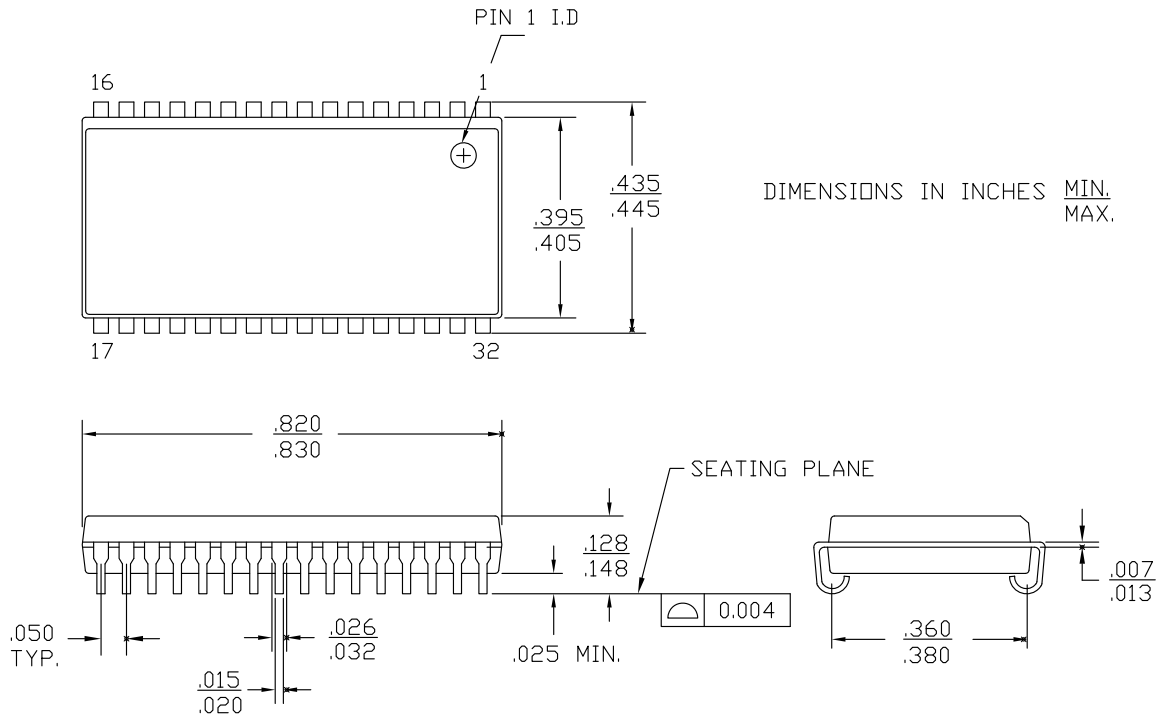
Ordering Code Definitions



Package Diagrams

Figure 9. 32-pin SOJ (400 Mils) V32.4 (Molded SOJ V33) Package Outline, 51-85033

32 Lead (400 MIL) Molded SOJ V33



51-85033 *E

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
\overline{CE}	Chip Enable
I/O	Input/Output
\overline{OE}	Output Enable
SOJ	Small-Outline J-leaded
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
\overline{WE}	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μs	microsecond
μA	microampere
mA	milliampere
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1046D, 4-Mbit (1 M x 4) Static RAM Document Number: 38-05705				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	307613	See ECN	RKF	New data sheet.
*A	399070	See ECN	NXR	<p>Changed from Advance to Preliminary</p> <p>Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court"</p> <p>Removed -20 speed bin</p> <p>Removed L-Version</p> <p>Redefined I_{CC} values for Com'l and Ind'l temperature ranges</p> <p>I_{CC} (Com'l): Changed from 70 and 55 mA to 75 and 70 mA for 12 and 15 ns speed bins respectively</p> <p>I_{CC} (Ind'l): Changed from 80, 70 and 55 mA to 90, 85 and 80 mA for 10, 12 and 15 ns speed bins respectively</p> <p>Added Industrial Operating Range</p> <p>Changed reference voltage level for measurement of Hi-Z parameters from ±500 mV to ±200 mV</p> <p>Changed V_{CC} to 3 V in the Input pulse waveform at the AC Test Loads and Waveforms on page # 3</p> <p>Changed t_{SCE} from 8 to 7 ns for -10 speed bin</p> <p>Added Truth Table</p> <p>Added 10 ns parts in the Ordering Information table</p> <p>Changed part names from V33 to V324 in the Ordering Information Table</p> <p>Shaded Ordering Information Table</p>
*B	459072	See ECN	NXR	<p>Converted from Preliminary to Final.</p> <p>Removed -12 and -15 Speed bins</p> <p>Removed Commercial Operating Range product information.</p> <p>Changed Maximum Rating for supply voltage from 7V to 6V</p> <p>Changed the Capacitance value of input pins and I/O pins from 6 pF to 8 pF</p> <p>Updated the Thermal Resistance table.</p> <p>Changed t_{HZWE} from 6 ns to 5 ns</p> <p>Added footnote #4 and 11</p> <p>Updated footnote #7 on High-Z parameter measurement</p> <p>Updated the Ordering Information and replaced Package Name column with Package Diagram in the Ordering Information table.</p>
*C	3059162	10/14/2010	PRAS	<p>Added Ordering Code Definitions.</p> <p>Updated Package Diagrams.</p>
*D	3098812	12/01/2010	PRAS	<p>Added Acronyms and Units of Measure.</p> <p>Minor edits and updated in new template.</p>
*E	3446913	11/24/2011	TAVA	<p>Removed Note referring to SRAM System Guidelines application note on page 1.</p> <p>Updated test conditions for IIX parameter.</p>
*F	4039540	06/25/2013	MEMJ	<p>Updated Functional Description.</p> <p>Updated Electrical Characteristics:</p> <p>Added one more Test Condition "V_{CC} = Max, I_{OH} = -0.1 mA" for V_{OH} parameter and added maximum value corresponding to that Test Condition.</p> <p>Added Note 2 and referred the same note in maximum value for V_{OH} parameter corresponding to Test Condition "V_{CC} = Max, I_{OH} = -0.1 mA".</p>
*G	4574311	11/20/2014	MEMJ	<p>Added related documentation hyperlink in page 1.</p> <p>Updated Figure 9 in Package Diagrams (spec 51-85033 *D to *E).</p>

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