

1:2 CML Fanout Buffer with Selectable Clock Input

Features

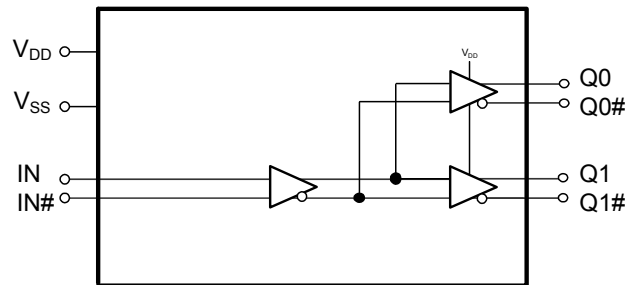
- One current mode logic (CML), High-speed current steering logic (HCSL), or low-voltage positive emitter-coupled logic (LVPECL) input pair distributed to two CML output pairs
- 20-ps maximum output-to-output skew
- 480-ps maximum propagation delay
- 0.15-ps maximum additive RMS phase jitter at 156.25 MHz (12-kHz to 20-MHz offset)
- Up to 1.5 GHz operation
- 8-pin thin shrunk small outline package (TSSOP) package
- 2.5-V or 3.3-V operating voltage ^[1]
- Commercial and industrial operating temperature range

Functional Description

The CY2DM1502 is an ultra-low noise, low-skew, low-propagation delay 1:2 CML, HCSL, or LVPECL to CML fanout buffer targeted to meet the requirements of high-speed clock distribution applications. The device has a fully differential internal architecture that is optimized to achieve low additive jitter and low skew at operating frequencies of up to 1.5 GHz.

For a complete list of related documentation, [click here](#).

Logic Block Diagram



Note

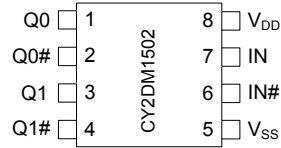
1. Input AC-coupling capacitors are required for voltage-translation applications.

Contents

Pinouts	3	Acronyms	11
Pin Definitions	3	Document Conventions	11
Absolute Maximum Ratings	4	Units of Measure	11
Operating Conditions	4	Document History Page	12
DC Electrical Specifications	5	Sales, Solutions, and Legal Information	14
Thermal Resistance	5	Worldwide Sales and Design Support	14
AC Electrical Specifications	6	Products	14
Ordering Information	9	PSoC@Solutions	14
Ordering Code Definitions	9	Cypress Developer Community	14
Package Diagram	10	Technical Support	14

Pinouts

Figure 1. 8-pin TSSOP Package pinout



Pin Definitions

Pin No.	Pin Name	Pin Type	Description
1, 3	Q(0:1)	Output	CML output clocks
2, 4	Q(0:1)#	Output	CML complementary output clocks
5	V _{SS}	Power	Ground
6	IN#	Input	CML/HCSL/LVPECL complementary input clock
7	IN	Input	CML/HCSL//LVPECL input clock
8	V _{DD}	Power	Power supply

Absolute Maximum Ratings

Parameter	Description	Condition	Min	Max	Unit
V _{DD}	Supply voltage	Nonfunctional	-0.5	4.6	V
V _{IN} ^[2]	Input voltage, relative to V _{SS}	Nonfunctional	-0.5	lesser of 4.0 or V _{DD} + 0.4	V
V _{OUT} ^[2]	DC output or I/O voltage, relative to V _{SS}	Nonfunctional	-0.5	lesser of 4.0 or V _{DD} + 0.4	V
T _S	Storage temperature	Nonfunctional	-55	150	°C
ESD _{HBM}	Electrostatic discharge (ESD) protection (Human body model)	JEDEC STD 22-A114-B	2000	-	V
L _U	Latch up		Meets or exceeds JEDEC Spec JESD78B IC Latch-up Test		
UL-94	Flammability rating	At 1/8 in	V-0		
MSL	Moisture sensitivity level		3		

Operating Conditions

Parameter	Description	Condition	Min	Max	Unit
V _{DD}	Supply voltage	2.5-V supply	2.375	2.625	V
		3.3-V supply	3.135	3.465	V
T _A	Ambient operating temperature	Commercial	0	70	°C
		Industrial	-40	85	°C
t _{PU}	Power ramp time	Power-up time for V _{DD} to reach minimum specified voltage (power ramp must be monotonic).	0.05	500	ms

Note

2. The voltage on any I/O pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.

DC Electrical Specifications

($V_{DD} = 3.3\text{ V} \pm 5\%$ or $2.5\text{ V} \pm 5\%$; $T_A = 0\text{ }^\circ\text{C}$ to $70\text{ }^\circ\text{C}$ (Commercial) or $-40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$ (Industrial))

Parameter	Description	Condition	Min	Max	Unit
I_{DD}	Operating supply current	All CML outputs floating (internal I_{DD})	–	50	mA
V_{IH}	Input high voltage, CML/HCSL/LVPECL inputs IN and IN#		–	$V_{DD} + 0.3$	V
V_{IL}	Input low voltage, CML/HCSL/LVPECL inputs IN and IN#		–0.3	–	V
V_{ID} ^[3]	Input differential amplitude	See Figure 2 on page 7	0.4	1.0	V
V_{ICM}	Input common mode voltage	See Figure 2 on page 7	0.2	$V_{DD} - 0.2$	V
I_{IH}	Input high current, CML/HCSL/LVPECL inputs IN and IN#	Input = V_{DD} ^[4]	–	150	μA
I_{IL}	Input low current, CML/HCSL/LVPECL inputs IN and IN#	Input = V_{SS} ^[4]	–150	–	μA
V_{OH}	CML output high voltage	Terminated with $50\ \Omega$ to V_{DD} ^[5]	$V_{DD} - 0.1$	–	V
V_{OL}	CML output low voltage	Terminated with $50\ \Omega$ to V_{DD} ^[5]	$V_{DD} - 0.7$	$V_{DD} - 0.3$	V
C_{IN}	Input capacitance	Measured at 10 MHz; per pin	–	3	pF

Thermal Resistance

Parameter ^[6]	Description	Test Conditions	8-pin TSSOP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	162	$^\circ\text{C}/\text{W}$
θ_{JC}	Thermal resistance (junction to case)		29	$^\circ\text{C}/\text{W}$

Notes

- V_{ID} minimum of 400 mV is required to meet all output AC Electrical Specifications. The device is functional with V_{ID} minimum of greater than 200 mV.
- Positive current flows into the input pin, negative current flows out of the input pin.
- Refer to [Figure 3 on page 7](#).
- These parameters are guaranteed by design and are not tested.

AC Electrical Specifications

($V_{DD} = 3.3\text{ V} \pm 5\%$ or $2.5\text{ V} \pm 5\%$; $T_A = 0\text{ }^\circ\text{C}$ to $70\text{ }^\circ\text{C}$ (Commercial) or $-40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$ (Industrial))

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{IN}	Input frequency		DC	–	1.5	GHz
F_{OUT}	Output frequency	$F_{OUT} = F_{IN}$	DC	–	1.5	GHz
V_{PP}	CML differential output voltage peak-to-peak, single-ended. Terminated with $50\ \Omega$ to V_{DD} ^[5]	$F_{out} = \text{DC to } 150\text{ MHz}$	250	–	700	mV
		$F_{out} = >150\text{ MHz to } 1.5\text{ GHz}$	250	–	600	mV
t_{PD} ^[7]	Propagation delay input pair to output pair	Input rise/fall time < 1.5 ns (20% to 80%)	–	–	480	ps
t_{ODC} ^[8]	Output duty cycle	50% duty cycle at input Frequency range up to 1 GHz	48	–	52	%
t_{SK1} ^[9]	Output-to-output skew	Any output to any output, with same load conditions at DUT	–	–	20	ps
t_{SK1D} ^[9]	Device-to-device output skew	Any output to any output between two or more devices. Devices must have the same input and have the same output load.	–	–	150	ps
PN_{ADD}	Additive RMS phase noise 156.25-MHz Input Rise/fall time < 150 ps (20% to 80%) $V_{ID} > 400\text{ mV}$	Offset = 1 kHz	–	–	–120	dBc/Hz
		Offset = 10 kHz	–	–	–130	dBc/Hz
		Offset = 100 kHz	–	–	–135	dBc/Hz
		Offset = 1 MHz	–	–	–145	dBc/Hz
		Offset = 10 MHz	–	–	–153	dBc/Hz
		Offset = 20 MHz	–	–	–155	dBc/Hz
t_{JIT} ^[10]	Additive RMS phase jitter (Random)	156.25 MHz, 12 kHz to 20 MHz offset; input rise/fall time < 150 ps (20% to 80%), $V_{ID} > 400\text{ mV}$	–	–	0.15	ps
t_R, t_F ^[11]	Output rise/fall time	50% duty cycle at input, 20% to 80% of full swing (V_{OL} to V_{OH}) Input rise/fall time < 1.5 ns (20% to 80%) Measured at 1 GHz	–	–	250	ps

Notes

7. Refer to [Figure 4 on page 7](#).
8. Refer to [Figure 5 on page 7](#).
9. Refer to [Figure 6 on page 8](#).
10. Refer to [Figure 7 on page 8](#).
11. Refer to [Figure 8 on page 8](#).

Figure 2. Input Differential and Common Mode Voltages

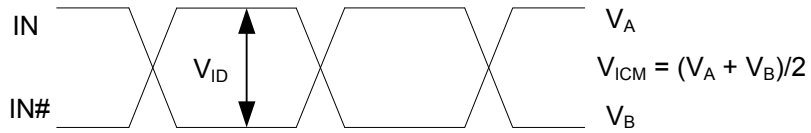


Figure 3. Output Differential Voltage

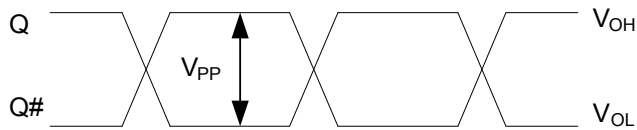


Figure 4. Input to Any Output Pair Propagation Delay

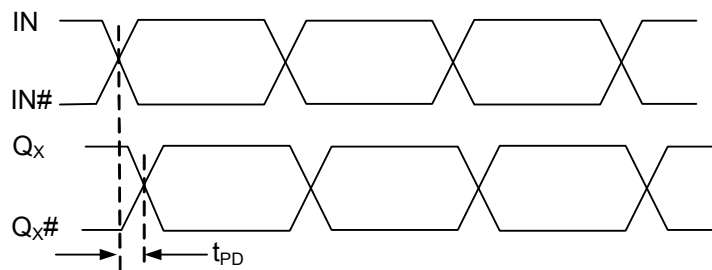


Figure 5. Output Duty Cycle

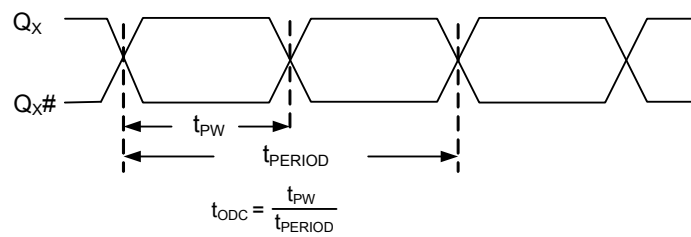


Figure 6. Output-to-Output and Device-to-Device Skew

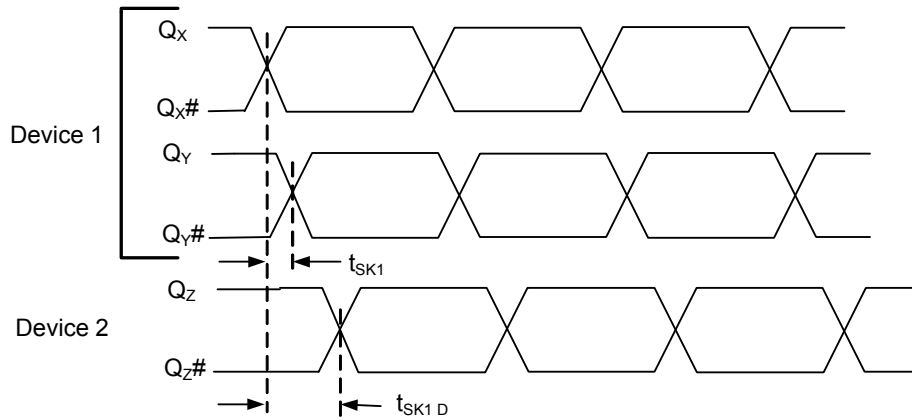


Figure 7. RMS Phase Jitter

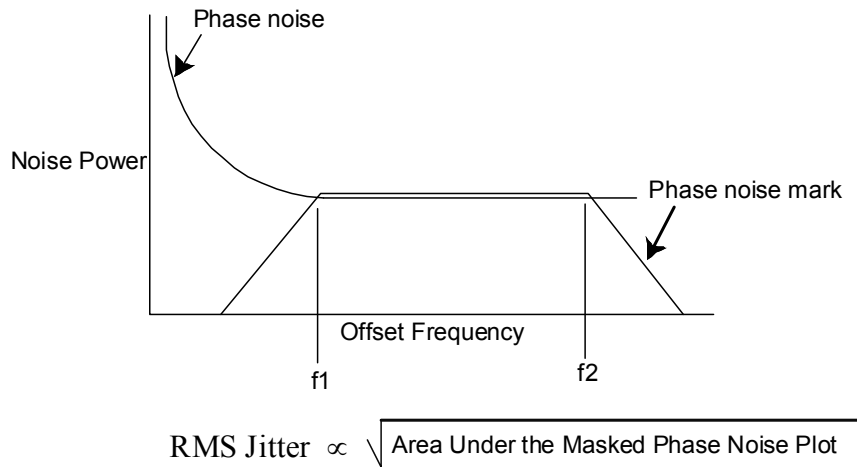
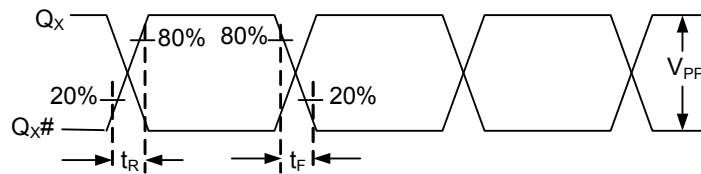


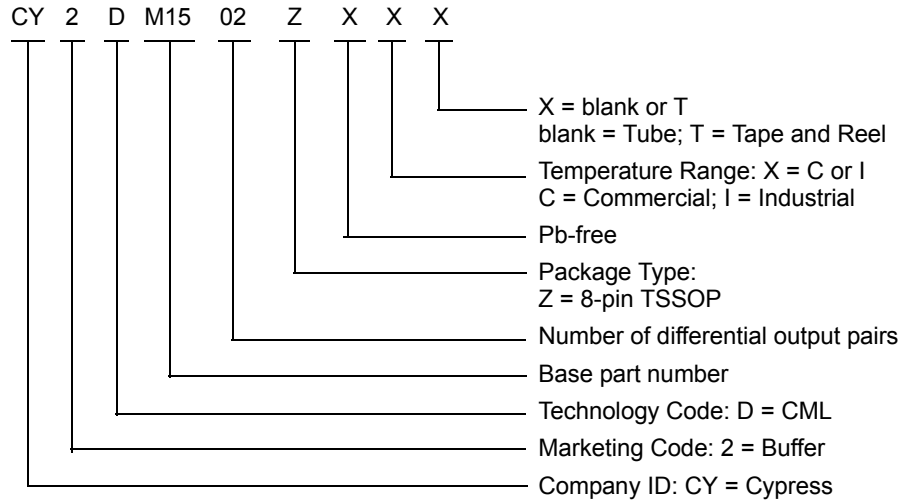
Figure 8. Output Rise/Fall Time



Ordering Information

Part Number	Type	Production Flow
Pb-free		
CY2DM1502ZXI	8-pin TSSOP	Industrial, -40 °C to 85 °C
CY2DM1502ZXIT	8-pin TSSOP tape and reel	Industrial, -40 °C to 85 °C

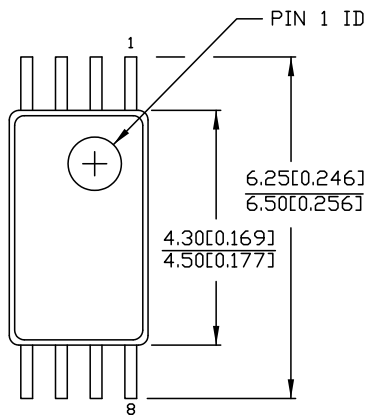
Ordering Code Definitions



Package Diagram

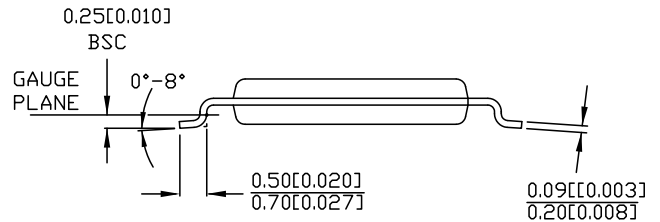
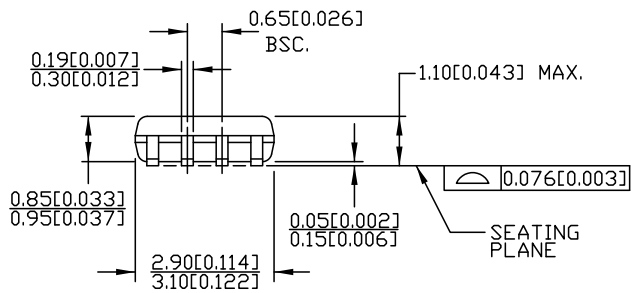
Figure 9. 8-pin TSSOP (4.40 MM Body) Z08.173/ZZ08.173 Package Outline, 51-85093

8 Lead TSSOP 4.40 MM BODY



DIMENSIONS IN MM[INCHES] MIN.
MAX.
REFERENCE JEDEC MO-153

PART #	
Z08.173	STANDARD PKG.
ZZ08.173	LEAD FREE PKG.



51-85093 *E

Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
CML	current mode logic
ESD	electrostatic discharge
HBM	human body model
HCSL	high-speed current steering logic
JEDEC	joint electron devices engineering council
LVDS	low-voltage differential signal
LVC MOS	low-voltage complementary metal oxide semiconductor
LVPECL	low-voltage positive emitter-coupled logic
RMS	root mean square
TSSOP	thin shrunk small outline package

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dBc	decibels relative to the carrier
GHz	gigahertz
Hz	hertz
kΩ	kilohm
μA	microampere
μF	microfarad
μs	microsecond
mA	milliampere
ms	millisecond
mV	millivolt
MHz	megahertz
ns	nanosecond
Ω	ohm
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY2DM1502, 1:2 CML Fanout Buffer with Selectable Clock Input				
Document Number: 001-56315				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2782891	CXQ	10/09/09	New Datasheet.
*A	2838916	CXQ	01/05/2010	<p>Changed status from "ADVANCE" to "PRELIMINARY".</p> <p>Changed from 0.34 ps to 0.25 ps maximum additive jitter in "Features" on page 1 and in t_{JIT} in the AC Electrical Specs table on page 4.</p> <p>Added t_{PU} spec to the Operating Conditions table on page 2.</p> <p>Removed V_{OH} spec maximum of V_{DD} in the DC Electrical Specs table on page 3.</p> <p>Changed V_{OL} spec min from $V_{DD} - 0.6V$ to $V_{DD} - 0.7V$; changed max from $V_{DD} - 0.4V$ to $V_{DD} - 0.3V$ in the DC Electrical Specs table on page 3.</p> <p>Removed V_{OD} spec of minimum 300 mV, maximum 450 mV in the DC Electrical Specs table on page 3.</p> <p>Added R_P spec in the DC Electrical Specs table on page 3. Min = 60 kΩ, Max = 140 kΩ.</p> <p>Added a measurement definition for C_{IN} in the DC Electrical Specs table on page 3.</p> <p>Added V_{PP} spec to the AC Electrical Specs table on page 4. V_{PP} max = 700 mV for DC - 150 MHz and max = 600 mV for 150 MHz to 1.5 GHz. V_{PP} min = 250 mV over the entire range.</p> <p>Changed letter case and some names of all the timing parameters in the AC Electrical Specs table on page 4 to be consistent with EROS.</p> <p>Lowered all additive phase noise mask specs by 3 dB in in the AC Electrical Specs table on page 4.</p> <p>Added condition to t_R and t_F specs in the AC Electrical specs table on page 4 that input rise/fall time must be less than 1.5 ns (20% to 80%).</p> <p>Changed letter case and some names of all the timing parameters in Figures 3, 4, 5, 6 and 8, to be consistent with EROS.</p>
*B	3011766	CXQ	08/20/2010	<p>Changed from 0.25 ps to 0.11 ps maximum additive jitter in "Features" on page 1 and in t_{JIT} in the AC Electrical Specs table.</p> <p>Added note 3 to describe I_{IH} and I_{IL} specs.</p> <p>Removed reference to data distribution from "Functional Description".</p> <p>Changed R_P for diff inputs from 100 kΩ to 150 kΩ in the Logic Block Diagram and from 60 kΩ min / 140 kΩ max to 90 kΩ min / 210 kΩ max in the DC Electrical Specs table.</p> <p>Added max V_{ID} of 1.0V in DC Electrical Specs table.</p> <p>Updated phase noise specs for 1 k/10 k/100 k/1 M/10 M/20 MHz offset to -120/-130/-135/-150/-150/-150dBc/Hz, respectively, in the AC Electrical Specs table.</p> <p>Added "Frequency range up to 1 GHz" condition to t_{ODC} spec.</p> <p>Updated package diagram.</p> <p>Added Acronyms and Ordering Code Definition.</p>
*C	3017258	CXQ	08/27/2010	Corrected Output Rise/Fall time diagram.
*D	3100234	CXQ	11/18/2010	<p>Updated Phase jitter to 0.15ps max from 0.11ps max.</p> <p>Changed V_{IN} and V_{OUT} specs from 4.0V to "lesser of 4.0 or $V_{DD} + 0.4$"</p> <p>Removed 200mA min LU spec, replaced with "Meets or exceeds JEDEC Spec JESD78B IC Latchup Test"</p> <p>Removed R_P spec for differential input clock pins IN_X and $IN_X\#$.</p> <p>Changed C_{IN} condition to "Measured at 10 MHz".</p> <p>Changed PN_{ADD} specs for 1MHz, 10MHz, and 20MHz offsets.</p> <p>Added condition "Measured at 1 GHz" to t_R, t_F specs.</p>
*E	3137726	CXQ	01/13/2011	<p>Removed "Preliminary" status heading.</p> <p>Removed resistors from $IN/IN\#$ in Logic Block Diagram.</p>
*F	3090938	CXQ	02/25/2011	Post to external web.

Document History Page (continued)

Document Title: CY2DM1502, 1:2 CML Fanout Buffer with Selectable Clock Input Document Number: 001-56315				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*G	3410372	PURU	10/18/2011	Adding HCSL to Features , Functional Description , Pin Definitions , and DC Electrical Specifications sections. The min value of V_{ICM} is changed from 0.5 to 0.2 in DC Electrical Specifications .
*H	3878396	PURU	01/21/2013	Updated to new template.
*I	4587249	PURU	12/04/2014	Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end. Updated Ordering Information : Removed the prune part numbers CY2DM1502ZXC and CY2DM1502ZXCT. Updated Package Diagram : spec 51-85093 – Changed revision from *D to *E.
*J	5272915	PSR	05/16/2016	Added Thermal Resistance . Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2009-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.