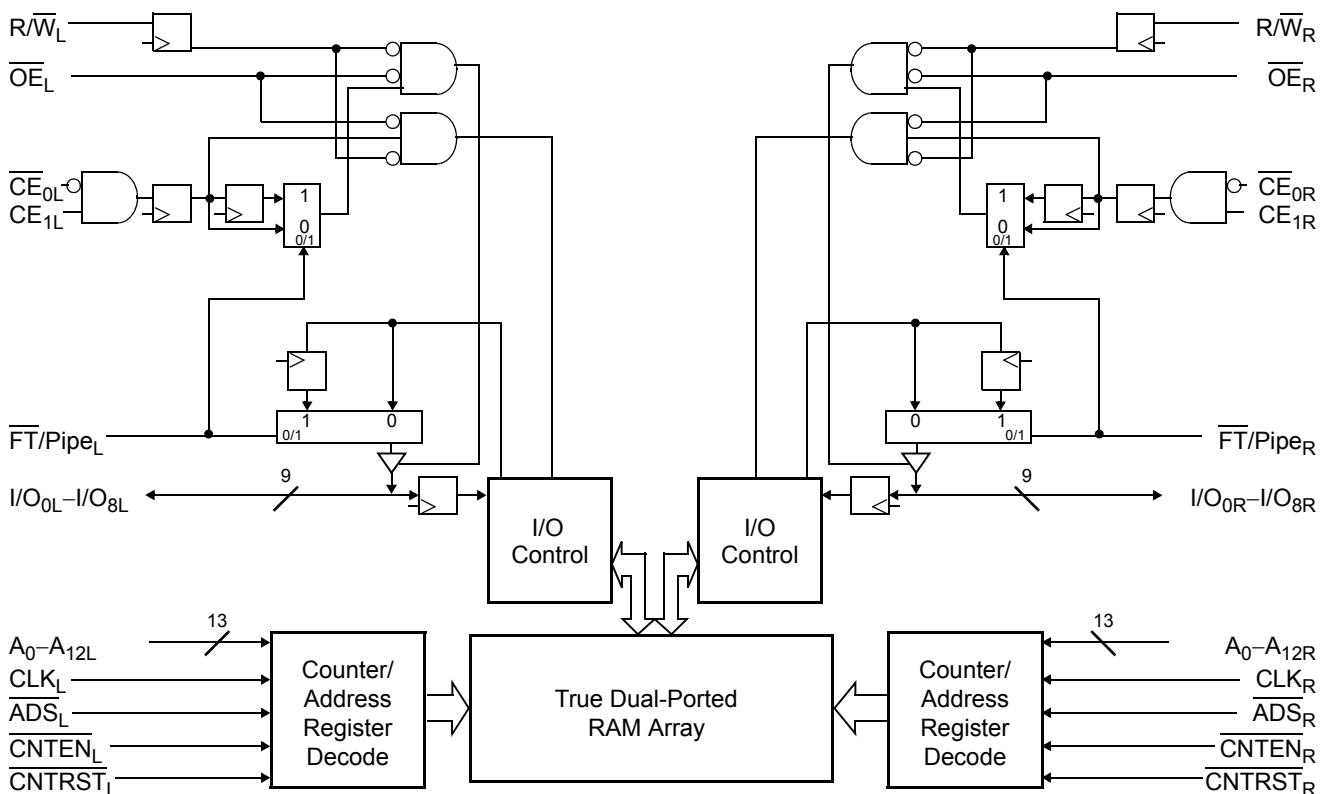


3.3-V 8 K × 9
Synchronous Dual Port Static RAM

Features

- True dual-ported memory cells which allow simultaneous access of the same memory location
 - Flow-through/Pipelined device
 - 8 K × 9 organization (CY7C09159AV)
 - Three Modes
 - Flow-through
 - Pipelined
 - Burst
 - Pipelined output mode on both ports allows fast 67-MHz operation
 - 0.35-micron complementary metal oxide semiconductor (CMOS) for optimum speed/power
 - High-speed clock to data access 9 ns (max.)
 - 3.3 V Low operating power
 - Active = 135 mA (typical)
 - Standby = 10 μA (typical)
 - Fully synchronous interface for easier operation
 - Burst counters increment addresses internally
 - Shorten cycle times
 - Minimize bus noise
 - Supported in Flow-through and Pipelined modes
 - Dual chip enables for easy depth expansion
 - Automatic power-down
 - Commercial temperature ranges
 - Available in 100-pin thin quad plastic flatpack (TQFP)
 - Pb-free packages available
- For a complete list of related documentation, [click here](#).

Logic Block Diagram



Functional Description

The CY7C09159AV is a high-speed synchronous CMOS 8 K × 9 dual-port static RAM. Two ports are provided, permitting independent, simultaneous access for reads and writes to any location in memory.^[1] Registers on control, address, and data lines allow for minimal setup and hold times. In pipelined output mode, data is registered for decreased cycle time. Clock to data valid $t_{CD2} = 9$ ns (pipelined). Flow-through mode can also be used to bypass the pipelined output register to eliminate access latency. In flow-through mode data will be available $t_{CD1} = 20$ ns after the address is clocked into the device. Pipelined output or flow-through mode is selected via the FT/Pipe pin.

Each port contains a burst counter on the input address register. The internal write pulse width is independent of the LOW- to-HIGH transition of the clock signal. The internal write pulse is self-timed to allow the shortest possible cycle times.

A HIGH on \overline{CE}_0 or LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce the static power consumption. The use of multiple Chip Enables allows easier

banking of multiple chips for depth expansion configurations. In the pipelined mode, one cycle is required with \overline{CE}_0 LOW and CE_1 HIGH to reactivate the outputs.

Counter enable inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for fast interleaved memory applications. A port's burst counter is loaded with the port's Address Strobe (ADS). When the port's Count Enable (\overline{CNTEN}) is asserted, the address counter will increment on each LOW-to-HIGH transition of that port's clock signal. This will read/write one word from/into each successive address location until \overline{CNTEN} is deasserted. The counter can address the entire memory array and will loop back to the start. Counter Reset (\overline{CNTRST}) is used to reset the burst counter.

All parts are available in 100-pin thin quad plastic flatpack (TQFP) packages.

Note

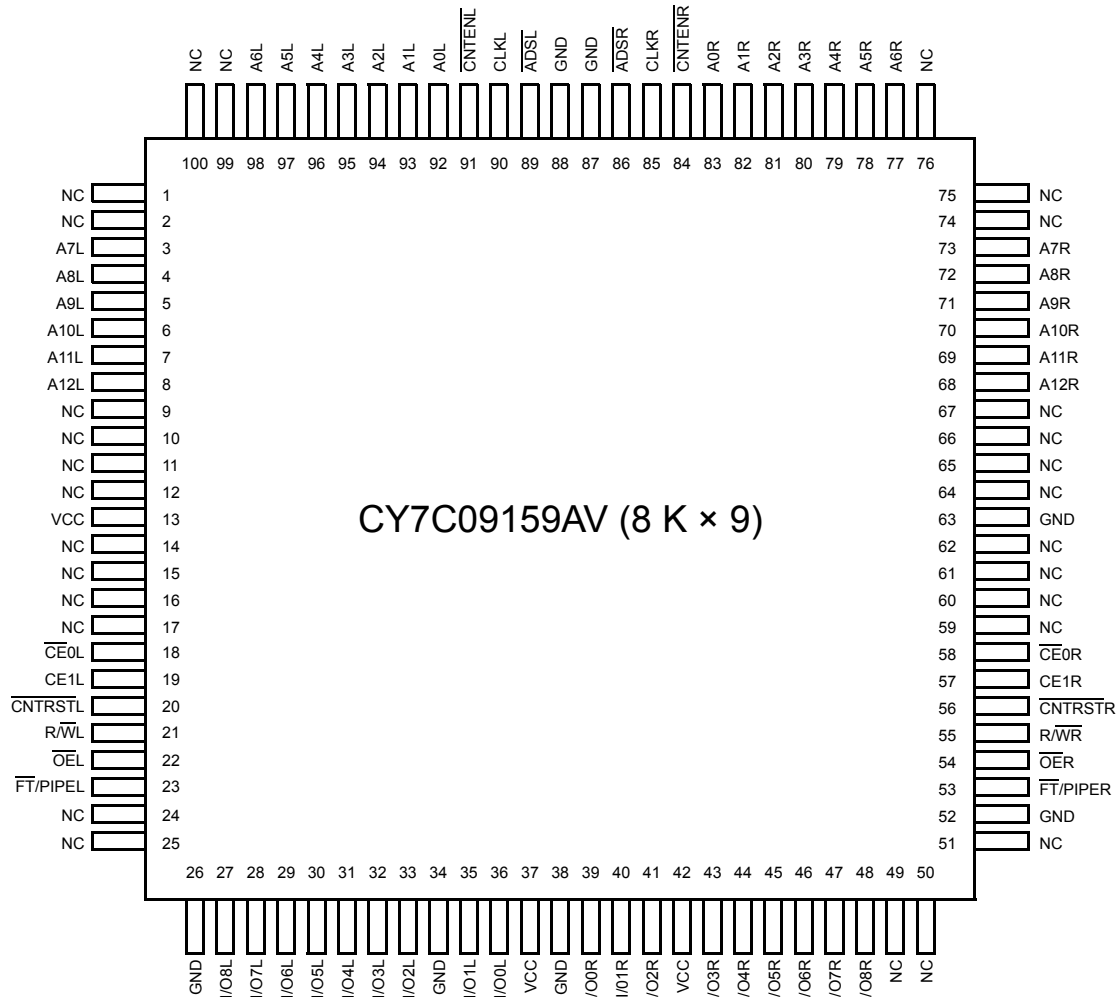
1. When simultaneously writing to the same location, final value cannot be guaranteed.

Contents

| | | | |
|---------------------------------------|----------|--|-----------|
| Pin Configuration | 4 | Switching Waveforms | 8 |
| 100-Pin TQFP (Top View) | 4 | Ordering Information | 16 |
| Selection Guide | 4 | Ordering Code Definitions | 16 |
| Pin Definitions | 5 | Package Diagram | 17 |
| Maximum Ratings | 5 | Acronyms | 17 |
| Operating Range | 5 | Document Conventions | 17 |
| Electrical Characteristics | | Units of Measure | 17 |
| Over the Operating Range | 6 | Document History Page | 18 |
| Capacitance | 6 | Sales, Solutions, and Legal Information | 19 |
| AC Test Loads | 6 | Worldwide Sales and Design Support | 19 |
| Switching Characteristics | | Products | 19 |
| Over the Operating Range | 7 | PSoC Solutions | 19 |

Pin Configuration

100-Pin TQFP (Top View)



Selection Guide

| | CY7C09159AV -9 | Unit |
|---|---------------------------|-------------|
| f_{MAX2} (Pipelined) | 67 | MHz |
| Max access time (clock to data, pipelined) | 9 | ns |
| Typical operating current I_{CC} | 135 | mA |
| Typical standby current for I_{SB1} (Both ports TTL level) | 20 | mA |
| Typical standby current for I_{SB3} (Both ports CMOS level) | 10 | μ A |

Pin Definitions

| Left Port | Right Port | Description |
|--------------------------------------|--------------------------------------|--|
| A _{0L} -A _{12L} | A _{0R} -A _{12R} | Address inputs (A ₀ -A ₁₂ for 8 K devices). |
| ADS _L | ADS _R | Address strobe input. Used as an address qualifier. This signal should be asserted LOW during normal read or write transactions. Asserting this signal LOW also loads the burst address counter with data present on the I/O pins. |
| CE _{0L} , CE _{1L} | CE _{0R} , CE _{1R} | Chip enable input. To select either the left or right port, both CE ₀ AND CE ₁ must be asserted to their active states (CE ₀ ≤ V _{IL} and CE ₁ ≥ V _{IH}). |
| CLK _L | CLK _R | Clock signal. This input can be free-running or strobed. Maximum clock input rate is f _{MAX} . |
| CNTEN _L | CNTEN _R | Counter enable input. Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK. CNTEN is disabled if ADS or CNTRST are asserted LOW. |
| CNTRST _L | CNTRST _R | Counter reset input. Asserting this signal LOW resets the burst address counter of its respective port to zero. CNTRST is not disabled by asserting ADS or CNTEN. |
| I/O _{0L} -I/O _{8L} | I/O _{0R} -I/O _{8R} | Data bus input/output (I/O ₀ -I/O ₈ for x9 devices). |
| OE _L | OE _R | Output enable input. This signal must be asserted LOW to enable the I/O data pins during read operations. |
| RW _L | RW _R | Read/Write enable input. This signal is asserted LOW to write to the dual-port memory array. For read operations, assert this pin HIGH. |
| FT/PIPE _L | FT/PIPE _R | Flow-through/Pipelined select input. For flow-through mode operation, assert this pin LOW. For pipelined mode operation, assert this pin HIGH. |
| GND | | Ground Input. |
| NC | | No connect. |
| V _{CC} | | Power input. |

Maximum Ratings^[2]

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

- Storage temperature -65 °C to +150 °C
- Ambient temperature with power applied . -55 °C to +125 °C
- Supply voltage to ground potential -0.5 V to +4.6 V
- DC voltage applied to outputs in High Z state -0.5 V to V_{CC}+0.5 V
- DC input voltage -0.5 V to V_{CC}+0.5 V
- Output current into outputs (LOW) 20 mA
- Static discharge voltage >2001 V
- Latch-up current >200 mA

Operating Range

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Commercial | 0 °C to +70 °C | 3.3 V ± 300 mV |

Note

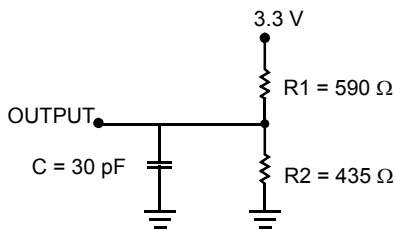
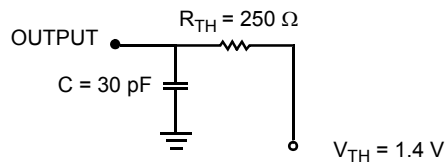
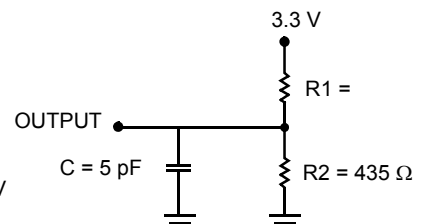
- 2. The voltage on any input or I/O pin can not exceed the power pin during power-up

Electrical Characteristics Over the Operating Range

| Parameter | Description | CY7C09159AV | | | Unit | |
|-----------------|---|-------------|-----|-----|---------------|---------------|
| | | -9 | | | | |
| | | Min | Typ | Max | | |
| V_{OH} | Output HIGH voltage ($V_{CC} = \text{Min.}$, $I_{OH} = -4.0 \text{ mA}$) | 2.4 | – | – | V | |
| V_{OL} | Output LOW voltage ($V_{CC} = \text{Min.}$, $I_{OH} = +4.0 \text{ mA}$) | – | – | 0.4 | V | |
| V_{IH} | Input HIGH voltage | 2.0 | – | – | V | |
| V_{IL} | Input LOW voltage | – | – | 0.8 | V | |
| I_{OZ} | Output leakage current | -10 | – | 10 | μA | |
| I_{CC} | Operating current ($V_{CC} = \text{Max.}$, $I_{OUT} = 0 \text{ mA}$) outputs disabled | Commercial | – | 135 | 230 | mA |
| | | Industrial | – | – | | mA |
| $I_{SB1}^{[3]}$ | Standby current (Both ports TTL level) $\overline{CE}_L \ \& \ \overline{CE}_R \geq V_{IH}$, $f = f_{MAX}$ | Commercial | – | 20 | 75 | mA |
| | | Industrial | – | – | | mA |
| $I_{SB2}^{[3]}$ | Standby current (One port TTL level) $\overline{CE}_L \ \ \overline{CE}_R \geq V_{IH}$, $f = f_{MAX}$ | Commercial | – | 95 | 155 | mA |
| | | Industrial | – | – | | mA |
| $I_{SB3}^{[3]}$ | Standby current (Both ports CMOS level) $\overline{CE}_L \ \text{and} \ \overline{CE}_R \geq V_{CC} - 0.2 \text{ V}$, $f = 0$ | Commercial | – | 10 | 500 | μA |
| | | Industrial | – | – | | μA |
| $I_{SB4}^{[3]}$ | Standby current (One port CMOS level) $\overline{CE}_L \ \ \overline{CE}_R \geq V_{IH}$, $f = f_{MAX}$ | Commercial | – | 85 | 115 | mA |
| | | Industrial | – | – | | mA |

Capacitance

| Parameter | Description | Test Conditions | Max | Unit |
|-----------|--------------------|---|-----|------|
| C_{IN} | Input capacitance | $T_A = 25 \text{ }^\circ\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = 3.3 \text{ V}$ | 10 | pF |
| C_{OUT} | Output capacitance | | 10 | pF |

AC Test Loads

(a) Normal Load (Load 1)

(b) Thévenin Equivalent (Load 1)

(c) Three-state Delay (Load 2)
(Used for t_{CKLZ} , t_{OLZ} , & t_{OHZ} including scope and jig)

Note

3. \overline{CE}_L and \overline{CE}_R are internal signals. To select either the left or right port, both \overline{CE}_0 AND \overline{CE}_1 must be asserted to their active states ($\overline{CE}_0 \leq V_{IL}$ and $\overline{CE}_1 \geq V_{IH}$).

Switching Characteristics Over the Operating Range

| Parameter | Description | CY7C09159AV | | Unit |
|----------------------------|--|-------------|-----|------|
| | | -9 | | |
| | | Min | Max | |
| f_{MAX1} | f_{Max} flow-through | – | 40 | MHz |
| f_{MAX2} | f_{Max} pipelined | – | 67 | MHz |
| t_{CYC1} | Clock cycle time – flow-through | 25 | – | ns |
| t_{CYC2} | Clock cycle time – pipelined | 15 | – | ns |
| t_{CH1} | Clock HIGH time – flow-through | 12 | – | ns |
| t_{CL1} | Clock LOW time – flow-through | 12 | – | ns |
| t_{CH2} | Clock HIGH time – pipelined | 6 | – | ns |
| t_{CL2} | Clock LOW time – pipelined | 6 | – | ns |
| t_R | Clock rise time | – | 3 | ns |
| t_F | Clock fall time | – | 3 | ns |
| t_{SA} | Address setup time | 4 | – | ns |
| t_{HA} | Address hold time | 1 | – | ns |
| t_{SC} | Chip enable setup time | 4 | – | ns |
| t_{HC} | Chip enable hold time | 1 | – | ns |
| t_{SW} | R/\overline{W} setup time | 4 | – | ns |
| t_{HW} | R/\overline{W} hold time | 1 | – | ns |
| t_{SD} | Input data setup time | 4 | – | ns |
| t_{HD} | Input data hold time | 1 | – | ns |
| t_{SAD} | \overline{ADS} setup time | 4 | – | ns |
| t_{HAD} | \overline{ADS} hold time | 1 | – | ns |
| t_{SCN} | \overline{CNTEN} setup time | 4 | – | ns |
| t_{HCN} | \overline{CNTEN} hold time | 1 | – | ns |
| t_{SRST} | \overline{CNTRST} setup time | 4 | – | ns |
| t_{HRST} | \overline{CNTRST} hold time | 1 | – | ns |
| t_{OE} | Output enable to data valid | – | 10 | ns |
| t_{OLZ} | \overline{OE} to Low Z | 2 | – | ns |
| t_{OHZ} | \overline{OE} to High Z | 1 | 7 | ns |
| t_{CD1} | Clock to data valid - flow-through | – | 20 | ns |
| t_{CD2} | Clock to data valid - pipelined | – | 9 | ns |
| t_{DC} | Data output hold after clock HIGH | 2 | – | ns |
| t_{CKHZ} | Clock HIGH to output high Z | 2 | 9 | ns |
| t_{CKLZ} | Clock HIGH to output low Z | 2 | – | ns |
| Port to Port Delays | | | | |
| t_{CWDD} | Write port clock high to read data delay | – | 40 | ns |
| t_{CCS} | Clock to clock setup time | – | 15 | ns |

Switching Waveforms

Figure 1. Read Cycle for Flow-Through Output ($\overline{\text{FT/PIPE}} = V_{\text{IL}}$)^[4, 5, 6, 7]

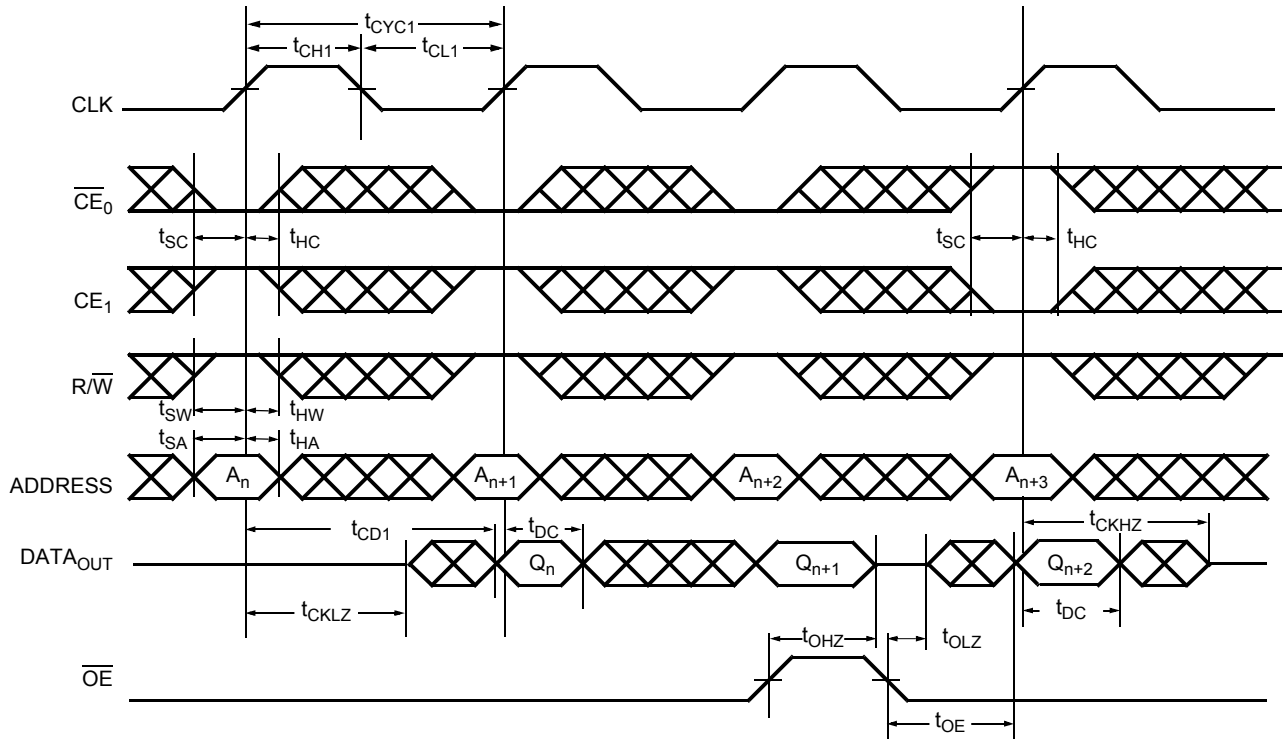
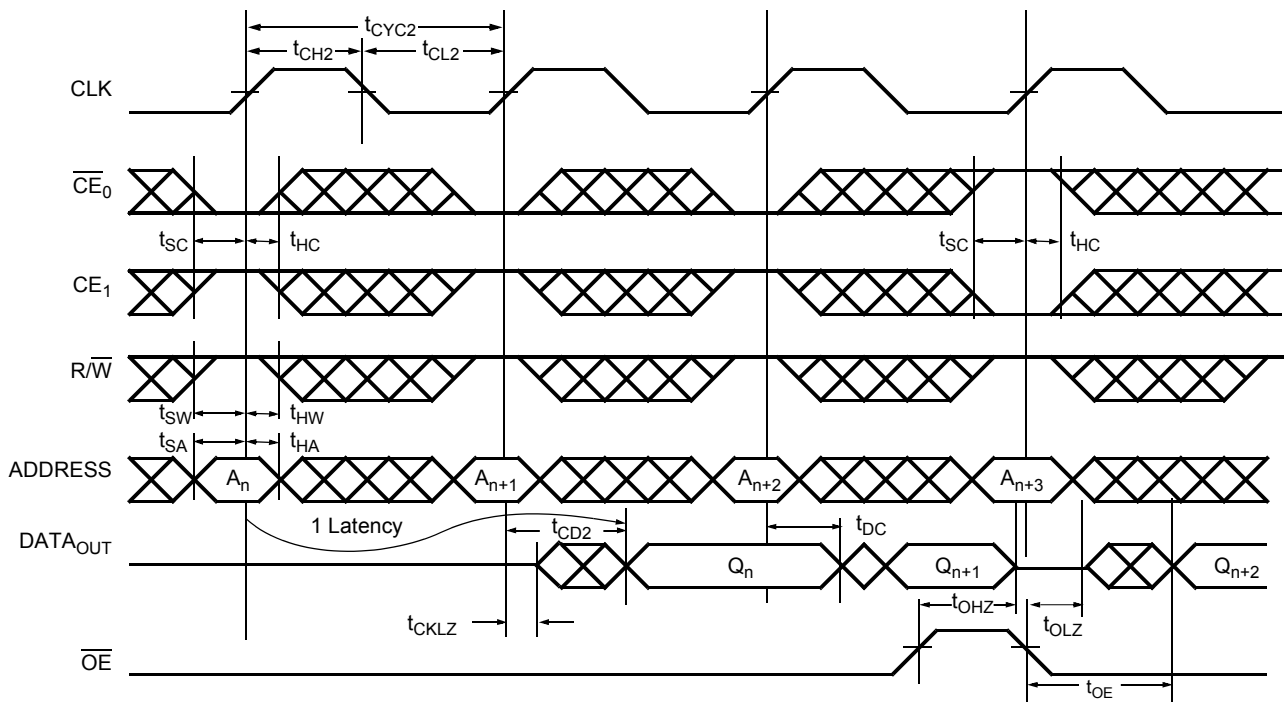


Figure 2. Read Cycle for Pipelined Operation ($\overline{\text{FT/PIPE}} = V_{\text{IH}}$)^[4, 5, 6, 7]



Notes

4. $\overline{\text{OE}}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
5. $\text{ADS} = V_{\text{IL}}$, CNTEN and $\text{CNTRST} = V_{\text{IH}}$
6. The output is disabled (high-impedance state) by $\overline{\text{CE}}_0 = V_{\text{IH}}$ or $\text{CE}_1 = V_{\text{IL}}$ following the next rising edge of the clock.
7. Addresses do not have to be accessed sequentially since $\text{ADS} = V_{\text{IL}}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

Switching Waveforms (continued)

Figure 3. Bank Select Pipelined Read^[8, 9]

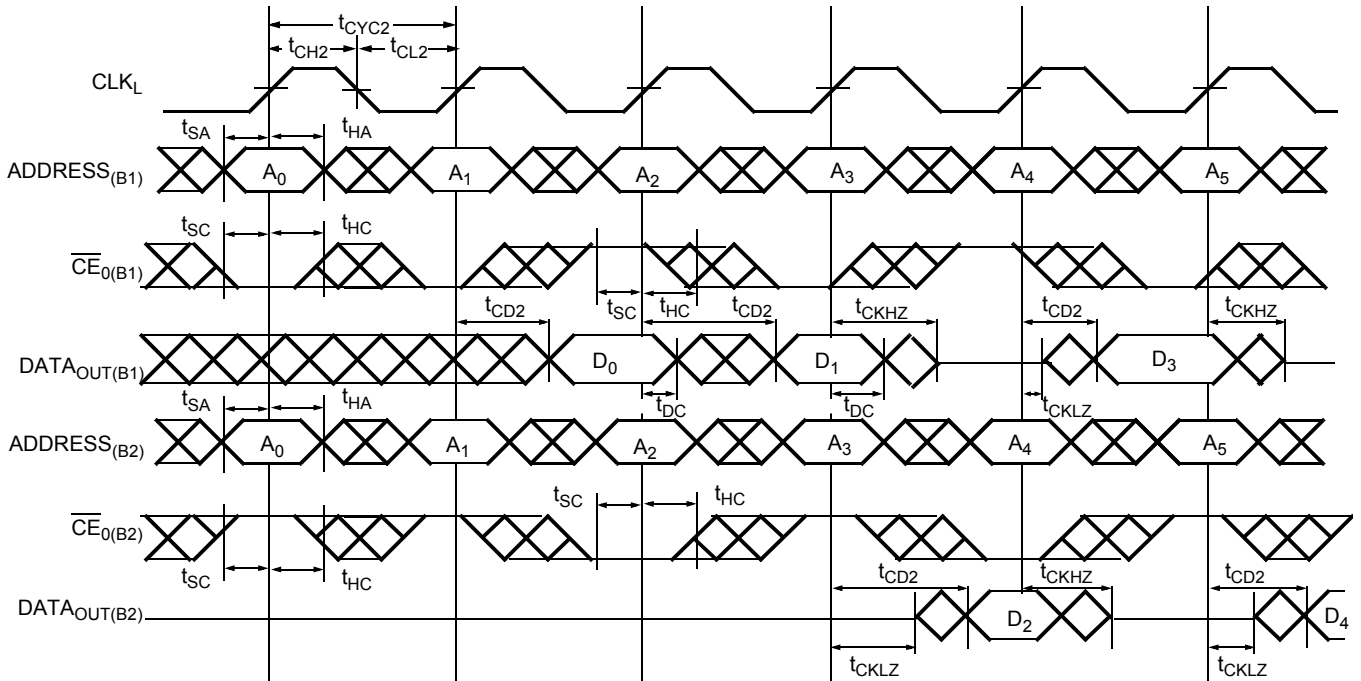
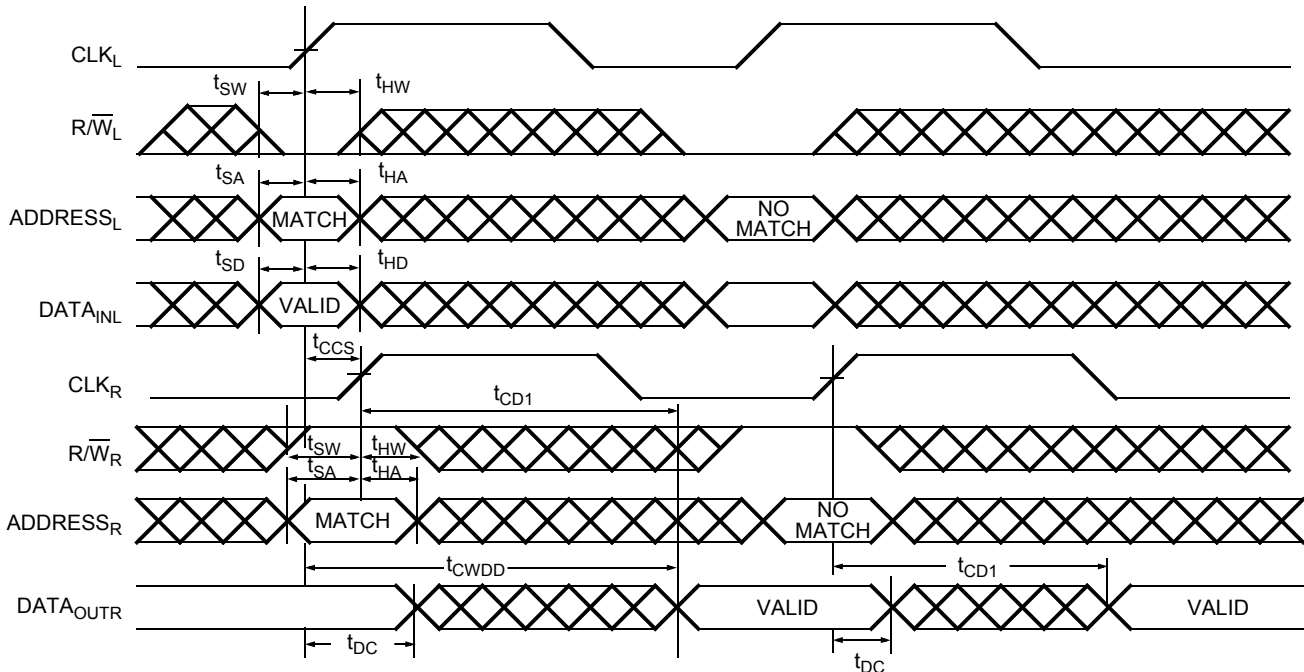


Figure 4. Left Port Write to Flow-Through Right Port Read^[10, 11, 12, 13]



Notes

8. In this depth expansion example, B1 represents Bank #1 and B2 is Bank #2; Each Bank consists of one Cypress dual-port device from this data sheet. ADDRESS_(B1) = ADDRESS_(B2).
9. OE and ADS = V_{IL}; CE_{1(B1)}, CE_{1(B2)}, R/W, CNTEN, and CNTRST = V_{IH}.
10. The same waveforms apply for a right port write to flow-through left port read.
11. CE₀ and ADS = V_{IL}; CE₁, CNTEN, and CNTRST = V_{IH}.
12. OE = V_{IL} for the right port, which is being read from. OE = V_{IH} for the left port, which is being written to.
13. If t_{CCS} ≤ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}. If t_{CCS} > maximum specified, then data is not valid until t_{CCS} + t_{CD1}. t_{CWDD} does not apply in this case.

Switching Waveforms (continued)

Figure 5. Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)^[14, 15, 16, 17]

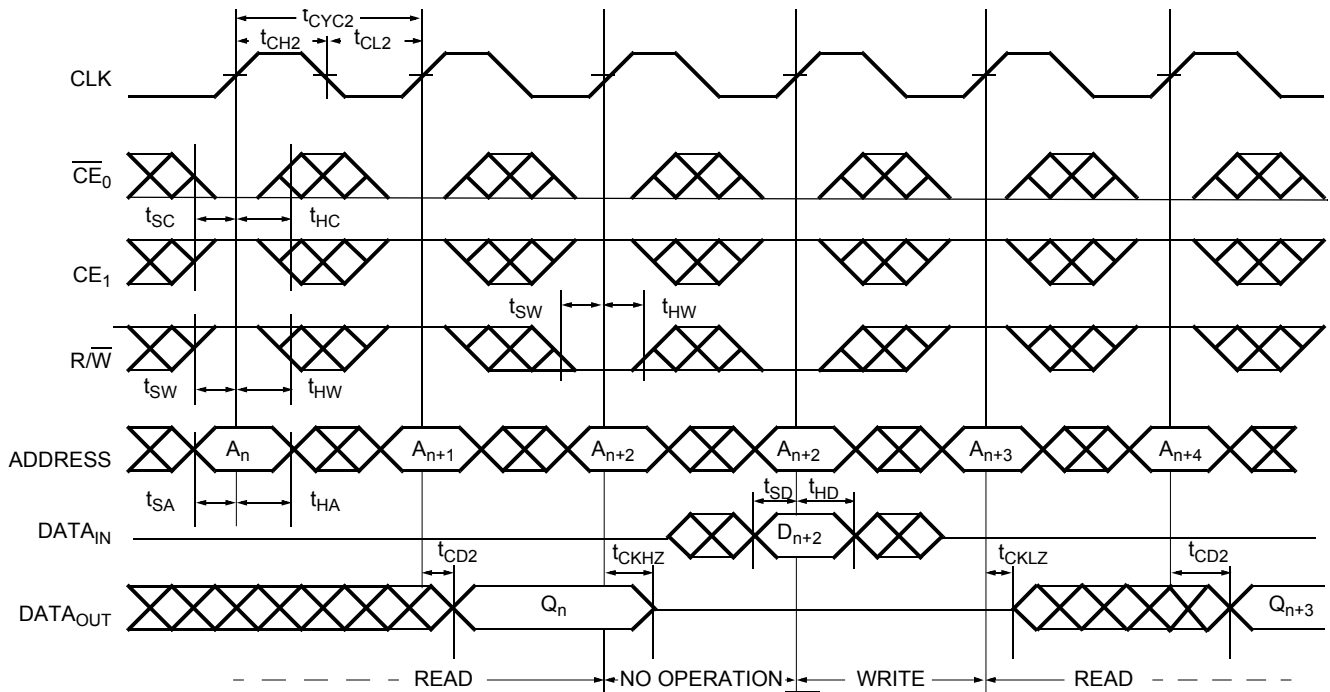
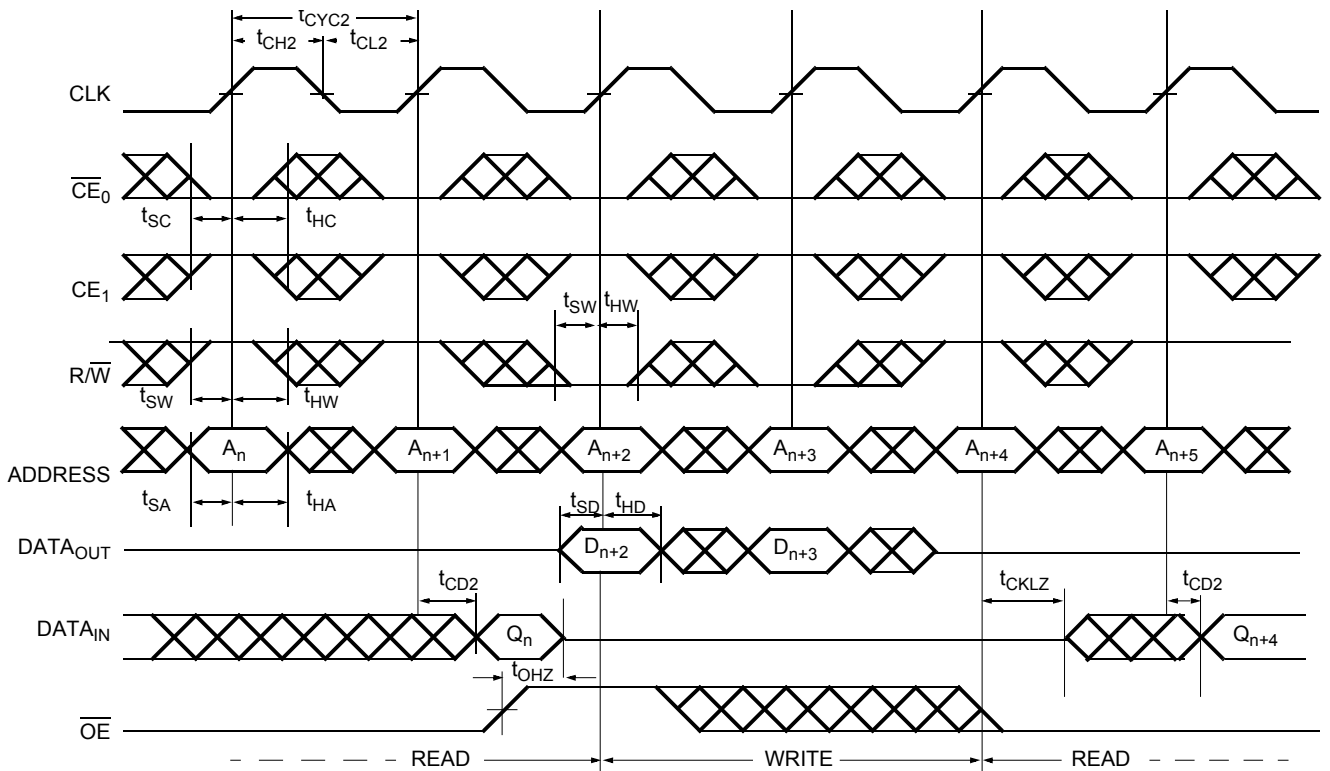


Figure 6. Pipelined Read-to-Write-to-Read (OE Controlled)^[14, 15, 16, 17]



Notes

- 14. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only
- 15. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.
- 16. \overline{CE}_0 and $\overline{ADS} = V_{IL}$; \overline{CE}_1 , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$.
- 17. During "No operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.

Switching Waveforms (continued)

Figure 7. Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)^[18, 19, 20, 21, 22]

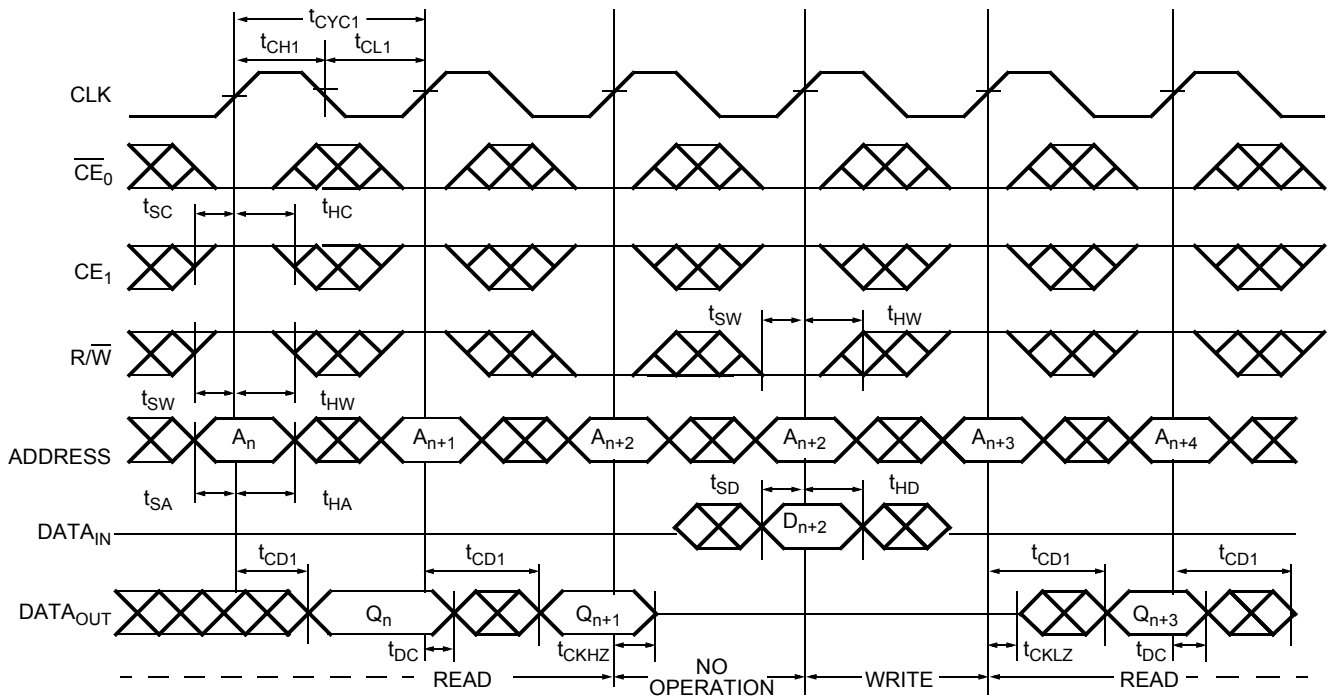
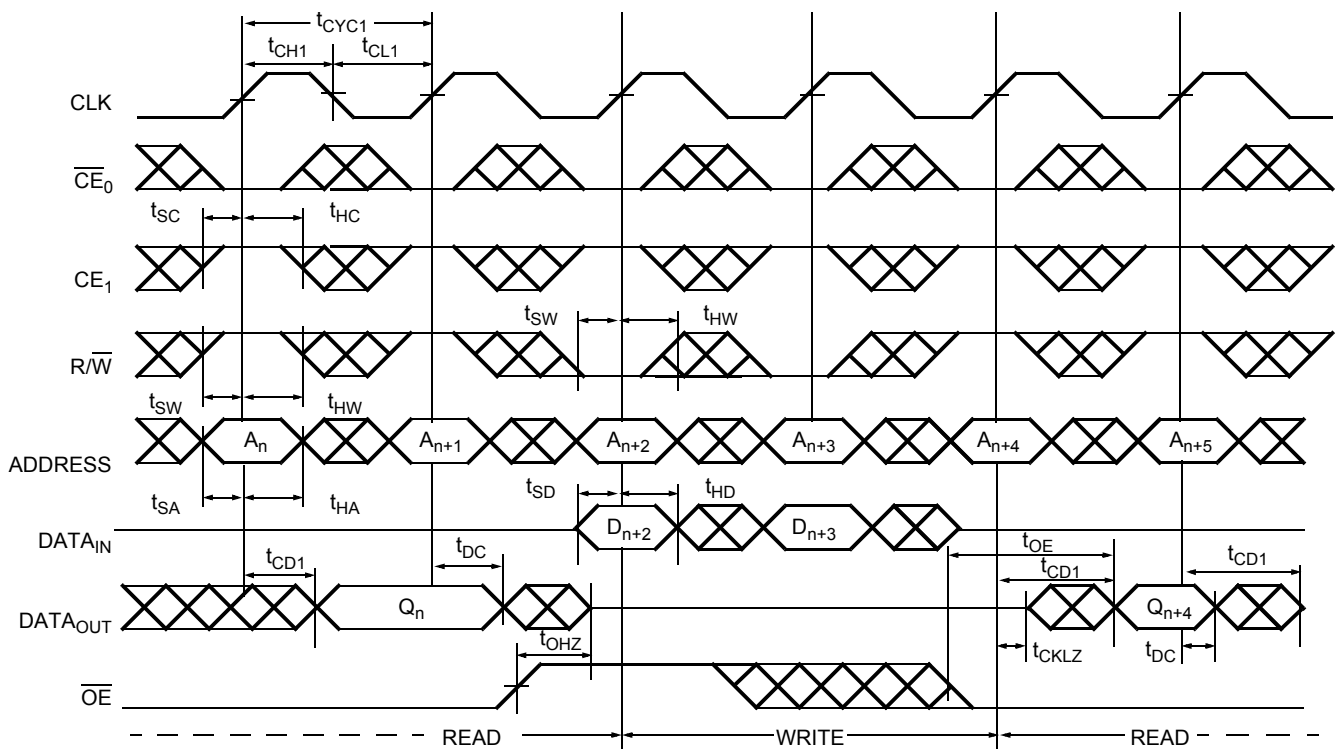


Figure 8. Flow-Through Read-to-Write-to-Read (\overline{OE} Controlled)^[18, 19, 20, 21, 22]



Notes

- 18. $ADS = V_{IL}$, \overline{CNTEN} and $\overline{CNTRST} = V_{IH}$
- 19. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only
- 20. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.
- 21. \overline{CE}_0 and $ADS = V_{IL}$; CE_1 , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$.
- 22. During "No operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.

Switching Waveforms (continued)

Figure 9. Pipelined Read with Address Counter Advance^[23]

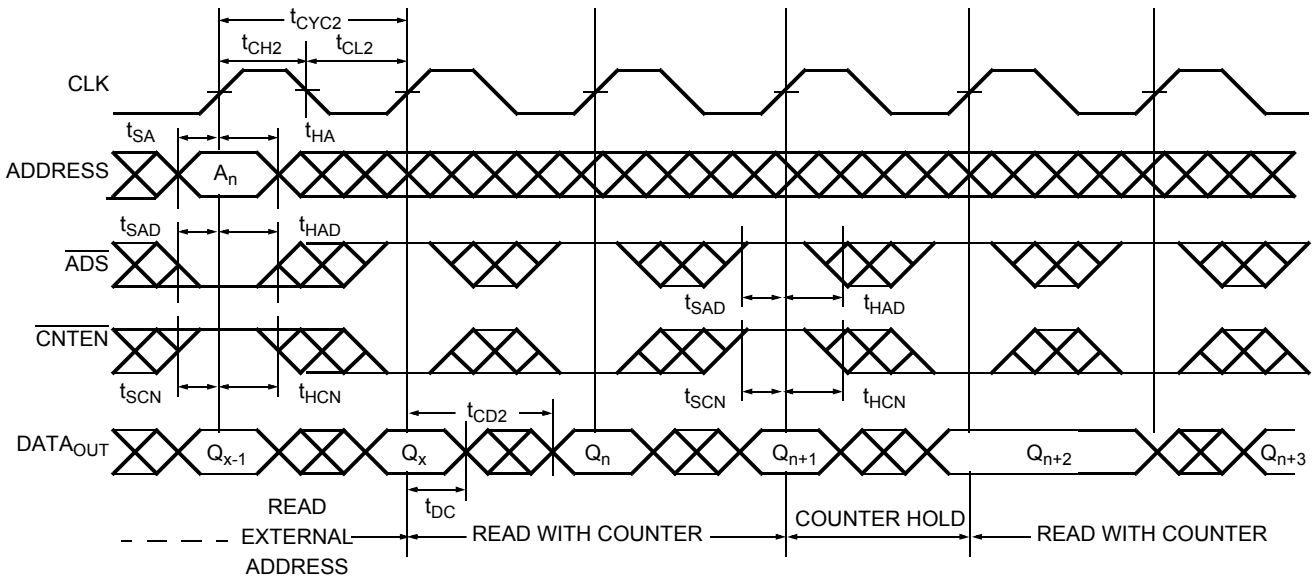
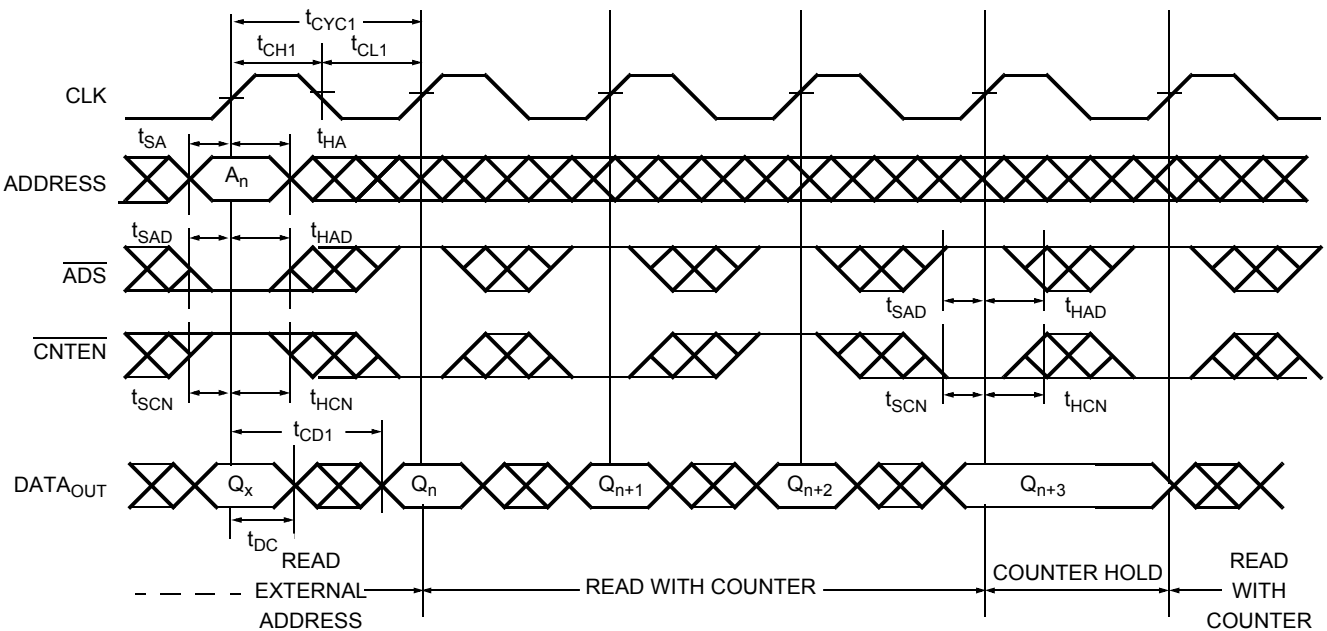


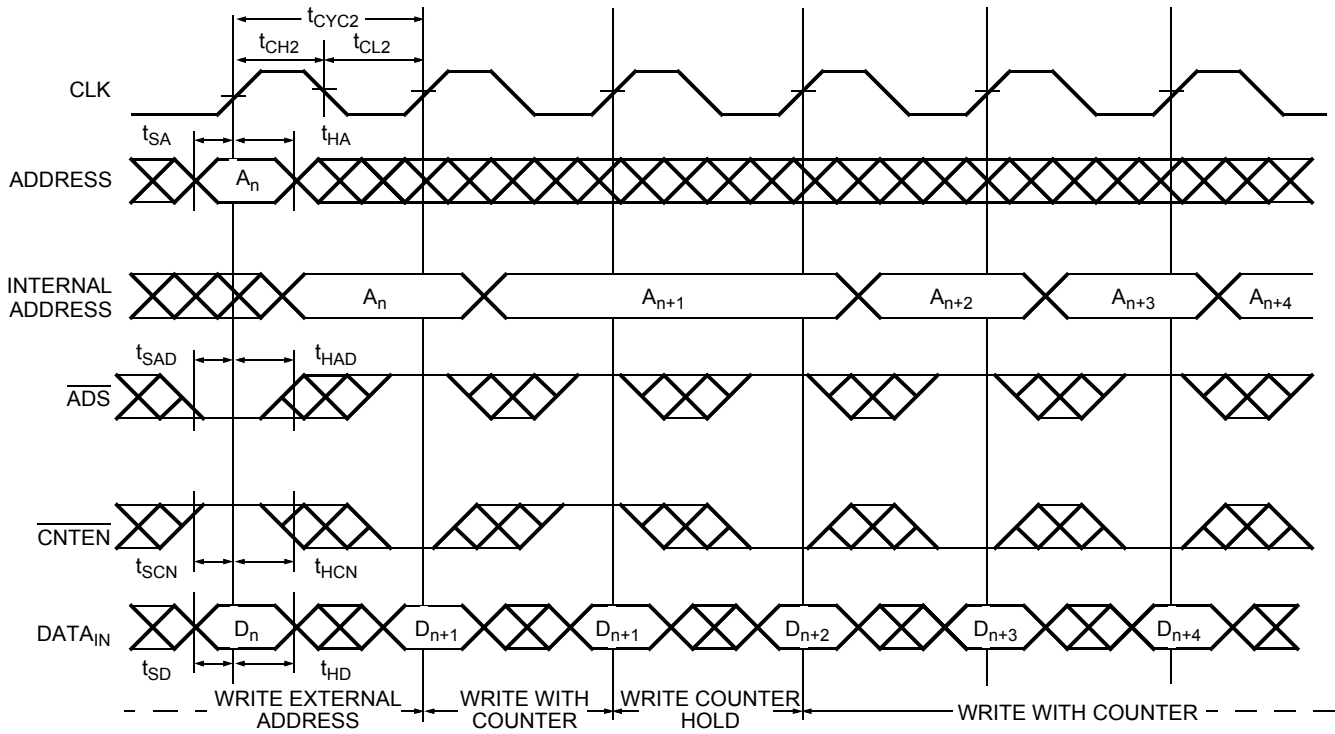
Figure 10. Flow-Through Read with Address Counter Advance^[23]



Note
23. \overline{CE}_0 and $\overline{OE} = V_{IL}$; $CE_1, R/\overline{W}$ and $\overline{CNTNST} = V_{IH}$.

Switching Waveforms (continued)

Figure 11. Write with Address Counter Advance (Flow-Through or Pipelined Outputs)^[24, 25]



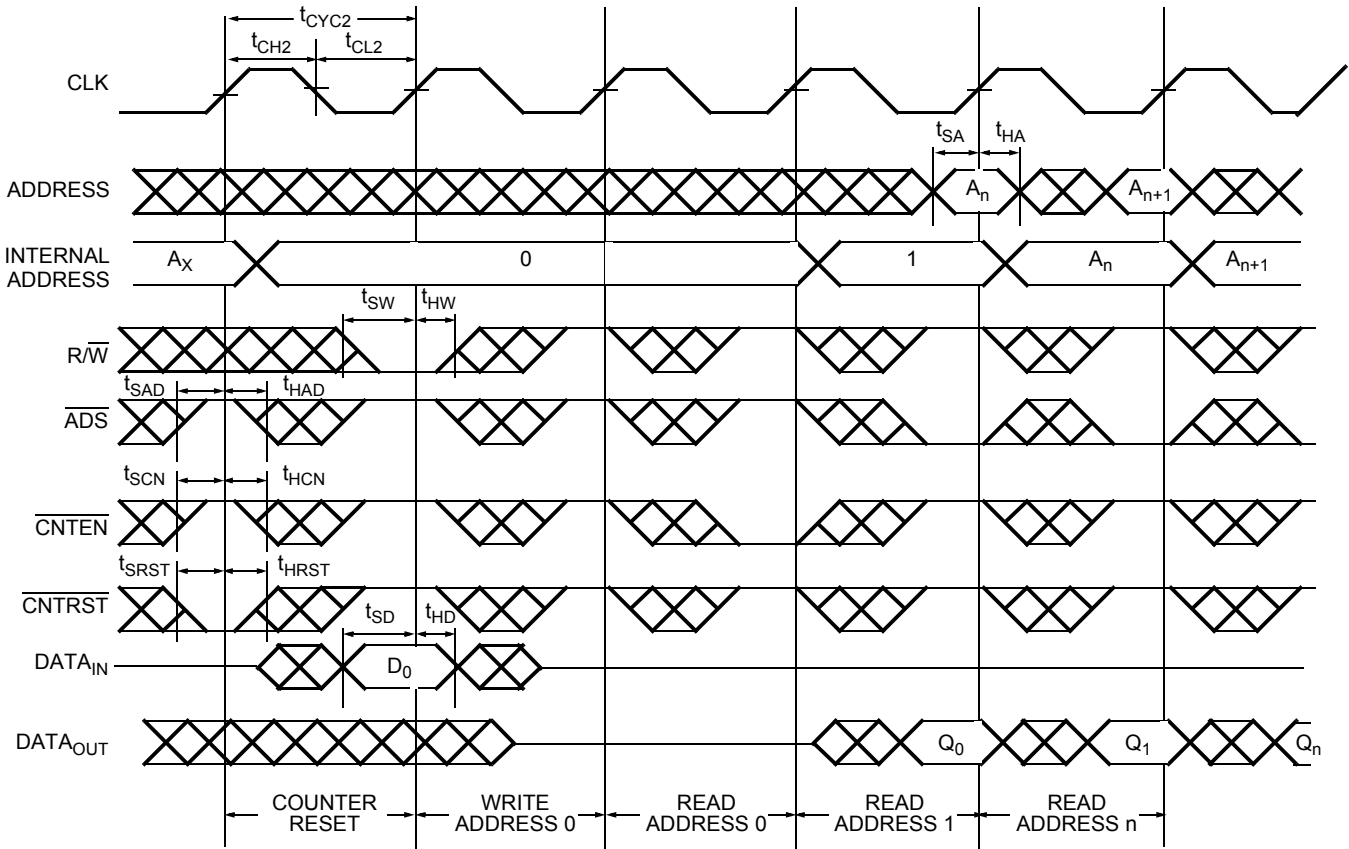
Notes

24. $\overline{CE_0}$ and $R/\overline{W} = V_{IL}$; $\overline{CE_1}$ and $\overline{CNTRST} = V_{IH}$.

25. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.

Switching Waveforms (continued)

Figure 12. Counter Reset (Pipelined Outputs)^[26, 27, 28, 29]



Notes

- 26. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only
- 27. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.
- 28. $CE_0 = V_{IL}$; $CE_1 = V_{IH}$.
- 29. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset.

Table 1. Read/Write and Enable Operation^[30, 31, 32]









| Inputs | | | | | Outputs | |
|--------|---|-----------------|-----------------|-----|------------------------------------|----------------------------|
| OE | CLK | CE ₀ | CE ₁ | R/W | I/O ₀ –I/O ₉ | Operation |
| X |  | H | X | X | High-Z | Deselected ^[33] |
| X |  | X | L | X | High-Z | Deselected ^[33] |
| X |  | L | H | L | D _{IN} | Write |
| L |  | L | H | H | D _{OUT} | Read ^[33] |
| H | X | L | H | X | High-Z | Outputs disabled |

Table 2. Address Counter Control Operation^[30, 34, 35, 36]

| Address | Previous Address | CLK | $\overline{\text{ADS}}$ | $\overline{\text{CNTEN}}$ | $\overline{\text{CNRST}}$ | I/O | Mode | Operation |
|----------------|------------------|---|-------------------------|---------------------------|---------------------------|-----------------------|-----------|---|
| X | X |  | X | X | L | D _{out(0)} | Reset | Counter reset to address 0 |
| A _n | X |  | L | X | H | D _{out(n)} | Load | Address load into counter |
| X | A _n |  | H | H | H | D _{out(n)} | Hold | External address blocked—counter disabled |
| X | A _n |  | H | L | H | D _{out(n+1)} | Increment | Counter enabled—internal address generation |

Notes

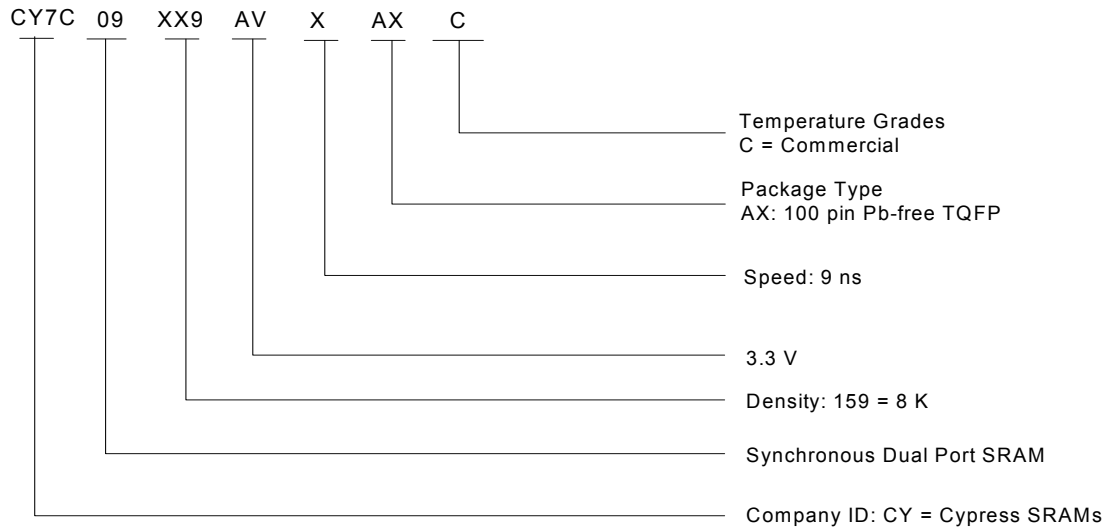
30. "X" = "don't care." "H" = V_{IH}, "L" = V_{IL}.
 31. $\overline{\text{ADS}}$, $\overline{\text{CNTEN}}$, $\overline{\text{CNRST}}$ = "don't care."
 32. OE is an asynchronous input signal.
 33. When CE changes state in the pipelined mode, deselection and read happen in the following clock cycle.
 34. $\overline{\text{CE}}_0$ and $\overline{\text{OE}}$ = V_{IL}; CE₁ and R/W = V_{IH}.
 35. Data shown for Flow-through mode; pipelined mode output will be delayed by one cycle.
 36. Counter operation is independent of CE₀ and CE₁.

Ordering Information

Table 3. 8 K × 9 3.3-V Synchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|------------------|--------------|-------------------------------------|-----------------|
| 9 | CY7C09159AV-9AXC | A100 | 100-Pin Pb-free Thin Quad Flat Pack | Commercial |

Ordering Code Definitions



Document History Page

| Document Title: CY7C09159AV 3.3-V 8 K × 9 Synchronous Dual Port Static RAM Document Number: 38-06053 | | | | |
|---|---------|-----------------|-----------------|--|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 110205 | SZV | 11/15/01 | Change from Spec number: 38-00839 to 38-06053 |
| *A | 122303 | RBI | 12/27/02 | Power up requirements added to Maximum Ratings Information |
| *B | 393581 | YIM | See ECN | Added Pb-Free Logo Added Pb-Free parts to ordering information: CY7C09159AV-9AXC, CY7C09159AV-12AXC, CY7C09169AV-12AXC, CY7C09169AV-12AXI |
| *C | 2897159 | RAME | 03/22/10 | Removed inactive parts from ordering information and updated package diagram. |
| *D | 3076884 | ADMU | 11/02/10 | Updated as per latest template Added Acronyms and Units of Measure table Added Ordering Code Definitions . |
| *E | 3432711 | ADMU | 11/08/11 | Updated template according to current CY standards. Removed information on CY7C09169AV. Removed speed bin –12. Updated package diagram. |
| *F | 4575241 | ADMU | 11/19/2014 | Added related documentation hyperlink in page 1. Updated Figure 13 in Package Diagram (spec 51-85048 *E to *I). |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

| | |
|--------------------------|--|
| Automotive | cypress.com/go/automotive |
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc cypress.com/go/plc |
| Memory | cypress.com/go/memory |
| Optical & Image Sensing | cypress.com/go/image |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2010-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.