

3.3 V 8 K / 16 K × 8 Asynchronous Dual-Port Static RAM

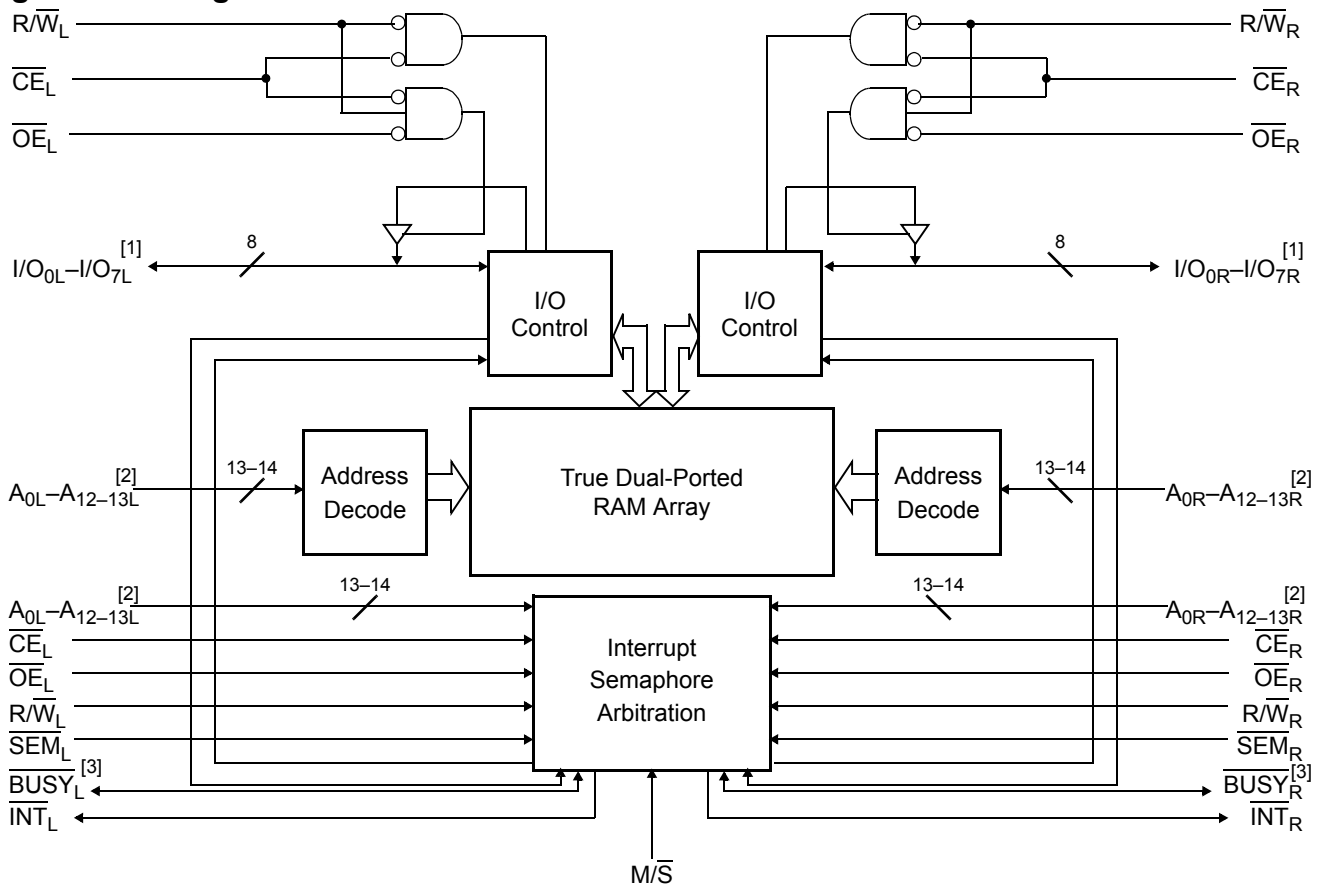
Features

- True dual-ported memory cells which allow simultaneous access of the same memory location
- 8 K / 16 K × 8 organizations (CY7C144AV/CY7C006AV)
- 0.35-micron complementary metal oxide semiconductor (CMOS) for optimum speed/power
- High-speed access: 25 ns
- Low operating power
 - Active: $I_{CC} = 115 \text{ mA}$ (typical)
 - Standby: $I_{SB3} = 10 \text{ } \mu\text{A}$ (typical)
- Fully asynchronous operation
- Automatic power-down
- Expandable data bus to 16 bits or more using Master/ Slave chip select when using more than one device
- On-chip arbitration logic
- Semaphores included to permit software handshaking between ports
- $\overline{\text{INT}}$ flag for port-to-port communication
- Pin select for Master or Slave
- Available in 64-pin thin quad flat pack (TQFP) (7C006AV and 7C144AV)
- Pb-free packages available

Functional Description

For a complete list of related documentation, [click here](#).

Logic Block Diagram



Notes

1. I/O₀-I/O₇ for × 8 devices.
2. A₀-A₁₂ for 8K devices; A₀-A₁₃ for 16K devices.
3. BUSY is an output in master mode and an input in slave mode.

Contents

| | | | |
|--|-----------|--|-----------|
| Pin Configurations | 3 | Non-Contending Read/Write | 16 |
| Selection Guide | 4 | Interrupt Operation Example | 16 |
| Pin Definitions | 4 | Semaphore Operation Example | 16 |
| Architecture | 4 | Ordering Information | 17 |
| Functional Overview | 4 | 8 K × 8 3.3 V Asynchronous Dual-Port SRAM | 17 |
| Read and Write Operations | 4 | 16 K × 8 3.3 V Asynchronous Dual-Port SRAM | 17 |
| Interrupts | 5 | Ordering Code Definitions | 17 |
| Busy | 5 | Package Diagrams | 18 |
| Master/Slave | 5 | Acronyms | 19 |
| Semaphore Operation | 5 | Document Conventions | 19 |
| Maximum Ratings | 6 | Units of Measure | 19 |
| Operating Range | 6 | Document History Page | 20 |
| Electrical Characteristics | 6 | Sales, Solutions, and Legal Information | 21 |
| Capacitance | 6 | Worldwide Sales and Design Support | 21 |
| AC Test Loads and Waveforms | 7 | Products | 21 |
| Data Retention Mode | 7 | PSoC® Solutions | 21 |
| Timing | 7 | Cypress Developer Community | 21 |
| Switching Characteristics | 8 | Technical Support | 21 |
| Switching Waveforms | 10 | | |

Pin Configurations

Figure 1. 64-pin TQFP pinout (Top View)

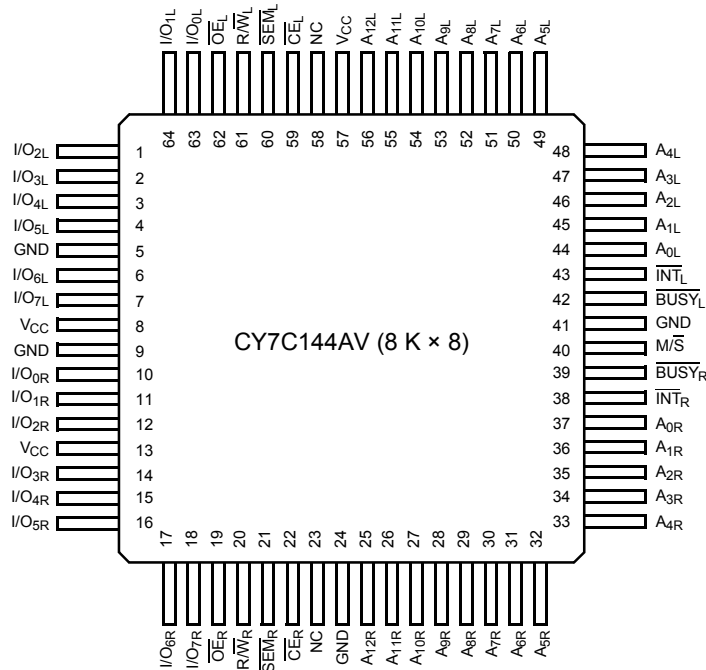
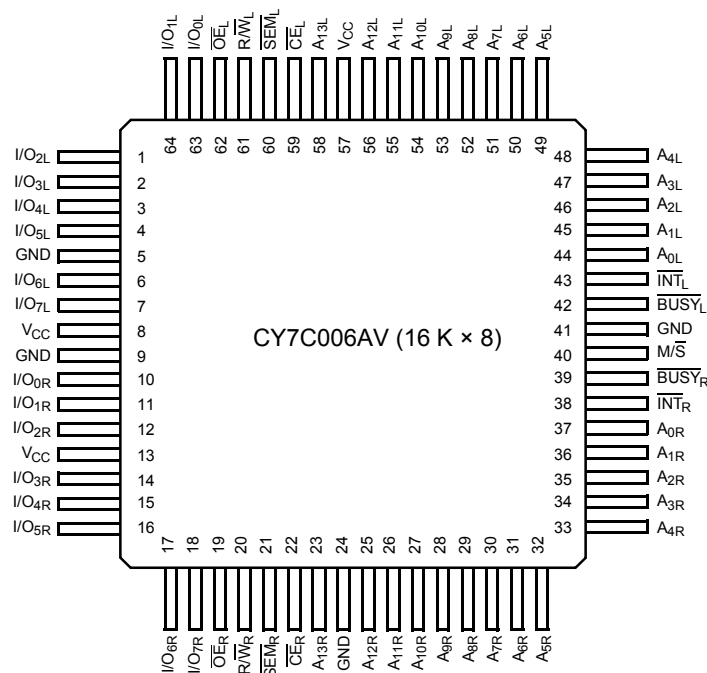


Figure 2. 64-pin TQFP pinout (Top View)



Selection Guide

| Description | CY7C144AV/CY7C006AV -25 |
|---|----------------------------|
| Maximum access time (ns) | 25 |
| Typical operating current (mA) | 115 |
| Typical standby current for I _{SB1} (mA) (Both ports TTL level) | 30 |
| Typical standby current for I _{SB3} (μA) (Both ports CMOS level) | 10 |

Pin Definitions

| Left Port | Right Port | Description |
|--------------------------------------|--------------------------------------|---|
| \overline{CE}_L | \overline{CE}_R | Chip enable |
| R/W_L | R/W_R | Read/Write enable |
| \overline{OE}_L | \overline{OE}_R | Output enable |
| A _{0L} -A _{12/13L} | A _{0R} -A _{12/13R} | Address (A ₀ -A ₁₂ for 8K devices; A ₀ -A ₁₃ for 16K devices) |
| I/O _{0L} -I/O _{7L} | I/O _{0R} -I/O _{7R} | Data bus input/output (I/O ₀ -I/O ₇ for × 8 devices) |
| \overline{SEM}_L | \overline{SEM}_R | Semaphore Enable |
| \overline{INT}_L | \overline{INT}_R | Interrupt flag |
| \overline{BUSY}_L | \overline{BUSY}_R | Busy flag |
| M/ \overline{S} | | Master or Slave select |
| V _{CC} | | Power |
| GND | | Ground |
| NC | | No connect |

Architecture

The CY7C144AV and CY7C006AV consist of an array of 8K and 16K words of 8 bits each of dual-port RAM cells, I/O and address lines, and control signals (CE, OE, R/W). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a BUSY pin is provided on each port. Two interrupt (INT) pins can be utilized for port-to-port communication. Two semaphore (SEM) control pins are used for allocating shared resources. With the M/ \overline{S} pin, the device can function as a master (BUSY pins are outputs) or as a slave (BUSY pins are inputs). The device also has an automatic power-down feature controlled by \overline{CE} . Each port is provided with its own output enable control (OE), which allows data to be read from the device.

Functional Overview

The CY7C144AV and CY7C006AV are low-power CMOS 8 K / 16 K × 8 dual-port static RAMs. Various arbitration schemes are included on the devices to handle situations when multiple processors access the same piece of data. Two ports are provided, permitting independent, asynchronous access for reads and writes to any location in memory. The devices can be utilized as standalone 8-bit dual-port static RAMs or multiple devices can be combined in order to function as a 16-bit or wider

master/slave dual-port static RAM. An M/ \overline{S} pin is provided for implementing 16-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: Chip Enable (\overline{CE}), Read or Write Enable (R/W), and Output Enable (\overline{OE}). Two flags are provided on each port (BUSY and INT). BUSY signals that the port is trying to access the same location currently being accessed by the other port. The Interrupt flag (INT) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a Chip Select (CE) pin.

Read and Write Operations

When writing data must be set up for a duration of t_{SD} before the rising edge of R/W in order to guarantee a valid write. A write operation is controlled by either the R/W pin (see Write Cycle No. 1 waveform) or the CE pin (see Write Cycle No. 2 waveform).

Required inputs for non-contention operations are summarized in [Table 1 on page 16](#).

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

When reading the device, the user must assert both the \overline{OE} and \overline{CE} pins. Data will be available t_{ACE} after \overline{CE} or t_{DOE} after \overline{OE} is asserted. If the user wishes to access a semaphore flag, then the \overline{SEM} pin must be asserted instead of the \overline{CE} pin and \overline{OE} must also be asserted.

Interrupts

The upper two memory locations may be used for message passing. The highest memory location (1FFF for the CY7C144AV and 3FFF for the CY7C006AV) is the mailbox for the right port and the second-highest memory location (1FFE for the CY7C144AV and 3FFE for the CY7C006AV) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it. If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin. The operation of the interrupts and their interaction with Busy are summarized in [Table 2 on page 16](#).

Busy

The CY7C144AV and CY7C006AV provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' \overline{CE} s are asserted and an address match occurs within t_{PS} of each other, the busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not predictable which port will get that permission. \overline{BUSY} will be asserted t_{BLA} after an address match or t_{BLC} after \overline{CE} is taken LOW.

Master/Slave

An $\overline{M/S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The \overline{BUSY} output of the master is connected to the \overline{BUSY} input of the slave. This will allow the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the \overline{BUSY} input has settled (t_{BLC} or t_{BLA}), otherwise,

the slave chip may begin a write cycle during a contention situation. When tied HIGH, the $\overline{M/S}$ pin allows the device to be used as a master and, therefore, the \overline{BUSY} line is an output. \overline{BUSY} can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C144AV and CY7C006AV provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, \overline{SEM} or \overline{OE} must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting \overline{SEM} LOW. The \overline{SEM} pin functions as a chip select for the semaphore latches (\overline{CE} must remain HIGH during \overline{SEM} LOW). A_{0-2} represents the semaphore address. \overline{OE} and R/W are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an available semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. [Table 3 on page 16](#) shows sample semaphore operations.

When reading a semaphore, all data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Maximum Ratings

Exceeding maximum ratings ^[4] may impair the useful life of the device. These user guidelines are not tested.

| | |
|---|----------------------------|
| Storage temperature | -65 °C to +150 °C |
| Ambient temperature with Power applied | -55 °C to +125 °C |
| Supply voltage to ground potential | -0.5 V to +4.6 V |
| DC voltage applied to Outputs in High Z state | -0.5 V to $V_{CC} + 0.5 V$ |

| | |
|-----------------------------------|----------------------------|
| DC input voltage ^[5] | -0.5 V to $V_{CC} + 0.5 V$ |
| Output current into outputs (LOW) | 20 mA |
| Static discharge voltage | > 2001 V |
| Latch-up current | > 200 mA |

Operating Range

| Range | Ambient Temperature | V_{CC} |
|------------|---------------------|----------------|
| Commercial | 0 °C to +70 °C | 3.3 V ± 300 mV |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | CY7C144AV/CY7C006AV | | | | Unit |
|-----------|--|---------------------|-----|-----|-----|------|
| | | -25 | | | | |
| | | Min | Typ | Max | | |
| V_{OH} | Output HIGH voltage ($V_{CC} = 3.3 V$) | 2.4 | - | - | V | |
| V_{OL} | Output LOW voltage | - | - | 0.4 | V | |
| V_{IH} | Input HIGH voltage | 2.0 | - | - | V | |
| V_{IL} | Input LOW voltage | - | - | 0.8 | V | |
| I_{OZ} | Output leakage current | -10 | - | 10 | μA | |
| I_{CC} | Operating current ($V_{CC} = \text{Max.}$, $I_{OUT} = 0 \text{ mA}$) Outputs Disabled | Commercial | - | 115 | 165 | mA |
| I_{SB1} | Standby current (Both ports TTL level) $CE_L \ \& \ CE_R \geq V_{IH}$, $f = f_{MAX}$ ^[6] | Commercial | - | 30 | 40 | mA |
| I_{SB2} | Standby current (One port TTL level) $CE_L \ \ CE_R \geq V_{IH}$, $f = f_{MAX}$ ^[6] | Commercial | - | 65 | 95 | mA |
| I_{SB3} | Standby current (Both ports CMOS level) $CE_L \ \& \ CE_R \geq V_{CC} - 0.2 V$, $f = 0$ ^[6] | Commercial | - | 10 | 500 | μA |
| I_{SB4} | Standby current (One port CMOS level) $CE_L \ \ CE_R \geq V_{IH}$, $f = f_{MAX}$ ^[6] | Commercial | - | 60 | 80 | mA |

Capacitance

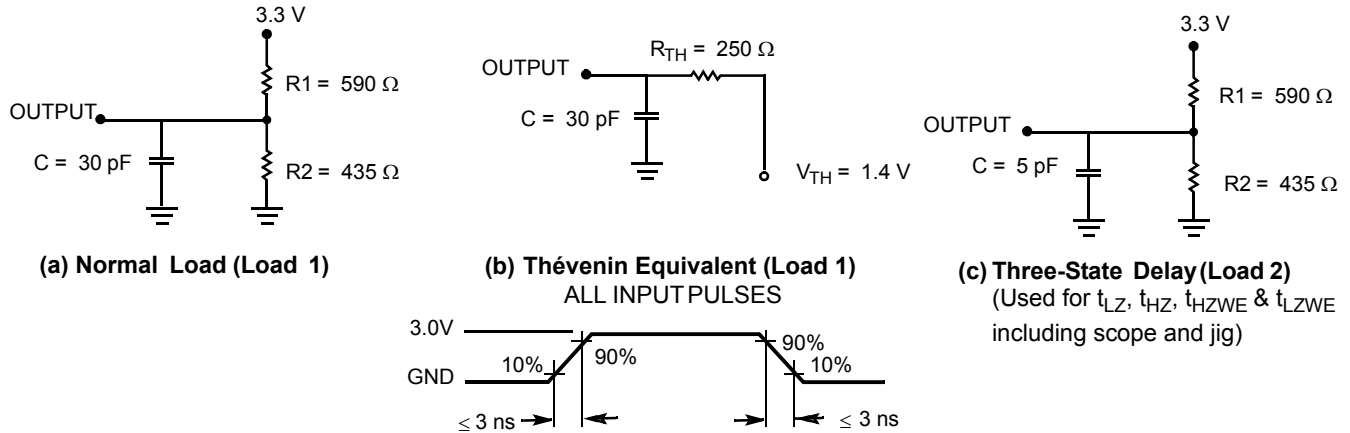
| Parameter ^[7] | Description | Test Conditions | Max | Unit |
|--------------------------|--------------------|--|-----|------|
| C_{IN} | Input capacitance | $T_A = 25 \text{ °C}$, $f = 1 \text{ MHz}$, $V_{CC} = 3.3 V$ | 10 | pF |
| C_{OUT} | Output capacitance | | 10 | pF |

Notes

- The Voltage on any input or I/O pin can not exceed the power pin during power-up.
- Pulse width < 20 ns.
- $f_{MAX} = 1/t_{RC}$. All inputs cycling at $f = 1/t_{RC}$ (except output enable). $f = 0$ means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3} .
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms

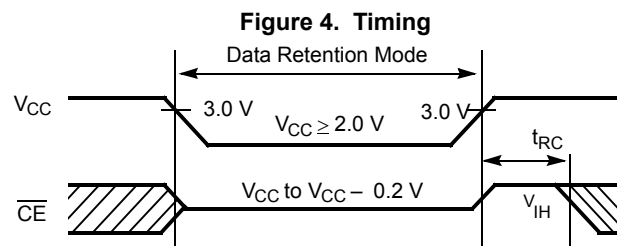


Data Retention Mode

The CY7C144AV and CY7C006AV are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip enable (\overline{CE}) must be held HIGH during data retention, within V_{CC} to $V_{CC} - 0.2$ V.
2. \overline{CE} must be kept between $V_{CC} - 0.2$ V and 70% of V_{CC} during the power-up and power-down transitions.
3. The RAM can begin operation > t_{RC} after V_{CC} reaches the minimum operating voltage (3.0 Volts).

Timing



| Parameter | Test Conditions [8] | Max | Unit |
|-------------|---------------------|-----|---------|
| I_{CCDR1} | @ $V_{CCDR} = 2$ V | 50 | μ A |

Note

8. $\overline{CE} = V_{CC}$, $V_{IN} = \text{GND to } V_{CC}$, $T_A = 25$ °C. This parameter is guaranteed but not tested.

Switching Characteristics

Over the Operating Range

| Parameter ^[9] | Description | CY7C144AV/CY7C006AV | | Unit |
|--------------------------|-------------------------------------|---------------------|-----|------|
| | | -25 | | |
| | | Min | Max | |
| READ CYCLE | | | | |
| t_{RC} | Read cycle time | 25 | – | ns |
| t_{AA} | Address to data valid | – | 25 | ns |
| t_{OHA} | Output hold from address change | 3 | – | ns |
| $t_{ACE}^{[10]}$ | \overline{CE} LOW to data valid | – | 25 | ns |
| t_{DOE} | \overline{OE} LOW to data valid | – | 13 | ns |
| $t_{LZOE}^{[11, 12]}$ | \overline{OE} Low to Low Z | 3 | – | ns |
| $t_{HZOE}^{[11, 12]}$ | \overline{OE} HIGH to High Z | – | 15 | ns |
| $t_{LZCE}^{[11, 12]}$ | \overline{CE} LOW to Low Z | 3 | – | ns |
| $t_{HZCE}^{[11, 12]}$ | \overline{CE} HIGH to High Z | – | 15 | ns |
| t_{PU} | \overline{CE} LOW to power-up | 0 | – | ns |
| t_{PD} | \overline{CE} HIGH to power-down | – | 25 | ns |
| WRITE CYCLE | | | | |
| t_{WC} | Write cycle time | 25 | – | ns |
| $t_{SCE}^{[10]}$ | \overline{CE} LOW to write end | 20 | – | ns |
| t_{AW} | Address valid to write end | 20 | – | ns |
| t_{HA} | Address hold from write end | 0 | – | ns |
| $t_{SA}^{[10]}$ | Address set-up to write start | 0 | – | ns |
| t_{PWE} | Write pulse width | 20 | – | ns |
| t_{SD} | Data set-up to write end | 15 | – | ns |
| t_{HD} | Data hold from write end | 0 | – | ns |
| t_{HZWE} | R/\overline{W} LOW to High Z | – | 15 | ns |
| t_{LZWE} | R/\overline{W} HIGH to Low Z | 3 | – | ns |
| $t_{WDD}^{[13]}$ | Write pulse to data delay | – | 50 | ns |
| $t_{DDD}^{[13]}$ | Write data valid to read data valid | – | 35 | ns |

Notes

9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OH}/I_{OH} and 30-pF load capacitance.
10. To access RAM, $\overline{CE} = L$, $\overline{SEM} = H$. To access semaphore, $\overline{CE} = H$ and $\overline{SEM} = L$. Either condition must be valid for the entire t_{SCE} time.
11. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE} .
12. Test conditions used are Load 3.
13. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.

Switching Characteristics (continued)

Over the Operating Range

| Parameter ^[9] | Description | CY7C144AV/CY7C006AV | | Unit |
|----------------------------------|---|---------------------|-----|------|
| | | -25 | | |
| | | Min | Max | |
| BUSY TIMING | | | | |
| t _{BLA} | $\overline{\text{BUSY}}$ LOW from address match | – | 20 | ns |
| t _{BHA} | $\overline{\text{BUSY}}$ HIGH from address mismatch | – | 20 | ns |
| t _{BLC} | $\overline{\text{BUSY}}$ LOW from $\overline{\text{CE}}$ LOW | – | 20 | ns |
| t _{BHC} | $\overline{\text{BUSY}}$ HIGH from $\overline{\text{CE}}$ HIGH | – | 17 | ns |
| t _{PS} | Port set-up for priority | 5 | – | ns |
| t _{WB} | R/W HIGH after $\overline{\text{BUSY}}$ (Slave) | 0 | – | ns |
| t _{WH} | R/W HIGH after $\overline{\text{BUSY}}$ HIGH (Slave) | 17 | – | ns |
| t _{BDD} ^[14] | $\overline{\text{BUSY}}$ HIGH to data valid | – | 25 | ns |
| INTERRUPT TIMING | | | | |
| t _{INS} | INT set time | – | 20 | ns |
| t _{INR} | INT reset time | – | 20 | ns |
| SEMAPHORE TIMING | | | | |
| t _{SOP} | SEM flag update pulse ($\overline{\text{OE}}$ or $\overline{\text{SEM}}$) | 12 | – | ns |
| t _{SWRD} | SEM flag write to read time | 5 | – | ns |
| t _{SPS} | SEM flag contention window | 5 | – | ns |
| t _{SAA} | SEM address access time | – | 25 | ns |

Note

14. t_{BDD} is a calculated parameter and is the greater of t_{WDD}–t_{PWE} (actual) or t_{DOD}–t_{SD} (actual).

Switching Waveforms

Figure 5. Read Cycle No. 1 (Either Port Address Access) [15, 16, 17]

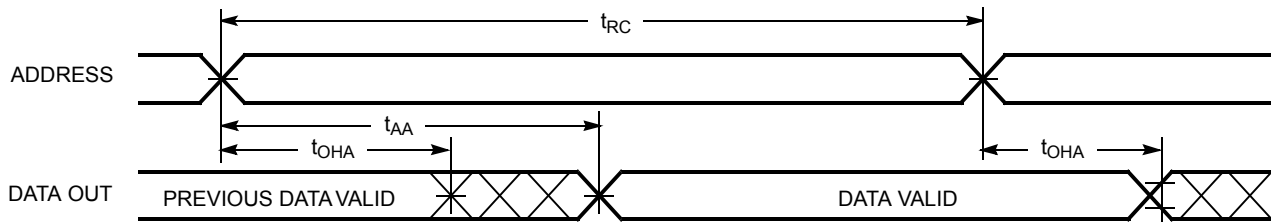


Figure 6. Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access) [15, 18, 19]

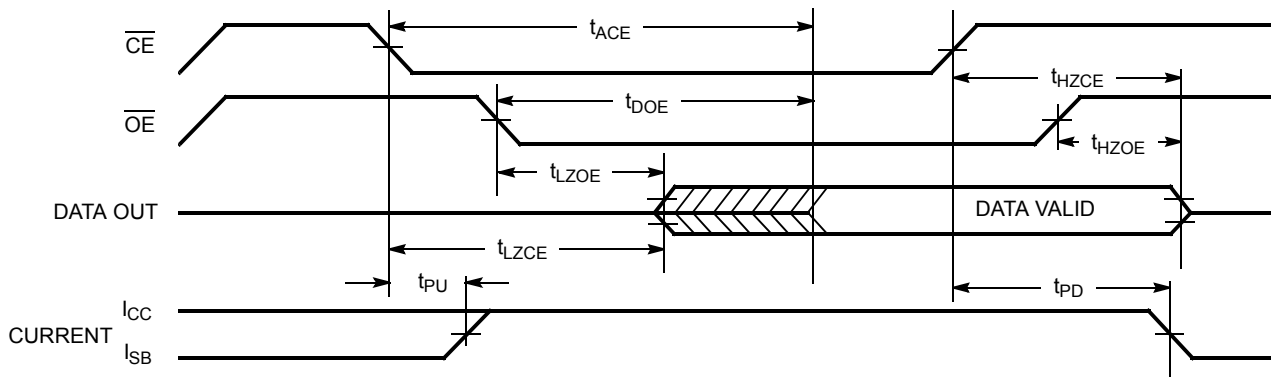
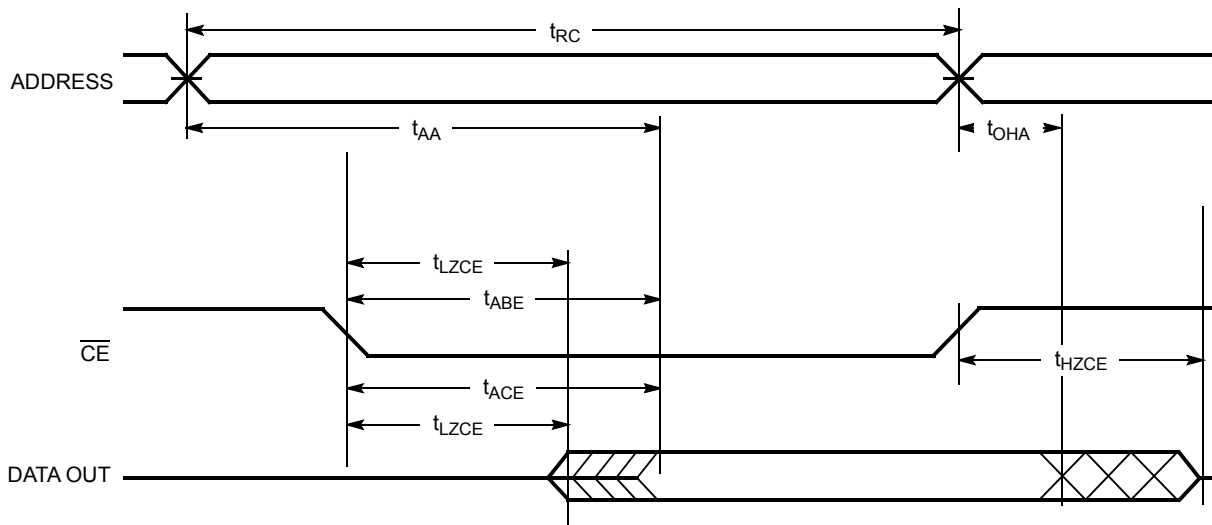


Figure 7. Read Cycle No. 3 (Either Port) [15, 17, 18, 19]



Notes

15. R/W is HIGH for read cycles.
16. Device is continuously selected $\overline{CE} = V_{IL}$. This waveform cannot be used for semaphore reads.
17. $\overline{OE} = V_{IL}$.
18. Address valid prior to or coincident with \overline{CE} transition LOW.
19. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 (R/W Controlled Timing) [20, 21, 22, 23]

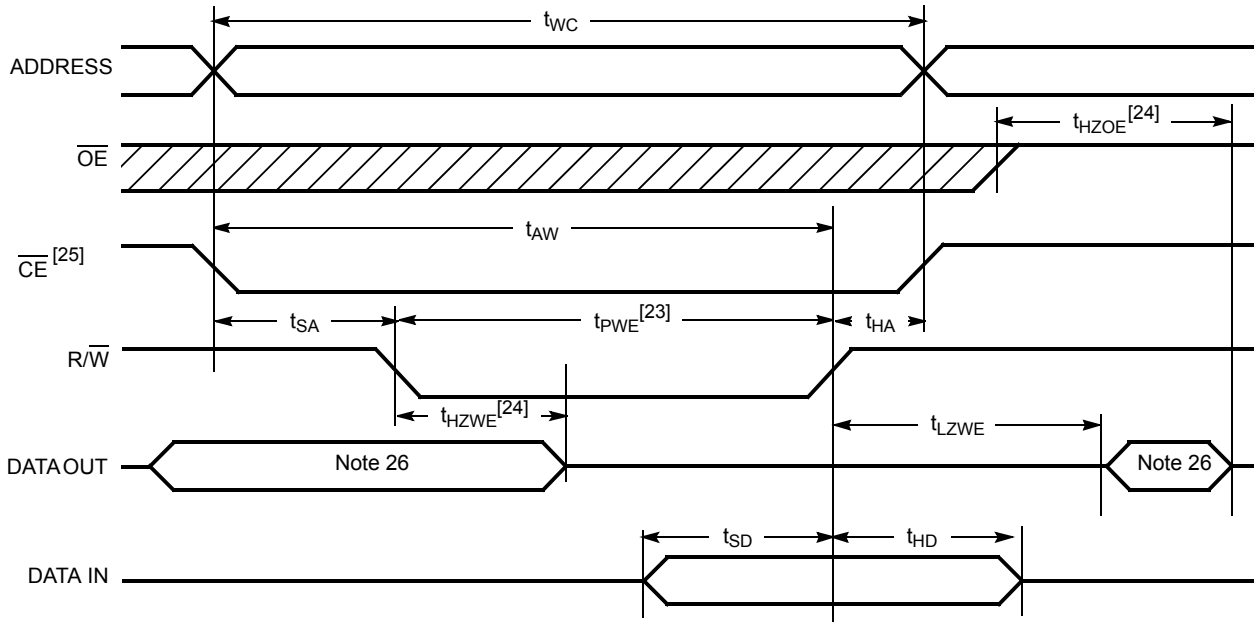
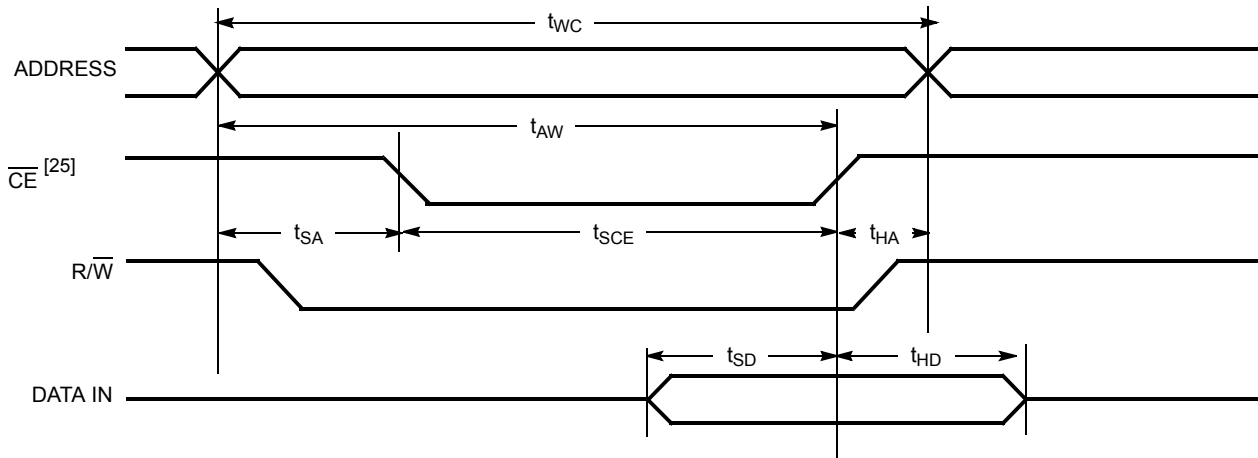


Figure 9. Write Cycle No. 2 (CE Controlled Timing) [20, 21, 22, 27]



Notes

- 20. R/W must be HIGH during all address transitions.
- 21. A write occurs during the overlap (t_{SCE} or t_{PWE}) of a LOW CE or SEM.
- 22. t_{HA} is measured from the earlier of CE or R/W or (SEM or R/W) going HIGH at the end of write cycle.
- 23. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{PWE} or ($t_{HZWE} + t_{SD}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD} . If OE is HIGH during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE} .
- 24. Transition is measured ± 500 mV from steady state with a 5-pF load (including scope and jig). This parameter is sampled and not 100% tested.
- 25. To access RAM, CE = V_{IL} , SEM = V_{IH} .
- 26. During this period, the I/O pins are in the output state, and input signals must not be applied.
- 27. If the CE or SEM LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the high-impedance state.

Switching Waveforms (continued)

Figure 10. Semaphore Read after Write Timing, either Side [28]

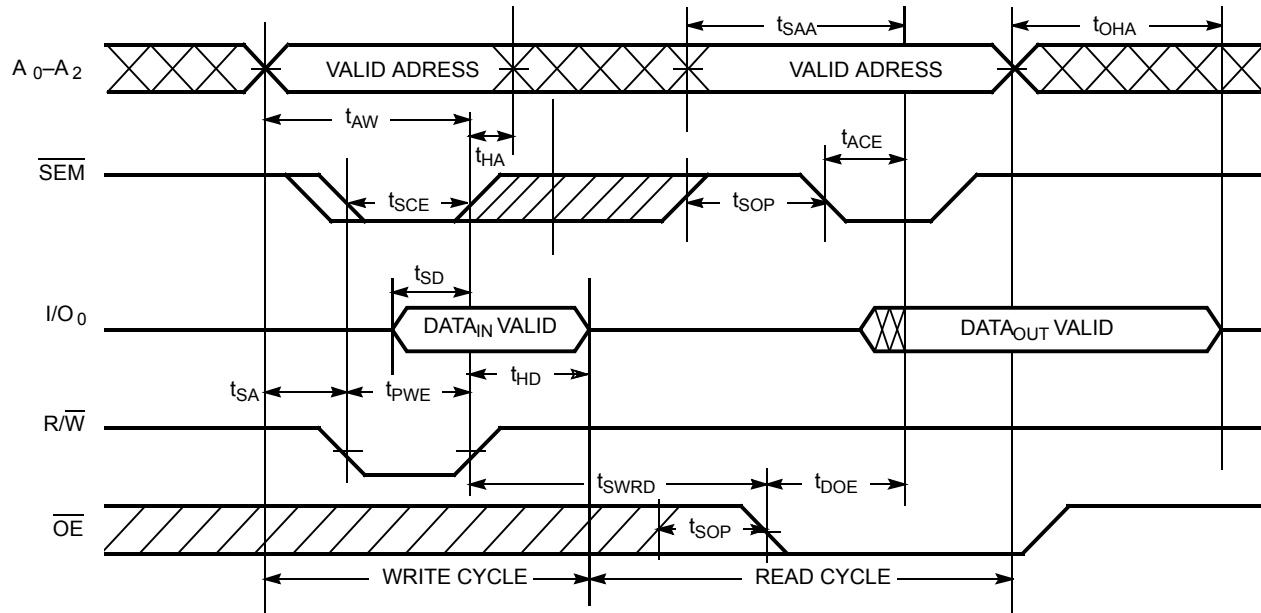
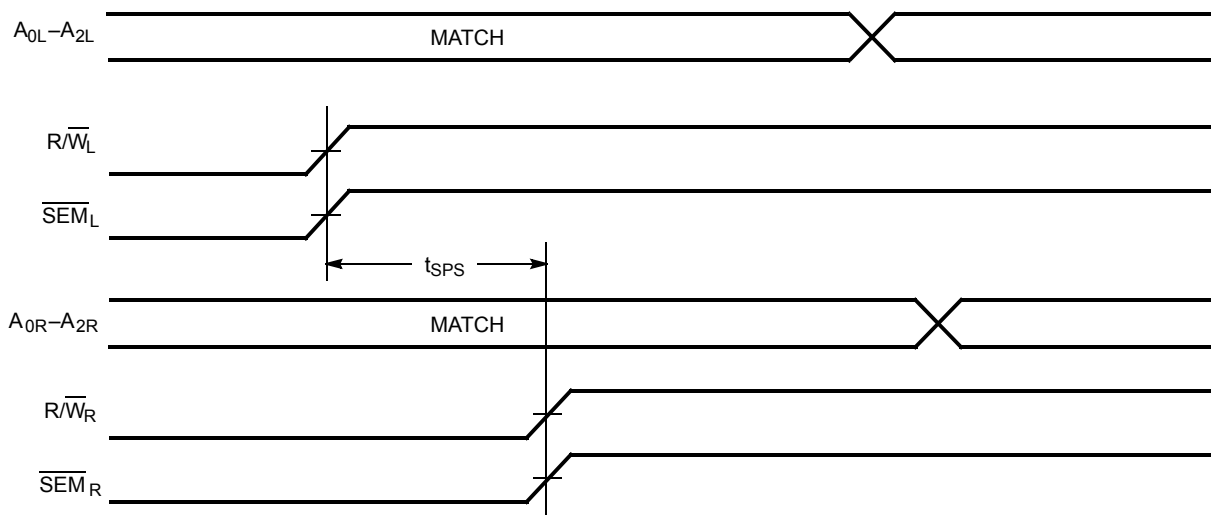


Figure 11. Timing Diagram of Semaphore Contention [29, 30, 31]



Notes

- 28. CE = HIGH for the duration of the above timing (both write and read cycle).
- 29. I/O_{0R} = I/O_{0L} = LOW (request semaphore); CE_R = CE_L = HIGH.
- 30. Semaphores are reset (available to both ports) at cycle start.
- 31. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but which side will get the semaphore is unpredictable.

Switching Waveforms (continued)

Figure 12. Timing Diagram of Read with $\overline{\text{BUSY}}$ ($\overline{\text{M/S}} = \text{HIGH}$) [32]

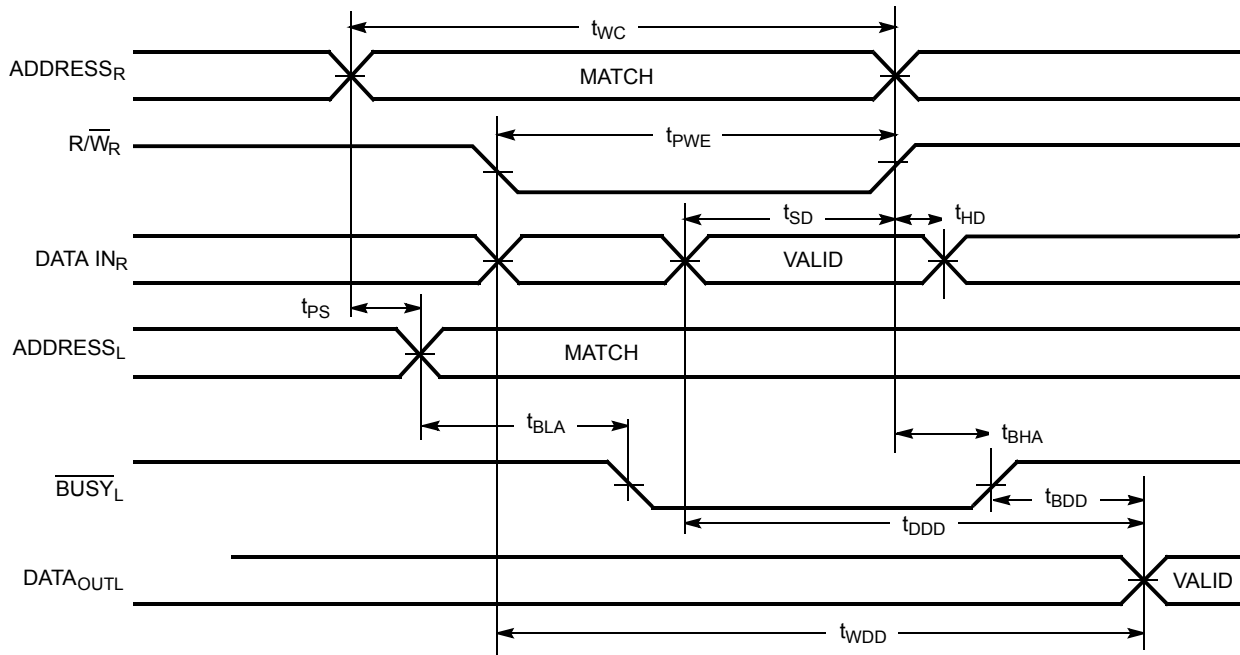
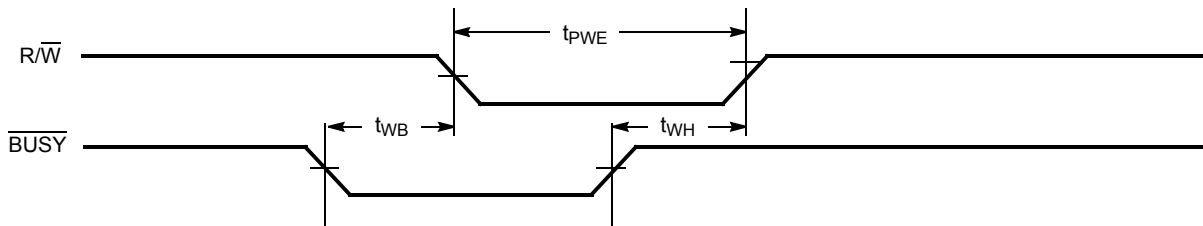


Figure 13. Write Timing with Busy Input ($\overline{\text{M/S}} = \text{LOW}$)



Note
32. $\overline{\text{CE}}_L = \overline{\text{CE}}_R = \text{LOW}$.

Switching Waveforms (continued)

Figure 14. Busy Timing Diagram No.1 (CE Arbitration) [33]

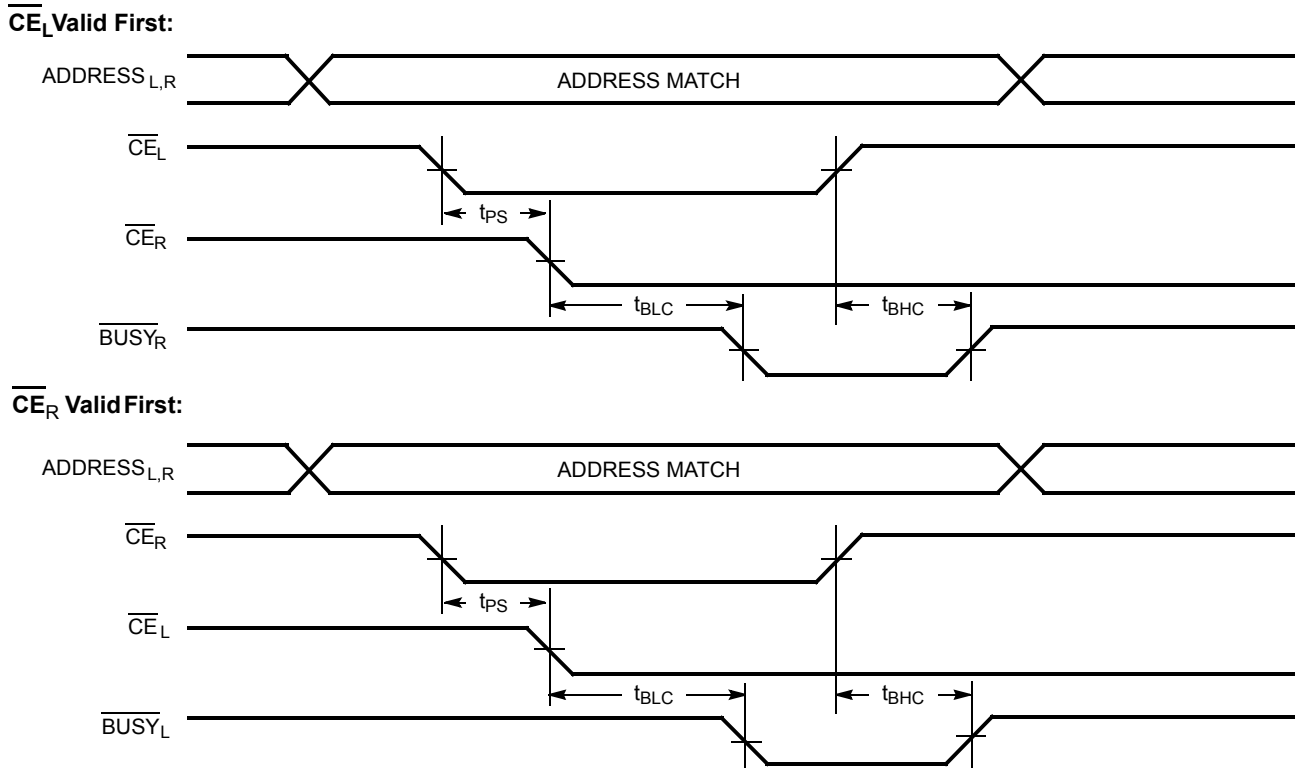
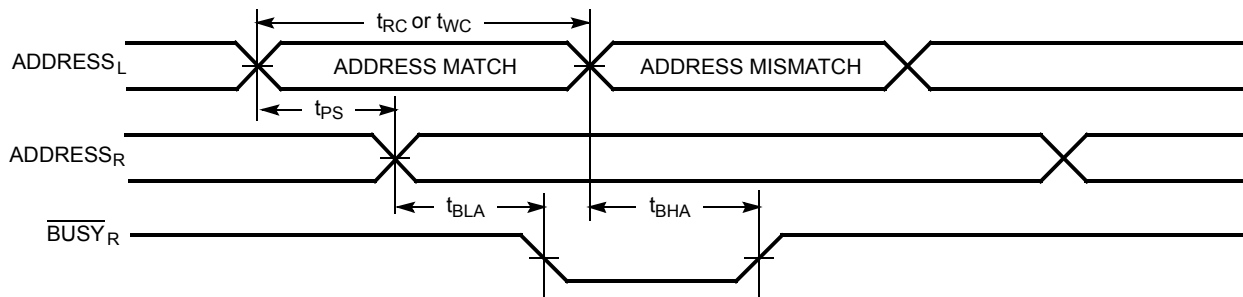
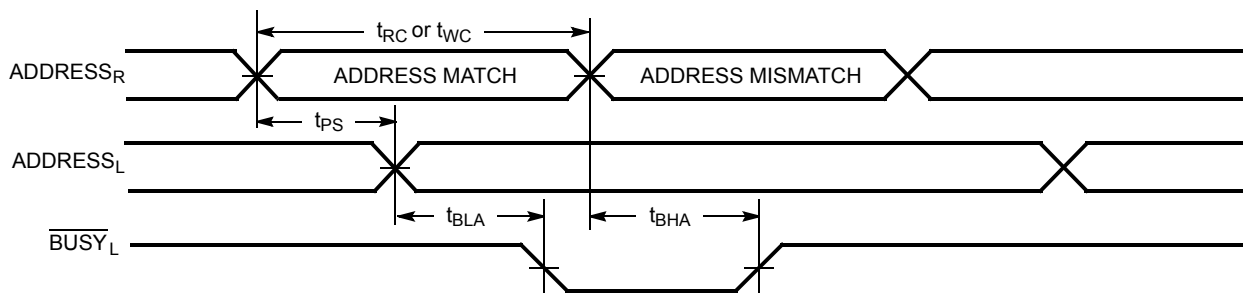


Figure 15. Busy Timing Diagram No.2 (Address Arbitration) [33]

Left Address Valid First



Right Address Valid First:

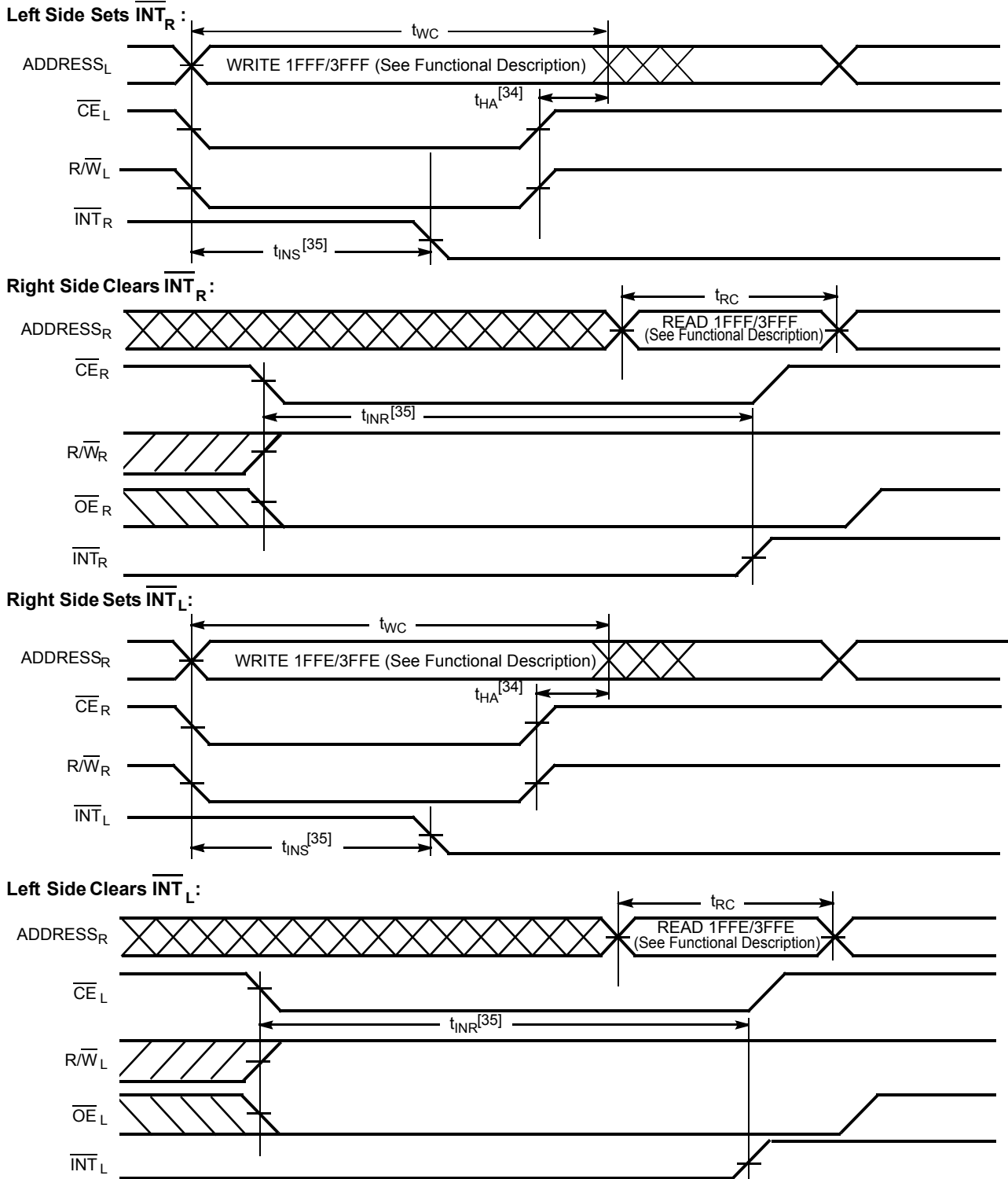


Note

33. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee to which side \overline{BUSY} will be asserted.

Switching Waveforms (continued)

Figure 16. Interrupt Timing Diagrams




Notes

- 34. t_{HA} depends on which enable pin (\overline{CE}_L or R/\overline{W}_L) is deasserted first.
- 35. t_{INS} or t_{INR} depends on which enable pin (\overline{CE}_L or R/\overline{W}_L) is asserted last.

Non-Contending Read/Write

Table 1. Non-Contending Read/Write

| Inputs | | | | Outputs | Operation |
|--------|---|----|-----|------------------------------------|-----------------------------|
| CE | R/W | OE | SEM | I/O ₀ –I/O ₇ | |
| H | X | X | H | High Z | Deselected: Power-down |
| H | H | L | L | Data out | Read data in semaphore flag |
| X | X | H | X | High Z | I/O lines disabled |
| H |  | X | L | Data in | Write into semaphore flag |
| L | H | L | H | Data out | Read |
| L | L | X | H | Data in | Write |
| L | X | X | L | | Not allowed |

Interrupt Operation Example

Table 2. Interrupt Operation Example (assumes $\overline{\text{BUSY}}_L = \overline{\text{BUSY}}_R = \text{HIGH}$)

| Function | Left Port | | | | | Right Port | | | | |
|--|------------------|-----------------|-----------------|---------------------------|-------------------|------------------|-----------------|-----------------|---------------------------|-------------------|
| | R/W _L | CE _L | OE _L | A _{0L–13L} | INT _L | R/W _R | CE _R | OE _R | A _{0R–13R} | INT _R |
| Set Right $\overline{\text{INT}}_R$ flag | L | L | X | 1FFF/3FFF ^[36] | X | X | X | X | X | L ^[37] |
| Reset Right $\overline{\text{INT}}_R$ flag | X | X | X | X | X | X | L | L | 1FFF/3FFF ^[36] | H ^[38] |
| Set Left $\overline{\text{INT}}_L$ flag | X | X | X | X | L ^[38] | L | L | X | 1FFE/3FFE ^[36] | X |
| Reset Left $\overline{\text{INT}}_L$ flag | X | L | L | 1FFE/3FFE ^[36] | H ^[37] | X | X | X | X | X |

Semaphore Operation Example

Table 3. Semaphore Operation Example

| Function | I/O ₀ –I/O ₇ Left | I/O ₀ –I/O ₇ Right | Status |
|----------------------------------|---|--|--|
| No action | 1 | 1 | Semaphore free |
| Left port writes 0 to semaphore | 0 | 1 | Left Port has semaphore token |
| Right port writes 0 to semaphore | 0 | 1 | No change. Right side has no write access to semaphore |
| Left port writes 1 to semaphore | 1 | 0 | Right port obtains semaphore token |
| Left port writes 0 to semaphore | 1 | 0 | No change. Left port has no write access to semaphore |
| Right port writes 1 to semaphore | 0 | 1 | Left port obtains semaphore token |
| Left port writes 1 to semaphore | 1 | 1 | Semaphore free |
| Right port writes 0 to semaphore | 1 | 0 | Right port has semaphore token |
| Right port writes 1 to semaphore | 1 | 1 | Semaphore free |
| Left port writes 0 to semaphore | 0 | 1 | Left port has semaphore token |
| Left port writes 1 to semaphore | 1 | 1 | Semaphore free |

Notes

36. See Functional Description for specific addresses by device part number.

37. If $\overline{\text{BUSY}}_L = \text{L}$, then no change.

38. If $\overline{\text{BUSY}}_R = \text{L}$, then no change.

Ordering Information

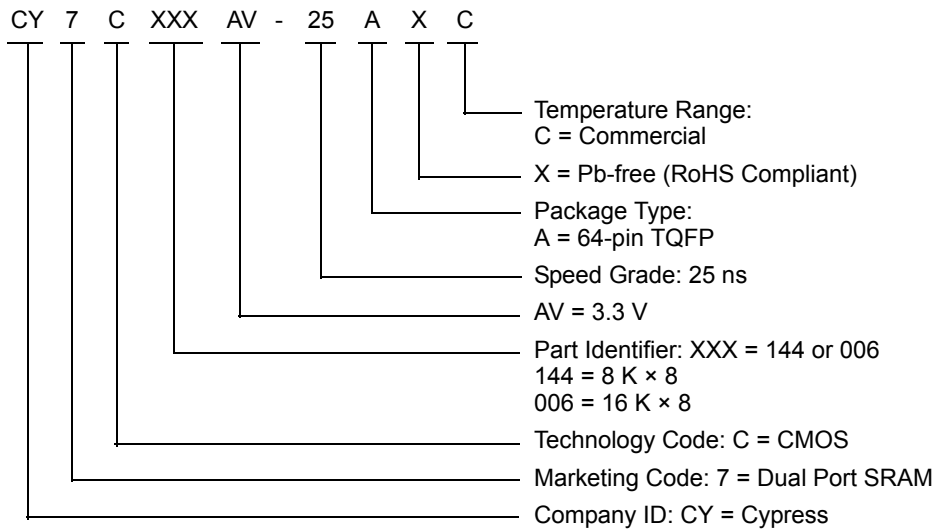
8 K × 8 3.3 V Asynchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|-----------------|--------------|-----------------------|-----------------|
| 25 | CY7C144AV-25AXC | A65 | 64-pin TQFP (Pb-free) | Commercial |

16 K × 8 3.3 V Asynchronous Dual-Port SRAM

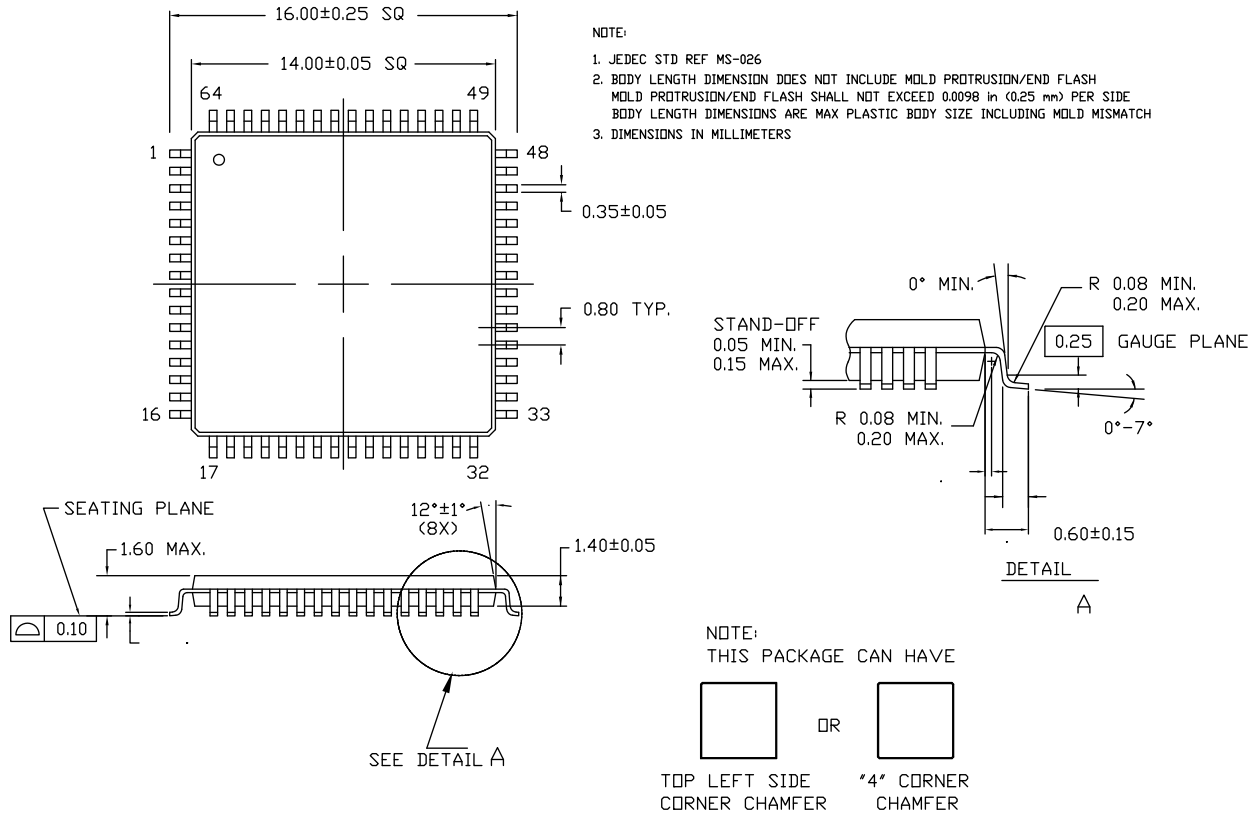
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|-----------------|--------------|-----------------------|-----------------|
| 25 | CY7C006AV-25AXC | A65 | 64-pin TQFP (Pb-free) | Commercial |

Ordering Code Definitions



Package Diagrams

Figure 17. 64-pin TQFP (14 × 14 × 1.4 mm) A64SA Package Outline, 51-85046



Acronyms

| Acronym | Description |
|-----------------|---|
| \overline{CE} | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| \overline{OE} | Output Enable |
| SRAM | Static Random Access Memory |
| TQFP | Thin Quad Flat Pack |
| TTL | Transistor-Transistor Logic |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| mA | milliampere |
| mm | millimeter |
| mV | millivolt |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

Document History Page

| Document Title: CY7C144AV/CY7C006AV, 3.3 V 8 K / 16 K × 8 Asynchronous Dual-Port Static RAM | | | | |
|---|---------|------------|-----------------|--|
| Document Number: 38-06051 | | | | |
| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| ** | 110203 | 12/02/01 | SZV | Change from Spec number: 38-00837 to 38-06051 |
| *A | 122301 | 12/27/02 | RBI | Updated Maximum Ratings (Added Power up requirements to Maximum Ratings Information). |
| *B | 237623 | See ECN | YDT | Updated Features (Removed cross information). |
| *C | 373615 | See ECN | PCX | Added Pb-Free Logo Updated Ordering Information (Added Pb-free parts to ordering information namely CY7C144AV-25AXC, CY7C144AV-25JXC, CY7C006AV-25AXC). |
| *D | 2896210 | 03/22/2010 | RAME | Updated Ordering Information . Updated Package Diagrams . |
| *E | 3161515 | 02/04/2011 | ADMU | Removed information for parts namely CY7C138AV, CY7C139AV, CY7C145AV, CY7C016AV, CY7C007AV, CY7C017AV across the document. Updated Ordering Information (Removed CY7C145AV-20JC). Updated Package Diagrams . |
| *F | 3352067 | 08/23/2011 | ADMU | Updated Features . Updated Operating Range (Removed industrial specification rows). Updated Electrical Characteristics (Removed industrial specification rows). Updated to new template. |
| *G | 3402091 | 10/12/2011 | ADMU | Updated Ordering Information (Removed pruned part CY7C144AV-25AC). Updated Package Diagrams . |
| *H | 3699185 | 08/01/2012 | SMCH | Updated title to read as "CY7C144AV/CY7C006AV, 3.3 V 8 K / 16 K × 8 Asynchronous Dual-Port Static RAM". Updated Switching Characteristics (Removed the Note "Test conditions used are Load 3." and its reference, removed the Note "Test conditions used are Load 2." and its reference, removed the Note "This parameter is guaranteed but not tested. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform." and its reference). Updated Switching Waveforms (Updated Figure 14). |
| *I | 4581667 | 11/27/2014 | SMCH | Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end. Updated Package Diagrams : spec 51-85046 – Changed revision from *E to *F. |
| *J | 4918791 | 09/14/2015 | VINI | Updated Package Diagrams : spec 51-85046 – Changed revision from *F to *G. Updated to new template. Completing Sunset Review. |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

| | |
|--------------------------|--|
| Automotive | cypress.com/go/automotive |
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc |
| Memory | cypress.com/go/memory |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |

PSoC[®] Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

Technical Support

cypress.com/go/support

© Cypress Semiconductor Corporation, 2001-2015. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.