CeraLink™

Capacitor for fast-switching semiconductors

Series/Type:	**Solder pin (SP) series**
Ordering code:	**B58033***
Date:	2016-06-09
Version:	2.2

EPCOS AG is a TDK Group Company.

Applications

- Designed for 650 V semiconductor modules
- Industrial power converters and inverters
- DC link/ snubber capacitor for power converters and inverters

Features

- High ripple current capability
- High temperature robustness
- Low equivalent serial inductance (ESL)
- Low equivalent serial resistance (ESR)
- Low power loss
- Low dielectric absorption
- Optimized for high frequencies up to several 100 kHz
- Increasing capacitance with DC bias up to operating voltage
- High capacitance density
- Minimized dielectric loss at high temperatures
- High reliability
- Qualification based on AEC-Q200 rev. D

Construction

- RoHS-compatible PLZT ceramic (lead lanthanum zirconium titanate)
- Copper inner electrodes
- Silver outer electrodes
- Silver coated copper pins
- Silicone based casting compound to UL 94 V-0
- Plastic housing to UL 94 V-0

Electrical specifications

Maximum peak operating voltage @ $V_{pk,max}$, 25 °C, 60 s	$V_{pk,max}$	**= 650 V**
Rated voltage Reference DC voltage for reliability tests	V_R	**= 500 V**
Operating voltage at maximum attenuation capability	V_{op}	**= 400 V**
Typical nominal capacitance @ Vop, quasistatic, 25 °C. See glossary (page 14) for definition of the nominal capacitance.	$C_{nom,typ}$	**> 20 µF**
Typical effective capacitance @ Vop, 0.5 V_{RMS}, 1 kHz, 25 °C	$C_{eff,typ}$	**= 12 µF**
Initial capacitance @ 0 V_{DC}, 0.5 V_{RMS}, 1 kHz, 25 °C	C_0	**= 6.5 µF ± 20%**
Dissipation factor @ 0 V_{DC}, 0.5 V_{RMS}, 1 kHz, 25 °C	tan δ	**< 0.02**
Insulation resistance @ V_{op}, t > 240 s, 25 °C	$R_{ins,typ}$	**> 1 GΩ**
Operating device temperature	T_{device}	**-40 °C... +150 °C**
Weight of device		**approx. 31 g**

Typical values

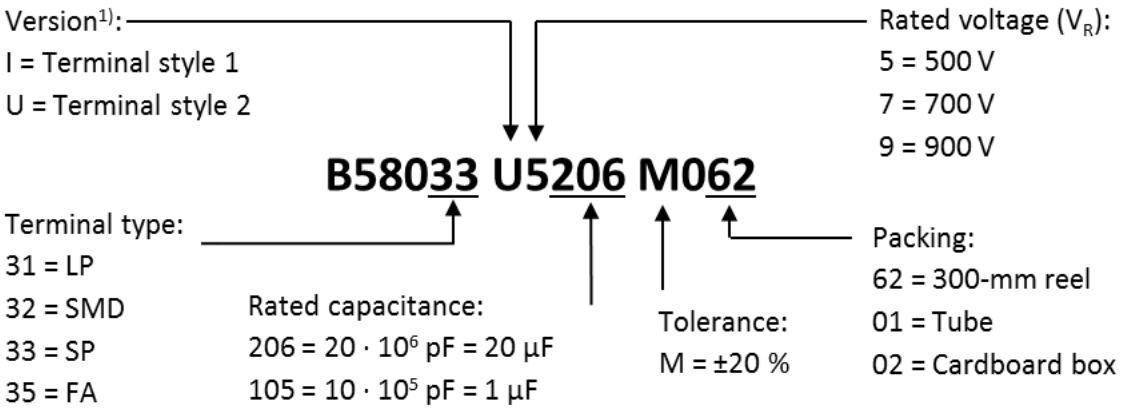
ESR 0 V_{DC}, 0.5 V_{RMS}, 25 °C, 100 kHz	**ESR** 0 V_{DC}, 0.5 V_{RMS}, 25 °C, 1 kHz	**ESL**	**I_{op}** [1)] 100 kHz T_A = 85 °C	**I_{op}** [1)] 100 kHz T_A = 105 °C
mΩ	**mΩ**	**nH**	**A_{RMS}**	**A_{RMS}**
3.5	275	3.5	31.5	24.5

[1)] Normal operating current without forced cooling at T_{device} = 125 °C. Higher values permissible at reduced lifetime.

Ordering code

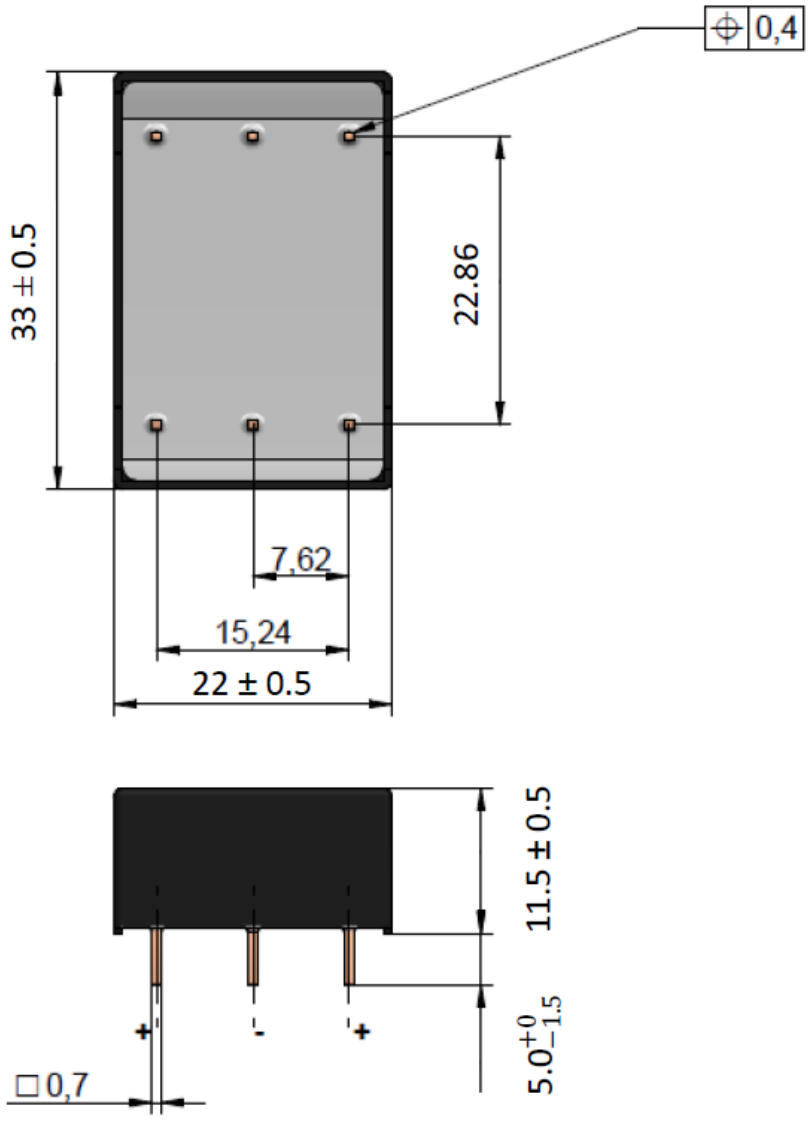
Packaging	Packaging unit pcs.	Ordering code	Rated voltage
Tube	20	B58033I5206M001	500 V

Code construction CeraLink™



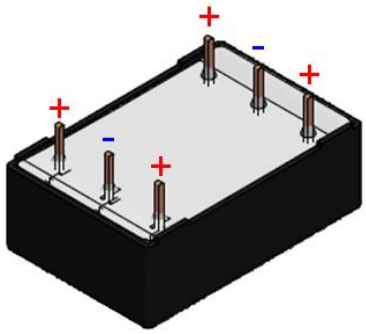
[1] LP series: Terminal style 1 = L-style terminal, Terminal style 2 = J-style terminal

Dimensional drawings

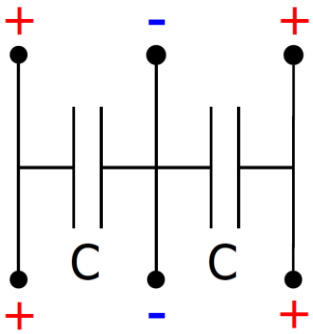


Dimensions in mm

Polarity



Equivalent circuit diagram



Marking of components

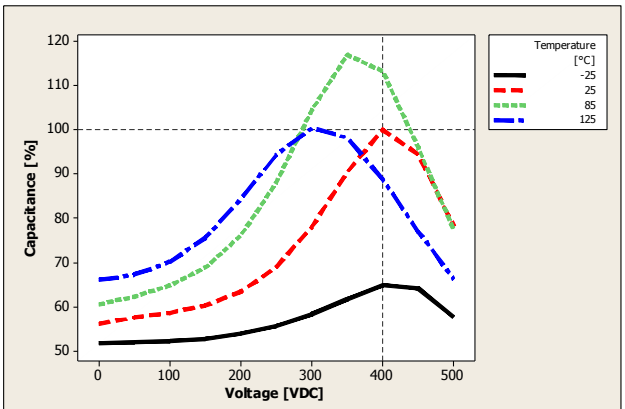
Manufacturer's logo
CeraLink™ type
Nominal capacitance
Rated voltage
Lot number, 9 digits

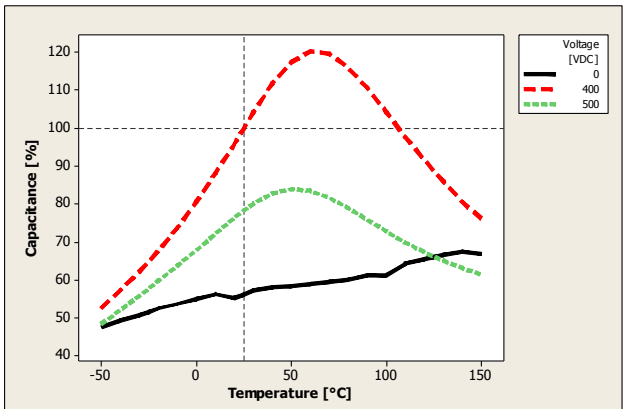
Typical characteristics as a function of temperature and voltage

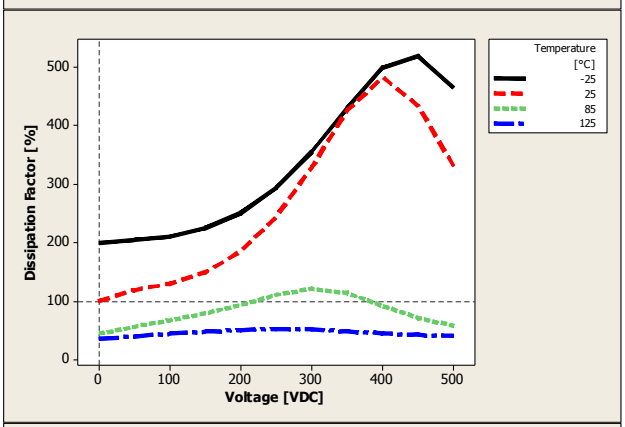
(V_{AC} = 0.5 V_{RMS}, frequency = 1 kHz)

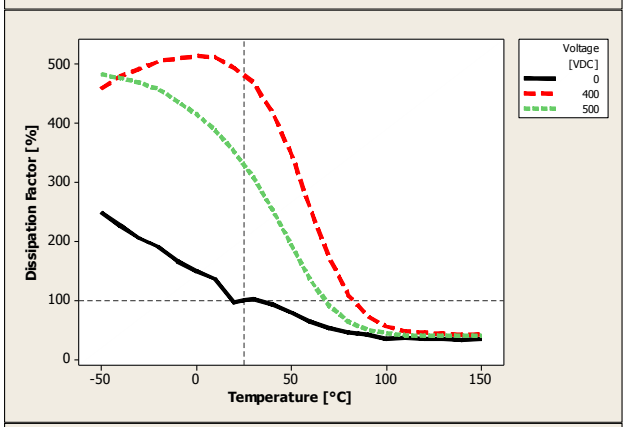
All given temperatures are device temperatures.

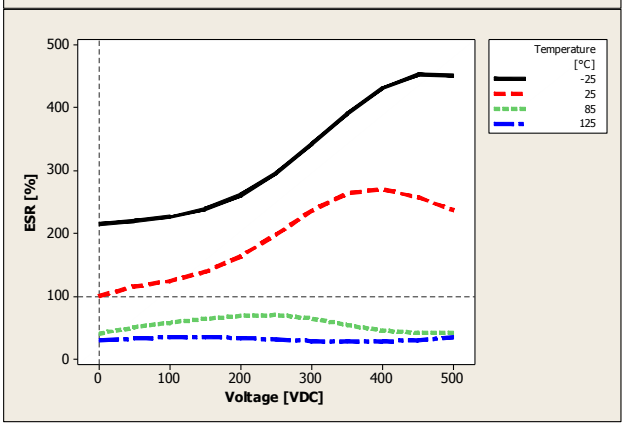
The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100% values correspond to $C_{eff,typ}$ and tan δ which are given on page 3 of this data sheet.

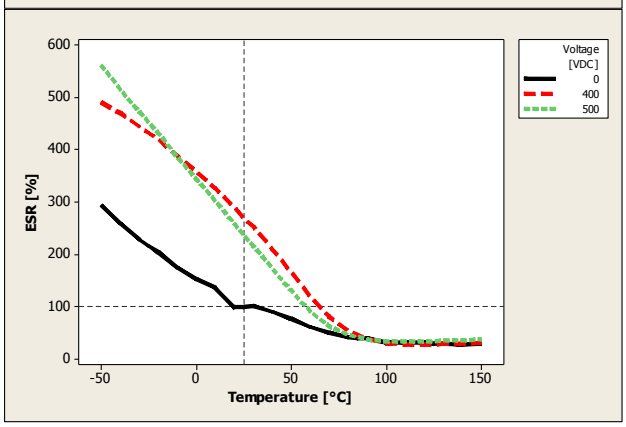




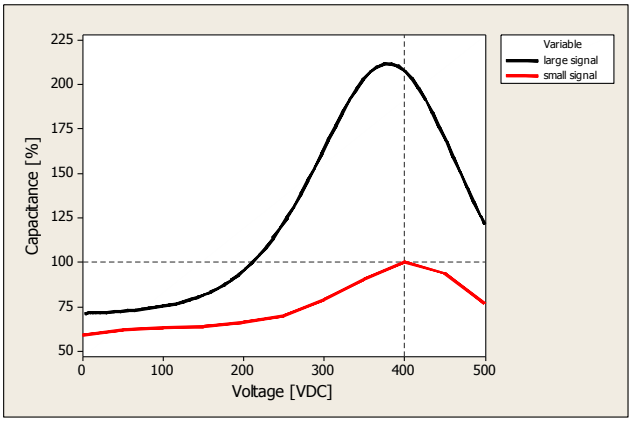








Typical capacitance values as a function of voltage

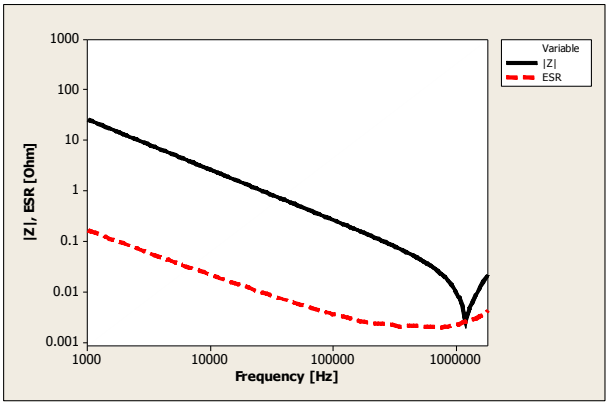


Large signal capacitance:
Quasistatic (slow variation of the voltage), 25 °C
The nominal capacitance is defined as the large signal capacitance at V_{op}.
See glossary for further information.

Small signal capacitance:
0.5 V_{RMS}, 1 kHz, 25 °C

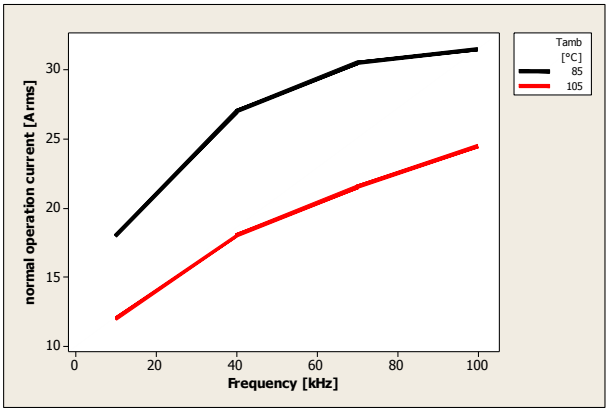
The effective capacitance is defined as the small signal capacitance at V_{op}.

Typical impedance and ESR as a function of frequency



V_{DC} = 0 V, V_{AC} = 0.5 V_{RMS}, T_{device} = 25 °C

Typical permissible current as a function of frequency



Measurement performed at V_{op}.
The values correspond to a device temperature of 125 °C.
No active cooling was used.

Aging

The capacitance has an aging behavior which shows a decrease of capacitance with time.
The typical aging rate is about 2.5% per logarithmic decade in hours.

Reliability

A. Preconditioning:

- Solder the capacitor on a PCB using the recommended soldering profile
- Check of external appearance
- Measurement of electrical parameters R_{ins}, C_0, tan δ
    - Apply $V_{pk,max}$ for 60 seconds and measure R_{ins} at room temperature:
      Isolation resistance (@$V_{pk,max}$, 60 s, 25 °C) **R_{ins} > 100 MΩ**
    - Measure C_0 and tan δ within 10 minutes to 1 hour afterwards:
      Initial capacitance (@ 0 V_{DC}, 0.5 V_{RMS}, 1 kHz, 25 °C) **C_0 = 6.5 µF ± 20%**
      Dissipation factor (@ 0 V_{DC}, 0.5 V_{RMS}, 1 kHz, 25 °C) **tan δ < 0.02**

B. Performance of a specific reliability test.

C. After performing a specific test:

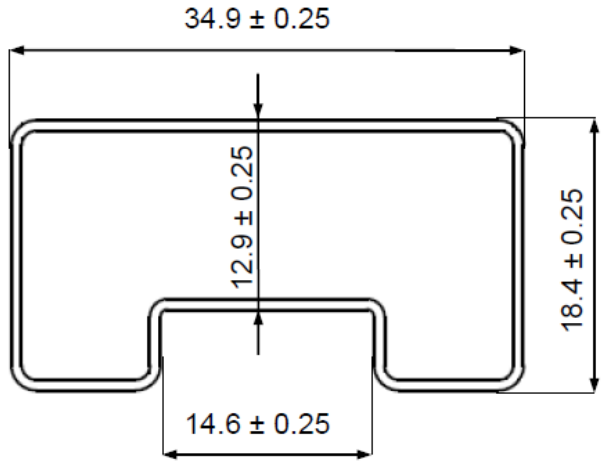
- Check the external appearance again
- Repeat the measurement of the electrical parameters
    - Apply $V_{pk,max}$ for 60 seconds and measure R_{ins} at room temperature:
      Isolation resistance (@$V_{pk,max}$, 60 s, 25 °C) **R_{ins} > 10 MΩ**
    - Measure C_0 and tan δ:
      Change of initial capacitance (@ 0 V_{DC}, 0.5 V_{RMS}, 1 kHz, 25 °C) **| Δ C_0 / C_0 | < 15%**
    - Dissipation factor (@ 0 V_{DC}, 0.5 V_{RMS}, 1 kHz, 25 °C) **tan δ < 0.05**

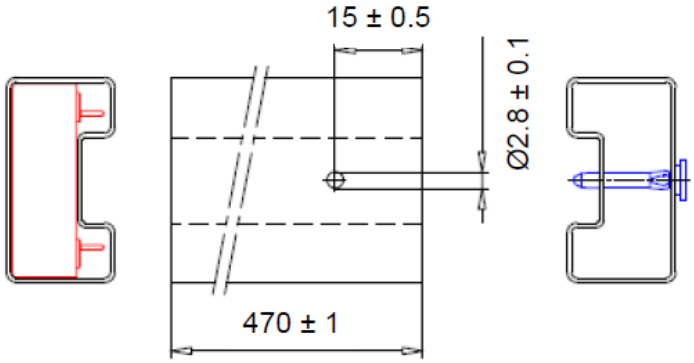
Test	Standard	Test conditions	Criteria
External appearance		Visual inspection with magnifying glass	No defects that might affect performance
High temperature operating life	MIL-STD-202, method 108	150 °C, V_R, 1000 hours	No mechanical damage Δ C_0, tan δ and R_{ins} within defined limits
High temperature exposure	MIL-STD-202, method 108	150 °C, unpowered, 1000 hours	No mechanical damage Δ C_0, tan δ and R_{ins} within defined limits
Biased humidity	MIL-STD-202, method 103	85 °C, 85% rel. hum., V_R, 1000 hours	No mechanical damage Δ C_0, tan δ and R_{ins} within defined limits
Moisture resistance	MIL-STD-202, method 106	25 °C to 65 °C 90% rel. hum. to 100% rel. hum. 10 cycles, unpowered	No mechanical damage Δ C_0, tan δ and R_{ins} within defined limits

Test	Standard	Test conditions	Criteria
Temperature shock	MIL-STD-202, method 107	-55 °C to +150 °C 20 seconds transfer time 15 minutes dwell time 1000 cycles	No mechanical damage ΔC_0, tan δ and R_{ins} within defined limits
Vibration	MIL-STD-202, method 204	5 g/ 20 min, 12 cycles, 3 axis 10 Hz to 2000 Hz	No mechanical damage ΔC_0, tan δ and R_{ins} within defined limits
Mechanical shock	MIL-STD-202, method 213	Acceleration 400 m/s² Half sine pulse duration 6 milliseconds 4000 bumps	No mechanical damage ΔC_0, tan δ and R_{ins} within defined limits
Resistance to soldering heat	MIL-STD-202, method 210, condition B	Dip test of contact areas in solder bath (260 °C for 10 seconds)	No damage of pin silver coating ΔC_0, tan δ and R_{ins} within defined limits
Solderability	J-STD-002, method A	Dip test of contact areas in solder bath (235 °C for 5 seconds)	Dipped surface is covered with solder coating
Resistance to solvent		Dipping and cleaning with isopropanol	Marking must be legible ΔC_0, tan δ and R_{ins} within defined limits
Geometry		Using a caliper and a gauge	Within specified values in the chapter dimensional drawing

Packaging

The CeraLink™ will be delivered in a tube and will be packed in a cardboard box.
The packaging unit is 20 pieces per tube. The tube is terminated with one pin and two plugs.

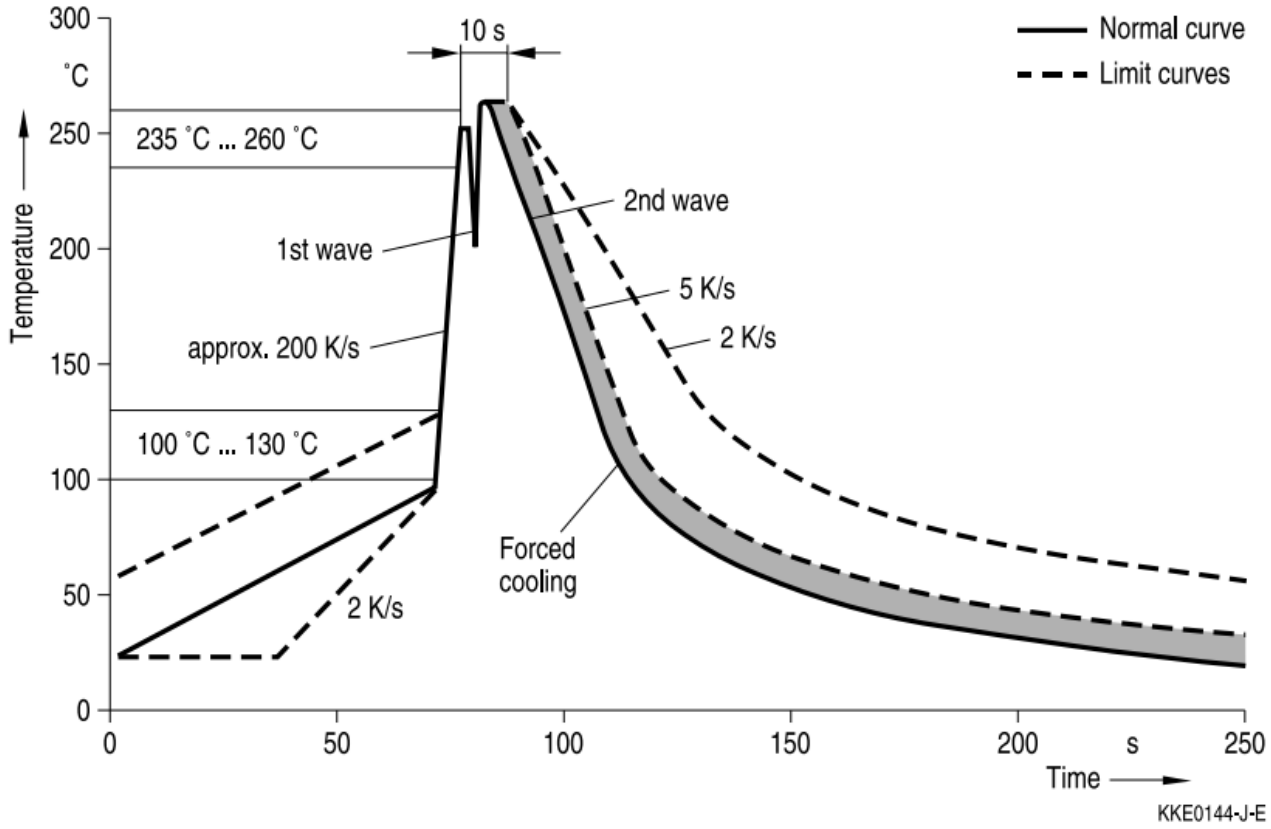




Dimensions in mm

Recommended wave soldering profile

Temperature characteristic at component terminal with dual-wave soldering



Notes:

The use of mild, non-activated fluxes for soldering is recommended, as well as proper cleaning of the PCB.

After the soldering process, the capacitance is lowered. Applying V_R to the device will re-establish the capacitance.

The components are suitable for reflow soldering to JEDEC J-STD-020D.

General technical information

Storage

- Only store CeraLink™ capacitors in their original packaging. Do not open the package prior to processing.
- Storage conditions in original packaging: temperature −25 °C to +45 °C, relative humidity ≤ 75% annual average, maximum 95%, dew precipitation is inadmissible.
- Do not store CeraLink™ capacitors where they are exposed to heat or direct sunlight. Otherwise the packaging material may be deformed or CeraLink™ may stick together, causing problems during mounting.
- Avoid contamination of the CeraLink™ surface during storage, handling and processing.
- Avoid storing CeraLink™ devices in harmful environments where they are exposed to corrosive gases (e.g. SOx, Cl).
- Use CeraLink™ as soon as possible after opening factory seals such as polyvinyl-sealed packages.
- Solder CeraLink™ components within 6 months after shipment from EPCOS.

Handling

- Do not drop CeraLink™ components or allow them to be chipped.
- Do not touch CeraLink™ with your bare hands - gloves are recommended.
- Avoid contamination of the CeraLink™ surface during handling.

Mounting

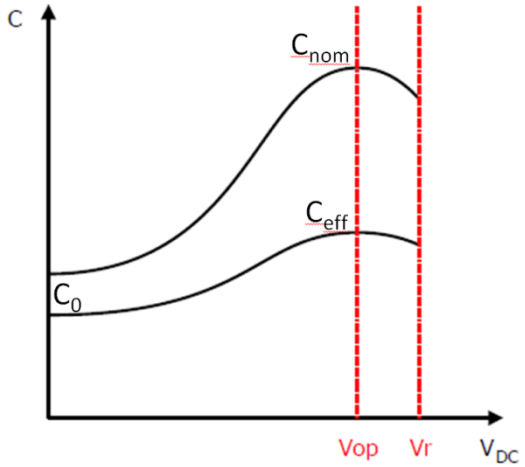
- Do not scratch the external electrodes before, during or after the mounting process.
- Make sure contacts and housings used for assembly with CeraLink™ components are clean before mounting.
- The surface temperature of an operating CeraLink™ can be higher than the ambient temperature. Ensure that adjacent components are placed at a sufficient distance from a CeraLink™ to allow proper cooling.
- Avoid contamination of the CeraLink™ surface during processing.

Soldering guidelines

- The use of mild, non-activated fluxes for soldering is recommended, as well as proper cleaning of the PCB.
- Complete removal of flux is recommended to avoid surface contamination that can result in an instable and/or high leakage current.
- Use resin-type or non-activated flux.
- Bear in mind that insufficient preheating may cause ceramic cracks.

- Rapid cooling by dipping in solvent is not recommended, otherwise a component may crack.
- If an unsuitable cleaning fluid is used, flux residue or foreign particles may stick to the CeraLink™ surface and deteriorate its insulation resistance. Insufficient or improper cleaning of the CeraLink™ may cause damage to the component.

Glossary



Initial capacitance C_0:	Is the value at the origin of the hysteresis without any applied direct voltage.
Effective capacitance C_{eff}:	Occurs at V_{op} and is measured with an applied ripple voltage of 0.5 V_{RMS} and 1 kHz. The CeraLink™ is designed to have its highest capacitance value at the operating voltage V_{op}.
Nominal capacitance C_{nom}:	Is the value derived by the tangent of the mean hysteresis as the derivation of the mean hysteresis is dQ/dV ~ C.

Symbols and terms

AC	Alternating current
C_0	Initial capacitance
$C_{eff,typ}$	Typical effective capacitance
$C_{nom,typ}$	Typical nominal capacitance
DC	Direct current
ESL	Equivalent serial inductance
ESR	Equivalent serial resistance
I_{op}	Operating ripple current, root mean square value of sinusoidal AC current
PCB	Printed circuit board
PLZT	Lead lanthanum zirconium titanate
R_{ins}	Insulation resistance
T_A	Ambient temperature
tan δ	Dissipation factor
T_{device}	Device temperature. $T_{device} = T_A + \Delta T$ (ΔT defines the self-heating of the device due to applied current).
V_{op}	Operating voltage
V_R	Rated voltage
V_{RMS}	Root mean square value of sinusoidal AC voltage
V_{ws}	Withstand voltage
ΔT	Increase of temperature during operation

Cautions and warnings

General

Not for use in resonant circuits, where a voltage of alternating polarity occurs.

Not for AC applications. Consult your sales representative for further details.

If used in snubber circuits, ensure that the sum of all voltages remains at the same polarity.

Some parts of this publication contain statements about the suitability of our CeraLink™ components for certain areas of application, including recommendations about incorporation/design-in of these products into customer applications. The statements are based on our knowledge of typical requirements often made of our CeraLink™ devices in the particular areas. We nevertheless expressly point out that such statements cannot be regarded as binding statements about the suitability of our CeraLink™ components for a particular customer application. As a rule, EPCOS is either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always incumbent on the customer to check and decide whether the CeraLink™ devices with the properties described in the product specification are suitable for use in a particular customer application.

- Do not use EPCOS CeraLink™ components for purposes not identified in our specifications.
- Ensure the suitability of a CeraLink™ in particular by testing it for reliability during design-in. Always evaluate a CeraLink™ component under worst-case conditions.
- Pay special attention to the reliability of CeraLink™ devices intended for use in safety-critical applications (e.g. medical equipment, automotive, spacecraft, nuclear power plant).

Design notes

- Consider derating at higher operating temperatures. As a rule, lower temperatures and voltages increase the life time of CeraLink™ devices.
- If steep surge current edges are to be expected, make sure your design is as low-inductive as possible.
- In some cases the malfunctioning of passive electronic components or failure before the end of their service life cannot be completely ruled out in the current state of the art, even if they are operated as specified. In applications requiring a very high level of operational safety and especially when the malfunction or failure of a passive electronic component could endanger human life or health (e.g. in accident prevention, life-saving systems, or automotive battery line applications such as clamp 30), ensure by suitable design of the application or other measures (e.g. installation of protective circuitry, fuse or redundancy) that no injury or damage is sustained by third parties in the event of such a malfunction or failure.
- Specified values only apply to CeraLink™ components that have not been subject to prior electrical, mechanical or thermal damage. The use of CeraLink™ devices in line-to-ground applications is therefore not advisable, and it is only allowed together with safety countermeasures such as thermal fuses.

Operation

- Use CeraLink™ only within the specified operating temperature range.
- Use CeraLink™ only within specified voltage and current ranges.
- The CeraLink has to be operated in a dry atmosphere, which must not contain any additional chemical vapors or substances.
- Environmental conditions must not harm the CeraLink™. Use the capacitors under normal atmospheric conditions only. A reduction of the oxygen partial pressure to below 1 mbar is not permissible.
- Prevent a CeraLink™ from contacting liquids and solvents.
- Avoid dewing and condensation.
- During operation, the CeraLink™ can produce audible noise due to its piezoelectric characteristic.
- EPCOS CeraLink™ components are mainly designed for encased applications. Under all circumstances avoid exposure to:
    - direct sunlight
    - rain or condensation
    - steam, saline spray
    - corrosive gases
    - atmosphere with reduced oxygen content

This listing does not claim to be complete, but merely reflects the experience of EPCOS AG.

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1. Some parts of this publication contain **statements about the suitability of our products for certain areas of application**. These statements are based on our knowledge of typical requirements that are often placed on our products in the areas of application concerned. We nevertheless expressly point out **that such statements cannot be regarded as binding statements about the suitability of our products for a particular customer application.** As a rule, EPCOS is either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always ultimately incumbent on the customer to check and decide whether an EPCOS product with the properties described in the product specification is suitable for use in a particular customer application.
2. We also point out that **in individual cases, a malfunction of electronic components or failure before the end of their usual service life cannot be completely ruled out in the current state of the art, even if they are operated as specified.** In customer applications requiring a very high level of operational safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health (e.g. in accident prevention or life-saving systems), it must therefore be ensured by means of suitable design of the customer application or other action taken by the customer (e.g. installation of protective circuitry or redundancy) that no injury or damage is sustained by third parties in the event of malfunction or failure of an electronic component.
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