

## Features

- ▶ 2-port IO-Link Master
- ▶ Integrated UART-Interface for each port
- ▶ Output drivers with typical 1 Ω
- ▶ Supporting external PMOS switches for IO-Link supply (L+) with current limitation
- ▶ Wake-up generation support
- ▶ Supply voltage range  
 $V_{VDDH}$ : 8V – 32V /  $V_{VDD}$ : 3.15V - 3.45V
- ▶ Over-current & short-circuit protection at output stages with configurable thresholds
- ▶ Digital inputs configurable for IO-LINK or IEC 61131-2 compatible interface
- ▶ SPI for communication, configuration, and diagnosis
- ▶ Under voltage monitor for all supplies
- ▶ Over temperature protection

## Applications

- ▶ IO-Link Master application in modular SPS
- ▶ Gateway applications

## General Description

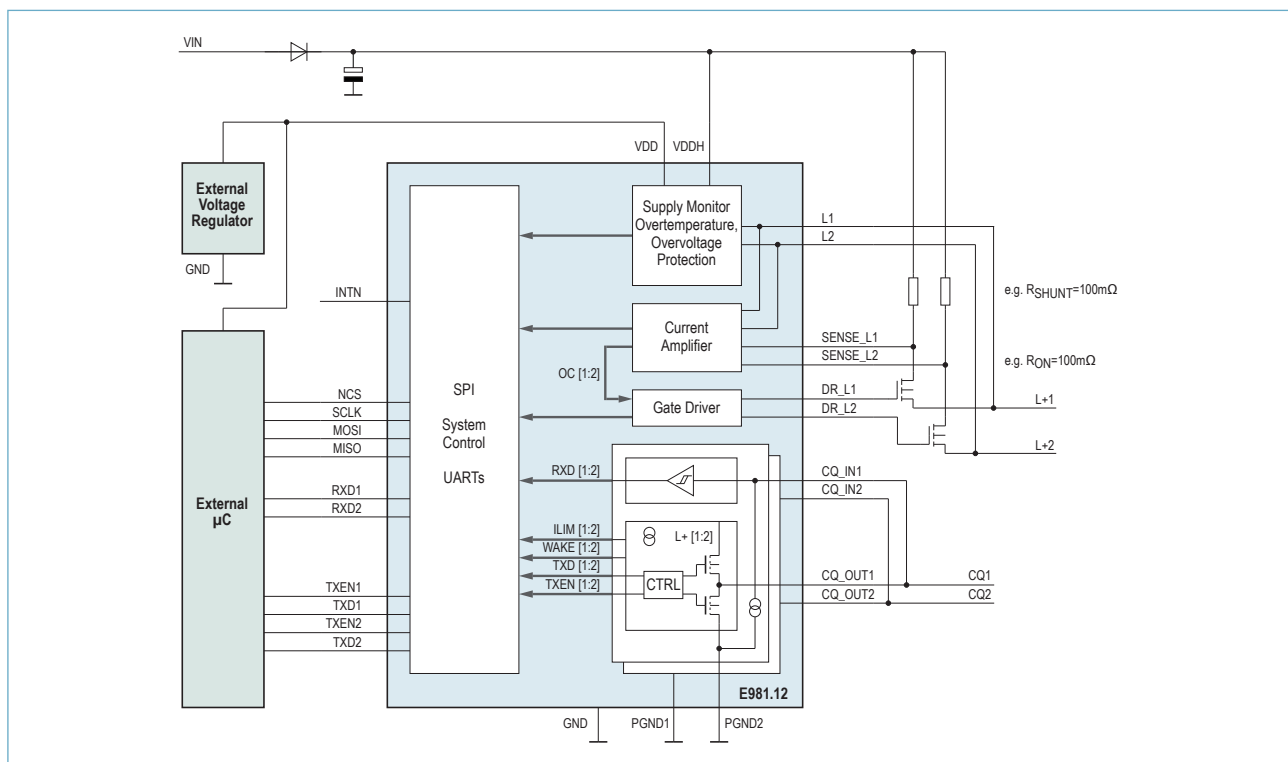
This device comes with two independently operating IO-Link MASTER PHYs which make it a perfect fit for 2/4/8/16-port Master applications. Especially for multi-port applications the integrated UARTs offer you high flexibility regarding scalability of Master ports and the choice of the  $\mu\text{C}$  used for the application. As the E981.12 allows the support of external MOSFETs for sensor supply, it enables cost-effective and power dissipation optimized system concepts.

The dual IO-Link Master is also available as SIP at RENE-SAS with embedded microcontroller for protocol handling.

## Ordering Information

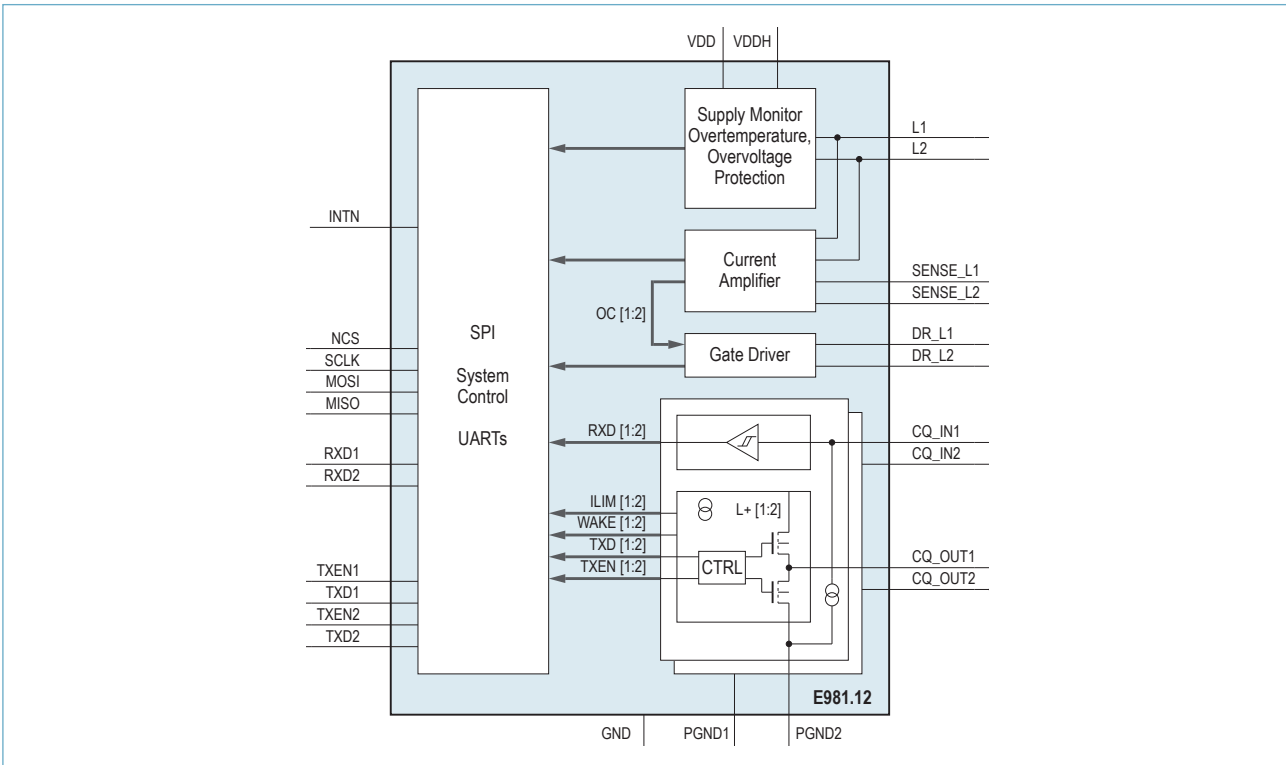
Ordering No.:	Ambient Temp. Range	Package
E98112A39B	-40°C to +105°C	QFN44L7

## Typical Application Circuit

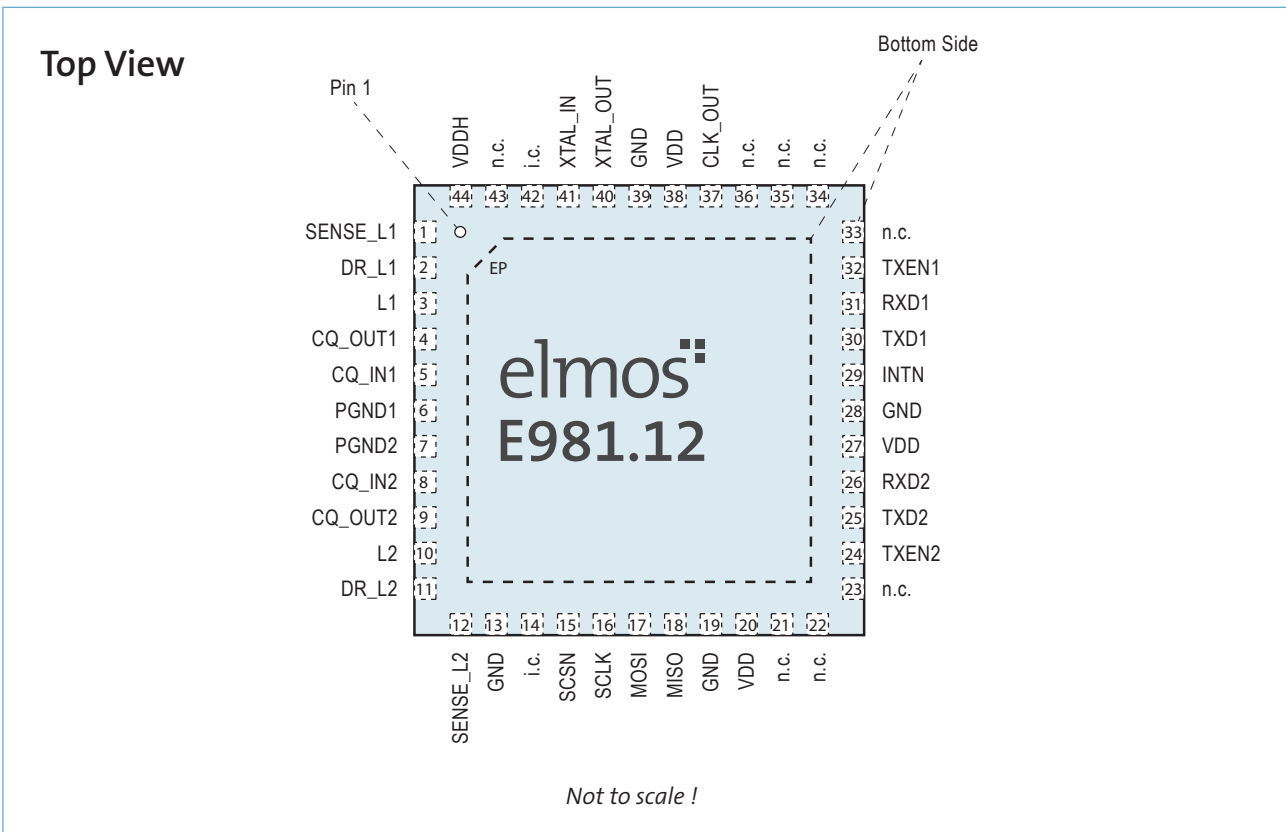


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### Functional Diagram



### Pin Configuration



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## Pin Description

Pin	Name	Type <sup>1)</sup>	Description
1	SENSE_L1	HV_A_I	Supply current sense input channel 1
2	DR_L1	HV_A_O	PMOS Gate control output channel 1
3	L1	HV_S	Transceiver supply input channel 1
4	CQ_OUT1	HV_A_O	Transmitter output channel 1
5	CQ_IN1	HV_A_I	Receiver / general purpose input channel 1
6	PGND1	HV_S	Power ground channel 1
7	PGND 2	HV_S	Power ground channel 2
8	CQ_IN2	HV_A_I	Receiver / general purpose input channel 2
9	CQ_OUT2	HV_A_O	Transmitter output channel 2
10	L2	HV_S	Transceiver supply input channel 2
11	DR_L2	HV_A_O	PMOS Gate control output channel 2
12	SENSE_L2	HV_A_I	Supply current sense input channel 2
13	GND	S	System ground
14	i.c.		Internally connected. For factory use only. Connect to GND in application
15	SCSN	D_I	SPI chip select input
16	SCLK	D_I	SPI serial clock input
17	MOSI	D_I	SPI master output slave input (data input)
18	MISO	D_O	SPI master input slave output (data output)
19	GND	S	System ground
20	VDD	S	3.3V voltage supply
21	n.c.		not connected
22	n.c.		not connected
23	n.c.		not connected
24	TXEN2	D_I	Transmitter enable channel 2
25	TXD2	D_I	Transmitter input channel 2
26	RXD2	D_O	Receiver output channel 2
27	VDD	S	3.3V voltage supply
28	GND	S	System ground
29	INTN	D_O	Interrupt output (low active)
30	TXD1	D_I	Transmitter input channel 1
31	RXD1	D_O	Receiver output channel 1
32	TXEN1	D_I	Transmitter enable channel 1
33	n.c.		not connected
34	n.c.		not connected
35	n.c.		not connected
36	n.c.		not connected
37	CLK_OUT	D_O	Clock output port
38	VDD	S	3.3V voltage supply
39	GND	S	System ground

1) A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

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Pin	Name	Type <sup>1)</sup>	Description
40	XTAL_OUT	D_O	External quartz
41	XTAL_IN	D_I	External quartz
42	i.c.		Internally connected. For factory use only. To be left open in application
43	n.c.		not connected
44	VDDH	S	High-voltage supply input
-	EP	S	Exposed Die Pad

1) A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

## 1 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages with respect to ground. Currents flowing into terminals are positive, those drawn out of a terminal are negative.

PGND1, PGND2, GND1 and the package exposed pad must be soldered to the same GND potential.

Description	Condition	Symbol	Min	Max	Unit
DC voltage at pin VDDH	continuous	$V_{SUP}$	-0.3	40	V
Transient voltage at pin VDDH (ESD, burst, surge)	$t < 500\mu s$	$V_{SUP,trans}$	-0.3	60	V
DC input voltage at pins CQ_INx	continuous	$V_{CQ\_IN\_dc}$	-5	40	V
DC input voltage at pins CQ_OUTx	continuous	$V_{CQ\_OUT\_dc}$	-0.3	$V_{DDH}+0.3$	V
DC voltage at pins Lx, SENSE_Lx, DR_Lx	continuous	$V_{L\_CTRL}$	-0.3	$V+0.3$	V
Synchronous transient voltage at pins CQ_OUTx and Lx	$t < 500\mu s$	$V_{L\_CTRL,trans}$	-0.3	60	V
Continuous DC voltage at VDD	continuous	$V_{VDD}$	-0.3	3.6	V
Voltage range for digital interface pins RXDx, TXDx, TXENx, INTN, MISO, MOSI, SCLK, SCSN	continuous	$V_{IF}$	-0.3	$V_{DD}+0.3$	V
Maximum IO current at each pin, if not specified otherwise		$I_{IO\_LUP}$	-10	10	mA
Junction temperature	continuous	$T_J$		150	°C
Storage temperature		$T_{STG}$	-40	150	°C
ESD protection at pins CQ_OUTx and CQ_INx	AEC-Q100-002 R=1.5k $\Omega$ , C=100pF chip level test	$V_{CQ\_ESD\_HBM}$	6		kV
ESD protection at pin VDDH	AEC-Q100-002 R=1.5k $\Omega$ , C=100pF chip level test	$V_{VDDH\_ESD\_HBM}$	6		kV
ESD protection at pins CQ_OUTx and CQ_INx	IEC 61000-4-2 R=330 $\Omega$ , C=150pF	$V_{CQ\_ESD}$	6		kV
ESD protection at pin VDDH	IEC 61000-4-2 R=330 $\Omega$ , C=150pF	$V_{VDDH\_ESD}$	6		kV
ESD protection at all other pins	AEC-Q100-002 R=1.5k $\Omega$ , C=100pF chip level test	$V_{pin\_ESD\_HBM}$	2		kV

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## 2 Recommended Operating Conditions

Parameters are guaranteed within the range of recommended operating conditions unless otherwise specified.

All voltages are referred to ground (0V).

Currents flowing into the circuit have positive values.

The first electrical potential connected to the IC must be GND.

Description	Condition	Symbol	Min	Typ	Max	Unit
Supply voltage at pin VDDH	SIO Mode	$V_{VDDH}$	8	24	32	V
Supply voltage at pin VDDH for IOLINK communication	IO_Link Mode	$V_{VDDH}$	18	24	32	V
Supply voltage at pin VDD		$V_{VDD}$	3.15	3.3	3.45	V
Operating ambient temperature range		$T_{OP}$	-40		+105	°C

## 3 Thermal Characteristics

Description	Condition	Symbol	Min	Typ	Max	Unit
Thermal resistance junction to case	QFN44L7 <sup>1)</sup>	$R_{TH\_JC\_7\_ABS}$		5		K/W
Thermal resistance junction to ambient, high conductivity	QFN44L7 <sup>1)</sup>	$R_{TH\_JAH\_7\_ABS}$		25		K/W

1) Values are based on multilayer PCB according to JEDEC JESD-51-5.

## 4 Electrical Characteristics

( $V_{VDDH} = +8V$  to  $+32V$  for SIO mode,  $V_{VDD} = 3.15V$  to  $3.45V$ ,  $T_{AMB} = -40^{\circ}C$  to  $+105^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{VDDH} = +24V$ ,  $V_{VDD} = +3.3V$  and  $T_{AMB} = +25^{\circ}C$ . Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
<b>Power Supplies</b>						
Supply voltage at pin VDDH for SIO mode	SIO mode	$V_{supSIO}$	8	24	32	V
Supply voltage at pin VDDH for IOLINK communication		$V_{supIOLINK}$	18	24	32	V
Supply voltage at pin VDD		$V_{DD}$	3.15	3.3	3.45	V
Supply current at pin VDDH		$I_{DDH}$		1.0	2.0	mA
Supply current at pin VDD		$I_{DD}$		3.5	5.5	mA
<b>Supply Monitors</b>						
Under voltage threshold VDDH, L1, L2 to switch-off the transmitters or the external P-FETs		$UV_{OFF}$	6.5	7	7.5	V
Under voltage monitor threshold at L1 and L2		$UV_{IOLINK}$	16	17	18	V
Debounce time for under voltage detection at VDDH, L1 and L2		$t_{deb\_UV}$	50		250	$\mu s$
VDD undervoltage threshold		$V_{DDUV}$	2.7		3	V
Hysteresis of VDDUV threshold		$V_{DDUVhyst}$		0.1		V

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## Electrical Characteristics (continued)

( $V_{VDDH} = +8V$  to  $+32V$  for SIO mode,  $V_{VDD} = 3.15V$  to  $3.45V$ ,  $T_{AMB} = -40^{\circ}C$  to  $+105^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{VDDH} = +24V$ ,  $V_{VDD} = +3.3V$  and  $T_{AMB} = +25^{\circ}C$ . Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Debounce time for VDDUV		$t_{deb\_VDDUV}$	50		250	$\mu s$
Hysteresis of VDDPOR signal		$V_{DDPORhyst}$		0.1		V
VDDPOR threshold		$V_{DDPOR}$	2.2		2.7	V
voltage difference between VDDUV threshold and POR		$\Delta(V_{DDUV} - V_{DDPOR})$		0.3		V
<b>IO-Link Transmitter</b>						
Driver ON resistance	$V(Lx) > 14V$ tested at $ I_{out}  = 200mA$	$R_{ON}$		1	2	$\Omega$
Driver ON resistance at low supply voltage	$8V < V(Lx) < 14V$ tested at $ I_{out}  = 200mA$	$R_{ON\_low\_supply}$		2	3	$\Omega$
Over current limitation threshold for CQ_OUT=Low		$I_{LIM\_L}$	550	750	1200	mA
Over current limitation threshold for CQ_OUT=High		$I_{LIM\_H}$	-1200	-750	-550	mA
first (default) configurable over current limitation threshold for CQ_OUT=Low		$I_{THL\_OFF\_CONF1}$	300	500	800	mA
second configurable over current limitation threshold for CQ_OUT=Low		$I_{THL\_OFF\_CONF2}$	150	250	425	mA
third configurable over current limitation threshold for CQ_OUT=Low		$I_{THL\_OFF\_CONF3}$	75	150	250	mA
fourth configurable over current limitation threshold for CQ_OUT=Low		$I_{THL\_OFF\_CONF4}$	50	100	175	mA
first (default) configurable over current limitation threshold for CQ_OUT= High		$I_{THH\_OFF\_CONF1}$	-800	-500	-300	mA
second configurable over current limitation threshold for CQ_OUT=High		$I_{THH\_OFF\_CONF2}$	-425	-250	-150	mA
third configurable over current limitation threshold for CQ_OUT=High		$I_{THH\_OFF\_CONF3}$	-250	-150	-75	mA
fourth configurable over current limitation threshold for CQ_OUT=High		$I_{THH\_OFF\_CONF4}$	-175	-100	-50	mA
Output voltage rise time in fast mode (bit FAST="1" in CH_CFG)	$C_{load} = 1-5nF$ , $R_{load} = 20k\Omega$ to GND, C/Q H/L transition, 10% - 90%	$t_{r\text{speed}}$	100		896	ns
Output voltage rise time in slow mode (bit FAST="0" in CH_CFG)	$C_{load} = 1-5nF$ , $R_{load} = 20k\Omega$ to GND, C/Q H/L transition, 10% - 90%	$t_{rl\text{speed}}$	0.8		5.2	$\mu s$

## Electrical Characteristics (continued)

( $V_{VDDH} = +8V$  to  $+32V$  for SIO mode,  $V_{VDD} = 3.15V$  to  $3.45V$ ,  $T_{AMB} = -40^{\circ}C$  to  $+105^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{VDDH} = +24V$ ,  $V_{VDD} = +3.3V$  and  $T_{AMB} = +25^{\circ}C$ . Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Output voltage fall time in fast mode (bit FAST="1" in CH_CFG)	$C_{load} = 1-5nF$ , $R_{load} = 20k\Omega$ to GND, C/Q L/H transition, 10% - 90%	$t_{fhspeed}$	100		896	ns
Output voltage fall time in slow mode (bit FAST="0" in CH_CFG)	$C_{load} = 1-5nF$ , $R_{load} = 20k\Omega$ to GND, C/Q L/H transition, 10% - 90%	$t_{flspeed}$	0.8		5.2	$\mu s$
Transmit propagation delay from TXD to CQ_OUT	$V(Lx) = 24V$ bit FAST="0"	$t_{pd\_lspeed}$		2.5 <sup>1)</sup>		$\mu s$
Transmit propagation delay from TXD to CQ_OUT	$V(Lx) = 24V$ bit FAST="1"	$t_{pd\_hspeed}$		1.2 <sup>1)</sup>		$\mu s$
Duty Cycle 1 <sup>3)</sup>	$V_{THHS}_{IOLINK} (max)$ , $V_{THLS} (max)$ <sup>2)</sup>	$D_{min,1}$	0.386			
Duty Cycle 2 <sup>3)</sup>	$V_{THHS}_{IOLINK} (min)$ , $V_{THLS} (min)$ <sup>2)</sup>	$D_{max,2}$			0.591	
Wake-up pulse duration	Wake-up request	$t_{WU}$	75	80	85	$\mu s$
OFF time after wake-up pulse	Wake-up procedure	$t_{dOFF\_WU}$		350	400	$\mu s$
ON time with overload		$t_{dON\_OL}$	85	100	115	$\mu s$
First OFF time after first ON or wake-up pulse		$t_{dOFF1\_OL}$		200 $*t_{dON\_OL}$		$\mu s$
OFF time after overload detection, default value	TDOFF1,2= „00“	$t_{dOFF2\_OL\_CONF1}$		200 $*t_{dON\_OL}$		$\mu s$
OFF time after overload detection, configured	TDOFF1,2= „01“	$t_{dOFF2\_OL\_CONF2}$		120 $*t_{dON\_OL}$		$\mu s$
OFF time after overload detection, configured	TDOFF1,2= „10“	$t_{dOFF2\_OL\_CONF3}$		64 $*t_{dON\_OL}$		$\mu s$
OFF time after overload detection, configured	TDOFF1,2= „11“	$t_{dOFF2\_OL\_CONF4}$		320 $*t_{dON\_OL}$		$\mu s$
Debounce time for over current detection		$t_{debOL}$		15		$\mu s$
<b>IO-Link Receiver</b>						
Input threshold high for IEC61131-2 type 2	$18V < V_{Lx} < 30V$	$V_{THHSIEC2}$	9	10	11	V
Input threshold high for IOLINK and IEC61131-2 type 1	$18V < V_{Lx} < 30V$	$V_{THHSIOLINK}$	11	12	13	V
Input threshold low	$18V < V_{Lx} < 30V$	$V_{THLS}$	8	9	10	V
Input threshold hysteresis for IEC61131-2 type 2	$18V < V_{Lx} < 30V$	$V_{HYSIEC2}$	0.5	1	1.5	V
Input threshold hysteresis for IOLINK and IEC61131-2 type 1	$18V < V_{Lx} < 30V$	$V_{HYS\_IOLINK}$	2	3	4	V
Receiver input debounce filter time	$t_{BIT}$ depends on BD1/ BD0	$t_{CQ\_deb}$		$1/9 * t_{BIT}$		ns

1) not production tested

2) tested at  $C_{Load} = 1-5nF$ ;  $R_{Load,min} = 20k\Omega$  to GND;  $V(Lx) / R_{Load,max} = 15 mA$

3)  $D = t_{CQH} / 2 * T_{Bit}$

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## Electrical Characteristics (continued)

( $V_{VDDH} = +8V$  to  $+32V$  for SIO mode,  $V_{VDD} = 3.15V$  to  $3.45V$ ,  $T_{AMB} = -40^{\circ}C$  to  $+105^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{VDDH} = +24V$ ,  $V_{VDD} = +3.3V$  and  $T_{AMB} = +25^{\circ}C$ . Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Input pull down current 1 for input IEC61131-2 type 2	PD-Source enabled $V_{CO\_INx} > 5V$	$I_{pdown1}$	6	8	12	mA
Input pull down current 2 for input IEC61131-2 type 2	PD-Source enabled $V_{CO\_INx} > 5V$	$I_{pdown2}$	2	4	7	mA
<b>UART</b>						
UART master tolerance		$UART_{TOL}$			0.1	%
UART receiver detects IDLE after $N_{BIT,IDLE}$ * bit times	at least one byte UART reception before	$N_{BIT,IDLE}$		5		
TRX buffer memory size		$n_{MEM}$		127		byte
<b>IO-Link Cycle Timer</b>						
IO-Link Cycle Time	UART of channel enabled	$T_{CYC}$	0.5		348	ms
Granularity of TCYC	depending on PRSC[1:0]	$T_{CYC\_STEP}$	0.5		4	ms
Low pulse @ pin SCSN for synchronization event	no SCK pulse	$t_{IOSYNC}$	10			$\mu s$
<b>Oscillator</b>						
Internal oscillator frequency		$f_{OSC,INT}$	-5%	8	+5%	MHz
Oscillator frequency accuracy with external quartz	external crystal 50ppm	$f_{OSC,QUARTZ}$	-0.01%		+0.01%	MHz
<b>PLL</b>						
Internal synchronization clock	Quartz enabled or XTAL_IN insertion	$f_{sync}$		1.0125		kHz
Synchronization clock frequency applied at pin XTAL_IN	Quartz disabled, XTAL_OUT n.c.	$f_{XTAL,sync}$	-0.02%	$f_{sync}$	+0.02%	
Frequency of CLK_OUT port, $C_{sync}$	Output enabled, Quartz enabled	$f_{CLK\_OUT}$	-0.02%	1.0125	+0.02%	kHz
<b>Temperature Monitor</b>						
Shut off over temperature threshold		$T_{OT}$	150			deg. C
Electrical hysteresis of over-temperature shut-off		$T_{OT,hyst}$		12		deg. C
<b>Host Interface</b>						
High level input voltage		$V_{IH}$	$0.7 * V_{VDD}$			V
Low level input voltage		$V_{IL}$			$0.3 * V_{VDD}$	V
High level output voltage	Iload=2mA	$V_{OH}$	$0.8 * V_{VDD}$			V
Low level output voltage	Iload=-2mA	$V_{OL}$			$0.2 * V_{VDD}$	V
Input pull-down current	Vpin= $V_{VDD}$	$I_{pd}$	10		80	$\mu A$
Input pull-up current	Vpin=0V	$I_{pu}$	-80		-10	$\mu A$
Time between rising edge of SCSN and high impedance at MISO		$t_{MISO\_Z}$			100	ns
MISO data valid time	$C_{MISO} < 20 pF$	$t_{valid}$			35	ns
SCK pulsewidth		$t_{P\_SCK}$	125			ns

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## Electrical Characteristics (continued)

( $V_{VDDH}$  = +8V to +32V for SIO mode,  $V_{VDD}$  = 3.15V to 3.45V,  $T_{AMB}$  = -40°C to +105°C, unless otherwise noted. Typical values are at  $V_{VDDH}$  = +24V,  $V_{VDD}$  = +3.3V and  $T_{AMB}$  = +25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Time between falling SCSN edge and first rising SCK edge		$t_{LS1}$	50		2000	ns
Time between last falling SCK edge and rising SCSN edge		$t_{LS2}$	50			ns
Inter byte gap relevant for two byte access between address and data byte only		$t_{IBG}$	550			ns
MOSI data setup time		$t_{setup}$	30			ns
MOSI data hold time		$t_{hold}$	20			ns
Number of data bytes during burst access to TRX buffers		$N_{SPI,burst}$	1		127	
<b>IO-Link Supply Control</b>						
Shutdown delay 1 including delay of current regulation	PDR_CFG1 [7:6]=00 Power FET dependent	$t_{d\_OFF1}$		1		ms
Shutdown delay 2 including delay of current regulation	PDR_CFG1 [7:6]=01 Power FET dependent	$t_{d\_OFF2}$		4		ms
Shutdown delay 3 including delay of current regulation	PDR_CFG1 [7:6]=10 Power FET dependent	$t_{d\_OFF3}$		10		ms
Shutdown duration 1	PDR_CFG1 [5:4]=00	$t_{OFF1}$		5		ms
Shutdown duration 2	PDR_CFG1 [5:4]=01	$t_{OFF2}$		20		ms
Shutdown duration 3	PDR_CFG1 [5:4]=10	$t_{OFF3}$		50		ms
Over current detection threshold at shunt resistor		$V_{IN\_OCCOMP}$	60	90	120	mV
Voltage drop across shunt in over current limitation state		$V_{IN\_OC}$	70	100	130	mV
Over current debounce time		$t_{deb\_OCCOMP}$		8		μs
Input current at pin SENSE_Lx	$V_{SENSE\_Lx} = V_{VDDH}$	$I_{SENSE}$	6	10	20	μA
Pull up resistance at Pins DR_L1 and DR_L2 in OFF state	$V_{VDDH} - V_{DR\_Lx} < 0.8V$	$R_{PU\_OFFSW}$		300	500	Ω
Output voltage at Pins DR_L1 and DR_L2 to switch external PMOS ON	$I_{DR\_Lx} = 100\mu A$	$V_{GATE\_min}$	$V_{VDDH} - 15$	$V_{VDDH} - 12$	$V_{VDDH} - 5$	V
Output voltage at Pins DR_L1 and DR_L2 to switch external PMOS OFF	$I_{DR\_Lx} = -100\mu A$	$V_{GATE\_max}$	$V_{VDDH} - 0.4$	$V_{VDDH} - 0.1$	$V_{VDDH}$	V
Maximum switch-off current for gate of external PMOS	PMOS active $V_{DR\_L} = V_{VDDH} - 4V$ $V_{shunt} = 300mV$	$I_{max\_OFF}$	-2	-3.8	-7	mA
Switch-on gate current for gate of external PMOS	PMOS active $V_{DR\_L} = V_{VDDH} - 4V$ $V_{shunt} = 55mV$	$I_{min\_NORM}$	0.5	1	3.5	mA
Transient response time OFF->ON	PMOS active $C_{DR\_L} = 0.8nF$	$t_{pd\_ON}$		10		μs
Transient response time ON->OFF	PMOS active $C_{DR\_L} = 0.8nF$	$t_{pd\_OFF}$		10		μs

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## 5 Functional Description

### 5.1 Power Supplies

The device has got four supply input pins:

VDDH – 24V supply

L1, L2 – 24V supply for the transceivers

VDD – 3.3V supply for the digital blocks

VDDH is the general high-voltage supply pin. It supplies an internal low-voltage regulator for safe power up, internal references and the voltage monitors.

Each of the transmitter supply pins L1 and L2 supplies one of the two internal transmitters. This supply can be controlled by external PMOS transis-

tors. The IC provides the gate voltage for these external transistors and a current monitor to be able to limit the maximum current. If no external current limited switches are needed the pins L1 and L2 has to be connected to the VDDH supply.

Pin VDD has to be supplied by an external voltage supply with nominal 3.3V. VDD supplies the host interface, the logic block and various other internal blocks. The logic block is set to its initial ("reset") state by a power-on-reset signal, delivered by the VDD monitor.

### 5.2 Supply Monitor

The supply monitor provides status information of the supply voltages VDD, VDDH, L1 and L2 in SPI register VMON STAT. For each flag an interrupt enable bit (IE)

can be configured in register VMON IE.

Read access to register VMON STAT will clear the interrupts.

### 5.3 VDDH, L1, L2 Monitor

If the supply voltage at L1 or L2 falls below the  $UV_{IOLINK}$  threshold this condition is set in the corresponding SPI register only and an interrupt is generated if configured. The transmitters keep active.

If the supply voltage at L1 or L2 falls below the  $UV_{OFF}$  threshold the transmitters are disabled.

If the VDDH supply voltage falls below the  $UV_{OFF}$  threshold the external PMOS-FETs are switched-off.

### 5.4 VDD Monitor

If the VDD supply voltage falls below the  $V_{DDUV}$  threshold a bit in the register VMON STAT is set. If VDD falls below  $V_{DDPOR}$  threshold a power-on-reset is generated.

### 5.5 Status and Control Registers

Table 1. Voltage Monitoring Register

Register Name	Address	Description
VMON STAT		CAN-ID [7:0]
VMON IE		CAN-ID [10:8] and CAN-IDE

Table 2. VMON STAT

VMON STAT (0x02)	MSB							LSB
Content	-	-	-	-	L2UV	L1UV	VDDHUV	VDDUV
Reset Value	0	0	0	0	1	1	1	1
Access	R	R	R	R	R	R	R	R
Bit Description	L2UV : 1 = Under voltage at L2 L1UV : 1 = Under voltage at L1 VDDHUV : 1 = Under voltage at VDDH VDDUV : 1 = Under voltage at VDD							

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Table 3. VMON IE

VMON IE (0x03)	MSB							LSB
Content	-	-	-	-	L2IE	L1IE	VDDHIE	VDDIE
Reset Value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W
Bit Description	L2IE : 1 = Interrupt enable L2 L1IE : 1 = Interrupt enable L1 VDDHIE : 1 = Interrupt enable VDDH VDDIE : 1 = Interrupt enable VDD							

### 5.6 IO-Link-Transceiver

The device contains two channels with a high-voltage digital transmitter (output: CQ\_OUTx) and receiver (input: CQ\_INx). The transmitter and receiver are accessible by both – a parallel interface (TXD, TXEN, RXD) and by SPI in IO-Link or SIO mode. The digital pins are supplied by VDD voltage. The input thresholds and output levels are referenced to this voltage.

It can be used in the following ways:

- a) CQ\_OUTx is used as standard output (SIO) to drive ohmic loads, inductive loads or bulb lamps
- b) CQ\_INx is used as standard digital input type 2 according to IEC 61131-2
- c) CQ\_OUTx and CQ\_INx are used together as IO-LINK port for data transfer rates of 4.8 kBaud, 38.4 kBaud or 230.4 kBaud.

### 5.7 IO-Link-Transmitter

The push-pull transmitter is activated with high level on pin TXEN and drives the CQ\_OUT pin Low or High in accordance to the inverted logic level on pin TXD. A slope control limits EMC emission.

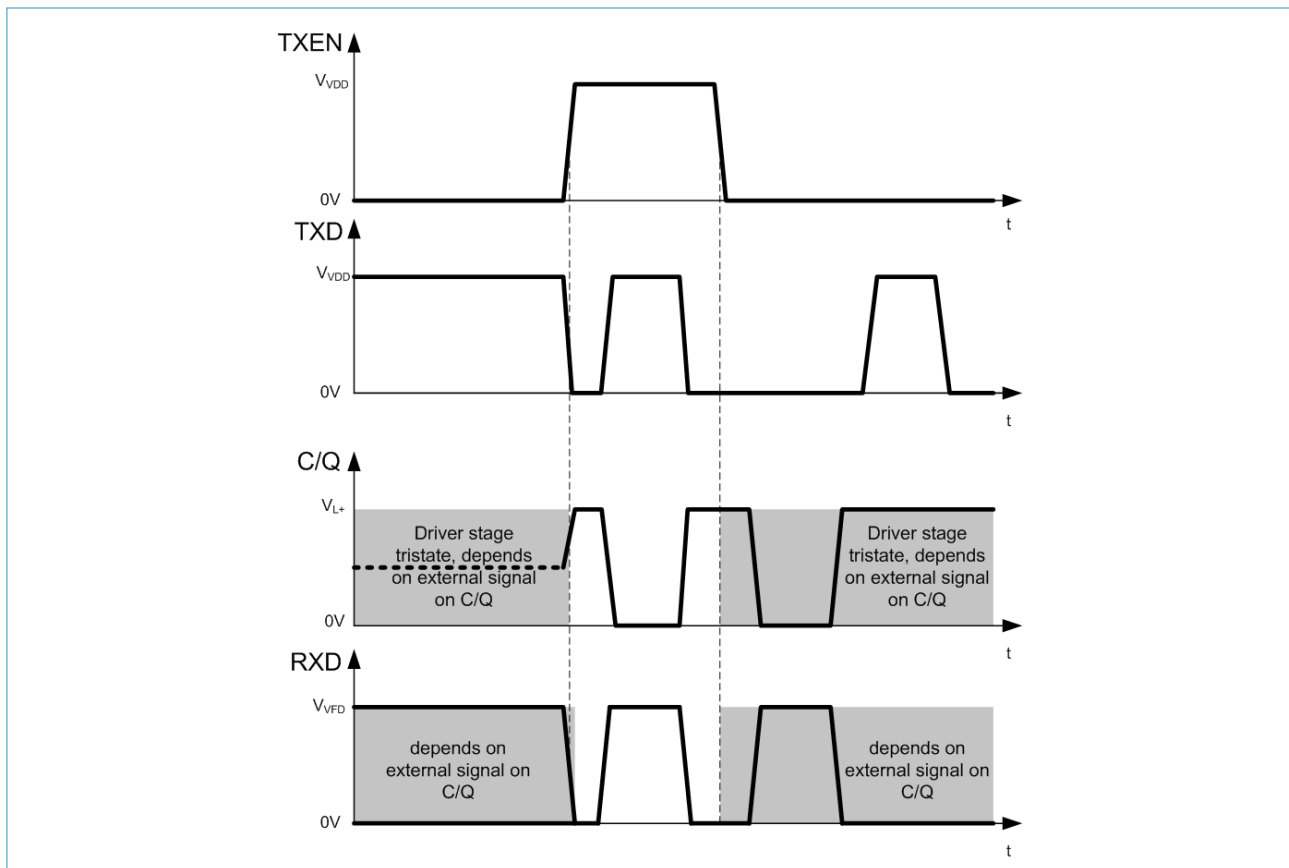


Figure 1. Transmitter polarity

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The transition times can be set for two different slope modes using register CH CFG. The transmitter is operable only if VDD, L+ and chip temperature are within their specified limits. Otherwise the transmitter is disabled.

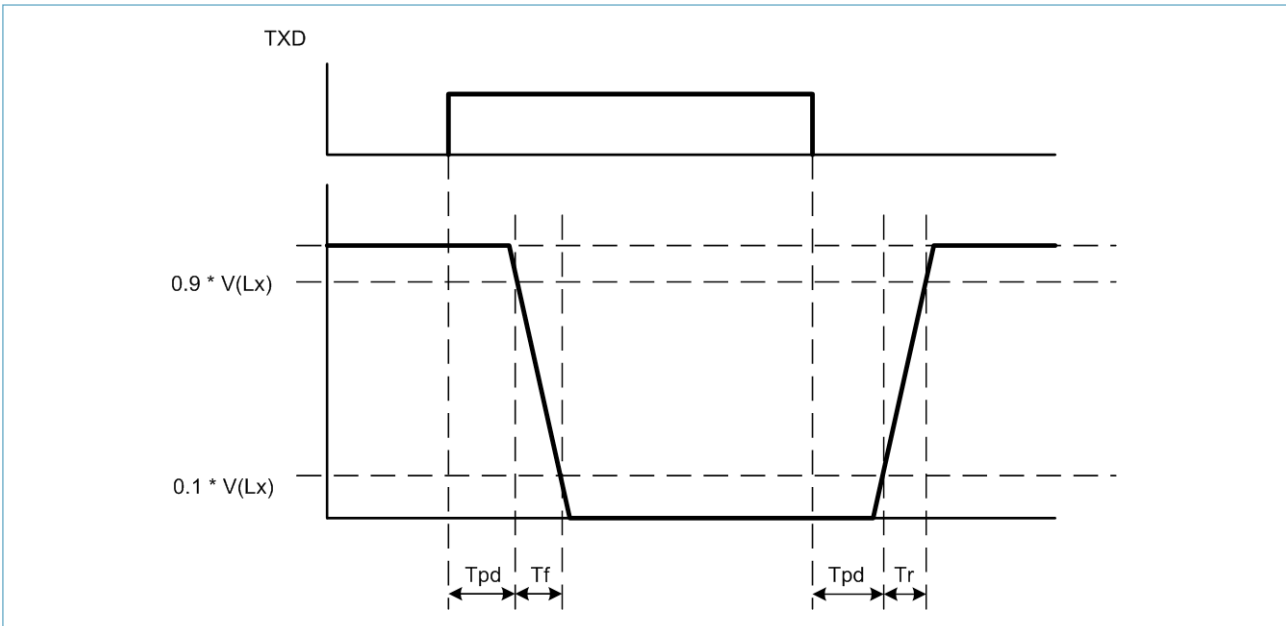


Figure 2. Transmitter characteristics

### 5.8 Transmitter Overload

In case of high power dissipation (e.g. due to short circuit of the driver) the chip temperature will increase. To protect the device, an internal over temperature sensor for each driver is implemented. In case of over temperature, the affected driver is disabled. The other output

driver can operate independently.

The transmitters are switched on after the over temperature condition disappeared. The over temperature flag is set in CH STAT, to generate an interrupt use bit OTIE in TRX CFG

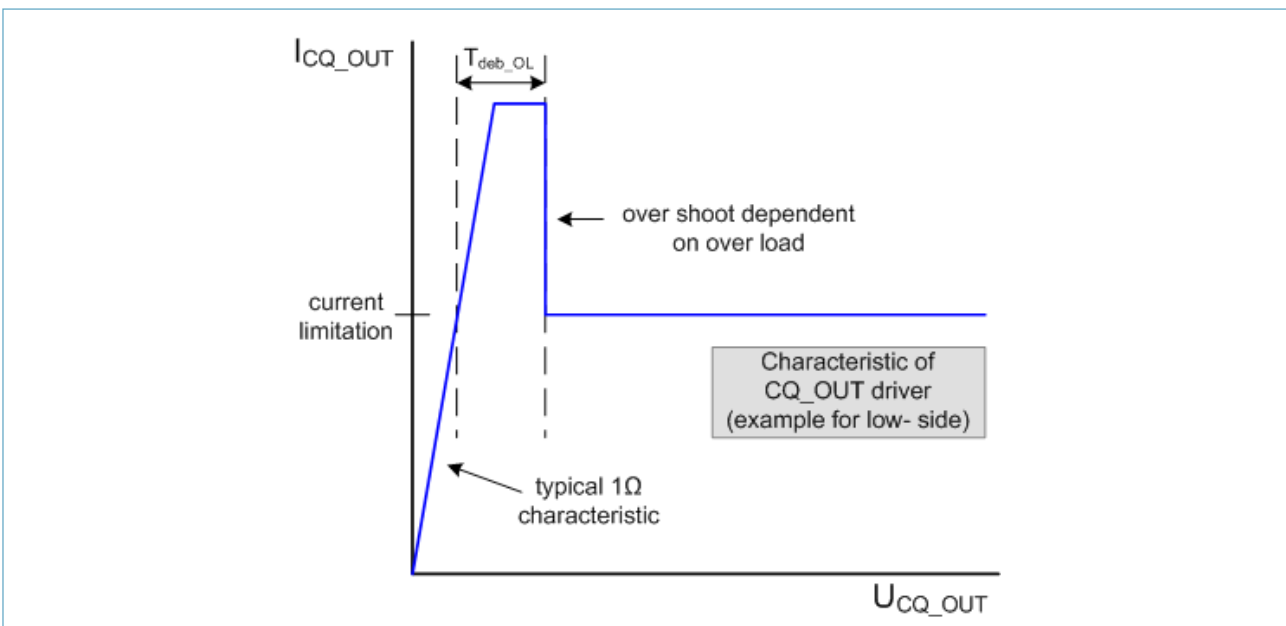


Figure 3. Transmitter characteristics at overload

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In case of an over current is detected directly after the transmitter is activated by setting the pin TXEN to high (or Bit STXEN=1), the output current is limited to an over current threshold  $I_{LIM\_x}$ . The transmitter remains active for  $T_{dON\_OL}$ . After this time the transmitter is disabled for  $T_{dOFF1\_OL}$ . After this first sequence a cyclic

overcurrent shutdown with a configurable current limitation ( $I_{TH\_OFF\_CONFx}$ ) and dutycycle ( $T_{dON\_OL} / T_{dOFF2\_OL\_CONFx}$ ) is implemented (see Fig. 4).

The configured dutycycle must not exceed the power dissipation limits of the device.

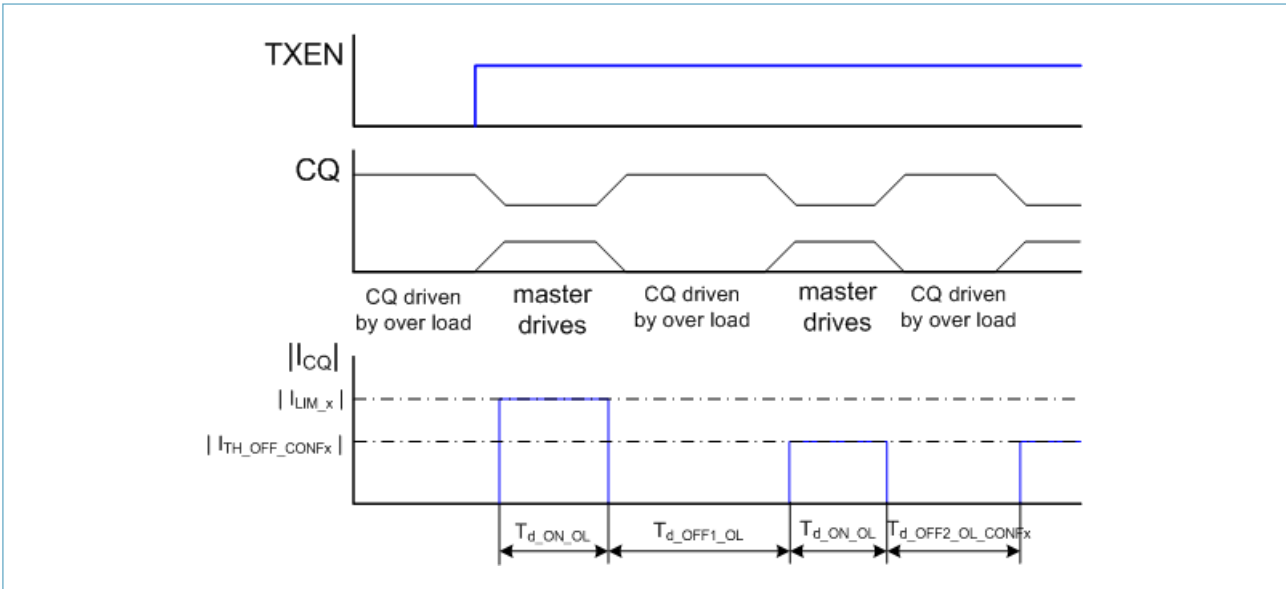


Figure 4. Transmitter over load sequence

If an overload occurs while the transmitter was already active, it will turn off immediately after a debounce time  $T_{deb\_OL}$  for  $T_{d\_Off2\_OL}$ , followed by the sequence described above using off times  $T_{d\_Off2\_OL\_confx}$  (see Fig. 5).

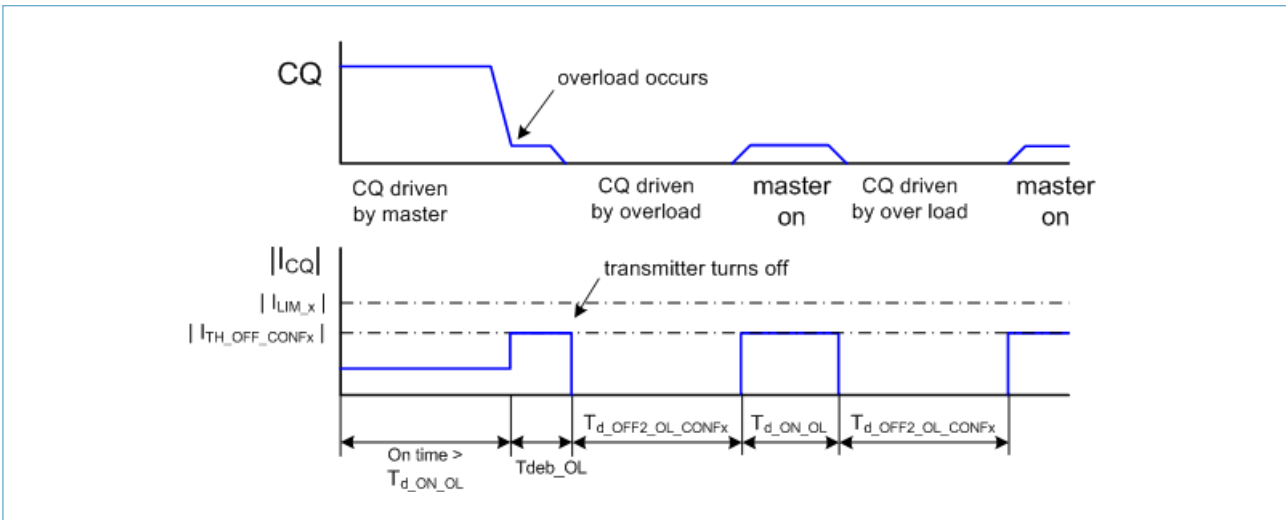


Figure 5. Over load while driver was already active

### 5.9 Transmitter Loads

In SIO mode the external load at CQ\_OUT may have resistive, capacitive or inductive characteristic or can be a bulb lamp. The loads can be connected between CQ\_OUTx and Lx or between CQ\_OUTx and PGNDx.

It is possible to switch the load in the following ways:

**TXEN = constant High, switching with TXD**

In this case CQ\_OUT is driven as push-pull output.

**TXD = Low:** high-side driver active

**TXD = High:** low-side driver active

In case of inductive loads the complementary driver acts as free-wheeling element.

**TXD constant, switching with TXEN**

In this case the high-side driver (if TXD = Low) or the low-side driver (if TXD = High) is used, so the load is switched either between "Active Low" and "Tristate" or between "Active High" and "Tristate".

In case of inductive loads inherent diodes of the drivers act as free-wheeling elements.

### 5.10 IO-LINK Receiver

The receiver converts the voltage level at the CQ\_IN pin to an inverted logic receive signal which is available at pin RXD and the internal UART. The receiver filter times depends on the configured baudrate. The receiver functionality is available in the specified IO-Link supply range.

The receiver can be configured by bit IEC-2 in [TRX\\_CFG](#)

either as standard IO-LINK / IEC61131-2 input or as standard IEC61131-1 input.

The input current source can be activated by bit PDEN in register [TRX\\_CFG](#). Setting bit PDAUTO the current source is disabled while the driver stage is active during SIO mode or communication mode (TXEN=1) in order to reduce power dissipation.

### 5.11 SIO-Mode

Each C/Q channel can be used as an input or output, while the output can be configured to switch between high side, low side and HiZ.

SIO mode can be used by pins TXEN, TXD, RXD or by SPI

control. The mode can be configured by register CH\_CFG. If bit SIO is set to „1“ the output control is done by SPI access to register TRX\_CFG bits STXD and STXEN. The receiver status can be read by register CH\_STAT bit RXD.

### 5.12 Transceiver UART

The IO-Link Master IC has two integrated UART interfaces. The UART provides the media access and bit decoding / encoding and byte framing capabilities as well. UART timing accuracy of 0.1% depends on the oscillator configuration described in chapter „Oscillator“.

UART mode is activated by SPI register CH\_CFG bit UART. For UART mode the bit „SIO“ has to be „0“. The

UART baudrate has to be configured in register CH\_CFG independently for each channel.

The UART byte frame consists of:

- one start bit (value "0")
- eight data bits (LSB first)
- an even parity bit and
- one stop bit (value "1").

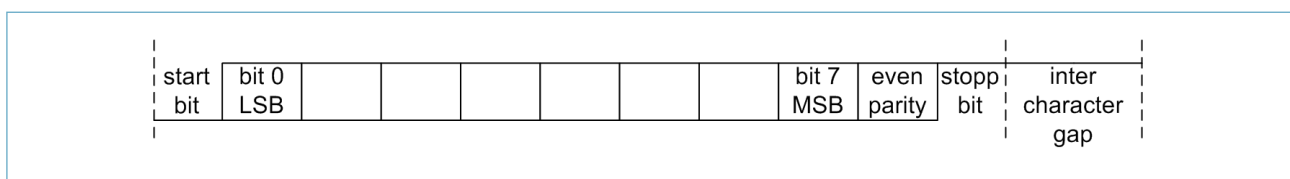


Figure 6. Uart byte frame

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Transmission and receive is controlled by the integrated IO-Link cycle timer. For UART communication the internal cycle timer must be configured and enabled (see chapter „IO-Link cycle timer“). Each received byte is checked for correct parity and right framing (stop bit). In case of receive errors the corresponding error flags are set in register RX\_STAT and [TIM\\_STAT](#).

The E981.12 provides a 127 byte shared TRX buffer to store transmit and receive frames. The number of bytes to be transmitted and received must be configured in register UART\_TXNUM and UART\_RXNUM. As soon as the configured number of bytes was successfully send and the response was received bit RDY in register TIM\_STAT is set. Optionally an interrupt can be enabled by RDYIE in register TIM\_IE.

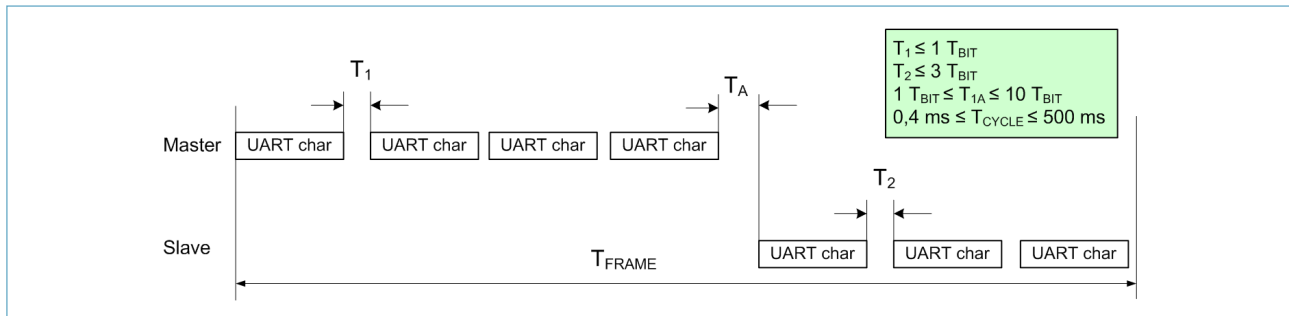


Figure 7. IO-Link frame and cycle timing

If no further UART characters are observed for longer than  $T_2$ , IDLE is detected. If the number of received characters differs from the value in UART\_RXNUM (as well as no reception at all was observed), the error flag

NUME will be set in register TIM\_STAT. Optionally an interrupt can be enabled by NUMIE in register TIM IE. The interrupt is cleared by read access to TIM\_STAT.

### 5.13 Host - PHY Communication

The timing diagram in Fig. 8 shows the communication between host microcontroller and IO-Link Master TRX buffer within one cycle when using the internal UARTs.

Before writing or reading the corresponding buffer the UART has to be enabled.

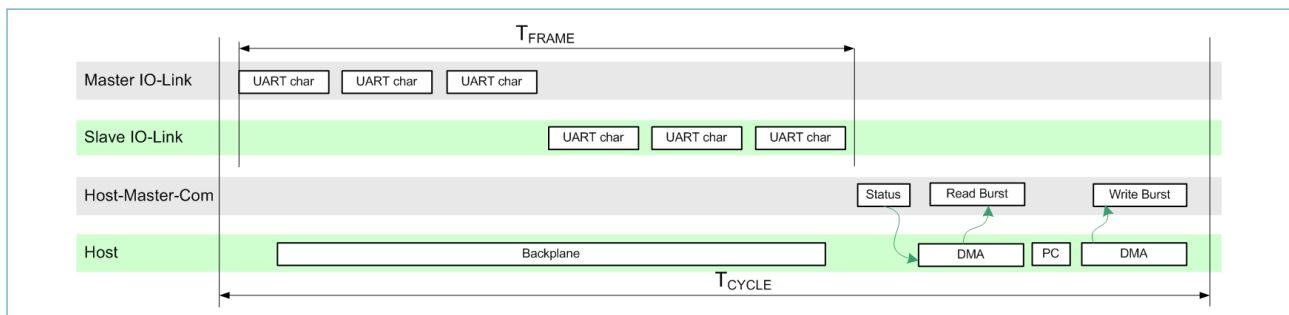


Figure 8. Host-PHY communication

After reading the response frame of the current cycle the host has to write the master frame for the next cycle to be transmitted before the current cycle has been ended. The buffered IO-Link master frame is sent by E981.12 starting with the next communication cycle (see chapter „IO-Link cycle timer“). The host microcontroller has to ensure to fill the TRX buffer with the master frame before the next cycle starts. If the TRX buffer access is not finished till the next cycle start (cy-

cle boundary violation), the transmission is started delayed. The TX bytes written to the TRX buffer by SPI are checked by XOR checksum. If the checksum fails the E981.12 does not transmit data in the next cycle. The TRX buffer access is implemented as SPI burst access to reduce the SPI communication overhead (see Chapter [5.23 SPI Interface](#)).

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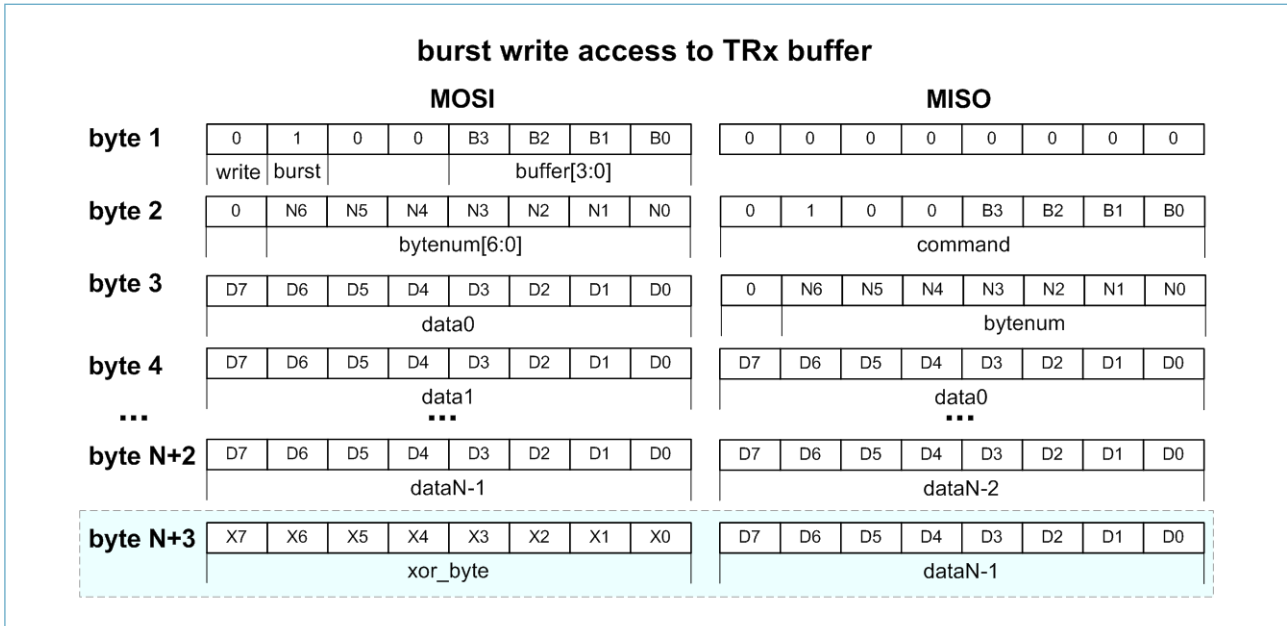


Figure 9. UART buffer burst write access

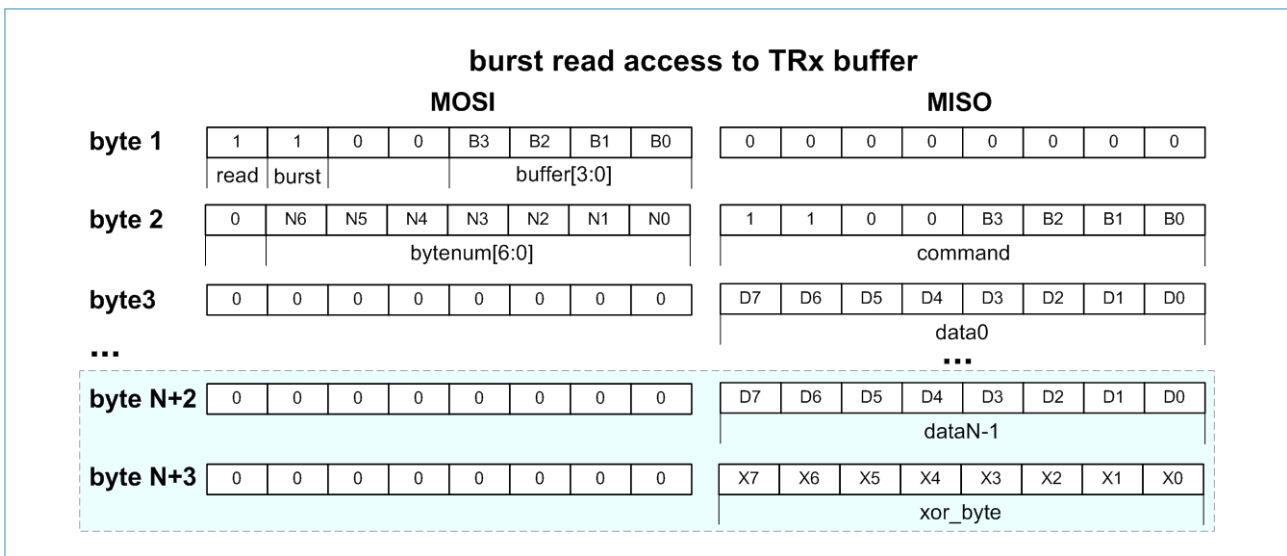


Figure 10. UART buffer burst read access

The buffer is selected by bits [B3:B0]. Channel 1 is selected by 0x5 (0101b). The buffer for channel 2 is selected by 0xA (1010b).

This buffer selection code must not be interpreted as starting address. The buffer read or write access always starts with data byte 0. It is not needed to read or write

all 127 bytes. The application has to ensure that the buffer content matches to the number of bytes to be transmitted in register UART\_TXNUM.

For further information about SPI access see chapter [5.23 SPI Interface](#).



### 5.14 Channel Status and Configuration Registers

Table 4. Transceiver Register

Register Name	Address	Description
<b>Channel 1</b>		
CH CFG	0x10	Channel 1 configuration
CH STAT	0x11	Channel 1 status and error register
TRX CFG	0x12	Transceiver config channel 1
TX OCCFG	0x13	Transmitter over current configuration register channel 1
UART TXNUM	0x14	Number of Bytes for TX channel 1
UART RXNUM	0x15	Number of Bytes for RX channel 1
RX STAT	0x1A	Receiver status and error register channel 1
<b>Channel 2</b>		
CH CFG	0x20	Channel 2 configuration
CH STAT	0x21	Channel 2 status and error register
TRX CFG	0x22	Transceiver config channel 2
TX OCCFG	0x23	Transmitter over current configuration register channel 2
UART TXNUM	0x24	Number of Bytes for TX channel 2
UART RXNUM	0x25	Number of Bytes for RX channel 2
RX STAT	0x2A	Receiver status and error register channel 2

Table 5. Channel configuration

[back to Table 4. Transceiver Register](#)

CH CFG Channel 1 (0x10) Channel 2 (0x20)	MSB							LSB
Content	-	FAST	BD1	BD0	-	-	SIO	UART
Reset Value	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R/W	R/W
Bit Description	<b>FAST :</b> Transmitter slope control 1 = fast slopes <b>BD1 / BD0 :</b> Baud rate selection and receiver filter configuration 00 = 4.8 kBaud 01 = 38.4 kBaud 10 = 230.4 kBaud 11 = analog mode (TXEN, TXD, RXD is used for communication) <b>SIO :</b> 1 = SIO Mode with register values 0 = SIO with TXEN, TXD, RXD <b>UART :</b> 1 = internal UART is used if bit „SIO“ is not set to „1“ (SIO has priority) 0 = UART disabled (TXEN, TXD, RXD is used for communication)							

Table 6. Channel status and error register

[back to Table 4. Transceiver Register](#)

CH STAT Channel 1 (0x11) Channel 2 (0x21)	MSB							LSB
Content	-	-	-	-	TXOC	TXOT	-	RXD
Reset Value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	<b>TXOC :</b> 1 = Transmitter Overcurrent detected, cleared by read access <b>TXOT :</b> 1 = Transmitter Over temp. detected, cleared by read access <b>RXD :</b> 1 = Current value of filtered receiver status							

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Table 7. Transceiver config

back to [Table 4. Transceiver Register](#)

TRX CFG Channel 1 (0x12) Channel 2 (0x22)	MSB							LSB
Content	IEC-2	IPD	PDAUTO	PDEN	OCIE	OTIE	STXD	STXEN
Reset Value	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	RR/W	R/W	R/W	R/W	RR/W
Bit Description	<p><b>IEC-2 :</b> 1 = Receiver threshold for input IEC61131-2 type 2 0 = Receiver threshold for IO-Link communication</p> <p><b>IPD :</b> 1 = Receiver channel 1 pull down current 1 Ipdwn1 0 = Receiver channel 1 pull down current 2 Ipdwn2</p> <p><b>PDAUTO :</b> 1 = automatic control of Receiver pull down source 0 = Receiver channel 1 pull down controlled by PDEN</p> <p><b>PDEN :</b> 1 = Receiver channel 1 pull down enabled 0 = Receiver channel 1 pull down disabled</p> <p><b>OCIE :</b> 1 = Over Current IRQ enable</p> <p><b>OTIE :</b> 1 = Over Temp IRQ enable</p> <p><b>STXD :</b> 1 = LS active (in SIO mode only) 0 = HS active (in SIO mode only)</p> <p><b>STXEN :</b> 1 = Transmitter enabled (in SIO mode only)</p>							

Table 8. Transmitter over current configuration register

back to [Table 4. Transceiver Register](#)

TX OCCFG Channel 1 (0x13) Channel 2 (0x23)	MSB							LSB
Content	-	-	TDOFF1	TDOFF0	-	DISOCTH	OCTHR1	OCTHR0
Reset Value	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R	R/W	R/W	R/W
Bit Description	<p><b>TDOFF1 / TDOFF0 :</b> configuration for TdOFF2_OL_CONFx</p> <p>00 = T<sub>dOFF2_OL_CONF1</sub></p> <p>01 = T<sub>dOFF2_OL_CONF2</sub></p> <p>10 = T<sub>dOFF2_OL_CONF3</sub></p> <p>11 = T<sub>dOFF2_OL_CONF4</sub></p> <p><b>DISOCTH :</b> 1 = Disable over current threshold configuration with OCTHR[1:0], threshold ILIM_H/L valid</p> <p><b>OCTHR1/OCTHR0:</b> configuration of Over current threshold ITHx_OFF_CONFx</p> <p>00 = I<sub>THx_OFF_CONF1</sub></p> <p>01 = I<sub>THx_OFF_CONF2</sub></p> <p>10 = I<sub>THx_OFF_CONF3</sub></p> <p>11 = I<sub>THx_OFF_CONF4</sub></p>							

Table 9. Number of Bytes for TX

back to [Table 4. Transceiver Register](#)

UART TXNUM Channel 1 (0x14) Channel 2 (0x24)	MSB							LSB
Content	-	NUM6	NUM5	NUM4	NUM3	NUM2	NUM1	NUM0
Reset Value	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	<b>NUM6 .. NUM0:</b> Number of Bytes to be transmitted							

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Table 10. Number of Bytes for RX

back to [Table 4. Transceiver Register](#)

UART RXNUM Channel 1 (0x15) Channel 2 (0x25)	MSB							LSB
Content	-	NUM6	NUM5	NUM4	NUM3	NUM2	NUM1	NUM0
Reset Value	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	<b>NUM6 .. NUM0:</b> Number of Bytes to be received							

Table 11. Receiver status and error register

back to [Table 4. Transceiver Register](#)

RX STAT Channel 1 (0x1A) Channel 2 (0x2A)	MSB							LSB
Content	-	-	-	-	-	-	FE	PE
Reset Value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	<b>FE :</b> 1 = Framing error (no stop bit), cleared by read access <b>PE :</b> 1 = Parity error, cleared by read access							

### 5.15 IO-Link Cycle Timer

The IO-Link cycle timer generates the communication cycle. It can be configured in range of 0.4 ms up to 132.8 ms in register TIM\_PER. The cycle time is configured by selecting one range out of three as shown in Table 12.

Table 12. IO-Link cycle time

PRSC[1:0]	T <sub>CYC_STEP</sub>	T <sub>CYC_OFFSET</sub>	T <sub>CYC</sub>
00b	0.1 ms	N.A.	0.4 ... 6.3 ms
01b	0.4 ms	6.4 ms Offset included	6.4 ... 31.6 ms
10b	1.6 ms	32 ms Offset included	32 ... 132.8 ms
11b	not used		

$$T_{CYC} = T_{CYC\_OFFSET} + T_{CYC\_STEP} \cdot TIM\_PER[5:0]$$

### 5.16 Cycle Synchronisation

In applications with several channels the device has implemented a cycle synchronization capability.

To enable the cycle synchronization feature set bit SYNC in register TIM\_CFG to „1“.

Because of independent internal oscillator of several devices in multi port applications the synchronization

has to be repeated after certain period of time. This period of time depends on oscillator accuracy and application needs. The cycle timer can be configured to run for a number of cycles determined by bits CNUM[2:0] in register TIM\_CFG (for details see Table below).

Table 13. Number of cycles without resynchronization in SYNC mode

CNUM[2:0]	Number of free running cycles
000b	0.1 ms
001b	0.4 ms
010b	1.6 ms
011b	not used
100b	
101b	
110b	
111b	

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If this number of cycles is reached, the bit WAIT4S in register TIM STAT is set and the cycle timer waits for a resynchronization event from the host controller. Optionally an interrupt can be activated by bit SYNCIE in register TIM IE to indicate that the device is waiting for an resynchronization event (WAIT4S in TIM STAT). This interrupt is set after the number of free running cycles is reached under two conditions:

- the slave response frame is received (number of received characters is equal UART\_RXNUM)
- idle is detected

The interrupt is cleared by reading TIM STAT.

The synchronization event is generated by the host micro controller using pin SCSN. If pin SCSN is driven low for  $T_{IOSYNC}$  and no SCK pulse is detected during this period the IO-Link Master IC will interpret this low pulse as synchronization event and will start the IO-Link cycle timer for the configured number of cycles immediately.

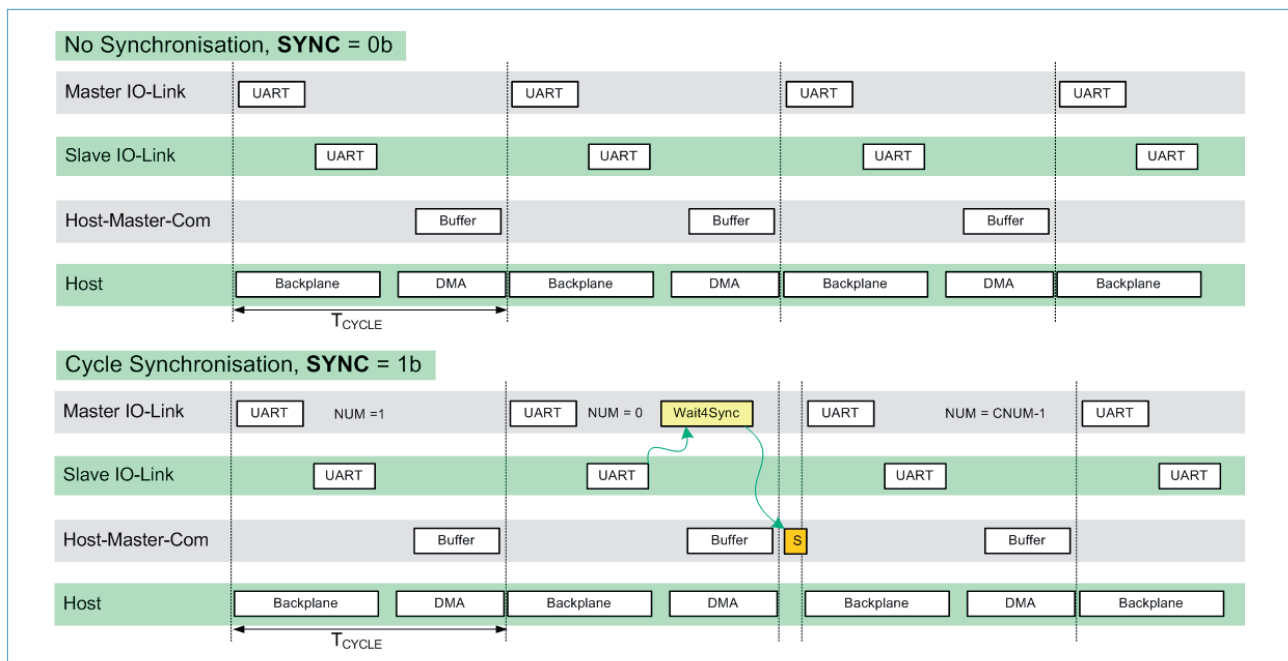


Figure 11. IO-Link cycle timing with and without synchronisation

## 5.17 Configuration and Status Register

Table 14. IO-Link Cycle Timer Register

Register Name	Address	Description
<b>Channel 1</b>		
TIM CFG	0x16	Timer config channel 1
TIM IE	0x17	Timer Interrupt enable register channel 1
TIM STAT	0x18	IO-Link Cycle Timer status register channel 1
TIM PER	0x19	IO-Link Cycle Timer Period and Prescale configuration channel 1
<b>Channel 2</b>		
TIM CFG	0x26	Timer config channel 2
TIM IE	0x27	Timer Interrupt enable register channel 2
TIM STAT	0x28	IO-Link Cycle Timer status register channel 2
TIM PER	0x29	IO-Link Cycle Timer Period and Prescale configuration channel 2

Table 15. Timer config

back to [Table 14. IO-Link Cycle Timer Register](#)

TIM CFG Channel 1 (0x16) Channel 2 (0x26)	MSB							LSB
Content	-	-	-	CNUM2	CNUM1	CNUM0	SYNC	EN
Reset Value	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit Description	<b>CNUM2 / CNUM1 / CNUM0</b> : Number of cycles between synchronisation 000 = 2 cycles 001 = 4 cycles 010 = 6 cycles 011 = 8 cycles 100 = 10 cycles 101 = 12 cycles 110 = 16 cycles 111 = 32 cycles <b>SYNC</b> : 1 = Enable synchronisation <b>EN</b> : 1 = Enable timer							

Table 16. Timer Interrupt enable register

back to [Table 14. IO-Link Cycle Timer Register](#)

TIM IE Channel 1 (0x17) Channel 2 (0x27)	MSB							LSB
Content	NUMIE	RDYIE	SYNCCIE	ACCIE	RXEIE	-	-	-
Reset Value	0	0	0	0	0	0	0	0
Internal Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External Access	R/W	R/W	R/W	R/W	R/W	R	R	R
Bit Description	<b>NUMIE</b> : 1 = Enable RXNUM Error interrupt <b>RDYIE</b> : 1 = Enable RDY interrupt <b>SYNCCIE</b> : 1 = Enable SYNC interrupt <b>ACCIE</b> : 1 = Enable Access Error interrupt <b>RXEIE</b> : 1 = Enable RX Error (FE, PE) interrupt							

Table 17. IO-Link Cycle Timer status register

back to [Table 14. IO-Link Cycle Timer Register](#)

TIM STAT Channel 1 (0x18) Channel 2 (0x28)	MSB							LSB
Content	NUME	RDY	WAIT4S	ACCE	RXE	IDLE	RX	TX
Reset Value	0	0	0	0	0	0	0	0
Internal Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External Access	R	R	R	R	R	R	R	R
Bit Description	<b>NUME</b> : 1 = RX Number Error: Number of RX character is smaller than value in UART_RXNUM or no reception at all in current cycle <b>RDY</b> : 1 = Transmission and Reception completed <b>WAIT4S</b> : 1 = Cycle timer waits for synchronization in SYNC mode <b>ACCE</b> : 1 = Buffer Access Error: micro controller write access to TRX buffer while active transmission or reception <b>RXE</b> : 1 = UART Rx error detected (PE, FE) <b>IDLE</b> : 1 = Cycle timer in idle phase <b>RX</b> : 1 = Cycle timer running, Reception ongoing <b>TX</b> : 1 = Cycle timer running, Transmission ongoing							

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Table 18. IO-Link Cycle Timer Period and Prescale configuration

back to [Table 14. IO-Link Cycle Timer Register](#)

TIM PER Channel 1 (0x19) Channel 2 (0x29)	MSB							LSB
Content	PRSC1	PRSC0	PER5	PER4	PER3	PER2	PER1	PER0
Reset Value	0	0	0	0	0	0	0	0
Internal Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	PRSC1 / PRSC0 : Cycle timer prescaler 00 = 0.4ms .. 6.3ms ( $T_{CYC\_STEP} = 0.1ms$ ) 01 = 6.4ms .. 31.6ms ( $T_{CYC\_STEP} = 0.4ms$ ) 10 = 32.0ms .. 132.8ms ( $T_{CYC\_STEP} = 1.6ms$ ) 11 = reserved PER5 .. PER0 : Timer period configuration in $n \cdot T_{CYC\_STEP}$							

### 5.18 Wake-Up

The wake-up signal can be generated by external microcontroller using the parallel interface (TXEN, TXD, RXD) or integrated wake-up support.

If the wake-up generation support for the port is enabled in *WTIM\_CFG*, the device will generate a signal at CQ\_OUTx depending on the CQ\_INx level. To apply a wake-up, select wake-up support register for channel x. The exact pulse timing is generated internally. For details see chapter 5.19.

The delay between RXDx evaluation and wake-up pulse

is minimized to reduce collisions by level change of external devices (race condition of wake-up signal and fast changes of device SIO-mode signal)

If the IO-LINK master is requested to send a wake-up symbol, the transmitter is turned on for a time  $T_{d\_WU}$  in order to perform a level inversion at pin CQ\_OUTx. A maximum current (limit  $I_{LIM\_L}$  or  $I_{LIM\_H}$ ) will be delivered for time  $T_{d\_WU}$ . The slave is expected to release the C/Q bus during this time. Afterwards the transmitter drives pin CQ\_OUTx to the pre-wake-up pulse level and then turns off for a recovery time of  $T_{d\_off\_WU}$ .

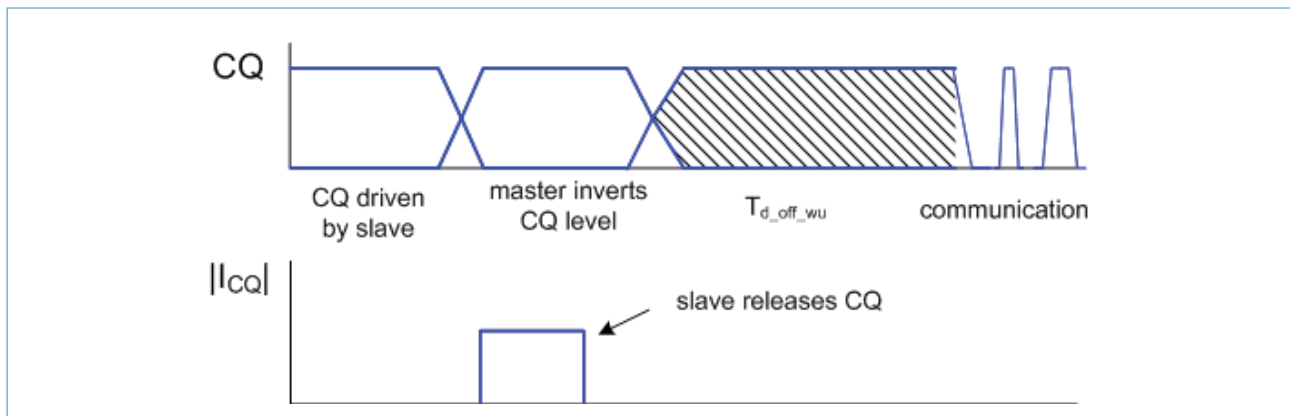


Figure 12. Wake up procedure

The WURQ timer generates the specified IO-Link wake-up request signal for both IO-Link channels selected by bits CH1 / CH2 in register *WTIM\_CFG*.

The wake-up sequence is started immediately after SPI setting bit START in register *WTIM\_CFG*. The host micro

controller can poll WURQ status information or enable a „wake-up completed interrupt“.

After  $T_{d\_off\_wu}$  the transmitter is ready to transmit and responds to requests from either TXENx and TXDx or the UART.

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### 5.19 WURQ Status and Control Registers

Table 19. WURQ Timer Register

Register Name	Address	Description
WTIM_CFG	0x04	WURQ configuration and status register

Table 20. WURQ configuration and status register

WTIM_CFG (0x04)	MSB							LSB
Content	RDY	BUSY	CH2	CH1	RDYIE	-	-	START
Reset Value	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R	R	R	R/W
Bit Description	RDY : 1 = Wake-up sequence completed. cleared by new START or read access to this register BUSY : 1 = Wake-up sequence ongoing CH2 : 1 = Wake-up sequence enabled for channel 2 CH1 : 1 = Wake-up sequence enabled for channel 1 RDYIE : 1 = Interrupt for RDY (wake-up sequence completed) enabled START : 1 = start a wake-up signal at channel (always read as '0')							

### 5.20 Oscillator

The oscillator provides the clock for internal and external digital circuitry. The required oscillator accuracy depends on the application concept. In applications using the parallel communication interface (TXEN, TXD, RXD) the external microcontroller pro-

vides the needed bit time accuracy. In this case the internal oscillator ( $OSC_{RC}$ ) is sufficient for system control and wakeup pulse generation and no external components are needed.

### 5.21 PLL

In applications using the internal UARTs and IO-Link cycle timer the system clock accuracy has to be better than 0.1%. The clock system structure is shown in Fig. 13

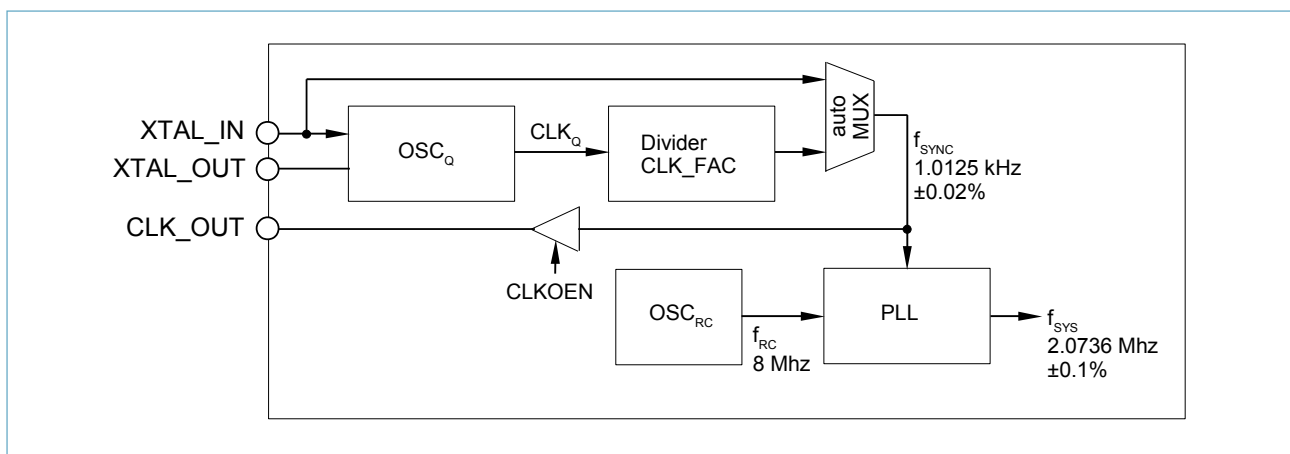


Figure 13. Clock system structure

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Clock accuracy can be reached by applying either an:

- external quartz at XTAL\_IN and XTAL\_OUT. No external capacitors are necessary. To increase the robustness to EMI the input XTAL\_IN shall be connected to GND if the quartz oscillator is not used.
- or an digital clock signal from an external clock source provided by an external microcontroller or by the CLK\_OUT signal of other E981.12 devices used in multi port applications.

This external signal is used to synchronize the internal PLL block.

If  $f_{XTAL\_IN}$  it is exactly  $f_{SYNC} = 1.0125$  kHz the multiplexer automatically switches directly to the XTAL\_IN signal path. In this case there is no need to configure the CLK\_FAC divider.

In case of higher input frequencies  $f_{XTAL\_IN}$  is divided by the CLK\_FAC divider block to get the 1.0125 kHz  $f_{SYNC}$  signal. The internal multiplexer automatically switches to this signal path.

Register CLK\_CTRL configures the XTAL input stage.

- If external clock input at pin XTAL is used Bit ENX has to set to "1"
- If internal quartz oscillator is used Bit ENX and Bit EXTQ has to set to "1"

If the quartz oscillator is not needed it can be disabled to reduce power dissipation.

The CLK\_FAC divider has a reset value of 0x1C71 (7281d). Using other quartz frequencies than 7.3728 MHz the CLK\_FAC value has to be changed to  $CLK\_FAC = f_{Quartz} / C_{sync} - 1$

The CLK\_FAC can be in range of 0x0400 (2048d) up to 0x3FFF (16383d) which allows a wide range of the input frequency. It is recommended to configure the CLK\_FAC registers reset condition of the IO-LINK Master IC.

Bit „LOCK“ in register CLK\_STAT indicates a locked PLL. The PLL has a locking tolerance of approximately 10%. Incorrect CLK\_FAC configuration results in locked PLL but incorrect system communication timing.

Table 21. Clock Register Table

Register Name	Address	Description
CLK_STAT	0x0C	Clock status register
CLK_CTRL	0x0D	Clock system control
CLK_FAC_LO	0x0E	Clock divider register
CLK_FAC_HI	0x0F	Clock divider register

Table 22. Clock system control

CLK_CTRL (0x0D)	MSB							LSB
Content	-	-	-	EXTQ	-	-	CLKOE	ENX
Reset Value	0	0	0	0	0	0	0	0
Internal Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External Access	R	R	R	R/W	R	R	R/W	R/W
Bit Description	<b>EXTQ :</b> 1 = XTAL_IN is used as clock input from extern clock source, XTAL_OUT is disabled (leave open) 0 = a quartz is connected to XTAL_IN and XTAL_OUT <b>CLKOE :</b> 1 = Clock output CLK_OUT enabled 0 = Clock output CLK_OUT disabled <b>ENX :</b> 1 = XTAL input stage enabled 0 = XTAL input stage disabled							

Table 23. Clock divider register low

CLK_FAC_LO (0x0E)	MSB							LSB
Content	FAC7	FAC6	FAC5	FAC4	FAC3	FAC2	FAC1	FAC0
Reset Value	0	1	1	1	0	0	0	1
Internal Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	<b>FAC7 :</b> Clock divider low byte							

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Table 24. Clock divider register high

CLK_FAC_HI (0x0F)	MSB							LSB
Content	-	-	FAC13	FAC12	FAC11	FAC10	FAC9	FAC8
Reset Value	0	0	0	1	1	1	0	0
Internal Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	<b>FAC13</b> : Clock divider high byte							

Table 25. Clock status register

CLK_STAT (0x0C)	MSB							LSB
Content	-	-	-	PLLE	-	-	-	LOCK
Reset Value	0	0	0	0	0	0	0	0
Internal Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External Access	R	R	R	R	R	R	R	R
Bit Description	<b>PLLE</b> : 0 = PLL error, cleared by read access <b>LOCK</b> : 1 = PLL locked							

## 5.22 Clock Distribution

This feature can be used in multi IO-Link channel systems with more than one E981.12 devices.

Using output pin CLK\_OUT the accurate  $f_{sync}$  clock can be distributed to XTAL\_IN of other devices on the PCB. The host has to configure the other master devices ac-

ordingly in CLK\_CTRL.

The CLK\_OUT port should be enabled after the IO-Link Master device completely configured to ensure the correct output frequency at system startup.

## 5.23 SPI Interface

The SPI interface is used for configuration, diagnostic and data transfer purposes. The SPI provides 16 bit read and write access as well as burst access to the internal transceiver (TRX) buffers.

The SPI interface consists of the pins SCSN, SCLK, MOSI, MISO, INTN supplied by VDD voltage. The input thresholds and output levels are referenced to this voltage. Digital input pins have pull-up/-down circuits described in chapter „Pinout description“

Several consecutive bytes are transferred during active

chip select form a SPI access. SPI characters are transferred MSB first. The E981.12 uses two different SPI access types:

- Standard register access (16 bit)
- TRX buffer burst access

The first byte of a SPI access is the command byte. It contains:

- Bit 7: 0 = read or 1 = write access
- Bit 6: 0 = single or 1 = burst access
- Bits 5/4: always 0
- Bits 3..0: register or buffer code

## 5.24 Standard Register Access

The standard register access is used for all configuration and status registers. An interbyte gap of  $t_{IBG}$  has to be ensured by the host.

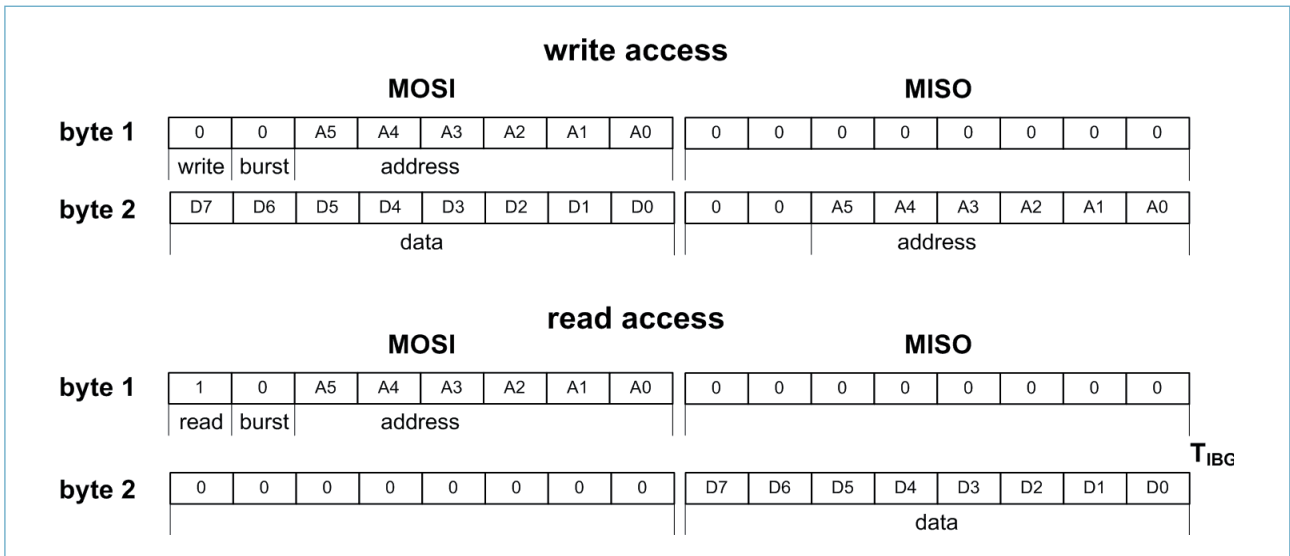


Figure 14. SPI single read and write access

### 5.25 TRX Buffer Burst Access

This access type is used for the UART TRX buffer (see chapter „Transceiver UART“). During burst access the second byte will contain the information about the number of data bytes which are read or written during SPI communication.

SPI transfer is secured by a XOR checksum to detect SPI communication errors. The last byte of the host trans-

mission contains the XOR checksum byte. For host write access the E981.12 compares this checksum with the calculated checksum. For host read access the host has to compare this checksum with the calculated checksum.

Transmission error is indicated by an interrupt XORIRQ in register ISTAT. This interrupt can not be masked.

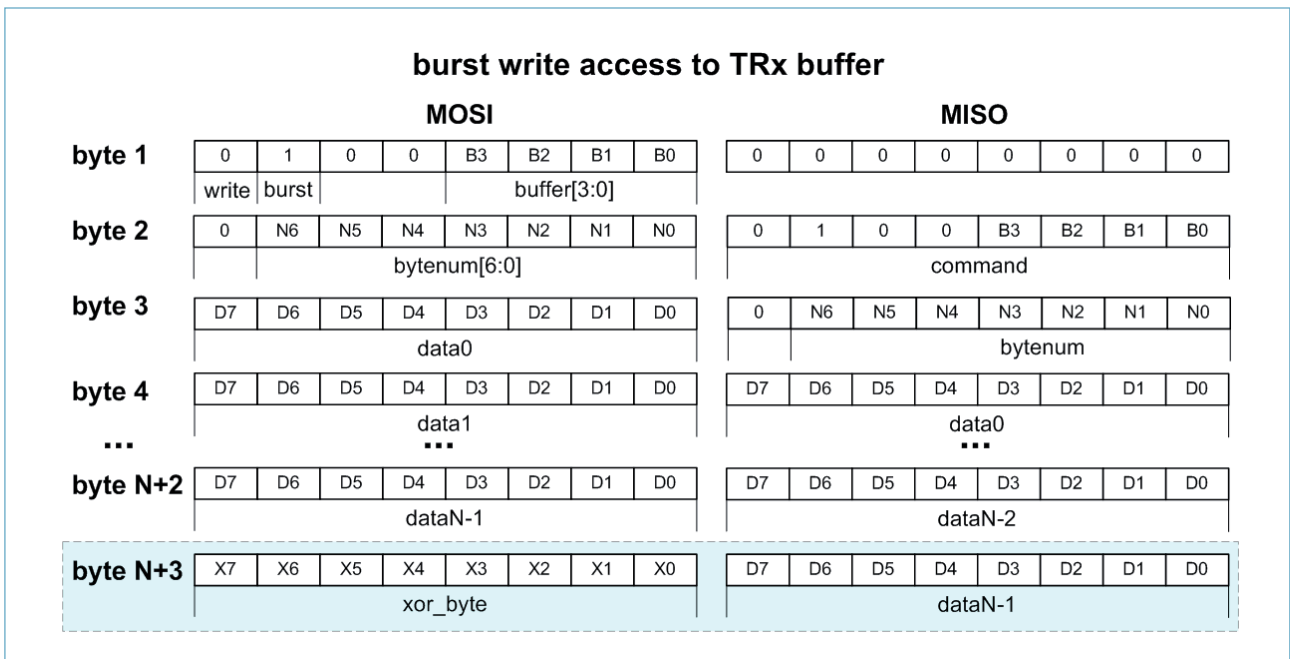


Figure 15. UART buffer burst write access

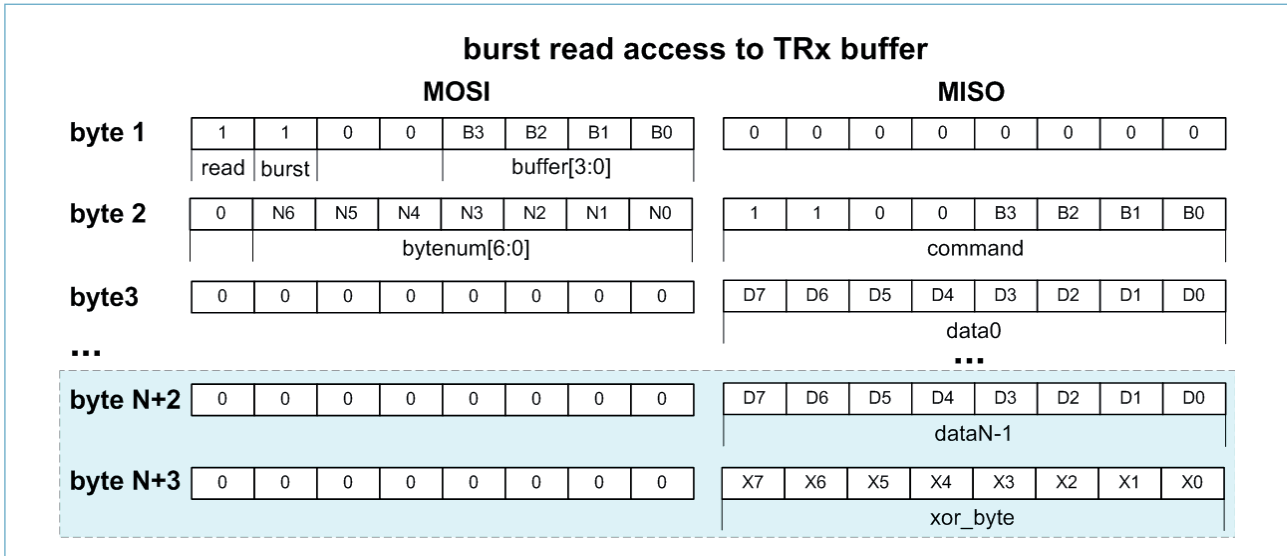


Figure 16. UART buffer burst read access

### 5.26 SPI Timing

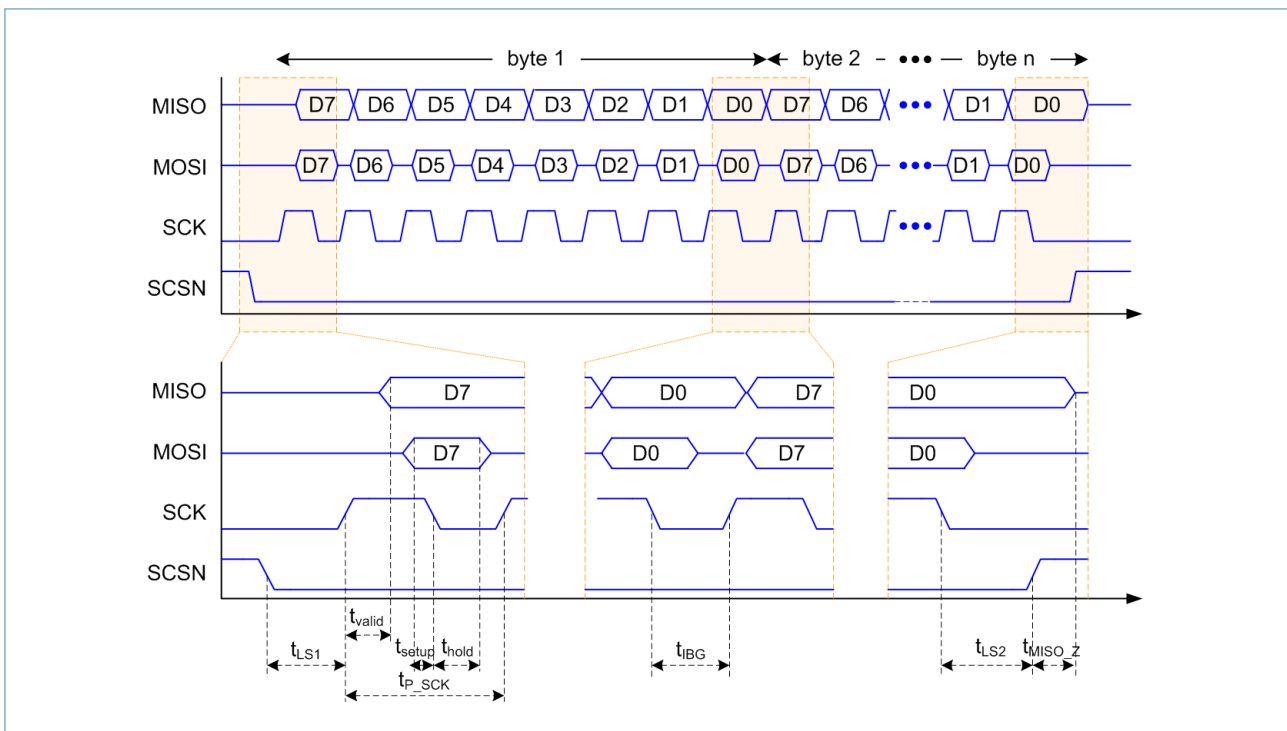
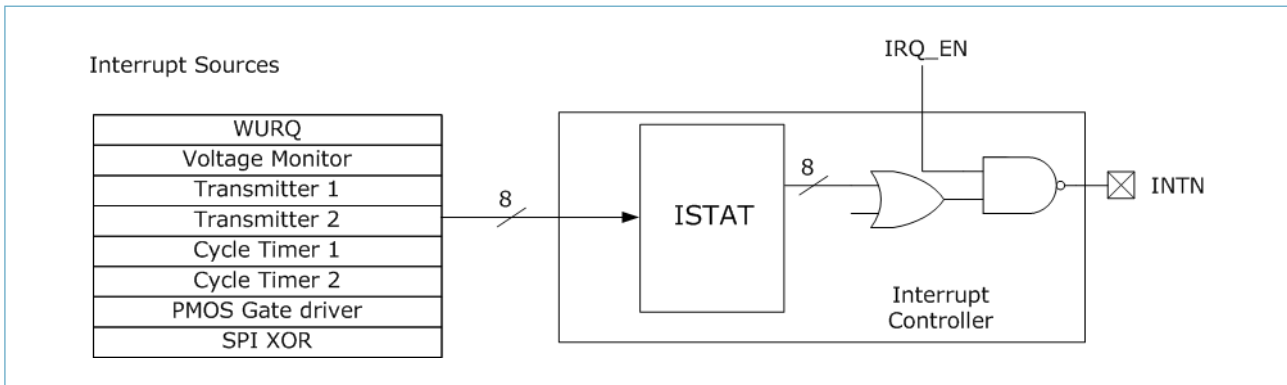


Figure 17. SPI timing

### 5.27 Interrupt Controller

The interrupt controller generates the output signal at pin INTN. All interrupt sources except of XORIRQ can be masked. ISTAT is the interrupt status register. The interrupt is kept active until the corresponding status register has been read. If all interrupts are masked the software is still able to recognize interrupts by polling the status register.

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The following Table lists all modules which can generate interrupts. The interrupts are explained in detail in the corresponding chapters.

Table 26. Interrupt Sources

Interrupt	Module	Description
UART & Timer Interrupt	Transceiver UART and IO-Link cycle timer	wait for Timer SYNC, RXNUM-Error, RDY and Buffer access violation
VMON interrupt	Voltage monitoring	One of the voltages not in specified range
Transmitter interrupt	Transmitter	Overcurrent or Overtemperature at CQ_OUTx
Gate driver interrupt	PMOS gate driver	PMOS Gate driver over current
SPI error interrupt	Host interface	Error during SPI burst access (XOR checksum not correct)
Wake-up ready interrupt	WURQ timer	Wake-up pulse completed

Table 27. Interrupt source register

Register Name	Address	Description
ISTAT	0x00	Interrupt source register

Table 28. ISTAT

ISTAT (0x00)	MSB							LSB
Content	WUIRQ	XORIRQ	PDIRQ	VMIRQ	TXIRQ2	TXIRQ1	TIRQ2	TIRQ1
Reset Value	0	0	0	0	0	0	0	0
External Access	R	R	R	R	R	R	R	R
Bit Description	WUIRQ : 1 = WURQ sequence IRQ XORIRQ : 1 = SPI error IRQ - XOR checksum not correct PDIRQ : 1 = PMOS gate driver IRQ VMIRQ : 1 = Voltage monitoring IRQ TXIRQ2 : 1 = Transmitter 2 IRQ TXIRQ1 : 1 = Transmitter 1 IRQ TIRQ2 : 1 = IO-Link cycle timer 2 IRQ TIRQ1 : 1 = IO-Link cycle timer 1 IRQ							

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## 5.28 IO-Link Supply Control

The IO-Link Supply Control controls the supply voltage Lx using an external PMOS power MOSFETs. The following figure shows the principle.

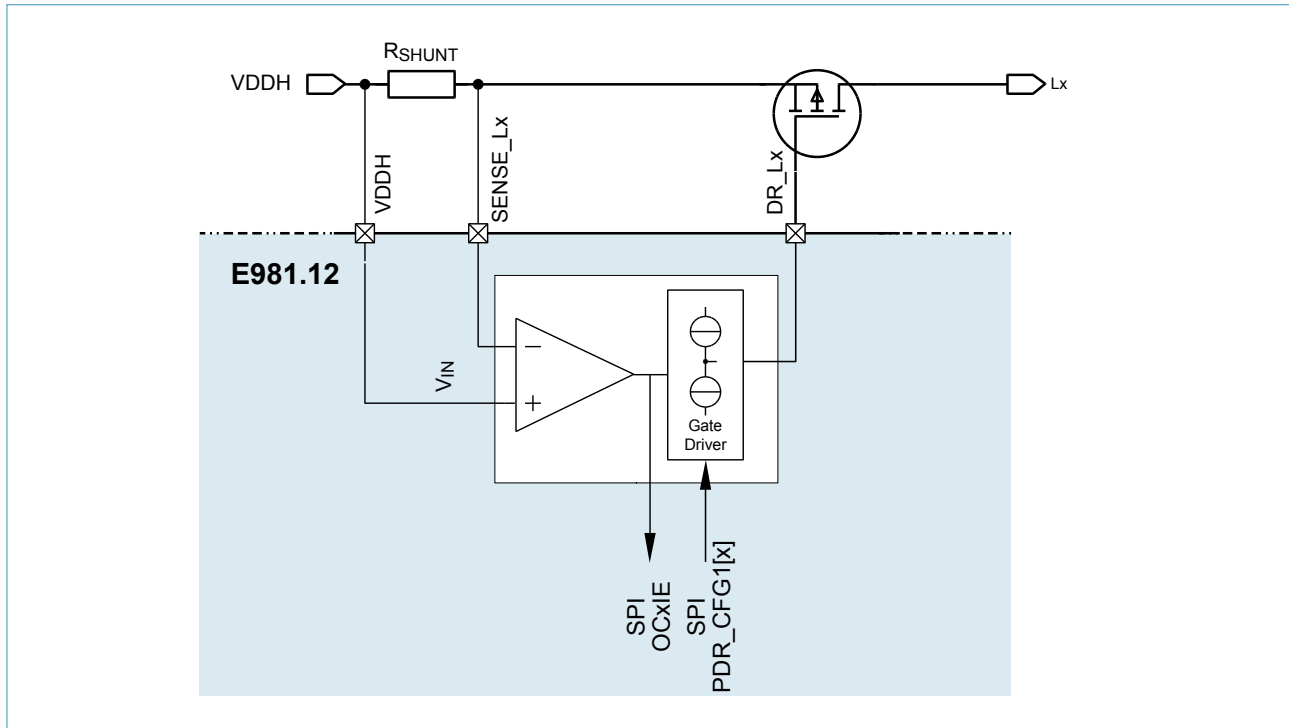


Figure 18. IO-Link Supply Control

The FET can be activated or deactivated by SPI register PDR\_CFG1.

To limit the current in case of failures it is measured using an external shunt resistor. If the voltage drop at the shunt resistor exceeds the threshold  $V_{IN\_OCCOMP}$ , the overcurrent condition is signaled in SPI register and optionally an interrupt is generated. The overcurrent detection threshold  $I_{TH(OC)}$  is typically  $V_{IN\_OCCOMP} / R_{shunt}$ , where  $R_{shunt}$  is the external shunt resistance (e.g.  $I_{TH(OC)} = 90\text{mV} / 100\text{mOhm} = 0.9\text{A}$ ).

The gate of the external FET is controlled according to the voltage drop of the shunt resistor so that the current is limited. The limit  $I_{TH(LIM)}$  is given by  $V_{IN\_OC} / R_{shunt}$  (e.g.  $I_{TH(LIM)} = 100\text{mV} / 100\text{mOhm} = 1\text{A}$ ). The external FET is switched off after a configurable time to limit power dissipation in this state. This event can trigger an interrupt if it has been enabled by OcxE in

register PDR\_CFG2.

After a configurable off-time the driver is switched on automatically. The duty cycle of this cyclic switching must be configured in register PDR\_CFG1 to keep the external FET within the safe operating area. Both automatic switching-off and switching-on can also be disabled in this register. When automatic switching-on is disabled the FET can be re-enabled by reading the register PDR\_STAT only. When automatic switching-off is disabled and an overcurrent has been detected, the FET remains in current limitation state.

The PMOS-Driver can simply work as a switch, when the bit HARDSW in the register PDR\_CFG2 is set. In case of detecting an overcurrent the external FET is switched off immediately. In this mode cyclic switching is disabled. To enable the FET after a shutdown the register PDR\_STAT has to be read.

## 5.29 Status and Control Registers

Table 29. PMOS gate driver register table

Register Name	Address	Description
PDR_CFG1	0x09	Configuration of PMOS gate control
PDR_CFG2	0x0A	Gate control interrupt enable
PDR_STAT	0x0B	Gate control status register

Table 30. Configuration of PMOS gate control

PDR_CFG1 (0x09)	MSB							LSB
Content	SHO1	SHO0	SHD1	SHD0	-	-	DR2	DR1
Reset Value	0	0	0	0	0	0	0	0
External Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	<b>SHO1 / SHO0:</b> Shutdown delay, parameter $t_{d,offx}$ <b>SHD1 / SHD0:</b> Shutdown duration, parameter $t_{offx}$ <b>DR2 :</b> 1 = Driver L2 enabled 0 = Driver L2 disabled <b>DR1 :</b> 1 = Driver L1 enabled 0 = Driver L1 disabled							

Table 31. Gate control interrupt enable

PDR_CFG2 (0x0A)	MSB							LSB
Content	-	-	OC2IE	-	-	-	OC1IE	HARDSW
Reset Value	0	0	0	0	0	0	0	0
External Access	R	R	R/W	R	R	R	R/W	R/W
Bit Description	<b>OC2IE :</b> 1 = Over current interrupt enable channel 2 <b>OC1IE :</b> 1 = Over current interrupt enable channel 1 <b>HARDSW :</b> 1 = External driver hard on/off switching							

Table 32. Gate control status register

PDR_STAT (0x0B)	MSB							LSB
Content	-	-	OC2IRQ	L2ON	-	-	OC1IRQ	L1ON
Reset Value	0	0	0	0	0	0	0	0
External Access	R	R	R	R	R	R	R	R
Bit Description	<b>OC2IRQ :</b> 1 = OC at L2 shunt interrupt flag. Cleared after read access. <b>L2ON :</b> 1 = Driver for L2 enabled 0 = Driver for L2 disabled (by register or OC) <b>OC1IRQ :</b> 1 = OC at L1 shunt interrupt flag. Cleared after read access. <b>L1ON :</b> 1 = Driver for L1 enabled 0 = Driver for L1 disabled by overcurrent							

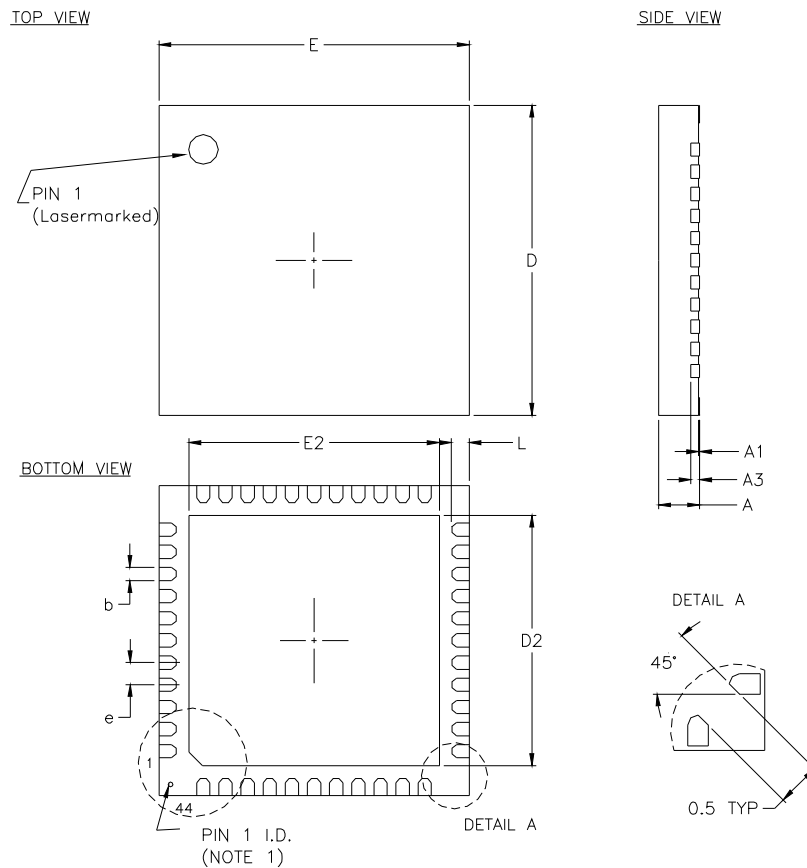
## 6 Register Table

Table 33. Register

Register Name	Address	Reference	Description
ISTAT	0x00	<a href="#">Page 28 Table 27</a>	Interrupt source register
VMON_STAT	0x02	<a href="#">Page 10 Table 2</a>	Voltage monitor status register
VMON_IE	0x03	<a href="#">Page 11 Table 3</a>	Voltage monitor interrupt enable register
WTIM_CFG	0x04	<a href="#">Page 23 Table 20</a>	WURQ configuration and status register
PDR_CFG1	0x09	<a href="#">Page 30 Table 30</a>	Configuration of PMOS gate control
PDR_CFG2	0x0A	<a href="#">Page 30 Table 31</a>	Gate control interrupt enable
PDR_STAT	0x0B	<a href="#">Page 30 Table 32</a>	Gate control status register
CLK_STAT	0x0C	<a href="#">Page 25 Table 25</a>	Clock status register
CLK_CTRL	0x0D	<a href="#">Page 24 Table 22</a>	Clock system control
CLK_FAC_LO	0x0E	<a href="#">Page 24 Table 23</a>	Clock divider register
CLK_FAC_HI	0x0F	<a href="#">Page 25 Table 24</a>	Clock divider register
CH_CFG	0x10	<a href="#">Page 17 Table 5</a>	Channel 1 configuration
CH_STAT	0x11	<a href="#">Page 17 Table 6</a>	Channel 1 status and error register
TRX_CFG	0x12	<a href="#">Page 18 Table 7</a>	Transceiver config channel 1
TX_OCCFG	0x13	<a href="#">Page 18 Table 8</a>	Transmitter over current configuration register channel 1
UART_TXNUM	0x14	<a href="#">Page 18 Table 9</a>	Number of Bytes for TX channel 1
UART_RXNUM	0x15	<a href="#">Page 19 Table 10</a>	Number of Bytes for RX channel 1
TIM_CFG	0x16	<a href="#">Page 21 Table 15</a>	Timer config channel 1
TIM_IE	0x17	<a href="#">Page 21 Table 16</a>	Timer Interrupt enable register channel 1
TIM_STAT	0x18	<a href="#">Page 21 Table 17</a>	IO-Link Cycle Timer status register channel 1
TIM_PER	0x19	<a href="#">Page 22 Table 18</a>	IO-Link Cycle Timer Period and Prescale configuration channel 1
RX_STAT	0x1A	<a href="#">Page 19 Table 11</a>	Receiver status and error register channel 1
CH_CFG	0x20	<a href="#">Page 17 Table 5</a>	Channel 2 configuration
CH_STAT	0x21	<a href="#">Page 17 Table 6</a>	Channel 2 status and error register
TRX_CFG	0x22	<a href="#">Page 18 Table 7</a>	Transceiver config channel 2
TX_OCCFG	0x23	<a href="#">Page 18 Table 8</a>	Transmitter over current configuration register channel 2
UART_TXNUM	0x24	<a href="#">Page 18 Table 9</a>	Number of Bytes for TX channel 2
UART_RXNUM	0x25	<a href="#">Page 19 Table 10</a>	Number of Bytes for RX channel 2
TIM_CFG	0x26	<a href="#">Page 21 Table 15</a>	Timer config channel 2
TIM_IE	0x27	<a href="#">Page 21 Table 16</a>	Timer Interrupt enable register channel 2
TIM_STAT	0x28	<a href="#">Page 21 Table 17</a>	IO-Link Cycle Timer status register channel 2
TIM_PER	0x29	<a href="#">Page 22 Table 18</a>	IO-Link Cycle Timer Period and Prescale configuration channel 2
RX_STAT	0x2A	<a href="#">Page 19 Table 11</a>	Receiver status and error register channel 2

## 7 Package Information

The E981.12 is available in a Pb free, RoHS compliant, QFN44L7 plastic package according to JEDEC MO-220 K, variant VKKD-3. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020D with a soldering peak temperature of  $(260 \pm 5)^\circ\text{C}$ .



Description	Symbol	mm			inch		
		min	typ	max	min	typ	max
Package height	A	0.80	0.90	1.00	0.031	0.035	0.039
Stand off	A1	0.00	0.02	0.05	0.000	0.00079	0.002
Thickness of terminal leads, including lead finish	A3	--	0.20 REF	--	--	0.0079 REF	--
Width of terminal leads	b	0.18	0.25	0.30	0.007	0.010	0.012
Package length / width	D / E	--	7.00 BSC	--	--	0.276 BSC	--
Length / width of exposed pad	D2 / E2	5.50	5.65	5.80	0.217	0.223	0.229
Lead pitch	e	--	0.5 BSC	--	--	0.020 BSC	--
Length of terminal for soldering to substrate	L	0.35	0.40	0.45	0.014	0.016	0.018
Number of terminal positions	N		44			44	

**Note:** the mm values are valid, the inch values contains rounding errors



## 8 Marking

### 8.1 Top Side

- ▶ Elmos Logo
- ▶ E981.12A
- ▶ XXXPLYWWR@

Signature	Explanation
E / M / T	Volume production / prototype / test circuit
000.01	Elmos project number
A	Elmos project revision code
XXX	Production lot number
P	Assembler code
L	Production line code
YWW	Year and week of assembly
R	Mask revision code
@	Elmos internal code

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