Features

- Supply voltage range 8V to 36V
- Integrated 5V voltage regulator
- Wake-up detection
- Driver capability up to 200mA
- C/Q reverse polarity protection
- 3.3V / 5V compatible digital interface
- Baud rate selection up to 230kBaud
- Load current monitor and over current protection
- Over temperature protection
- Junction temperature up to +150°C
- QFN20L4 package

Applications

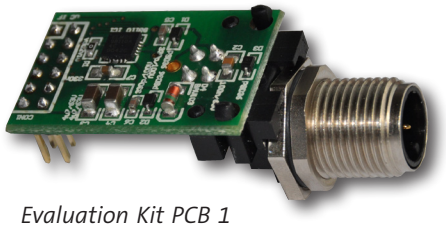
IO-Link is a point-to-point interface between existing field busses and sensor/actuator devices. IO-Link serves the transmission of specific parameters or data, like diagnosis information.

General Description

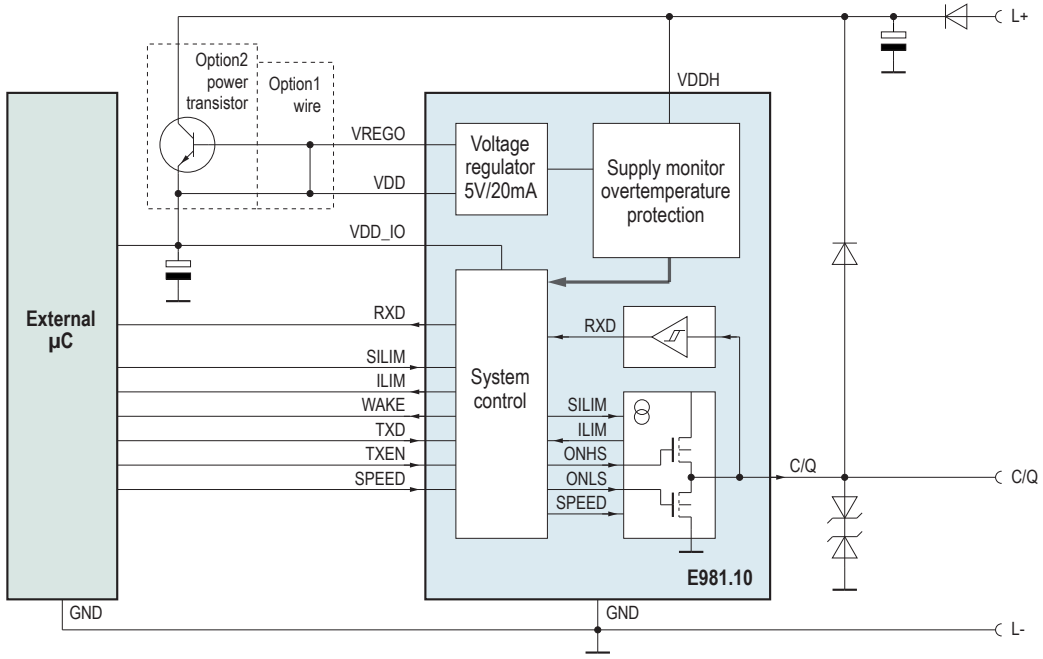
This IC is intended to be used as transceiver in IO-Link and standard IO mode applications in sensor and actuator devices. Communication and power supply work across a common three wire cable to the IO-Link Master, so continued use of available wiring is possible.

The integrated voltage regulator provides 5V/20mA for external purposes. The output driver provides up to 200mA and features reverse polarity protection plus over current protection. It can be configured as low side, high side, or push-pull driver. The switchable slew rate allows low and optimized electromagnetic radiation.

The tiny package outline allows usage even in applications with very limited board space.



Evaluation Kit PCB 1



1 Pinout

1.1 Pin description

No	Name	Type [1)]	Pull	Description	Connection
1	VDD_IO	S	-	Supply host interface	See specification
2	SILIM	D_I	Down	Reduced overcurrent limitation threshold	See specification
3	GND2	S	-	Ground	Connect to system ground
4	TEST	D_I	Down	Test	Connect to system ground
5	NC			Not internally connected	Connect to system ground
6	ATB	A_IO	-	Test	Not connected or connect to system ground (prefered)
7	VDD	S	-	Internal supply I/O	See specification
8	VREGO	HV_A_IO	-	Regulator control output	See specification
9	NC			Not internally connected	Not connected (reduce risk of leakage or short circuit to neighbour pins)
10	VDDH	S	-	Main supply	See specification
11	NC			Not internally connected	Not connected (reduce risk of leakage or short circuit to neighbour pins)
12	C/Q	HV_A_IO	-	IO-Link interface	See specification
13	NC			Not internally connected	Not connected (reduce risk of leakage or short circuit to neighbour pins)
14	GND1	S	-	Ground	Connect to system ground
15	ILIM	D_O	-	Overcurrent signal	See specification
16	WAKE	D_O	-	Wake-up request	See specification
17	RXD	D_O	-	Receive signal	See specification
18	TXD	D_I	Up	Transmit signal	See specification
19	SPEED	D_I	Down	Baud rate / slope control	See specification
20	TXEN	D_I	Down	Transmitter enable	See specification
21	GND3, Exposed die pad	S	-	The exposed die pad is the backside metal pad of the package	Connect to system ground

1) D = Digital, A = Analog, S = Supply, I = Input, O = Output, HV = High Voltage

1.2 Package pinout QFN20L4

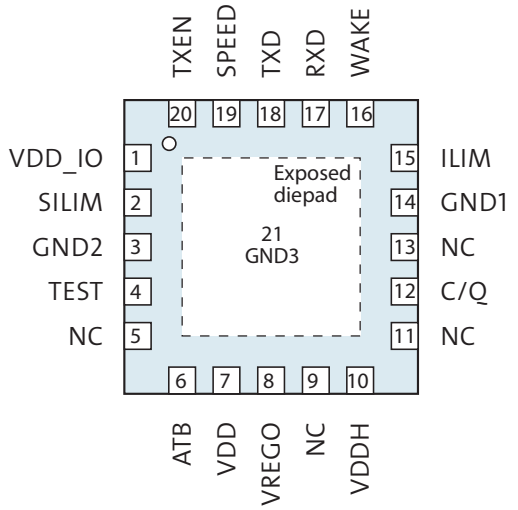


Figure 1: Package pinout top view

All GND pins have to be connected to local GND of the application.

2 Block Diagram

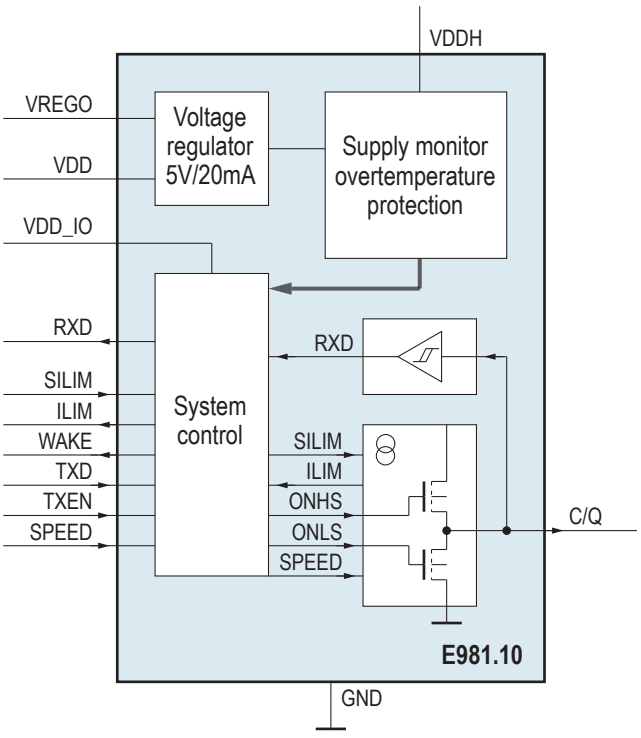


Figure 2: Block Diagram

3 Operating Conditions

3.1 Absolute Maximum Ratings

Continuous operation of the device above these ratings is not recommended and may destroy the device. All potentials referred to GROUND (GND) unless otherwise specified. Currents flowing into the circuit pins have positive values.

No.	Description	Condition	Symbol	Min.	Max.	Unit
1	Continous DC voltage at VDDH		VDDH	-0.3	40	V
2	Continous DC voltage at VDD_IO		VDD_IO	-0.3	5.5	V
3	Continous DC voltage at C/Q pin	C/Q-GND	VCQ	-40	40	V
4	Voltage at C/Q	t<500ms C/Q-GND		-40	60	V
5	Continous DC voltage at C/Q pin	VDDH-C/Q	VCQ		40	V
6	Voltage at C/Q	t<500ms VDDH-C/Q			60	V
7	Continous DC voltage at digital I/Os		VIO_DIG	-0.3	VDD_IO+0.3	V
8	AEC Q100-002 (HBM)		ESD immunity	2		kV
9	Storage temperature		Tstg	-40	125	°C
10	Junction temperature		Tj		150	°C
11	Ambient temperature		Ta		125	°C
12	Power dissipation		PV		900	mW

3.2 Recommended Operating Conditions

The following conditions apply unless otherwise stated. All potentials referred to GROUND (GND) unless otherwise specified.Currents flowing into the circuit pins have positive values.

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Supply voltage at pin VDDH		VDDH	8	24	36	V
2	Digital interface supply	3.3V interface supply	VDD_IO	3	3.3	3.6	V
3	Digital interface supply	5V interface supply	VDD_IO	4.5	5	5.5	V
4	Operating temperature range		Top	-40		100	°C
5	Supply voltage at pin VDDH for IO-Link communication		VDDH	18	24	30	V

4 Detailed Electrical Specification

4.1 Power Supply

4.1.1 VDDH

4.1.1.1 DC Characteristics

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Supply current at VDDH	No external load at VDD / VREGO TXEN=LOW	IDDH		1.5	4	mA

4.1.2 VDD_IO

4.1.2.1 DC Characteristics

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Supply current at VDD_IO	Static condition	IDD_IO		20	50	µA
2	VDD_IO undervoltage threshold		VDD_IO_UV	1.5		3	V

4.1.3 VDD / VREGO

4.1.3.1 DC Characteristics

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Voltage at Pin VDD	VDDH=8 ... 36V	VDD	4.75	5	5.25	V
2	Voltage at Pin VREGO	External NPN transistor used	VREGO		VDD+ 0.7		V
3	Available output current for external application	VDD=VREGO	IREG_ext			20	mA
4	VDD undervoltage threshold		VDD_UV	3.5		4.5	V
5	VDD supply current	VDD=5V	IDD		0.6	2	mA

4.1.3.2 AC Characteristics

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Decoupling capacitor at VDD		C_VDD	100/330 [1)]		2000	nF

1) C_VDD = 100nF is sufficient for the stable operation of the voltage regulator. However for a good blocking of the 5V supply (spike supression) it is recommended to use 330nF or more (up to 2µF).

4.2 Host interface

4.2.1 DC Characteristics

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	High level input voltage	Input Pins	VDIG_IH	0.7			VDD_IO
2	Low level input voltage	Input Pins	VDIG_IL			0.3	VDD_IO
3	High level output voltage	Iload=2mA; Pins RXD, WAKE, ILIM	VDIG_OH	0.8			VDD_IO
4	Low level output voltage	Iload=-2mA; Pins RXD, WAKE, ILIM	VDIG_OL			0.2	VDD_IO
5	Input pull down or pull up current	Vpin= VDD_IO= 5V Vpin= VDD_IO= 3.3V	Ipd		30 15		µA

4.3 Transmitter

4.3.1 DC Characteristics

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	DC driver residual voltage low	IQLs=100mA, TXD=high,	VRQLs			1.5	V
2	DC driver residual voltage high	IQHs=-100mA, TXD=low,	VRQHs	VSUP-1.7			V
3	DC driver residual voltage low	IQLs=200mA, TXD=high 8V ≤ VDDH < 15V	VRQLs			2.5	V
4	DC driver residual voltage low	IQLs=200mA, TXD=high, 15V ≤ VDDH ≤ 36V	VRQLs			2.0	V
5	DC driver residual voltage high	IQHs=-200mA, TXD=low, 8V ≤ VDDH < 15V	VRQHs	VSUP-2.5			V
6	DC driver residual voltage high	IQHs=-200mA, TXD=low, 15V ≤ VDDH ≤ 36V	VRQHs	VSUP-2.0			V
7	Overcurrent shutoff threshold low	Driver current low, TXD=high SILIM=low	ITHL_OFF	220	350	480	mA
8	Overcurrent shutoff threshold high	Driver current high, TXD=low SILIM=low	ITHH_OFF	-480	-350	-220	mA
9	Reduction of overcurrent shutoff threshold (Divided by) in contrast to SILIM=low	SILIM=high			2		

4.3.2 AC Characteristics

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Output voltage rise time 230.4kBaud	Cload=5nF, Rload=2k SPEED=high, TXD high to low transition	TDR			896	ns
2	Output voltage rise time 38.4kBaud	Cload=5nF, Rload=2k SPEED=low, TXD high to low transition	TDR			5.2	µs
3	Output voltage fall time 230.4kBaud	Cload=5nF, Rload=2k SPEED=high, TXD low to high transition	TDF			896	ns
4	Output voltage fall time 38.4kBaud	Cload=5nF, Rload=2k SPEED=low, TXD low to high transition	TDF			5.2	µs
5	On time with overload	Short to supply, single overload event	TON_OL	5		75	µs
6	Off time after overload detection	VDDH=8V	TOFF_OL_8V	5	12	25	TON_OL
7	Off time after overload detection	VDDH=36V	TOFF_OL_36V	15	35	80	TON_OL
8	Setup time TXD stable before transition TXEN=LOW to TXEN=HIGH	Application information	Tsetup	1			µs
9	Hold time TXD stable after transition TXEN=HIGH to TXEN=LOW	Application information	Thold	1			µs
10	Propagation Delay TXEN to transmitter enable after transition TXEN=LOW to TXEN=HIGH		Tprop_txen			1	µs

4.4 Receiver

4.4.1 DC Characteristics

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Input threshold high	18V < VDDH < 30V	VTHHs	10.5		13	V
2	Input threshold low	18V < VDDH < 30V	VTHLs	8		11.5	V
3	Input threshold hysteresis	18V < VDDH < 30V	VHYSs	1	2.5	4	V
4	Receiver input resistance	-3V < VCQ < VSUP+3V	RRX	10	20	40	kOhm
5	VDDH voltage range for IO-Link conform communication		VDDH	18		30	V

4.4.2 AC Characteristics

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Receiver delay	Information parameter	TD_RX		200	300	ns
2	Accepted minimum bit length (debounce window)		TBIT_MIN	250		1000	ns

4.5 Wake-up

4.5.1 DC Characteristics

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Supply voltage at VDDH for wake-up functionality		VDDH	18		32	V

4.5.2 AC Characteristics

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Wake-up debounce time	Single event of over-load with receiver level change opposite to TXD	Twu	20		74	µs

4.6 Temperature monitor

4.6.1 DC Characteristics

No.	Description	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Overtemperature threshold		Tover	155	175	200	°C

5 Functional Description

5.1 Power Supply

VDDH is the main supply pin. Pin VDD_IO supplies the host interface and allows an adaptation to 3.3V or 5V host supply levels. Pin VREGO is the voltage regulator output and Pin VDD is 5V sense input and internal supply. An external 5V supply can be applied at VDD, if the internal regulator is not intended to be used. In this case VREGO must be left open. If the internal regulator is used, pin VDD has to be connected to the regulator output pin VREGO. If external components must be supplied with the regulated 5V, the regulator current driving capability can be extended by an external NPN transistor.

5.1.1 VDDH

VDDH is the main supply voltage for the IC.

5.1.2 VDD_IO

VDD_IO is the supply voltage for the IO-stages between the IC and the host. It can be at 3.3V or 5V level. If VDD_IO is under VDD_IO_UV the transmitter is disabled.

5.1.3 VDD

Pin VDD supplies the internal blocks. The supply voltage VDD can be applied externally or generated by the internal 5V regulator. An external NPN boost transistor can be connected to pins VREGO (Base) and VDD (Emitter) in order to supply external devices too. If the voltage regulator is used without external transistor, both pins have to be connected. If VDD is lower than VDD_UV the transmitter is disabled.

Power supply	Pin VREGO	Pin VDD	Supply current for external components
1. With internal voltage regulator	Short to VDD	Short to VREGO	<20 mA
2. With external supply	Open	Connected to external supply	External supply
3. With external boost transistor (collector to VDDH)	Connected to base of npn transistor	Connected to emitter of npn transistor	Depends on npn transistor

5.1.4 Power up sequences

As the supply voltage VDDH is applied, an internal voltage generator supplies the bandgap reference with 5V. The voltage regulator starts up and supplies the internal circuitry and optionally external circuits as well. The power on reset circuit releases the digital logic.
The supply voltage VDD_IO must be present in order to supply the host interface and enable the transmitter.
If the internal voltage regulator is not used, an external 5V has to be applied at pin VDD. No sequence is mandatory in order to apply VDD and VDD_IO.

5.2 Host interface

The logic level at the digital interface pins must be in accordance with the supply of the external control circuitry. This supply voltage is applied to pin VDD_IO. Level shifter adapt the logic information to the internal supply. Thus the IC can operate together with control devices operating from 3.3V or 5V supplies. Digital input pins have pull-up/down circuits in order to avoid erroneous response of the IC in case of broken control lines.

Input pins: TXEN, TXD, SPEED, SILIM
Output pins: RXD, WAKE, ILIM

A high level at pin TXEN enables the transmitter. A low level (default value if not connected) turns the transmitter off.
TXD determines the output level of the active transmitter. The default level is high. A low level at pin SPEED (default level) sets the transmitter to a transmission rate of 38.4 kBaud, high level to 230.4 kBaud.
A high level at pin SILIM divides the overcurrent threshold in low side and high side driver by 2 in contrast to the low level at SILIM.
Pin RXD provides the receiver output information from reading the level at pin CQ.
A high level at pin WAKE indicates the detection of a wake up event.
A high level at pin ILIM signals an overcurrent condition for the transmitter at pin CQ.

TXEN	TXD	C/Q	RXD
LOW	LOW	HIGH-Z	Inverted C/Q
LOW	HIGH	HIGH-Z	Inverted C/Q
HIGH	LOW	HIGH	LOW
HIGH	HIGH	LOW	HIGH

5.3 Transmitter

The push- pull transmitter is activated with a high level on pin TXEN and drives the C/Q pin low or high in accordance with the inverted logic level on pin TXD. A slope control limits EME. The transition times can be set for two different baud rates. SPEED=low is default 38.4 kBaud or 4.8 kBaud, SPEED=high sets the transmission speed to 230.4 kBaud.
The transmitter is operable only if VDD and VDD_IO are within their specified limits.

Pin SPEED	Transmission rate
LOW	38.4 kBaud
HIGH	230.4 kBaud

In SIO mode the transmitter must be used in highspeed mode (SPEED=high) to enable a wide range of different load conditions.

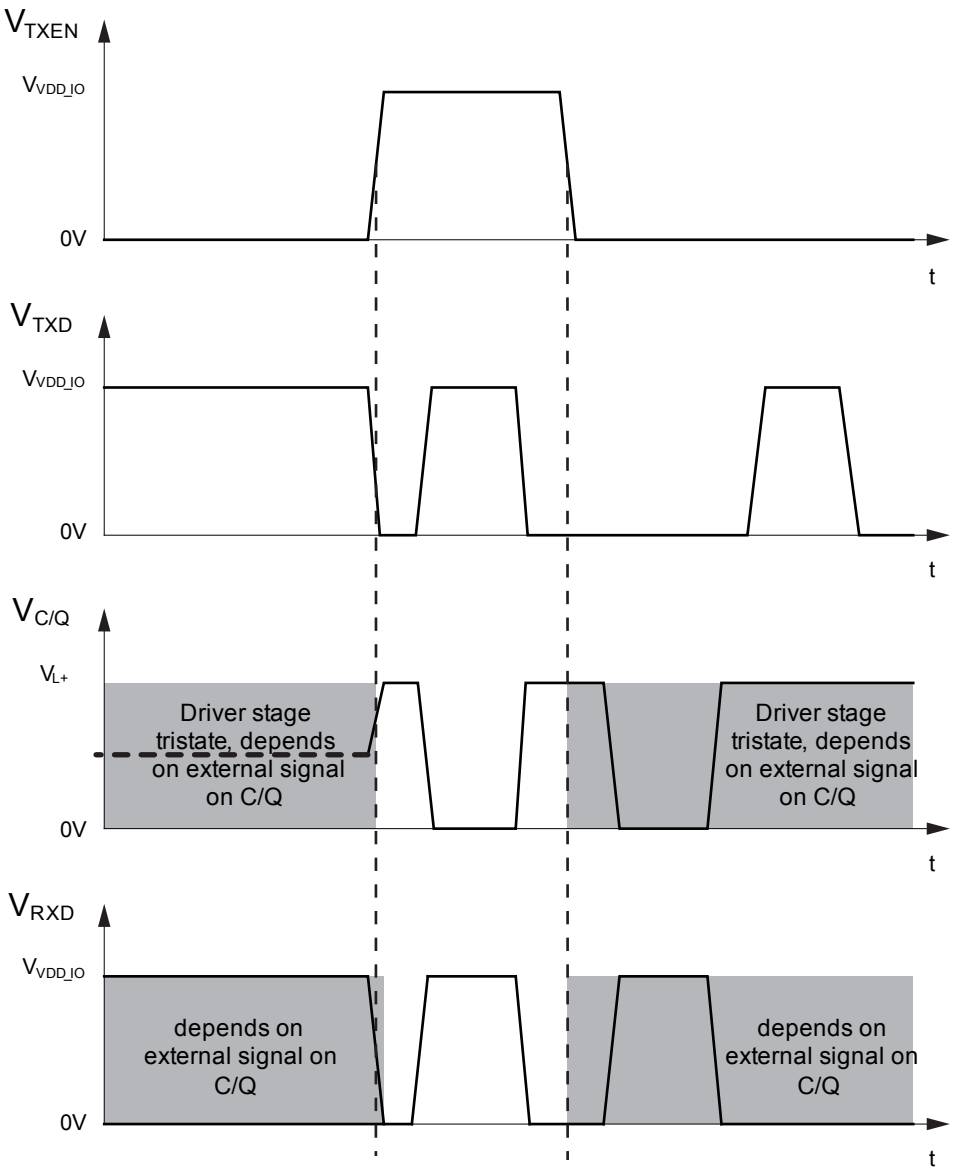


Figure 3: Transmitter polarity

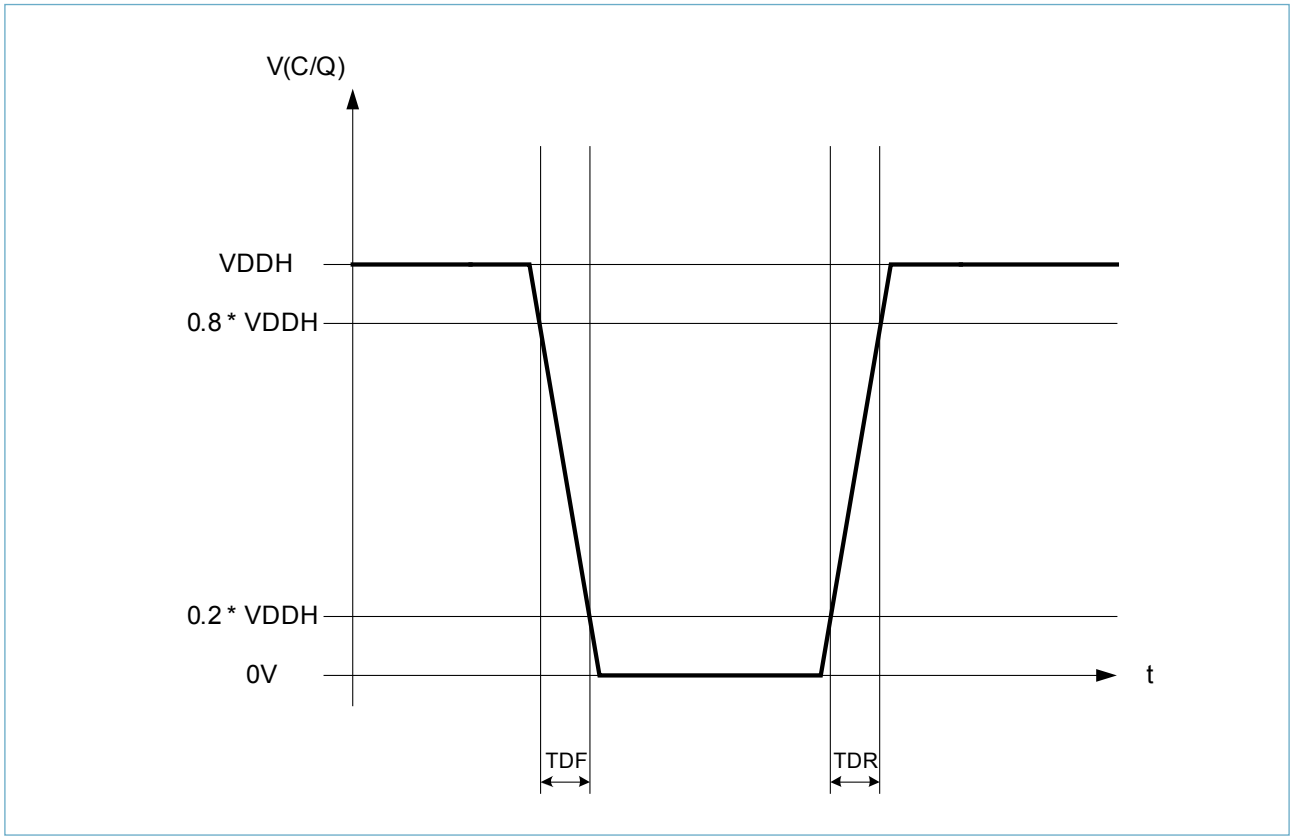


Figure 4: Transmitter characteristics

5.3.1 Transmitter overload

The transmitter is disabled in case of overcurrent, overtemperature or improper supply conditions and switched on after a time constant after the error condition has disappeared. The overcurrent information can be read from pin ILIM during the driver shutoff period. The off time after detecting an overcurrent or overtemperature is proportional to the supply voltage at pin VDDH.

The overcurrent threshold of the low side and high side drivers can be selected with the pin SILIM. The default level of SILIM is low. An high level at this pin divides the overcurrent threshold by 2.

5.3.2 Transmitter loads

Loads may be resistive or capacitive. If the load is inductive, the voltage at pin C/Q must be limited by properly dimensioned external clamping diodes.
The overload turn off time TOFF_OL_xx depends on the supply voltage level VDDH. Thus overload protection and lamp drive current cover a wide supply current range.
The on time after detecting an overcurrent depends on the assumption of a potential wake up condition (RXD changes state without changes in the control signals) or the assumption of a normal overload case (overload immediately detected after turn on). Inductive overloads may simulate a wake up condition and cause the driver to turn off for the current TXEN=low phase.

5.4 Receiver

The receiver reads logic information from the C/Q pin and proceeds it to the control unit. The data bits are filtered in order to suppress erroneous glitches on the C/Q pin and to increase EMC robustness. The receiver functionality will not be available in the whole IC supply range due to absolute thresholds. If the transceiver supply voltage falls below 18V, the system may not be able to guarantee sufficient high levels on the C/Q pin and the receiver will output a constant low level on pin RXD.

5.5 Wake-up

In case of an active transmitter the receiver monitors pin C/Q in order to detect wake up events. If the information read from the C/Q pin changes state, while TXD remains constant, a wake up event is assumed. Alternatively the change to an overcurrent state is evaluated in the same way. The transmitter remains on despite having detected an overload. After Twu the wake up event is signalled at pin WAKE and the transmitter is turned off. It can be reset with a TXEN=low and activated again with a new TXEN=high. The figure below shows the functionality of the overcurrent and wake up recognition as well as the resulting behavior at the pin ILIM and WAKE UP in detail.

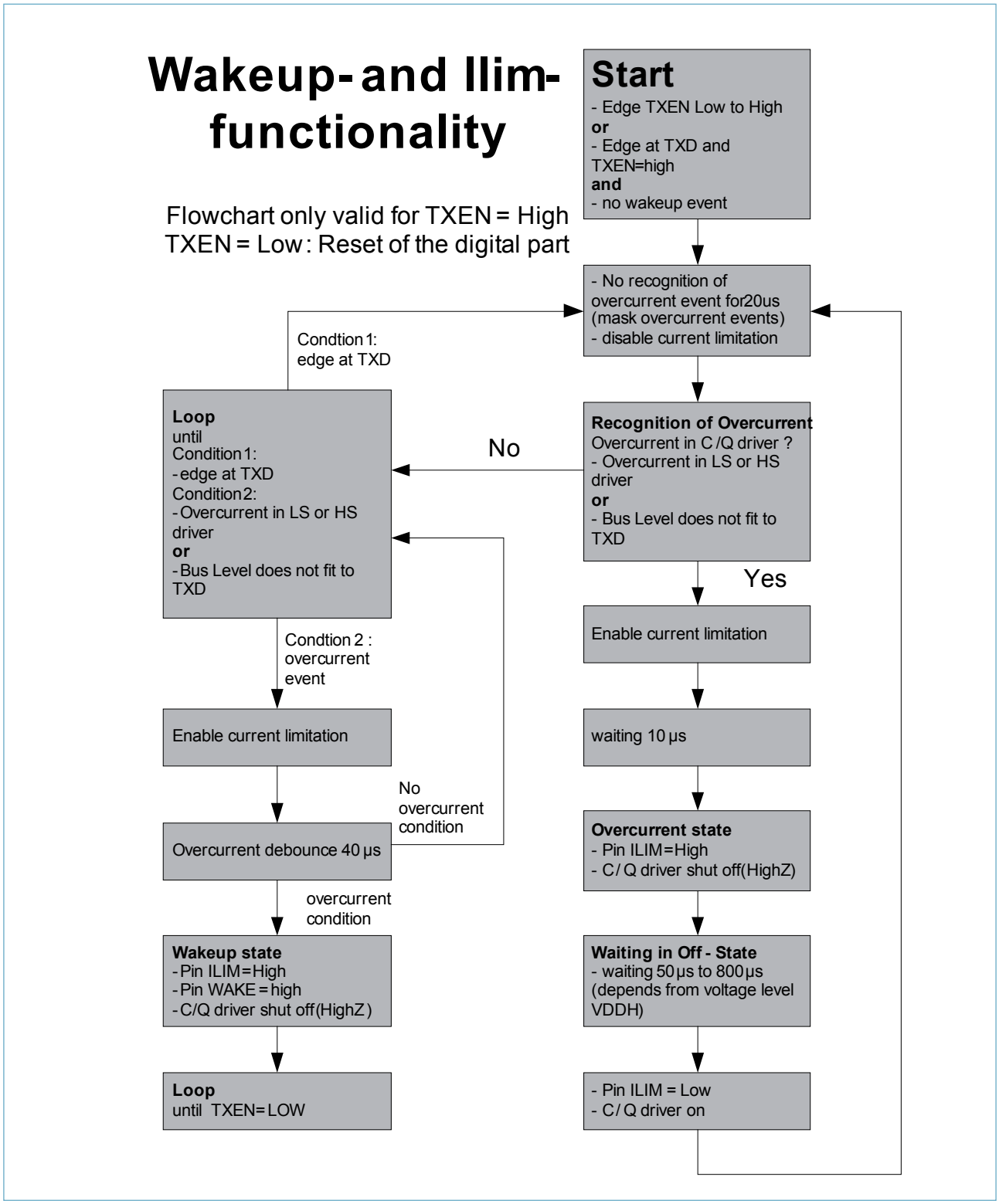


Figure 5: Overcurrent and wake up functionality

5.6 Temperature monitor

The temperature monitor shuts the transmitter off in case of excessive junction temperature which can occur with a too high ambient temperature and/or the dissipation of too much power within the IC.

6 Package Dimensions and Ratings

Package Type: QFN 4x4, 0.5mm pitch, 20 Pins
The package dimensions and ratings refer to JEDEC MO220 VGGD-5.

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