# elmos

## POWER LIN2.X STEPPER WITH STALL DETECTION
### PRODUCTION DATA - DEC 18, 2013

RoHS compliant

## Features

- For 1 bipolar  stepper or up to 3 DC motors
- Motor currents up to  2* 800mA (peak)
- Programmable chopper current values for sinus or customized micro-stepping
- 5.5 - 20V supply voltage  (load dump 42V)
- Very low sleep mode current,  typ.  30µA
- 8bit µController with assistance logic and
  - 256 Byte RAM,   boot-loader
  - 8kByte FLASH or ROM (opt. firmware)
  - 64 Byte EEPROM for customer parameters
- 3 * Hall-sensor/potentiometer inputs+supply
- LIN 2.x, SAE J2602 or bidirect. PWM-interface compatible to LIN2.2Rev.A, 2.2, 2.1, 2.0, 1.3
- QFN32L6 package

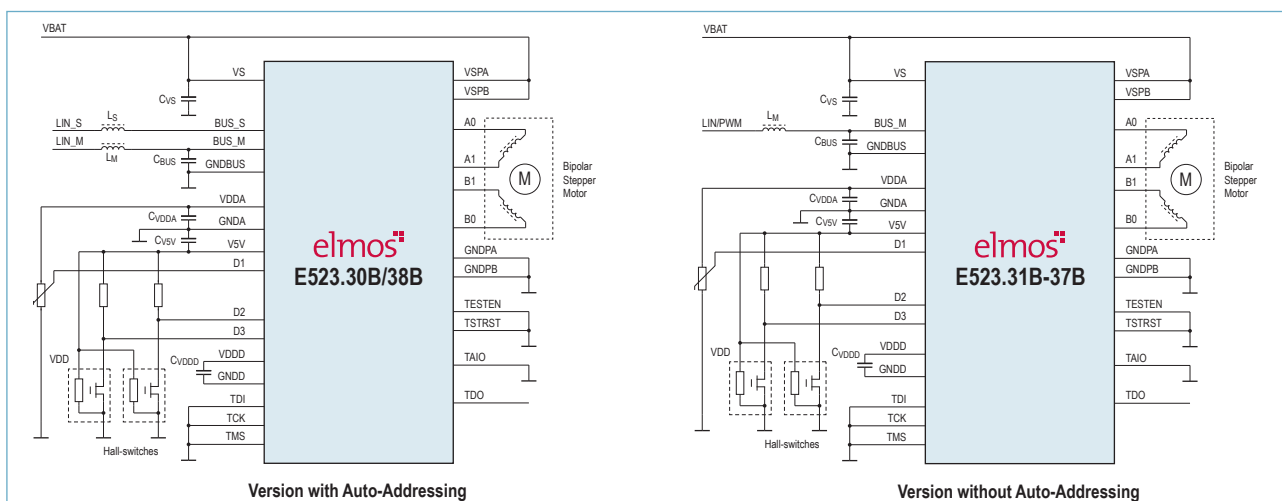## Added value factors

- Sensor less "stall detection"
- JTAG or LIN FLASH programming
- -40°C - +150°C peak junction temperature ( for higher temperatures please contact local supplier )
- optional: LIN with Auto-Addressing (SNPD)

## Applications

- Automotive  Head-Light-Adjust
- Automotive  Front-Grill-Shutter
- Automotive  Water-Valves

## General Description

This system-in-a-chip IC controls bipolar stepper actuators with current-choppered micro-stepping. The IC is controlled by a LIN2.x interface. It's LIN-address can calculated by the "auto-addressing" feature (called "SNPD" in official LIN-specification). Alternatively the IC can be controlled by a PWM-interface, with diagnosis feedback. The integrated sensor-less "stall-detection" detects mechanical end-positions and stops the motor to re-duce acoustical noise during initialization runs. The calculating heart is an 8-bit controller which is assisted by powerful circuitry. For absolute precise positioning, up to 3 Hall-sensors or potentiometers can read out. The IC can also drive up to 3 DC motors or other loads. ICs with FLASH-memory are programmable via JTAG interface or LIN in normal or high speed mode. The IC is available with standard firmware as well as  with a development system for individual firmware.
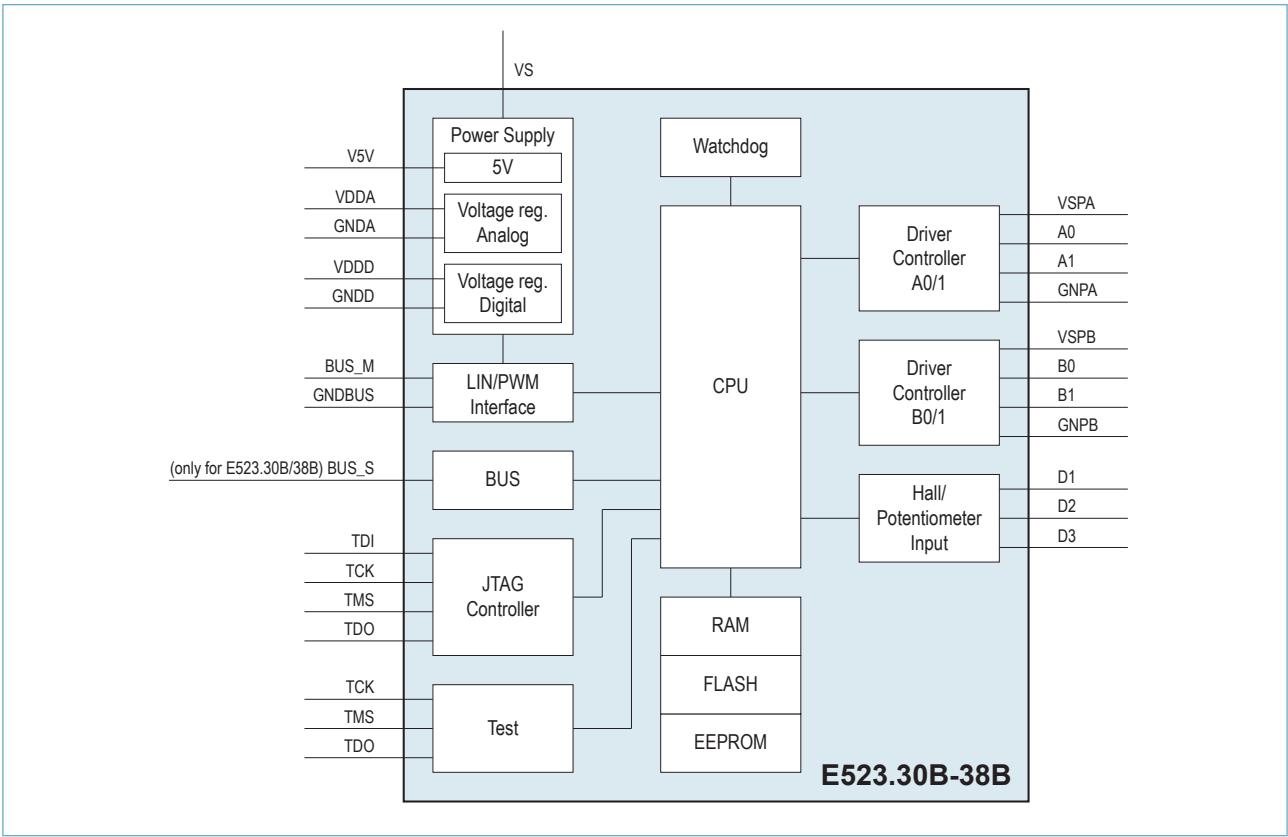
## Ordering Information

| Product ID | Features |
|---|---|
| E523.30B | LIN or PWM-interface, LIN auto-addressing, 8k customer FLASH |
| E523.31B | LIN with firmware (FLASH) |
| E523.32B | LIN with firmware (ROM) |
| E523.33B | LIN or PWM with 8k customer ROM |
| E523.34B | PWM interface 8k customer FLASH |
| E523.35B | PWM interface with firmware (FLASH) |
| E523.36B | PWM interface with firmware (ROM) |
| E523.37B | LIN or PWM with 8k customer FLASH |
| E523.38B | LIN, auto-addressing, 8k customer ROM |

## Typical Application Circuit



Version with Auto-Addressing



Version without Auto-Addressing

*Elmos Semiconductor AG reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.*

Elmos Semiconductor AG          Data Sheet          QM-No.: 25DS0115E.01

## Functional Diagram



## Pin Configuration
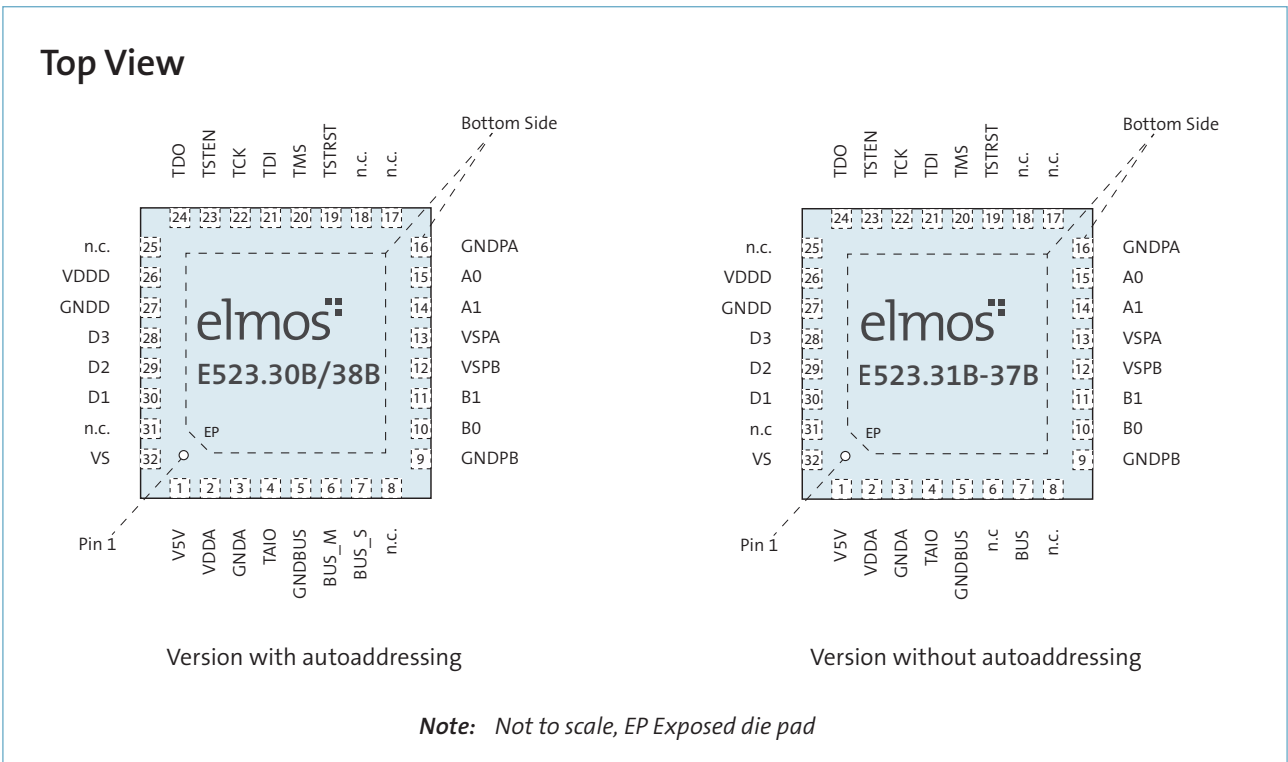
### Top View



Version with autoaddressing

Version without autoaddressing

*Note:* Not to scale, EP Exposed die pad

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## Pin Description

| Pin | Name | Type [1] | Description | Power-up state |
|---|---|---|---|---|
| 1 | V5V | S | Hall sensor supply | off |
| 2 | VDDA | S | Regulator output for analog supply | |
| 3 | GNDA | S | Ground for analog supply | |
| 4 | TAIO | IO | Analog test bus | |
| 5 | GNDBUS | S | LIN or PWM ground | |
| 6 | BUS_M or n.c. | IO | LIN bus (master direction) or PWM interface, not connected at versions without auto-addressing | Transmitter off |
| 7 | BUS_S or BUS | IO | LIN bus interface (sensing toward slave direction) or not connected | BUS pull-up off (OEM requirements) Receiver Wake-up threshold enabled |
| 8 | n.c. | - | Not connected | |
| 9 | GNDPB | S | Ground for half bridges B | |
| 10 | B0 | O | Motor coil driver B output 0 | |
| 11 | B1 | O | Motor coil driver B output 1 | Driver off |
| 12 | VSPB | S | Power supply for driver B | Driver off |
| 13 | VSPA | S | Power supply for driver A | |
| 14 | A1 | O | Motor coil driver A output 1 | |
| 15 | A0 | O | Motor coil driver A output 0 | Driver off |
| 16 | GNDPA | S | Ground for half bridges A | Driver off |
| 17 | n.c. | - | not connected | |
| 18 | n.c. | - | not connected | |
| 19 | TSTRST | I | Test mode reset | |
| 20 | TMS | I | Test mode select (JTAG) | |
| 21 | TDI | I | Test data in (JTAG) | |
| 22 | TCK | I | Test clock (JTAG) | |
| 23 | TESTEN | I | Test mode enable | |
| 24 | TDO | O | Test data out (JTAG) | |
| 25 | n.c. | - | not connected | |
| 26 | VDDD | S | Regulator output for digital supply | |
| 27 | GNDD | S | Ground for digital supply | |
| 28 | D3 | IO | General purpose I/O, Hall-sensor or potentiometer input | |
| 29 | D2 | IO | General purpose I/O, Hall-sensor or potentiometer input | |
| 30 | D1 | IO | General purpose I/O, Hall-sensor or potentiometer input | |
| 31 | NC | - | not connected | |
| 32 | VS | S | Battery voltage for internal supplies | |
| - | EP | S | Exposed Die Pad | |

1) A = Analog, D = Digital, S = Supply, I = Input, O = Output, HV = High Voltage

The QFN die pad shall be connected to ground. For ESD details see section "ESD".

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

# 1 Absolute Maximum Ratings

*Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages with respect to ground. Currents flowing into terminals are positive, those drawn out of a terminal are negative.*

| Description | Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Absolute maximum supply voltage | | $V_{VS}$, $V_{VSPA}$, $V_{VSPB}$ LIN2.2A-spec. Param11: $V_{SUP\_NON\_OP}$ | -0.3 | 40 | V |
| Continuous operating voltage | Half-bridge drivers activated | $V_{VS}$, $V_{VSPA}$, $V_{VSPB}$ | -0.3 | 20 | V |
| Jump start operating voltage | T ≤ 60s | $V_{VS}$, $V_{VSPA}$, $V_{VSPB}$ | -0.3 | 28 | V |
| Load dump operating voltage | T ≤ 0.5s | $V_{VS}$, $V_{VSPA}$, $V_{VSPB}$ | -0.3 | 42 | V |
| Reverse polarity supply voltage | T < 0.5s $I_{VS}$ > -1.0A | $V_{VS}$, $V_{VSPA}$, $V_{VSPB}$ | -1 | | V |
| Voltage difference between any two pins out of GNDA, GNDD and exposed pad | | $V_{GND1}$ | -0.3 | 0.3 | V |
| Voltage difference between GNDA and any pin out of GNDPA, GNDPB, GNDBUS | | $V_{GND2}$ | -0.8 | 0.8 | V |
| Junction temperature | | $T_J$ | -40 | 150 | °C |
| Storage temperature range | | $T_{ST}$ | -45 | 150 | °C |
| Thermal resistance (Junction to ambient) | QFN32L6 | $R_{TH,J-A}$ | 18 | 20 | K/W |
| Voltage at pin V5V | | $V_{V5V}$ | -0.3 | 5.5 | V |
| Voltage at pins VDDA and VDDD | | $V_{VDD}$ | -0.3 | 3.6 | V |
| Voltage at pins A0, A1, B0, B1 | | $V_{BRIDGE}$ | -1 | 43 | V |
| Voltage at test pins (TDI, TCK, TMS, TDO, TSTEN, TSTRST, TAIO) | [1] | $V_{TEST}$ | -0.3 | 3.6 or VDDD+0.3 | V |
| Voltage at D1, D2, D3 (digital IOs) | D1, D2, D3 programmed as digital IOs [1] | $V_{DxD}$ | -0.3 | 5.5 or V5V+0.3 | V |
| Voltage at D1, D2, D3 (analog ADC input) | D1, D2, D3 programmed as analog ADC input [1] | $V_{DxA}$ | -0.3 | 3.6 or VDDA+0.3 | V |
| Current into D1, D2, D3 | | $I_{DX}$ | -10 | 10 | mA |
| Current into pins A0, A1, B0, B1 | | $I_{BRIDGE}$ | -900 | 900 | mA |
| External load current drawn from pin V5V | | $I_{LOADV5V}$ | -45 | 0 | mA |
| External load current drawn from pin VDDA | | $I_{LOADVDDA}$ | -5 | 0 | mA |
| Current into test pins (TDI, TCK, TMS, TDO, TSTEN, TSTRST, TAIO) | | $I_{TEST}$ | -10 | 10 | mA |
| Voltage at pin BUS_S, BUS_M | | $V_{BUS}$ | -12 | 40 | V |
| Voltage at pin BUS_S, BUS_M, load dump | t<0.5s | $V_{BUS}$ | | 42 | V |

1) Whichever is smaller.

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E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## 2 Recommended Operating Conditions

| Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage [1] | LIN Bus operating | $V_{VS}$, $V_{VSP}$ LIN2.2A-spec. Param10: $V_{SUP}$ | 7 | | 18 | V |
| Supply voltage [1] | PWM interface operating and ECU running | $V_{VS}$, $V_{VSP}$ LIN2.2A-spec. Param9: $V_{BAT}$:>8V | 5.5 | | 18 | V |
| Supply voltage [1] | FLASH programming | $V_{VSFL}$ | 11 | | 15 | V |
| Operating junction temperature range | | $T_J$ | -40 | | 150 | °C |
| Operating ambient temperature | | $T_{amb}$ | -40 | | 125 | °C |
| Ambient temperature for FLASHing | | $T_{amb}$ | 0 | | 50 | °C |
| Blocking capacitor for supply voltage | | $C_{VS}$ | | 100 | | nF |
| Blocking capacitor for Hall supply voltage | | $C_{V5V}$ | | 1 | | μF |
| Blocking capacitor for analog supply voltage | | $C_{VDDA}$ | | 1 | | μF |
| Blocking capacitor for digital supply voltage | | $C_{VDDD}$ | | 1 | | μF |
| External load current drawn from pin V5V | | $I_{LOADV5V}$ | -40 | | 0 | mA |
| External load current drawn from pin VDDA | | $I_{LOADVDDA}$ | -4 | | 0 | mA |
| Number of LIN slaves capable of auto-addressing | | $N_{SL,AA}$ | | | 15 | |
| Ferrite RF attenuator proposal (optional for increasing performance at pin BUS, BUS_M, BUS_S) | High attenuation of RF Disturbances | $L_{M, LS}$ | | TDK MMZ201-2Y202B or equivalent | | |
| Source impedance at GPIO pins D1, D2, D3 | Pin Dx configured as 3.3V analog input | $R_{Dx}$ | | | 10 | kΩ |
| Input voltage on D1, D2 and D3 in analog mode | configured as analog input | $V_{D1}$, $V_{D2}$, $V_{D3}$ | 0V | | $V_{VDDA}$ | |
| Input voltage on D1, D2 and D3 in digital mode | configured as digital input | $V_{D1}$, $V_{D2}$, $V_{D3}$ | 0V | | $V_{V5V}$ | |

1) Above 18V the software must disable drivers and BUS before reaching the absolute max. rating of 20V.

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

# 3 ESD Protection

| Description | Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| ESD HBM Protection at all Pins | 1) | $V_{ESD(HBM)}$ | -2 | 2 | kV |
| ESD HBM Protection at Pin BUS/ BUS_M/BUS_S to system ground | 1) | $V_{ESD(HBM)}$ | -6 | 6 | kV |
| ESD HBM Protection at Pin VS/VSPA/ VSPB to system ground | 1) | $V_{ESD(HBM)}$ | -4 | 4 | kV |
| ESD CDM Protection at all Pins | 2) | $V_{ESD(CDM)}$ | -500 | 500 | V |
| ESD CDM Protection at Edge Pins | 2) | $V_{ESD(CDM)C}$ | -750 | 750 | V |
| ESD Machine Model | 3) | $V_{ESD(MM)}$ | -100 | 100 | V |

1)  According to AEC-Q100-002 (HBM) chip level test
2) According to AEC-Q100-011 (CDM) chip level test
3) According to AEC-Q100-003 (MM) chip level test

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## 4 Electrical Characteristics

($V_{VS}$ = +5.5V to +18V, $T_J$ = -40°C to +150°C, unless otherwise noted. Slew rate at pin VS < 1V/µs. Typical values are at $V_{VS}$ = +12V and $T_J$ = +25°C. Positive currents flow into the device pins.)

| Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Voltages** | | | | | | |
| Supply current | All motor drivers off, $I_{BUS}$=0, $I_{V5V}$=0 $V_{VS}$<18V | $I_{SUP}$ | | 8 | 15 | mA |
| Sleep mode current | $V_{VS}$<14V $T_{amb}$<50°C | $I_{VS\_sleep}$ | | 30 | 50 | µA |
| Power-on reset low threshold | $V_{VDDx}$ falling [1] | $V_{TL,POR}$ | 0.77 | 0.82 | 0.87 | $V_{VDDx}$ |
| Power-on reset high threshold | $V_{VDDx}$ rising [1] | $V_{TH,POR}$ | 0.85 | 0.90 | 0.95 | $V_{VDDx}$ |
| Power-on reset hysteresis | | $V_{HYST,POR}$ | 200 | | | mV |
| V5V hall sensor supply during ON | $V_{VS}$≥7V, $T_{amb}$<85°C $I_{V5V}$≤40mA or $V_{VS}$≥7V, $T_J$<150°C $I_{V5V}$≤10mA; | $V_{V5V}$ | 4.75 | 5 | 5.25 | V |
| V5V current limitation | | $I_{V5V\_lim}$ | 41 | 82 | 160 | mA |
| Internal analog supply voltage | external $C_{VDDA}$ connected, no sleep mode | $V_{VDDA}$ | 3.13 | 3.3 | 3.47 | V |
| Internal digital supply voltage | external $C_{VDDD}$ connected, no sleep mode | $V_{VDDD}$ | 3.0 | 3.3 | 3.6 | V |
| Power-on reset on threshold referred to $V_{VS}$ | $V_{VS}$ falling | $V_{TL,POR,VS}$ | | | 3.8 | |
| Power-on reset off threshold referred to $V_{VS}$ | $V_{VS}$ rising | $V_{TH,POR,VS}$ | | | 4.1 | |
| **Temperature Control** | | | | | | |
| High temperature threshold | $T_J$ rising [2] | $T_{OFF}$ | 155 | 165 | 175 | °C |
| Low temperature threshold | $T_J$ falling [2] | $T_{ON}$ | 135 | 145 | 155 | °C |
| **Oscillator** | | | | | | |
| Output frequency | | $f_{OSC}$ | 31 | 32 | 33 | MHz |
| Clock frequency for digital part | | $f_{CLK}$ | | 0.25 | | $f_{OSC}$ |
| Clock period for digital part | | $t_{CLK}$ | | $1/f_{CLK}$ | | |

1) VDDx means VDDD or VDDA, whichever reaches the threshold first.

2) Functionality of over-temperature shutoff is tested. Temperature thresholds are not tested in production.

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## Electrical Characteristics (continued)

($V_{VS}$ = +5.5V to +18V, $T_J$ = -40°C to +150°C, unless otherwise noted. Slew rate at pin VS < 1V/µs. Typical values are at $V_{VS}$ = +12V and $T_J$ = +25°C. Positive currents flow into the device pins.)

| Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LIN Transceiver ( according to LIN standard ) [1]** | | | | | | |
| **DC Characteristics of LIN Transceiver** | | | | | | |
| Current Limitation for Driver dominant state | $V_{BUS}$=18V | $I_{BUS\_LIM}$ Param12: 40-200mA) | 40 | 75 | 200 | mA |
| Input Leakage Current, at the Receiver incl. Pull-Up Resistor | transmitter passive, 7V<$V_{VS}$<18V, $V_{BUS}$=0V | $I_{BUS\_PAS\_dom}$ Param 13: min:-1mA for VS=12V | -1 | | | mA |
| Input Leakage Current, Driver Off | 7V<$V_{VS}$<18V [5] 7V<$V_{BUS}$<18V $V_{BUS}$≥$V_{VS}$ | $I_{BUS\_PAS\_rec}$ Param14: max:20µA for 8V..18V | | | 20 | µA |
| Input Leakage Current, Driver Off, under in typical conditions | V(LIN)=12V, VS=9-12V, Tjunct.< +50°C | $I_{BUS\_PAS\_rec\_50C}$ | | 6 | 12 | µA |
| Input Leakage current, control unit disconnected from GND | 12V ≤ $V_{VS}$ ≤ 13.5V, 0V < $V_{BUS}$< 18V | $I_{BUS\_NO\_GND}$ Param15: -1..1mA for $V_{Vs}$=12V | -1 | | 0.1 | mA |
| Leakage current, supply disconnected | $V_{VS}$=0V, 0V<$V_{BUS}$<18V [6] | $I_{BUS\_NO\_BAT}$ Param16: max 100µA | | | 10 | µA |
| Receiver dominant level | rising and falling edge | $V_{BUSdom}$ Param17: max : 0.4$V_{Vs}$ | | | 0.4 | $V_{VS}$ |
| Receiver recessive level | | $V_{BUSrec}$ Param18: min: 0.6$V_{Vs}$ | 0.6 | | | $V_{VS}$ |
| Center voltage | [2] | $V_{BUS\_CNT}$ Param19: 0.475-0.525$V_{Vs}$ | 0.475 | 0.5 | 0.525 | $V_{VS}$ |
| Threshold hysteresis voltage | [3] | $V_{HYS}$ Param20: max. 0.175$V_{Vs}$ | 0.03 | 0.05 | 0.175 | $V_{VS}$ |
| Pull-up resistance | $V_{BUS}$ = 0V [4] | $R_{slave}$ Param25: 20-60kOhm | 30 | - | 60 | kΩ |

*In sleep mode the pull-up is deactivated.*

*1) The IC is conform to the parameter limitations of the "LIN Physical Layer Spec. Revision 1.3" up to "LIN Physical Layer Spec. Revision 2.2A". In some parameters the IC provides better performance to meet the enhanced requirements of leading European OEMs.*

$$2) \quad V_{BUS\_CENTER} = \frac{V_{BUS\_THRES+} + V_{BUS\_THRES-}}{2}$$

$$3) \quad V_{BUS\_HYS} = V_{BUS\_THRES+} - V_{BUS\_THRES-}$$

*where $V_{BUS\_THRES+}$ : receiver threshold of the recessive to dominant bus edge and*
*$V_{BUS\_THRES-}$ : receiver threshold of the dominant to recessive bus edge.*

*4) In sleep or unpowered mode the pull-up is deactivated, due to special OEM requirements.*

*5) max.-limit valid for Tj≤85°C, for Tj≤25°C the limit is 10µA, for Tj≥85°C the limit is 40µA*

*6) max.-limit valid for Tj≤85°C, for Tj≤85°C the limit is 100µA*

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E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## Electrical Characteristics (continued)

($V_{VS}$ = +5.5V to +18V, $T_J$ = -40°C to +150°C, unless otherwise noted. Slew rate at pin VS < 1V/µs. Typical values are at $V_{VS}$ = +12V and $T_J$ = +25°C. Positive currents flow into the device pins.)

| Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Recessive output voltage with active pullup | $I_{BUS}$=0mA<br>Bus recessive | $V_{BUS\_REC}$ | $V_{VS}$-1V | | $V_{VS}$ | |
| Dominant output voltage | Bus dominant, $V_{VS}$=7.0V, $R_{BUS}$=0.5kΩ to $V_S$ | $V_{BUSDOM}$ | | 0.7 | 1.2 | V |
| Dominant output voltage | Bus dominant, $V_{VS}$=18V, $R_{BUS}$=0.5kΩ to $V_{VS}$ | $V_{BUSDOM}$ | | 1.1 | 2.0 | V |
| Leakage current, supply disconnected | V(LIN)=12V, VS=0V, Tjunct<50°C | $I_{BUS,50}$ | | 1 | 2 | µA |
| Clamping voltage, not production tested | $V_{VS}$=0V, $I_{BUS}$=1mA | $V_{BUS,CLAMP}$ | 42 | | | V |
| **LIN2.x Transceiver , AC Characteristics** | | | | | | |
| Input capacitance | 7V<$V_S$<18V | $C_{LIN,PIN}$ | | | 30 | pF |
| Output slew-rate | $C_{LIN}$=1-10nF, $R_{LIN}$=0.5-1kΩ, 1µs<$t_{LIN}$<5µs, $V_{VS}$=18V | $SR_{LIN,OUT}$ | 1 | | 3 | V/µs |
| Output slew-rate | $C_{LIN}$=1-10nF, $R_{LIN}$=0.5-1kΩ, 1µs<$t_{LIN}$<5µs, $V_{VS}$=7V | $SR_{LIN,OUT}$ | 0.5 | | 3 | V/µs |
| Symmetry of rising and falling edge | $V_{VS}$=18V [6] | $t_{LIN,SYM}$ | -5 | | 5 | µs |
| Transmit propagation delay | [6] | $t_{tx\_pdr}$ , $t_{tx\_pdf}$ | | | 4 | µs |
| Transmit propagation delay symmetry | $t_{tx\_sym}=t_{tx\_pdf}-t_{tx\_pdr}$ [6] | $t_{tx\_sym}$ | -2 | | 2 | µs |
| Propagation delay BUS to RXD | | $t_{rx\_pdr}$ , $t_{rx\_pdf}$ | | | 6 | µs |
| Propagation delay symmetry receiver | $t_{rx\_sym}=t_{rx\_pdf}-t_{rx\_pdr}$ | $t_{rx\_sym}$ | -2 | | 2 | µs |
| LIN bus pulse receiver debounce time | | $t_{LIN,DB}$ | 0.3 | | 6 | µs |
| Wake-up debounce time | | $t_{LIN,WU}$ | 70 | | 150 | µs |
| Duty cycle 1 | [1] [5]<br>$TH_{Rec(max)}$=0.744 *$V_{VS}$<br>$TH_{Dom(max)}$=0.581 *$V_{VS}$<br>7V ≤ $V_S$ ≤ 18V<br>$t_{Bit}$=50µs | D1 | | 0.396 | | |

1)  $D1 = \dfrac{t_{BUS\_REC(MIN)}}{2 * t_{Bit}}$    2)  $D2 = \dfrac{t_{BUS\_REC(MAX)}}{2 * t_{Bit}}$    3)  $D3 = \dfrac{t_{BUS\_REC(MIN)}}{2 * t_{Bit}}$    4)  $D4 = \dfrac{t_{BUS\_REC(MAX)}}{2 * t_{Bit}}$

5)  *LIN driver, bus load conditions (CBUS; RBUS): 1nF; 1kΩ / 6.8nF; 660Ω / 10nF; 500Ω*

6)  *This parameters are a documentation of LIN1.3 specification only and not valid for this product. Referring to the LIN2.2A-specification (extract see below) LIN2.2A transceivers are compatible to LIN1.3 without being confirm to this parameter limits.*
*LIN Specification Package Revision 2.2A December 31, 2010; Page 15*

***1.1.7.1 Compatibility with LIN 1.3***

*LIN 2.2 is a superset of LIN 1.3.......................The LIN 2.2 physical layer is backwards compatible with the LIN1.3 physical layer. But not the other way around. The LIN 2.2 physical layer sets  harder requirement, i.e. a node using the LIN 2.2 physical layer can operate in a LIN 1.3 cluster.*

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## Electrical Characteristics (continued)

($V_{VS}$ = +5.5V to +18V, $T_J$ = -40°C to +150°C, unless otherwise noted. Slew rate at pin VS < 1V/μs. Typical values are at $V_{VS}$ = +12V and $T_J$ = +25°C. Positive currents flow into the device pins.)

| Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Duty cycle 2 | [4) 7)] $TH_{Rec(min)}$=0.422 $*V_{VS}$ $TH_{Dom(min)}$=0.284 $*V_{VS}$ 7.6V ≤ $V_S$ ≤ 18V $t_{Bit}$=50μs | D2 | | | 0.581 | |
| Duty cycle 3 | [5) 7)] $TH_{Rec(max)}$=0.778 $*V_{VS}$ $TH_{Dom(max)}$=0.616 $*V_{VS}$ 7V ≤ $V_S$ ≤ 18V $t_{Bit}$=96μs | D3 | 0.417 | | | |
| Duty cycle 4 | [6) 7)] $TH_{Rec(min)}$=0.389 $*V_{VS}$ $TH_{Dom(min)}$=0.251 $*V_{VS}$ 7.6V ≤ $V_{VS}$ ≤ 18V $t_{Bit}$=96μs | D4 | | | 0.590 | |
| **Additional LIN Parameters** | | | | | | |
| Timeout for LIN dominant clamping failure (deactivated for PWM version) | | $t_{LIN,BUS,DOM}$ | | 12 | | ms |
| Baud rate for FLASH memory update via BUS | special mode to be activated via register, in send and receive mode | R | | 125 | | kB |
| **LIN auto-addressing ( only valid for products including this function )** | | | | | | |
| Bus pull-up current source for auto-addressing | 0°C<$T_J$<50°C $V_{BUS}$=0V | $I_{PD}$ | 1.84 | 2.050 | 2.26 | mA |
| Bus shunt resistor [2)] | 0°C<$T_J$<50°C | $R_{SHUNT}$ | 0.75 | 1.00 | 1.25 | Ω |
| Temperature coefficient of bus shunt resistor [1)] | 0°C<$T_J$<50°C | $TK_{SHUNT}$ | | 0.4 | | %/K |
| Differential amplifier differential input voltage range [3)] | 0°C<$T_J$<50°C | $V_{DIFF\_AMP}$ | -10 | | 30 | mV |
| Differential amplifier common mode input voltage range [3)] | 0°C<$T_J$<50°C | $V_{COM\_AMP}$ | 0.00 | | 2.50 | V |
| Differential amplifier gain [2)] | 0°C<$T_J$<50°C 0V<$V_{BUS}$<2.5V | $A_{DIFF}$ | 65 | 70 | 74 | 1 |

*Note)*   *The auto-addressing parameters are valid only under the following conditions:*

*Ground shift: DC ≤ 0.45V, AC ≤ 100mV for f<1kHz*

*Noise ≤ 250μV for a bandwidth less than f<1kHz*

$V_{BUSDOM\_MASTER\_MIN}$=0.60V therefore $V_{BUS\_INPUT\_SLAVE}$ *is always positive: 0.60V - 0.45V (max. ground shift) = 0.15V*

1)  Not tested in production.
2)  Total gain of auto-addressing path is tested through digital ADC output.
3)  Operation outside of common mode and/or differential input voltage range will not result in damage, but will produce invalid results on the differential amplifier's output.

4)   $D2 = \dfrac{t_{BUS\_REC(MAX)}}{2 * t_{Bit}}$      5)   $D3 = \dfrac{t_{BUS\_REC(MIN)}}{2 * t_{Bit}}$      6)   $D4 = \dfrac{t_{BUS\_REC(MAX)}}{2 * t_{Bit}}$

7)  LIN driver, bus load conditions (CBUS; RBUS): 1nF; 1kΩ / 6.8nF; 660Ω / 10nF; 500Ω

## Electrical Characteristics (continued)

($V_{VS}$ = +5.5V to +18V, $T_J$ = -40°C to +150°C, unless otherwise noted. Slew rate at pin VS < 1V/μs. Typical values are at $V_{VS}$ = +12V and $T_J$ = +25°C. Positive currents flow into the device pins.)

| Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Hall Sensor or Potentiometer Input** | | | | | | |
| Low level input threshold D1, D2, D3 | | $V_{TL,DIG}$ | 0.7 | | - | V |
| High level input threshold D1, D2, D3 | | $V_{TH,DIG}$ | - | | 2.1 | V |
| Hysteresis D1, D2, D3 | | $V_{HYS,DIG}$ | 0.2 | | 1.4 | V |
| Low output level D1, D2, D3 | $I_{Dx}$ = +3.0mA [1] | $V_{OL,DIG}$ | | | 0.8 | V |
| High output level D1, D2, D3 | $I_{Dx}$ = -3.0mA [1] | $V_{OH,DIG}$ | 4.2 | | | V |
| Pull-up current D1, D2, D3 | $0<V_{IN}<V_{TH,DIG}$ [2] | $I_{PU}$ | -50 | | -25 | μA |
| Pull-down current D1, D2, D3 | $V_{V5V}>V_{IN}>V_{TL,DIG}$ [2] | $I_{PD}$ | 25 | | 50 | μA |
| **ADC and Input Multiplexer** | | | | | | |
| Supply voltage division factor | | $G_{VS\_ADC}$ | 11.75 | 12 | 12.25 | |
| Temperature zero point | | $K_0$ | | 107.2 | | LSB |
| Temperature coefficient | | $G_T$ | | -3.16 | | °C/LSB |
| On-chip temperature measurement error | | $T_{ERR}$ | -15 | | 15 | °C |
| Reference Low voltage | | $V_{REFL}$ | | $V_{GNDA}$ | | V |
| Reference High voltage | | $V_{REFH}$ | | $V_{VDDA}$ | | V |
| Resolution | | N | | 8 | | bit |
| Conversion time | | $t_{CONV}$ | | 21 | | $t_{CLK}$ |
| Conversion time during LIN auto-addressing | | $t_{CONV,AA}$ | | 171 | | $t_{CLK}$ |
| Differential non-linearity | | DNL | | 0.9 | | LSB |
| Integral non-linearity | | INL | | 0.9 | | LSB |
| Missing codes | | MC | | 0 | | LSB |
| Offset error | | $ERROR_{OFFSET}$ | -0.5 | | 0.5 | LSB |
| Gain error | | $ERROR_{GAIN}$ | -0.5 | | 0.5 | LSB |
| Total unadjusted error | | $ERROR_{TOTAL}$ | -2 | | 2 | LSB |
| **Half Bridge Drivers** | | | | | | |
| High leakage current of both half bridges together | Half bridge off $I_{PD}$ switched off $V_{A/Bx}=V_{VS}$ $V_{VS},V_{VSPx}<14V$ $T_{amb}<85°C$ | $I_{LEAKH}$ | -10 | | 10 | μA |
| Low leakage current of both half bridges together | Half bridge off $I_{PD}$ switched off $V_{A/Bx}=0V$ $V_{VS},V_{VSPx}<14V$ $T_{amb}<85°C$ | $I_{LEAKL}$ | -10 | | 10 | μA |

1) Dx means D1, D2 or D3. Dx is configured as digital output.
2) Pull-up, pull-down or high resistive is configurable by software. Dx is configured as digital output.

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## Electrical Characteristics (continued)

($V_{VS}$ = +5.5V to +18V, $T_J$ = -40°C to +150°C, unless otherwise noted. Slew rate at pin VS < 1V/μs. Typical values are at $V_{VS}$ = +12V and $T_J$ = +25°C. Positive currents flow into the device pins.)

| Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| A/B coil current threshold range 1 | IDACx = 0xFF | $I_{TH,MAX1}$ | 720 | 800 | 880 | mA |
| A/B coil current threshold range 2 | IDACx = 0xFF | $I_{TH,MAX2}$ | 540 | 600 | 660 | mA |
| A/B coil current threshold range 3 | IDACx = 0xFF | $I_{TH,MAX3}$ | 270 | 300 | 330 | mA |
| Chopper current error | $T_{amb}$<85°C | $\Delta I_{nom}$ | -10 | | 10 | % |
| A/B coil current mismatch range 1 | IDACx = 0xFF | $I_{THDIFFAB1}$ | -6 | | +6 | % |
| A/B coil current mismatch range 1 | IDACx = 0xFF | $I_{THDIFFAB2}$ | -6 | | +6 | % |
| A/B coil current mismatch range 1 | IDACx = 0xFF | $I_{THDIFFAB3}$ | -6 | | +6 | % |
| A/B coil current mismatch range 1 | IDACx = 0xFF 12V<$V_{VS}$<14V -20°C<$T_J$<85°C | $I_{THDIFFAB,R1}$ | -5% | | +5% | % |
| A/B coil current mismatch range 2 | IDACx = 0xFF 12V<$V_{VS}$<14V -20°C<$T_J$<85°C | $I_{THDIFFAB,R2}$ | -5% | | +5% | % |
| A/B coil current mismatch range 3 | IDACx = 0xFF 12V<$V_{VS}$<14V -20°C<$T_J$<85°C | $I_{THDIFFAB,R3}$ | -5% | | +5% | % |
| Chopper current comparator propagation delay | | $t_{CC-DEL}$ | | 250 | | ns |
| Half bridge high side on resistance | $I_{LOAD}$=-600mA $V_{VS},V_{VSPx}$=13.5V $T_J$=50°C | $R_{ONH13RT}$ | | 450 | 550 | mΩ |
| Half bridge high side on resistance | $I_{LOAD}$=-600mA $V_{VS},V_{VSPx}$=13.5V $T_J$=150°C | $R_{ONH13HT}$ | | 650 | 750 | mΩ |
| Half bridge high side on resistance | $I_{LOAD}$=-600mA $V_{VS},V_{VSPx}$=8V $T_J$=50°C | $R_{ONH8RT}$ | | 500 | 600 | mΩ |
| Half bridge high side on resistance | $I_{LOAD}$=-600mA $V_{VS},V_{VSPx}$=8V $T_J$=150°C | $R_{ONH8HT}$ | | 800 | 950 | mΩ |
| Half bridge low side on resistance | $I_{LOAD}$=600mA $V_{VS},V_{VSPx}$=13.5V $T_J$=50°C | $R_{ONL13RT}$ | | 550 | 650 | mΩ |
| Half bridge low side on resistance | $I_{LOAD}$=600mA $V_{VS},V_{VSPx}$=13.5V $T_J$=150°C | $R_{ONL13HT}$ | | 950 | 1050 | mΩ |
| Half bridge low side on resistance | $I_{LOAD}$=600mA $V_{VS},V_{VSPx}$=8V $T_J$=50°C | $R_{ONL8RT}$ | | 700 | 800 | mΩ |
| Half bridge low side on resistance | $I_{LOAD}$=600mA $V_{VS},V_{VSPx}$=8V $T_J$=150°C | $R_{ONL8HT}$ | | 1150 | 1250 | mΩ |
| Reverse diode voltage | $I_{DIODE}$=600mA $T_{amb}$=25°C | $V_{DIODE}$ | | 0.9 | | V |

1) *Not tested in production.*

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E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## Electrical Characteristics (continued)

($V_{VS}$ = +5.5V to +18V, $T_J$ = -40°C to +150°C, unless otherwise noted. Slew rate at pin VS < 1V/µs. Typical values are at $V_{VS}$ = +12V and $T_J$ = +25°C. Positive currents flow into the device pins.)

| Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Half bridge pull-down current | Half bridge off $V_{A/Bx}=V_{VS}=V_{VSPx}$ | $I_{PD}$ | 20 | 60 | 100 | µA |
| Slew-rate of driver | Rising edge $I_{LOAD}>0$ SLEW[1:0]=10$_b$ | $SR_{R10}$ | | 70 | | V/µs |
| Slew-rate of driver | Falling edge $I_{LOAD}>0$ SLEW[1:0]=10$_b$ | $SR_{F10}$ | | -70 | | V/µs |
| Slew-rate of driver | Rising edge $I_{LOAD}>0$ SLEW[1:0]=11$_b$ | $SR_{R11}$ | | 110 | | V/µs |
| Slew-rate of driver | Falling edge $I_{LOAD}>0$ SLEW[1:0]=11$_b$ | $SR_{F11}$ | | -110 | | V/µs |
| Propagation delay digital signal to driver pin | | $t_{DEL}$ | | 1 | | µs |
| Zero Crossing Comparator Offset Voltage | | $V_{ZC\_OFF}$ | -150 | | 150 | mV |
| Zero Crossing Comparator common mode range | | $V_{ZC\_CM}$ | -0.1 | | 2.5 | V |
| Zero Crossing Comparator propagation delay | | $t_{ZC-DEL}$ | - | 410 | - | ns |
| **Motor Control** | | | | | | |
| PWM frequency | | $f_{PWM}$ | 20 | 23.8 | | kHz |
| PWM period | | $t_{PWM}$ | | $1/f_{PWM}$ | | |
| PWM step resolution | | $t_{PWM,RES}$ | | $2/f_{CLK}$ | | |
| Current comparator mask | adjustable | $t_{MASK}$ | 5 | | 24 | $t_{CLK}$ |
| **JTAG Interface** | | | | | | |
| Pull-down resistance at pins TSTEN, TCK, TDI, TMS and TSTRST | | $R_{PD}$ | 90 | 125 | 160 | kΩ |
| Output voltage at TDO for 'low' logic level | $I_{TDO}$=1.5mA JTAG access | $V_{TDO,LOW}$ | 0 | | 0.8 | V |
| Output voltage at TDO for 'high' logic level | $I_{TDO}$=-1.5mA JTAG access | $V_{TDO,HIGH}$ | $V_{VDDD}$-0.8 | | $V_{VDDD}$ | V |
| **EEPROM** | | | | | | |
| Memory size | | $N_{EEPROM}$ | | 64 | | Byte |
| Data retention time (1) | $T_J$<85°C | $t_{RET}$ | 10 | | | a |
| Data retention time 1) | $T_J$<150°C | $t_{RET}$ | 1 | | | a |
| Programming cycles 1) | $T_J$<85° | $N_{END}$ | $10^5$ | | | |
| Programming cycles 1) | $T_J$<125° | $N_{END}$ | $10^4$ | | | |
| Wake-up time | | $t_{WAKEUP,EE}$ | | 50 | | µs |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## Electrical Characteristics (continued)

($V_{VS}$ = +5.5V to +18V, $T_J$ = -40°C to +150°C, unless otherwise noted. Slew rate at pin VS < 1V/µs. Typical values are at $V_{VS}$ = +12V and $T_J$ = +25°C. Positive currents flow into the device pins.)

| Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **FLASH ( only in products with FLASH memory )** | | | | | | |
| Memory size for E523.30 FLASH version | | $N_{FLASH\_8k}$ | | 8 | | k Byte |
| Data retention biased: operating life ( IC powered up, operating mode) | $T_J$= -40..150°C $N_{CYC}$=1 | $t_{OP}$ | 10000 | | | h |
| Data retention biased: operating life ( IC powered up, operating mode) | $T_J$= -40..150°C $N_{CYC}$=100 | $t_{OP}$ | 5500 | | | h |
| Data retention unbiased, unpowered or sleep mode | $T_J$= -40..85°C | $t_{STOR}$ | 87600 | | | h |
| Data retention unbiased, unpowered or sleep mode | $T_J$= 125°C | $t_{STOR}$ | 10800 | | | h |
| Data retention unbiased, unpowered or sleep mode | $T_J$= 150°C | $t_{STOR}$ | 1000 | | | h |
| Programming cycles | $T_J$<85°C $t_{OP}$ < 120h | $N_{END}$ | 10000 | | | |
| Wake-up time | | $t_{WAKEUP,FL}$ | | 20 | | µs |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## 5 Typical Operating Characteristics

| | |
|---|---|
| VS+VSPA+VSPB sleep mode current at +13.5V depending on temperature (-40 .. +170°C) (with VCC connected to GND ) | VS+VSPA+VSPB sleep mode current depending on voltage (5-28V) at T= 50°C (with VCC connected to GND ) |
| VS+VSPA+VSPB sleep mode current and V(LIN) ramp 0V>13V>0V over time at T= 50°, VS=13V | VCC depending on VS (5-28V) with I(VCC = 10mA |
| RON via Temp . (-40 .. +170°C) | Temperature Sensor Voltage after ADC (-40 .. +170°C) |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

# 6 Functional Description

## 6.1 Chip Control

## 6.2 Internal Supply Voltage for Analog and Digital Parts

The analog and digital 3.3V regulators are supplied by the external supply voltage VS. An internal short circuit protection prevents the device from damage. Each internal supply voltage requires an external blocking capacitor. It is recommended to place the external capacitors as close as possible to the related pins. During sleep mode the regulators are deactivated.

The analog regulator is not intended to supply any external components, except for potentiometers at the input pins D1..D3 if the analog capability of the GPIO interface is selected.

The digital regulator is not intended to supply any external components.

An internal pre-regulator provides the supply voltage for the LIN receiver and the wake-up logic during sleep mode.

## 6.3 Hall-Sensor Supply

The Hall-sensor supply voltage requires an external blocking capacitor. An internal short circuit protection prevents the device from damage. During sleep mode V5V is deactivated. When leaving the sleep mode, the Hall-sensor supply pin V5V is inactive and has to be turned on explicitly by writing into the μC register GPIO Control Register during running mode.

## 6.4 Power-On Reset

The power-on reset depends on the internal 3.3V supply voltages $V_{VDDD}$, $V_{VDDA}$ and the pre-regulator resets. The internal reset signal is set when at least one of these 3.3V supply voltages reaches the corresponding threshold level and is cleared, if all internal voltages are available. After power-on-reset the device is in active mode ( μcontroller supply on) and all drivers off .

There is no hardware supply monitoring for the supply voltage VVS in the case of its under-voltage or over-voltage. If under-voltage or over-voltage at VS occurs, necessary actions (e.g. disabling the H4 half bridges) have to be conducted by software. In case of an under-voltage event at the 3.3V supplies the CPU is shut down and the device goes in sleep mode, so no software counter measure can be taken. The device is in sleep mode until a LIN-wake-up or a power-on reset takes place. In this case the drivers are set to high-impedance state by hardware. The thresholds for power-on reset and an example of software driver shutdown are shown at the figure below. In case of a power-up or after an under-voltage situation with a reset condition, the device wakes up.
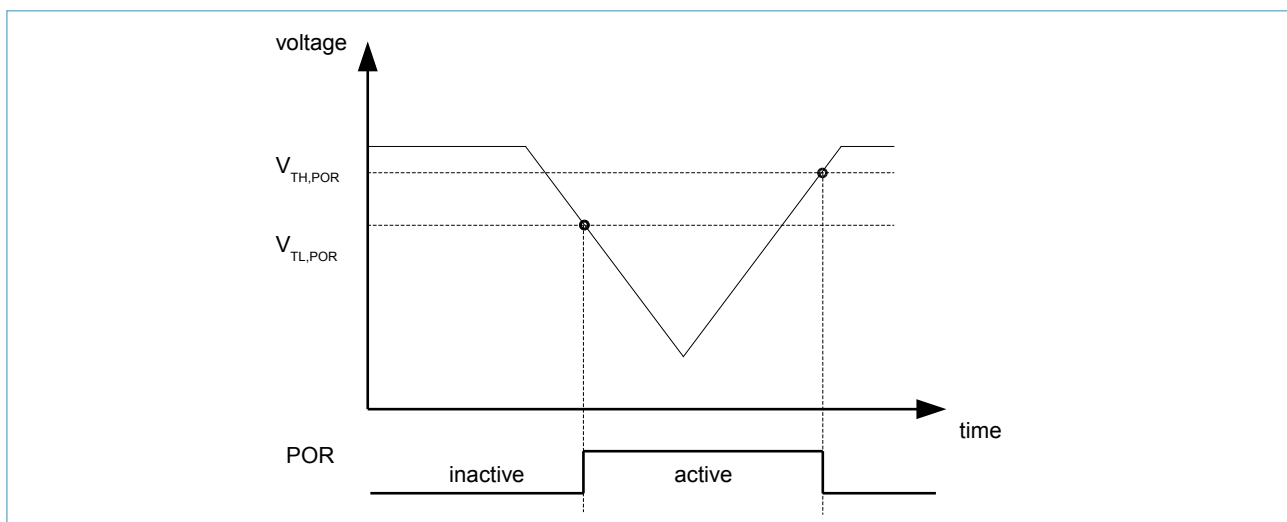


*Figure 1. Under-voltage/Over-voltage Detection and POR Timing Diagram*

## 6.5 Wake-up

The IC will automatically wake-up after power-up or after under-voltage conditions and features a remote wake-up from sleep-mode via the LIN interface. A falling edge at the LIN bus followed by a dominant bus level maintained for a time period $t_{LIN,WU}$ and a rising edge on the LIN bus results in a remote wake-up. After wake-up it is possible to evaluate the reason for the last sleep situation, by examining the RESSTAT register. The following events affect the RESSTAT register.

- Power-up:
  - all bits cleared, except for the under-voltage identifier, which can be read out via µC..

- VDDA or VDDD under-voltage:
  - digital part is reset,
  - none of the identifiers is modified
- Watchdog or LIN timeout:
  - digital part is reset,
  - watchdog identifier can be read out via µC.
- Over-temperature:
  - no reset or sleep mode initialized,
  - IC remains alive, only drivers are disabled,
  - over-temperature identifier can be read out via µC.
- µC sleep mode:
  - µC sleep mode identifier can be read out via µC.

*Note: To detect a reset at VDDA/VDDD the precondition is, that the software has to clear the UV bit. After a new reset the UV bit displays '1' if the reset was forced by pre-regulator undervoltage (i.e. VS power-on). If the reset was forced by VDDA/VDDD undervoltage, then no change occurs in the status bits.*

Table 1. Reset Status Register Table

| Register Name | Address | Description |
|---|---|---|
| RESSTAT | 0x0408 | Reset Status Register |

Table 2. Reset Status Register

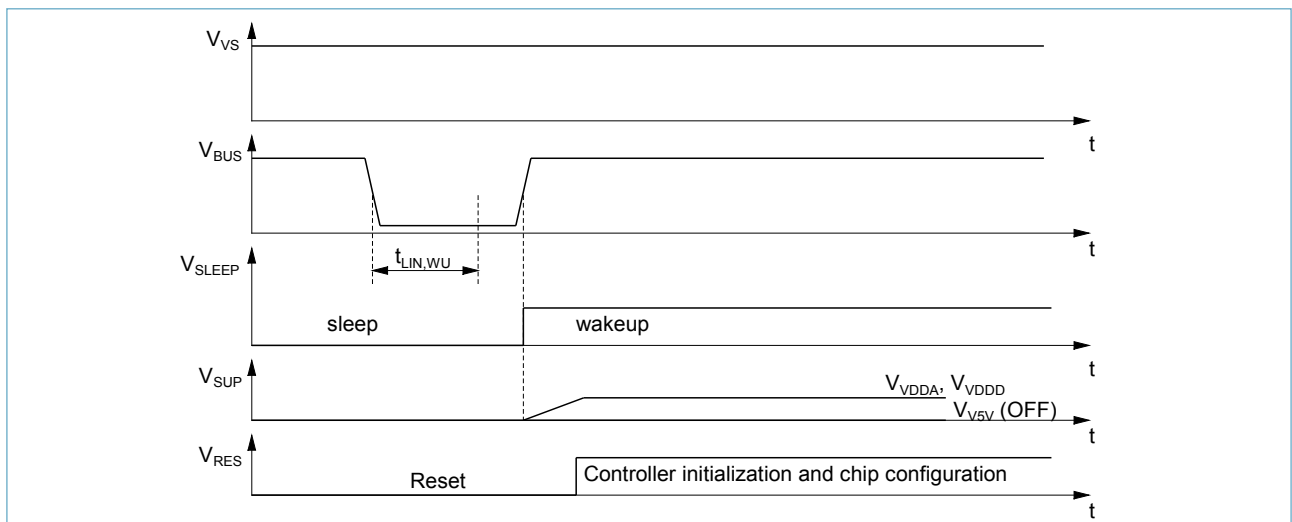| RESSTAT | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | CLR | - | - | - | WD | SLP | OT | UV |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Internal access | | | | | | | | |
| External access | R/W | R | R | R | R | R | R | R |
| Bit Description | **CLR** : $1_b$ : Clears the reset status bits<br>**WD** : $1_b$ : Watchdog or LIN timeout forced reset<br>**SLP** : $1_b$ : µC sleep mode forced reset<br>**OT** : $1_b$ : Overtemperature event occurred<br>**UVN** : $1_b$ : Preregulator undervoltage event (VS power-on) forced reset | | | | | | | |



*Figure 2.   Wake-up via BUS Timing Diagram*

## 6.6 Sleep Mode

The sleep mode may be initialized via software register (Table 3 General Configuration Register Table) access or during an under-voltage situation with a reset condition. When entering the sleep mode the following actions are applied:

- deactivating all driver outputs,
- resetting of registers,
- deactivating all circuit parts not needed in sleep mode to minimize sleep current consumption,
- deactivating the V5V regulator (Hall-sensor supply),
- deactivating LIN pullup

The sleep mode current of the device will not rise even in the case of slowly floating bus levels.
The following test criteria according to the "Klima-Arbeitskreis" are met:

1. $V_{BUS}$=13V; wait for 1min; check sleep mode current
2. step down $V_{BUS}$ by 1V; wait for 1min; check sleep mode current
3. do 2. until $V_{BUS}$= 0V
4. step up $V_{BUS}$ by 1V; wait for 1min; check sleep mode current
5. do 4. until $V_{BUS}$=13V

General configurations of the processor periphery have to be made by setting up the GENCFG register. The sleep mode is also activated via GENCFG. As a result of the sleep mode activation, the processor is reset, the control hardware is reset and the supplies are set in power down. A restart is only possible with a wake-up pulse on the BUS pin.

Table 3. General Configuration Register Table

| Register Name | Address | Description |
|---|---|---|
| GENCFG | 0x0401 | General Configuration Register |

Table 4. General Configuration Register

| GENCFG | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | SLEEP | - | - | - | - | - | LOWEMC | BSWT |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R | R | R | R | R | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **SLEEP** : $1_b$ : activates sleep mode<br>**LOWEMC** : $1_b$ : activates spread-spectrum clock (least-significant oscillator adjust bit is toggled with driver PWM frame frequency, that is approx. 150kHz FSK with 12kHz modulation frequency)<br>**BSWT** : $0_b$ : LIN2.1 mode<br>$1_b$ : PWM interface mode | | | | | | | |

## 6.7 Temperature Control

The IC has an on-chip temperature sensing. The temperature value can be read out by the integrated µC via the integrated ADC. Additionally to this feature, the voltage threshold of the over-temperature detection can be read out via ADC, too. It is possible to implement a temperature warning threshold at system level to reduce the power dissipation, if necessary. Furthermore the IC generates an over-temperature signal to shut off the half bridge driver and Hall-supply. For the reaction to over-temperature please refer to the following status table.

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## 6.8 Status Table

Hardware reaction is defined for the following cases:

Table 5. Status Table

| Event | Reset | Active or Sleep mode | V5V supply | Motor drivers |
|---|---|---|---|---|
| Power-on | Yes | Active-Mode | Off | Off |
| Wake-up | Yes | Active-Mode | Off | Off |
| Over-temperature | No | Active-Mode | Off | Off |
| Watchdog or LIN timeout | Yes | Active-Mode | Off | Off |
| Half bridge short circuit | No | Active-Mode | No change | System-level action only |
| µP initiates sleep mode | Yes | Sleep-Mode | Off | Off |

## 6.9 Oscillator

The IC has an on-chip 32Mhz oscillator. The digital circuitry is clocked with 8MHz. For the motor - PWM generation a frequency jitter is selectable via register LOWEMC.

It is possible to activate a spread-spectrum clock (least-significant oscillator adjust bit is toggled with driver PWM frame frequency, that is approx. 150kHz FSK with 24kHz modulation frequency)

Table 6. General Configuration Register Table

| Register Name | Address | Description |
|---|---|---|
| GENCFG | 0x0401 | General Configuration Register |

Table 7. General Configuration Register

| GENCFG | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | SLEEP | - | - | - | - | - | LOWEMC | BSWT |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **SLEEP** : see chapter Sleep-mode<br>**LOWEMC** : $1_b$ : activates spread-spectrum clock (least-significant oscillator adjust bit is toggled with driver PWM frame frequency, that is approx. 150kHz FSK with 24kHz modulation frequency)<br>**BSWT** : see chapters LIN and PWM interface | | | | | | | |

## 6.10 PWM interface (Receiving PWM Data)

The bus PWM interface can be used to receive position or speed requirements from an external PWM interface master. The bus PWM interface uses an internal frequency with 8 bit resolution. The PWM Input Interface can be configured by setting the PWMFREQ status bit in then PWMCFG Register (Table 13 BUS PWM Configuration Register Table) with a sampling clock of 500kHz. Otherwise the sampling clock is set to 250kHz (with a processor clock of 8MHz).
The registers are updated after equidistant time steps:
250kHz • 256 = 1.024ms or
500kHz • 256 = 0.512ms
These PWMLH and PWMHL registers contain the relative time values of edge events at BUS / RXD of the previous sample period. The value "255" means, that no proper edge was found. To signalize the availability of new register values, an interrupt is generated. If the controller does not read the register values within the given time slot, the old values will be overwritten by the new ones.

The sampling clock is not depending on the PWM frequency of the interface. So, with slow PWM interfaces it may take a number of readouts by the IC to be able to calculate the information, which is transferred by the PWM interface. The advantage of this "open" solution is, that the controller is able to analyze even special PWM codings with additional information hidden inside the cycle.
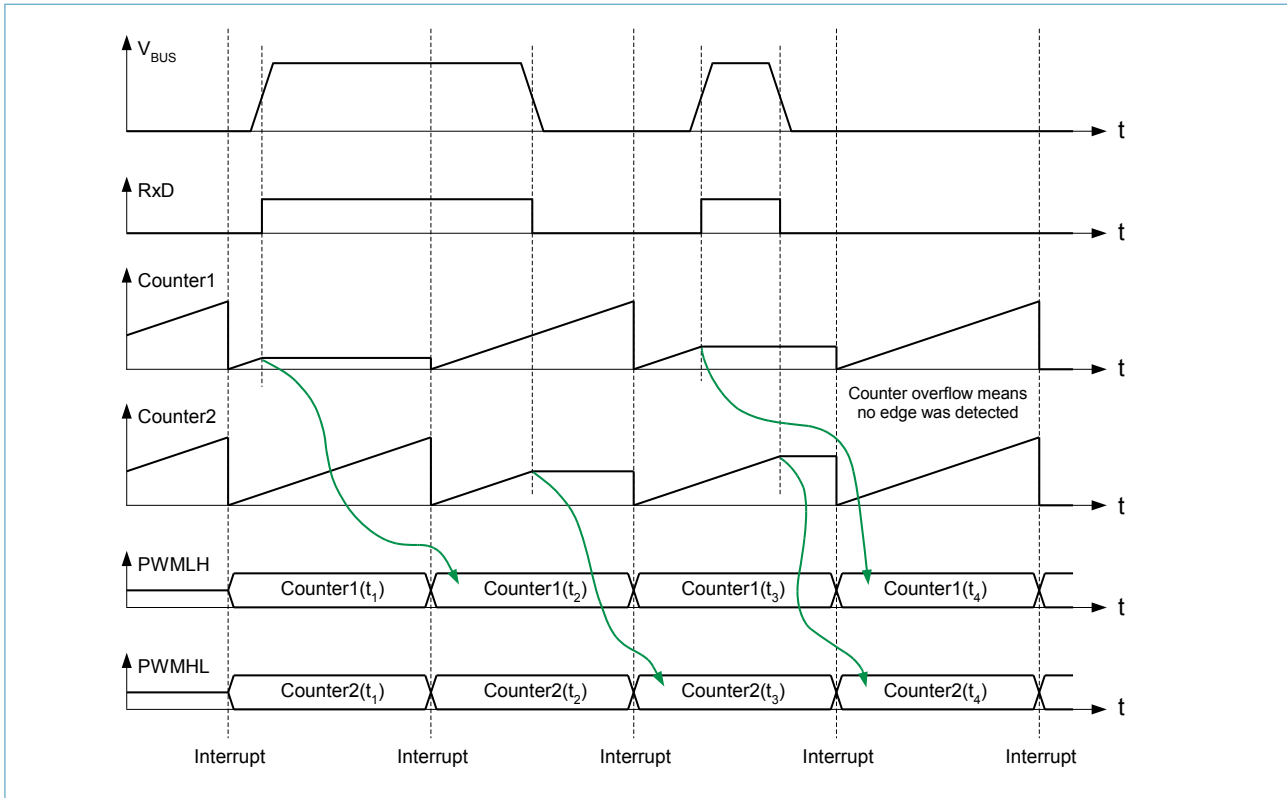
*Figure 3.   PWM Flow*

Table 8.  BUS PWM Control Register Table

| Register Name | Address | Description |
|---|---|---|
| PWMCTRL | 0x000C | PWM Control Register |

Table 9.  PWM Control Register

| PWMCTRL | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | - | - | - | - | IRQ_EN | IRQ_CLR | IRQ | TXD |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Internal access | R | R | R | R | R/W | R/W | R | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **IRQ_EN** : IRQ Mask Bit<br>1 : IRQ is unmasked<br>0 : IRQ is masked<br>**IRQ_CLR** : IRQ Clear Bit(is automatically reset to '0')<br>1 : clears the actually pending IRQ<br>(Note: should be set in ISR and before iret)<br>0 : <none><br>**IRQ** : IRQ Pending Bit<br>1 : An IRQ is pending<br>0 : No IRQ is pending<br>**TXD** : CPU access to BUS:<br>0 : bus dominant<br>1 : bus recessive | | | | | | | |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Table 10.  BUS PWM Position Register Table

| Register Name | Address | Description |
|---|---|---|
| PWMLH | 0x000A | BUS PWM Rising Edge Position Register |
| PWMHL | 0x000B | PWM Falling Edge Position Register |

Table 11.  BUS PWM Rising Edge Position Register

| PWMLH | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | PWM-LH[7..0] | PWM-LH[7..0] | PWM-LH[7..0] | PWM-LH[7..0] | PWM-LH[7..0] | PWM-LH[7..0] | PWM-LH[7..0] | PWM-LH[7..0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R | R | R | R | R | R | R | R |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | | | | | | | | |

Table 12.  PWM Falling Edge Position Register

| PWMHL | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | PWM-HL[7..0] | PWM-HL[7..0] | PWM-HL[7..0] | PWM-HL[7..0] | PWM-HL[7..0] | PWM-HL[7..0] | PWM-HL[7..0] | PWM-HL[7..0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R | R | R | R | R | R | R |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | | | | | | | | |

Table 13.  BUS PWM Configuration Register Table

| Register Name | Address | Description |
|---|---|---|
| PWMCFG | 0x0402 | BUS PWM Configuration Register |

Table 14.  BUS PWM Configuration Register

| PWMCTRL | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | - | - | - | - | - | - | - | PWMFREQ |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R | R | R | R | R | R | R | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **PWMFREQ** : PWMCFG[0]<br>0 : sample frequency = 250kHz<br>1 : sample frequency = 500kHz | | | | | | | |

**Transmitting Data**

By writing the TXD register bit, the pin BUS can be directly activated by the controller. The "LIN TXD Time Out" functionality is deactivated when the pin BUS is set to PWM interface mode.

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## 6.11 LIN interface ( only for products with LIN interface )

The bus interface can be either set to LIN mode or to PWM interface-mode by configuring the bit BSWT of GENCFG register (Table 16 General Configuration Register). This setup should be done directly after µC start (after power-up or reset condition). The LIN pull-up resistor can be activated or deactivated by setting of the bit ON30K in the LINAA register (Table 30 LIN Auto-addressing Register). In sleep mode the pull-up is deactivated. The pullup is activated automatically after wake-up.

Table 15.   General Configuration Register Table

| Register Name | Address | Description |
|---|---|---|
| GENCFG | 0x0401 | General Configuration Register |

Table 16.   General Configuration Register

| GENCFG | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | SLEEP | - | - | - | - | - | LOWEMC | BSWT |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **SLEEP** : see chapter Sleep-mode<br>**LOWEMC** : see chapter oscillator<br>**BSWT** : $0_b$ : LIN mode<br>$\quad\quad\quad 1_b$ : PWM mode | | | | | | | |

The LIN communication module consists of:
- LIN receiver with a capability of speed up to 125 kbit/s,
- LIN transmitter with a capability of speed up to 125 kbit/s,
- LIN-UART : SCI interface (Serial Communication Interface)
- Auto-addressing.
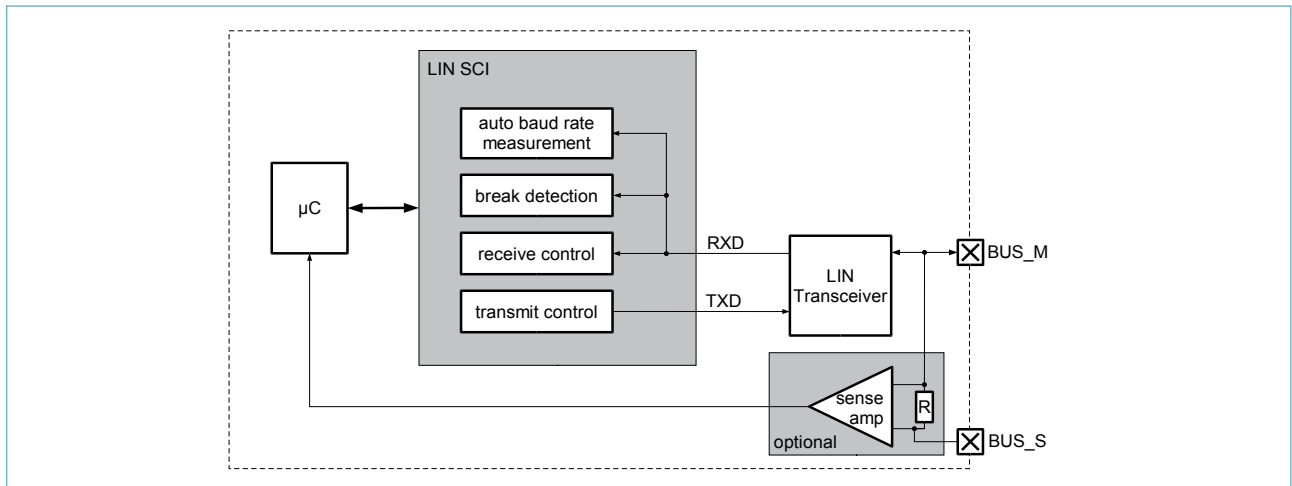


*Figure 4.   Block diagram of LIN SCI*

The parameters of the following bus timing diagram are specified in section LIN Transceiver.
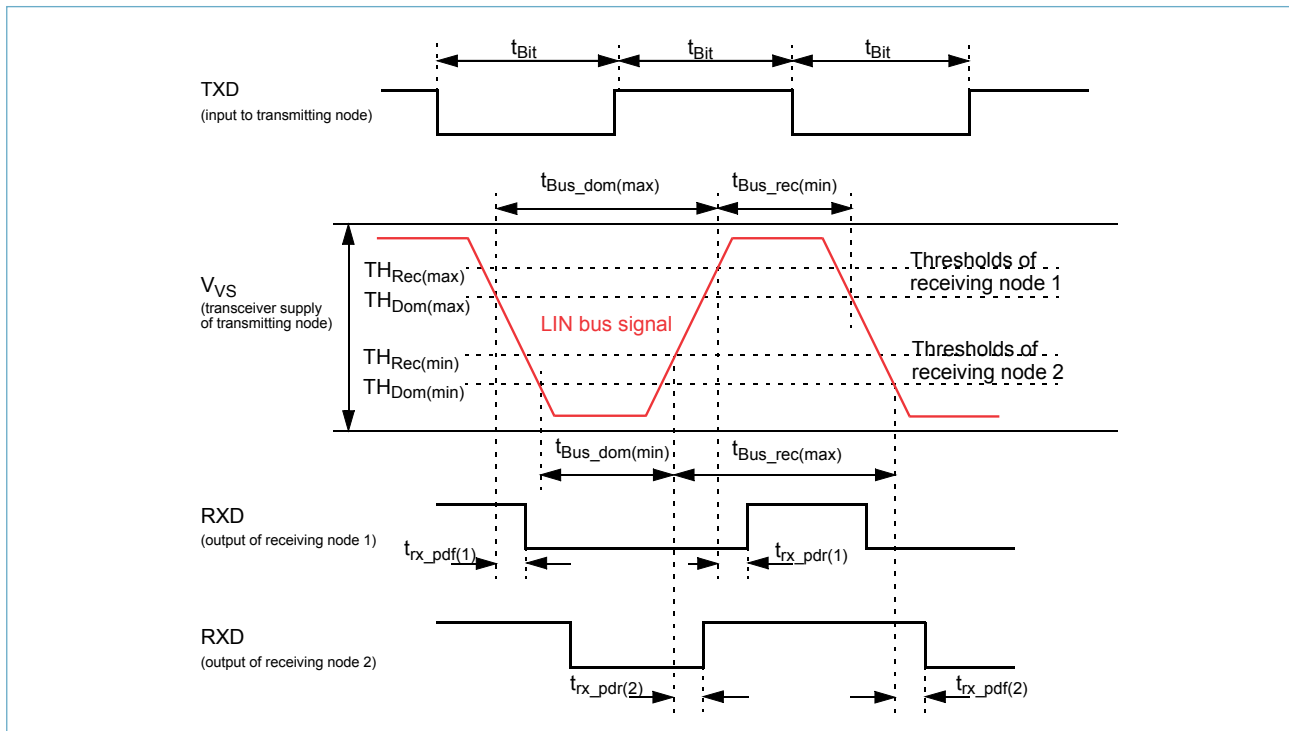


*Figure 5. LIN Timing*

## 6.12 LIN Receiver

The LIN transceiver consists of a receiver and a transmitter. The figure below shows a block diagram of the receiver.
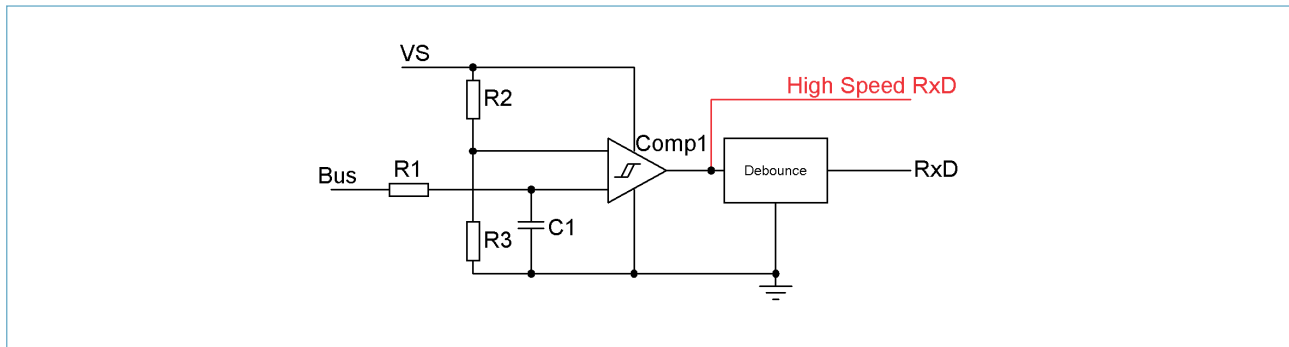


*Figure 6. Block Diagram of the LIN Receiver*

The low-pass filter at the input filters out high frequency components and assures faultless communication even under severe RF conditions. The reference voltage of the comparator is derived from the supply voltage. This way a duty cycle close to 50% is achieved under all supply conditions. The debounce filter is chosen so, that the digital SCI receives a signal without any spikes. This ensures a good decoding of the received data even in a harsh automotive environment. The debounce filter is bypassed in 125kbit/s high-speed LIN mode.

## 6.13  LIN Transmitter

The transmitter is slew-rate controlled through the feedback capacitor C1 to minimize electrical noise on the bus line. Both negative and positive edges are regulated. Due to the construction, a positive edge is only controlled by the device when the slew-rate is higher that the time constant on the bus pin (capacitance and wiring of all nodes connected to the bus).

The output stage is protected against short circuit to VVS with a current limiting circuit. To protect the device against loss of ground the diode D2 is included. This minimizes the disturbing current on the bus lines when the ground line is broken. The recessive output voltage is defined by the diode D1 and the pull up resistance. The dominant voltage is generated through M1 and D2.

A block diagram of the transmitter circuit is shown in figure below.
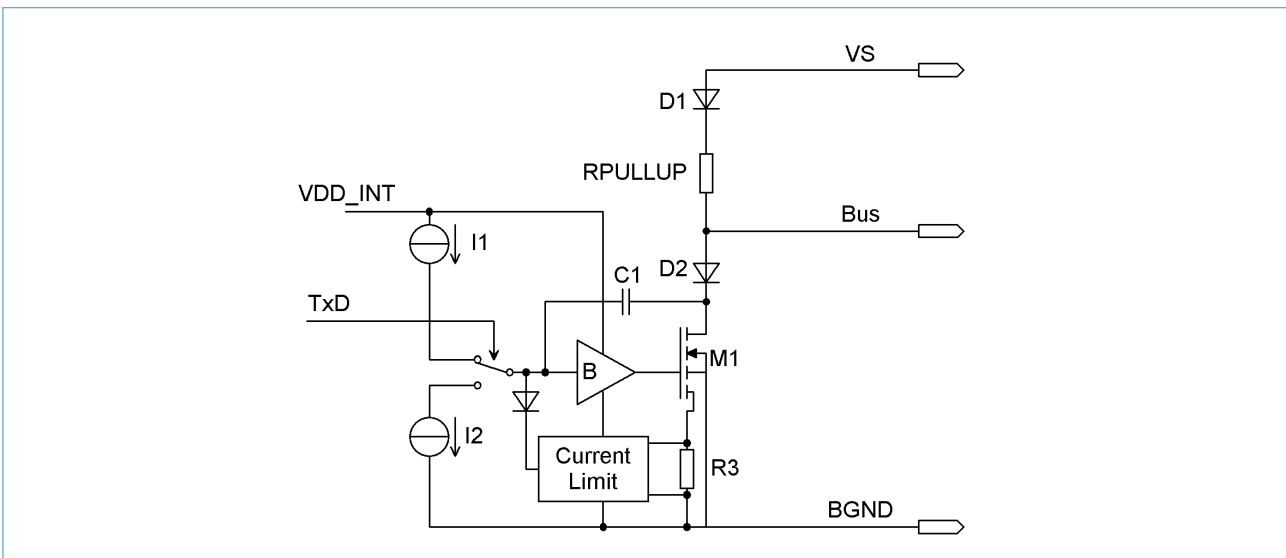


*Figure 7.   Block Diagram of the LIN Transmitter*

**TXD Timeout Functionality**

If the TXD signal is dominant for the time $t > t_{LIN,BUS,DOM}$ the device gets an internal reset. This implies that the TXD signal switches to a recessive level and further this prevents the LIN bus being blocked by a dominant

level. In the initial state of the device the TXD Timeout Functionality is enabled. But it can be disabled anytime by setting the TXD_TO_DIS-Bit in the LIN_MODE register (Table 18 LIN Mode Configuration Register)
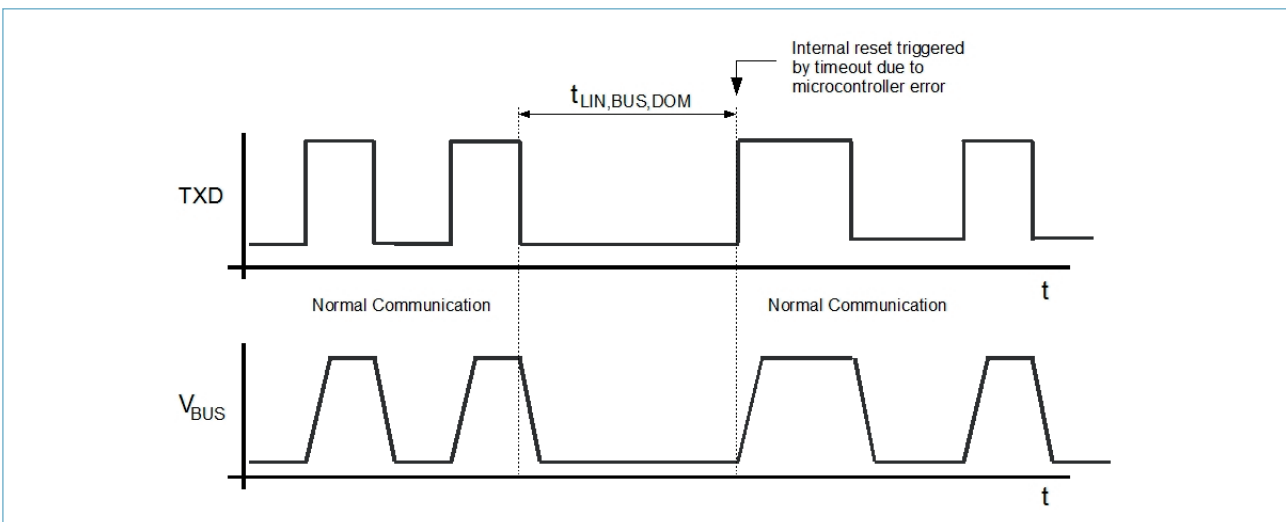


*Figure 8.   TXD Timeout*

## 6.14 LIN-UART / LIN- SCI   Controlling the LIN-Interface

Features of LIN SCI:
• Full duplex operation
• 8N1 data format, standard mark/space NRZ format
• extended baud rate selection options
• Interrupt-driven operation with four flags:
    1. receiver full
    2. transmitter empty
    3. measurement finished
    4. break character received
Special LIN support:
• 13 bit break generation
• 11 bit break detection threshold
• A fractional-divide baud rate pre-scaler that allows fine adjustment of the baud rate

• Measurement counter which has 16 bits and can be used as a mini-timer to measure break and bit times (baud rate recovery).
• Baud measurement results can directly be fed into the baud register to adjust the baud rate (baud self-synchronization with SYNC byte)
• A special high-speed LIN mode allows an increasing of receiver bit transfer up to 125 kbit/s.

The LIN SCI uses a clock whose frequency is 16 times $1/t_{Bit}$. The detection of the start bit takes place at S1 in figure below. The sampling of the received signal occurs in the middle of the bit with three samples. The majority of the samples defines the bit level. This way the LIN requirements $t_{BFS}$, $t_{EBS}$ and $t_{LBS}$ are fulfilled.
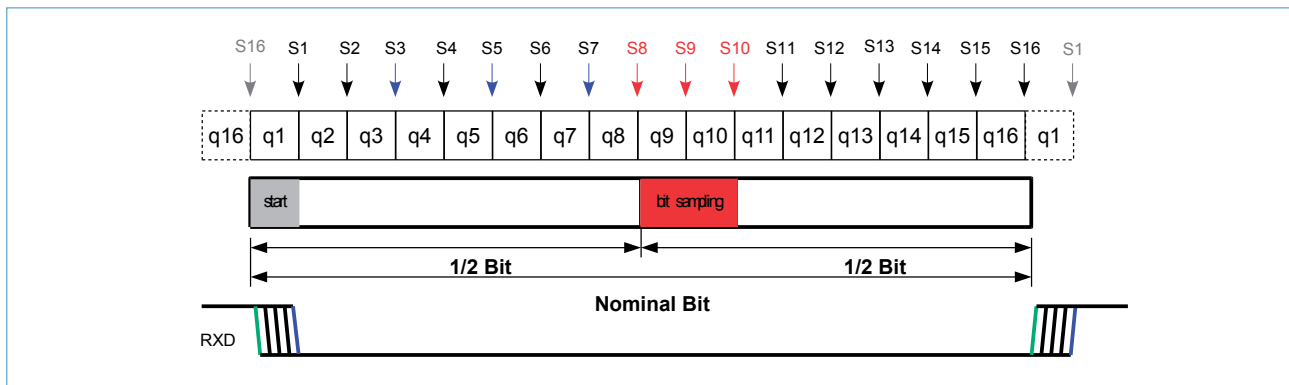


*Figure 9.   LIN SCI Operations*

The LIN_MODE register is used to select between the normal and high speed LIN mode. The high speed LIN mode allows data transmission rates of up to 125 kbit/s. Additionally, the SCI module can be disabled in order to control the LIN transceiver directly by CPU. This can be used to set up a custom specific protocol.

Table 17.   LIN Mode Configuration, Status and Data Register Table

| Register Name | Address | Description |
|---|---|---|
| SCIBRH | 0x0010 | SCI Baud Rate Register High Byte |
| SCIBRL | 0x0011 | SCI Baud Rate Register Low Byte |
| SCICTRL | 0x0013 | SCI Control Register |
| SCISTATH | 0x0014 | SCI Status Register High Byte |
| SCISTATL | 0x0015 | SCI Status Register Low Byte |
| SCIDATA | 0x0017 | SCI Data Register |
| SCIMEASCTRH | 0x0018 | SCI Measurement Control Register High Byte |
| SCIMEASCTRL | 0x0019 | SCI Measurement Control Register Low Byte |
| SCIMEASDATH | 0x001A | SCI Measurement Data Register High Byte |
| SCIMEASDATL | 0x001B | SCI Measurement Data Register Low Byte |
| LIN_MODE | 0x001E | LIN Mode Configuration Register |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Table 18.   LIN Mode Configuration Register

| LIN_MODE | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | TXD_TO_DIS | RXD_F_IRQ | RXD_R_IRQ | RXD_IRQ_EN | HS_EN | SCI_DIS | TXD | RXD |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 1 | - |
| Internal access | | | | | | | | |
| External access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R |
| Bit Description | **TXD_TO_DIS** : disable TXD timeout functionality:<br>$1_b$ : functionality disabled<br>$0_b$ : functionality enabled<br>**RXD_F_IRQ** : RXD falling edge interrupt<br>$1_b$ : indicates a falling edge on the bus input<br>Write '0' to clear this bit.<br>**RXD_R_IRQ** : RXD rising edge interrupt<br>$1_b$ : indicates a rising edge on the bus input<br>Write '0' to clear this bit.<br>**RXD_IRQ_EN** : RXD edge interrupt enable<br>$0_b$ : interrupt disabled<br>$1_b$ : interrupt enabled<br>**HS_EN** : enable high speed receiver:<br>$0_b$ : normal LIN mode<br>$1_b$ : high speed receiver enabled<br>**SCI_DIS** : disable internal SCI module:<br>$0_b$ : SCI module active<br>$1_b$ : SCI module disabled, LIN transmitter controlled by bit number 1 'TXD'<br>**TXD** : CPU access to BUS (only if SCI_DIS=1):<br>$0_b$ : bus dominant<br>$1_b$ : bus recessive<br>**RXD** : read current bus state | | | | | | | | |

Table 19.   SCI Baud Rate Register High Byte

| SCIBRH | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | BD[15] | BD[14] | BD[13] | BD[12] | BD[11] | BD[10] | BD[9] | BD[8] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **BD[15]** : MSB of SCI baud rate divisor select high byte<br>**BD[8]** : LSB of SCI baud rate divisor select low byte | | | | | | | |

Table 20.   SCI Baud Rate Register Low Byte

| SCIBRL | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | BD[7] | BD[6] | BD[5] | BD[4] | BD[3] | BD[2] | BD[1] | BD[0] |
| Reset value | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **BD[7]** : MSB of SCI baud rate divisor select low byte<br>**BD[0]** : LSB of SCI baud rate divisor select low byte<br><br>Divisor: $$BD[15:0] = \frac{2 \cdot f_{CLK}}{Baudrate}$$<br>Set BD[15:0] as follows:<br>BD[15:0]=0x0080 for 125kbit/s<br>BD[15:0]=0x0341 for 19.2kbit/s<br>BD[15:0]=0x0683 for 9.6kbit/s<br>BD[15:0]=0x0000 means bypassing the baud rate divisor | | | | | | | |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Table 21.  SCI Control Register

| SCICTRL | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | TIE | LIN | RIE | BIE | TE | RE | MFIE | SBK |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **TIE** : TxD Interrupt Enable (generates SCI_TIE_IRQ interrupt when TDRE is set)<br>**LIN** : Lin Mode:<br>LIN break transmit enable (13 bit break symbol instead of 10 bit),<br>LIN break receive detection enable (detects a 11 bit break symbol instead of 10 bit)<br>**RIE** : RxD Interrupt Enable (generates SCI_RIE IRQ interrupt when RDRF is set)<br>**BIE** : Break detection Interrupt Enable (generates SCI_BIE_IRQ interrupt when BRF is set)<br>**TE** : Transmitter Enable<br>If software clears TE while a transmission is in progress (TC = 0), the frame in the transmit shift register continues to shift out. To avoid accidentally cutting off the last frame in a message, always wait for TDRE to go high after the last frame before clearing TE.<br>**RE** : Receiver Enable<br>RE set to '0' suppresses start bit recognition.<br>Setting RE to '1' during an ongoing transfer can cause erroneous data reception and interrupt generation (RDRF).<br>Setting RE to '0' during an ongoing transfer can cause erroneous data reception and interrupt generation (RDRF), received data should be ignored.<br>**MFIE** : Measurement Finish Interrupt Enable (generates SCI_MFIE_IRQ interrupt when MF is set)<br>**SBK** : Send BreaK bit<br>Toggling SBK sends one break character (10 logic zeros, respectively 13 logic zeros if LIN is set). Toggling implies clearing the SBK bit before the break character has finished transmitting. As long as SBK is set, the transmitter continues to send complete break characters (10 bits respectively 13 bits). | | | | | | | | |

Table 22.  SCI Status Register High Byte

| SCISTATH | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | - | - | - | - | - | - | ABT | AMT |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R | R | R | R | R | R | R | R |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **ABT** : Auto Baud Triggered<br>Set when new baud value was copied automatically to baud configuration register after a valid SNYC byte measurement. Cleared when reading the MSB of the status word.<br>**AMT** : Auto Meas Triggered<br>Set when measurement was started automatically after reception of a valid break. Cleared when reading the MSB of the status word. | | | | | | | | |

Table 23.   SCI Baud Rate Register Low Byte

| SCISTATL | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | TDRE | TC | RDRF | BRF | OV | MRUN | MF | FE |
| Reset value | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R | R | R | R | R | R | R | R |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **TDRE** : Transmit Data Register Empty<br>Clear TDRE by writing to SCI data register. Write will be ignored when transmit register is not empty, so check if TDRE = 1 before writing to transmit register.<br>**TC** : Transmit Complete flag<br>TC is set to '0' while a transmission is in progress<br>**RDRF** : Receive Data Register Full flag<br>Clear RDRF by reading SCI status with RDRF set and then reading SCI data register.<br>NOTE: RDRF will be set:<br>a) in case of data reception: 1/8 nominal bit length after the recognized stop bit. Since the bits are sampled in the middle of a nominal bit length, the flags and the interrupt will be set after the estimated end of the active stop bit.<br>b) in case of break reception: see BRF description below<br>**BRF** : Break Received Flag (LIN mode dependent)<br>Clear BRF by reading SCI status with BRF set and then reading SCI data register.<br>The BR flag will be set when the start bit is followed by 8 (respectively 9 when LIN mode is set) logic 0 data bits and a logic 0 where the stop bit should be.<br>When BRF is set FE and RDRF will be set, too. The SCI data register will be cleared.<br>Note: flag generation (incl. BRF) will be suppressed when AAM is set.<br>**OV** : receiver overrun detected<br>Clear OV by reading SCI status with OV set and then reading SCI data register.<br>OV will be set when a received data byte is not read before the data byte of the next frame or a break character arrives. The second data byte will be ignored.<br>**MRUN** : Measurement Running<br>**MF** : Measurement Finish flag<br>Clear MF by read accessing the measurement counter.<br>**FE** : Framing Error flag<br>FE is set when the logic does not detect a logic 1 where the stop bit should be.<br>FE will be updated at the same time as RDRF. | | | | | | | | |

Table 24.   SCI Data Register

| SCIDATA | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | SCIDATA[7] | SCIDATA[6] | SCIDATA[5] | SCIDATA[4] | SCIDATA[3] | SCIDATA[2] | SCIDATA[1] | SCIDATA[0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **SCIDATA[7]** : MSB of SCI data register<br>**SCIDATA[0]** : LSB of SCI data register<br>write SCIDATA[7:0] for transmitting a byte, read it for a received byte | | | | | | | |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Table 25.  SCI Measurement Control Register High Byte

| SCIMEASCTRH | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | - | - | DBC[6] | DBC[5] | DBC[4] | DBC[3] | DBC[2] | DBC[1] |
| Reset value | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| Internal access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **DBC[6]** : MSB of debouncing filter value<br>**DBC[1]** : DBC[6:1] - debouncing filter threshold for baud rate measurement (MMODE=0)<br>DBC[0] is always set to logic 1. DBC[6:0] set the debouncing time as follows:<br>$t_{debounce}$ = DBC[6:0] • $t_{CLK}$<br>The reset value is decimal 41 (nominally 5125ns). | | | | | | | |

Table 26.  SCI Measurement Control Register Low Byte

| SCIMEASCTRL | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | - | - | - | - | AB | AM | MMODE | MEN |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R | R | R | R | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **AB** : AutoBaud<br>Automatically copy baud measurement result to baud config register after a valid baud measurement (expecting SYNC byte). The ABT flag will be set.<br>NOTE: During baud measurement the receiver is disabled an therefore no data will be received, only the measurement logic is active which will set the MF flag (configurable as interrupt).<br>**AM** : Auto Meas<br>Automatically start a baud rate measurement after reception of a valid break. The AMT flag will be set.<br>NOTE: AUTO_MEAS mode suppresses the flag specific flag generation (see SCI_status -> BRF).<br>**MMODE** : Measurement Mode Select<br>0 : Baud rate measurement, counter runs with system clock and measures time between 4 falling edges (8 bit times are measured), debouncer is enabled.<br>NOTE: The baud measurement expects a 0x55 data byte to measure, this is the SYNC byte in the LIN protocol.<br>1 : break time measurement, counter runs with 16-fold baud rate, measures time when RxD line is zero.<br>NOTE: only applicable together with MEN control bit.<br>**MEN** : Measurement Enable<br>Set to '1' to start a measurement.<br>After the measurement is finished, the MEN bit will be cleared automatically.<br>NOTE: When the AM bit is set, MEN must not be used.<br>NOTE: Writing a '0' to MEN resets the measurement logic and allows a safe restart. | | | | | | | |

Table 27.  SCI Measurement Data Register High Byte

| SCIMEASDATH | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | MC[15] | MC[14] | MC[13] | MC[12] | MC[11] | MC[10] | MC[9] | MC[8] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **MC[15]** : MSB of Measurement Counter high byte<br>**MC[8]** : MSB of Measurement Counter high byte | | | | | | | |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Table 28. SCI Measurement Data Register Low Byte

| SCIMEASDATL | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | MC[7] | MC[6] | MC[5] | MC[4] | MC[3] | MC[2] | MC[1] | MC[0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | MC[7] : MSB of Measurement Counter low byte<br>MC[0] : LSB of Measurement Counter low byte<br>The counter is cleared by every start of a new measurement.<br>When the measurement counter overflows, the counter value is saturated to 0xFFFF and the measurement will be stopped (MF flag set). The measurement should be repeated with an adapted baud rate setting.<br>Note: in baud measurement mode the resulting 16 bit value MC[15:0] can be fed into the baud rate register to adjust the baud rate BD[15:0]. | | | | | | | |

The following diagram shows the automatic baud rate measurement process with AM=1. The measurement run (MRUN) starts automatically after lin break detection and ends after sync-field measurement. The up- date_baud signal indicates the baud rate register update time, if AB=1. During the baud rate measurement the flags in the SCISTATL register are not updated.
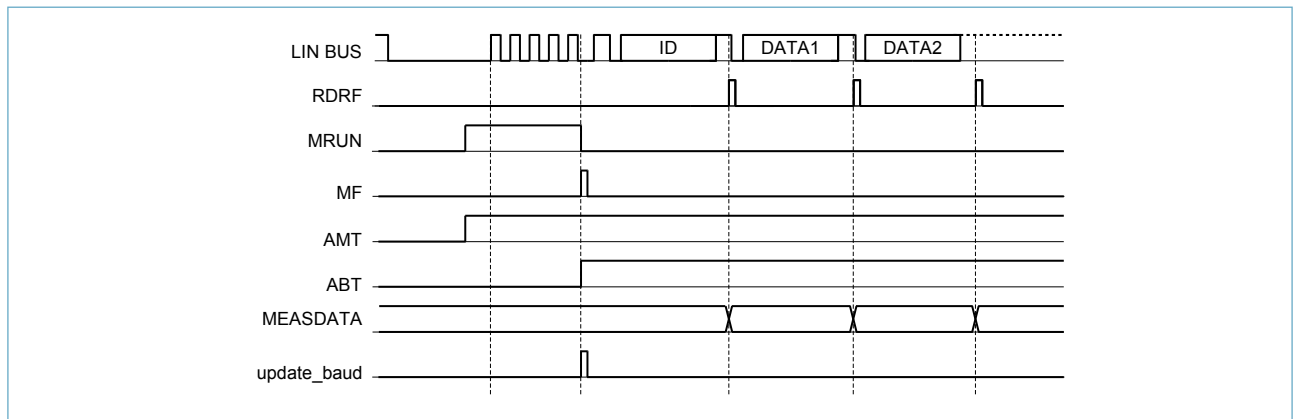


Figure 10. Timing Diagram of Autobaud Measurement

## 6.15 LIN Auto-addressing ( only in products with LIN Auto-addressing )

**Called "SNPD" in official LIN-specification**

Table 29. LIN Auto-addressing Register Table

| Register Name | Address | Description |
|---|---|---|
| LINAA | 0x001F | LIN Auto-addressing Register |

Table 30. LIN Auto-addressing Register

| LINAA | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | - | REF_ON | REF_SEL | I2MEN | ON30K | AAEN | - | - |
| Reset value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Internal access | R | R/W | R/W | R/W | R/W | R/W | R | R |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | REF_ON : $1_b$ : activates 100µA reference current source of the LIN bus<br>REF_SEL : $1_b$ : selects the 10Ω reference resistor<br>$0_b$ : selects the 1Ω auto-addressing resistor<br>I2MEN : $1_b$ : activates the 2mA current source of the LIN bus<br>ON30K : $1_b$ : activates the pull-up resistor on the LIN bus<br>AAEN : $1_b$ : LIN auto-addressing enable | | | | | | | |

### Auto-addressing Mechanism

The auto-addressing feature added to the normal LIN bus functionality allows that slaves to detect their relative position within a bus system. The hardware extensions needed for that purpose are a shunt resistor between the BUS_M and BUS_S nodes of the slave, a pull-up current source of typically 2mA and a circuitry that allows to measure the differential voltage across the bus shunt. The measurement is performed via the internal ADC. The slaves within such a bus system have to be connected as a displayed below. The following diagram shows such a bus architecture:
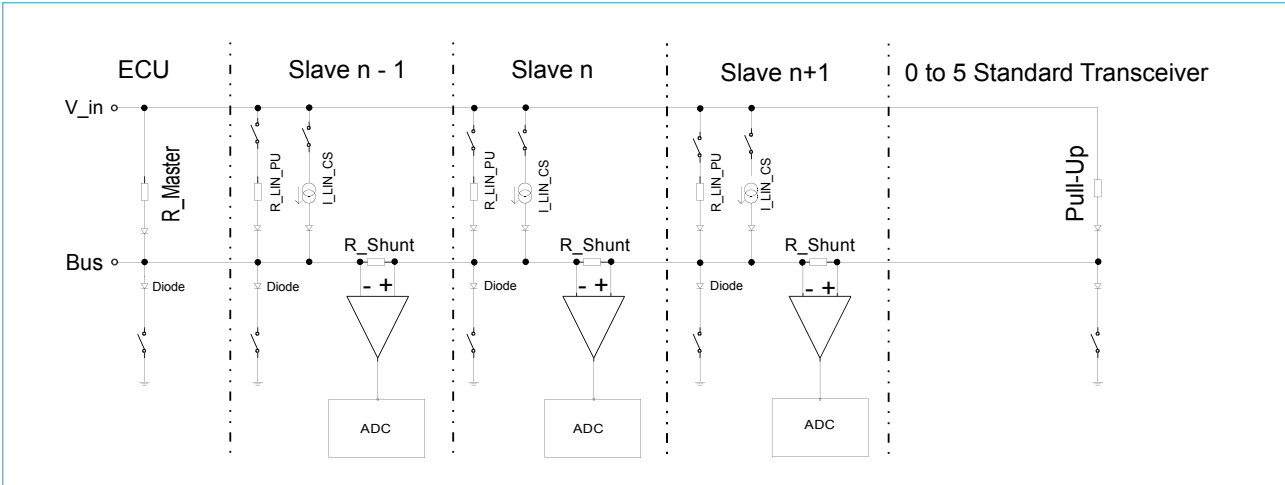


*Figure 11.   LIN Bus Auto-addressing Architecture*
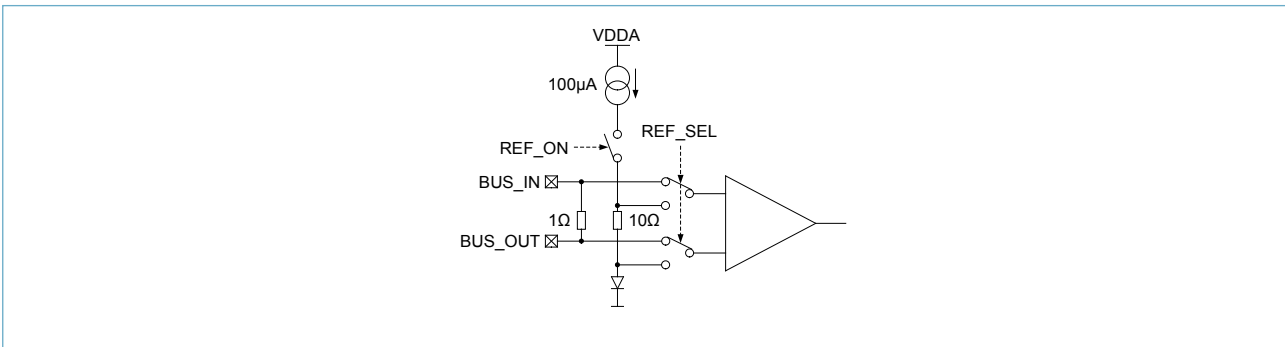


*Figure 12.   LIN Auto-addressing Reference Threshold Generation*

On the left side of the schematic the ECU is terminating the LIN bus. Next there is a group of addressable slaves, each of them having its own auto-addressing circuitry. Finally, shown on the right side of the schematic, there may be some standard LIN bus transceivers without auto-addressing capability. As well they may be mixed up with the addressable slaves in any possible position.

The start of the addressing sequence is initialized by the ECU, with a command sent to the slaves telling them that the addressing sequence starts with the next sync break. After receiving this message, the slave performs a self-calibration. The 100µA reference current source is enabled, the amplifier input is multiplexed to the 10Ω reference resistor and a reference threshold voltage is measured by the ADC, see figure above. During the next sync break each slave starts its auto-address-ing sequence. The sequence is divided up in measuring the offset current on the bus line, measuring the bus load and, depending on the bus load, switching on the current source for the detection of the last not addressed slave in the line. It is recommended to use a threshold value of 1mA for the decision in the following flow chart (as derived by the self-calibration measurement). This gives the maximum noise immunity to the low value (0mA) and the high value (2mA if only one other slave is behind).

In order to assure that the different steps of the auto-addressing sequence are executed synchronously by all the slaves, a timing scheme for the sync break is defined. The time reference is the bit time $t_{BIT,SLAVE}$. The following timing diagram shows the requested timing for the different steps to executed during the sync break.

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B
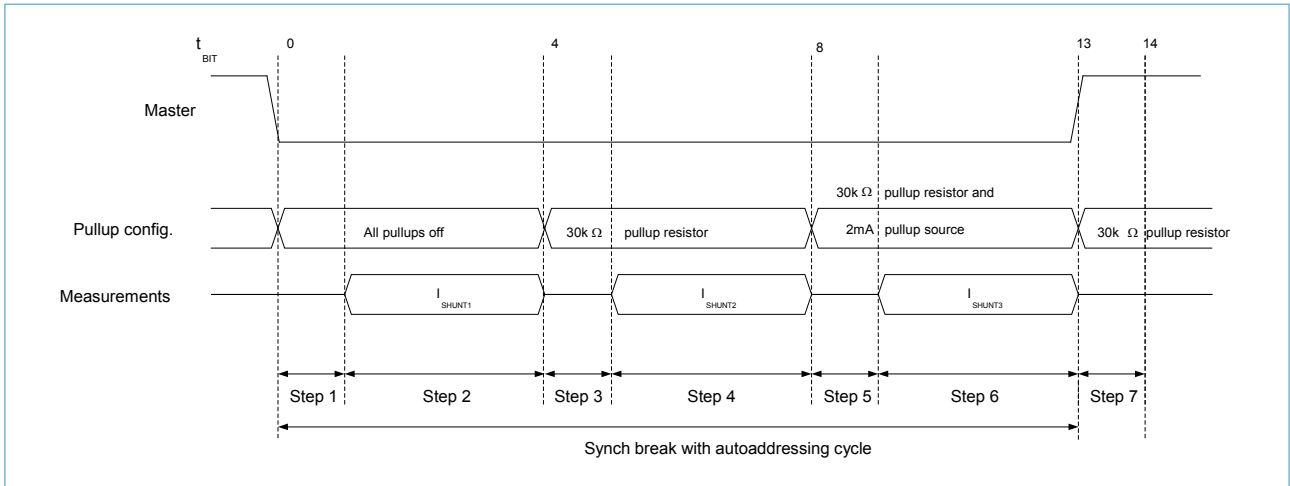
*Figure 13.   Timing Diagram Auto-addressing Process*

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E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

The following flowchart shows the command sequence, that is executed during every synch break within the auto-addressing process.

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B



```
                    START

          Master sends autoaddressing            ┆  Step 1
                  command                         ┆

              All slaves
          detect synch break

          All addressable slaves
        switch off 30kΩ LIN pullup

    Y  ◁── Slave already addressed ? ──▷
                      │ N
          Measure bus current I_SHUNT1            ┆  Step 2
                                                  ┆  Step 3
          All not addressed slaves
        switch on 30kΩ LIN pullup                 ┆  Step 4

          Measure bus current I_SHUNT2

          Calculate difference                    ┆  Step 5
          I_DIFF21 = I_SHUNT2 - I_SHUNT1

    Y  ◁── I_DIFF21 > threshold ? ──▷
                      │ N
  Switch off 30kΩ LIN pullup   All not addressed slaves   ┆  Step 6
  and wait for end of          switch on 2mA pullup source
  procedure
                               Measure bus current I_SHUNT3

                               Calculate difference         ┆  Step 7
                               I_DIFF31 = I_SHUNT3 - I_SHUNT1

                     Y  ◁── I_DIFF31 > threshold ? ──▷
                                          │ N
                               Slave saves address contained
                               in autoaddressing command

          All slaves
          switch off 2mA pullup source
          and switch on 30kΩ LIN pullup

        Master checks:               N
        all slaves addressed?  ──────▷
                  │ Y
                STOP
```

Figure 14.   Flowchart Auto-addressing Process

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## 6.16 Hall Sensor or Potentiometer Input

The pins D1, D2, D3 have two functions:

1. The pins are 3.3V analog inputs. The input voltage can be measured with the internal ADC. The maximum measurable voltage is equal to the internal ADC reference voltage ).

2. The pins are configured as 5V general purpose inputs or outputs. They can individually be configured as input or as output. In input mode they can interface digital Hall-sensors.

It is possible to set the functionality of each pin D1, D2, D3 individually, e.g. D1 is configured as 3.3V analog input, D2 as 5V digital input and D3 as 5V digital output. If the pins are used, the V5V regulator has to be turned on, regardless of the configuration of the pins.

The pins are equipped with software-controllable pull-up and pull-down structures. These can be configured individually for each pin.

It is possible to generate an interrupt, if the state of the input pins is changed. The interrupt is enabled with GPIO_IE in the register GPIOCFG by writing a '1'. A pending interrupt is reset by writing a '0' at GPIO_IE.

*NOTE: The three features analog/digital input, digital output level and pull-up/pull-down can be configured in an arbitrary manner for each pin. For analog input pins care has to be taken, that the reduced analog input voltage range is met by the configuration.*
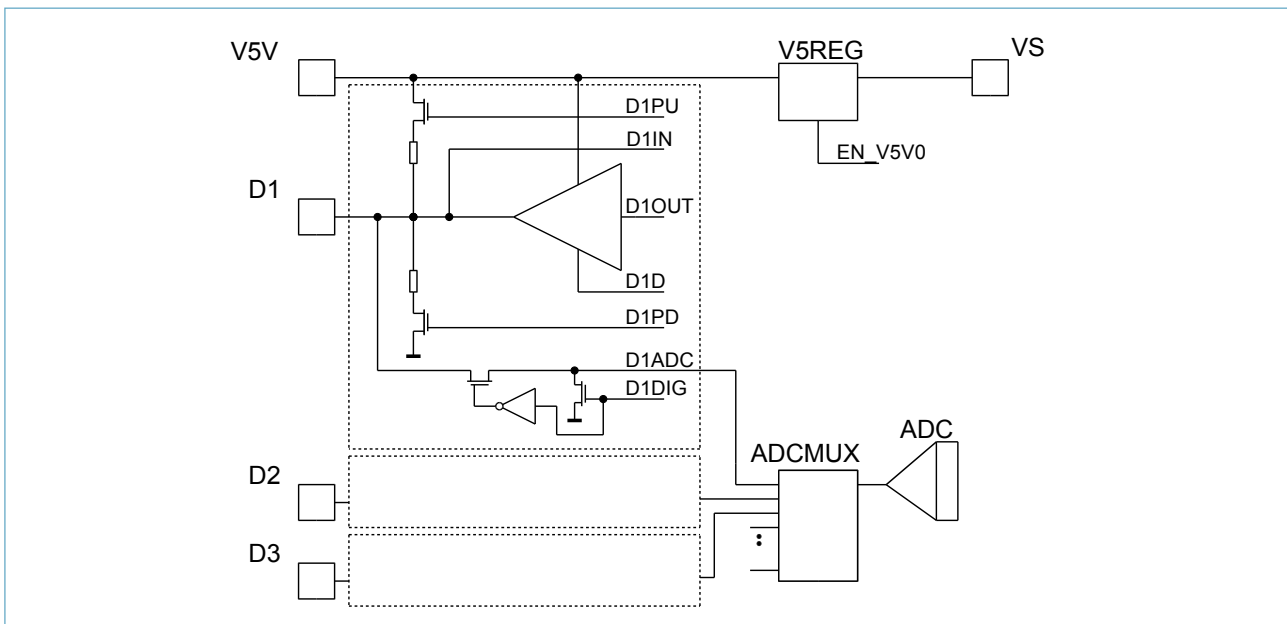


*Figure 15.   GPIO block diagram*

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Table 31.  GPIO Register Table

| Register Name | Address | Description |
|---|---|---|
| GPIO | 0x0002 | GPIO Input Register |
| GPIOPUD | 0x0003 | GPIO Pull-up and Pull-down |
| GPIOCFG | 0x0403 | GPIO Control Register |

Table 32.  GPIO Control Register

| GPIOCFG | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | EN_V5V0 | GPIO_IE | D3DIG | D2DIG | D1DIG | D3D | D2D | D1D |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **EN_V5V0** : Enable Hall-sensor supply regulator<br>**GPIO_IE** : $1_b$ Enables interrupt at GPIO<br>$\quad\quad\quad 0_b$ Resets a pending interrupt<br>**D3DIG** :  $1_b$ Pin D3 is configured as 5V GPIO<br>$\quad\quad\quad 0_b$ Pin D3 is configured as 3.3V analog input<br>**D2DIG** :  $1_b$ Pin D2 is configured as 5V GPIO<br>$\quad\quad\quad 0_b$ Pin D3 is configured as 3.3V analog input<br>**D1DIG** :  $1_b$ Pin D1 is configured as 5V GPIO<br>$\quad\quad\quad 0_b$ Pin D3 is configured as 3.3V analog input<br>**D3D** :  $1_b$ If configured as 5V GPIO, then pin D3 is output<br>$\quad\quad\quad 0_b$ If configured as 5V GPIO, then pin D3 is input<br>**D2D** :  $1_b$ If configured as 5V GPIO, then pin D2 is output<br>$\quad\quad\quad 0_b$ If configured as 5V GPIO, then pin D2 is input<br>**D1D** :  $1_b$ If configured as 5V GPIO, then pin D1 is output<br>$\quad\quad\quad 0_b$ If configured as 5V GPIO, then pin D1 is input | | | | | | | | |

Table 33.  GPIO Input Register

| GPIO | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | - | - | - | - | - | D3 | D2 | D1 |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | - | - | - | - | - | R/W | RW | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **D3** : State of D3<br>**D2** : State of D2<br>**D1** : State of D1 | | | | | | | |

Table 34.  GPIO Pull-up and Pull-down

| GPIOPUD | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | - | D3PD | D2PD | D1PD | - | D3PU | D2PU | D1PU |
| Reset value | - | 0 | 0 | 0 | - | 0 | 0 | 0 |
| Internal access | - | R/W | R/W | R/W | - | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **D3PD** : $1_b$ Enables pull-down resistor on D3<br>**D2PD** : $1_b$ Enables pull-down resistor on D2<br>**D1PD** : $1_b$ Enables pull-down resistor on D1<br>**D3PU** : $1_b$ Enables pull-up resistor on D3<br>**D2PU** : $1_b$ Enables pull-up resistor on D2<br>**D1PU** : $1_b$ Enables pull-up resistor on D1 | | | | | | | |

## 6.17 ADC and Input Multiplexer

The controller has access to an internal 8-bit ADC. The ADC has different input sources:

1. Potentiometer input D1,
2. Potentiometer input D2,
3. Potentiometer input D3,
4. Resistively divided supply voltage,
5. Temperature monitor,
6. Temperature shutoff threshold.

The ADC source is selectable with SEL[2:0] in the ADCCNTR register.

The pins D1 to D3 are configurable as Hall or potentiometer inputs via the GPIOCNTR register. The measurement principle is ratio-metric, if an external potentiometer of typically 10kΩ is connected between VDDA and GNDA, as the internal ADC references are equal to the VDDA/GNDA voltages. Ambient temperature measurements are also possible if an external sensor is used.

The supply voltage is divided by 12. The input range is $0..12*V_{VDDA}$. It is possible to realize over- or under-voltage warning thresholds at system level.

The chip temperature is also monitored. It is possible to program a hot or cold warning function at system level. The measured temperature is scaled in the following way: $T_J(°C)= (ADC-K_0)*G_T$. The temperature shutoff threshold is calculated in the same way.

Following decimal values are typically expected: 120 @ -40°C, 99 @ 25°C, 68 @ 125°C and 60 @ 150°C.

The ADC is a 8-Bit SAR ADC. The ADC consists of two parts, the analog and the digital ones. The ADC uses a charge redistribution split array DAC and a comparator in a successive-approximation loop to achieve a conversion time of 21 $t_{CLK}$ clock cycles. The ADC conversion time of the chip is therefore 2.625µs (4 clk for sampling window) . If the channel for the LIN Auto Addressing is set, the conversion time is 171 $t_{CLK}$ clock cycles (128 $t_{CLK}$ for sampling window) or approximately 21.4µs.

Table 35.   ADC Register Table

| Register Name | Address | Description |
|---|---|---|
| ADCCNTR | 0x0020 | ADC Control Register |
| ADCDAT | 0x0021 | ADC Data |

Table 36.   ADC Control Register

| ADCCNTR | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | EOC | TADC1 | TADC0 | SEL[3] | SEL[2] | SEL[1] | SEL[0] | SOC |
| Reset value | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R | R | R | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **EOC** : End of conversion<br>**TADC1** : Test<br>**TADC0** : Test<br>**SEL[3]** : ADC input select 3<br>**SEL[2]** : ADC input select 2<br>**SEL[1]** : ADC input select 1<br>**SEL[0]** : ADC input select 0<br>$0000_b$: D1 voltage<br>$0001_b$: D2 voltage<br>$0010_b$: D3 voltage<br>$0011_b$: $V_{VS}$/12<br>$0100_b$: $T_J$<br>$0101_b$: $T_{shutoff,thr.}$<br>$0110_b$: LIN Auto Addressing<br>$0111_b$:<br>$1000_b$: TDAIO<br>$1001_b$: Zero<br>**SOC** : Start of conversion | | | | | | | | |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Table 37.   ADC Data

| ADCDAT | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | ADC[7] | ADC[6] | ADC[5] | ADC[4] | ADC[3] | ADC[2] | ADC[1] | ADC[0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R | R | R | R | R | R | R | R |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | | | | | | | | |

# 7 Half Bridge Drivers

## 7.1  Output Drivers and Control

The output drivers A0/A1 and B0/B1 are composed of two H-bridges. Each driver of the H-bridge is accessible separately through a control register. If an over-temperature condition is detected, the drivers are switched off by hardware. The following diagram shows the structure of one full bridge.
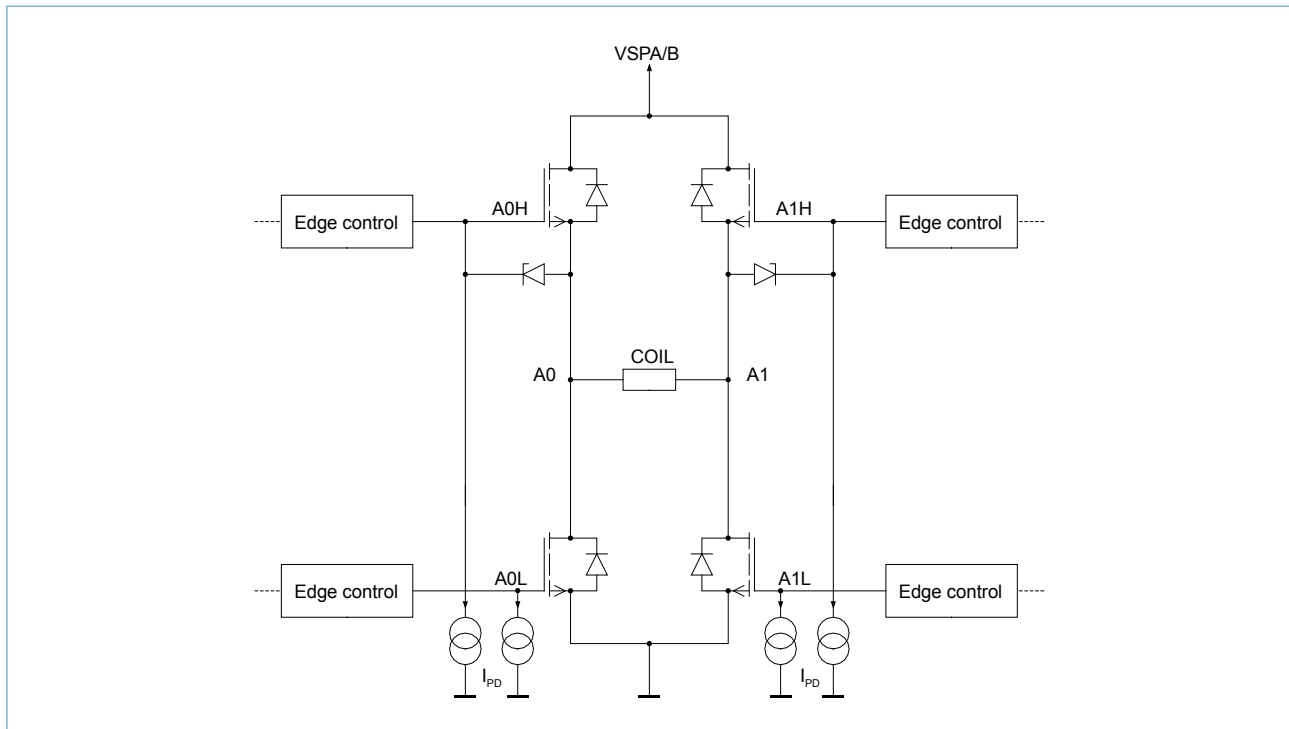


*Figure 16.   Current Control Loop*

## 7.2  Chopper Current Control Loop

A chopper control is for torque control and micro-stepping implemented. The IC provides a fixed frequency PWM to allow a more precise supply filtering for EMI reduction. The chopper $t_{ON}$ phase starts with the base frequency. The $t_{ON}$ phase ends if the comparator indicates that the current level is reached. Due to the fact that there may be short current peaks at the beginning of each tON phase caused by capacitive loads on A0/1 or B0/1, the current measurement hardware will be masked for a defined time $t_{mask}$ after the beginning of any $t_{ON}$ phase. The off-time will not be present if the peak current is not attained during the PWM on-time. The current level for coils A and B are set up with the values of registers IDACA and IDACB.

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

*Figure 17. Simplified schematic of the current control loop of one full bridge*

The driver currents $I_{A0}$ and $I_{A1}$ are mirrored into the current measurement hardware by splitting the related power transistors into two sections. The driver and sense transistors of each half bridge share common gate and source nodes, the drain nodes of both sense transistors belonging to one full bridge are tied together. Due to the fact that only one of the full bridge's low-side drivers may be enabled at a time, these two drain nodes may be connected without any additional switch.

In order to make the driver current and the sensed current match the width relation of driver and sense transistor, the drain voltage has to be controlled by an operation amplifier. The reference voltage of this control loop is one of the half bridge output voltages $V_{A0}$ or $V_{A1}$, depending on the state of the full bridge. If the full bridge is disabled or in its tOFF phase, the input voltage of the operation amplifier has to be tied to a defined bias voltage.

The output signal of the circuitry around the low side driver transistors equals the coil current divided by a special mirror factor, that was defined by the driver/ sense transistor width relation. This internal sense current will be mirrored a second time and then will be compared to a reference current $I_{DAC}$.

Due to the fact that there may be short current peaks at the beginning of each $t_{ON}$ phase caused by capacitive loads on A0 or A1, the current measurement hardware will be masked for a defined time $t_{MASK}$ after the beginning of any tON phase. During this phase the current measurement hardware is held in a safe state (COMP=$0_b$). After the end of the mask time the current measurement hardware will settle from this initial state to the normal operating condition. For setting the masking time, refer to register HBCTRL (Table 43 Half Bridge Control Register).

The following table shows the setup of the current control loop for the different configurations of the half bridge A.

Table 38.   Current Control and Half Bridge State Table

| Phase | A0H | A0L | A1H | A1L | S0 | S1 | $A_{INT}$ | $I_{A,INT}$ |
|---|---|---|---|---|---|---|---|---|
| $t_{ON}$ | - | ON | ON | - | ON | - | $V_{A0}$ | $I_{A0}/M$ |
| $t_{ON}$, reversed direction | ON | - | - | ON | - | ON | $V_{A1}$ | $I_{A1}/M$ |
| $t_{OFF}$ | ON | - | ON | - | - | - | Idle | 0 |
| Drivers disabled | - | - | | - | - | - | Idle | 0 |

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## 7.3 Motor Register Control

The half bridge drivers get their control signals from the motor control logic. The rotational position of the motor and the torque of the motor is controlled by the current of coils A and B. The control logic includes the PWM generation, the current control and the stall detection. Waveform Control to be done by software with minimum 10 kHz refresh rate.

Table 39. Motor Control Register Table

| Register Name | Address | Description |
|---|---|---|
| STLDTHR | 0x0000 | Motor Configuration Register 1 ( please contact supplier for optimized values ) |
| CNTFBC | 0x000D | Motor Configuration Register    ( read only, not needed for application         ) |
| STLFINC | 0x000E | Motor Configuration Register 2 ( please contact supplier for optimized values ) |
| STLFLVL | 0x000F | Motor Configuration Register 3 ( please contact supplier for optimized values ) |
| HBCTRL | 0x0028 | Half Bridge Control Register |
| HBDATA | 0x0029 | Half Bridge Data Register |
| HBSTATUS | 0x002A | Half Bridge Status Register |
| IDACA | 0x002B | Chopper Current Register of Half Bridge A |
| IDACB | 0x002C | Chopper Current Register of Half Bridge B |
| DECCTRL | 0x002D | Decay Control Register |
| ONTIME | 0x002E | On-Time Register |
| MOTSTA | 0x002F | Motor Status Register |
| STLFTHR | 0x0411 | Motor Configuration Register 4 ( please contact supplier for optimized values ) |

Table 40. Motor Configuration Register 1

| STLDTHR (0x0000) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | - | DTHR[6] | DTHR[5] | DTHR[4] | DTHR[3] | DTHR[2] | DTHR[1] | DTHR[0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **DTHR[6:0 ]**Motor Configuration Register 1 ( please contact supplier for optimized values ) | | | | | | | |

Table 41. Motor Configuration Register 2

| STLFINC (0x000E) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | FINC[5] | FINC[4] | FINC[3] | FINC[2] | FINC[1] | FINC[0] | MOTP-WM_IE | MOTP-WM_IRQ |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **FINC[5:0]** Motor configuration Parameter Set 2 (please contact supplier for optimized values)<br>**MOTPWM_IE** : $1_b$ enables the MOTPWM Interrupt<br>**MOTPWM_IRQ** : Indicates the beginning of a new PWM cycle, Setting $1_b$ resets the bit | | | | | | | |

Table 42. Motor Configuration Register 3

| STLFLVL (0x000F) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | FLVL[7] | FLVL[6] | FLVL[5] | FLVL[4] | FLVL[3] | FLVL[2] | FLVL[1] | FLVL[0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **FLVL[7:0]** : Motor Configuration Parameter Set 3 (please contact supplier for optimized values) | | | | | | | |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Table 43.   Half Bridge Control Register

| HBCTRL (0x0028) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | MASK[1:0] | MASK[1:0] | - | SLEW | FDECA | FDECB | RNG[1:0] | RNG[1:0] |
| Reset value | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **MASK[1:0]** masks current comparator signal at the leading edge for a defined time $t_{mask}$<br>$00_b$ : 750ns<br>$01_b$ : 1500ns<br>$10_b$ : 2250ns<br>$11_b$ : 3000ns<br>**SLEW** : SLEW[1:0] sets the slew rate control<br>$0_b$ : 70V/µs mode<br>$1_b$ : 110V/µs mode<br>**FDECA** : Enable Fast Decay on Coil A<br>**FDECB** : Enable Fast Decay on Coil B<br>Note: No simultaneous setting of FDECA and FDECB allowed. In such a case only FDECA gets effective.<br>**RNG[1:0]** : sets the motor current range<br>$00_b$ : 300mA<br>$10_b$ : 600mA<br>$11_b$ : 800mA | | | | | | | |

Table 44.   Half Bridge Data Register

| HBDATA (0x0029) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | ENA0 | ENA1 | ENB0 | ENB1 | SETA0 | SETA1 | SETB0 | SETB1 |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **ENA0** : $1_b$ : Enables half bridge A0 (not tri-state)<br>**ENA1** : $1_b$ : Enables half bridge A1 (not tri-state)<br>**ENB0** : $1_b$ : Enables half bridge B0 (not tri-state)<br>**ENB1** : $1_b$ : Enables half bridge B1 (not tri-state)<br>**SETA0** : $1_b$ : Switches half bridge A0 to High, otherwise to Low<br>**SETA1** : $1_b$ : Switches half bridge A1 to High, otherwise to Low<br>**SETB0** : $1_b$ : Switches half bridge B0 to High, otherwise to Low<br>**SETB1** : $1_b$ : Switches half bridge B1 to High, otherwise to Low<br>Note, that HBDATA values get effective at the beginning of the next PWM frame and the bridge output is also affected by the chopper logic. | | | | | | | |

Table 45.   Half Bridge Status Register

| HBSTATUS (0x002A) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | ZCCA | ZCCB | CCA | CCB | x | x | x | x |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R | R | R | R |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **ZCCA** : Zero crossing comparator A (transparent)<br>**ZCCB** : Zero crossing comparator B (transparent)<br>**CCA** : Chopper Current comparator A (transparent)<br>**CCB** : Chopper Current comparator B (transparent) | | | | | | | |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Table 46. Chopper Current Register of Half Bridge A

| IDACA (0x002B) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | IDACA[7] | IDACA[6] | IDACA[5] | IDACA[4] | IDACA[3] | IDACA[2] | IDACA[1] | IDACA[0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **IDACA[7..0]** : Chopper threshold for current in coil A<br>Note, that IDACA values get effective at the beginning of the next PWM frame. When the register is read, the actual IDACA value is returned, that may differ from the last written value due to the aforementioned. | | | | | | | |

Table 47. Chopper Current Register of Half Bridge B

| IDACB (0x002C) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | IDACB[7] | IDACB[6] | IDACB[5] | IDACB[4] | IDACB[3] | IDACB[2] | IDACB[1] | IDACB[0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **IDACB[7..0]** : Chopper threshold for current in coil B.<br>Note, that IDACB values get effective at the beginning of the next PWM frame. When the register is read, the actual IDACB value is returned, that may differ from the last written value due to the aforementioned. | | | | | | | |

Table 48. Decay Control Register

| DECCTRL (0x002D) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | DECCTRL[7] | DEC-CTRL[6] | DEC-CTRL[5] | DEC-CTRL[4] | DEC-CTRL[3] | DEC-CTRL[2] | DEC-CTRL[1] | DEC-CTRL[0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **DECCTRL[7..0]** : Length of fast decay (1LSB means $t_{PWM,RES}$) | | | | | | | |

Table 49. On-Time Register

| ONTIME (0x002E) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | ONT[7] | ONT[6] | ONT[5] | ONT[4] | ONT[3] | ONT[2] | ONT[1] | ONT[0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R | R | R | R | R | R | R | R |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **ONT[7..0]** : shows on-time of the last PWM frame (1LSB means $t_{PWM,RES}$) of the phase, where fast decay was set. If neither FDECA nor FDECB was set, then ONT[7:0] is set to 0x00. | | | | | | | |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Table 50.   Motor Status Register

| MOTSTA (0x002F) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | STOP | STEN | ZCC_IE | ICAP | ESEL | CSEL | STE | STW |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R | R/W | R/W | R/W | R | R |
| External access | | | | | | | | |
| Bit Description | **STOP** :   Motor behavior in case of stall detected<br>**STEN** :   Stall detection enable<br>**ZCC_IE** : Zero crossing interrupt enable<br>**ICAP** :   Zero crossing input capture, $1_b$ when zero crossing has been detected,<br>        if writing $1_b$ the zero crossing interrupt is reset<br>**ESEL** :   Edge selection for zero crossing, $1_b$ rising edge is selected<br>**CSEL** :   Comparator selection for zero crossing, $1_b$ comparator A is selected<br>**STE** :   Stall detection error, $1_b$ indicates a confirmed stall detection<br>**STW** :   Stall detection warning, $1_b$ indicates a possible stall detection | | | | | | | | |

Table 51.   Motor Configuration Register 4

| STLFTHR (0x0411) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | FTHR[7] | FTHR[6] | FTHR[5] | FTHR[4] | FTHR[3] | FTHR[2] | FTHR[1] | FTHR[0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | | | | | | | | |
| Bit Description | **FTHR[7:0]** : Motor Configuration Register 4 ( please contact supplier for optimized values ) | | | | | | | |

## 7.4  Chopper Control

A chopper control is for torque control and microstepping implemented. The IC provides a fixed frequency PWM to allow a more precise supply filtering for EMI reduction. The chopper $t_{ON}$ phase starts with the base frequency. The $t_{ON}$ phase ends if the comparator indicates that the current level is reached. Due to the fact that there may be short current peaks at the beginning of each $t_{ON}$ phase caused by capacitive loads on A0/1 or B0/1, the current measurement hardware will be masked for a defined time $t_{mask}$ after the beginning of any $t_{ON}$ phase. The off-time will not be present if the peak current is not attained during the PWM on-time. The current level for coils A and B are set up with the values of registers IDACA and IDACB.

## 7.5 Current Decay

The IC offers the possibility to select between fast, slow and mixed decay mode.

- Slow decay is favorable when the current is rising from step to step. This occurs when the phase winding is shorted by switching on both high side FETs in the full bridge.
- Fast decay is most effective when the current is falling from step to step. This occurs when the voltage on the phase is reversed. To activate Fast or Mixed Decay Mode the corresponding bit in the register HBCTRL (Table 43 Half Bridge Control Register) has to be set. It is only possible to set the fast decay mode for one coil.

The setting of FDECA and FDECB simultaneously is not allowed.

One disadvantage of fast decay is the increased current ripple in the phase winding. To reduce the current rip-ple, the fast decay is used only a short time followed by the slow decay for the remainder PWM off-time. This technique is called mixed decay.

The decay behavior is selectable by software via the DECCTRL register and . A value of 0x00 means slow decay for the entire $t_{off}$ phase is selected. A value of 0xff means that fast decay is selected. Mixed decay means that the fast decay period starts with the beginning of the $t_{off}$ phase. The decay mode is switched to slow after a time of DECCTRL*$t_{PWM,RES}$. Automatic decay is feasible by software.

The length of the $t_{ON}$ phase gives an indication of the current ripple. Therefore it may be helpful to know the $t_{ON}$ time. It is measured in every cycle for the coil which is in Fast or Mixed Decay mode and is readable in the ONTIME register.
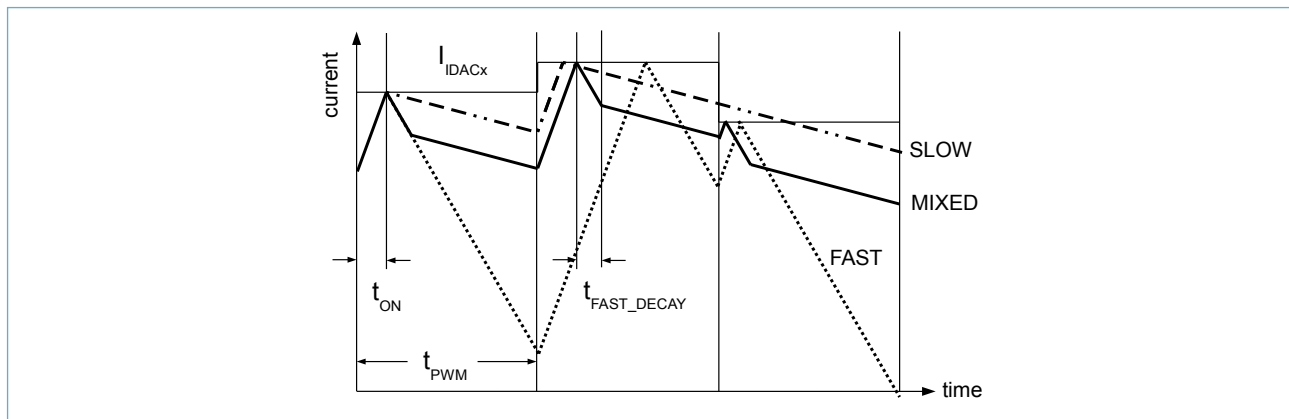


Figure 18.   Current Decay Waveform

## 7.6  Waveform Control

Waveform Control shall be done by software with minimum 10 kHz refresh rate.

## 7.7  Stall Detection

For proper stall detection functionality
the following motor configuration registers have to be set .( please contact supplier for optimized values )

Table 52.   Motor Configuration Register Table

| Register Name | Address | Description |
|---|---|---|
| STLDTHR | 0x0000 | Motor Configuration Register 1 |
| STLFINC | 0x000E | Motor Configuration Register 2 |
| STLFLVL | 0x000F | Motor Configuration Register 3 |
| STLFTHR | 0x0411 | Motor Configuration Register 4 |

It has to be guaranteed by the software, that the stepping frequency is not jittering more than +/-2%. Long term stepping frequency change, due to slow speed changes or oscillator temperature dependency, is tolerated by the stall detection logic. Further configurations recommended for stepper motor with stall detection are:

a) In the last step before reaching zero current in coil A or B

- check register 0x00D. If it's "zero" clear register bit STW of register Register MOTSTAT (0x002F) (see below)
- activate the stall detection by setting bit "STEN" of register "MOTSTA" (please also refer to chapter "Controlling the motor functions")

b) Set the half-bridge on the concerning coil, which is high, to low and the other which is low, to high impedance.

The stall detection analysis starts automatically, when STEN is set and the HBDATA value is transferred to the half bridge.

The stall detection logic will generate two status signal bits in register MOTSTA.

The first signal indicates a potential stall condition and sets the referred stall warning flag STW. If STW is $1_b$, it is recommended that the controller saves the current motor position for later use.

The second signal called stall error flag STE indicates a confirmed stall condition. If STE is $1_b$, the pre-viously saved position should be considered as the actual mechanical position by the controller. This procedure allows to minimize the mismatch between mechanical stop and the position where STE is set, which is caused by the stall detection filters. When a confirmed stall condition has been indicated by the STE flag, the controller is in charge to stop the motor movement, in order to prevent from noise or too high mechanical load.

If a stall condition has been confirmed and the related flag bit STE is set, the behavior of the circuit depends on the configuration of the STOP control bit. If the STOP bit is $0_b$, a confirmed stall condition does not have any effects on the motor drivers. The integrated controller is in charge to stop the motor movement.

Depending on the stepper motor type or mechanical characteristics of gearbox or bearing it may be necessary to perform an additional filtering of the STE flag in the external controller. If a stall warning or a confirmed stall condition disappears, the related flags STW or STE will be automatically cleared by the logic without further acknowledgment by the micro-controller. If the STOP bit is $1_b$, the confirmed stall condition information can be used by the controller to lead in a stop scenario, which may be "driver off" or "all drivers to GND" or "apply hold PWM" to increase the motors hold torque. In order to recover from this stall condition, the controller has first to stop and then to start the continuous motor stepping.

*Note: For using "stall detection" there is no need to handle register bits regarding "zero crossing". ZCC_IE can be off.*

Table 53.   Motor Status Register

| MOTSTA (0x002F) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | STOP | STEN | ZCC_IE | ICAP | ESEL | CSEL | STE | STW |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R | R/W | R/W | R/W | R | R |
| External access | | | | | | | | |
| Bit Description | **STOP** :   Motor behavior in case of stall detected<br>**STEN** :   Stall detection enable<br>**ZCC_IE** : Zero crossing interrupt enable<br>**ICAP** :   Zero crossing input capture, $1_b$ when zero crossing has been detected,<br>                    if writing $1_b$ the zero crossing interrupt is reset<br>**ESEL :   Edge selection for zero crossing, $1_b$ rising edge is selected**<br>**CSEL :   Comparator selection for zero crossing, $1_b$ comparator A is selected**<br>**STE** :   Stall detection error, $1_b$ indicates a confirmed stall detection<br>**STW** :   Stall detection warning, $1_b$ indicates a possible stall detection | | | | | | | | |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## 7.8 Zero Crossing Detection



*Figure 19.   Zero Crossing Comparator*

In "1 phase ON" mode it is possible to determine the point in time when the BEMF crosses through zero by observing the non-supplied coil. This signal may be used for an auto commutation application. The figure demonstrates the principle of the measurement.

After the micro-controller writes into the ZCTL register, the zero crossing detection starts. After the detection of the selected edge, the flag ICAP is set by the hardware and an interrupt is generated. The interrupt can be disabled by setting the bit ZCCS_I_EN. For using the zero crossing comparator please also refer to chapter "Controlling the motor functions" , register MOTSTA. For using "zero crossing" there is no need to handle register bits regarding "stall detection". STEN can be off.

## 7.9 Watchdog

The watchdog timer is implemented as a window watchdog. It starts after the first write to the window mode bits (WDCFG = 1) and can not be stopped any more. It triggers a reset pulse for the micro-controller system when software operation does not write the signature of 0x55 to the watchdog register within a configured watchdog window. The watchdog timer is clocked with $f_{CLK}$, so its resolution is 125ns.

The watchdog unit can be configured as simple time-out watchdog (means: open time window) or window watchdog (means: closed time window). Configuration is done by writing a specified value to Watchdog Register.

*NOTE: A (re-)configuration of the watchdog unit does not influence the watchdog timer! For resetting the watchdog timer the signature 0x55 must be written to the watchdog register in the configured time window. That means within the configured open/closed watchdog timing range.*

Table 54.   Watchdog Register Table

| Register Name | Address | Description |
|---|---|---|
| WDREG | 0x0001 | Watchdog Register |

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E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Table 55.   Watchdog Register

| WDREG (0x0001) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | WDCFG | WDM[1] | WDM[0] | WDPRE | - | - | - | - |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | W | R/W | R/W | R/W | R | R | R | R |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **WDCFG** :  Configure Watchdog $1_b$: Current write access is used to configure the watchdog mode<br><br>$0_b$: Watchdog is triggered if the value being written is 0x55<br>**WDM[1,0]**  if watchdog config. is (WDCFG=1) then WDREG[6:5] contains the selected Mode:<br><br>$00_b$ : Simple Time-Out Watchdog<br>$01_b$ : Window Watchdog1<br>$10_b$ : Window Watchdog2<br>$11_b$ : Window Watchdog3<br>**WDPRE** : Watchdog clock pre-divider | | | | | | | |

Table 56.   Watchdog Window Settings Description WDPRE = 0

| WDM[1:0] | Start window (number of clocks) | Start window (number of clocks) | Time for $f_{BUS}$ = 8 MHz /µs |
|---|---|---|---|
| 00 | 0 | 2048 | 0-256 |
| 01 | 256 | 2048 | 32-256 |
| 10 | 256 | 1024 | 32-128 |
| 11 | 512 | 2048 | 64-256 |

Table 57.   Watchdog Window Settings Description WDPRE = 1

| WDM[1:0] | Start window (number of clocks) | Start window (number of clocks) | Time for $f_{BUS}$ = 8 MHz /µs |
|---|---|---|---|
| 00 | 0 | 65536 | 0-8192 |
| 01 | 8192 | 65536 | 1024-8192 |
| 10 | 8192 | 32786 | 1024-4096 |
| 11 | 16384 | 65536 | 2048-8192 |

## 7.10  Counter

The timer is implemented as a 16 bit free running counter. To ensure the readout of consistent timer values the timer low byte is latched if the timer high byte is read. The compare register can be used to generated defined timer compare interrupts.

- Counter overflow flag (OTF) is cleared by writing a logical '1' into bit TOF of counter status register CNTSTAT.

- Compare overflow flag (OCF) is cleared by reading register CNTCMPL.
- Interrupts may be enabled by setting bit INTD to a logical '0' and bits OCIE/TFOI of control register CNTCTRL.
- In order to use interrupts an interrupt enable command CLI should be performed.
- Interrupts are disabled by STI command.

Table 58.   Counter Register Table

| Register Name | Address | Description |
|---|---|---|
| CNTH | 0x0022 | Counter High Byte Register |
| CNTL | 0x0023 | Counter Low Byte Register |
| CNTCMPH | 0x0024 | Counter Compare High Byte Register |
| CNTCMPL | 0x0025 | Counter Compare Low Byte Register |
| CNTCTRL | 0x0026 | Counter Control Register |
| CNTSTAT | 0x0027 | Counter Status Register |

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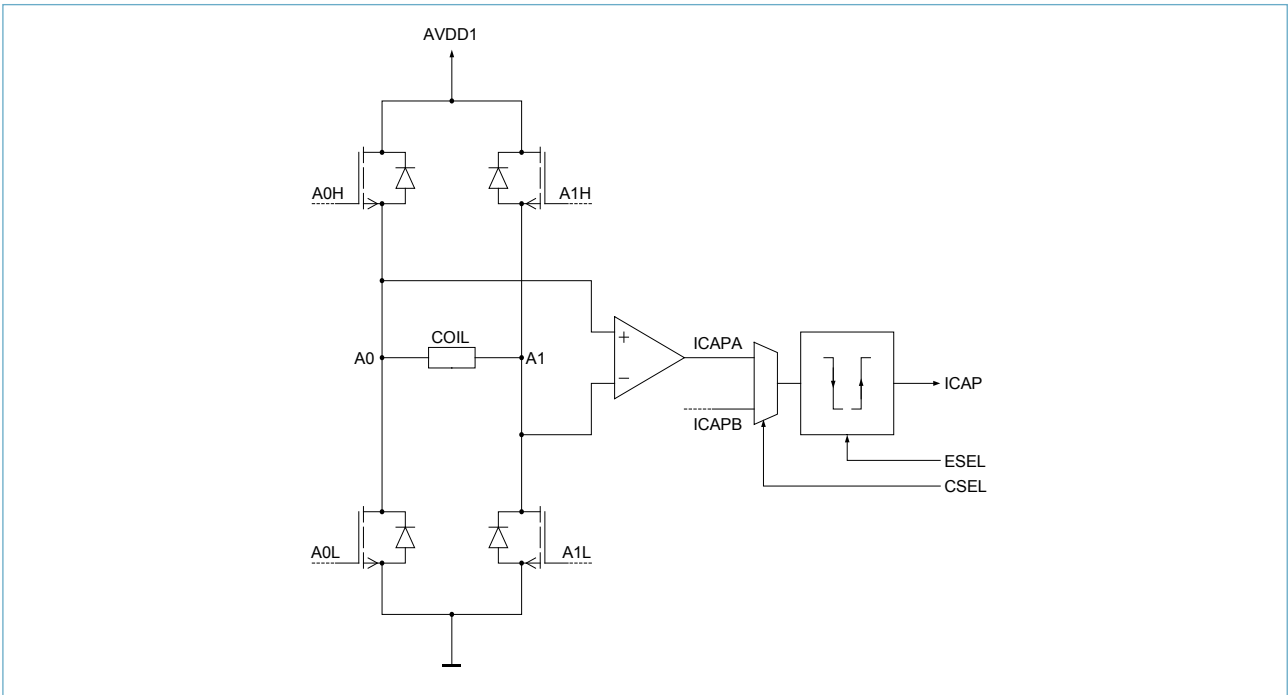
Table 59.    Counter high byte register

| CNTH (0x0022) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | TR[15] | TR[14] | TR[13] | TR[12] | TR[11] | TR[10] | TR[9] | TR[8] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R | R | R | R | R | R | R | R |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **TR[15:8]** : high byte of timer register , access latches TIM1RL | | | | | | | |

Table 60.    Counter low byte register

| CNTL (0x0023) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | TR[7] | TR[6] | TR[5] | TR[4] | TR[3] | TR[2] | TR[1] | TR[0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R | R | R | R | R | R | R | R |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **TR[7:0]** : low byte of timer register | | | | | | | |

Table 61.    Counter compare high byte register

| CNTCMPH (0x0024) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | TCMP[15] | TCMP[14] | TCMP[13] | TCMP[12] | TCMP[11] | TCMP[10] | TCMP[9] | TCMP[8] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **TCMP[15:8]** : high byte of timer compare register | | | | | | | |

Table 62.    Counter compare low byte register

| CNTCMPL (0x0025) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | TCMP[7] | TCMP[6] | TCMP[5] | TCMP[4] | TCMP[3] | TCMP[2] | TCMP[1] | TCMP[0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **TCMP[7:0]** : low byte of timer compare register | | | | | | | |

Table 63.    Counter control register

| CNTCTRL (0x0026) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | - | OCIE | TOFIE | INTD | - | PRE[1] | PRE[0] | - |
| Reset value | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Internal access | R | R/W | R/W | R/W | R | R/W | R/W | R |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **OCIE** : interrupt enable for output compare<br>**TOFIE** : interrupt enable for counter overflow<br>**INTD** : interrupt disable for all counter interrupts<br>1 : disables all<br>**PRE[1:0]** : selects the pre-scaler for the timer register<br>00 : counter incremented with $f_{osc}$ / 2<br>01 : counter incremented with $f_{osc}$ / 4<br>10 : counter incremented with $f_{osc}$ / 8<br>11 : counter incremented with $f_{osc}$ / 16 | | | | | | | |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Table 64.  Counter status register

| CNTSTAT (0x0027) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | - | OCF | TOF | - | - | - | - | - |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R | R | R/W | R | R | R | R | R |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | OCF : flag for output compare :<br>- set by timer hardware when values of CNTH/CNTL and of CNTCMPH/CNTCMPL register match. No further comparison is made until the OCF bit is cleared by reading of the CNTC-MPL register.<br>TOF : flag for counter overflow :<br>- set by counter hardware<br>- cleared by writing a '1' to TOF bit | | | | | | | |

## 7.11  Integrated µC ( CPU ) with RAM, ROM, FLASH , EEPROM

## 7.12  Central Processing Unit (CPU)

The range of CPU functions is:
- Control of peripherals such as LIN transceiver, PWM interface,
- Hall and potentiometer analysis,
- Stepper motor control.

The CPU may be reset by any of these sources:
- Power-on,
- Under-voltage at VDDD or VDDA,
- Internal watchdog timeout.

The CPU may be interrupted by any of these sources:
- Software interrupt instruction (SWI),
- SCI interface,
- EEPROM,
- GPIO pins,
- Timer.
- Motor controller.

Two different versions are available. The first one has 8KByte FLASH memory for application programs and 4KByte ROM for system routines (SysROM). The second version has 8KByte ROM for application software and

4KByte SysROM.

### Device Operation Modes
The CPU provides two different device operation modes:

### Configuration mode
1. Self test mode 2. Production test support
3. Adjustment setting
4. Programming of customer memory area via LIN protocol

### Operational mode
1. LIN or PWM protocol processing
2. Stepper motor control
3. Error detection and handling

After power-on reset the IC is in the configuration mode. It may be switched to operation mode by writing the value 0xA5 to the CPU Mode Register.

Table 65.  CPU Mode Register Table

| Register Name | Address | Description |
|---|---|---|
| CPUMOD | 0x0400 | CPU Mode Register |

Table 66.  CPU Mode Register

| CPUMOD (0x0400) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | MODCFG[7] | MOD-CFG[6] | MOD-CFG[5] | MOD-CFG[4] | MOD-CFG[3] | MOD-CFG[2] | MOD-CFG[1] | MOD-CFG[0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | W | W | W | W | W | W | W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | MODCFG[7] : current device state   0:configuration mode,   1:operational mode<br>MODECFG[7:0]: write 0xA5 to switch from configuration to operational mode | | | | | | | |

*Elmos Semiconductor AG reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.*

**Memory Map - Base Address Table**

The memory map is designed to provide both configuration and operational modes. It is achieved by switching of memory addresses as shown in (Figure 20 Memory Map of 8KByte FLASH Version) .

**Wake-up:**

The μC always starts in configuration mode after wake-up (Boot Manager Module is started). In this mode the FLASH firmware memory (only the FLASH version of the IC) or EEPROM cells can be erased/programmed via LIN2.1. After power-on reset the memory map for con-figuration mode is valid.

**Switching to operational mode:**

The device changes to operational mode either after a timeout or after receiving a bmmcommand_CLOSE message. In operational mode only the highest 16 bytes of EEPROM are erasable/programmable. FLASH access is read-only in this mode.

According to this mode switching, the memory spaces of the customer programmable FLASH firmware memory/ROM and the SysROM are modified as shown in (Figure 20 Memory Map of 8KByte FLASH Version) .
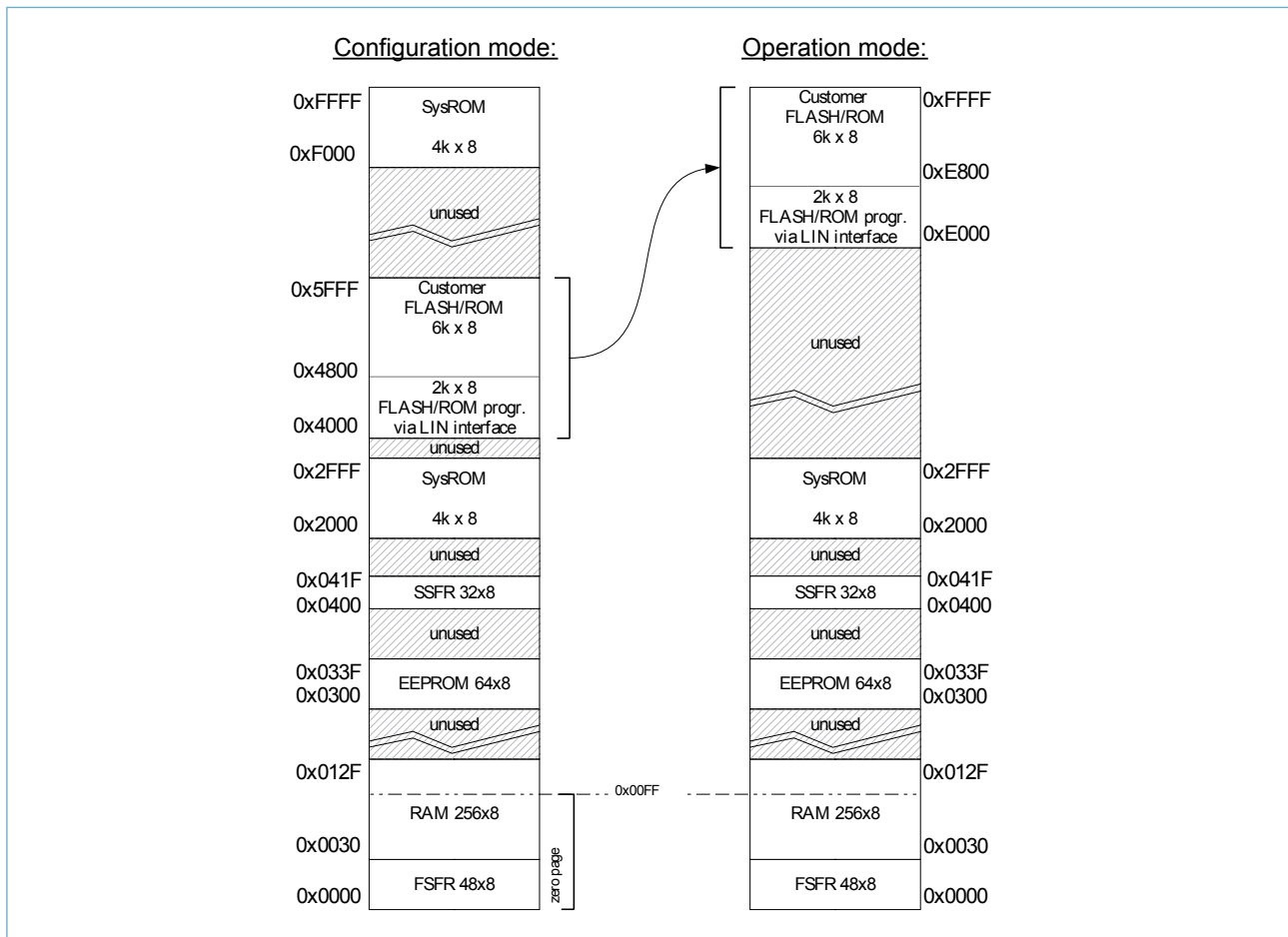


*Figure 20.   Memory Map of 8KByte FLASH Version*

Table 67.   Base Address Table of Operational Mode for 8KByte FLASH Version

| Base Address | Size | Module Name |
|---|---|---|
| 0xE000 | 0x2000 | FLASH 8K X 8 or AppROM |
| 0x3000 | 0xB000 | unused |
| 0x2000 | 0x1000 | SysROM 4K X 8 |
| 0x0420 | 0x1BE0 | unused |
| 0x0400 | 0x0020 | SSFR 32x8 |
| 0x0340 | 0x00C0 | unused |
| 0x0300 | 0x0040 | EEPROM 64 X 8 |
| 0x0130 | 0x01D0 | unused |
| 0x0030 | 0x0100 | RAM 256 X 8 |
| 0x0000 | 0x0030 | FSFR 48 X 8 |

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E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Table 68.  Base Address Table of Configuration Mode for 8KByte FLASH Version

| Base Address | Size | Module Name |
|---|---|---|
| 0xF000 | 0x1000 | SysROM 4K X 8 |
| 0x6000 | 0x9000 | unused |
| 0x4000 | 0x2000 | FLASH 8K X 8 or AppROM |
| 0x3000 | 0x1000 | unused |
| 0x2000 | 0x1000 | SysROM 4K X 8 |
| 0x0420 | 0x1BE0 | unused |
| 0x0400 | 0x0020 | SSFR 32x8 |
| 0x0340 | 0x00C0 | unused |
| 0x0300 | 0x0040 | EEPROM 64 X 8 |
| 0x0130 | 0x01D0 | unused |
| 0x0030 | 0x0100 | RAM 256 X 8 |
| 0x0000 | 0x0030 | FSFR 48 X 8 |

Table 69.  SFR Address Table

| Base Address | Size | Module Name |
|---|---|---|
| 0x0411 | STLFTHR | Motor Control |
| 0x0410 | FLASH_KEY4 | FLASH |
| 0x040f | FLASH_KEY3 | FLASH |
| 0x040e | FLASH_KEY2 | FLASH |
| 0x040d | FLASH_KEY1 | FLASH |
| 0x040c | FLASH_KEY_OK | FLASH |
| 0x0408 | RESSTAT | DIGITAL |
| 0x0404 | EE64IRQ | EEPROM |
| 0x0403 | GPIOCFG | GPIO Interface |
| 0x0402 | PWMCFG | PWM Interface |
| 0x0401 | GENCFG | Periphery |
| 0x0400 | CPUMOD | CPU |
| 0x0402 | PWMCFG | PWM Interface |
| 0x0401 | GENCFG | Periphery |
| 0x0400 | CPUMOD | CPU |
| 0x002F | MOTSTAT | Motor Control |
| 0x002E | ONTIME | Motor Control |
| 0x002D | DECCTRL | Motor Control |
| 0x002C | IDACB | Motor Control |
| 0x002B | IDACA | Motor Control |
| 0x002A | HBSTATUS | Motor Control |
| 0x0029 | HBDATA | Motor Control |
| 0x0028 | HBCTRL | Motor Control |
| 0x0027 | CNTSTAT | Counter |
| 0x0026 | CNTCTRL | Counter |
| 0x0025 | CNTCMPL | Counter |
| 0x0024 | CNTCMPH | Counter |
| 0x0023 | CNTL | Counter |
| 0x0022 | CNTH | Counter |
| 0x0021 | ADCDAT | ADC |
| 0x0020 | ADCCNTR | ADC |
| 0x001F | LINAA | BUS Interface |
| 0x001E | LIN_MODE | SCI |
| 0x001B | SCIMEASDATL | SCI |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

| Base Address | Size | Module Name |
|---|---|---|
| 0x001A | SCIMEASDATH | SCI |
| 0x0019 | SCIMEASCTRL | SCI |
| 0x0018 | SCIMEASCTRH | SCI |
| 0x0017 | SCIDATA | SCI |
| 0x0015 | SCISTATL | SCI |
| 0x0014 | SCISTATH | SCI |
| 0x0013 | SCICTRL | SCI |
| 0x0011 | SCIBRL | SCI |
| 0x0010 | SCIBRH | SCI |
| 0x000F | STLFLVL | Motor Control |
| 0x000E | STLFINC | Motor Control |
| 0x000D | CNTFBC | Motor Control |
| 0x000C | PWMCTRL | PWM Interface |
| 0x000B | PWMHL | PWM Interface |
| 0x000A | PWMLH | PWM Interface |
| 0x0009 | FLECR | FLASH |
| 0x0008 | FLCR | FLASH |
| 0x0007 | EE64ECC | EEPROM |
| 0x0006 | EE64LKR | EEPROM |
| 0x0005 | EE64CSR | EEPROM |
| 0x0004 | EE64TST | EEPROM |
| 0x0003 | GPIOPUD | GPIO |
| 0x0002 | GPIO | GPIO |
| 0x0001 | WDREG | Watchdog |
| 0x0000 | STLDTHR | Motor Control |

**Interrupt vector**

The following table shows a summary of all interrupt sources and their vector addresses. The interrupt number represents the priority, the highest number has the highest priority.

Table 70.   Reset and Interrupt Vectors List

| Number | Block | Vector Address | Source |
|---|---|---|---|
| 15 | POR/WD | 0xFFFE - 0xFFFF | Power-on reset watchdog |
| 14 | CPU | 0xFFFC - 0xFFFD | Software interrupt (SWI) |
| 13 | EEPROM EE_ERR_IRQ | 0xFFFA - 0xFFFB | Wrong write sequence detected |
| 12 | EEPROM EE_READY_IRQ | 0xFFF8 - 0xFFF9 | Erase/programming finished |
| 11 | EEPROM EE_ECCERR_IRQ | 0xFFF6 - 0xFFF7 | ECC error detected |
| 10 | Counter Counter_OC_IRQ | 0xFFF4 - 0xFFF5 | Counter output compare |
| 9 | Counter Counter_OF_IRQ | 0xFFF2 - 0xFFF3 | Counter overflow |
| 8 | SCI SCI_BIE_IRQ PWM PWM_EIE_IRQ | 0xFFF0 - 0xFFF1 | LIN Break detected<br><br>PWM Edge detected |
| 7 | SCI SCI_MFIE_IRQ | 0xFFEE - 0xFFEF | LIN Measurement finished |
| 6 | SCI SCI_RIE_IRQ | 0xFFEC - 0xFFED | LIN Receive register full |

| Number | Block | Vector Address | Source |
|---|---|---|---|
| 5 | SCI SCI_TIE_IRQ | 0xFFEA - 0xFFEB | LIN Transmit register empty |
| 4 | GPIO GPIO_IRQ | 0xFFE8 - 0xFFE9 | GPIO edge event on D1-D3 |
| 3 | Motor Control ZC_IRQ | 0xFFE6 - 0xFFE7 | Zero Crossing comparator |
| 2 | Motor Control MOTPWM_IRQ | 0xFFE4 - 0xFFE5 | Start of new PWM frame |
| 1 | - | 0xFFE2 - 0xFFE3 | Reserved |
| 0 | - | 0xFFE0 - 0xFFE1 | Reserved |

**Software interrupt (SWI):**

A jump of the program counter to an unused ROM/ FLASH address has to lead to a software interrupt. So it is strongly recommended to fill all unused storage with the interrupt vector address of the software interrupt (see above).

**CPU EL3.5 Core**

1. 6805 instruction set compatible including 8 by 8 multiplication

2. 2. 15 interrupt vectors
3. 1 reset vector
4. 16 bit address bus width
5. 64 KByte data/program address space (0x0000 - 0xFFFF)
6. Clock frequency 8MHz
7. 6 bit stack pointer
8. 16 bit extended program counter
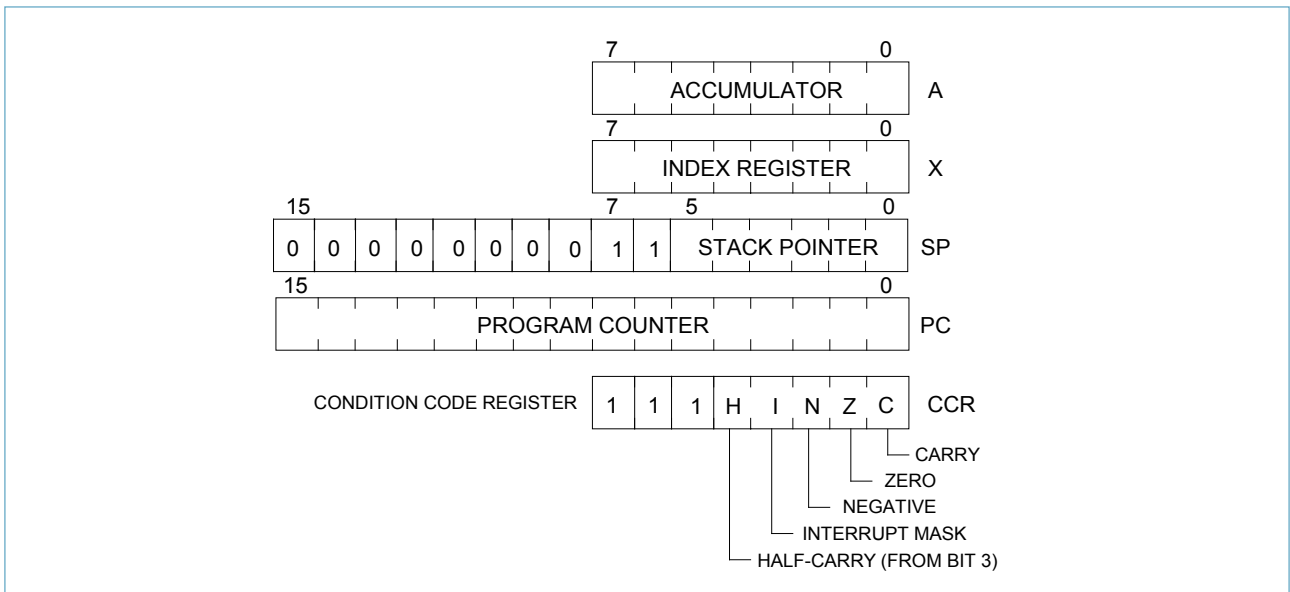


*Figure 21.   Programming Model*

**The EL3.5 CPU can be reset in variable ways:**
- by an initial power-on reset,
- by a watchdog reset,
- by a switching from configuration mode to operational mode.

Any of these resets will bring:
- the program counter to its starting address,
- all registers to their reset values,
- the interrupt mask bit set to interrupt disable,
- the stack pointer to 0x00FF.

The interrupt controller accepts several different interrupt sources. To accept interrupts the CCR I bit has to be cleared with the CLI instruction.

Please note that interrupt masking via CCR I bit does not disable the interrupt sources. It's only working as a masking. Before the reactivation interrupts again by clearing CCT I bit, it's recommended to clear possible interrupt events which may occurred during interrupt masking time.

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## Debug Interface

The IC supports debugging of the EL3.5 CPU. To access the debug structures of the EL3.5 CPU a 4-wire standard JTAG interface is used while the TESTEN pin is set to high level. Resetting TESTEN to low level resets all test and debug structures and the IC operates in normal mode.

## CPU Registers

The accumulator A is used for general calculations. The X register is used for indirect and indexed addressing. The stack pointer SP is used internally by the CPU. The first 2 bits of the SP register are fixed to one. This is to protect the rest of the RAM in case of a stack overflow. The program counter is 16 bit long. So the maximum addressable code area is 64KByte.

Table 71.  CPU Register Table

| Name | Size | Description |
|---|---|---|
| CCR | 5 bits | Condition Code Register |
| PC | 16 bits | Program Counter |
| SP | 6 bits | Stack Pointer |
| X | 8 bits | Index Register |
| A | 8 bits | Accumulator |
| STACK | 64 bytes | Stack 64 byte LIFO (last-in first-out) |

Table 72.  Condition Code Register

| Bit | Name | Description |
|---|---|---|
| 4 | H | Half-Carry (from bit 3) |
| 3 | I | Interrupt mask |
| 2 | N | Negative flag |
| 1 | Z | Zero flag |
| 0 | C | Carry bit |
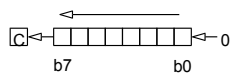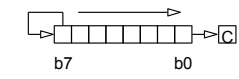
E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

*Elmos Semiconductor AG reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.*

## 7.13  Instruction Set

| Source Form | Operation | Description | Effect on CCR | | | | | Address Mode | Opcode | Operand | Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | H | I | N | Z | C | | | | |
| ADC #opr | | | | | | | | IMM | A9 | ii | 2 |
| ADC opr | | | | | | | | DIR | B9 | dd | 3 |
| ADC opr | | | | | | | | EXT | C9 | hh ll | 4 |
| ADC opr,X | Add with Carry | A ← (A) + (M) + (C) | $\updownarrow$ | — | $\updownarrow$ | $\updownarrow$ | $\updownarrow$ | IX2 | D9 | ee ff | 4 |
| ADC opr,X | | | | | | | | IX1 | E9 | ff | 4 |
| ADC ,X | | | | | | | | IX | F9 | | 3 |
| ADD #opr | | | | | | | | IMM | AB | ii | 2 |
| ADD opr | | | | | | | | DIR | BB | dd | 3 |
| ADD opr | | | | | | | | EXT | CB | hh ll | 4 |
| ADD opr,X | Add without Carry | A ← (A) + (M) | $\updownarrow$ | — | $\updownarrow$ | $\updownarrow$ | $\updownarrow$ | IX2 | DB | ee ff | 4 |
| ADD opr,X | | | | | | | | IX1 | EB | ff | 4 |
| ADD ,X | | | | | | | | IX | FB | | 3 |
| AND #opr | | | | | | | | IMM | A4 | ii | 2 |
| AND opr | | | | | | | | DIR | B4 | dd | 3 |
| AND opr | | | | | | | | EXT | C4 | hh ll | 4 |
| AND opr,X | Logical AND | A ← (A) $\wedge$ (M) | — | — | $\updownarrow$ | $\updownarrow$ | — | IX2 | D4 | ee ff | 4 |
| AND opr,X | | | | | | | | IX1 | E4 | ff | 4 |
| AND ,X | | | | | | | | IX | F4 | | 3 |
| ASL opr | | | | | | | | DIR | 38 | dd | 5 |
| ASLA | | | | | | | | INH | 48 | | 3 |
| ASLX | Arithmetic Shift Left (Same as LSL) | | — | — | $\updownarrow$ | $\updownarrow$ | $\updownarrow$ | INH | 58 | | 3 |
| ASL opr,X | | | | | | | | IX1 | 68 | ff | 6 |
| ASL ,X | | | | | | | | IX | 78 | | 5 |
| ASR opr | | | | | | | | DIR | 37 | dd | 5 |
| ASRA | | | | | | | | INH | 47 | | 3 |
| ASRX | Arithmetic Shift Right | | — | — | $\updownarrow$ | $\updownarrow$ | $\updownarrow$ | INH | 57 | | 3 |
| ASR opr,X | | | | | | | | IX1 | 67 | ff | 6 |
| ASR ,X | | | | | | | | IX | 77 | | 5 |
| BCC rel | Branch if Carry Bit Clear | PC ← (PC) + 2 +rel ?  C = 0 | — | — | — | — | — | REL | 24 | rr | 3 |
| | | | | | | | | DIR (b0) | 11 | dd | 5 |
| | | | | | | | | DIR (b1) | 13 | dd | 5 |
| | | | | | | | | DIR (b2) | 15 | dd | 5 |
| BCLR n opr | Clear Bit n | Mn ← 0 | — | — | — | — | — | DIR (b3) | 17 | dd | 5 |
| | | | | | | | | DIR (b4) | 19 | dd | 5 |
| | | | | | | | | DIR (b5) | 1B | dd | 5 |
| | | | | | | | | DIR (b6) | 1D | dd | 5 |
| | | | | | | | | DIR (b7) | 1F | dd | 5 |
| BCS rel | Branch if Carry Bit Set (Same as BLO) | PC ← (PC) + 2 +rel ?  C = 1 | — | — | — | — | — | REL | 25 | rr | 3 |
| BEQ rel | Branch if Equal | PC ← (PC) + 2 +rel ?  Z = 1 | — | — | — | — | — | REL | 27 | rr | 3 |
| BHCC rel | Branch if Half-Carry Bit Clear | PC ← (PC) + 2 +rel ?  H = 0 | — | — | — | — | — | REL | 28 | rr | 3 |
| BHCS rel | Branch if Half-Carry Bit Set | PC ← (PC) + 2 +rel ?  H = 1 | — | — | — | — | — | REL | 29 | rr | 3 |
| BHI rel | Branch if Higher | PC ← (PC) + 2 +rel ?  C $\vee$ Z = 0 | — | — | — | — | — | REL | 22 | rr | 3 |
| BHS rel | Branch if Higher or Same | PC ← (PC) + 2 +rel ?  C = 0 | — | — | — | — | — | REL | 24 | rr | 3 |

*Figure 22.   Instruction Set Summary (Sheet 1 of 6)*

| Source Form | Operation | Description | H | I | N | Z | C | Address Mode | Opcode | Operand | Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BIT #opr | | | | | | | | IMM | A5 | ii | 2 |
| BIT opr | | | | | | | | DIR | B5 | dd | 3 |
| BIT opr | Bit Test Accumulator with Memory Byte | (A) $\wedge$(M) | — | — | $\updownarrow$ | $\updownarrow$ | — | EXT | C5 | hh ll | 4 |
| BIT opr,X | | | | | | | | IX2 | D5 | ee ff | 4 |
| BIT opr,X | | | | | | | | IX1 | E5 | ff | 4 |
| BIT ,X | | | | | | | | IX | F5 | | 3 |
| BLO rel | Branch if Lower (Same as BCS) | PC ← (PC) + 2 +rel ? C = 1 | — | — | — | — | — | REL | 25 | rr | 3 |
| BLS rel | Branch ifLower orSame | PC ← (PC) + 2 +rel ? C $\vee$Z = 1 | — | — | — | — | — | REL | 23 | rr | 3 |
| BMC rel | Branch if Interrupt Mask Clear | PC ← (PC) + 2 +rel ? I = 0 | — | — | — | — | — | REL | 2C | rr | 3 |
| BMI rel | Branch if Minus | PC ← (PC) + 2 +rel ? N = 1 | — | — | — | — | — | REL | 2B | rr | 3 |
| BMS rel | Branch if Interrupt Mask Set | PC ← (PC) + 2 +rel ? I = 1 | — | — | — | — | — | REL | 2D | rr | 3 |
| BNE rel | Branch if Not Equal | PC ← (PC) + 2 +rel ? Z = 0 | — | — | — | — | — | REL | 26 | rr | 3 |
| BPL rel | Branch if Plus | PC ← (PC) + 2 +rel ? N = 0 | — | — | — | — | — | REL | 2A | rr | 3 |
| BRA rel | Branch Always | PC ← (PC) + 2 +rel ? 1 = 1 | — | — | — | — | — | REL | 20 | rr | 3 |
| BRCLR n opr rel | Branch if Bit n Clear | PC ← (PC) + 2 +rel ? Mn = 0 | — | — | — | — | $\updownarrow$ | DIR (b0) | 01 | dd rr | 5 |
| | | | | | | | | DIR (b1) | 03 | dd rr | 5 |
| | | | | | | | | DIR (b2) | 05 | dd rr | 5 |
| | | | | | | | | DIR (b3) | 07 | dd rr | 5 |
| | | | | | | | | DIR (b4) | 09 | dd rr | 5 |
| | | | | | | | | DIR (b5) | 0B | dd rr | 5 |
| | | | | | | | | DIR (b6) | 0D | dd rr | 5 |
| | | | | | | | | DIR (b7) | 0F | dd rr | 5 |
| BRN rel | Branch Never | PC ← (PC) + 2 +rel ? 1 = 0 | — | — | — | — | — | REL | 21 | rr | 3 |
| BRSET n opr rel | Branch if Bit n Set | PC ← (PC) + 2 +rel ? Mn = 1 | — | — | — | — | $\updownarrow$ | DIR (b0) | 00 | dd rr | 5 |
| | | | | | | | | DIR (b1) | 02 | dd rr | 5 |
| | | | | | | | | DIR (b2) | 04 | dd rr | 5 |
| | | | | | | | | DIR (b3) | 06 | dd rr | 5 |
| | | | | | | | | DIR (b4) | 08 | dd rr | 5 |
| | | | | | | | | DIR (b5) | 0A | dd rr | 5 |
| | | | | | | | | DIR (b6) | 0C | dd rr | 5 |
| | | | | | | | | DIR (b7) | 0E | dd rr | 5 |
| BSET n opr | Set Bit n | Mn ← 1 | — | — | — | — | — | DIR (b0) | 10 | dd | 5 |
| | | | | | | | | DIR (b1) | 12 | dd | 5 |
| | | | | | | | | DIR (b2) | 14 | dd | 5 |
| | | | | | | | | DIR (b3) | 16 | dd | 5 |
| | | | | | | | | DIR (b4) | 18 | dd | 5 |
| | | | | | | | | DIR (b5) | 1A | dd | 5 |
| | | | | | | | | DIR (b6) | 1C | dd | 5 |
| | | | | | | | | DIR (b7) | 1E | dd | 5 |
| BSR rel | Branch to Subroutine | PC ← (PC) + 2; push (PCL)<br>SP ← (SP) – 1; push (PCH)<br>SP ← (SP) – 1<br>PC ← (PC) +rel | — | — | — | — | — | REL | AD | rr | 6 |
| CLC | Clear Carry Bit | C ← 0 | — | — | — | — | 0 | INH | 98 | | 2 |
| CLI | Clear Interrupt Mask | I ← 0 | — | 0 | — | — | — | INH | 9A | | 2 |

*Figure 23.  Instruction Set Summary (Sheet 2 of 6)*

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Elmos Semiconductor AG          Data Sheet          QM-No.: 25DS0115E.01

| Source Form | Operation | Description | Effect on CCR | | | | | Address Mode | Opcode | Operand | Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | H | I | N | Z | C | | | | |
| CLR opr | | M ← $00 | | | | | | DIR | 3F | dd | 5 |
| CLRA | | A ← $00 | | | | | | INH | 4F | | 3 |
| CLRX | Clear Byte | X ← $00 | — | — | 0 | 1 | — | INH | 5F | | 3 |
| CLR opr,X | | M ← $00 | | | | | | IX1 | 6F | ff | 6 |
| CLR ,X | | M ← $00 | | | | | | IX | 7F | | 5 |
| CMP #opr | | | | | | | | IMM | A1 | ii | 2 |
| CMP opr | | | | | | | | DIR | B1 | dd | 3 |
| CMP opr | Compare Accumulator with Memory Byte | (A) – (M) | — | — | ↕ | ↕ | ↕ | EXT | C1 | hh ll | 4 |
| CMP opr,X | | | | | | | | IX2 | D1 | ee ff | 5 |
| CMP opr,X | | | | | | | | IX1 | E1 | ff | 4 |
| CMP ,X | | | | | | | | IX | F1 | | 3 |
| COM opr | | M ← ($\overline{M}$) = $FF – (M) | | | | | | DIR | 33 | dd | 5 |
| COMA | | A ← ($\overline{A}$) = $FF – (A) | | | | | | INH | 43 | | 3 |
| COMX | Complement Byte (One's Complement) | X ← ($\overline{X}$) = $FF – (X) | — | — | ↕ | ↕ | 1 | INH | 53 | | 3 |
| COM opr,X | | M ← ($\overline{M}$) = $FF – (M) | | | | | | IX1 | 63 | ff | 6 |
| COM ,X | | M ← ($\overline{M}$) = $FF – (M) | | | | | | IX | 73 | | 5 |
| CPX #opr | | | | | | | | IMM | A3 | ii | 2 |
| CPX opr | | | | | | | | DIR | B3 | dd | 3 |
| CPX opr | Compare Index Register with Memory Byte | (X) – (M) | — | — | ↕ | ↕ | ↕ | EXT | C3 | hh ll | 4 |
| CPX opr,X | | | | | | | | IX2 | D3 | ee ff | 5 |
| CPX opr,X | | | | | | | | IX1 | E3 | ff | 4 |
| CPX ,X | | | | | | | | IX | F3 | | 3 |
| DEC opr | | M ← (M) – 1 | | | | | | DIR | 3A | dd | 5 |
| DECA | | A ← (A) – 1 | | | | | | INH | 4A | | 3 |
| DECX | Decrement Byte | X ← (X) – 1 | — | — | ↕ | ↕ | — | INH | 5A | | 3 |
| DEC opr,X | | M ← (M) – 1 | | | | | | IX1 | 6A | ff | 6 |
| DEC ,X | | M ← (M) – 1 | | | | | | IX | 7A | | 5 |
| EOR #opr | | | | | | | | IMM | A8 | ii | 2 |
| EOR opr | | | | | | | | DIR | B8 | dd | 3 |
| EOR opr | EXCLUSIVE OR Accumulator with Memory Byte | A ← (A) ⊕ (M) | — | — | ↕ | ↕ | — | EXT | C8 | hh ll | 4 |
| EOR opr,X | | | | | | | | IX2 | D8 | ee ff | 5 |
| EOR opr,X | | | | | | | | IX1 | E8 | ff | 4 |
| EOR ,X | | | | | | | | IX | F8 | | 3 |
| INC opr | | M ← (M) + 1 | | | | | | DIR | 3C | dd | 5 |
| INCA | | A ← (A) + 1 | | | | | | INH | 4C | | 3 |
| INCX | Increment Byte | X ← (X) + 1 | — | — | ↕ | ↕ | — | INH | 5C | | 3 |
| INC opr,X | | M ← (M) + 1 | | | | | | IX1 | 6C | ff | 6 |
| INC ,X | | M ← (M) + 1 | | | | | | IX | 7C | | 5 |
| JMP opr | | | | | | | | DIR | BC | dd | 2 |
| JMP opr | | | | | | | | EXT | CC | hh ll | 3 |
| JMP opr,X | Unconditional Jump | PC ← Jump Address | — | — | — | — | — | IX2 | DC | ee ff | 4 |
| JMP opr,X | | | | | | | | IX1 | EC | ff | 3 |
| JMP ,X | | | | | | | | IX | FC | | 2 |

*Figure 24.   Instruction Set Summary (Sheet 3 of 6)*
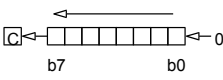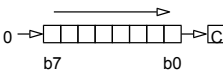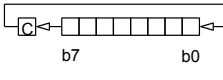
| Source Form | Operation | Description | H | I | N | Z | C | Address Mode | Opcode | Operand | Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|
| JSR opr<br>JSR opr<br>JSR opr,X<br>JSR opr,X<br>JSR ,X | Jump to Subroutine | PC ← (PC) + n (n = 1, 2, or 3)<br>Push (PCL); SP ← (SP) – 1<br>Push (PCH); SP ← (SP) – 1<br>PC ← Effective Address | — | — | — | — | — | DIR<br>EXT<br>IX2<br>IX1<br>IX | BD<br>CD<br>DD<br>ED<br>FD | dd<br>hh ll<br>ee ff<br>ff | 5<br>6<br>6<br>6<br>5 |
| LDA #opr<br>LDA opr<br>LDA opr<br>LDA opr,X<br>LDA opr,X<br>LDA ,X | Load Accumulator with Memory Byte | A ← (M) | — | — | ↕ | ↕ | — | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX | A6<br>B6<br>C6<br>D6<br>E6<br>F6 | ii<br>dd<br>hh ll<br>ee ff<br>ff | 2<br>3<br>4<br>4<br>4<br>3 |
| LDX #opr<br>LDX opr<br>LDX opr<br>LDX opr,X<br>LDX opr,X<br>LDX ,X | Load Index Register with Memory Byte | X ← (M) | — | — | ↕ | ↕ | — | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX | AE<br>BE<br>CE<br>DE<br>EE<br>FE | ii<br>dd<br>hh ll<br>ee ff<br>ff | 2<br>3<br>4<br>4<br>4<br>3 |
| LSL opr<br>LSLA<br>LSLX<br>LSL opr,X<br>LSL ,X | Logical Shift Left (Same as ASL) |  | — | — | ↕ | ↕ | ↕ | DIR<br>INH<br>INH<br>IX1<br>IX | 38<br>48<br>58<br>68<br>78 | dd<br><br><br>ff | 5<br>3<br>3<br>6<br>5 |
| LSR opr<br>LSRA<br>LSRX<br>LSR opr,X<br>LSR ,X | Logical Shift Right |  | — | — | 0 | ↕ | ↕ | DIR<br>INH<br>INH<br>IX1<br>IX | 34<br>44<br>54<br>64<br>74 | dd<br><br><br>ff | 5<br>3<br>3<br>6<br>5 |
| MUL | Unsigned Multiply | X : A ← (X) × (A) | 0 | — | — | — | 0 | INH | 42 | | 11 |
| NEG opr<br>NEGA<br>NEGX<br>NEG opr,X<br>NEG ,X | Negate Byte (Two's Complement) | M ← –(M) = $00 – (M)<br>A ← –(A) = $00 – (A)<br>X ← –(X) = $00 – (X)<br>M ← –(M) = $00 – (M)<br>M ← –(M) = $00 – (M) | — | — | ↕ | ↕ | ↕ | DIR<br>INH<br>INH<br>IX1<br>IX | 30<br>40<br>50<br>60<br>70 | dd<br><br><br>ff | 5<br>3<br>3<br>6<br>5 |
| NOP | No Operation | | — | — | — | — | — | INH | 9D | | 2 |
| ORA #opr<br>ORA opr<br>ORA opr<br>ORA opr,X<br>ORA opr,X<br>ORA ,X | Logical OR Accumulator with Memory | A ← (A) ∨ (M) | — | — | ↕ | ↕ | — | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX | AA<br>BA<br>CA<br>DA<br>EA<br>FA | ii<br>dd<br>hh ll<br>ee ff<br>ff | 2<br>3<br>4<br>4<br>4<br>3 |
| ROL opr<br>ROLA<br>ROLX<br>ROL opr,X<br>ROL ,X | Rotate Byte Left through Carry Bit |  | — | — | ↕ | ↕ | ↕ | DIR<br>INH<br>INH<br>IX1<br>IX | 39<br>49<br>59<br>69<br>79 | dd<br><br><br>ff | 5<br>3<br>3<br>6<br>5 |

*Figure 25. Instruction Set Summary (Sheet 4 of 6)*

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B
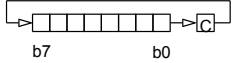
| Source Form | Operation | Description | Effect on CCR | | | | | Address Mode | Opcode | Operand | Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | H | I | N | Z | C | | | | |
| ROR opr<br>RORA<br>RORX<br>ROR opr,X<br>ROR ,X | Rotate Byte Right through Carry Bit |  | — | — | ↕ | ↕ | ↕ | DIR<br>INH<br>INH<br>IX1<br>IX | 36<br>46<br>56<br>66<br>76 | dd<br><br><br>ff<br> | 5<br>3<br>3<br>6<br>5 |
| RSP | Reset Stack Pointer | SP ← $00FF | — | — | — | — | — | INH | 9C | | 2 |
| RTI | Return from Interrupt | SP ← (SP) + 1; Pull (CCR)<br>SP ← (SP) + 1; Pull (A)<br>SP ← (SP) + 1; Pull (X)<br>SP ← (SP) + 1; Pull (PCH)<br>SP ← (SP) + 1; Pull (PCL) | ↕ | ↕ | ↕ | ↕ | ↕ | INH | 80 | | 9 |
| RTS | Return from Subroutine | SP ← (SP) + 1; Pull (PCH)<br>SP ← (SP) + 1; Pull (PCL) | — | — | — | — | — | INH | 81 | | 6 |
| SBC #opr<br>SBC opr<br>SBC opr<br>SBC opr,X<br>SBC opr,X<br>SBC ,X | Subtract Memory Byte and Carry Bit from Accumulator | A ← (A) − (M) − (C) | — | — | ↕ | ↕ | ↕ | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX | A2<br>B2<br>C2<br>D2<br>E2<br>F2 | ii<br>dd<br>hh ll<br>ee ff<br>ff<br> | 2<br>3<br>4<br>4<br>4<br>3 |
| SEC | Set Carry Bit | C ← 1 | — | — | — | — | 1 | INH | 99 | | 2 |
| SEI | Set Interrupt Mask | I ← 1 | — | 1 | — | — | — | INH | 9B | | 2 |
| STA opr<br>STA opr<br>STA opr,X<br>STA opr,X<br>STA ,X | Store Accumulator in Memory | M ← (A) | — | — | ↕ | ↕ | — | DIR<br>EXT<br>IX2<br>IX1<br>IX | B7<br>C7<br>D7<br>E7<br>F7 | dd<br>hh ll<br>ee ff<br>ff<br> | 4<br>5<br>5<br>5<br>4 |
| STX opr<br>STX opr<br>STX opr,X<br>STX opr,X<br>STX ,X | Store Index Register In Memory | M ← (X) | — | — | ↕ | ↕ | — | DIR<br>EXT<br>IX2<br>IX1<br>IX | BF<br>CF<br>DF<br>EF<br>FF | dd<br>hh ll<br>ee ff<br>ff<br> | 3<br>4<br>4<br>4<br>3 |
| SUB #opr<br>SUB opr<br>SUB opr<br>SUB opr,X<br>SUB opr,X<br>SUB ,X | Subtract Memory Byte from Accumulator | A ← (A) − (M) | — | — | ↕ | | ↕ | IMM<br>DIR<br>EXT<br>IX2<br>IX1<br>IX | A0<br>B0<br>C0<br>D0<br>E0<br>F0 | ii<br>dd<br>hh ll<br>ee ff<br>ff<br> | 2<br>3<br>4<br>4<br>4<br>3 |

*Figure 26.   Instruction Set Summary (Sheet 5 of 6)*

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

| Source Form | Operation | Description | Effect on CCR | | | | | Address Mode | Opcode | Operand | Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | H | I | N | Z | C | | | | |
| SWI | Software Interrupt | PC ← (PC) + 1; Push (PCL)<br>SP ← (SP) – 1; Push (PCH)<br>SP ← (SP) – 1; Push (X)<br>SP ← (SP) – 1; Push (A)<br>SP ← (SP) – 1; Push (CCR)<br>SP ← (SP) – 1; I ← 1<br>PCH ← Interrupt Vector High Byte<br>PCL ← Interrupt Vector Low Byte | — | 1 | — | — | — | INH | 83 | | 10 |
| TAX | Transfer Accumulator to Index Register | X ← (A) | — | — | — | — | — | INH | 97 | | 2 |
| TSTopr | | | — | — | ↕ | | ↕ | DIR | 3D | dd | 4 |
| TSTA | | | | | | | | INH | 4D | | 3 |
| TSTX | Test Memory Byte for Negative or Zero | (M) – $00 | | | | | | INH | 5D | | 3 |
| TSTopr,X | | | | | | | | IX1 | 6D | ff | 5 |
| TST ,X | | | | | | | | IX | 7D | | 4 |
| TXA | Transfer Index Register to Accumulator | A ← (X) | — | — | — | — | — | INH | 9F | | 2 |

| | | | | |
|---|---|---|---|---|
| A | Accumulator | | opr | Operand (one or two bytes) |
| C | Carry/borrow flag | | PC | Program counter |
| CCR | Condition code register | | PCH | Program counter high byte |
| dd | Direct address of operand | | PCL | Program counter low byte |
| dd rr | Direct address of operand and relative offset of branch instruction | | REL | Relative addressing mode |
| DIR | Direct addressing mode | | rel | Relative program counter offset byte |
| ee ff | High and low bytes of offset in indexed, 16-bit offset addressing | | rr | Relative program counter offset byte |
| EXT | Extended addressing mode | | SP | Stack pointer |
| ff | Offset byte in indexed, 8-bit offset addressing | | X | Index register |
| H | Half-carry flag | | Z | Zero flag |
| hh ll | High and low bytes of operand address in extended addressing | | # | Immediate value |
| I | Interrupt mask | | ∧ | Logical AND |
| ii | Immediate operand byte | | ∨ | Logical OR |
| IMM | Immediate addressing mode | | ⊕ | Logical EXCLUSIVE OR |
| INH | Inherent addressing mode | | ( ) | Contents of |
| IX | Indexed, no offset addressing mode | | –( ) | Negation (two's complement) |
| IX1 | Indexed, 8-bit offset addressing mode | | ← | Loaded with |
| IX2 | Indexed, 16-bit offset addressing mode | | ? | If |
| M | Memory location | | : | Concatenated with |
| N | Negative flag | | ↕ | Set or cleared |
| n | Any bit | | — | Not affected |

*Figure 27.    Instruction Set Summary (Sheet 6 of 6)*

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B



Figure 28.   Instruction Set Op-code Map

Elmos Semiconductor AG reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

## 7.14  RAM

This Random Access Memory (RAM) module is a static volatile memory block. The module contains a 256 word by 8 bit RAM array. The RAM block has a synchronous read and write interface.

## 7.15  EEPROM

Characteristics of EEPROM:
- a nonvolatile reprogrammable memory,
- 64 word EEPROM with a word length of 12 bits (8 data bits + 4 ECC bits),
- erase/program access is limited to the upper 16 bytes in operational mode,
- single byte mode and all-in-one/two step mode for erase/programming,
- internal slew rate control of the programming pulses,
- internal voltage regulator for the programming/ erase voltage VPP.

The application has to guarantee safe operating conditions (e.g. temperature) for the duration of the erasing and programming.
For enhanced data integrity, the EEPROM is equipped with an error checking and correction hardware.
It is capable of correcting a single bit error and to detect a double bit error and can't be disabled. If the ECC code which is automatically calculated from the read data does not match the ECC code stored in the EEPROM cell, then the ECCERR bit in the EE64CSR register will be set and the interrupt EE_ECCERR_IRQ will be triggered (if not masked).

The access to the EEPROM adds 4 additional wait cycles for a read operation of the EL3.5.

For information regarding the number writing cycles, reliability and condition parameters please refer to the parameter table.

The EEPROM array is intended for customer configuration data, motor parameter and customer adjustment data. An additional array is available for chip adjustments. This array is protected in the normal operational mode.
There are two ways for programming of EEPROM, a single byte or all-in-one programming mode. There are auxiliary routines in SysROM space that provide both procedures. The writing of data can only be achieved to empty cells. So it is indispensable to erase the EEPROM space before writing to it.
The EEPROM erasing/programming voltage is generated internally. The EEPROM is secured from unintentional erasing/programming by a predetermined sequence of conditions.
Analog to its programming, the EEPROM may be erased in two ways, byte-wise or all at once. The erasing operations are available as SysROM routines.

Table 73.  EEPROM Control and Status Register Table

| Register Name | Address | Description |
|---|---|---|
| EE64CSR | 0x0005 | EEPROM Control and Status Register |
| EE64LKR | 0x0006 | EEPROM Lock Register |
| EE64ECC | 0x0007 | EEPROM Error Correction Code Register |
| EE64IRQ | 0x0404 | EEPROM Interrupt Configuration Register |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Table 74.   EEPROM Control and Status Register

| EE64CSR (0x0005) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | AL | PGM | ER | VHI | VLO | INFO | LOCK | ECCERR |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R | R |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **AL** : enables block write/erase<br>**PGM** : selects writing of memory during programming<br>**ER** : selects erasing of memory during programming<br>**VHI** : enables verify mode with high read voltage reference<br>**VLO** : enables verify mode with low read voltage reference<br>**INFO** : always write 0b<br>**LOCK** : status bit indicating, that erase/programming is in progress,<br>bit is set/reset by hardware, EE_READY_IRQ is cleared by writing 1b.<br>**ECCERR** : indicates, that the last EEPROM read-access contains an ECC error,<br>bit and EE_ECCERR_IRQ are cleared by writing 1b. | | | | | | | |

Table 75.   EEPROM Lock Register

| EE64LKR (0x0006) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | S[3] | S[2] | S[1] | S[0] | CNT[3:0] | CNT[3:0] | CNT[3:0] | CNT[3:0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R | R | R | R | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **S[3]** : counter parity<br>S3 = CNT1 xor CNT3<br>**S[2]** : S2 = CNT0 xor CNT2<br>**S[1]** : S1 = CNT2 xor CNT3<br>**S[0]** : S0 = CNT0 xor CNT1<br>**CNT[3:0]** : CNT[3:0] : lock counter<br>The EE64LKR register cannot be accessed via the JTAG interface. | | | | | | | |

Table 76.   EEPROM Error Correction Code Register

| EE64ECC (0x0007) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | - | - | - | - | ECC[3] | ECC[2] | ECC[1] | ECC[0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R | R | R | R | R | R | R | R |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **ECC[3:0]** : ECC[3:0] : single bit failure correction ECC<br>The ECC bits can be written by setting the bit ECC_OFF=1. Read access is available at any time.<br>The EE64ECC register cannot be accessed in the JTAG mode. | | | | | | | |

Table 77.   EEPROM Interrupt Configuration Register

| EE64IRQ (0x0404) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | - | - | - | - | - | - | - | EEIRQ_EN |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R | R | R | R | R | R | R | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **EEIRQ_EN** : enable bit for EEPROM interrupts EE_ERR_IRQ, EE_READY_IRQ and EE_ECCERR_IRQ<br>1 : interrupts enabled<br>0 : interrupts disabled | | | | | | | |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

```
                          ┌─────────┐
                          │  start  │
                          └─────────┘
                               │
                               ▼
                    ┌──────────────────────┐
                    │    reset EEPROM       │
                    │      counter          │
                    └──────────────────────┘
                               │ EE64LKR=0xA0
                               ▼
                    ┌──────────────────────┐
          ┌────────▶│   set  EEPROM counter │
          │         │    to value 0x0B      │
          │         └──────────────────────┘
          │                    │ EE64LKR=0x0A
  loop +1 │                    ▼
          │              ◇───────────◇
          └────── yes ───│  loop < 11 │
                         ◇───────────◇
                               │ no
                               ▼
                    ┌──────────────────────┐
                    │    write to  EEPROM   │
                    └──────────────────────┘
                               │ ee_data(ee_addr)=value
                               ▼
                    ┌──────────────────────┐
                    │   set EEPROM counter  │
                    │    to value 0x0C      │
                    └──────────────────────┘
                               │ EE64LKR=0x0A
                               ▼
                         ◇───────────◇
            yes ─────────│ erase/program│
             │           │  all bytes?  │
             ▼           ◇───────────◇
    ┌─────────────┐            │ no
    │ erase/program│           │
    │  all bytes   │           │
    └─────────────┘            │
     EE64CSR(AL)=1 ────────────┤
                               ▼
                         ◇───────────◇
          erase ─────────│    mode?    │───────── program
             │           ◇───────────◇              │
             ▼                                       ▼
    ┌─────────────┐                        ┌──────────────────┐
    │enable erase  │                       │enable program mode│
    │    mode      │                       └──────────────────┘
    └─────────────┘                         EE64CSR(PGM)=1
     EE64CSR(ER)=1                                 │
             │                                     │
             ▼                                     ▼
          ┌──────────────────────────┐
          │   wait for erasing/       │◀───────┐
          │ programming time period   │        │
          └──────────────────────────┘        │
                     │ EE64CSR(LOCK)           │
                     ▼                         │
              ◇─────────────────◇              │
              │ EE64CSR(LOCK)=0  │── no ────────┘
              ◇─────────────────◇
                     │ yes
                     ▼
          ┌──────────────────────┐
          │   disable erase/      │
          │  programming mode     │
          └──────────────────────┘
                     │ EE64CSR(PGM)=0 /
                     │ EE64CSR(ER)  =0 /
                     │ EE64CSR(AL)  =0
                     ▼
               ┌─────────┐
               │ finish  │
               └─────────┘
```
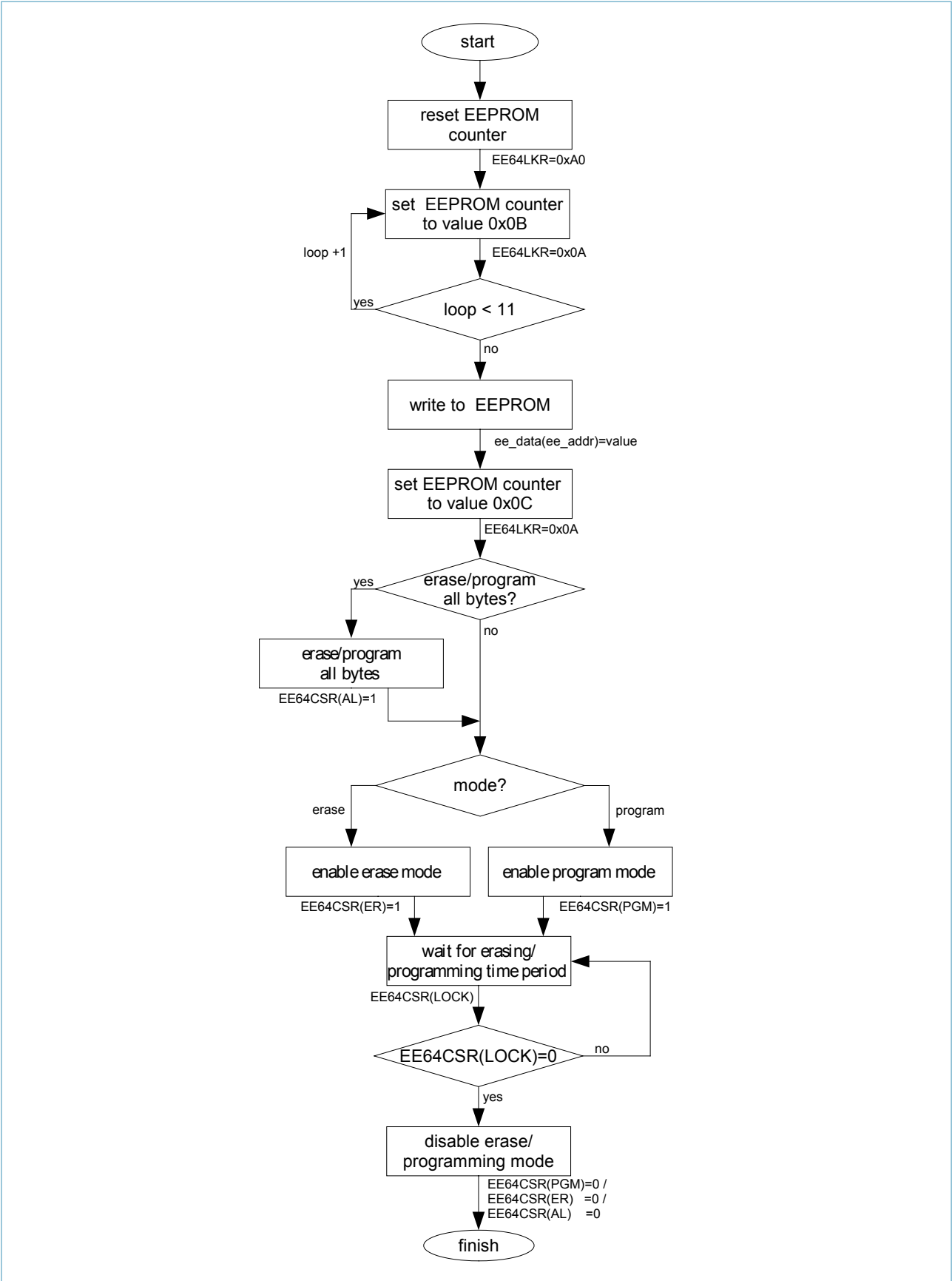
*Figure 29.   Flow of EEPROM Erasing/Programming*

## 7.16  FLASH (only available in IC types with included FLASH memory)

The device contains customer programmable FLASH firmware memory. For information regarding the number writing cycles, reliability and condition parameters please refer to the memory parameter table.
Characteristics of customer programmable FLASH firmware memory:

• nonvolatile memory,
• customer programmable FLASH firmware memory, in configuration mode or via JTAG interface
• read-only access in operational mode,
• programming up to 64 Bytes at once,
• mass erase mode,
• data verification for erased and programmed states.

Safe environment conditions must be guaranteed (especially supply voltage, programming time and temperature). Re-flashing is not allowed under automotive ambient conditions variations. Supply voltage and temperature should be in very controlled production limits. Re-flashing under (even temporarily) uncontrolled conditions can affect the data retention of the FLASH information and may lead to errors during re-flashing.

The supply voltage at the IC pin has to be in the range of 11..15V and must be free of noise and ripple and must never be interrupted during re-flash procedure. For re-flashing the IC temperature has to be between 0°C and 50°C. It's recommended to protocol the values for the ambient conditions during re-flashing.
The FLASH memory is programmable at end-of-line via JTAG interface or via LIN interface in configuration mode. The LIN re-flashing procedure is part of the boot manager module, located in the SysROM. Details of the re-flashing procedure can be found in the boot manager description. The re-flashing capability via LIN can be disabled via setting the configuration time to zero. It is strongly recommended to disable the re-flashing capability via LIN if not needed
For enhanced data integrity, the FLASH is equipped with an error checking and correction hardware. It is capable of correcting a single bit error and to detect a double bit error and can't be disabled. If the ECC code which is automatically calculated from the read data does not match the ECC code stored in the FLASH cell, then the ECCERR bit in the FLECR register will be set.

**32 bit security key for avoiding unwanted programming/ erasing:**

The FLASH memory may be programmed in two ways, via JTAG or via the CPU. A programming via JTAG can only be performed in JTAG flash mode.
The second way of programming via CPU is supported by software routines located in the SysROM area. The FLASH key and the data to be programmed are transmitted over LIN in this case. FLASH cells shall be erased before programming. The FLASH programming/erasing voltage is generated internally. This FLASH programming can be performed in configuration mode only. The flash is secured from unwanted programming/ erasing via CPU by an additional condition. A program-

ming/erasing process is only enabled if a 32 bit key was written and the FLASH_KEY_OK register was read. The key of 0x84913BAC must be written byte-wise in the correct order: FLASH_KEY3=0x91, FLASH_KEY2=0x3B, FLASH_KEY4=0x84 and at last FLASH_KEY1=0xAC (see below). Programming/erasing is then enabled until any byte of the key register is written again. After that the complete process must be done again. Otherwise an internal circuit provides erasing/programming of Flash is locked. It is strongly recommended not to store the key in the FLASH memory itself, it should be transmitted over LIN.

Table 78.   Flash programming/ erasing enable register

| Register Name | Address | Description |
| --- | --- | --- |
| FLASH_KEY_OK | 0x040C | Flash key status |
| FLASH_KEY1 | 0x040D | Flash key register 1 |
| FLASH_KEY2 | 0x040E | Flash key register 2 |
| FLASH_KEY3 | 0x040F | Flash key register 3 |
| FLASH_KEY4 | 0x0410 | Flash key register 4 |

Table 79. Flash key status

| FLASH_KEY_OK (0x040C) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | - | - | - | - | - | - | - | FLASH_KEY_OK |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | R | R | R | R | R | R | R | R |
| Bit Description | **FLASH_KEY_OK** : 1: The correct key was written in the correct order. Flash programming/erasing is now enabled. 0: The key or the sequence of writing was not correct | | | | | | | |

Table 80. Flash key register 1

| FLASH_KEY1 (0x040D) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | FLASH_KEY1 | - | - | - | - | - | - | - |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | W | W | W | W | W | W | W | W |
| Bit Description | **FLASH_KEY1** : bit [7:0] of the 32 bit key - 0xAC | | | | | | | |

Table 81. Flash key register 2

| FLASH_KEY2 (0x040E) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | FLASH_KEY2 | - | - | - | - | - | - | - |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | W | W | W | W | W | W | W | W |
| Bit Description | **FLASH_KEY2** : bit [15:8] of the 32 bit key - 0x3B | | | | | | | |

Table 82. Flash key register 3

| FLASH_KEY3 (0x040F) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | FLASH_KEY3 | - | - | - | - | - | - | - |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | W | W | W | W | W | W | W | W |
| Bit Description | **FLASH_KEY3** : bit [23:16] of the 32 bit key - 0x91 | | | | | | | |

Table 83. Flash key register 4

| FLASH_KEY4 (0x0410) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | FLASH_KEY4 | - | - | - | - | - | - | - |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | W | W | W | W | W | W | W | W |
| Bit Description | **FLASH_KEY4** : bit [31:24] oft the 32 bit key - 0x84 | | | | | | | |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

Table 84.  FLASH Control Register Table

| Register Name | Address | Description |
|---|---|---|
| FLCR | 0x0008 | FLASH Control Register |
| FLECR | 0x0009 | FLASH ECC Control Register |

Table 85.  FLASH Control Register

| FLCR (0x0008) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | PGM | MER2 | VERIFY | VERIFY1 | HVEN | BPGM | MER6 | Reserved |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **PGM** : Program control bit configures the memory for program operation.<br>**MER2** : Enables mass erase mode for customer 2k-FLASH. Data of the whole array will be cleared with next step.<br>**VERIFY** : Enables verify read mode for programmed cell state (logical '1').<br>**VERIFY1** : Enables verify read mode for erased cell state (logical '0').<br>**HVEN** : Enables high voltages for program/erase operation.<br>HVEN can only be set if either PGM = '1' or MER2 = '1' or MER6 = '1'.<br>**BPGM** : Enables bulk programming mode<br>**MER6** : Enables mass erase mode for customer 6k-FLASH. Data of the whole array will be cleared with next<br>**Reserved** : Always write logical '0' | | | | | | | |

Table 86.  FLASH ECC Control Register

| FLECR (0x0009) | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Content | ECCERR | BIT[6] | BIT[5] | BIT[4] | BIT[3] | BIT[2] | BIT[1] | BIT[0] |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Internal access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| External access | - | - | - | - | - | - | - | - |
| Bit Description | **ECCERR** : Indicates that a previous FLASH read-access contains an ECC error. Clear this bit by writing '1' into it.<br>**BIT[6]** : MSB of reserved bits.<br>**BIT[0]** : LSB of reserved bits.<br>Always write BIT[6:0]=0000000$_b$. | | | | | | | |

## 7.17 Test Controller

The IC can be set in test-mode with TESTEN at high. The tests are for production test purposes. They are not intended for customer usage, that means the test mode must be inactive in the application mode. To ensure proper operation of the IC, always connect the pin TESTEN to GND. When the test mode is active, the chip is controlled by the JTAG test pins. The different test modes are set up via the Instruction Register (IR) of the test controller. In test mode the clock can be controlled external by a special JTAG instruction, too. Two pulses on TCK are needed for switching internal clock net to the external clock on TCK. While the test mode is active, the chip can be reset with TSTRST at high. There are four additional JTAG pins in use, TCK (clock), TMS (select), TDI (data in) and TDO (data out). Figure below shows the state diagram of the JTAG TAP controller. By setting TMS and clocking TCK different states can be reached. For details on the JTAG test procedure, see IEEE-standard 1149.1.
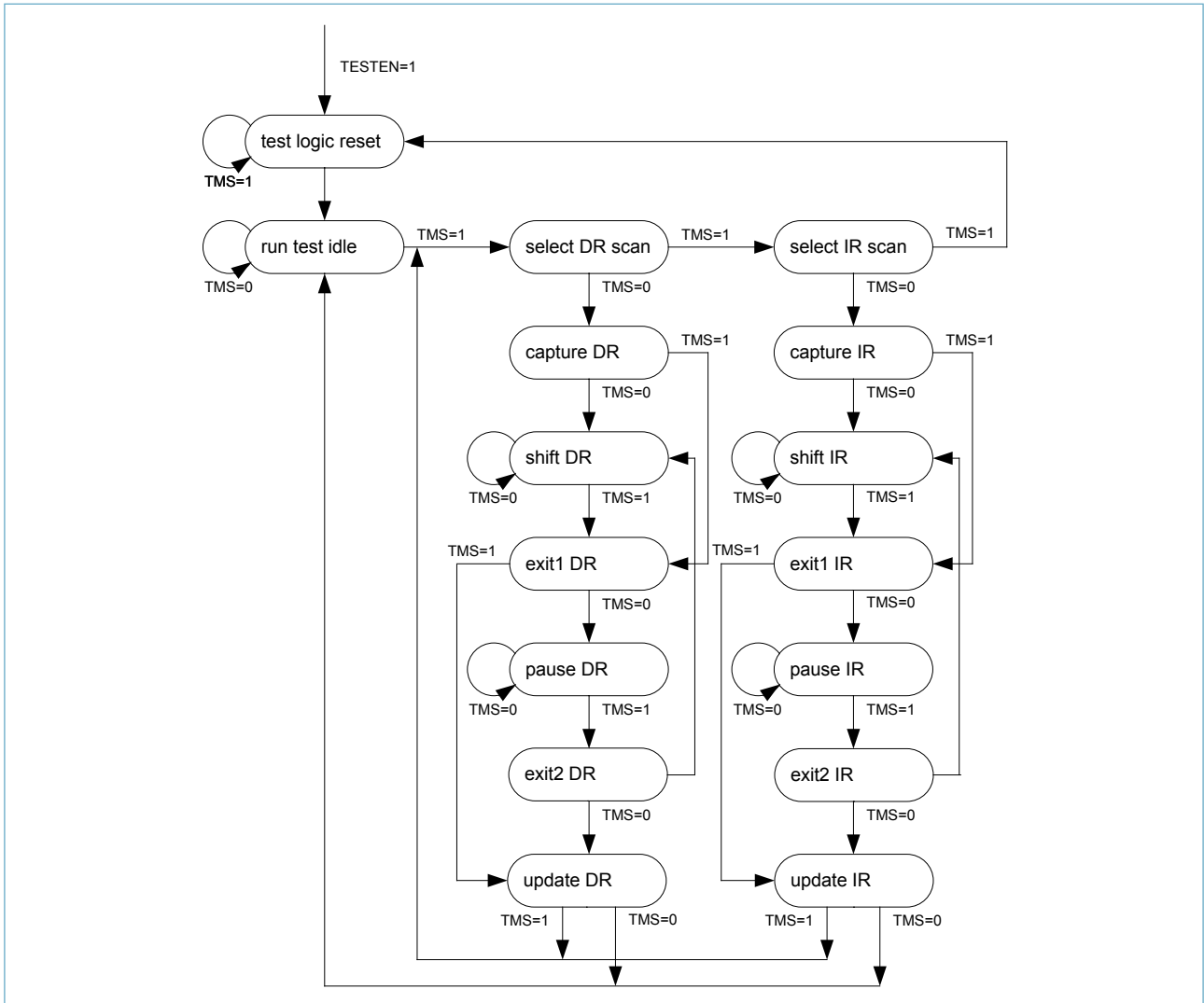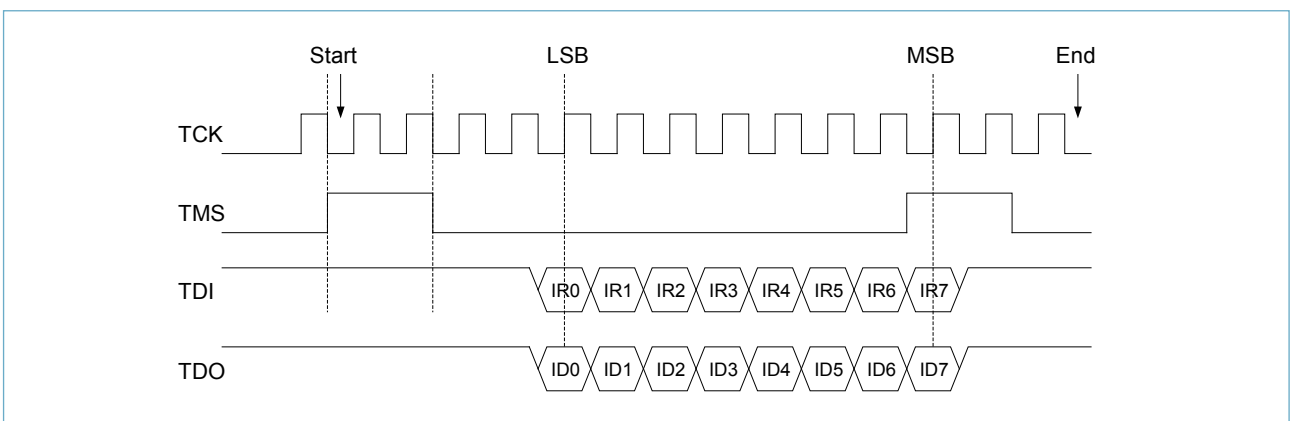
*Figure 30.   JTAG State Diagram*



*Figure 31.   JTAG Instruction Register Access (8 bit)*

JTAG instructions must be sent LSB first. Be aware, that while sending the last instruction bit TCK is active and TMS is already inactive (high).

## 7.18 Electromagnetic Compatibility

For Electromagnetic Compatibility (EMC) tests the pins GNDA, GNDPA and GNDPB are shorted together. Furthermore, the device pins are classified into global and local pins.

Global pins are:
- VS,
- VSPA, VSPB shorted together,
- depending whether LIN auto-addressing. is included or not: either BUS_M and BUS_S or BUS, respectively.

Local pins are:
- VDDA,
- V5V,
- D1, D2, D3.

Special local pins are the motor driver pins A0, A1, B0, B1. These are not tested for emission, as the external circuitry (i.e. the motor) and the selected slew-rate largely influence the emissions.

In accordance with section 5.3 of Hardware Requirements for LIN, CAN and Flex-Ray Interfaces in Automotive Applications, v1.2 of 2011-03-25., the pins BUS_S, D2, D3, A1, B0 and B1 are not tested, as their functionality is represented by BUS_M, D1 and A0, respectively.

**150Ω-Method Emission Limits**
Emissions are measured according to the 150Ω-method of the IEC 61967-4 standard in the frequency range from 150kHz to 1GHz.

The limit lines are defined in Hardware Requirements for LIN, CAN and Flex-Ray Interfaces in Automotive Applications, v1.3 of 2012.
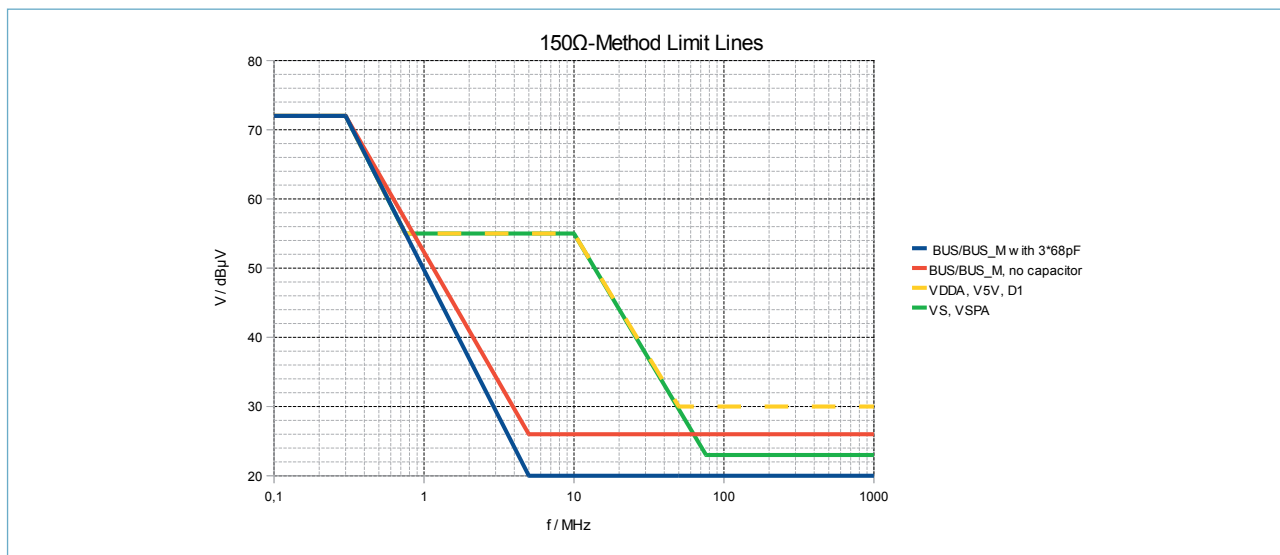


Figure 32.    150Ω-Method Limit Lines

**DPI Immunity Limits**

The Direct Power Injection (DPI) immunity tests are conducted according to IEC 62132-4.

Measurement parameters:
- frequency range: 1MHz to 1GHz,
- modulation: CW and AM 80% 1kHz (same peak),
- the stepper motor is replaced by an RL-circuit and operated in continuous stepping mode tbd. in detail.

Detailed measurement setup description:
- Global pin BUS/BUS_M without bus capacitor: CW and AM,
- Global pins VS, BUS/BUS_M with 3*68pF bus capacitor: only CW,
- Global pins VSPA, VSPB shorted together: only CW.

Failure criterion is an increased jitter and/or reduced voltage swing (pass/fail mask) tbd. at the pin A0.

The limit lines are defined in Hardware Requirements for LIN, CAN and Flex-Ray Interfaces in Automotive Applications, v1.3 of 2011-03-25.
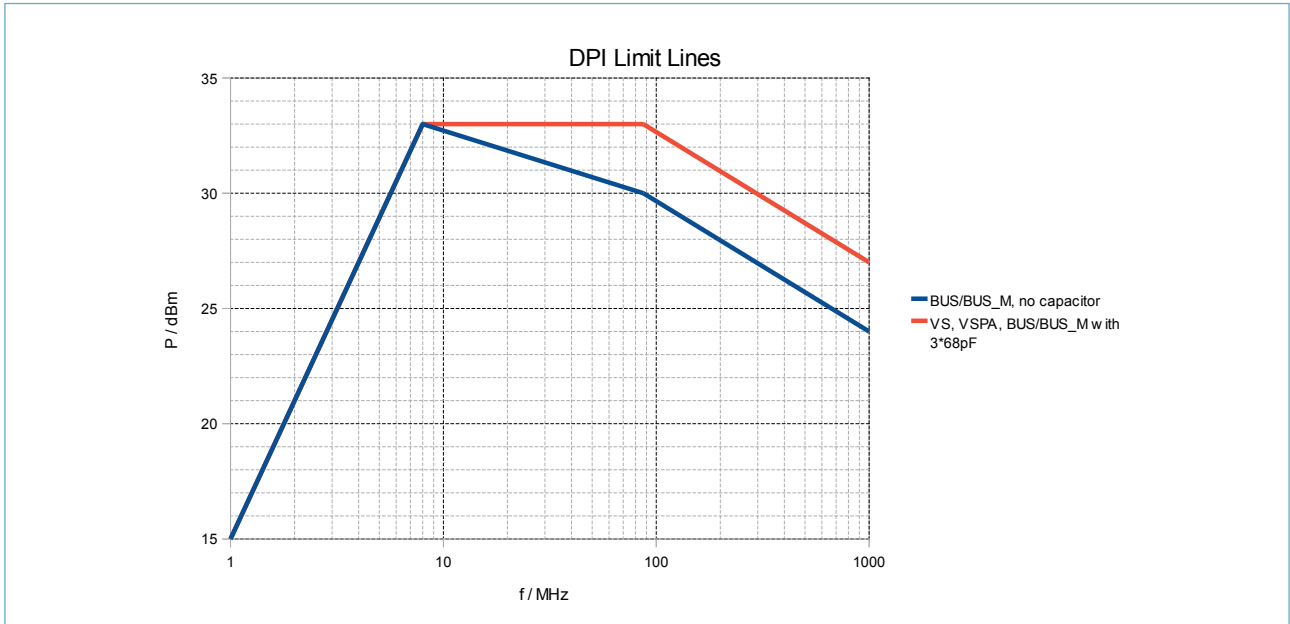
*Figure 33.    DPI Immunity Limit Lines*

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## 8 Application Information
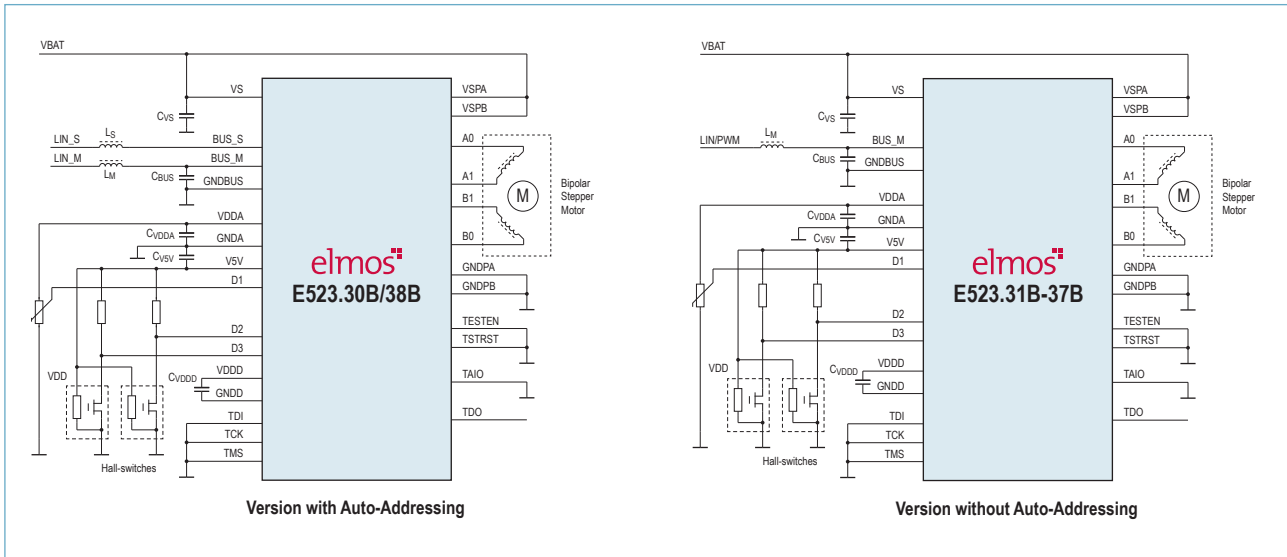


*Figure 34.   Application circuits*

| Description | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Ferrite RF attenuator ( optional for EMC optimization) | High attenuation of RF Disturbances | $L_M$, $L_S$ | | TDK MMZ2-012Y2-02B or equivalent | | |
| Blocking capacitor for supply voltage | | $C_{VS}$ | | 100 | | µF |
| Blocking capacitor for Hall supply voltage | | $C_{V5V}$ | | 1 | | µF |
| Blocking capacitor for analog supply voltage | | $C_{VDDA}$ | | 1 | | µF |
| Blocking capacitor for digital supply voltage | | $C_{VDDD}$ | | 1 | | µF |

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# 9 Package Information

All devices are available in a Pb free, RoHs compliant QFN32L6 plastic package according to JEDEC MO-220 K, variant VJJC-2. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of (260+5)°C.
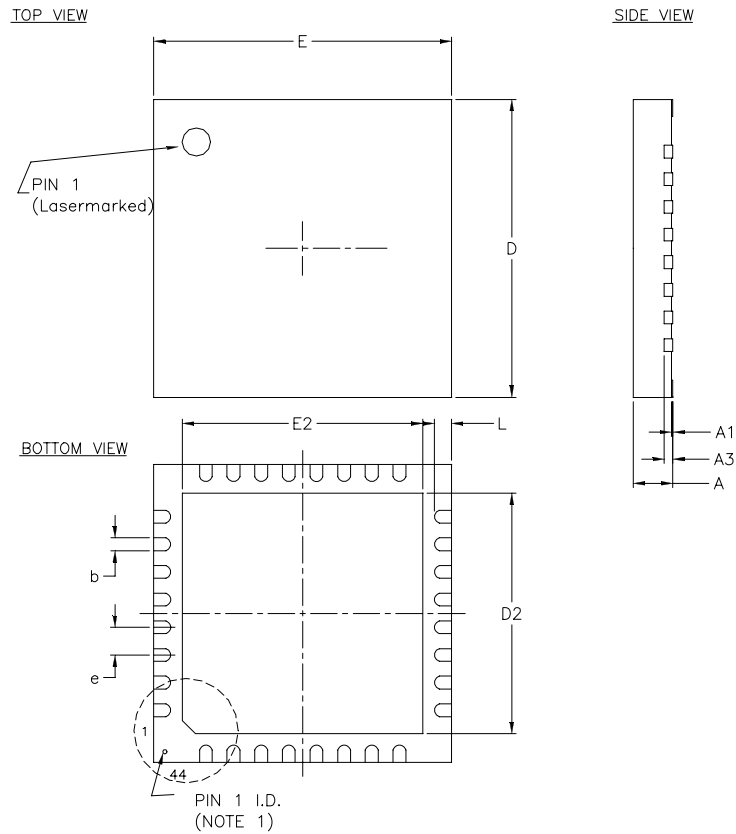


| Description | Symbol | mm | | | inch | | |
|---|---|---|---|---|---|---|---|
| | | **min** | **typ** | **max** | **min** | **typ** | **max** |
| Package height | A | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| Stand off | A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.00079 | 0.002 |
| Thickness of terminal leads, including lead finish | A3 | -- | 0.20 REF | -- | -- | 0.0079 REF | -- |
| Width of terminal leads | b | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| Package length / width | D / E | -- | 6.00 BSC | -- | -- | 0.237 BSC | -- |
| Length / width of exposed pad | D2 / E2 | 4.50 | 4.65 | 4.80 | 0.177 | 0.183 | 0.189 |
| Lead pitch | e | -- | 0.65 BSC | -- | -- | 0.026 BSC | -- |
| Length of terminal for soldering to substrate | L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| Number of terminal positions | N | | 32 | | | 32 | |

**Note:** the mm values are valid, the inch values contains rounding errors

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## 10   Marking

### 10.1  Top Side

► Elmos (Logo)
► 52330B
► YWW*#
► XXXXU

| Signature | Explanation |
|-----------|-------------|
| 52330 | Elmos project number |
| B | Elmos project revision code |
| Y | Year of assembly (e.g. 2013) |
| WW | Week of assembly |
| * | Mask revision code |
| # | Elmos internal code |
| XXXX | Production lot number (1 to 4 digits) |
| U | Assembler Code |

E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

## 11   Record of Revision

| Chapter | Revision | Change and Reason for Change | Date | Released Elmos |
|---------|----------|------------------------------|------|----------------|
| 10.1 | .01 | Marking, signature and explanation updated | Dec 18, 2013 | ROWE/ZOE |
| 11 | .01 | New chapter | Dec 18, 2013 | ROWE/ZOE |
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E523.30B, E523.31B, E523.32B, E523.33B, E523.34B, E523.35B, E523.36B, E523.37B, E523.38B

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