EN5339QI
3A Low Profile Synchronous Buck DC-DC Converter with Integrated Inductor

RoHS Compliant
Halogen Free

Description

The EN5339 is a low profile 3A, high efficiency, synchronous buck PowerSoC. The device features integrated inductor, PWM controller, MOSFETS, and compensation providing the smallest possible solution size.

The EN5339QI is pin compatible with Enpirion's EN5322QI 2A PowerSoC enabling a family of scalable solutions.

The high frequency operation allows for the use of tiny MLCC capacitors. It also enables a very wide control loop bandwidth providing excellent transient performance and reduced output impedance. The internal compensation is designed for unconditional stability across all operating conditions.

The output voltage is set via a simple and flexible resistor divider network.

The very high efficiency and low profile design make this device optimal for space constrained applications requiring up to 3A of continuous output current.

Features

- Integrated Inductor
- Solution Footprint as Small as 55 mm^2
- Low profile, 1.1mm
- High Reliability Solution: 28,200 Years in MTTF
- High Efficiency, up to 95 %
- Low Output Ripple Voltage; <5mV_{P-P} Typical
- ±3% Output Variation Over Line, Load, Temp
- 2.4 V to 5.5 V Input Voltage Range
- 3A Continuous Output Current Capability
- Output Enable and Power OK Signal
- Under Voltage Lockout, Over Current, Short Circuit, and Thermal Protection
- RoHS Compliant; Halogen Free; 260℃ Reflow

Applications

- Applications with Low Profile Requirement such as SSD and Embedded Computing
- SAN/NAS accelerator appliance
- Controllers, Raid, Processors, Network Processors, DSPs' FPGAs, and ASICs
- Noise sensitive applications

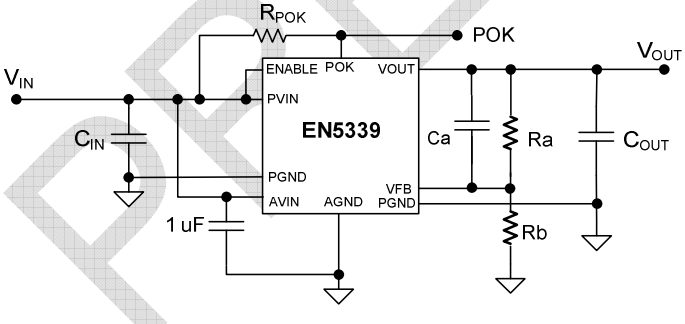


Figure 1. Simplified Applications Circuit

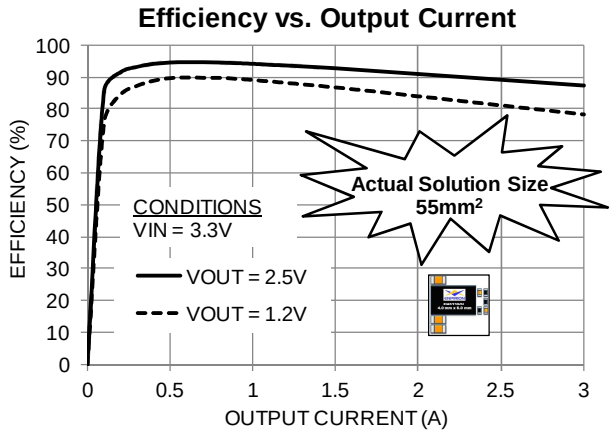


Figure 2. Highest Efficiency in Smallest Solution Size

Ordering Information

Part Number	Package Markings	Temp Rating (℃)	Package Description
EN5339QI	EN5339	-40 to +85	24-pin (4mm x 6mm x 1.1mm) QFN T&R
EN5339QI-E	EN5339	QFN Evaluation Board	

Pin Assignments (Top View)

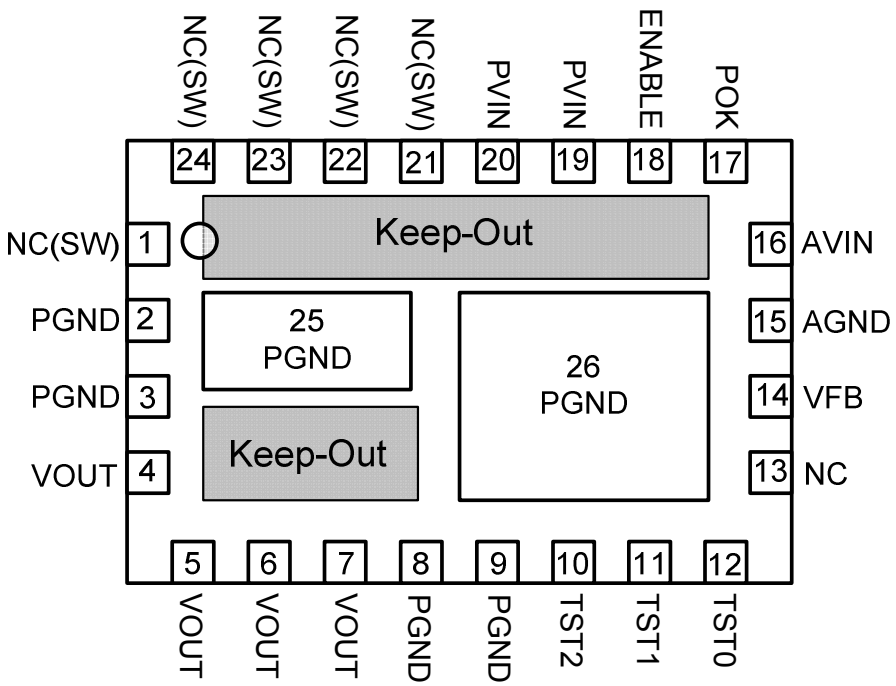


Figure 3: Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: Grey area highlights exposed metal on the bottom of the package that is not to be mechanically or electrically connected to the PCB. There should be no traces on PCB top layer under these keep out areas.

NOTE C: White 'dot' on top left is pin 1 indicator on top of the device package.

Pin Description

PIN	NAME	FUNCTION
1, 21-24	NC(SW)	NO CONNECT: These pins are internally connected to the common switching node of the internal MOSFETs. They must be soldered to PCB but not be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in device damage.
2-3, 8-9	PGND	Input and output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. See VOUT, PVIN descriptions and Layout Recommendation for more details.
4-7	VOUT	Regulated converter output. Connect to the load and place output filter capacitor(s) between these pins and PGND pins 7 and 8. See layout recommendation for details
10	TST2	Test Pin. For Enpirion internal use only. Connect to AVIN at all times.
11	TST1	Test Pin. For Enpirion internal use only. Connect to AVIN at all times.
12	TST0	Test Pin. For Enpirion internal use only. Connect to AVIN at all times.

PIN	NAME	FUNCTION
13	NC	NO CONNECT: This pin must be soldered to PCB but not electrically connected to any other pin or to any external signal, voltage, or ground. This pin may be connected internally. Failure to follow this guideline may result in device damage.
14	VFB	This is the external feedback input pin. A resistor divider connects from the output to AGND. The mid-point of the resistor divider is connected to VFB. A feed-forward capacitor is required parallel to the upper feedback resistor (R_A). The output voltage regulation is based on the VFB node voltage equal to 0.600V.
15	AGND	The quiet ground for the control circuits. Connect to the ground plane with a via right next to the pin.
16	AVIN	Analog input voltage for the control circuits. Connect this pin to the input power supply (PVIN) at a quiet point. Decouple with a 1uF capacitor to AGND.
17	POK	POK is an open drain output. Refer to Power OK section for details.
18	ENABLE	Input Enable. A logic high level on this pin enables the output and initiates a soft start. A logic low signal disables the output and discharges the output to GND. This pin must not be left floating.
19-20	PVIN	Input power supply. Connect to input power supply and place input filter capacitor(s) between these pins and PGND pins 2 to 3.
25,26	PGND	Not a perimeter pin. Device thermal pad to be connected to the system GND plane for heat-sinking purposes. See Layout Recommendation section.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Voltages on : PVIN, AVIN, VOUT		-0.3	6.5	V
Voltages on: ENABLE, POK, TST0, TST1, TST2		-0.3	V_{IN}+0.3	V
Voltages on: VFB		-0.3	2.7	V
Storage Temperature Range	T_{STG}	-65	150	℃
Maximum Operating Junction Temperature	$T_{J\text{-}ABS\ Max}$		150	℃
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (Human Body Model)			2000	V
ESD Rating (Charge Device Model)			500	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.4	5.5	V
Output Voltage Range (Note 1)	V_{OUT}	0.6	$V_{IN} - V_{DO}$	V
Output Current	I_{OUT}	0	3	A
Operating Ambient Temperature	T_A	-40	+85	℃
Operating Junction Temperature	T_J	-40	+125	℃

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient (0 LFM) (Note 2)	θ_{JA}	36	℃/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	6	℃/W
Thermal Shutdown	T_{SD}	155	℃
Thermal Shutdown Hysteresis	T_{SDH}	15	℃

Note 1: V_{DO} (dropout voltage) is defined as (I_{LOAD} x Dropout Resistance). Please see Electrical Characteristics Table.

Note 2: Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

Electrical Characteristics

NOTE: VIN = 5V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25°C.

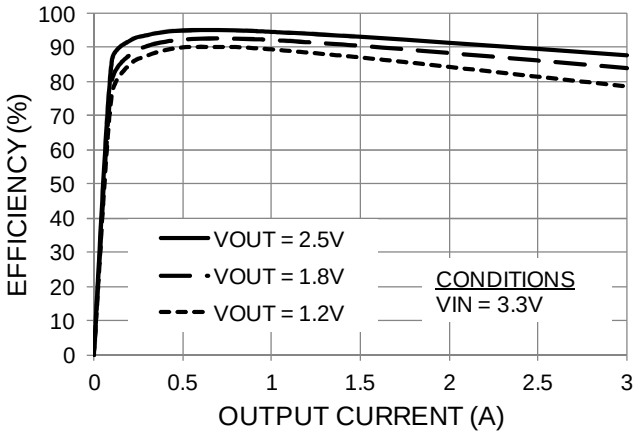
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		2.4		5.5	V
Feedback Node Initial Accuracy	V_{VFB}	T_A = 25°C; V_{IN} = 5V I_{LOAD} = 100 mA	0.588	0.6	0.612	V
Output Variation (Note 3) (Line, Load, Temperature)	V_{OUT}	2.4V ≤ V_{IN} ≤ 5.5V 0 ≤ I_{LOAD} ≤ 3A	-3		+3	%
VFB, ENABLE, TST0/1/2 Pin Input Current (Note 4)					+/-40	nA
Shutdown Current		ENABLE Low		18		µA
Under Voltage Lock-out – V_{IN} Rising	V_{UVLOR}	Voltage Above Which UVLO is Not Asserted		2.2		V
Under Voltage Lock-out – t_{VIN} Falling	V_{UVLOF}	Voltage Below Which UVLO is Asserted		2.1		V
Soft Start Time		Time from Enable High	0.91	1.40	1.89	ms
Dropout Resistance				150	300	mΩ
ENABLE Voltage Threshold		Logic Low Logic High	0.0 1.4		0.4 V_{IN}	V
POK Threshold		V_{OUT} Rising		92		%
POK Threshold		V_{OUT} Falling		90		%
POK Low Voltage		I_{SINK} = 5 mA		0.15	0.4	V
POK Pin V_{OH} Leakage Current		POK High			500	nA
Current Limit Threshold		2.4V ≤ V_{IN} ≤ 5.5V	3.5	5		A
Operating Frequency	F_{OSC}			3.5		MHz
Output Ripple Voltage	V_{RIPPLE}	C_{OUT} = 3 x 22 µF 0805 X5R MLCC, V_{OUT} = 3.3 V, I_{LOAD} = 3A		4.2		mV_{P-P}
		C_{OUT} = 3 x 22 µF 0805 X5R MLCC, V_{OUT} = 1.8 V, I_{LOAD} = 3A		5.5		mV_{P-P}

Note 3: Output voltage variation is based on using 0.1% accuracy resistor values.

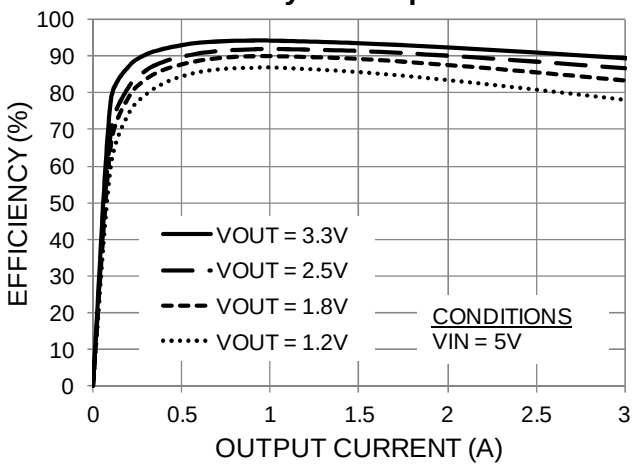
Note 4: Parameter not production tested but is guaranteed by design.

Typical Performance Curves

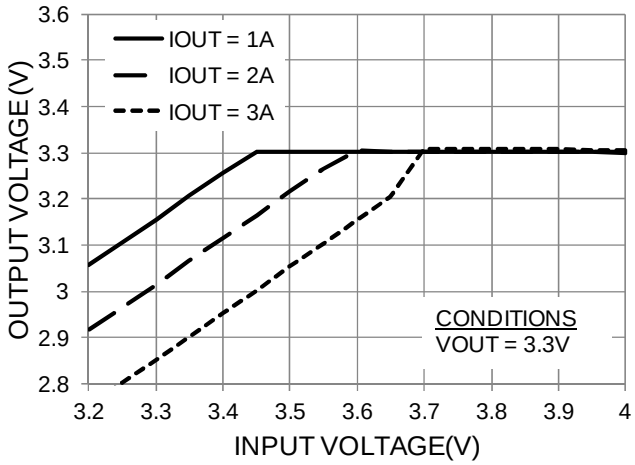
Efficiency vs. Output Current



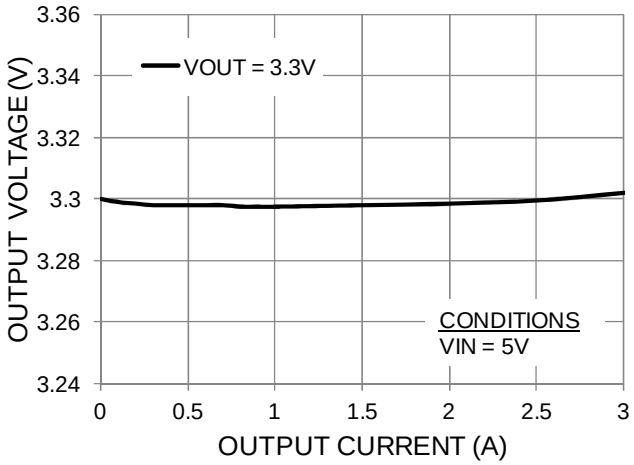
Efficiency vs. Output Current



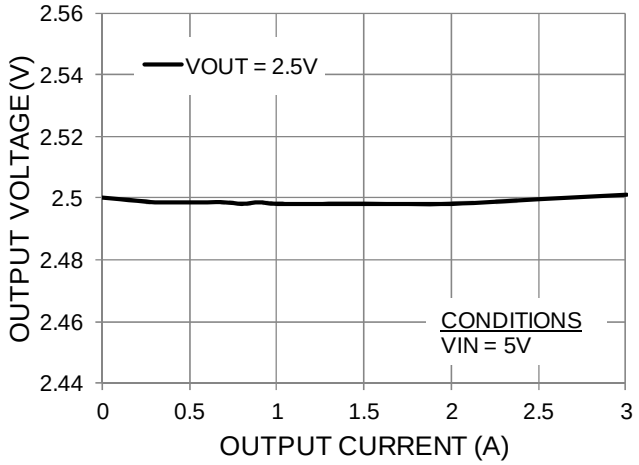
Dropout Voltage



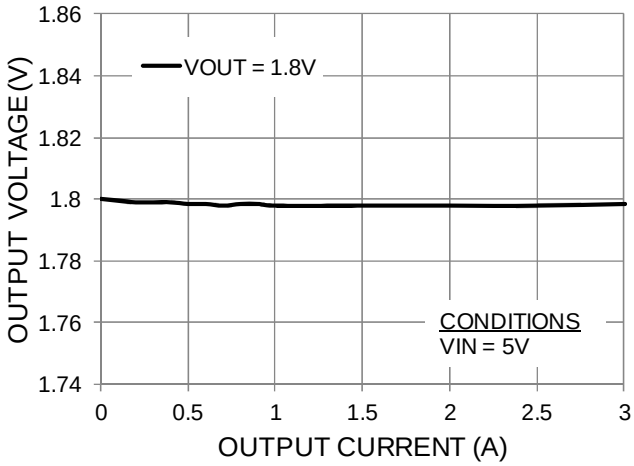
Output Voltage vs. Output Current



Output Voltage vs. Output Current

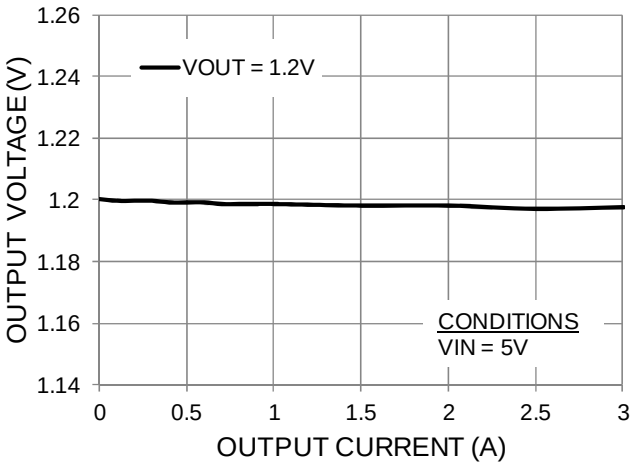


Output Voltage vs. Output Current

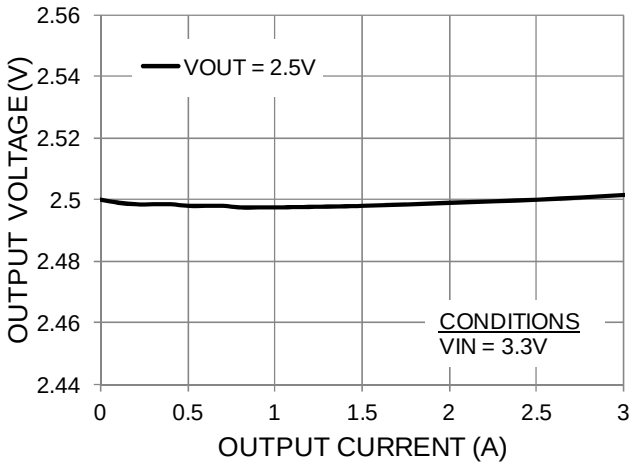


Typical Performance Curves (Continued)

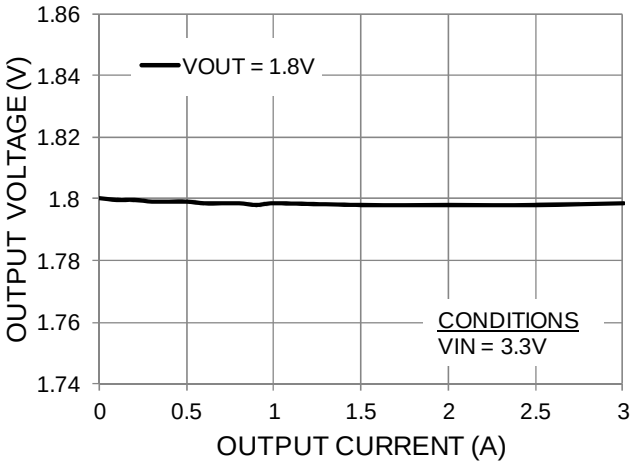
Output Voltage vs. Output Current



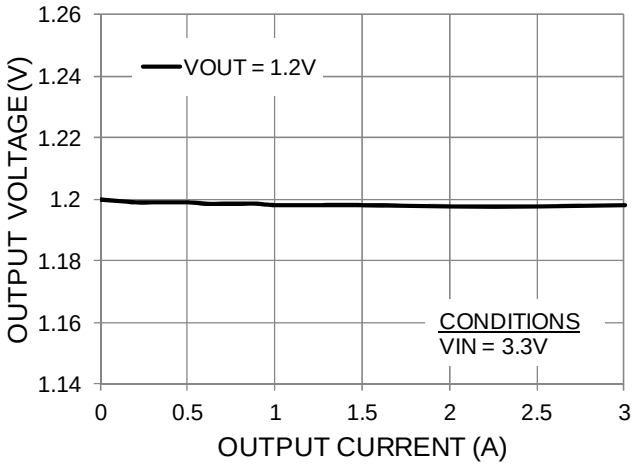
Output Voltage vs. Output Current



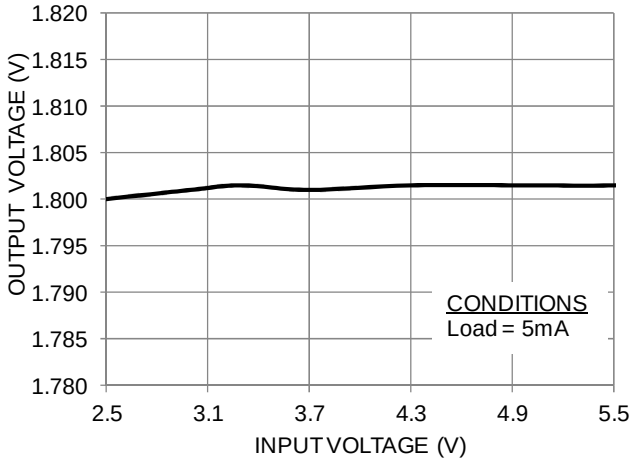
Output Voltage vs. Output Current



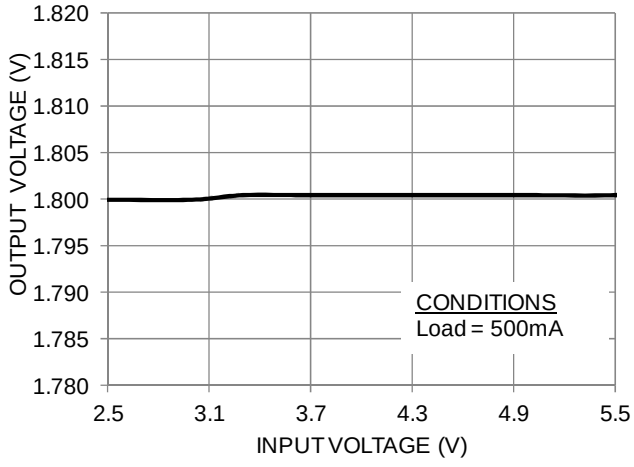
Output Voltage vs. Output Current



Output Voltage vs. Input Voltage

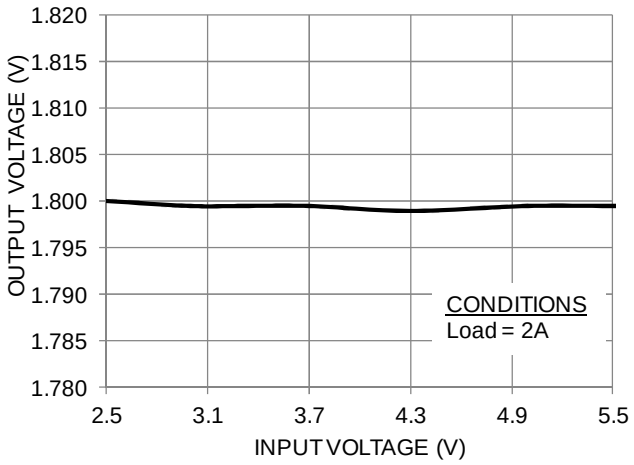


Output Voltage vs. Input Voltage

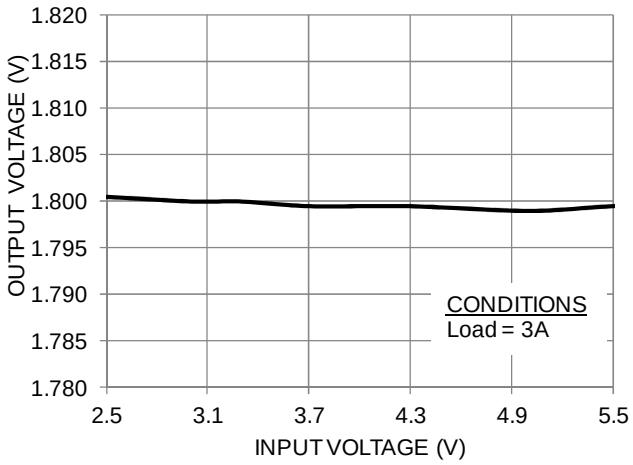


Typical Performance Curves (Continued)

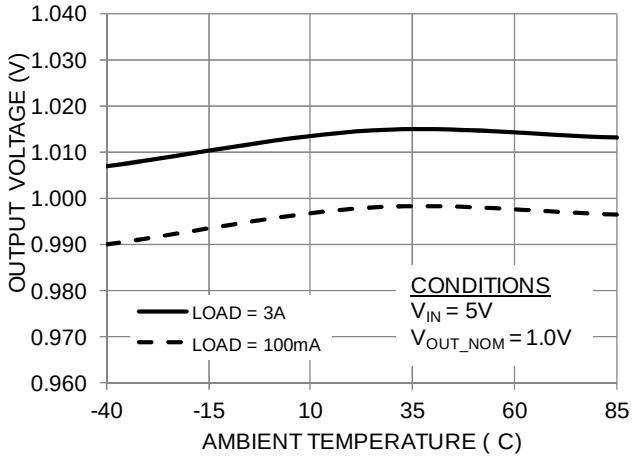
Output Voltage vs. Input Voltage



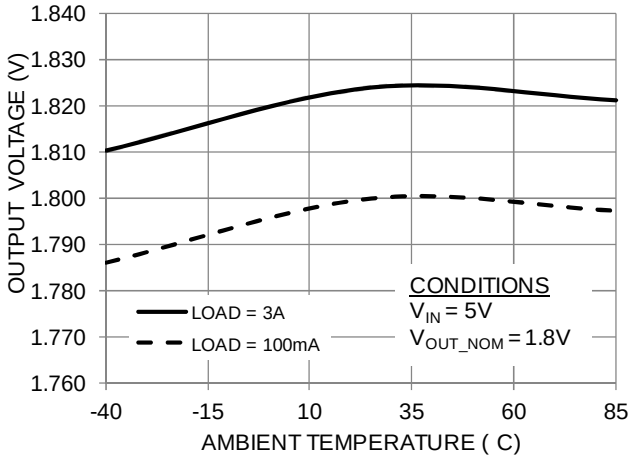
Output Voltage vs. Input Voltage



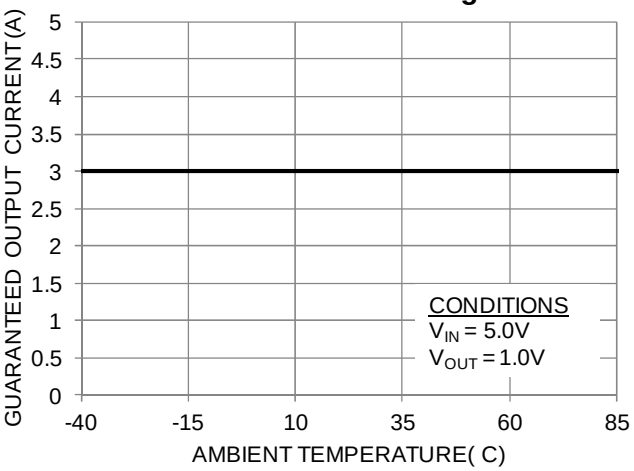
Output Voltage vs. Temperature



Output Voltage vs. Temperature



No Thermal Derating



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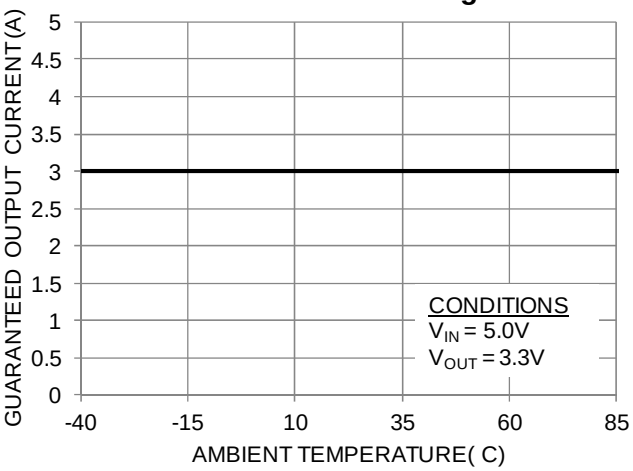
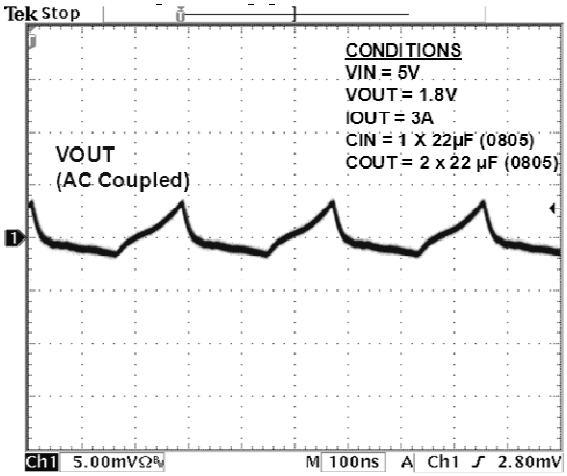
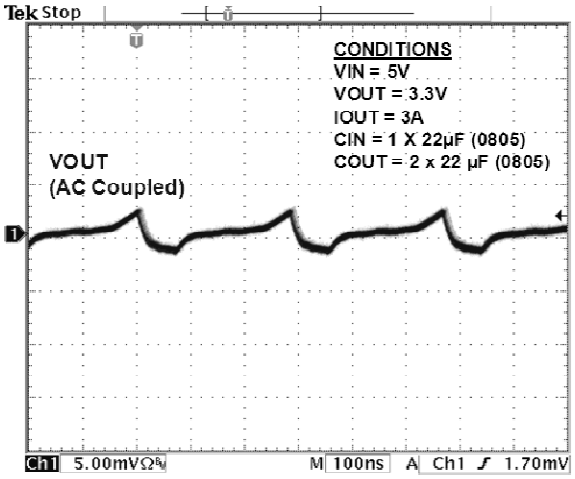


Typical Performance Characteristics (Continued)

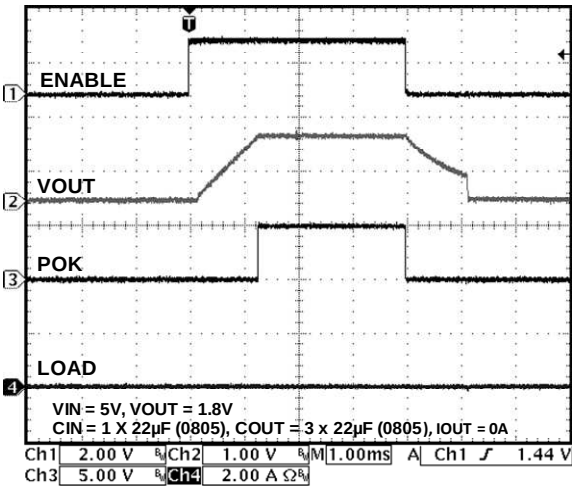
Output Ripple at 20MHz



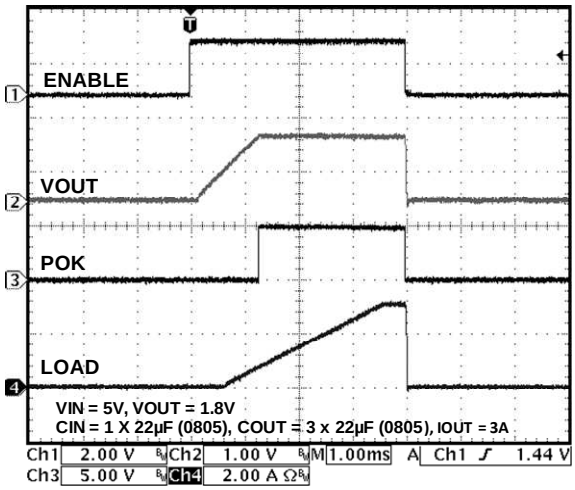
Output Ripple at 20MHz



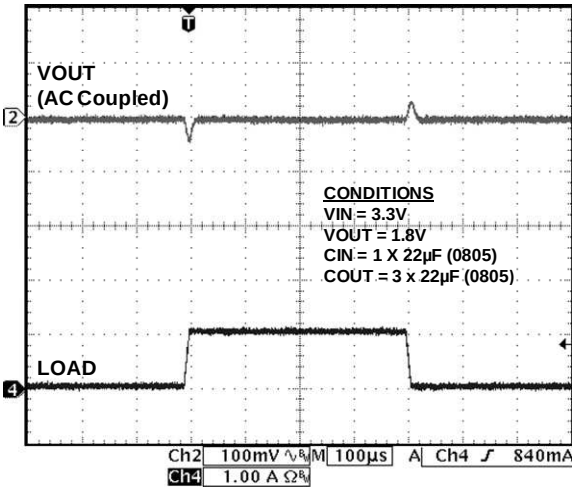
Startup Waveforms at 0A



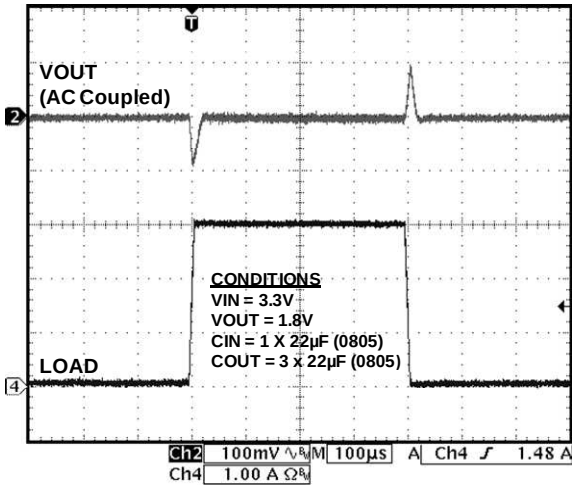
Startup Waveforms at 3A



Load Transient from 0 to 1A

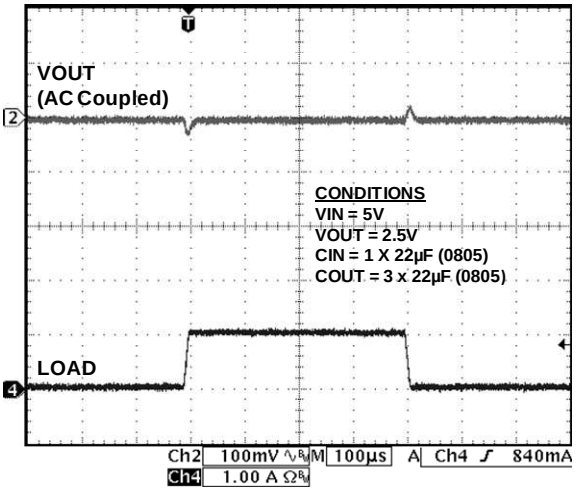


Load Transient from 0 to 3A

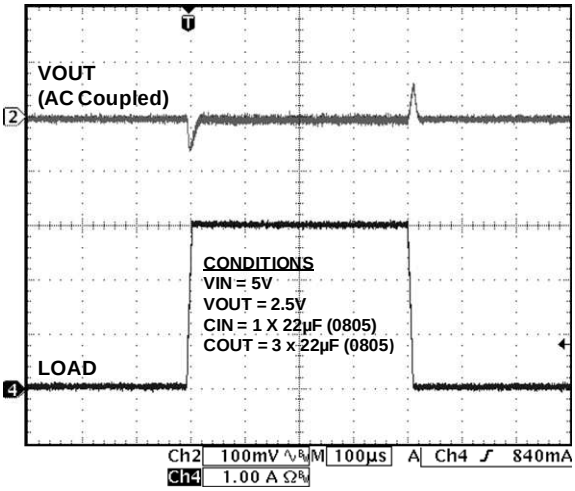


Typical Performance Characteristics (Continued)

Load Transient from 0 to 1A



Load Transient from 0 to 3A



Functional Block Diagram

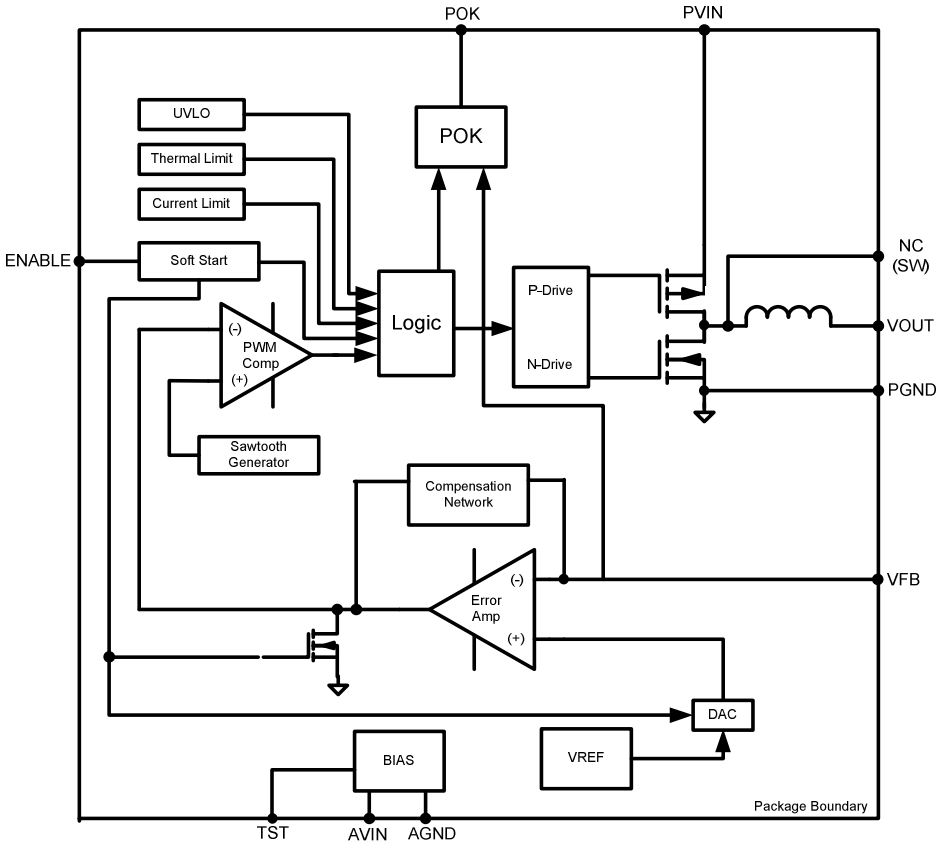


Figure 4: Functional Block Diagram

Functional Description

Overview

The EN5339QI leverages advanced CMOS technology to provide high switching frequency, while also maintaining high efficiency.

Packaged in a 4 mm x 6 mm x 1.1 mm QFN, the EN5339QI provides a high degree of flexibility in circuit design while maintaining a very small footprint. High switching frequency allows for the use of very small MLCC input and output filter capacitors.

The converter uses Type III voltage mode control to provide high noise immunity, low output impedance and excellent load transient response.
POK monitors the output voltage and signals if it is within ±10% of nominal. Protection features include under voltage lockout (UVLO), over current protection, short circuit protection, and thermal overload protection.

Stability over Wide Range of Operating Conditions

The EN5339QI utilizes an internal compensation network and is designed to provide stable operation over a wide range of operating conditions. To improve transient performance or reduce output voltage ripple with dynamic loads you have the option to add supplementary capacitance to the output.

Soft Start

The EN5339QI has an internal soft-start circuit that controls the ramp of the output voltage. The control circuitry limits the V_{OUT} ramp rate to levels that are safe for the Power MOSFETS and the integrated inductor.

The EN5339QI has a constant startup up time which is independent of the VOUT setting. This means that the output slew rate is a function of the output voltage setting. The startup time is given in

the electrical characteristics table.

Excess bulk capacitance on the output of the device can cause an over-current condition at startup. Since the slew rate varies with the output voltage setting, the maximum capacitance is a function of the VOUT setting.
The maximum capacitance on the output power rail, including the output filter capacitors and all decoupling and bulk capacitors on the supply rail is given by:
$C_{OUT\_TOTAL\_MAX}$ [F] = $3.6x10^{-3}/V_{OUT}$

NOTE: The above number and formula assume a no load condition at startup.

Over Current/Short Circuit Protection

When an over current condition occurs, V_{OUT} is pulled low. This condition is maintained for a period of 1.2 ms and then a normal soft start cycle is initiated. If the over current condition still persists, this cycle will repeat.

Under Voltage Lockout

An under voltage lockout circuit will hold off switching during initial power up until the input voltage reaches sufficient level to ensure proper operation. If the voltage drops below the UVLO threshold the lockout circuitry will again disable switching. Hysteresis is included to prevent chattering between UVLO high and low states.

Enable

The ENABLE pin provides means to shut down the converter or initiate normal operation. A logic high will enable the converter to go through the soft start cycle and regulate the output voltage to the desired value. A logic low will allow the device to discharge the output and go into shutdown mode for minimal power consumption. When the output is discharged, an auxiliary NFET turns on and limits the discharge current to 300 mA or below. The ENABLE pin must not be left floating.

Thermal Shutdown

When excessive power is dissipated in the device, its junction temperature rises. Once the junction temperature exceeds the thermal shutdown temperature 155℃, the thermal shutdown circuit turns off the converter, allowing the device to cool. When the junction temperature drops 15℃, the device will be re-enabled and go through a normal startup process.

Power OK

The EN5339 provides an open drain output to indicate if the output voltage stays within 92% to 111% of the set value. Within this range, the POK output is allowed to be pulled high. Outside this range, POK remains low. However, during transitions such as power up, power down, and dynamic voltage scaling, the POK output will not change state until the transition is complete for enhanced noise immunity.
The POK has 5 mA sink capability for events where it needs to feed a digital controller with standard CMOS inputs. When POK is pulled high, the pin leakage current is as low as 500 nA maximum over temperature. This allows a large pull up resistor such as 100 kΩ to be used for minimal current consumption in shutdown mode.
The POK output can also be conveniently used as an ENABLE input of the next stage for power sequencing of multiple converters.

Application Information

Setting the Output Voltage

The EN5339 uses a simple and flexible resistor divider network to program the output voltage. Table 1 shows the recommended component values for the feedback network as a function of VIN, VOUT, and anticipated maximum load current. It is recommended to use 1% or better feedback resistors to ensure high accuracy. The value of resistor Ra is given in the table for the specific operating conditions. Based on that value, the value of the bottom resistor Rb is given below as:

$$Rb = \frac{Ra \times V_{REF}}{V_{OUT} - V_{REF}}$$

Where V_{OUT} is the output voltage and V_{REF} is 0.6V nominally.

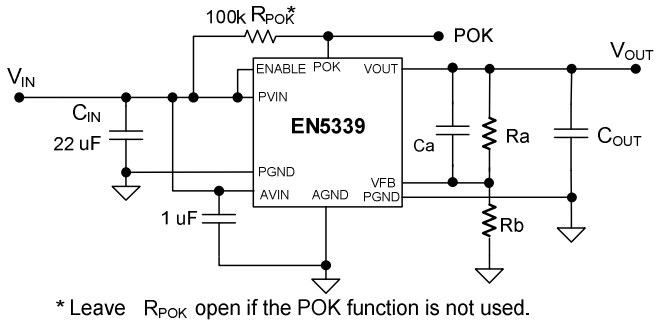


Figure 5. Typical Application Circuit with External Resistor Divider

(*NOTE:* Enable can be separated from PVIN if the application requires it)

AVIN Filter Capacitor

A 1.0 µF, 10V, 0402 MLCC capacitor should be placed between the AVIN and AGND pins. This will provide high frequency bypass to ensure clean chip supply for optimal performance.

Input Filter Capacitor Selection

A single 22 µF, 0805 X5R MLCC capacitor is needed on PVIN for all applications. Connect between the PVIN and PGND pins. Make sure that the capacitor is placed as close to the pins of the EN5339QI as the application allows. Placement of this part is critical to ensure low conducted and radiated EMI.

Low ESR MLCC capacitors with X5R or X7R or equivalent dielectric should be used for the input capacitors. Y5V or equivalent dielectrics lose too much capacitance with frequency, DC bias, and temperature. Therefore, they are not suitable for switch-mode DC-DC converter filtering, and must be avoided.

Output Filter Capacitor Selection

Table 1 provides the recommended output capacitor configuration based on operating conditions. For details regarding other configurations, contact Enpirion Applications Engineering (techsupport@enpirion.com).

Table 1. Typical Recommended Components
(Note: Follow Layout Recommendations)

VIN (V)	IOUT	VOUT	COUT	Ra (kΩ)	Ca (pF)
2.5 to 5.5	3A	0.9V	3x 22µF (0805)	348	10
		1V			
		1.2V			
		1.5V			
		1.8V			
		2.5			8.2
		2.85V			
		3.3V			

Layout Recommendations

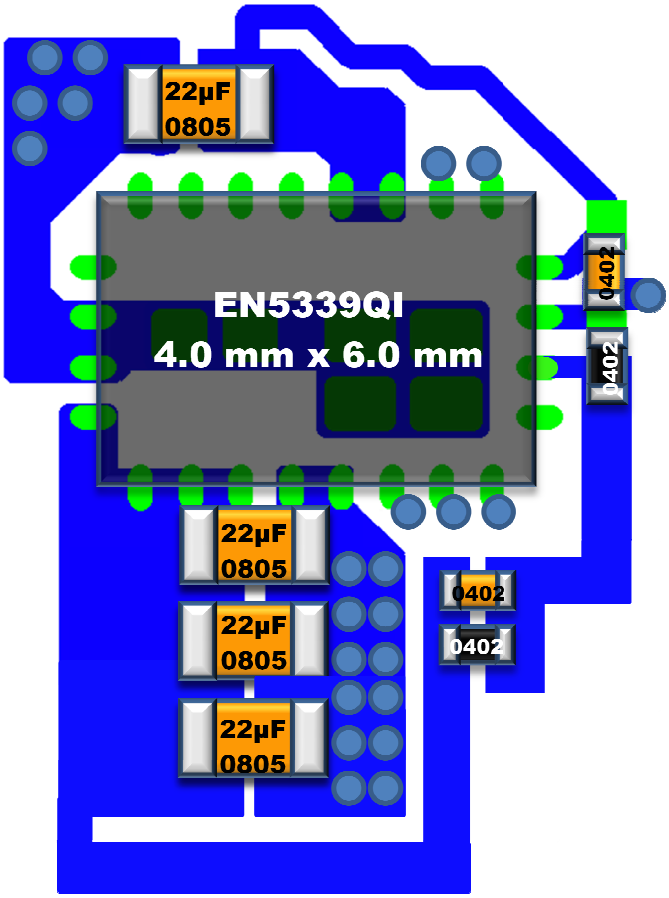


Figure 6. Optimized Layout Recommendations

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN5339QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN5339QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors.

Recommendation 3: The thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

Recommendation 4: Multiple small vias (the same size as the thermal vias discussed in recommendation 3) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops.

Recommendation 5: AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 6 this connection is made at the input capacitor. Connect a 1µF capacitor from the AVIN pin to AGND.

Recommendation 6: The layer 1 metal under the device must not be more than shown in Figure 6. See the section regarding exposed metal on bottom of package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 7: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node.

Recommendation 8: Keep R_A, C_A, and R_B, close to the VFB pin (See Figures 6). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane.

Recommendation 13: Enpirion provides schematic and layout reviews for all customer designs. Please contact local sales representatives for references to Enpirion Applications Engineering support (techsupport@enpirion.com).

Design Considerations for Lead-Frame Based Modules

Exposed Metal Pads on Package Bottom

QFN lead-frame based package technology utilizes exposed metal pads on the bottom of the package that provide improved thermal dissipation, lower package thermal resistance, smaller package footprint and thickness, larger lead size and pitch, and excellent lead co-planarity. As the EN5339 package is a fully integrated module consisting of multiple internal devices, the lead-frame provides circuit interconnection and mechanical support of these devices resulting in multiple exposed metal pads on the package bottom.

Only the two large thermal pads and the perimeter leads are to be mechanically/electrically connected to the PCB through a SMT soldering process. All other exposed metal is to remain free of any interconnection to the PCB. Figure 7 shows the recommended PCB metal layout for the EN5339 package. A GND pad with a solder mask "bridge" to separate into two pads and 24 signal pads are to be used to match the metal on the package. The PCB should be clear of any other metal, including traces, vias, etc., under the package to avoid electrical shorting.

The Solder Stencil Aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package. Please consult the Enpirion Manufacturing Application Note for more details and recommendations.

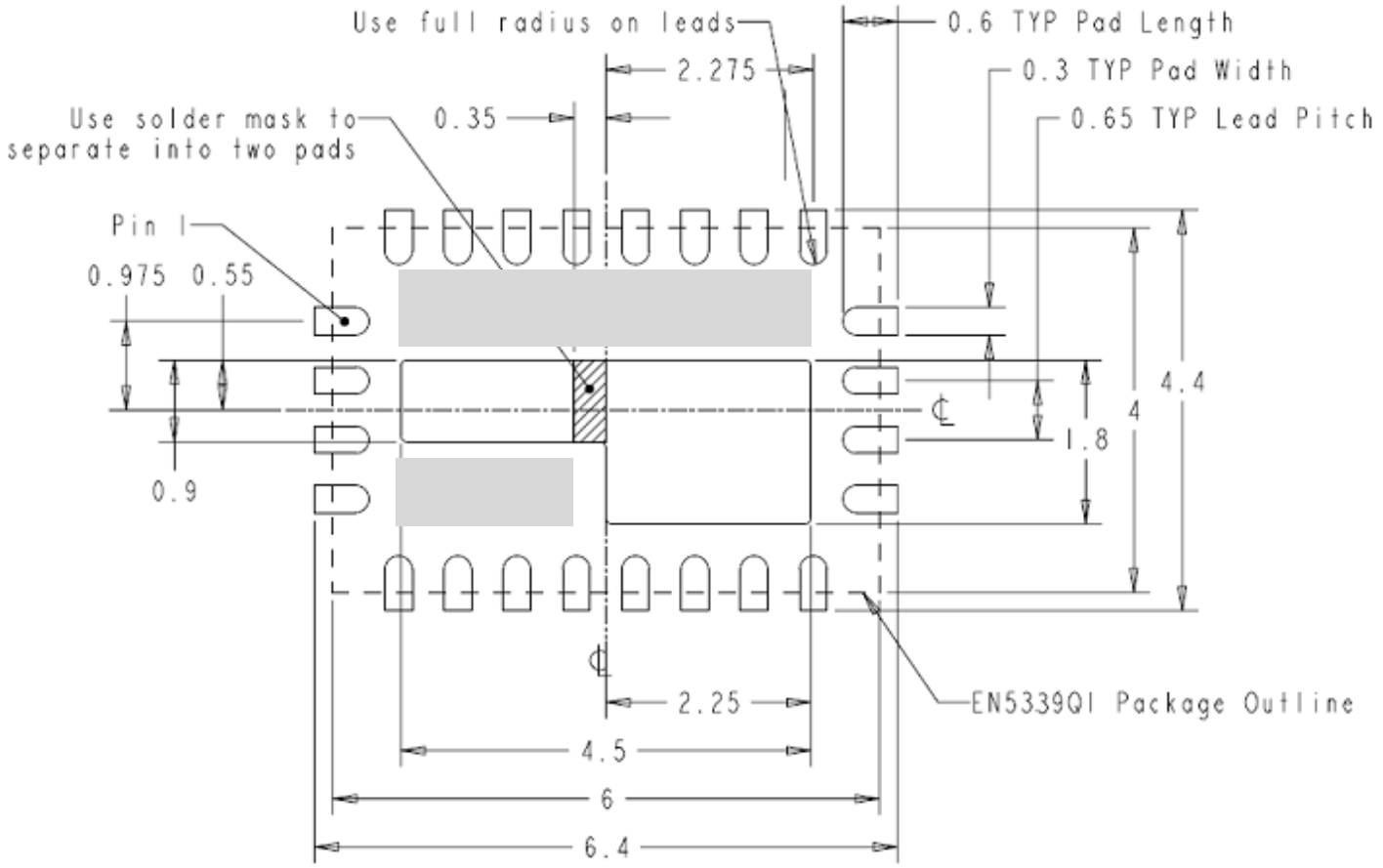


Figure 7. Recommended Footprint for PCB (Top View)

Grey area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

Package Mechanical

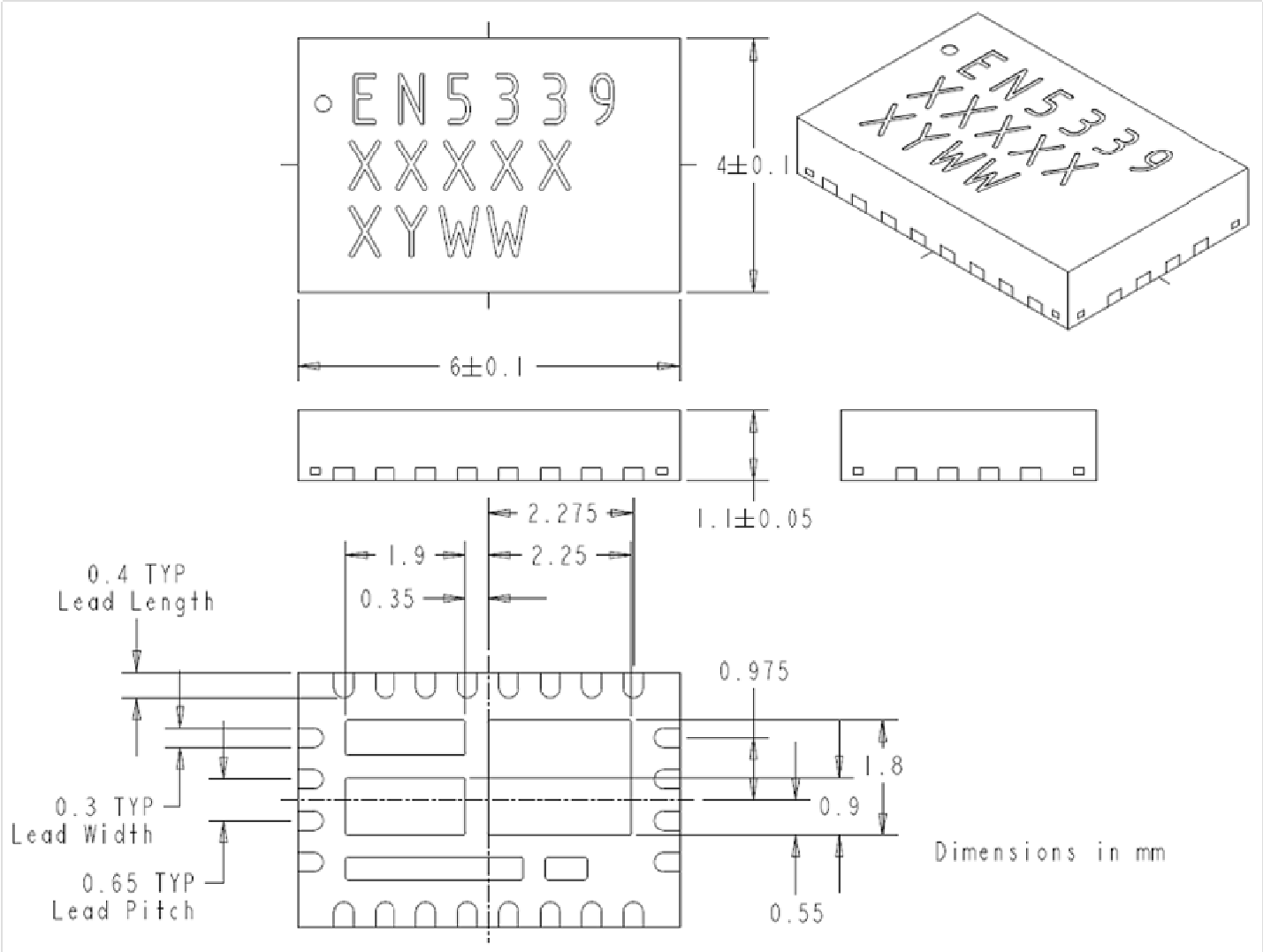


Figure 8. EN5339QI Package Dimensions (Bottom View)

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