EN2340QI
4A Voltage Mode Synchronous Buck PWM DC-DC Converter with Integrated Inductor PowerSOC

Description

The EN2340QI is a Power System on a Chip (PowerSoC) DC-DC converter. It integrates MOSFET switches, small-signal control circuits, compensation and an integrated inductor in an advanced 8x11x3mm QFN module. It offers high efficiency, excellent line and load regulation over temperature and up to the full 4A load range. The EN2340QI operates over a wide input voltage range and is specifically designed to meet the precise voltage and fast transient requirements of high-performance products. The EN2340 features frequency synchronization to an external clock, power OK output voltage monitor, programmable soft-start along with thermal and over current protection. The device's advanced circuit design, ultra high switching frequency and proprietary integrated inductor technology delivers high-quality, ultra compact, non-isolated DC-DC conversion.

The Enpirion solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, overall system level reliability is improved given the small number of components required with the Enpirion solution.

All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

Features

- Integrated Inductor, MOSFETs, Controller
- Wide Input Voltage Range: 4.5V – 14V
- Guaranteed 4A I_{OUT} at 85°C with No Airflow
- Frequency Synchronization (External Clock)
- 2% V_{OUT} Accuracy (Over Line/Load/Temperature)
- High Efficiency (Up to 95%)
- Output Enable Pin and Power OK signal
- Programmable Soft-Start Time
- Pin Compatible with the EN2360QI (6A)
- Under Voltage Lockout Protection (UVLO)
- Programmable Over Current Protection
- Thermal Shutdown and Short Circuit Protection
- RoHS Compliant, MSL Level 3, 260°C Reflow

Applications

- Space Constrained Applications
- Distributed Power Architectures
- Output Voltage Ripple Sensitive Applications
- Beat Frequency Sensitive Applications
- Servers, Embedded Computing Systems, LAN/SAN Adapter Cards, RAID Storage Systems, Industrial Automation, Test and Measurement, and Telecommunications

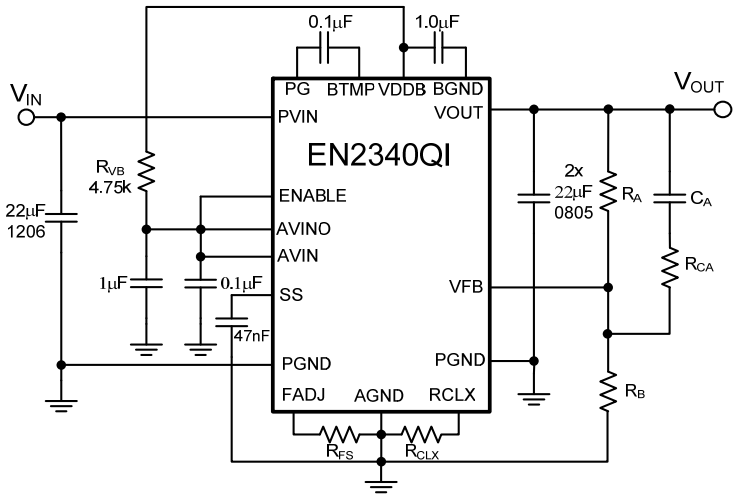


Figure 1. Simplified Applications Circuit (Footprint Optimized)

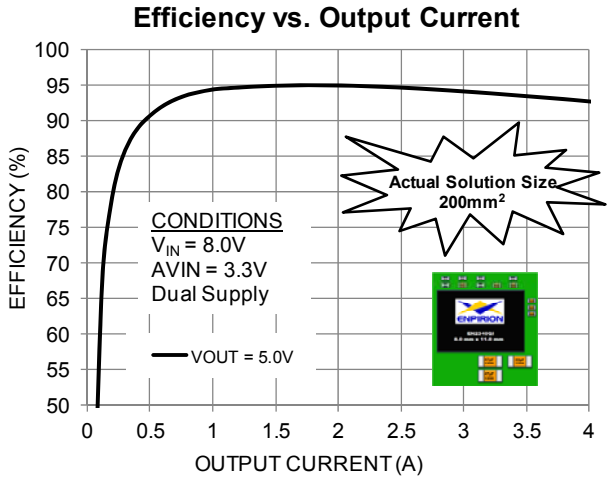


Figure 2. Highest Efficiency in Smallest Solution Size

Ordering Information

Part Number	Package Markings	Temp Rating (°C)	Package Description
EN2340QI	EN2340QI	-40 to +85	68-pin (8mm x 11mm x 3mm) QFN T&R
EN2340QI-E	EN2340QI	QFN Evaluation Board	

Packing and Marking Information: http://www.enpirion.com/resource-center-packing-and-marking-information.htm

Pin Assignments (Top View)

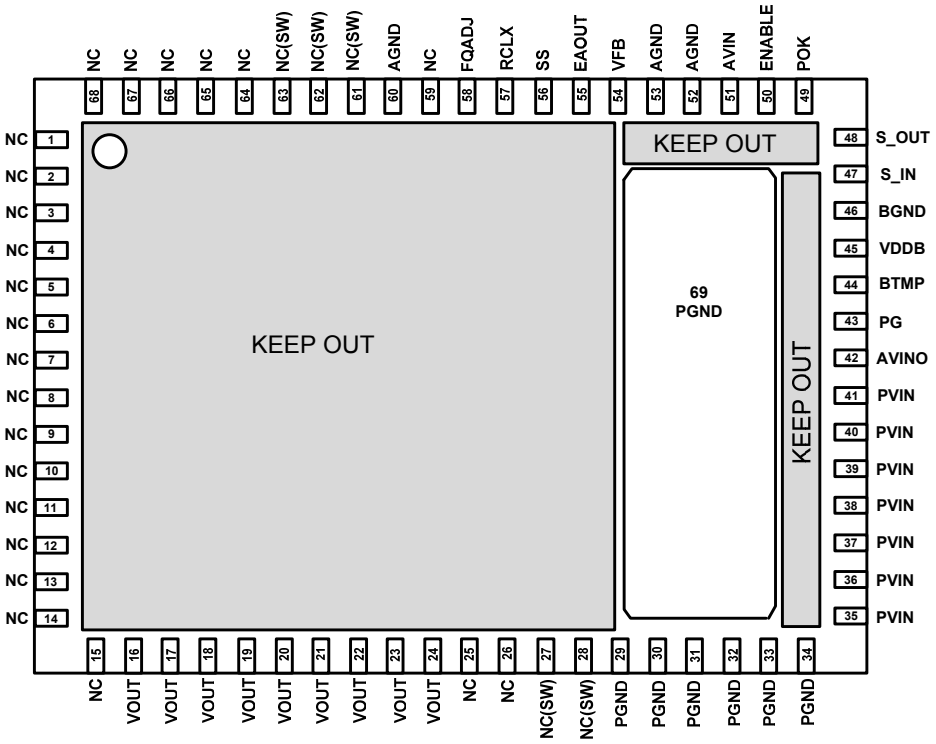


Figure 3: Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: Shaded area highlights exposed metal below the package that is not to be mechanically or electrically connected to the PCB. Refer to Figure 10 for details.

NOTE C: White 'dot' on top left is pin 1 indicator on top of the device package.

Pin Description

I/O Legend: P=Power G=Ground NC=No Connect I=Input O=Output I/O=Input/Output

PIN	NAME	I/O	FUNCTION
1-15, 25-26, 59, 64-68	NC	NC	NO CONNECT – These pins may be internally connected. Do not connect them to each other or to any other electrical signal. Failure to follow this guideline may result in device damage.
16-24	VOUT	O	Regulated converter output. Connect these pins to the load and place output capacitor between these pins and PGND pins 29-34.
27-28, 61-63	NC(SW)	NC	NO CONNECT – These pins are internally connected to the common switching node of the internal MOSFETs. They are not to be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in damage to the device.

PIN	NAME	I/O	FUNCTION
29-34	PGND	G	Input/output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. See VOUT and PVIN pin descriptions for more details.
35-41	PVIN	P	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND pins 29-34.
42	AVINO	O	Internal 3V linear regulator output. Connect this pin to AVIN (Pin 51) for applications where operation from a single input voltage (PVIN) is required. If AVINO is being used, place a 1µF, X5R/X7R, capacitor between AVINO and AGND as close as possible to AVINO.
43	PG	I/O	Place a 0.1µF, X5R/X7R, capacitor between this pin and BTMP.
44	BTMP	I/O	See pin 43 description.
45	VDDB	O	Internal regulated voltage used for the internal control circuitry. Place a 1.0µF, X7R, capacitor between this pin and BGND.
46	BGND	G	See pin 45 description.
47	S_IN	I	Digital Input. This pin accepts either an input clock to phase lock the internal switching frequency or a S_OUT signal from another EN2340QI. Leave this pin floating if not used.
48	S_OUT	O	Digital Output. PWM signal is output on this pin. Leave this pin floating if not used.
49	POK	O	Power OK is an open drain transistor (pulled up to AVIN or similar voltage) used for power system state indication. POK is logic high when VOUT is within -10% of VOUT nominal.
50	ENABLE	I	Input Enable. Applying a logic high to this pin enables the output and initiates a soft-start. Applying a logic Low disables the output. Do not leave floating.
51	AVIN	P	3.3V Input power supply for the controller. Place a 0.1µF, X7R, capacitor between AVIN and AGND.
52, 53, 60	AGND	G	Analog Ground. This is the Ground return for the controller. Needs to be connected to a quiet ground.
54	VFB	I/O	External Feedback Input. The feedback loop is closed through this pin. A voltage divider at VOUT is used to set the output voltage. The mid-point of the divider is connected to VFB. A phase lead capacitor from this pin to VOUT is also required to stabilize the loop.
55	EAOUT	O	Optional Error Amplifier output. Allows for customization of the control loop.
56	SS	I/O	Soft-Start node. The soft-start capacitor is connected between this pin and AGND. The value of this capacitor determines the startup time.
57	RCLX	I/O	Programmable over-current protection. Placement of a resistor on this pin will adjust the over-current protection threshold. See Table 2 for the recommended RCLX Value to set OCP at the nominal value specified in the Electrical Characteristics table.
58	FADJ	I/O	Adding a resistor (R_{FS}) to this pin will adjust the switching frequency of the EN2340QI. See Table 1 for suggested resistor values on R_{FS} for various PVIN/VOUT combinations to maximize efficiency. Do not leave floating.
69	PGND		Not a perimeter pin. Device thermal pad to be connected to the system GND plane for heat-sinking purposes.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Voltages on : PVIN, VOUT		-0.5	15	V
Voltages on: EN, POK, M/S		-0.3	V_{IN}+0.3	V
PVIN Slew Rate		0.3	3	V/ms
Pin Voltages – AVINO, AVIN, ENABLE, POK, S_IN, S_OUT		2.5	6.0	V
Pin Voltages – VFB, SS, EAOUT, RCLX, FADJ		-0.5	2.75	V
Storage Temperature Range	T_{STG}	-65	150	°C
Maximum Operating Junction Temperature	$T_{J\text{-}ABS\ Max}$		150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (based on Human Body Model)			2000	V
ESD Rating (based on CDM)			500	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	PVIN	4.5	14	V
AVIN: Controller Supply Voltage	AVIN	2.5	5.5	V
Output Voltage Range (Note 1)	V_{OUT}	0.75	5	V
Output Current	I_{OUT}		4	A
Operating Ambient Temperature	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient (0 LFM) (Note 2)	θ_{JA}	18	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	2	°C/W
Thermal Shutdown	T_{SD}	160	°C
Thermal Shutdown Hysteresis	T_{SDH}	35	°C

Note 1: RCLX resistor value may need to be raised for $V_{OUT} > V_{IN} – 2.5V$ to increase current limit threshold.

Note 2: Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

Electrical Characteristics

NOTE: V_{IN}=12V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	PVIN		4.5		14.0	V
Controller Input Voltage	AVIN		2.5		5.5	V
AVIN Under Voltage Lock-Out Rising	$AVIN_{UVLOR}$	Voltage above which UVLO is not asserted		2.3		V
AVIN Under Voltage Lock-Out Falling	$AVIN_{OVLOF}$	Voltage below which UVLO is asserted		2.1		V
AVIN pin Input Current	I_{AVIN}			7		mA
Internal Linear Regulator Output	AVINO			3.3		V
Shut-Down Supply Current	$IPVIN_S$	PVIN=12V, AVIN=3.3V, ENABLE=0V		500		µA
	$IAVIN_S$	PVIN=12V, AVIN=3.3V, ENABLE=0V		50		µA
Feedback Pin Voltage	V_{FB}	V_{IN} = 12V, I_{LOAD} = 0, T_A = 25°C Only	0.7425	0.750	0.7575	V
Feedback Pin Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 14V; 0A ≤ I_{LOAD} ≤ 4A	0.735	0.750	0.765	V
Feedback Pin Input Leakage Current	I_{FB}	VFB pin input leakage current (Note 3)	-5		5	nA
V_{OUT} Rise Time	t_{RISE}	C_{SS} = 47nF (Note 4 and Note 5)		3.2		ms
Soft-Start Capacitor Range	C_{SS_RANGE}		10	47	68	nF
Maximum Continuous Output Current	$I_{OUT\_Max\_Cont}$				4	A
Over Current Trip Level	I_{OCP}	Reference Table 2		6		A
Disable Threshold	$V_{DISABLE}$	ENABLE pin logic Low	0.0		0.6	V
ENABLE Threshold	V_{ENABLE}	ENABLE pin logic High	1.8		AVIN	V
ENABLE Lockout Time	$T_{ENLOCKOUT}$			8		ms
ENABLE Input Current	I_{ENABLE}	180k internal pull-down (Note 3)		4		µA
Switching Frequency	F_{SW}	R_{FS} =3kΩ		1.0		MHz
External SYNC Clock Frequency Lock Range	F_{PLL_LOCK}	Range of SYNC clock frequency	0.9		1.3	MHz
S_IN Threshold – Low	$V_{S\_IN\_LO}$	S_IN clock logic low level			0.8	V
S_IN Threshold – High	$V_{S\_IN\_HI}$	S_IN clock logic high level	1.8		2.5	V
S_OUT Threshold – Low	$V_{S\_OUT\_LO}$	S_OUT clock logic low level			0.8	V
S_OUT Threshold – High	$V_{S\_OUT\_HI}$	S_OUT clock logic high level	1.8		2.5	V
POK Lower Threshold	POK_{LT}	V_{OUT} / V_{OUT_NOM}		90		%
POK Output low Voltage	V_{POKL}	With 4mA current sink into POK			0.4	V
POK Output Hi Voltage	V_{POKH}	PVIN range: 4.5V ≤ V_{IN} ≤ 14V			AVIN	V
POK pin V_{OH} leakage current (Note 3)	I_{POKL}	POK high			1	µA

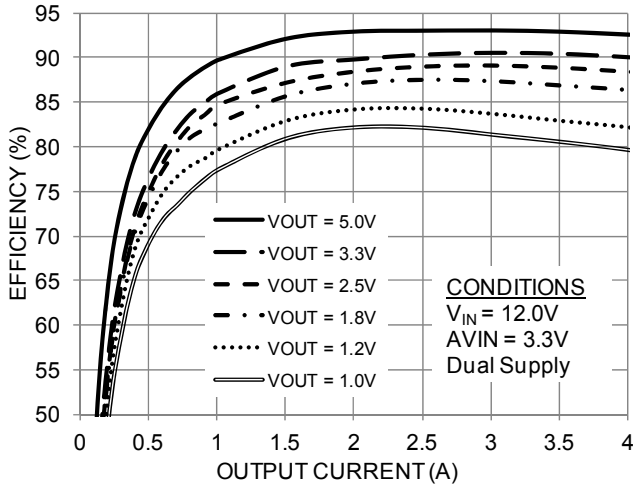
Note 3: Parameter not production tested but is guaranteed by design.

Note 4: Rise time calculation begins when AVIN > V_{UVLO} and ENABLE = HIGH.

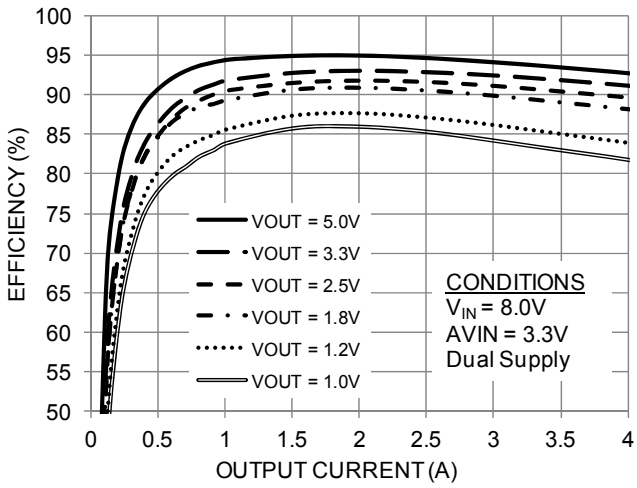
Note 5: V_{OUT} Rise Time Accuracy does not include soft-start capacitor tolerance.

Typical Performance Curves

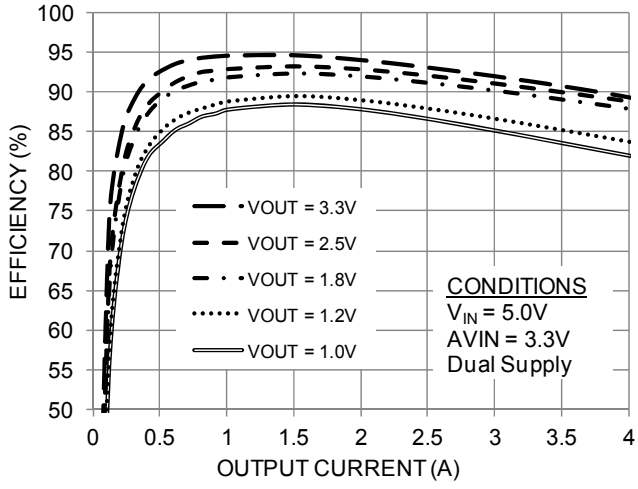
Efficiency vs. Output Current



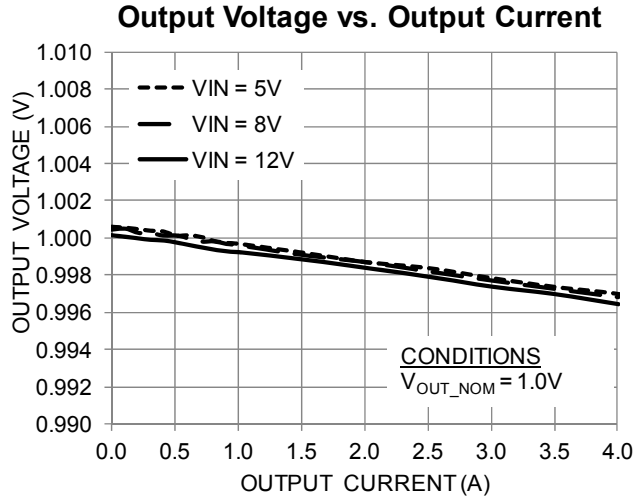
Efficiency vs. Output Current



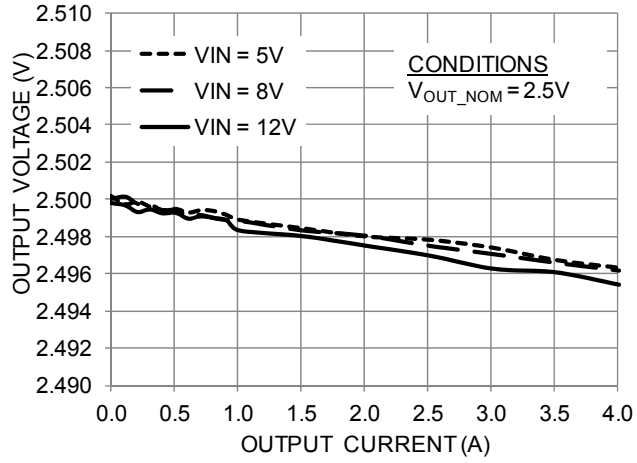
Efficiency vs. Output Current



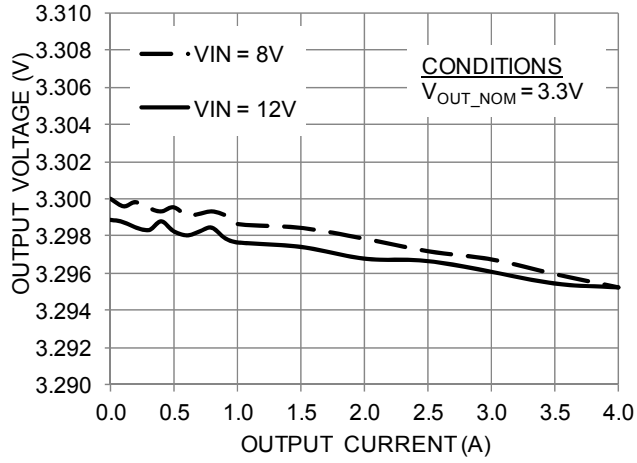
Output Voltage vs. Output Current



Output Voltage vs. Output Current

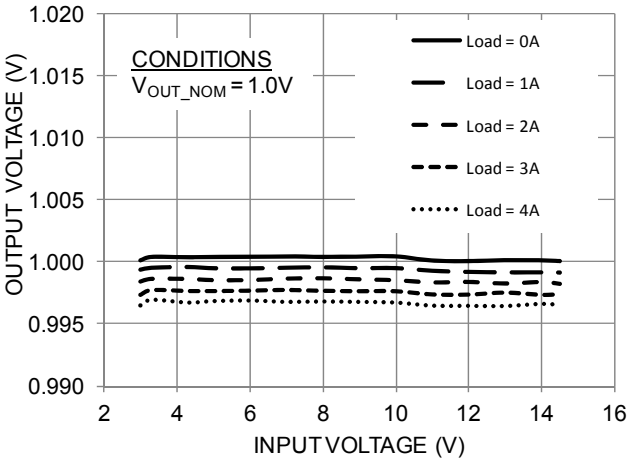


Output Voltage vs. Output Current

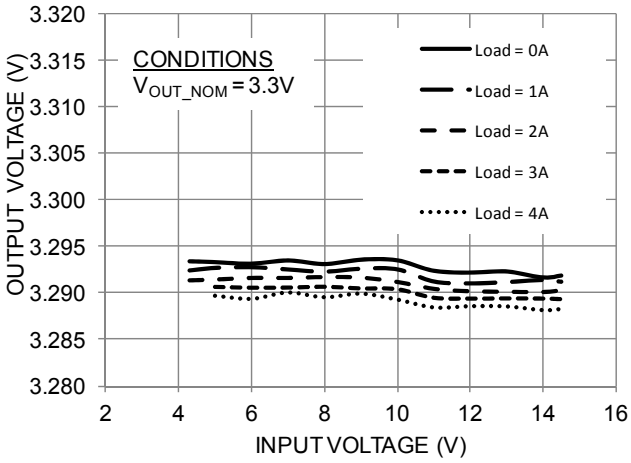


Typical Performance Curves (Continued)

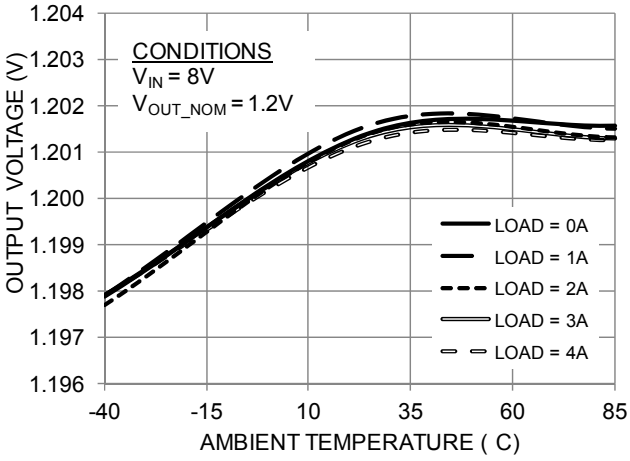
Output Voltage vs. Input Voltage



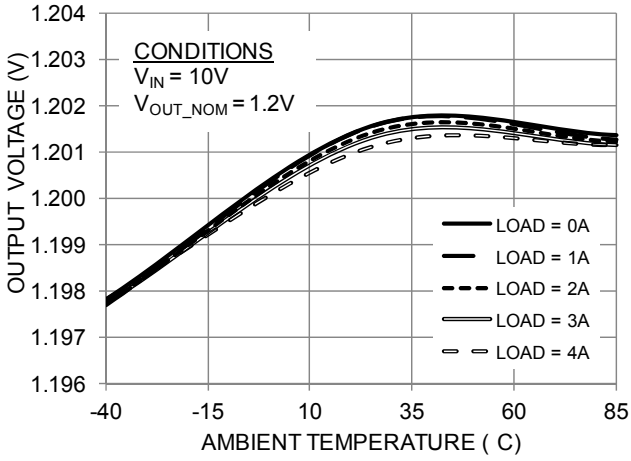
Output Voltage vs. Input Voltage



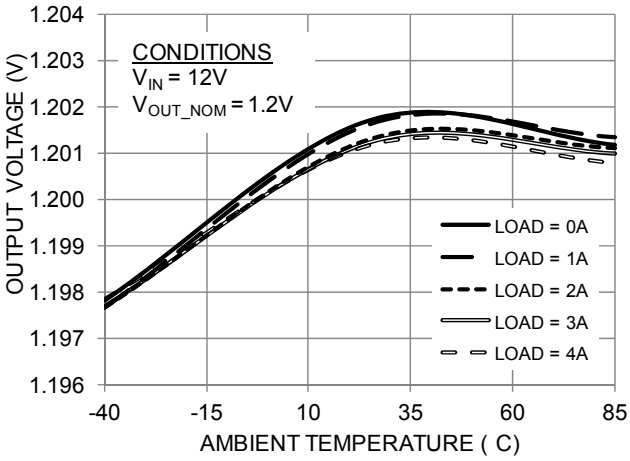
Output Voltage vs. Temperature



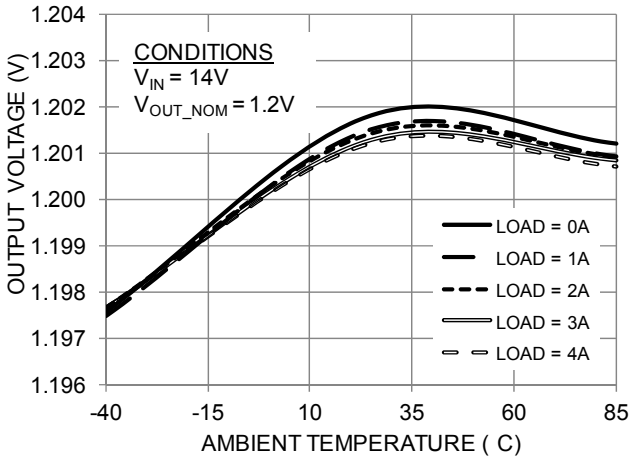
Output Voltage vs. Temperature



Output Voltage vs. Temperature

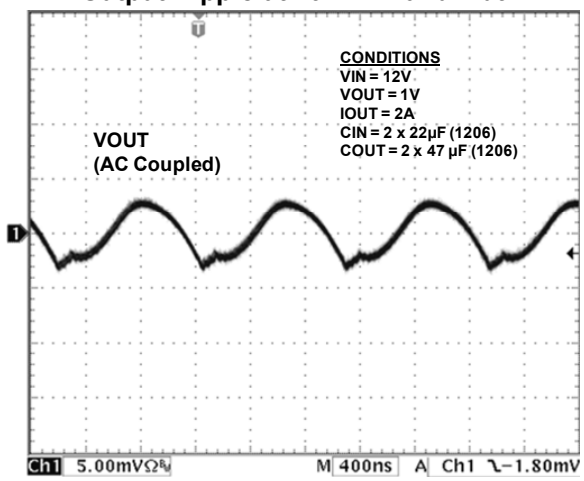


Output Voltage vs. Temperature

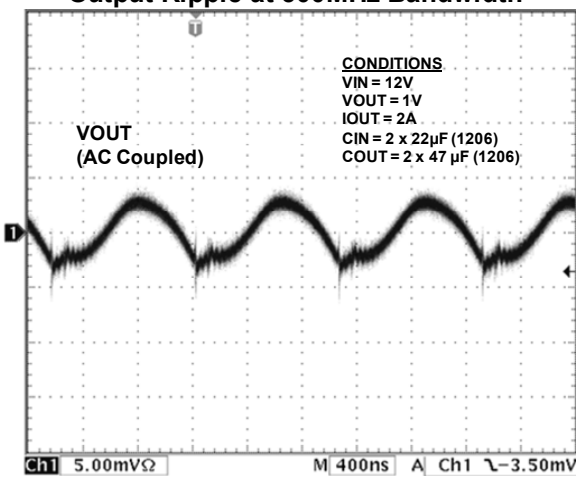


Typical Performance Characteristics

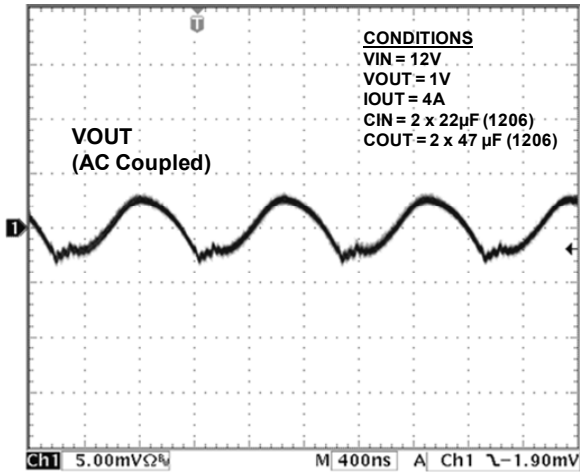
Output Ripple at 20MHz Bandwidth



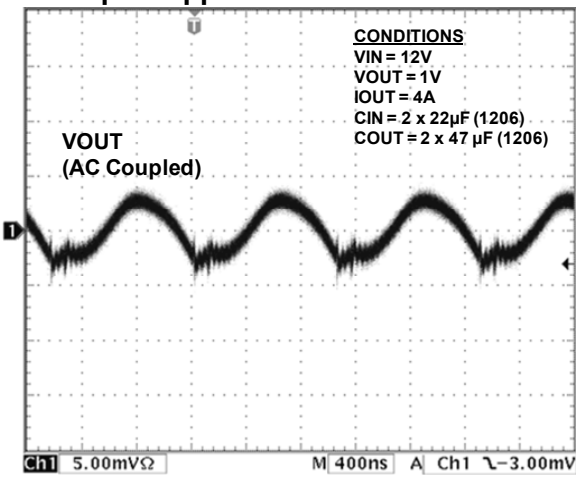
Output Ripple at 500MHz Bandwidth



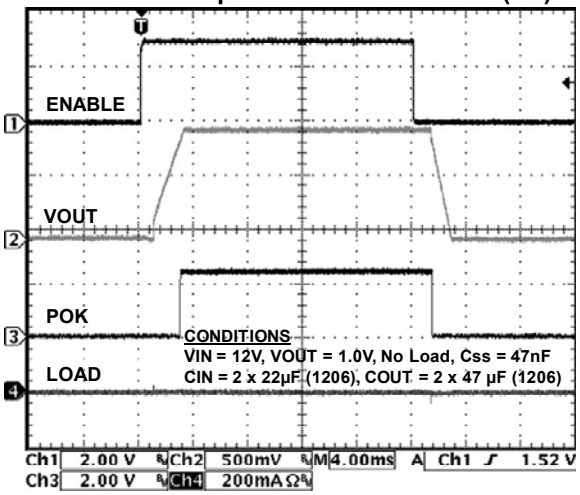
Output Ripple at 20MHz Bandwidth



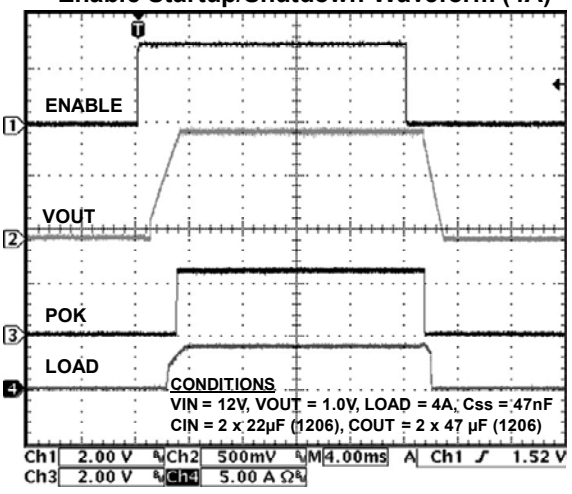
Output Ripple at 500MHz Bandwidth



Enable Startup/Shutdown Waveform (0A)

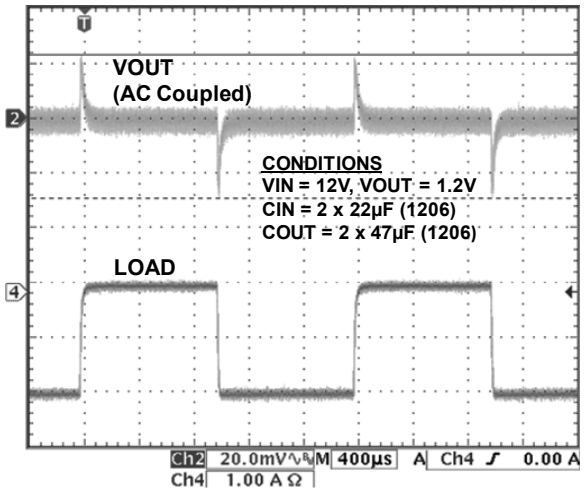


Enable Startup/Shutdown Waveform (4A)

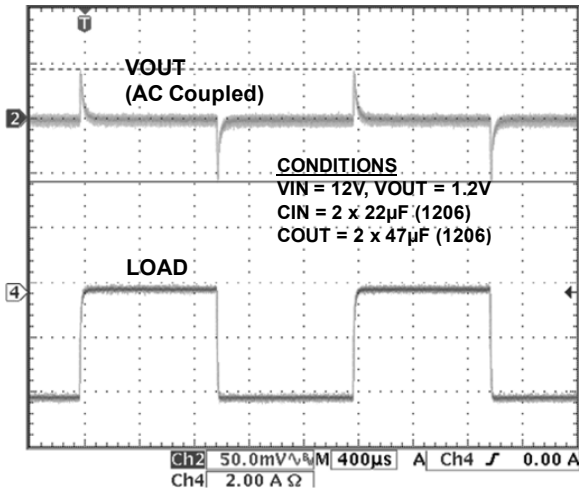


Typical Performance Characteristics (Continued)

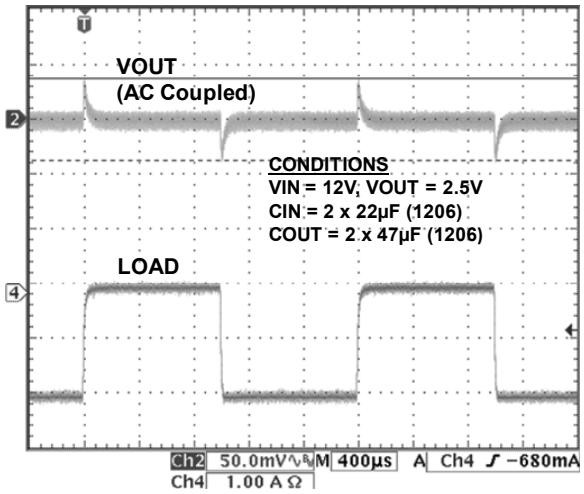
Load Transient from 0 to 2A



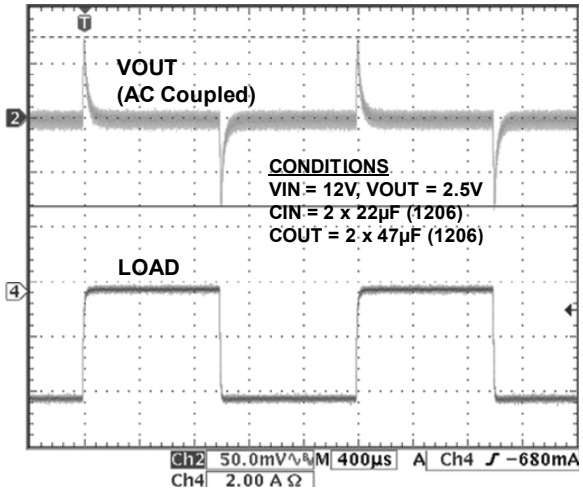
Load Transient from 0 to 4A



Load Transient from 0 to 2A



Load Transient from 0 to 4A



Functional Block Diagram

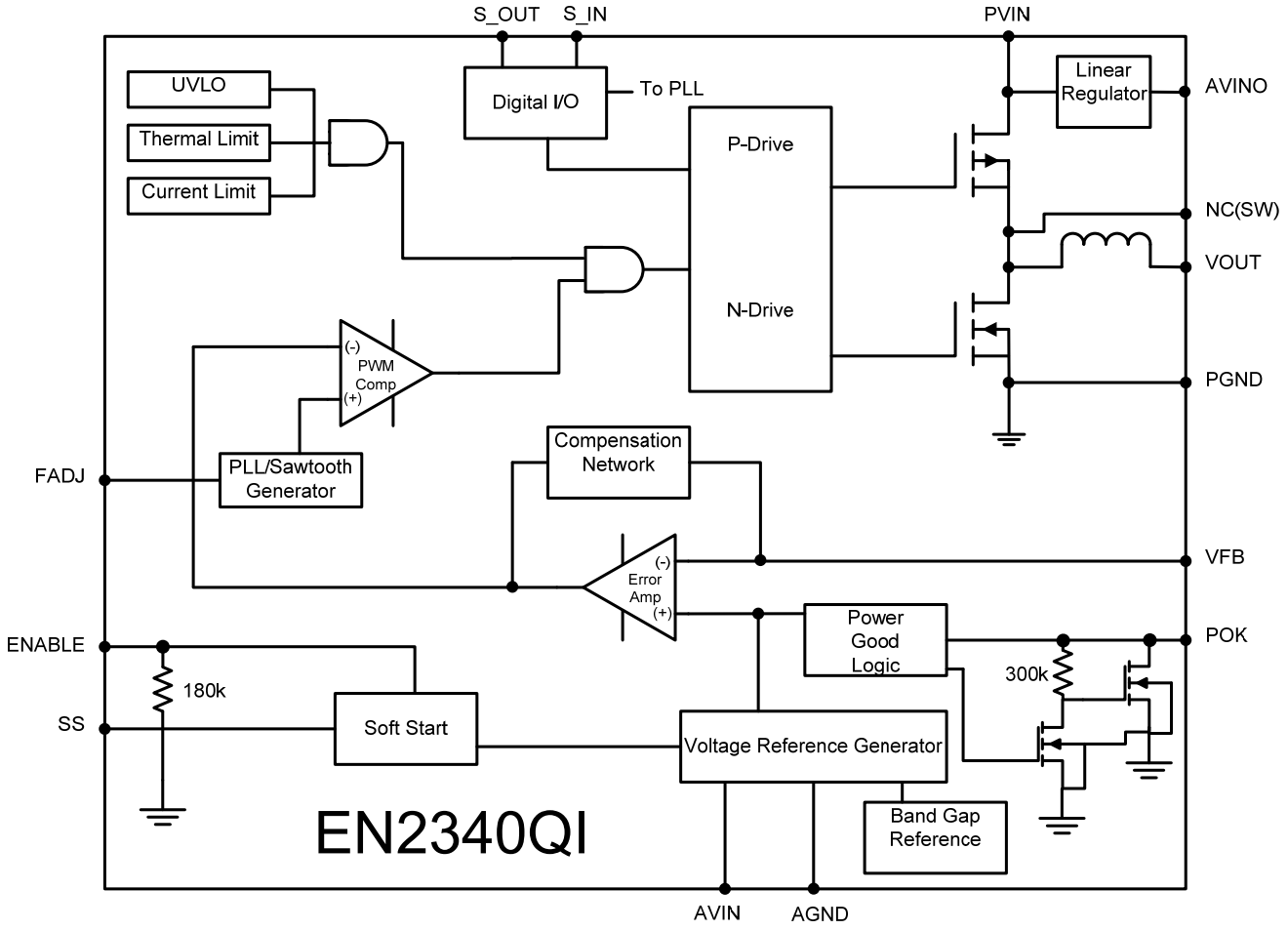


Figure 4: Functional Block Diagram

Functional Description

Synchronous Buck Converter

The EN2340QI is a highly integrated synchronous, buck converter with integrated controller, power MOSFET switches and integrated inductor. The nominal input voltage (PVIN) range is 4.5V to 14V and can support up to 4A of continuous output current. The output voltage is programmed using an external resistor divider network. The control loop utilizes a Type IV Voltage-Mode compensation network and maximizes on a low-noise PWM topology. Much of the compensation circuitry is internal to the device. However, a phase lead capacitor is required along with the output voltage feedback resistor divider to complete the Type IV compensation network.. The high switching frequency of the EN2340QI enables the use of small size input and output capacitors, as well as a wide loop bandwidth within a small foot print.

Protection Features:

The power supply has the following protection features:

- Programmable Over-Current Protection
- Thermal Shutdown with Hysteresis.
- Under-Voltage Lockout Protection

Additional Features:

- Switching Frequency Synchronization.
- Programmable Soft-Start
- Power OK Output Monitoring

Power Up Sequence

The EN2340QI is designed to be powered by either a single input supply (PVIN) or two separate supplies: one for PVIN and the other for AVIN.

Single Input Supply Application (PVIN):

The EN2340QI has an internal linear regulator that converts PVIN to 3.0V. The output of the linear regulator is provided on the AVINO pin. AVINO should be connected to AVIN on the EN2340QI. In this application, the following external components are required: Place a 1µF, X5R/X7R, capacitor between AVINO and AGND as close as possible to AVINO. Place a 0.1µF, X5R/X7R, capacitor between AVIN and AGND as close as possible to AVIN. In addition, place a resistor (R_{VB}) between VDDB and AVIN, as shown in Figure 1. Enpirion recommends R_{VB}=4.75kΩ. In this application, ENABLE cannot be asserted before PVIN. If no external enable signal is used, tying ENABLE to AVIN meets this requirement.

Dual Input Supply Application (PVIN and AVIN):

In this application, place a 0.1µF, X7R, capacitor between AVIN and AGND as close as possible to AVIN. Refer to Figure 5 for a recommended schematic for a dual input supply application.

For dual input supply applications, the sequencing of the two input supplies, PVIN and AVIN, is very important. During power up, neither ENABLE nor PVIN should be asserted before AVIN. There are two common acceptable turn-on/off sequences for the device. ENABLE can be tied to AVIN and come up with it, and PVIN can be ramped up and down as needed. Alternatively, PVIN can be brought high after AVIN is asserted, and the device can be turned on and off by toggling the ENABLE pin.

Enable Operation

The ENABLE pin provides a means to enable normal operation or to shut down the device. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted (high) the device will undergo a normal soft-start. A logic low will disable the converter. A logic low will power down the device in a controlled manner and the device is subsequently shut down. The ENABLE signal has to be low for at least the ENABLE Lockout Time (8ms) in order for the device to be re-enabled.

Pre-Bias Operation

The EN2340QI is not designed to be turned on into a pre-biased output voltage.

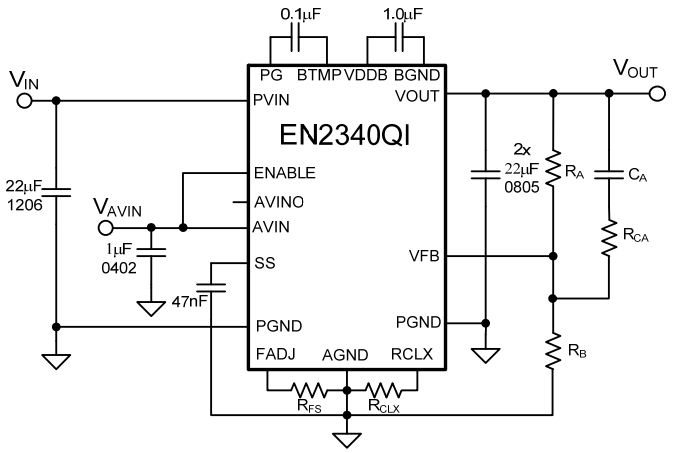


Figure 5: Dual Input Supply (PVIN and AVIN) Recommended Schematic

Frequency Synchronization

The switching frequency of the EN2340QI can be phase-locked to an external clock source to move unwanted beat frequencies out of band. The internal switching clock of the EN2340QI can be phase locked to a clock signal applied to the S_IN pin. An activity detector recognizes the presence of an external clock signal and automatically phase-locks the internal oscillator to this external clock. Phase-lock will occur as long as the input clock frequency is in the range of 0.9MHz to 1.3MHz. When no clock is present, the device reverts to the free running frequency of the internal oscillator. Adding a resistor (R_{FS}) to the FADJ pin will adjust the frequency lower. If a 3KΩ resistor is placed on FADJ the nominal switching frequency of the EN2340QI is 1MHz. The efficiency performance of the EN2340QI for various PVIN/VOUT combinations can be optimized by adjusting the switching frequency. Table 1 shows recommended R_{FS} values for various PVIN/VOUT combinations in order to optimize performance of the EN2340QI.

PVIN	VOUT	R_{FS}
12V	5.0V	15K
	3.3V	15K
	2.5V	10K
	1.2V	1.65K
	1.0V	1.3K
5V	2.5V	22.1K
	1.2V	4.87K
	1.0V	3.01K

Table 1: Recommended R_{FS} Values

Spread Spectrum Mode

The external clock frequency may be swept between 0.9MHz and 1.3MHz at repetition rates of up to 10 kHz in order to reduce EMI frequency components.

Soft-Start Operation

Soft start is a means to ramp the output voltage gradually upon start-up. The output voltage rise time is controlled by the choice of soft-start capacitor, which is placed between the SS pin (pin 56) and the AGND pin (pin 52).

Rise Time (ms): $T_R \approx C_{ss}$ [nF] x 0.067

During start-up of the converter, the reference voltage to the error amplifier is linearly increased to its final level by an internal current source of approximately 10µA. Typical soft-start rise time is ~3.2ms with SS capacitor value of 47nF. The rise time is measured from when $V_{IN} > V_{UVLOR}$ and ENABLE pin voltage crosses its logic high threshold to when V_{OUT} reaches its programmed value.

POK Operation

The POK signal is an open drain signal (requires a pull up resistor to AVIN or similar voltage) from the converter indicating the output voltage is within the specified range. Typically, a 100kΩ or lower resistance is used as the pull-up resistor. The POK signal will be logic high (AVIN) when the output voltage is above 90% of the programmed V_{OUT}. If the output voltage goes outside of this range, the POK signal will be a logic low.

Over-Current Protection (OCP)

The current limit function is achieved by sensing the current flowing through a sense PFET. When the sensed current exceeds the current limit, both power FETs are turned off for the rest of the switching cycle. If the over-current condition is removed, the over-current protection circuit will re-enable PWM operation. If the over-current condition persists, the circuit will continue to protect the load.

The OCP trip point is nominally set as specified in the Electrical Characteristics table. In the event the OCP circuit trips consistently in normal operation, the device enters a hiccup mode. While in hiccup mode, the device is disabled for a short while and restarted with a normal soft-start. The hiccup time is approximately 32ms. This cycle can continue indefinitely as long as the over current condition persists.

The OCP trip point can be programmed to trip at a lower level via the RCLX pin. The value of the resistor connected between RCLX and ground will determine the OCP trip point. Generally, the higher the RCLX value, the higher the current limit threshold. Note that if RCLX pin is left open the output current will be unlimited and the device will not have current limit protection. Reference Table 2 for a list of recommended resistor values on RCLX that will set the OCP trip point at the typical value of 6A, also specified in the Electrical Characteristics table.

V_{OUT} Range	R_{CLX} Value
$0.75V < V_{OUT} \leq 1.2V$	31.6kΩ
$1.2V < V_{OUT} \leq 2.0V$	33.2kΩ
$2.0V < V_{OUT} \leq 5.0V$	36.5kΩ

Table 2: Recommended R_{CLX} Values vs. V_{OUT}

Thermal Overload Protection

Thermal shutdown circuit will disable device operation when the junction temperature exceeds approximately 150ºC. After a thermal shutdown event, when the junction temperature drops by approx 20ºC, the converter will re-start with a normal soft-start.

Input Under-Voltage Lock-Out (UVLO)

Internal circuits ensure that the converter will not start switching until the input voltage is above the specified minimum voltage. Hysteresis, input de-glitch and output leading edge blanking ensures high noise immunity and prevents false UVLO triggers.

Application Information

Output Voltage Programming and Loop Compensation

The EN2340QI output voltage is programmed using a simple resistor divider network. A phase lead capacitor (C_A) plus a resistor (R_{CA}) are required for stabilizing the loop. Figure 6 shows the required components and the equations to calculate their values. The values recommended for C_A and R_{CA} will vary with each PVIN and VOUT combination. The EN2340 solution can be optimized for either smallest size or highest performance. Please see Table 5 for a list of recommended C_A and R_{CA} values for each solution option.

The EN2340QI output voltage is determined by the voltage presented at the VFB pin. This voltage is set by way of a resistor divider between VOUT and AGND with the midpoint going to VFB.

The EN2340QI uses a type IV compensation network. Most of this network is integrated. However a phase lead capacitor and a resistor are required in parallel with the upper resistor of the external feedback network (see Figure 6). Total compensation is optimized for either low output ripple or small solution size, and will result in a wide loop bandwidth and excellent load transient performance for most applications. See Table 5 for compensation values for both options based on input and output voltage conditions.

In some cases modifications to the compensation may be required. The EN2340QI provides the capability to modify the control loop response to allow for customization for specific applications. For more information, contact Enpirion Applications Engineering support (techsupport@enpirion.com).

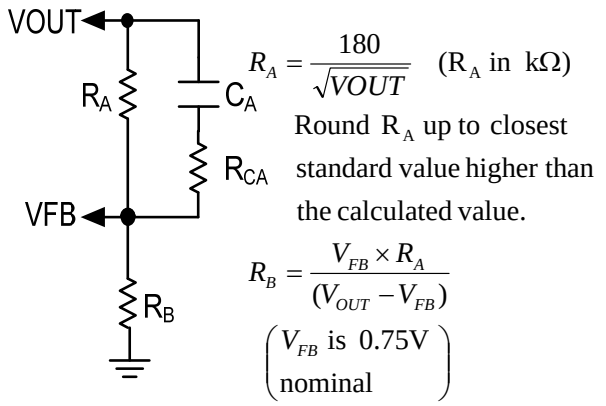


Figure 6: V_{OUT} Resistor Divider & Compensation Components. RA equation is only valid for Low V_{OUT} ripple option. For small solution size, see Table 5.

Input Capacitor Selection

The EN2340QI requires a 22µF/1206 input capacitor. Low-cost, low-ESR ceramic capacitors should be used as input capacitors for this converter. The dielectric must be X5R or X7R rated. **Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.** In some applications, lower value capacitors are needed in parallel with the larger, capacitors in order to provide high frequency decoupling. Table 3 contains a list of recommended input capacitors.

Recommended Input Capacitors

Description	MFG	P/N
22µF, 16V, X5R, 10%, 1206	Murata	GRM31CR61C226ME15
22µF, 16V, X5R, 20%, 1206	Taiyo Yuden	EMK316ABJ226ML-T

Table 3: Recommended Input Capacitors

Output Capacitor Selection

As seen from Table 5, the EN2340QI has been optimized for use with either two 47µF/1206 or two 22µF/0805 output capacitors. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. **Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.** Table 4 contains a list of recommended output capacitors

Output ripple voltage is determined by the aggregate output capacitor impedance. Capacitor impedance, denoted as Z, is comprised of capacitive reactance, effective series resistance, ESR, and effective series inductance, ESL reactance.

Placing output capacitors in parallel reduces the impedance and will hence result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

Recommended Output Capacitors

Description	MFG	P/N
47µF, 6.3V, X5R, 20%, 1206	Murata	GRM31CR60J476ME19L
47µF, 10V, X5R, 20%, 1206	Taiyo Yuden	LMK316BJ476ML-T
22µF, 10V, X5R, 20%, 0805	Panasonic	ECJ-2FB1A226M
22µF, 10V, X5R, 20%, 0805	Taiyo Yuden	LMK212BJ226MG-T

Table 4: Recommended Output Capacitors

		Low V_{OUT} Ripple C_{IN} = 1 x 22µF/1206 C_{OUT} = 2 x 47µF/1206 R_A= 180/(Vout$^{0.5}$) kΩ				Smallest Solution Size C_{IN} = 1 x 22µF/1206 C_{OUT} = 2 x 22µF/0805				
PVIN	**V_{OUT}**	**C_A (pF)**	**R_{CA} (kΩ)**	**Nominal Ripple (mV)**	**Nominal Deviation (mV) (Note 6)**	**R_A (kΩ)**	**C_A (pF)**	**R_{CA} (kΩ)**	**Nominal Ripple (mV)**	**Nominal Deviation (mV) (Note 6)**
14V	≤1.0V	10	30	≤5	≤47	75	27	0.1	≤10	≤34
	1.2V	12	27	6	48	43	39	0.1	13	33
	1.5V	15	27	5	53	56	39	0.1	15	38
	1.8V	22	27	6	54	56	39	0.1	18	41
	2.5V	27	24	8	55	51	39	0.1	26	59
	3.3V	39	18	11	63	51	33	0.1	35	63
	5.0V	47	8.2	18	97	75	22	5.1	42	115
12V	≤1.0V	18	22	≤4	≤48	27	47	0.1	≤10	≤35
	1.2V	22	22	5	49	75	47	0.1	13	37
	1.5V	27	20	5	53	75	47	0.1	15	38
	1.8V	33	20	6	54	75	47	0.1	17	44
	2.5V	47	18	7	54	56	47	0.1	25	59
	3.3V	56	15	10	66	51	39	0.1	32	63
	5.0V	56	10	16	99	75	22	5.1	39	128
10V	≤1.0V	33	18	≤3	≤45	27	82	0.1	≤9	≤35
	1.2V	39	18	4	46	30	100	0.1	13	39
	1.5V	47	18	5	54	30	100	0.1	14	43
	1.8V	56	16	6	56	30	100	0.1	17	50
	2.5V	68	12	7	57	75	56	0.1	26	70
	3.3V	82	10	9	68	56	47	0.1	30	83
	5.0V	100	4.3	14	98	75	33	5.1	33	140
8.0V	≤1.0V	100	8.2	≤3	≤51	100	100	0.1	≤10	≤41
	1.2V	100	8.2	4	51	100	100	0.1	12	43
	1.5V	100	8.2	4	54	100	100	0.1	14	46
	1.8V	100	8.2	5	57	100	100	0.1	16	53
	2.5V	100	8.2	6	64	91	82	0.1	23	71
	3.3V	100	8.2	8	70	75	56	0.1	25	85
	5.0V	100	8.2	10	110	75	56	5.1	30	127
6.6V	≤1.0V	100	8.2	≤3	≤60	100	100	0.1	≤9	≤46
	1.2V	100	8.2	4	63	100	100	0.1	12	51
	1.5V	100	8.2	4	65	100	100	0.1	14	56
	1.8V	100	8.2	5	68	100	100	0.1	16	61
	2.5V	100	8.2	5	75	100	100	0.1	19	83
	3.3V	100	8.2	6	85	91	82	0.1	22	106
5V	≤1.0V	100	8.2	≤3	≤73	100	100	0.1	≤9	≤56
	1.2V	100	8.2	3	75	100	100	0.1	11	63
	1.5V	100	8.2	4	76	100	100	0.1	13	70
	1.8V	100	8.2	4	80	100	100	0.1	13	78
	2.5V	100	8.2	4	88	100	100	0.1	14	98

Table 5: R_A, C_A, and R_{CA} Values for Various PVIN/VOUT Combinations: Low V_{OUT} Ripple vs. Smallest Solution Size. See Figure 6. Use the equations in Figure 6 to calculate R_A (for low V_{OUT} ripple option) and R_B.

Note 6: Nominal Deviation is for a 2A load transient step.

Thermal Considerations

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be accounted for. The Enpirion PowerSoC helps alleviate some of those concerns.

The Enpirion EN2340QI DC-DC converter is packaged in an 8x11x3mm 68-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 150°C.

The EN2340QI is guaranteed to support the full 4A output current up to 85°C ambient temperature. The following example and calculations illustrate the thermal performance of the EN2340QI.

Example:

V_{IN} = 12V

V_{OUT} = 3.3V

I_{OUT} = 4A

First calculate the output power.

P_{OUT} = 3.3V x 4A = 13.2W

Next, determine the input power based on the efficiency (η) shown in Figure 7.

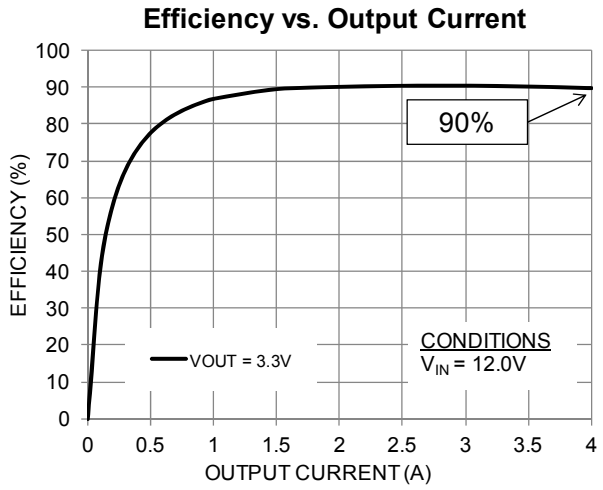


Figure 7: Efficiency vs. Output Current

For V_{IN} = 12V, V_{OUT} = 3.3V at 4A, η ≈ 90%

η = P_{OUT} / P_{IN} = 90% = 0.9

P_{IN} = P_{OUT} / η

P_{IN} ≈ 13.2W / 0.9 ≈ 14.67W

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

P_D = P_{IN} – P_{OUT}

≈ 14.67W – 13.2W ≈ 1.47W

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EN2340QI has a θ_{JA} value of 18 ºC/W without airflow.

Determine the change in temperature (ΔT) based on P_D and θ_{JA}.

ΔT = P_D x θ_{JA}

ΔT ≈ 1.47W x 18°C/W = 26.46°C ≈ 27°C

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

T_J = T_A + ΔT

T_J ≈ 25°C + 27°C ≈ 52°C

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

T_{AMAX} = T_{JMAX} – P_D x θ_{JA}

≈ 125°C – 27°C ≈ 98°C

The maximum ambient temperature the device can reach is 98°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.

Engineering Schematic

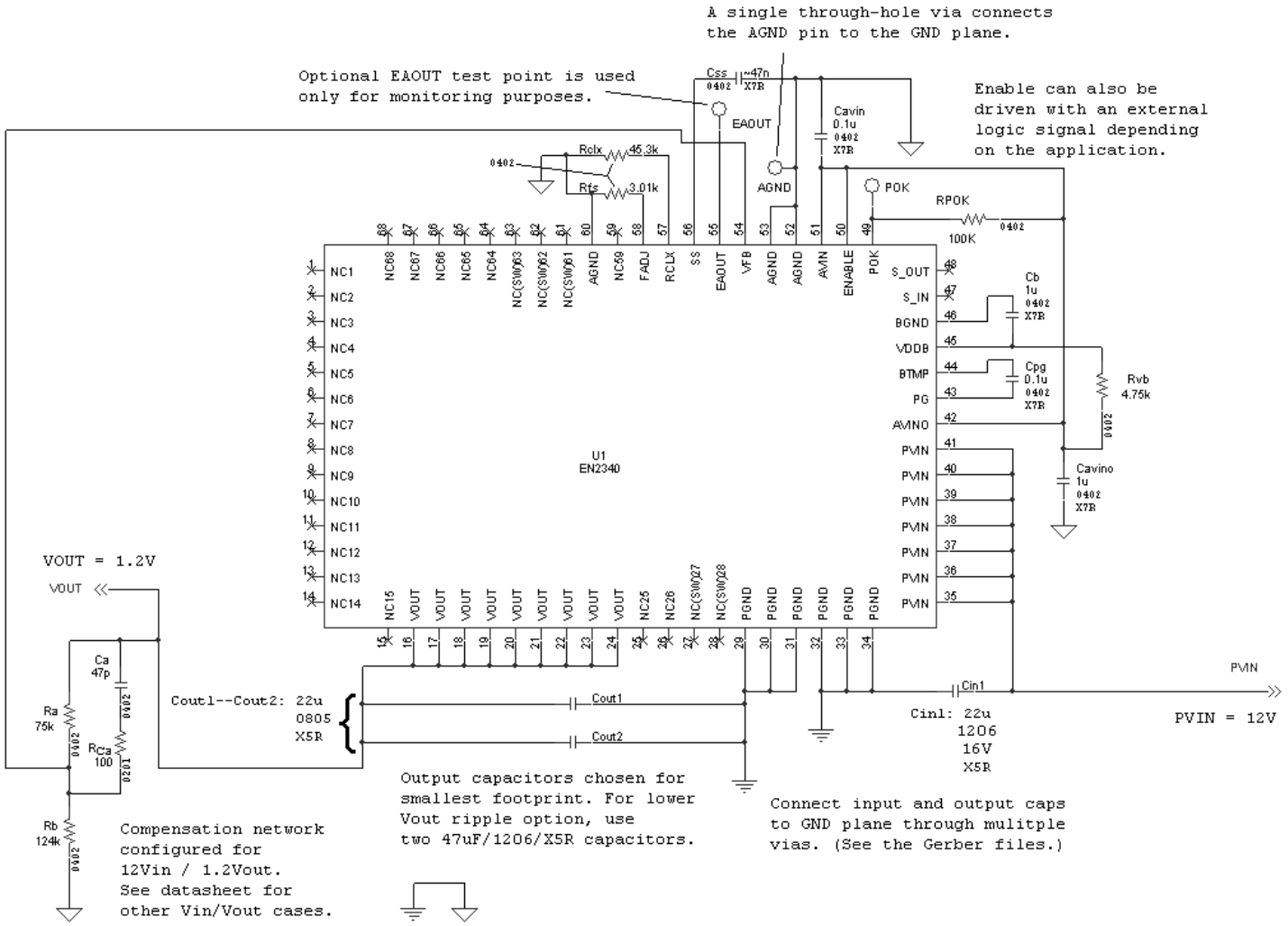


Figure 8: Engineering Schematic with Engineering Notes

Layout Recommendation

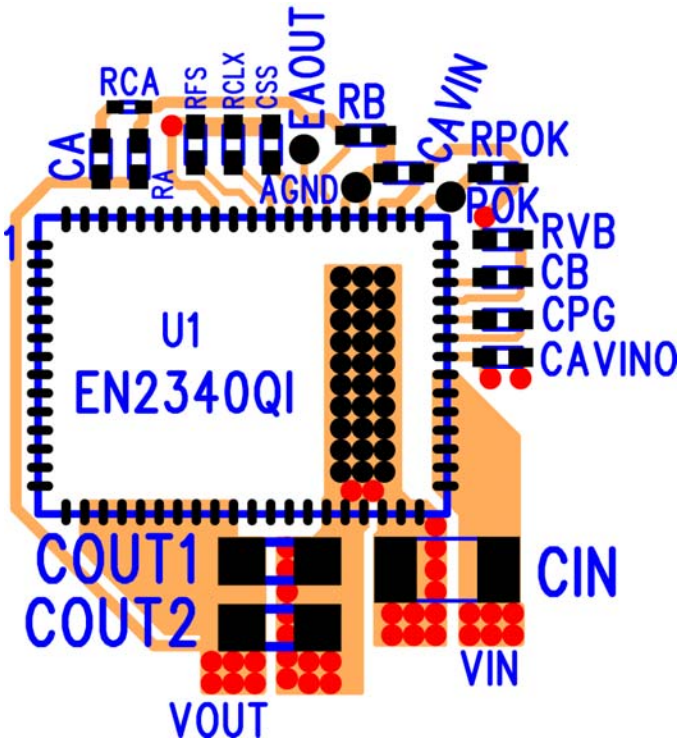


Figure 9: Top Layer Layout with Critical Components (Top View). See Figure 8 for corresponding schematic.

This layout only shows the critical components and top layer traces for minimum footprint in single-supply mode with ENABLE tied to AVIN. Alternate circuit configurations & other low-power pins need to be connected and routed according to customer application. Please see the Gerber files at www.enpirion.com for details on all layers.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN2340QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN2340QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The PGND connections for the input and output capacitors on layer 1 need to have a slit between them in order to provide some separation between input and output current loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors.

Recommendation 4: The thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

Recommendation 5: Multiple small vias (the same size as the thermal vias discussed in recommendation 4) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops. If vias cannot be placed under the capacitors, then place them on both sides of the slit in the top layer PGND copper.

Recommendation 6: AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 9 this connection is made at the input capacitor.

Recommendation 7: The layer 1 metal under the device must not be more than shown in Figure 9. Refer to the section regarding Exposed Metal on Bottom of Package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 8: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node. Contact Enpirion Technical Support for any remote sensing applications.

Recommendation 9: Keep R_A, C_A, R_B, and R_{CA} close to the VFB pin (Refer to Figure 9). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pins 52 and 53 instead of going through the GND plane.

Recommendation 10: Follow all the layout recommendations as close as possible to optimize performance. Enpirion provides schematic and layout reviews for all customer designs. Contact Enpirion Applications Engineering for detailed support (techsupport@enpirion.com).

Design Considerations for Lead-Frame Based Modules

Exposed Metal on Bottom of Package

Lead-frames offer many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package, as shown in Figure 10.

Only the thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN2340QI should be clear of any metal (copper pours, traces, or vias) except for the thermal pad. The “shaded-out” area in Figure 10 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the shaded-out area runs the risk of undesirable shorted connections even if it is covered by soldermask.

The solder stencil aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package. Please consult the Enpirion Manufacturing Application Note for more details and recommendations.

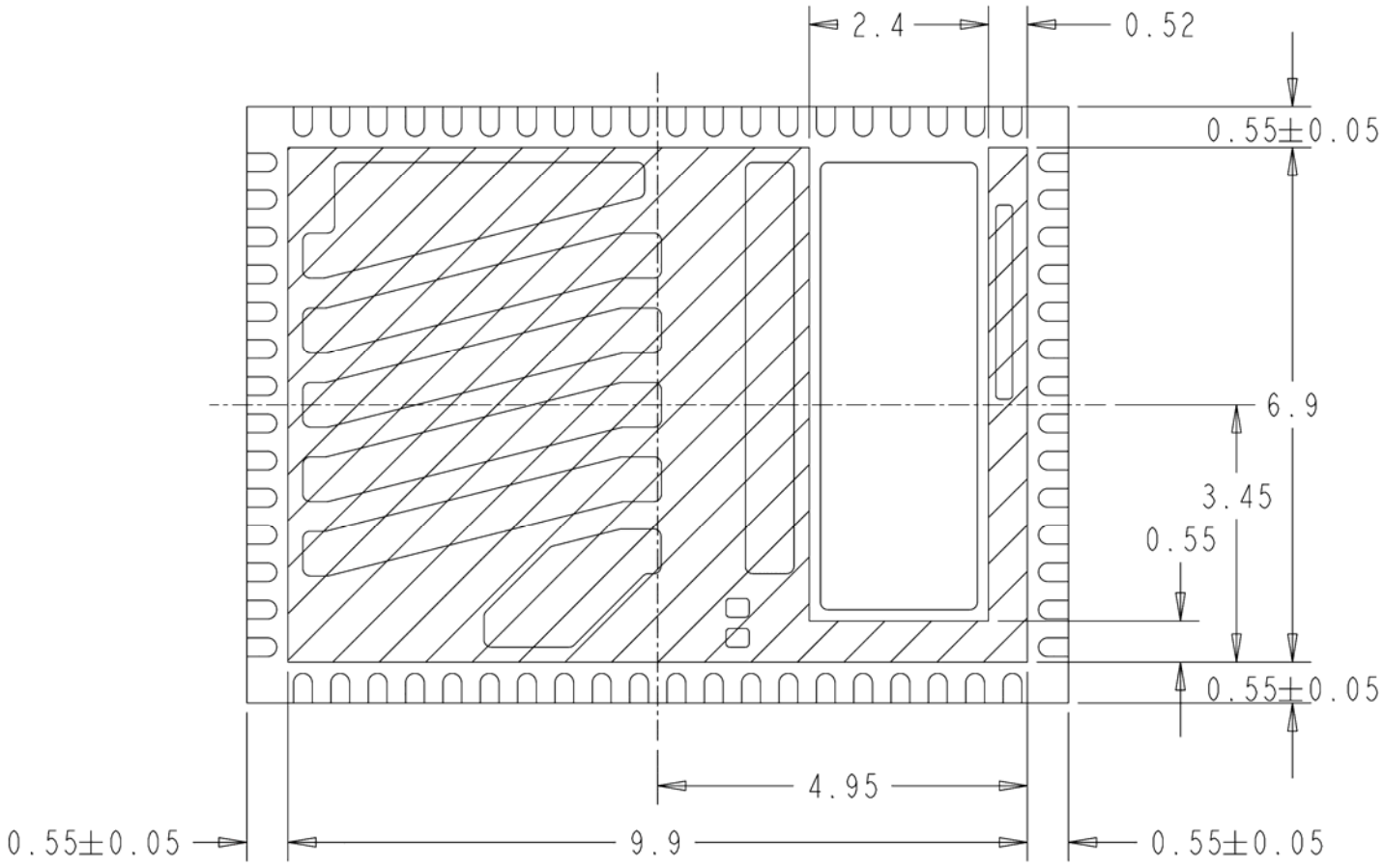


Figure 10: Lead-Frame exposed metal (Bottom View)

Shaded area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

Recommended PCB Footprint

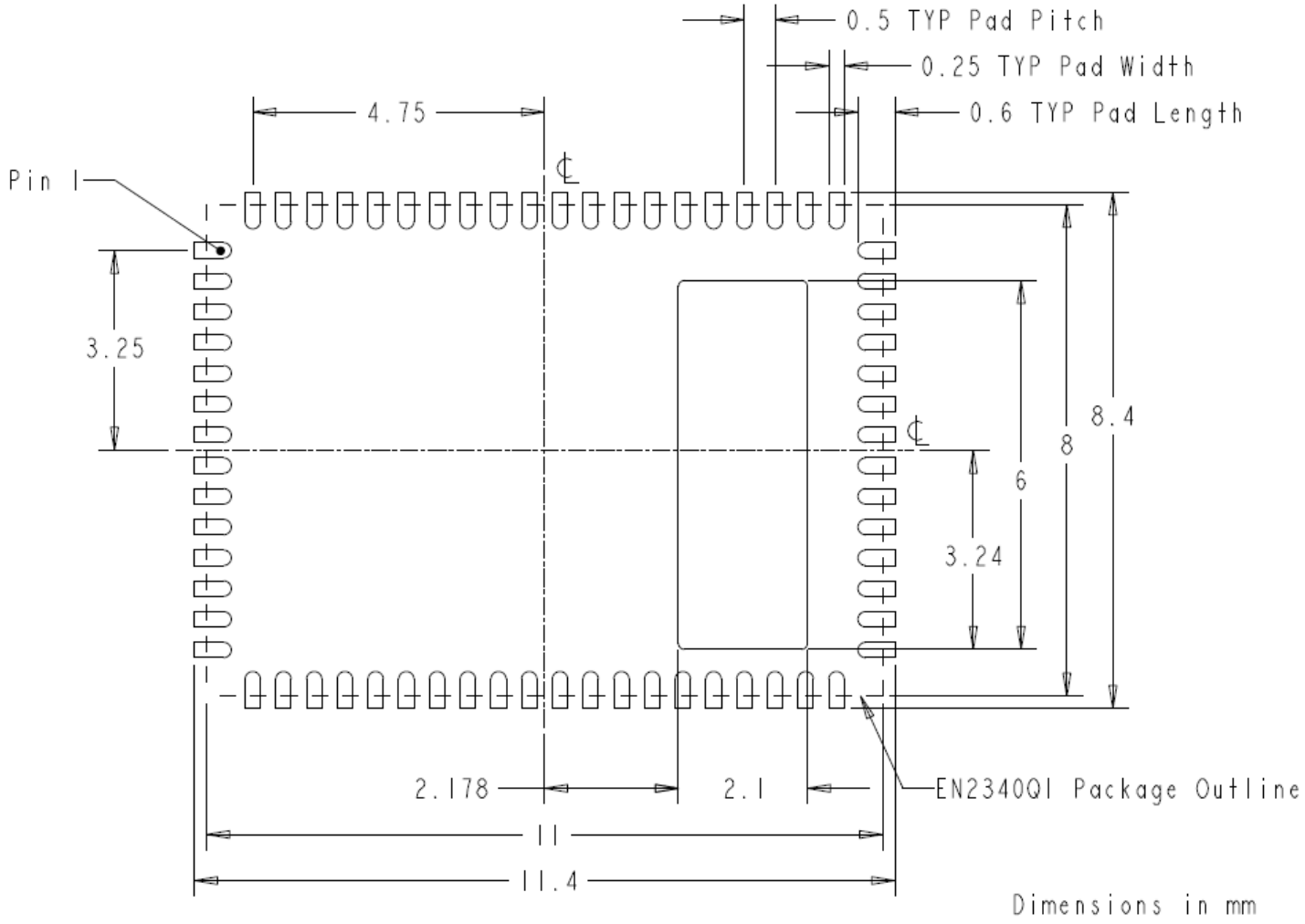


Figure 11: EN2340QI PCB Footprint (Top View)

Package and Mechanical

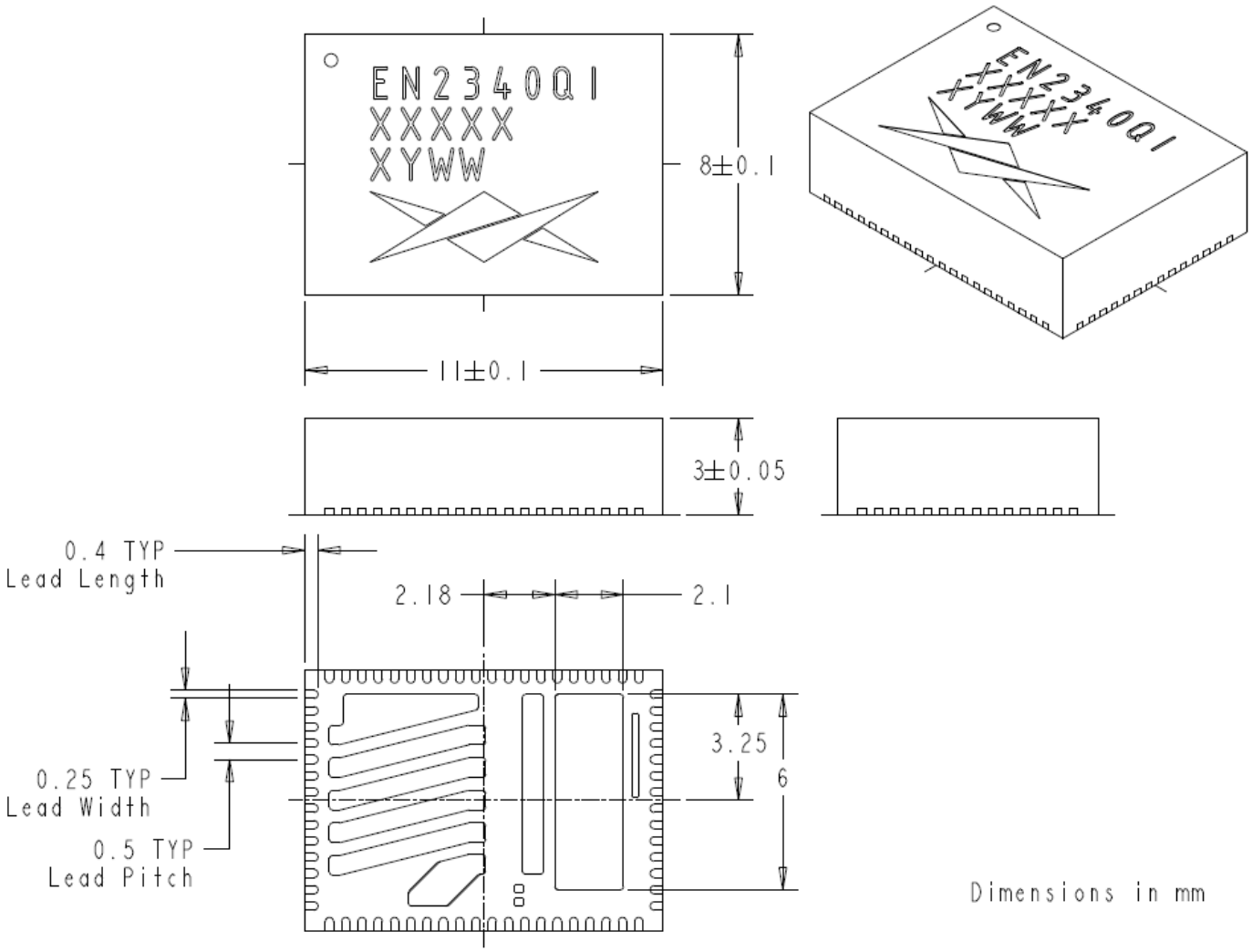


Figure 12: EN2340QI Package Dimensions (Bottom View)

Packing and Marking Information: http://www.enpirion.com/resource-center-packing-and-marking-information.htm

Contact Information

Enpirion, Inc.
Perryville III Corporate Park
53 Frontage Road - Suite 210
Hampton, NJ 08827 USA
Phone: 1.908.894.6000
Fax: 1.908.894.6090