A New Direction in Mixed-Signal

CLC1002

Ultra-Low Noise Amplifier

General Description

The CLC1002 is a high-performance, voltage feedback amplifier with ultra-low input voltage noise, 0.6nV/√Hz. The CLC1002 provides 965MHz gain bandwidth product and 170V/µs slew rate making it well suited for high-speed data acquisition systems requiring high levels of sensitivity and signal integrity. This high-performance amplifier also offers low input offset voltage.

The CLC1002 is designed to operate from 4V to 12V supplies. It consumes only 13mA of supply current per channel and offers a power saving disable pin that disables the amplifier and decreases the supply current to below 225µA. The CLC1002 amplifier operates over the extended temperature range of -40°C to +125°C.

If larger bandwidth or slew rate is required, a higher minimum stable gain version is available, the CLC1001 offers a minimum stable gain of 10 with 2.1GHz GBWP and 410V/µs slew rate.

FEATURES

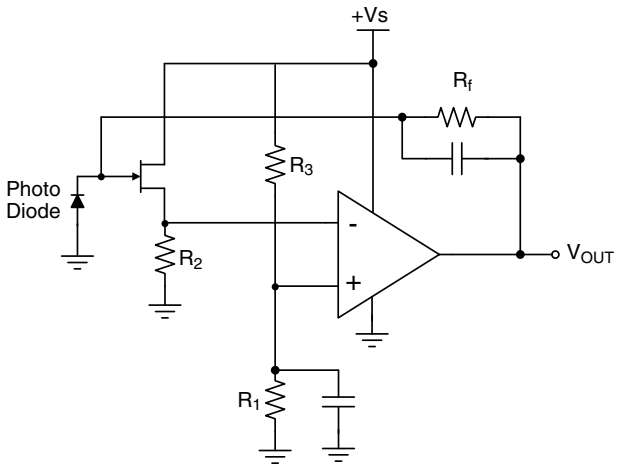
- 0.6nV/√Hz input voltage noise
- 1mV maximum input offset voltage
- 965MHz gain bandwidth product
- Minimum stable gain of 5
- 170V/µs slew rate
- 130mA output current
- -40°C to +125°C operating temperature range
- Fully specified at 5 and ±5V supplies
- CLC1002: ROHS compliant TSOT-6, SOIC-8 package options

APPLICATIONS

- Transimpedance amplifiers
- Pre-amplifier
- Low noise signal processing
- Medical instrumentation
- Probe equipment
- Test equipment
- Ultrasound channel amplifier

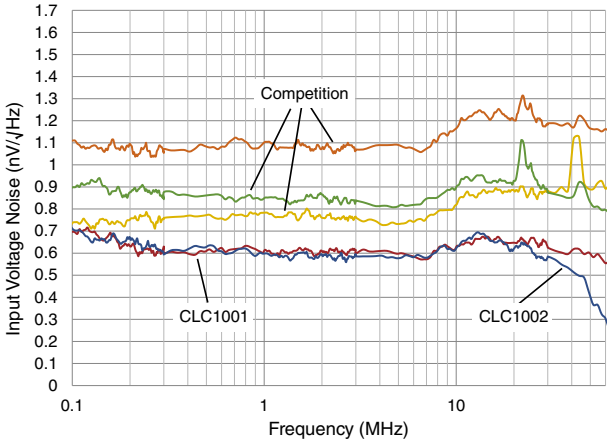
Ordering Information - back page

Typical Application



Single Supply Photodiode Amplifier

Input Voltage Noise vs Competition



Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

V_S ..... 0V to +14V

V_{IN} ..... $-V_S$ - 0.5V to $+V_S$ +0.5V

Operating Conditions

Supply Voltage Range ..... 4V to 12V

Operating Temperature Range .....-40°C to 125°C

Junction Temperature .....150°C

Storage Temperature Range.....-65°C to 150°C

Lead Temperature (Soldering, 10s) .....260°C

Package Thermal Resistance

θ_{JA} (TSOT-6).....192°C/W

θ_{JA} (SOIC-8).....150°C/W

Package thermal resistance (θ_{JA}), JEDEC standard, multi-layer test boards, still air.

ESD Protection

CLC1002 (HBM) 2kV

ESD Rating for HBM (Human Body Model).

Electrical Characteristics at +5V

T_A = 25°C, V_S = +5V, R_f = 100Ω, R_L = 500Ω to V_S/2; G = 5; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GBWP	-3dB Gain Bandwidth Product	G = +21, V_{OUT} = 0.2V_{pp}		910		MHz
BW_{SS}	-3dB Bandwidth	G = +5, V_{OUT} = 0.2V_{pp}		265		MHz
$f_{0.1dBSS}$	0.1dB Gain Flatness Small Signal	G = +5, V_{OUT} = 0.2V_{pp}		37		MHz
BW_{LS}	Large Signal Bandwidth	G = +5, V_{OUT} = 2V_{pp}		54		MHz
$f_{0.1dBLS}$	0.1dB Gain Flatness Large Signal	G = +5, V_{OUT} = 2V_{pp}		29		MHz
Time Domain						
t_R, t_F	Rise and Fall Time	V_{OUT} = 1V step; (10% to 90%)		4,2		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		12		ns
OS	Overshoot	V_{OUT} = 1V step		3		%
SR	Slew Rate	4V step		160		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	10MHz, V_{OUT} = 1V_{pp}		72		dBc
HD3	3rd Harmonic Distortion	10MHz, V_{OUT} = 1V_{pp}		74		dBc
THD	Total Harmonic Distortion	10MHz, V_{OUT} = 1V_{pp}		70		dB
e_n	Input Voltage Noise	>100kHz		0.6		nV/√Hz
i_n	Input Current Noise	>100kHz		4.2		pA/√Hz
DC Performance						
V_{IO}	Input Offset Voltage			0.1		mV
d_{VIO}	Average Drift			2.7		µV/°C
I_B	Input Bias Current			28		µA
dI_B	Average Drift			46		nA/°C
I_{OS}	Input Offset Current			0.1		µA
PSRR	Power Supply Rejection Ratio	DC		83		dB
A_{OL}	Open Loop Gain	V_{OUT} = V_S / 2		80		dB
I_S	Supply Current	per channel		12.5		mA
Disable Characteristics						
t_{ON}	Turn On Time	1V step, 1% settling		80		ns
t_{OFF}	Turn Off Time			220		ns
OFF_{ISO}	Off Isolation	2V_{pp} , 5MHz		73		dB
$OFFC_{OUT}$	Off Output Capacitance			5.8		pF
V_{OFF}	Power Down Voltage	Disabled if $\overline{DIS}$ pin is grounded or pulled below V_{OFF}	Disabled if $\overline{DIS}$ < 1.5			V
V_{ON}	Enable Voltage	Enabled if $\overline{DIS}$ pin is floating or pulled above V_{ON}	Enabled if $\overline{DIS}$ > 3			V
I_{SD}	Disable Supply Current	No Load, DIS pin tied to ground		130		µA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		4.2		MΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common Mode Input Range			0.8 to 5.1		V
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = 1.5V to 4V		94		dB
Output Characteristics						
V_{OUT}	Output Swing	R_L = 500Ω		0.97 to 4		V
		R_L = 2kΩ		0.96 to 4.1		V
I_{OUT}	Output Current			±125		mA
I_{SC}	Short Circuit Current	V_{OUT} = V_S / 2		±150		mA

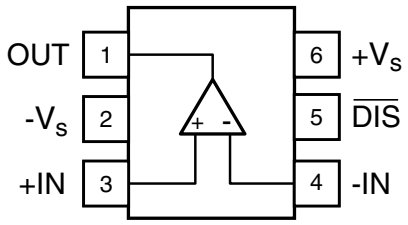
Electrical Characteristics at ±5V

T_A = 25°C, V_S = ±5V, R_f = 100Ω, R_L = 500Ω to GND; G = 5; unless otherwise noted.

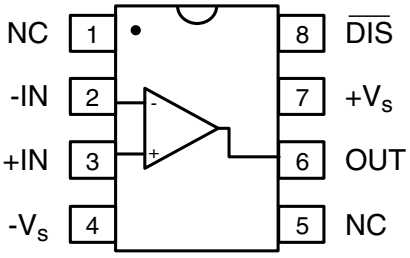
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GBWP	-3dB Gain Bandwidth Product	G = +21 V_{OUT} = 0.2V_{pp}		965		MHz
BW_{SS}	-3dB Bandwidth	G = +5, V_{OUT} = 0.2V_{pp}		290		MHz
$f_{0.1dBSS}$	0.1dB Gain Flatness Small Signal	G = +5, V_{OUT} = 0.2V_{pp}		45		MHz
BW_{LS}	Large Signal Bandwidth	G = +5, V_{OUT} = 2V_{pp}		61		MHz
$f_{0.1dBLS}$	0.1dB Gain Flatness Large Signal	G = +5, V_{OUT} = 2V_{pp}		32		MHz
Time Domain						
t_R, t_F	Rise and Fall Time	V_{OUT} = 1V step; (10% to 90%)		3.8		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		12		ns
OS	Overshoot	V_{OUT} = 1V step		2		%
SR	Slew Rate	4V step		170		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	10MHz, V_{OUT} = 2V_{pp}		75		dBc
HD3	3rd Harmonic Distortion	10MHz, V_{OUT} = 2V_{pp}		66		dBc
THD	Total Harmonic Distortion	10MHz, V_{OUT} = 2V_{pp}		65.5		dB
e_n	Input Voltage Noise	>100kHz		0.6		nV/√Hz
i_n	Input Current Noise	>100kHz		4.2		pA/√Hz
DC Performance						
V_{IO}	Input Offset Voltage		-1	0.5	1	mV
d_{VIO}	Average Drift			4.3		µV/°C
I_B	Input Bias Current		-60	30	60	µA
dI_B	Average Drift			44		nA/°C
I_{OS}	Input Offset Current			0.3	6	µA
PSRR	Power Supply Rejection Ratio	DC	78	83		dB
A_{OL}	Open Loop Gain	V_{OUT} = V_S / 2	70	83		dB
I_S	Supply Current	per channel		13	16	mA
Disable Characteristics						
t_{ON}	Turn On Time	1V step, 1% settling		115		ns
t_{OFF}	Turn Off Time			210		ns
OFF_{ISO}	Off Isolation	2V_{pp} , 5MHz		73		dB
$OFFC_{OUT}$	Off Output Capacitance			5.6		pF
V_{OFF}	Power Down Voltage	Disabled if $\overline{DIS}$ pin is grounded or pulled below V_{OFF}	Disabled if $\overline{DIS}$ < 1.3			V
V_{ON}	Enable Voltage	Enabled if $\overline{DIS}$ pin is floating or pulled above V_{ON}	Enabled if $\overline{DIS}$ > 3			V
I_{SD}	Disable Supply Current	No Load, DIS pin tied to ground		180	225	µA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		9.4		MΩ
C_{IN}	Input Capacitance			1.82		pF
CMIR	Common Mode Input Range			-4.3 to 5		V
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = -3.5V to 4V	75	90		dB
Output Characteristics						
V_{OUT}	Output Swing	R_L = 500Ω	-3.3	±4	3.6	V
		R_L = 2kΩ		±4		V
I_{OUT}	Output Current			±130		mA
I_{SC}	Short Circuit Current	V_{OUT} = V_S / 2		±165		mA

CLC1002 Pin Configurations

TSOT-6



SOIC-8



CLC1002 Pin Assignments

TSOT-6

Pin No.	Pin Name	Description
1	OUT	Output
2	$-V_S$	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	$\overline{DIS}$	Disable. Enabled if pin is left floating or pulled above V_{ON}, disabled if pin is grounded or pulled below V_{OFF}.
6	$+V_S$	Positive supply

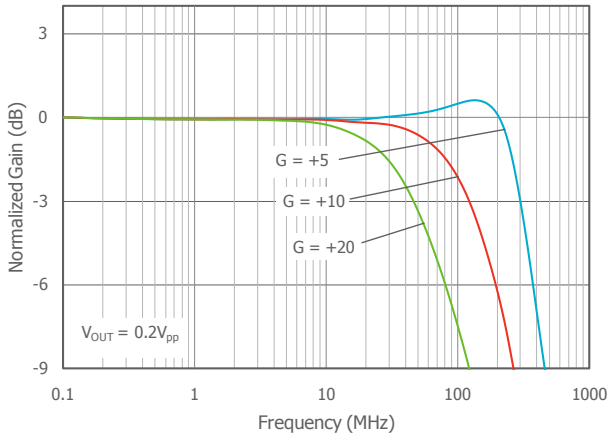
SOIC-8

Pin No.	Pin Name	Description
1	NC	No Connect
2	-IN	Negative input
3	+IN	Positive input
4	$-V_S$	Negative supply
5	NC	No Connect
6	OUT	Output
7	$+V_S$	Positive supply
8	$\overline{DIS}$	Disable. Enabled if pin is left floating or pulled above V_{ON}, disabled if pin is grounded or pulled below V_{OFF}.

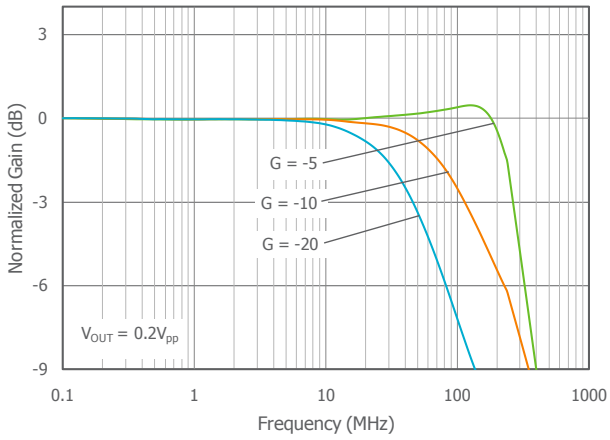
Typical Performance Characteristics

T_A = 25°C, V_S = ±5V, R_f = 100Ω, R_L = 500Ω, G = +5; unless otherwise noted.

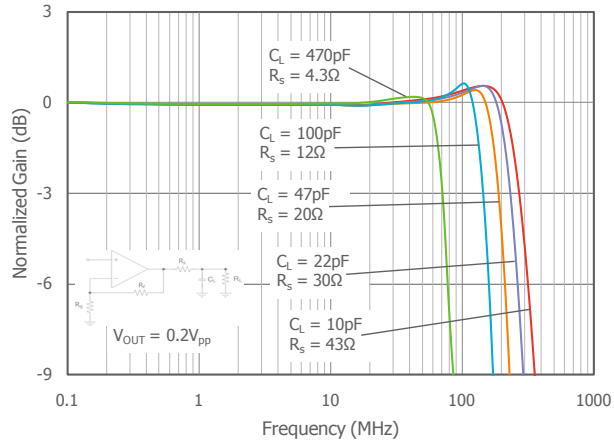
Non-Inverting Frequency Response



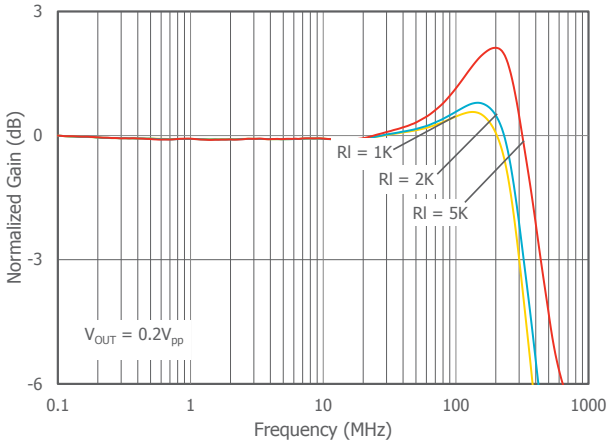
Inverting Frequency Response



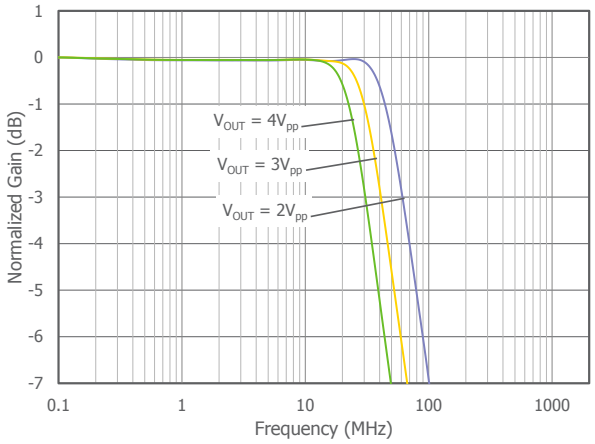
Frequency Response vs. C_L



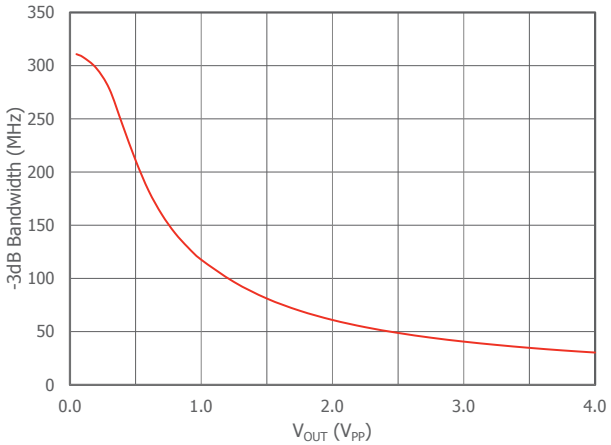
Frequency Response vs. R_L



Frequency Response vs. V_{OUT}



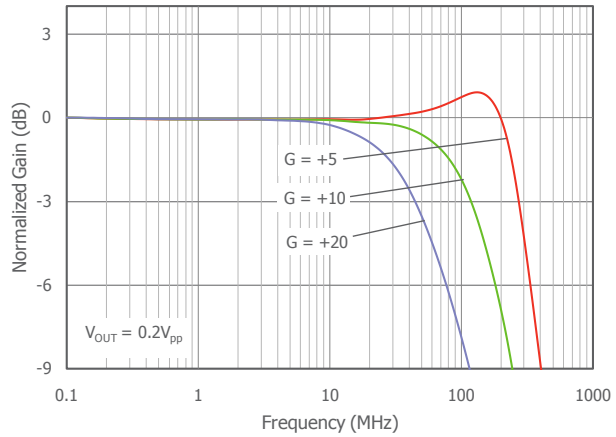
-3dB Bandwidth vs. Output Voltage



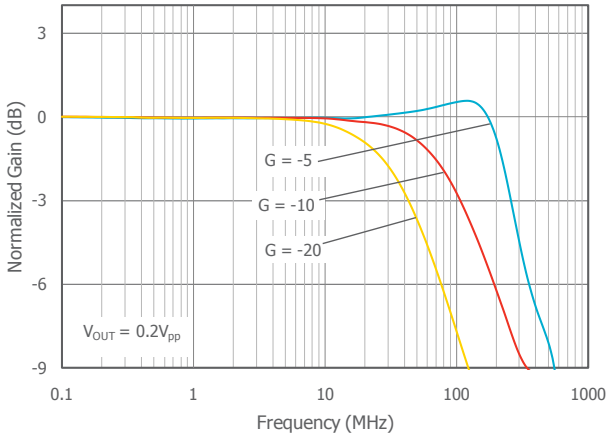
Typical Performance Characteristics

T_A = 25°C, V_S = ±5V, R_f = 100Ω, R_L = 500Ω, G = +5; unless otherwise noted.

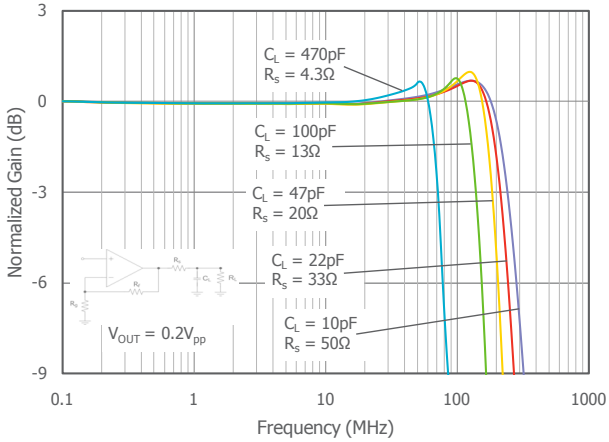
Non-Inverting Frequency Response at V_S = 5V



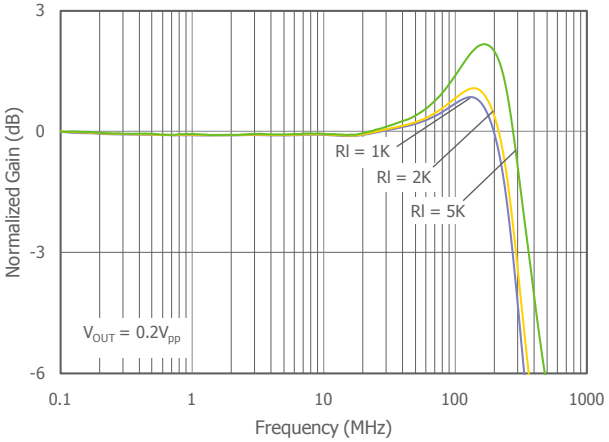
Inverting Frequency Response at V_S = 5V



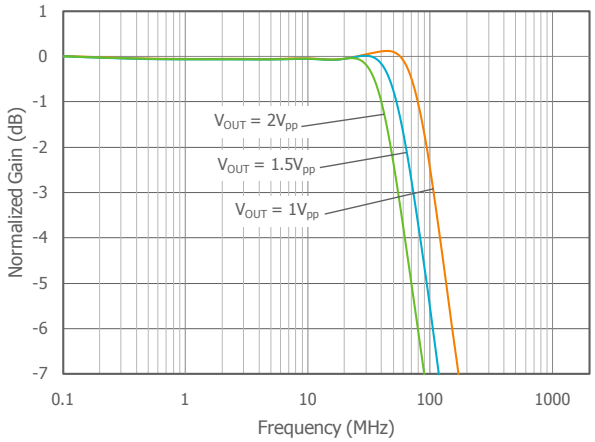
Frequency Response vs. C_L at V_S = 5V



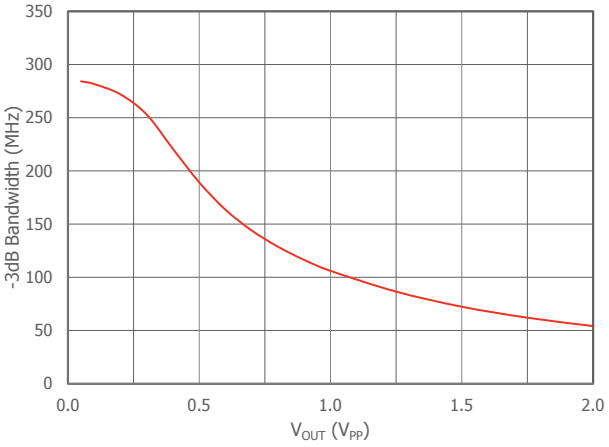
Frequency Response vs. R_L at V_S = 5V



Frequency Response vs. V_{OUT} at V_S = 5V



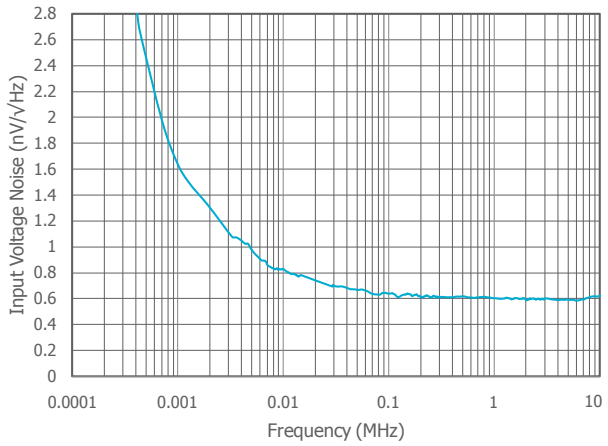
-3dB Bandwidth vs. Output Voltage at V_S = 5V



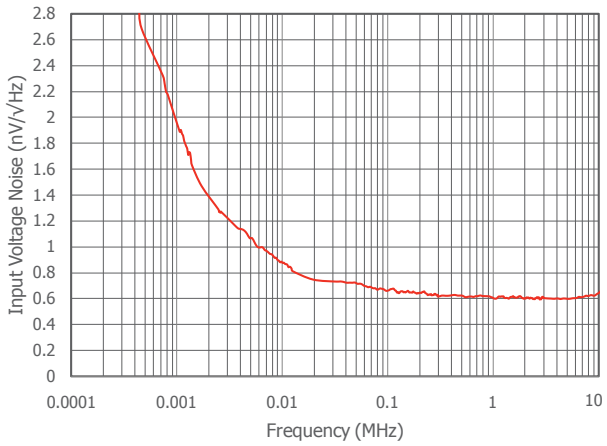
Typical Performance Characteristics

T_A = 25°C, V_S = ±5V, R_f = 100Ω, R_L = 500Ω, G = +5; unless otherwise noted.

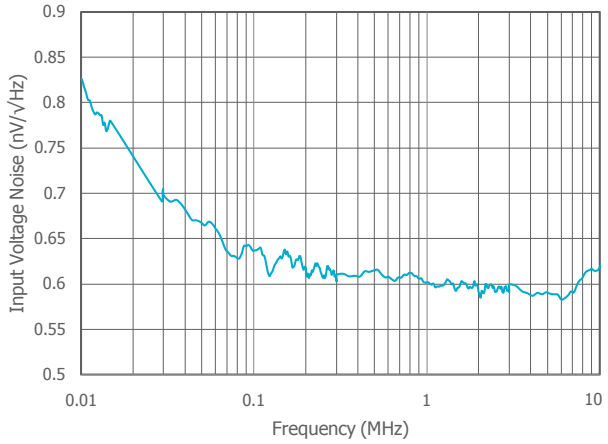
Input Voltage Noise



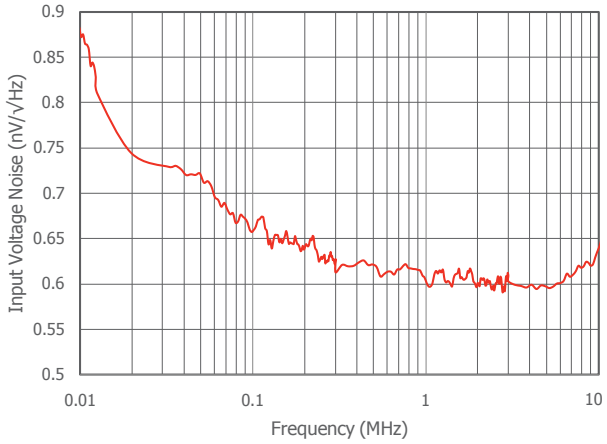
Input Voltage Noise at V_S = 5V



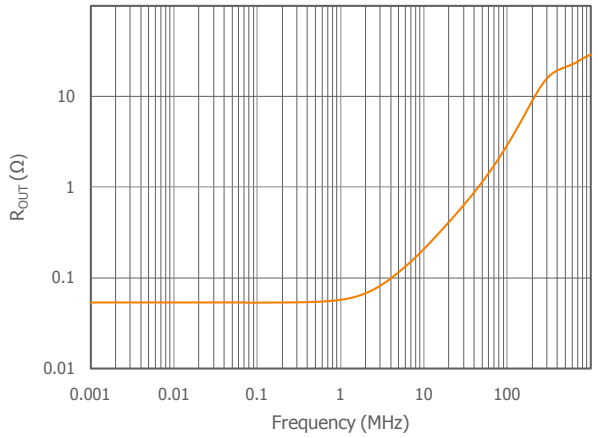
Input Voltage Noise (>10kHz)



Input Voltage Noise at V_S = 5V (>10kHz)



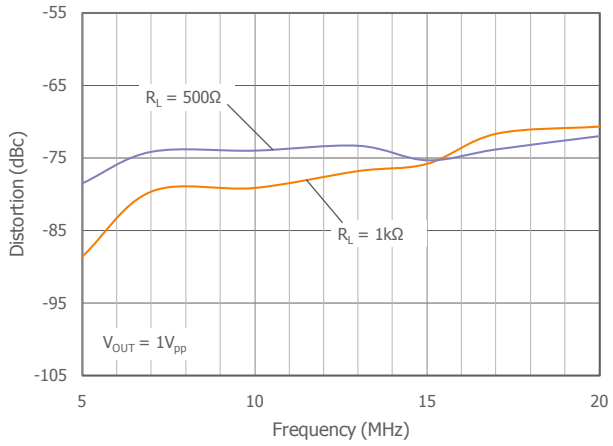
R_{OUT} vs. Frequency



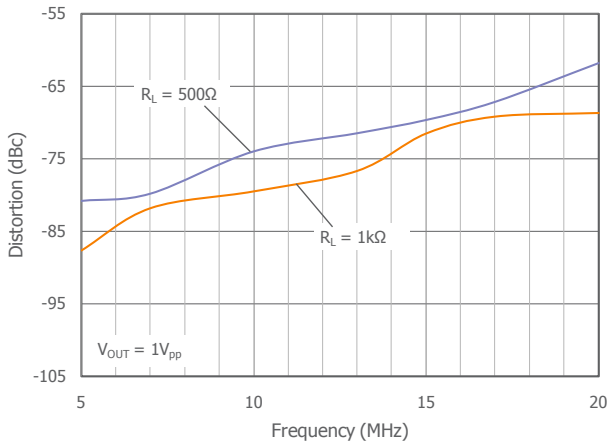
Typical Performance Characteristics

T_A = 25°C, V_S = ±5V, R_f = 100Ω, R_L = 500Ω, G = +5; unless otherwise noted.

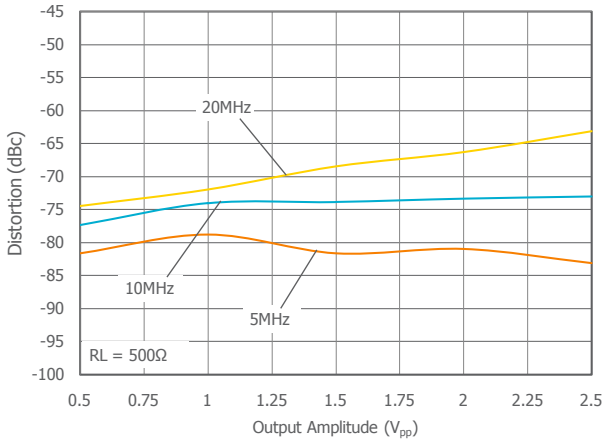
2nd Harmonic Distortion vs. R_L



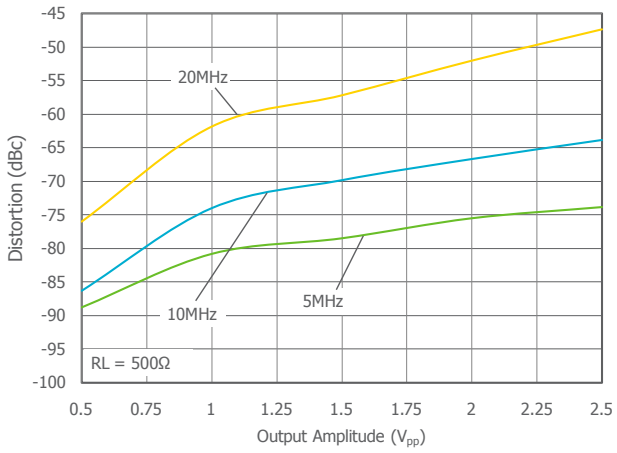
3rd Harmonic Distortion vs. R_L



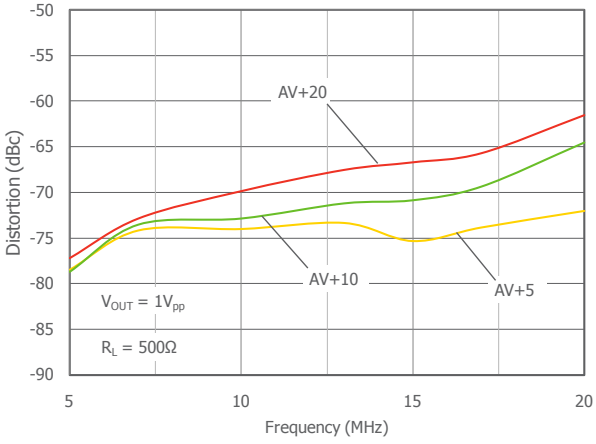
2nd Harmonic Distortion vs. V_{OUT}



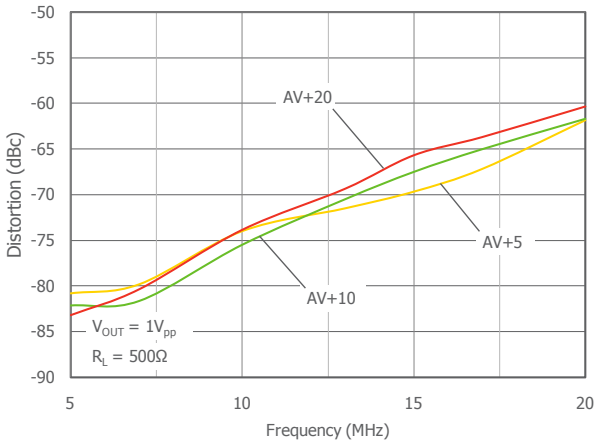
3rd Harmonic Distortion vs. V_{OUT}



2nd Harmonic Distortion vs. Gain



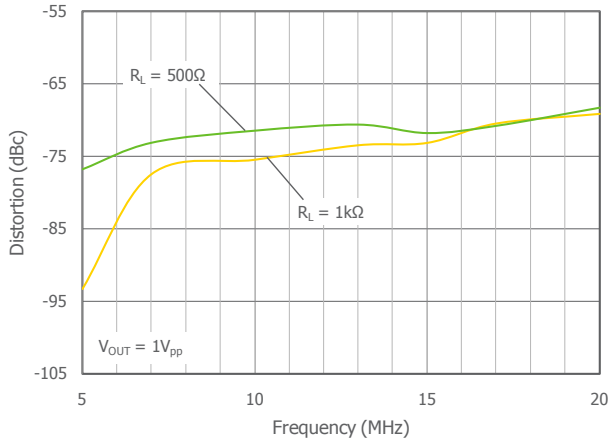
3rd Harmonic Distortion vs. Gain



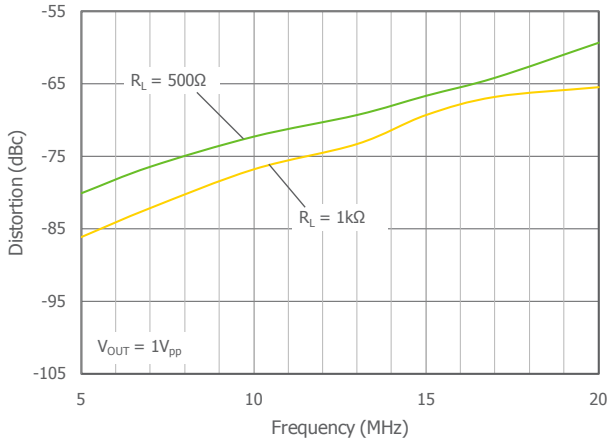
Typical Performance Characteristics

T_A = 25°C, V_S = ±5V, R_f = 100Ω, R_L = 500Ω, G = +5; unless otherwise noted.

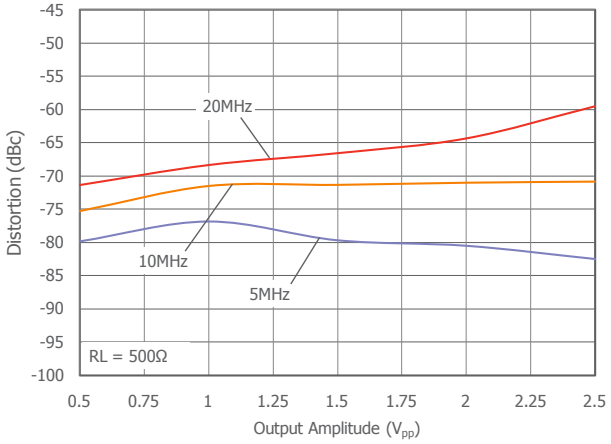
2nd Harmonic Distortion vs. R_L at V_S = 5V



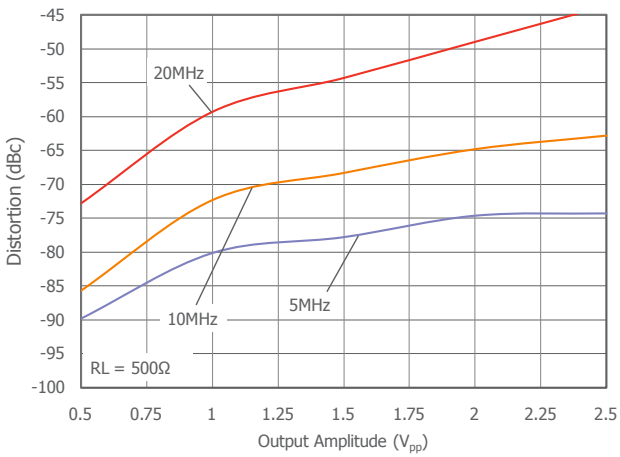
3rd Harmonic Distortion vs. R_L at V_S = 5V



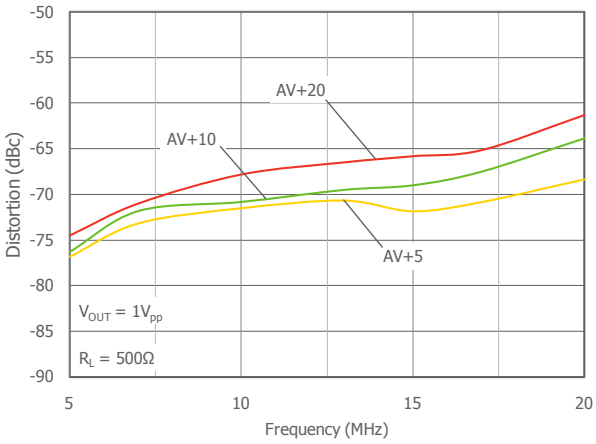
2nd Harmonic Distortion vs. V_{OUT} at V_S = 5V



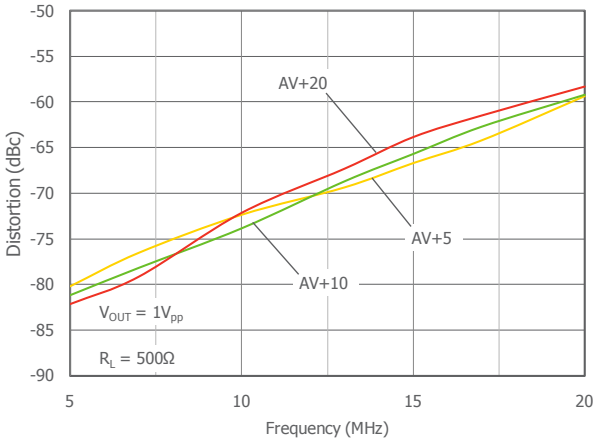
3rd Harmonic Distortion vs. V_{OUT} at V_S = 5V



2nd Harmonic Distortion vs. Gain at V_S = 5V



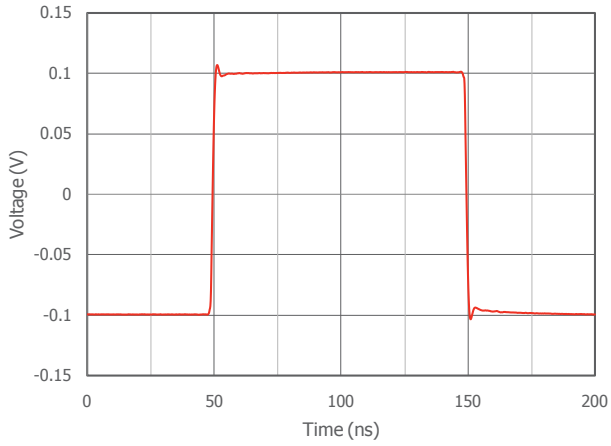
3rd Harmonic Distortion vs. Gain at V_S = 5V



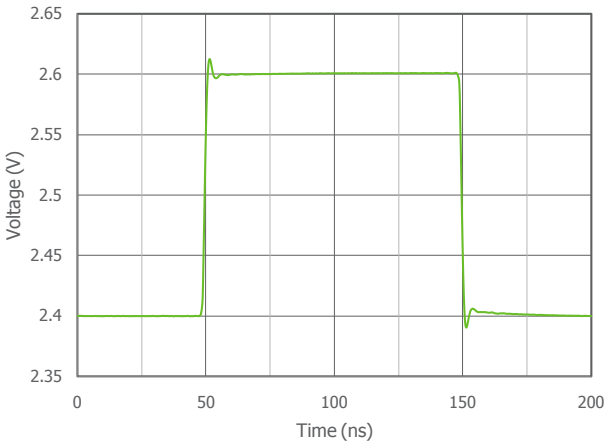
Typical Performance Characteristics

T_A = 25°C, V_S = ±5V, R_f = 100Ω, R_L = 500Ω, G = +5; unless otherwise noted.

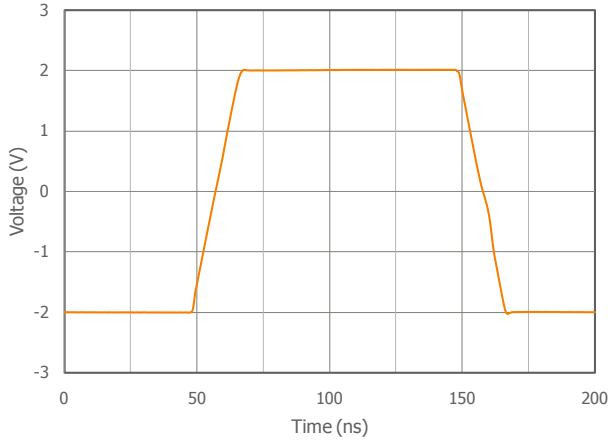
Small Signal Pulse Response



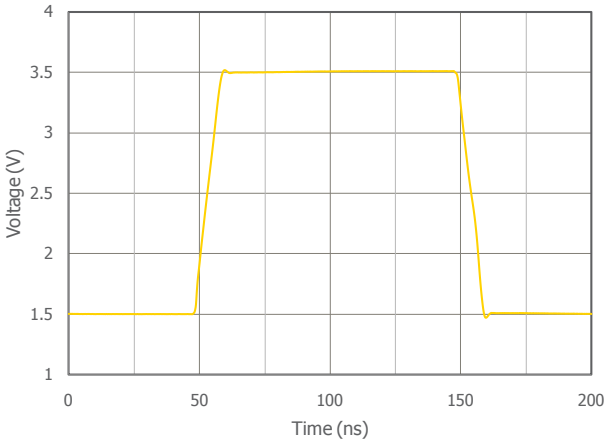
Small Signal Pulse Response at V_S = 5V



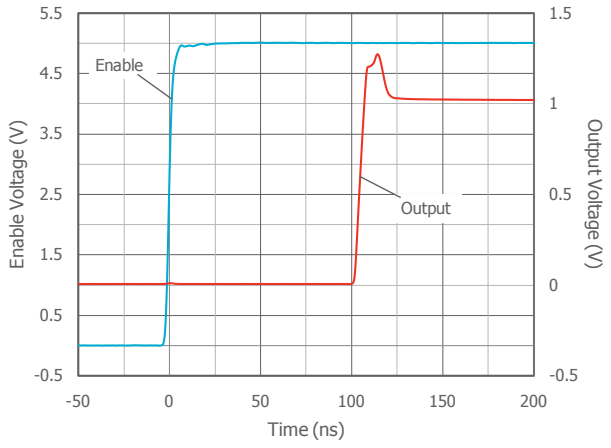
Large Signal Pulse Response



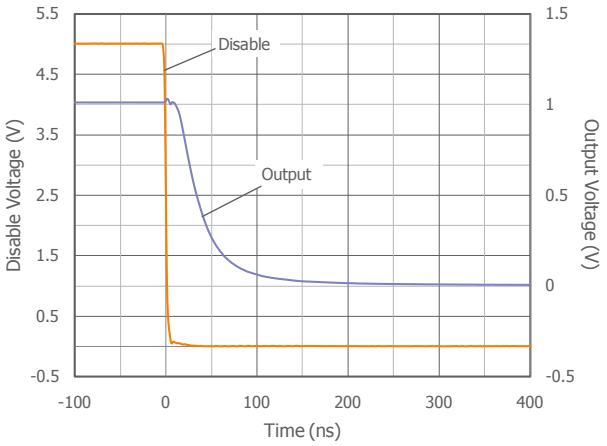
Large Signal Pulse Response at V_S = 5V



Enable Response



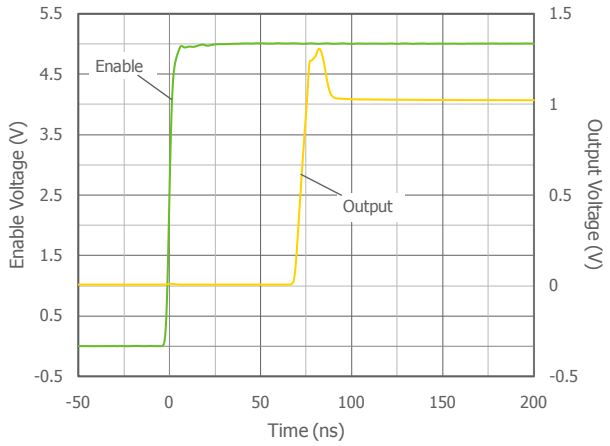
Disable Response



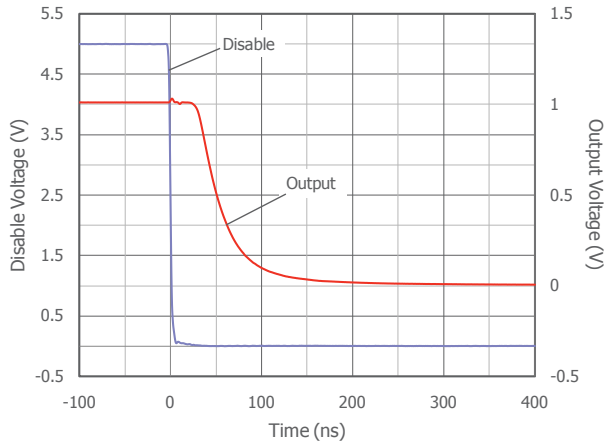
Typical Performance Characteristics

T_A = 25°C, V_S = ±5V, R_f = 100Ω, R_L = 500Ω, G = +5; unless otherwise noted.

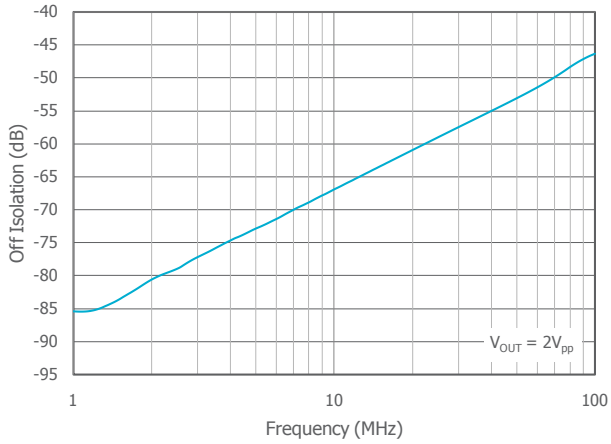
Enable Response at V_S = 5V



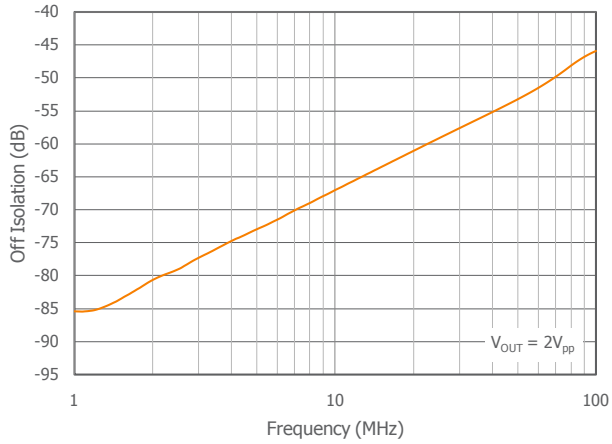
Disable Response at V_S = 5V



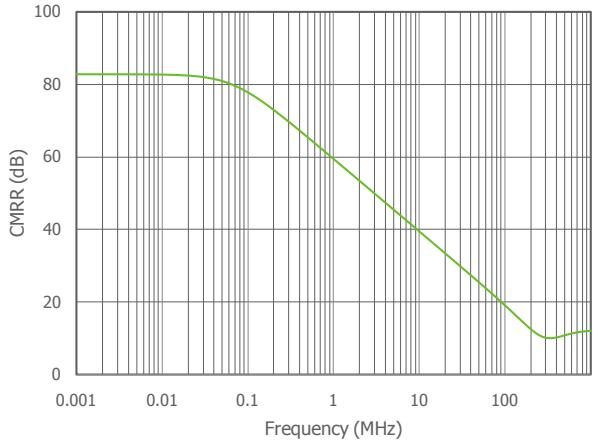
Off Isolation



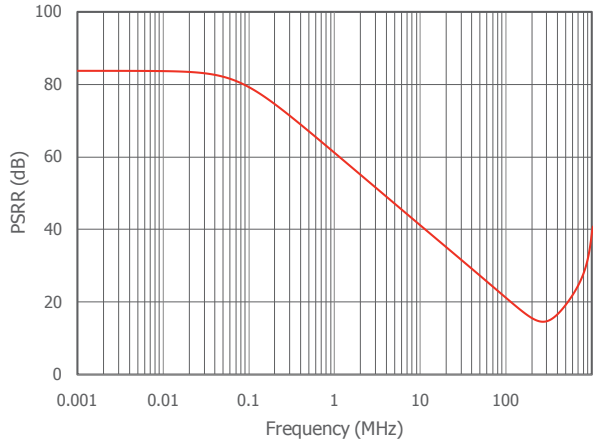
Off Isolation at V_S = 5V



CMRR vs. Frequency



PSRR vs. Frequency



Application Information

Basic Information

Figures 1 and 2 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations.

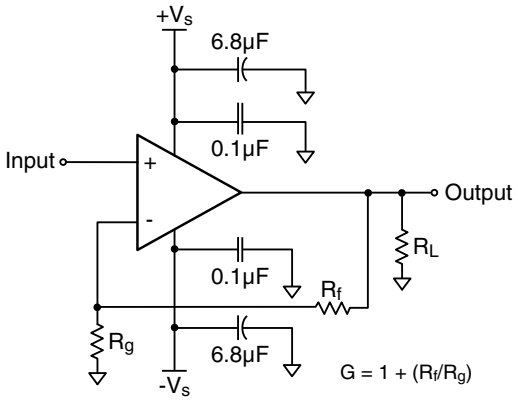


Figure 1: Typical Non-Inverting Gain Circuit

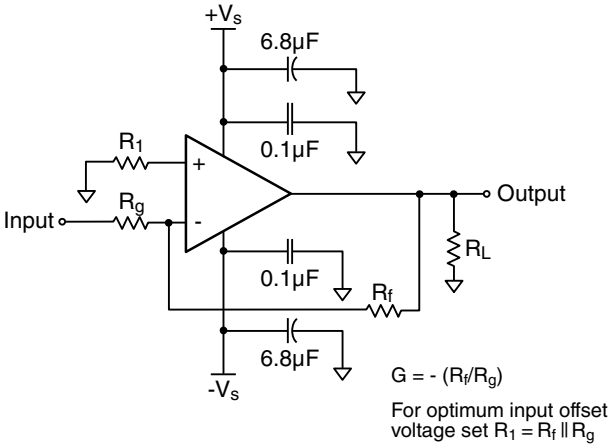


Figure 2: Typical Inverting Gain Circuit

Achieving Low Noise in an Application

Making full use of the low noise of the CLC1002 requires careful consideration of resistor values. The feedback and gain set resistors (R_f and R_g) and the non-inverting source impedance (R_{source}) all contribute noise to the circuit and can easily dominate the overall noise if their values are too high. The datasheet is specified with an R_g of 25Ω, at which point the noise from R_f and R_g is about equal to the noise from the CLC1002. Lower value resistors could be used at the expense of more distortion.

Figure 3 shows total input voltage noise (amp+resistors) versus R_f and R_g. As the value of R_f increases, the total input referred noise also increases.

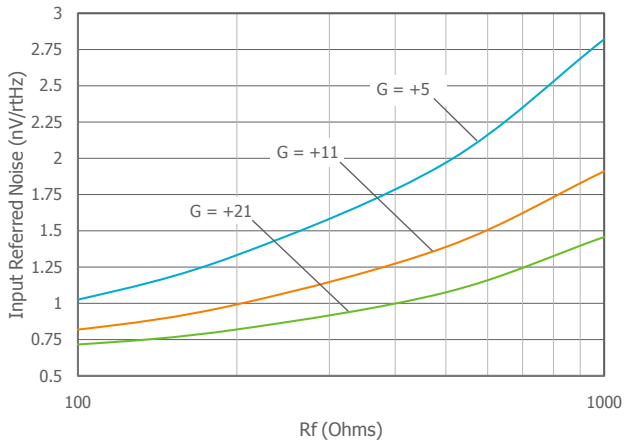


Figure 3: Input Referred Voltage Noise vs. R_f and R_g

The noise caused by a resistor is modeled with either a voltage source in series with the resistance:

$$\sqrt{4kTR}$$

Or a current source in parallel with it:

$$i_R = \sqrt{\frac{4kT}{R}}$$

Op amp noise is modeled with three noise sources, e_n, i_n, i_n and i_i. These three sources are analogous to the DC input voltage and current errors V_{os}, I_{bn} and I_{bi}.

The noise models must be analyzed in-circuit to determine the effect on the op amp output noise.

Since noise is statistical in nature rather than a continuous signal, the set of noise sources in circuit add in an RMS (root mean square) fashion rather than in a linear fashion. For uncorrelated noise sources, this means you add the squares of the noise voltages. A typical non-inverting application (see figure 1) results in the following noise at the output of the op amp:

$$e_o^2 = e_n^2\left(1+\frac{R_f}{R_g}\right)^2 + in^2R_s^2\left(1+\frac{R_f}{R_g}\right)^2 + i_i^2R_f^2$$

op amp noise terms e_n, i_n and i_i

$$+ e_{Rs}^2\left(1+\frac{R_f}{R_g}\right)^2 + e_{Rg}^2\left(\frac{R_f}{R_g}\right)^2 + e_{Rf}^2$$

external resistor noise terms for R_S, R_g and R_f

High source impedances are sometimes unavoidable, but they increase noise from the source impedance and also make the circuit more sensitive to the op amp current noise. Analyze all noise sources in the circuit, not just the op amp itself, to achieve low noise in your application.

Power Dissipation

Power dissipation should not be a factor when operating under the stated 500Ω load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value $Theta_{JA}$ (θ_{JA}) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{supply} - P_{load}$$

Supply power is calculated by the standard power equation.

$$P_{supply} = V_{supply} \times I_{RMSsupply}$$

$$V_{supply} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{load} = ((V_{load})_{RMS}^2)/Rload_{eff}$$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in Figure 3 would be calculated as:

$$R_L \parallel (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$$P_D = P_{Quiescent} + P_{Dynamic} - P_{load}$$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{supply}. Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{load})_{RMS} = V_{peak} / \sqrt{2}$$

$$(I_{load})_{RMS} = (V_{load})_{RMS} / Rload_{eff}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{Dynamic} = (V_{S+} - V_{load})_{RMS} \times (I_{load})_{RMS}$$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

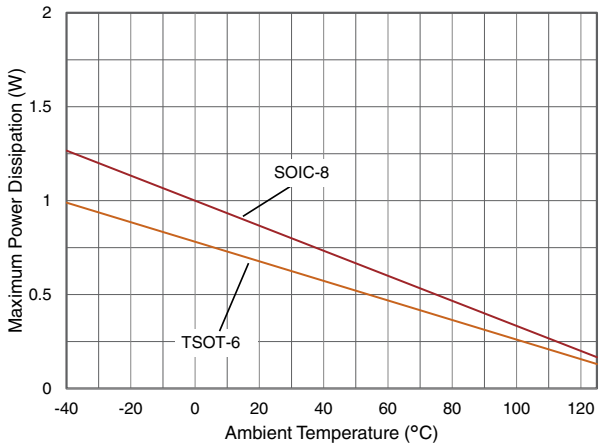


Figure 4. Maximum Power Derating

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 5.

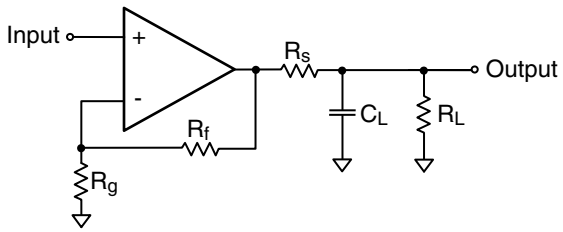


Figure 5. Addition of R_S for Driving Capacitive Loads

Table 1 provides the recommended R_S for various capacitive loads. The recommended R_S values result in approximately <1dB peaking in the frequency response. The Frequency Response vs. C_L plots, on page 6 and 7, illustrate the response of the CLC1002.

C_L (pF)	R_S (Ω)	-3dB BW (MHz)
10	43	275
22	30	235
47	20	190
100	12	146
470	4.3	72

Table 1: Recommended R_S vs. C_L

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Overdrive Recovery

For an amplifier, an overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The CLC1002 will typically recover in less than 25ns from an overdrive condition. Figure 6 shows the CLC1002 in an overdriven condition.

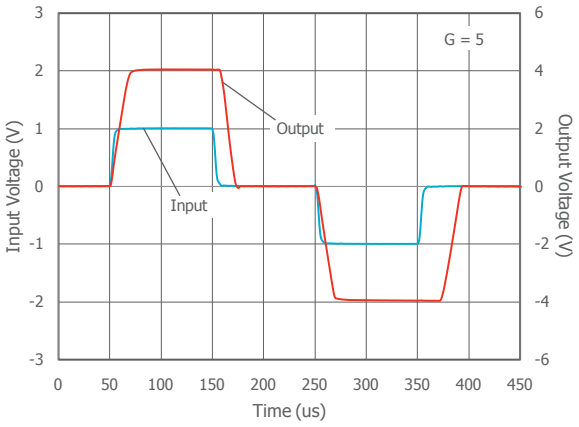


Figure 6: Overdrive Recovery

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Exar has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.1µF ceramic capacitors for power supply decoupling
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board #	Products
CEB002	CLC1002 in TSOT
CEB003	CLC1002 in SOIC

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 7-11 These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short $-V_S$ to ground.
2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

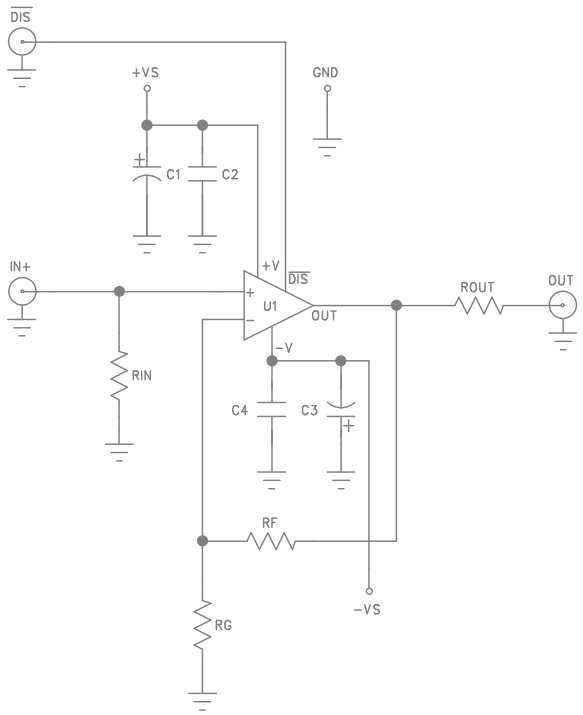


Figure 7. CEB002 & CEB003 Schematic

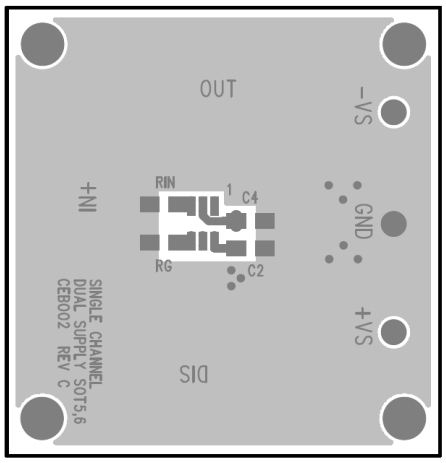


Figure 8. CEB002 Top View

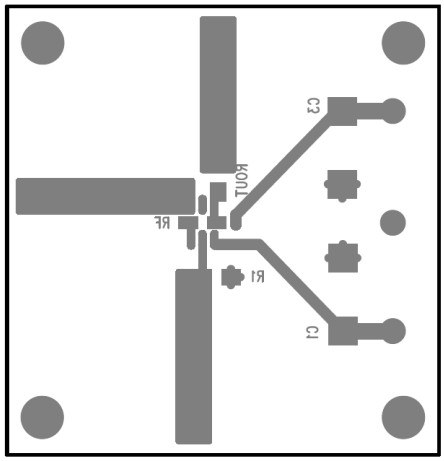


Figure 9. CEB002 Bottom View

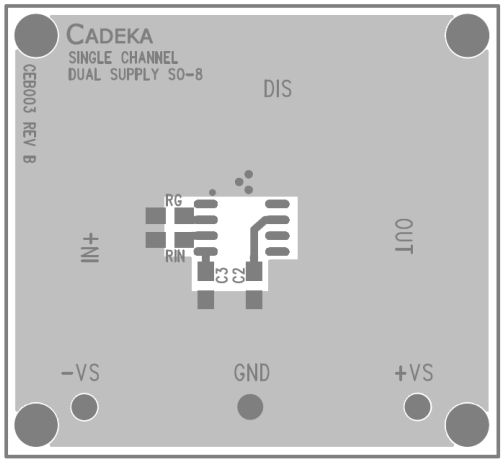


Figure 10. CEB003 Top View

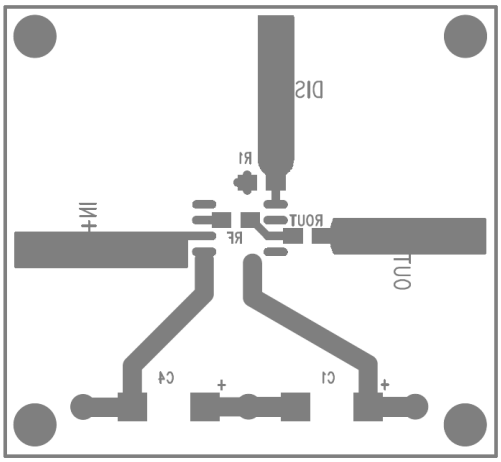
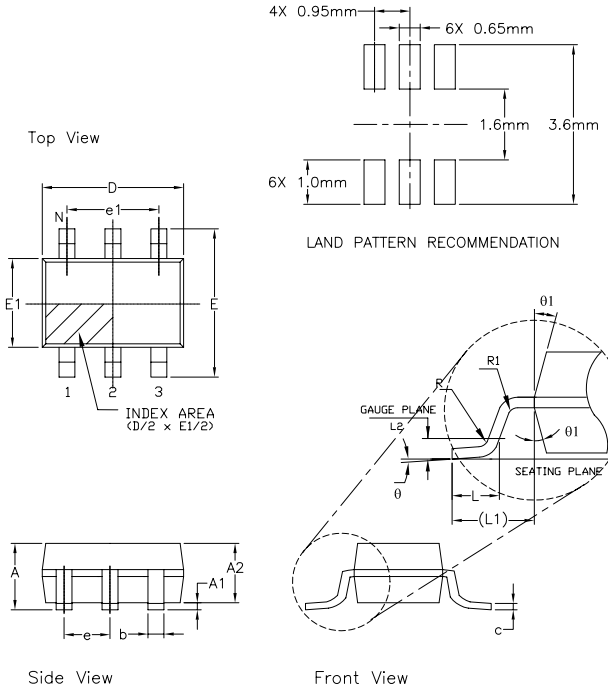


Figure 11. CEB003 Bottom View

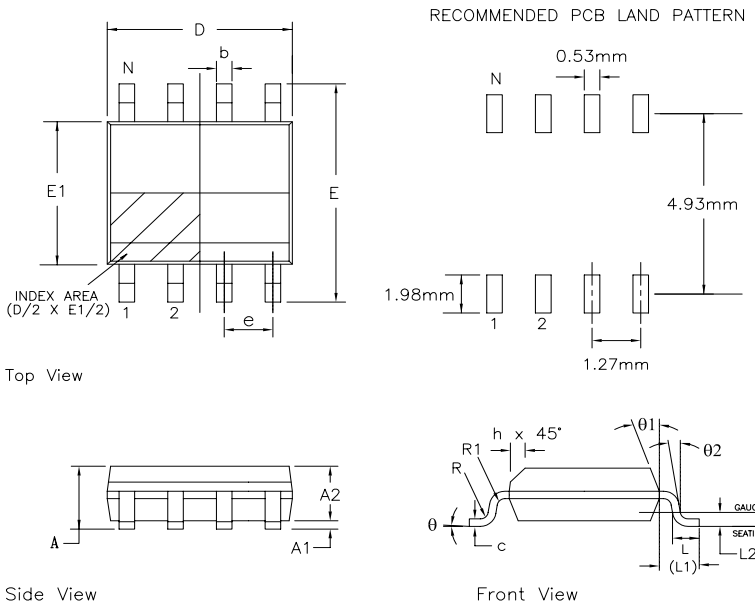
Mechanical Dimensions

TSOT-6 Package



6 PIN TSOT (OPTION 2)						
SYMBOLS	DIMENSION IN MM (Control Unit)			DIMENSION IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	0.80	0.030	—	0.031
A1	0.00	—	0.05	0.000	—	0.002
A2	0.70	0.75	0.78	0.028	0.036	0.031
b	0.35	—	0.50	0.012	—	0.020
c	0.10	—	0.20	0.003	—	0.008
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
e	0.95 BSC			0.038 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.37	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
θ	0°	4°	8°	0°	4°	8°
θ1	4°	10°	12°	4°	10°	12°
N	6			6		

SOIC-8 Package



8 Pin SOICN JEDEC MS-012 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	4.90 BSC			0.193 BSC		
N	8			8		

Ordering Information

Part Number	Package	Green	Operating Temperature Range	Packaging Quantity
CLC1002 Ordering Information				
CLC1002IST6X	TSOT-6	Yes	-40°C to +125°C	2.5k Tape & Reel
CLC1002IST6MTR	TSOT-6	Yes	-40°C to +125°C	250 Tape & Reel
CLC1002IST6EVB	Evaluation Board	N/A	N/A	N/A
CLC1002ISO8X	SOIC-8	Yes	-40°C to +125°C	2.5k Tape & Reel
CLC1002ISO8MTR	SOIC-8	Yes	-40°C to +125°C	250 Tape & Reel
CLC1002ISO8EVB	Evaluation Board	N/A	N/A	N/A

Moisture sensitivity level for all parts is MSL-1.

Revision History

Revision	Date	Description
1H (ECN 1442-01)	October 2014	Reformat into Exar data sheet template. Updated ordering information table to include MTR and EVB part numbers. Increased "I" temperature range from +85 to +125°C. Removed "A" temp grade parts, since "I" is now equivalent. Updated thermal resistance numbers and package outline drawings.

For Further Assistance:

Email: CustomerSupport@exar.com or HPATechSupport@exar.com

Exar Technical Documentation: http://www.exar.com/techdoc/

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A New Direction in Mixed-Signal