XRP6142

Synchronous Step-Down Controller with DDR Memory Termination

March 2010 Rev. 1.0.0

GENERAL DESCRIPTION

The XRP6142 is a synchronous step down switching controller for over 15 Amps point-of-loads converters and optimized to generate and support DDR I, II and III memory voltages requirements.

Optimized to operate from standard 3.3V and 5V rails, the XRP6142 supports conversions down to 0.5V from an input voltage as low as 1V and can reach efficiencies of up to 96%. Based on a constant on-time control scheme and operating at a constant switching frequency over the whole input voltage range, it provides excellent load transient response while requiring no external compensation components. Three selectable on-time options allow for further switching frequency, solution footprint and efficiency optimization.

Dedicated support for DDR I, II and II memories is also provided. The XRP6142 easily generates V_{DDQ} (V_{DD}) or V_{TT} voltages while an on board buffer provides the buffered V_{TT} reference voltage.

Under-voltage Lock out, short-circuit and over-current and over-temperature protection insure safe operations under abnormal operating conditions.

The XRP6142 is available in a compact RoHS compliant "green"/halogen free 16-pin QFN package.

APPLICATIONS

- **High-Power Point-of-Loads Converters**
- **Audio-Video Equipments**
- **FPGA and DSP Power Supplies**
- **DDR Memory Based Embedded Systems**

FEATURES

- **Over 15A Point-of-Load Capable**
  - Down to 0.5V Output Voltage Conversion
  - Up to 96% Efficiency
- **Wide 1.0V-5.5V Input Voltage Range Conversions**
  - Single Input 3.3V and 5V rails Operations
- **Constant On-Time Operations**
  - Constant Frequency Operations
  - No External Compensation
- **DDR I, II & III Termination Support**
  - V_{DDQ}/V_{DD} or V_{TT} Voltages Generation
  - Buffered V_{TT} Ref. Voltage Generation
- **Soft-Start and Enable Functions**
- **UVLO, Short Circuit and Over Current Protection**
- **RoHS Compliant "Green"/Halogen Free 3mm x 3mm 16-Pin QFN Package**

TYPICAL APPLICATION DIAGRAM

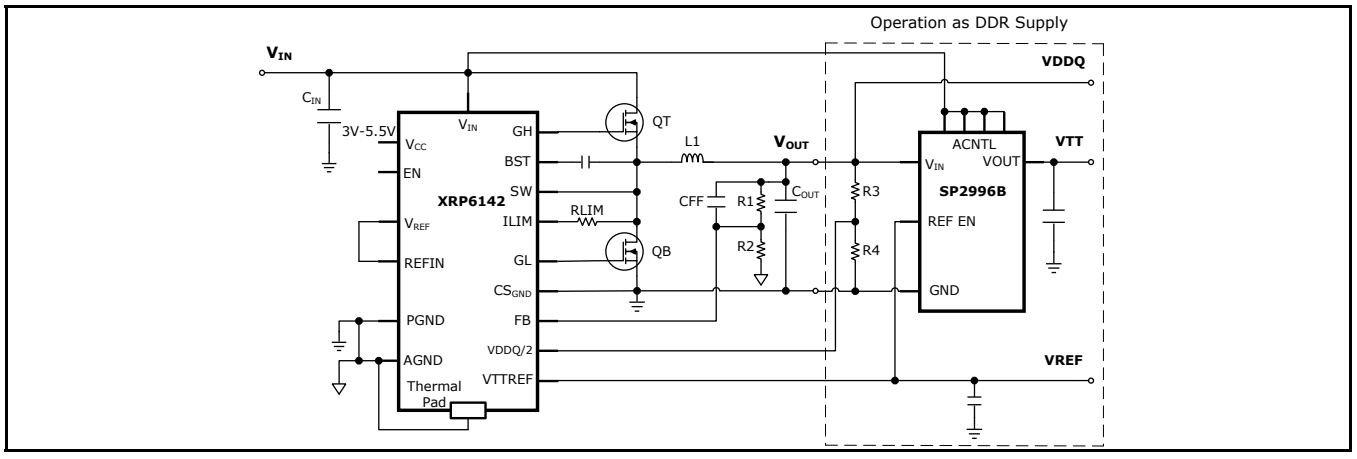


Figure. 1: XRP6142 as a Step-Down Converter or a DDR Supply

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only, and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} 7.0V
V_{IN} 7.0V
BST 13.5V
SW .....-1V to 7.0V
BST-SW .....-0.3V to 6V
All other pins ..... -0.3V to V_{CC}+0.3V
Storage Temperature ..... -65°C to 150°C
Power Dissipation ..... Internally Limited
Lead Temperature (Soldering, 10 sec) ..... 300°C
ESD Rating (HBM - Human Body Model) 2kV
ESD Rating (MM - Machine Model) 500V

OPERATING RATINGS

Input Voltage Range V_{CC} .....3.0V to 5.5V
Input Voltage Range V_{IN}.....1.0V to 5.5V
Junction Temperature Range .....-40°C to 125°C
Thermal Resistance θ_{JA} ..... 33.3°C/W

ELECTRICAL SPECIFICATIONS

Specifications are for an Operating Junction Temperature of T_J = 25°C; limits applying over the full Operating Junction Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{CC} = V_{IN} = 3.3V.

Parameter	Min.	Typ.	Max.	Units		Conditions
V_{REF}, Reference Voltage	0.495	0.5	0.505	V		
	0.492	0.5	0.508	V	•	
V_{FB} offset		7		mV		V_{REFIN} = V_{REF}
V_{REFIN}, Voltage Range	VREF		1.3	V		
$V_{DDQ/2}$, Input Impedance		60		MΩ		
V_{TTREF} , Output Error	-1.25		+1.25	%	•	$V_{DDQ/2}$ = 0.75V, I_{VTTR}=0mA
V_{TTREF} Current Limit	±20	±40	±65	mA	•	Sourcing: V_{TTREF}=0, $V_{DDQ/2}$=V_{REF} Sinking: V_{TTREF}=2V
I_Q, Operating Quiescent Current		400	600	µA		Not switching, V_{FB}=V_{REFIN}+0.1V
I_{OFF}, Shutdown current		0.1		µA		EN=0V
T_{ON}, Switch On-Time	0.4	0.5	0.6	µs	•	XR6142EL0-5-F (T_{ON}=500ns)
	0.8	1.0	1.2		•	XR6142EL1-0-F (T_{ON}=1000ns)
	1.6	2.0	2.4		•	XR6142EL2-0-F (T_{ON}=2000ns)
T_{OFF_MIN}, Minimum Off-Time		300	400	ns	•	All T_{ON} options
T_D, Gate Drive Dead-Time		50		ns		
V_{IH_EN}, EN Pin Rising Threshold	1.15	1.2	1.25	V	•	
V_{EN_HYS}, EN Pin Hysteresis		50	200	mV		
I_{FB}, Feedback Pin Bias Current		50		nA		V_{FB}=2.0V
V_{CCUVLO}, Under-Voltage Lockout		2.8	3.0	V	•	V_{CC} rising edge
V_{CCUVLO_HYS}, Under-Voltage Lock out Hysteresis		500		mV		
V_{SC_TH}, Feedback Pin Short Circuit Latch Threshold	55	65	75	%	•	% of VREFIN
ILIM Pin Source Current	42.5	50	57.5	µA		
ILIM Current Temperature Coefficient		0.3		%/C		
V_{ILIM} Current Limit Trip Level	-20	0	+20	mV	•	
Current Limit Blanking		130		ns		GL Rising > 1.0V

Parameter	Min.	Typ.	Max.	Units		Conditions
Hiccup Timeout		110		ms		0.5µs, 1µs and 2µs option, V_{OUT}=1V
Soft Start time	3	5	10	ms		
$R_{DS(ON)1}$, GH FET driver pull-up On resistance		2.5		Ω		I_{GH}=20 mA
$R_{DS(ON)2}$, GH FET driver pull-down On resistance		2		Ω		I_{GH}=20 mA
$R_{DS(ON)3}$, GL FET driver pull-up On resistance		2.5		Ω		I_{GL}=20 mA
$R_{DS(ON)4}$, GL FET driver pull-down On resistance		2		Ω		I_{GL}=20 mA

BLOCK DIAGRAM

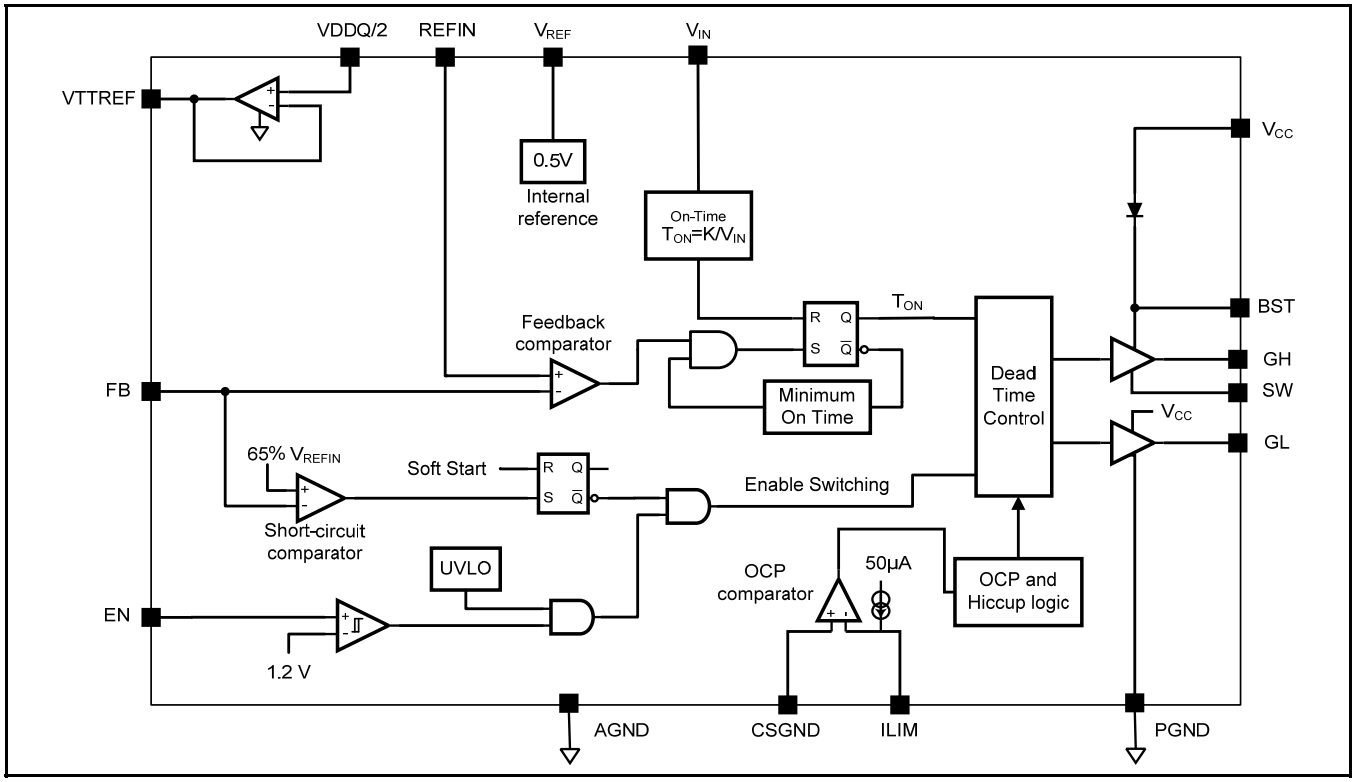


Figure. 2: XRP6142 Block Diagram

PIN ASSIGNMENT

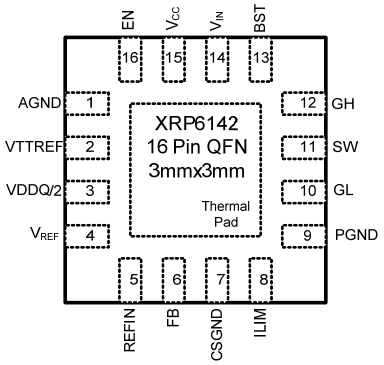


Figure. 3: XRP6142 Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
AGND	1	Analog Ground
VTTREF	2	Buffered output of VDDQ/2 V_{TT} reference voltage for DDR applications.
VDDQ/2	3	Buffer input voltage. Voltage used for the input to the V_{TTREF} buffer
V_{REF}	4	Precision reference output
REFIN	5	Reference input to the switching-regulator feedback comparator
FB	6	Feedback input to feedback comparator
CSGND	7	Current-sense ground
ILIM	8	Connect a resistor between this pin and the low-side current-sense element in order to set the current-limit-trip threshold. See applications section for instructions on how to set this resistor
PGND	9	Gate driver GND.
GL	10	Low-side N-channel MOSFET driver
SW	11	Switch node for floating-high-side gate drive
GH	12	High-side N-channel MOSFET driver
BST	13	Bootstrap capacitor to drive the high-side gate driver, GH
V_{IN}	14	Input voltage for the power train
Vcc	15	Input voltage for the XRP6142 internal circuitry and gate drives. V_{IN} and V_{CC} can be tied together when $V_{IN} \geq 3.0V$
EN	16	Precision enable pin. Pulling this pin above 1.2V will turn the part on
Thermal pad	-	Internally connected to AGND

ORDERING INFORMATION

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1	Note 2
XRP6142EL0-5-F	-40°C≤T_J≤+125°C	6142E YYWW05 X	16-pin QFN	Bulk	RoHS Compliant Halogen Free	0.5µs on time
XRP6142ELTR0-5-F	-40°C≤T_J≤+125°C	6142E YYWW05 X	16-pin QFN	3K/Tape & Reel	RoHS Compliant Halogen Free	0.5µs on time
XRP6142EL1-0-F	-40°C≤T_J≤+125°C	6142E YYWW10 X	16-pin QFN	Bulk	RoHS Compliant Halogen Free	1.0µs on time
XRP6142ELTR1-0-F	-40°C≤T_J≤+125°C	6142E YYWW10 X	16-pin QFN	3K/Tape & Reel	RoHS Compliant Halogen Free	1.0µs on time
XRP6142EL2-0-F	-40°C≤T_J≤+125°C	6142E YYWW20 X	16-pin QFN	Bulk	RoHS Compliant Halogen Free	2.0µs on time
XRP6142ELTR2-0-F	-40°C≤T_J≤+125°C	6142E YYWW20 X	16-pin QFN	3K/Tape & Reel	RoHS Compliant Halogen Free	2.0µs on time
XRP6142EVB	XRP6142 Evaluation Board – XRP6142EL2-0-F based					

"YY" = Year – "WW" = Work Week – "X" = Lot Number

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at V_{IN} = 3V to 5.5V, T_J = T_A = 25°C, unless otherwise specified - Schematic and BOM from Application Information section of this datasheet.

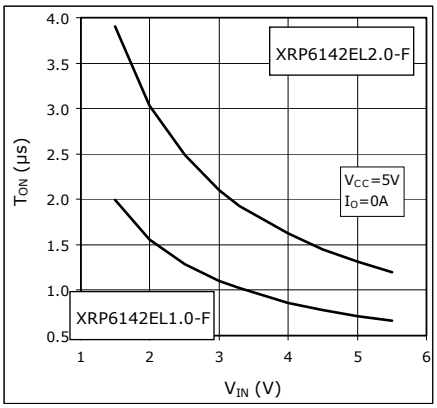


Fig. 4: T_{ON} versus V_{IN}

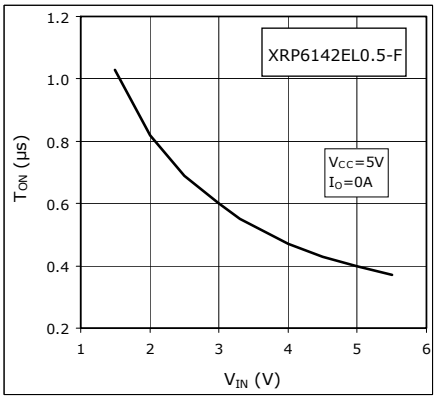


Fig. 5: T_{ON} versus V_{IN}

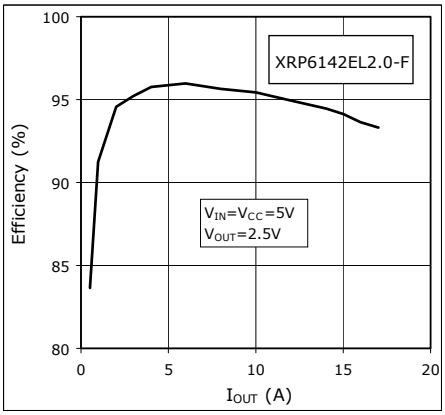


Fig. 6: Efficiency versus I_{OUT}

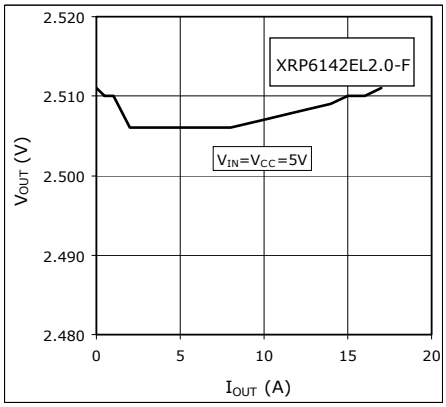


Fig. 7: Load regulation

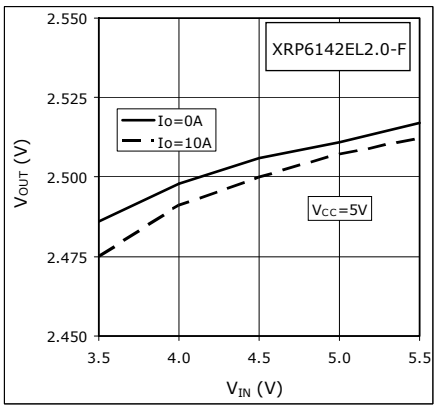


Fig. 8: Line regulation

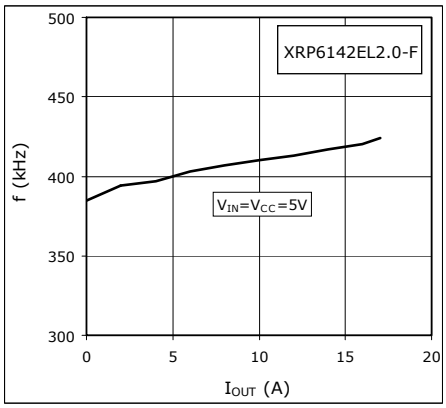


Fig. 9: Frequency versus I_{OUT}

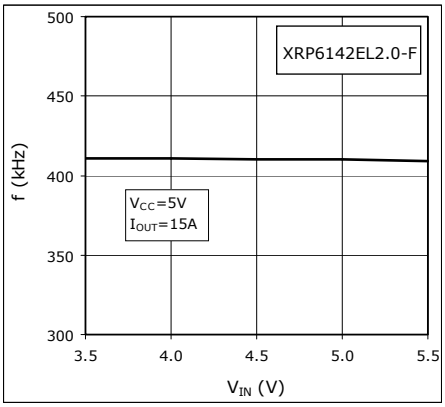


Fig. 10: Frequency versus V_{IN}

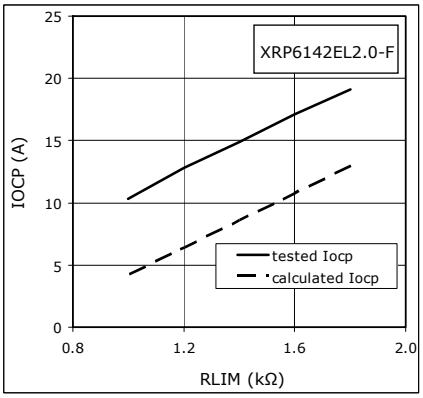


Fig. 11: IOCP versus RLIM

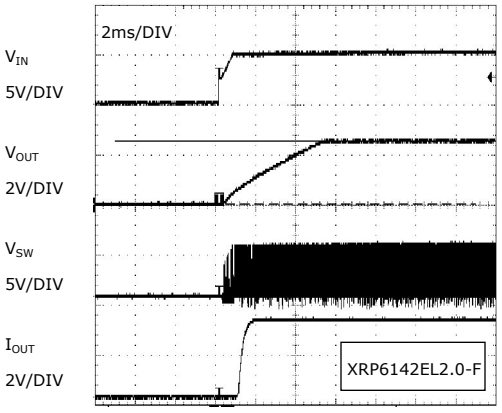


Fig. 12: Power-up into a 15A load, V_{IN}=5V, V_{OUT}=2.5V

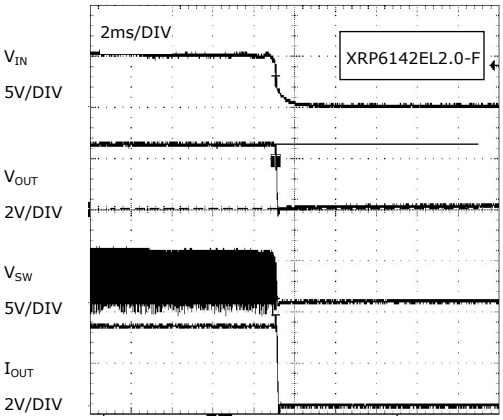


Fig. 13: Power-down from a 15A load, V_{IN}=5V, V_{OUT}=2.5V

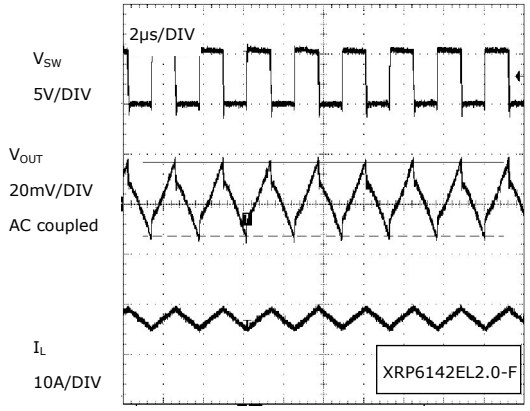


Fig. 14: Steady state, output ripple is 30mV p-p, V_{OUT}=2.5V

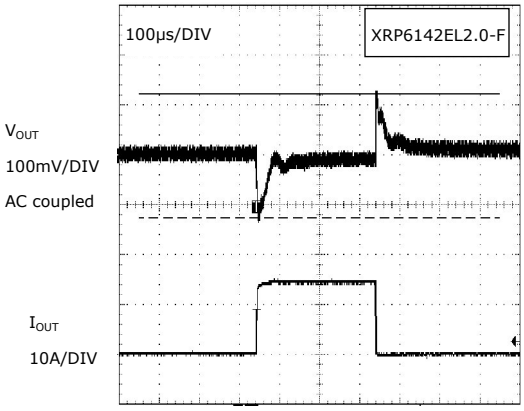


Fig. 15: Transient response, 250mV p-p, 15A load step

THEORY OF OPERATION

The XRP6142 synchronous buck controller utilizes the constant-on-time principle. The on-time is internally set and is available in three different set points to allow for different frequency options. The XRP6142 automatically adjusts the on-time during operation inversely with the input voltage V_{IN}, to maintain a constant frequency. Therefore, the switching frequency is independent of the inductor and capacitor size, unlike hysteretic controllers.

At the beginning of the cycle, the XRP6142 turns on the high-side FET for a fixed duration. The on time is internally set and adjusted by V_{IN}. At the end of the on time, the high-side FET is turned off, for a predetermined minimum off time (nominally 300ns). After $T_{OFF-MIN}$ has expired, the high-side FET will stay off until the feedback comparator trip point of 0.5V has been reached. Then the high-side FET turns on again and the cycle repeats. The operation of the low-side FET is complementary to the high-side FET. A short dead-time prevents shoot-through from occurring.

TIMING OPTIONS

Three versions of XRP6142 (Timing Options) are identified by their on times at V_{IN}=3.3V. For each version, T_{ON} is inversely proportional to V_{IN}. The constant of proportionality K, is shown in the table below. Variation of T_{ON} versus V_{IN} is shown graphically in figures 4 and 5.

Part Number	T_{ON} at V_{IN}=3.3V	K=T_{ON}xV_{IN} (µs.V)
XRP6142EL0.5-F	0.5µs	1.65
XRP6142EL1.0-F	1.0µs	3.3
XRP6142EL2.0-F	2.0µs	6.6

Note that for a Buck converter the switching frequency is given by:

$$f = \frac{V_{OUT}}{V_{IN} \times T_{ON}}$$

Since for each XRP6142 Timing Option, the product of V_{IN} and T_{ON} is a constant, then frequency is determined by V_{OUT} as shown in the following table.

V_{OUT}	f(kHz) for each Timing Option		
	0.5µs	1.0µs	2.0µs
0.8	485	242	121
1.0	606	303	152
1.2	727	364	182
1.5	909	455	227
1.8	1091	545	273
2.5	---	758	379
3.3	---	---	500

INTERNAL SOFT-START

Soft-start time is internally set at 5ms (nominal). This removes the need for external components associated with soft-start function, and helps save cost and reduce PCB space.

ENABLE

A precision enable function is provided (1.20V ±0.05V). EN should be tied to V_{CC} in applications that do not require this function.

INTERNAL REFERENCE VOLTAGE

A high-precision 0.5V internal reference is provided at the V_{REF} pin. This is normally tied to the REFIN pin, thus setting the threshold of the voltage comparator.

INTERNAL BOOTSTRAP DIODE

XRP6142 includes an internal low-Vf bootstrap diode. Place a 0.1uF capacitor between BST and SW pins to provide drive voltage for the high-side FET.

UNDER-VOLTAGE LOCKOUT

UVLO monitors V_{CC} and ensures adequate voltage exists before starting to switch the FETs.

SHORT CIRCUIT PROTECTION

An internal short-circuit comparator monitors the feedback voltage. If feedback voltage falls below 65% of reference voltage (this is equivalent to output voltage falling below 65% of nominal value) the IC will latch off. V_{CC} has

to be recycled in order for IC to resume operation.

OVERCURRENT PROTECTION (OCP)

OCP function is implemented by monitoring the voltage across the low-side FET when it is on. OCP is programmed via a resistor RLIM connected between ILIM and SW pins. An internal constant-current source ILIM (50uA nominal) establishes a voltage across RLIM. This voltage sets the trip point of the OCP comparator. If the OCP comparator is triggered for eight consecutive switching cycles, then a hiccup timeout, as described in the next section, is initiated. Calculate RLIM from:

$$RLIM = \frac{\left[\left(IOCP + \frac{\Delta IL}{2}\right) \times R_{DS(ON)}\right] + 20mV}{42.5\mu A}$$

Where:

IOCP is the output current at which overcurrent protection is activated (usually set 20% above maximum I_{OUT})

ΔIL is inductor current ripple nominally set at 30% of I_{OUT}

$R_{DS(ON)}$ is the maximum rated on resistance of the FET

20mV is the OCP comparator offset spec

42.5μA is the minimum spec of the ILIM source

The actual IOCP is 50% to 100% higher than expected IOCP as seen in figure 11. This is because RLIM in the above equation is calculated based on worst case parameters.

A temperature coefficient of 0.3%/°C has been designed into ILIM. This useful feature nulls out the positive temperature coefficient of the FET $R_{DS(ON)}$ to a first order. Thus IOCP should be largely independent of operating temperature.

HICCUP TIMEOUT

When an over current condition is detected, the internal FET drivers are turned off for 110ms, following which, a soft-start is attempted. If the OCP condition is still present, then the timeout and soft-start cycle repeat. This is referred to as hiccup timeout.

PROGRAMMING VOUT

A pair of output resistors is used to set the output voltage V_{OUT}. Calculate R1 from:

$$R1 = R2\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

Where:

R2 is nominally set at 10k (bottom resistor)

V_{REF} is reference voltage (0.5V)

Note that V_{OUT} must contain some voltage ripple in order for XRP6142 to regulate the output. Since XRP6142 regulates the bottom of the output ripple the average value will be higher (see figure 16).

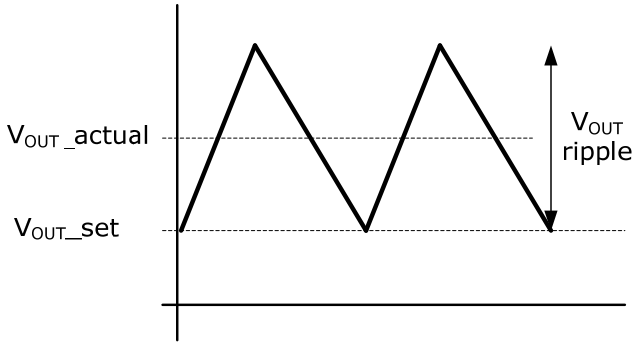


Fig. 16: V_{OUT} Voltage Ripple

V_{OUT} can be programmed more precisely from:

$$R1 = R2\left(\frac{V_{OUT} - (0.5 \times V_{OUT}, ripple)}{V_{REF}} - 1\right)$$

Where:

$$V_{OUT}, ripple = \Delta IL \times ESR$$

ESR is the output capacitor's Equivalent Series Resistance.

OUTPUT CAPACITOR

C_{OUT} is the most critical component for proper operation, since the XRP6142 relies on V_{OUT}

voltage ripple for regulating the output. To ensure stable operation two constraints must be met:

First the C_{OUT} must have sufficient ESR in order to get enough voltage ripple at feedback pin. It is recommended that XRP6142 be operated with at least 25mV ripple at feedback pin. Assuming majority of output voltage ripple is from ESR, we get:

$$ESR \geq \frac{25mV}{\Delta IL} \quad \text{..... (1)}$$

Where ΔIL is inductor current ripple nominally set at 30% of I_{OUT}.

Note that V_{OUT} ripple, is attenuated by the resistor divider R1/R2, and a smaller ripple is seen at FB pin. For example if V_{OUT} ripple is 25mV and R1=R2=10k, then the voltage ripple at FB is only 12.5mV. One solution to this problem is to increase the output ripple accordingly, such that ripple at FB is 25mV. A more desirable solution is to provide a high-frequency/low-impedance path for the output ripple to be transmitted to FB without attenuation. This can be done by placing a small feed-forward capacitor CFF in parallel with R1. As a starting point calculate CFF from:

$$CFF = \frac{10}{2 \times \pi \times R1 \times fs}$$

Where fs is the switching frequency

In general, a CFF of 1nF should provide satisfactory feed-forward for most applications based on the XRP6142.

The second constraint for stability establishes a relation between ESR and C_{OUT}.

$$ESR \geq \frac{Ton}{C_{OUT}} \quad \text{..... (2)}$$

Once ESR is calculated from equation (1), equation (2) can be used to calculate C_{OUT}.

The aforementioned are in addition to the usual requirements for C_{OUT} for a buck converter. The usual constraint in order to meet load step transient requirement is given by:

$$C_{OUT} \geq \frac{I_2^{\,2} - I_1^{\,2}}{Vos^2 - V_{OUT}^{\,2}}$$

Where:

I_2 is load step high-level current

I_1 is load step low-level current

V_{OUT} is output voltage including transient (nominally this is set 3% higher than V_{OUT})

In general, the best capacitors are the ones with known and consistent ESR across operating temperature range. Examples include POSCAPs, Tantalums and certain Aluminum Electrolytics.

OUTPUT INDUCTOR

Select the output inductor for inductance and current rating. As a rule of thumb the DC current rating and saturation current should be at least 50% higher than maximum output current. Calculate the inductance from:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta IL \times fs}$$

Where:

D is duty cycle

fs is switching frequency

ΔIL is inductor current ripple nominally set at 30% of I_{OUT}.

INPUT CAPACITOR

Select the input capacitor for capacitance, voltage rating and RMS current rating. As a rule of thumb, the voltage rating should be twice the maximum input voltage of the converter. RMS current rating can be approximated from:

$$I_{RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

Calculate C_{IN} such that input voltage ripple does not exceed 2% of V_{IN}. Ceramic input capacitors are recommended. This choice minimizes input voltage ripple due to ESL and ESR. Thus a simplified expression for C_{IN} can be written:

$$C_{IN} = \frac{I_{OUT,MAX} \times V_{OUT} \times (V_{IN} - V_{OUT})}{fs \times 0.02 V_{IN} \times V_{IN}^{2}}$$

SYNCHRONOUS FET (LOW-SIDE FET)

Select the synchronous FET for voltage rating BV_{DSS}, on resistance rating $R_{DS(ON)}$ and gate drive rating V_{GS}. As a rule of thumb, voltage rating should be at least twice the converter input voltage. FETs with voltage rating of up to 30V should provide satisfactory performance. Drive voltage of 4.5V is sufficient for applications with minimum input voltage of 4.5V. For applications with a lower input voltage a FET with 2.5V gate drive should be selected. Switching losses of the Synchronous FET are negligible in comparison to its conduction losses. $R_{DS(ON)}$ is calculated based on conduction losses from:

$$R_{DS(ON)} \le \frac{P_{Conduction}}{(1-D) \times I_{OUT}^{2}}$$

It is common practice to allocate 50% of the total FET losses to the synchronous FET. As an example, consider a 10W buck converter with a target efficiency of 90%. Therefore, the target total power loss is 1.1W. Assume that the only significant non-FET loss is the inductor loss estimated at 0.1W. Thus the maximum conduction loss of the synchronous FET should not exceed 0.5W. By using this value in the above equation $R_{DS(ON)}$ can be calculated and a suitable FET selected.

SWITCHING FET (HIGH-SIDE FET)

Select the switching FET for voltage rating BV_{DSS}, on-resistance rating $R_{DS(ON)}$, gate drive rating V_{GS}, rise time t_r and fall time t_f. BV_{DSS} and V_{GS} selection guidelines are the same as Synchronous FET. The switching FET incurs switching (i.e., transitional) as well as conduction losses. $R_{DS(ON)}$ is calculated based on conduction losses from:

$$R_{DS(ON)} \le \frac{P_{Conduction}}{D \times I_{OUT}^{2}}$$

It is common practice to allocate 50% of the total high-side FET losses to conduction. Proceeding with the example from previous section the total target loss is 0.5W, and thus target conduction loss equals 0.25W. By using this value in the above equation $R_{DS(ON)}$ can be calculated. Rise and fall time can be approximated from:

$$t_r + t_f = \frac{P_{Switching}}{V_{IN} \times I_{out} \times f_s}$$

Since the allotted switching loss budget is 0.25W, t_r and t_f can be calculated from the above equation.

For a detailed explanation of FET losses and FET selection procedure refer to EXAR application note ANP-20.

R-C SNUBBER (OPTIONAL)

An R-C snubber placed across the synchronous FET eliminates the ringing and reduces the amplitude of overshoot at SW node. Use surface-mount components and place them close to the FET drain-source. Calculate the value of snubber capacitor Csnb from:

$$Csnb = 3 \times Coss$$

Coss is the output capacitance of the synchronous FET corresponding to V_{IN}.

Calculate the value of the snubber resistor Rsnb from:

$$Rsnb = \frac{2 \times V_{OUT}}{I_{OUT}}$$

DDR MEMORY POWER APPLICATIONS

XRP6142 can be used to generate the required V_{DDQ} (V_{DD}) or V_{TT} Reference voltages for DDR I, II and III memories and provides a 40mA buffered V_{TT} Reference voltage. When used in conjunction with Exar's SP2996 DDR Memory Termination, the XRP6142 provides a complete DDR power management solution. A cost-effective DDR2 solution is shown on page 15. XRP6142 provides the VDDQ and VTTREF voltages. SP2996 provides the VTT voltage. Please note that the current output of VDDQ can be increased up to 10A by using a larger QT/QB MOSFET and scaling the L1 and C3 accordingly.

PCB LAYOUT GUIDELINES

The following guidelines will help attain stable operation and reduce jitter:

1- Place all the power components; C_{IN}, QT, QB, L1 and C_{OUT} on the same side of the board if possible.

2- Make the loop between C_{IN}, QT and QB as small as possible and use low-impedance traces.

3- Make the loop between QB, L1 and C_{OUT} as small as possible and use low-impedance traces.

4- Place the source of QT, drain of QB and input connection of L1 as close as possible and use low-impedance traces.

5- Use a short trace and connect AGND to the thermal pad. This forms the signal ground.

6- Use a short trace and connect PGND to AGND.

7- Use a low-impedance trace and connect the PGND pin to the C_{OUT}.

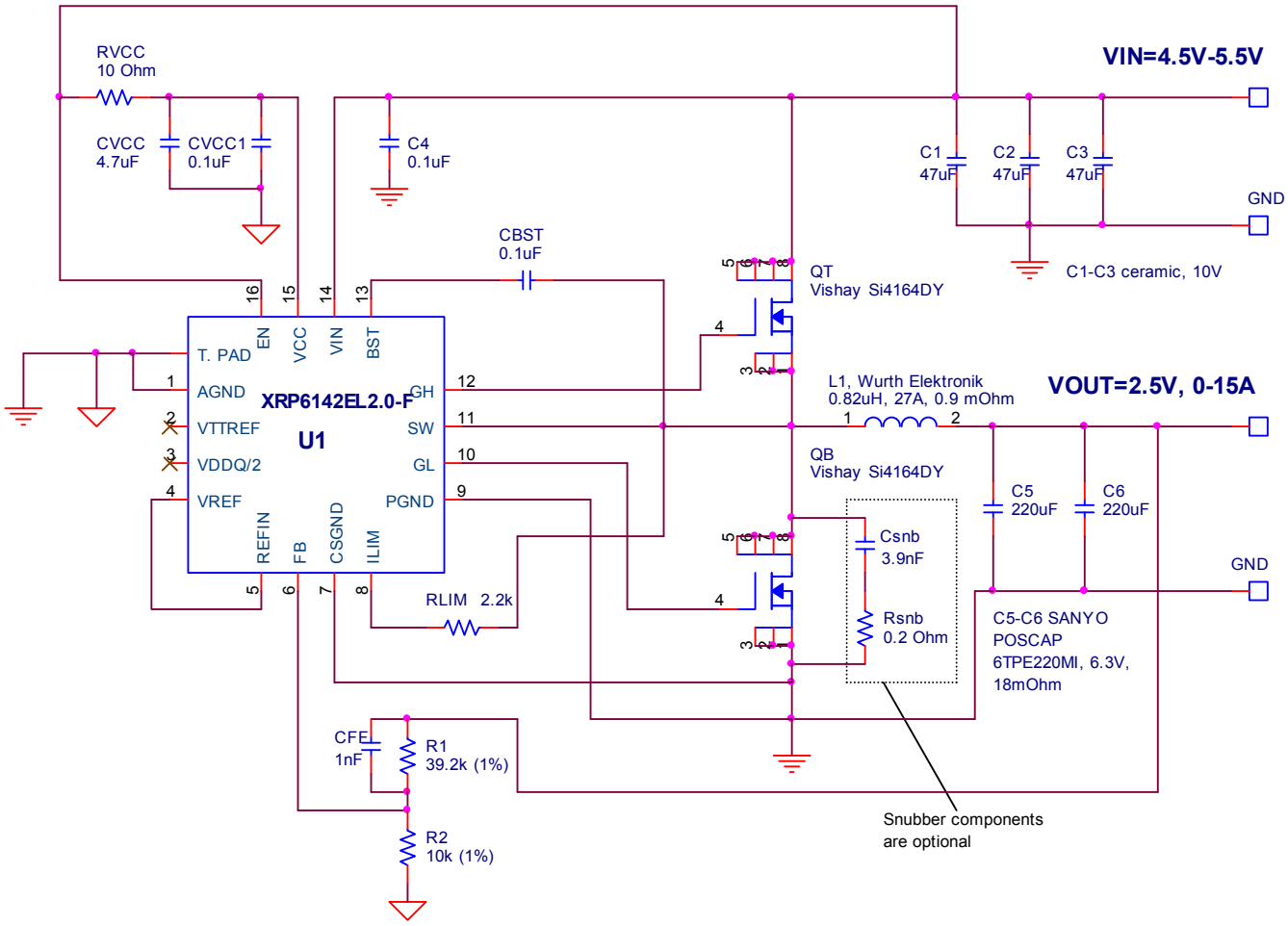
8- Place CFF, R1 and R2 close to the IC, and connect R2 to signal ground. Use a short trace and connect R1 to C_{OUT}.

9- Bypass the V_{CC} pin to signal ground with a ceramic capacitor(s) as close to the IC as possible. Connect the V_{CC} pin to V_{IN} or an independent V_{CC} source through a 10Ω resistor. This will help filter out noise from V_{CC}.

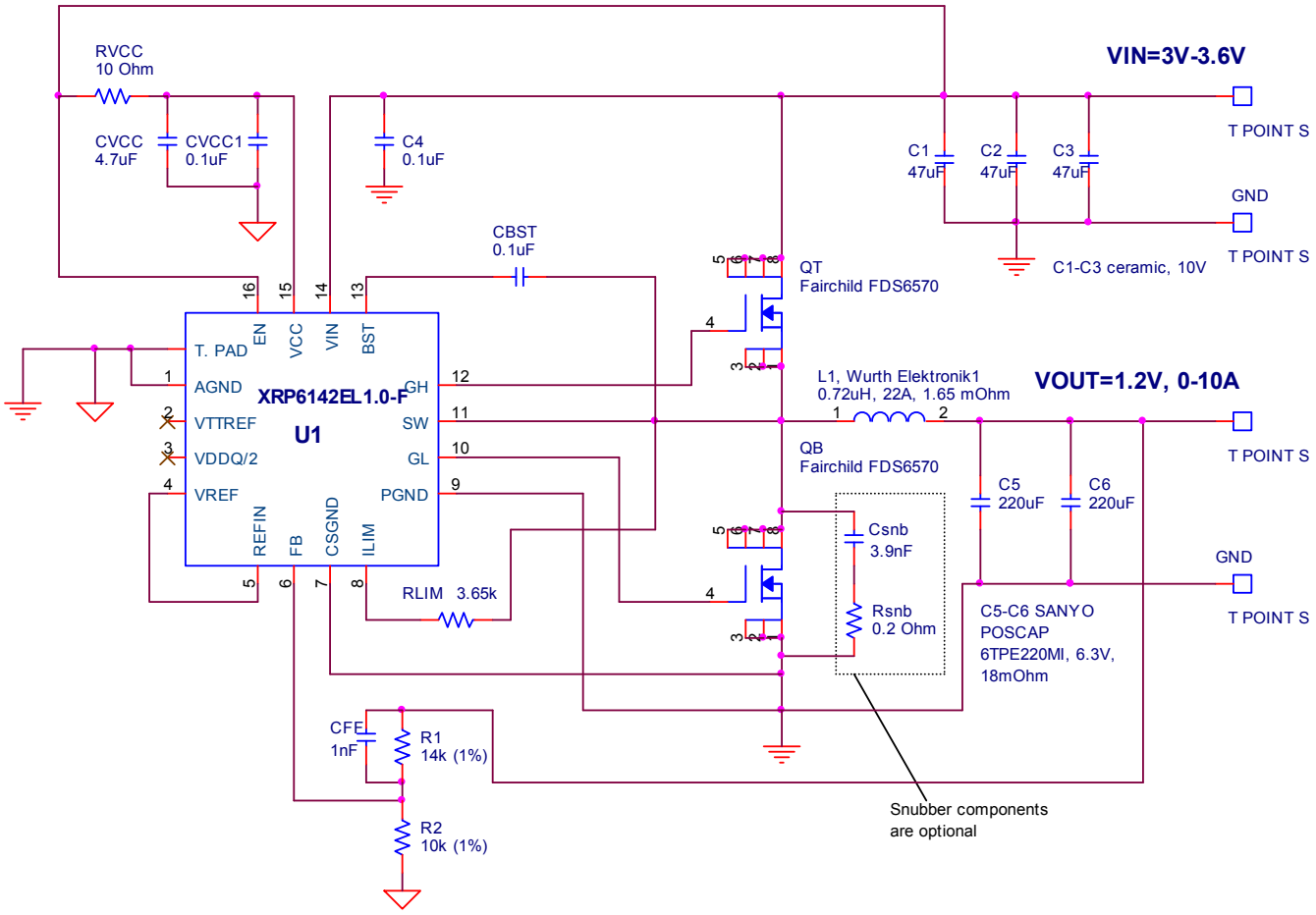
DESIGN EXAMPLES

5V STEP-DOWN CONVERTER

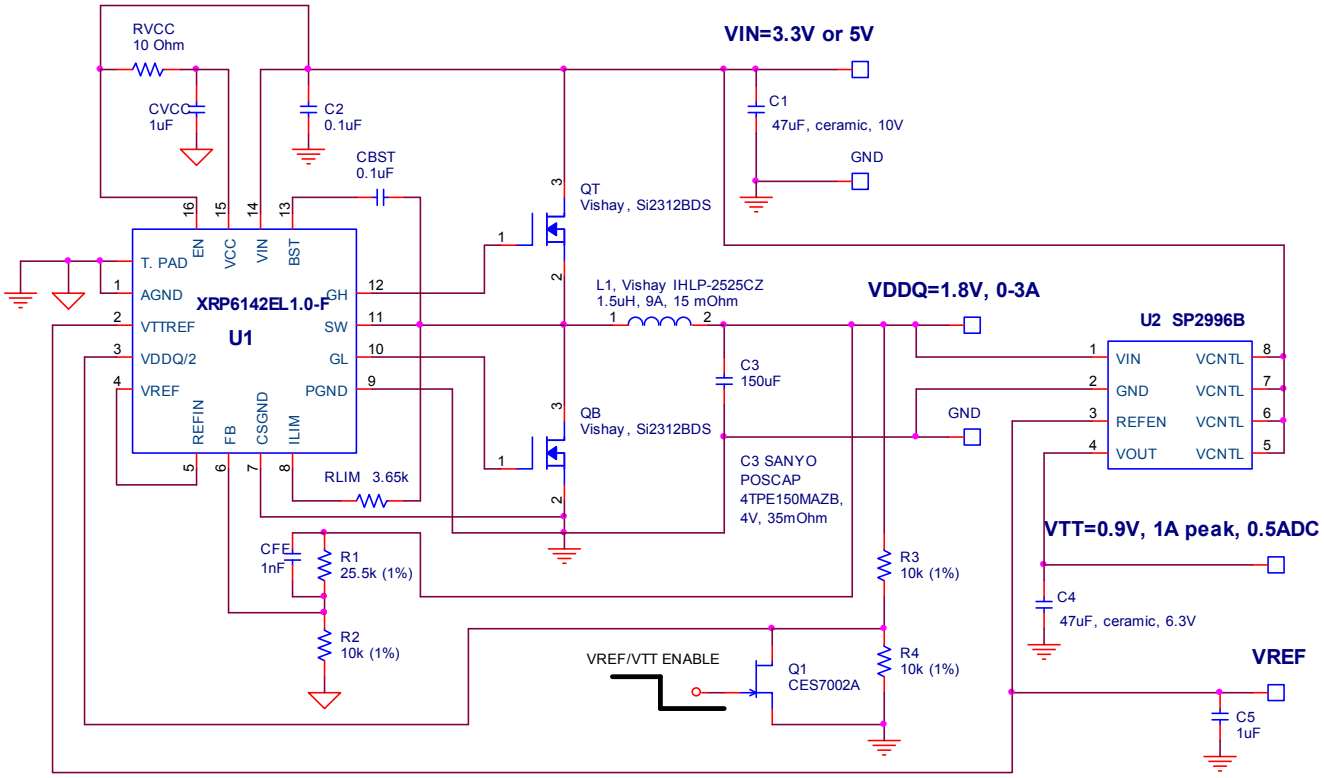
Note: The data shown in figures 6 trough 15 was collected using this circuit.



3.3V STEP-DOWN CONVERTER

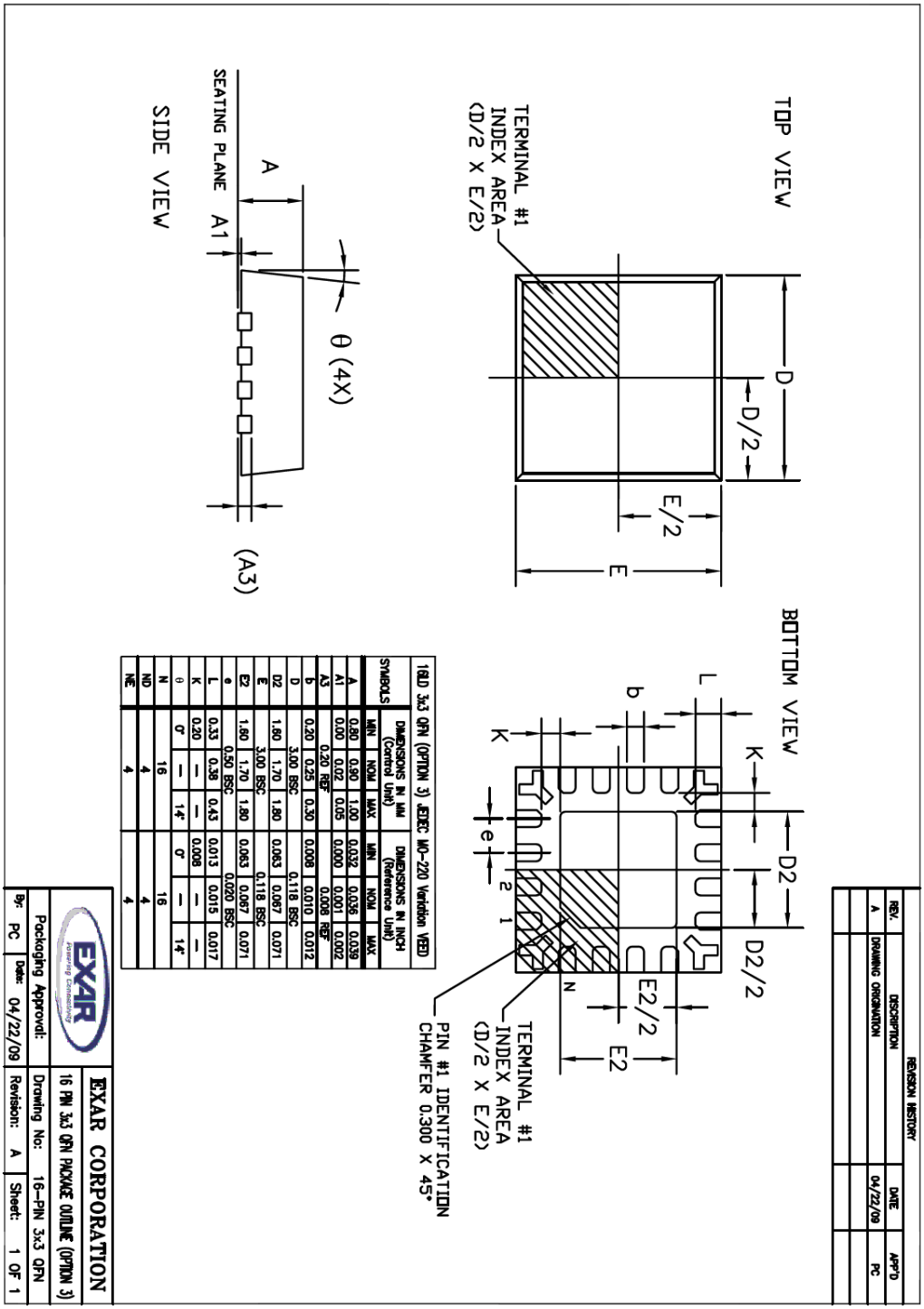


DDR2 MEMORY SOLUTION



PACKAGE SPECIFICATION

16-PIN QFN



16LD 3x3 QFN (OPTION 3) JEDEC MO-220 Variation VEED

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.036	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.20	0.25	0.30	0.008	0.010	0.012
D		3.00 BSC			0.118 BSC	
D2	1.80	1.70	1.80	0.063	0.067	0.071
E		3.00 BSC			0.118 BSC	
E2	1.80	1.70	1.80	0.063	0.067	0.071
e		0.50 BSC			0.020 BSC	
L	0.33	0.38	0.43	0.013	0.015	0.017
K	0.20	—	—	0.008	—	—
θ	0°	—	14°	0°	—	14°
N	16			16		
ND	4			4		
NE	4			4		

REVISION HISTORY

Revision	Date	Description
1.0.0	03/24/2010	Initial release of datasheet

FOR FURTHER ASSISTANCE

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