Future Technology Devices International Ltd.

FT313H

(USB2.0 HS Embedded Host Controller)

The FT313H is a Hi-Speed Universal Serial Bus (USB) Host Controller compatible with Universal Serial Bus Specification Rev 2.0 and supports data transfer speeds of up to 480M bit/s. The FT313H has the following advanced features:

- Single chip USB2.0 Hi-Speed compatible.
- Compatible to Enhanced Host Controller Interface Specification Rev 1.0.
- The USB1.1 host is integrated into the USB2.0 EHCI compatible host controller.
- Single USB host port.
- Supports data transfer at high-speed (480M bit/s), full-speed (12M bit/s), and low-speed (1.5M bit/s).
- Supports the Isochronous, Interrupt, Control, and Bulk transfers.
- Supports the split transaction for high-speed Hub and the preamble transaction for full-speed Hub.
- Supports multiple processor interfaces with 8-bit or 16-bit bus: SRAM, NOR Flash, and General multiplex.
- Single configurable interrupt (INT) line for host controller.
- Integrated 24kB high speed RAM memory.
- Supports DMA operation.
- Integrated Phase-Locked Loop (PLL) supports external 12MHz, 19.2MHz, and 24MHz crystal, and direct external clock source input.
- Low power consumption for portable application.
- Supports bus interface I/O voltage from 1.62V to 3.63V.
- Supports hybrid power mode; VCC(3V3) is not present, VCC(I/O) is powered.
- Internal voltage regulator supplies 1.2v to the digital core.
- Supports Battery Charging Specification Rev 1.2.
- The downstream port can be configured as SDP, CDP or DCP.
- Supports VBUS power switching and over current control.
- -40°C to 85°C extended operating temperature range.
- Available in compact Pb-free 64 Pin QFN, LQFP and TQFP packages (all RoHS compliant).

1 Typical Applications

- TV/TV box
- Printer
- Instrumentation
- Media player
- Tablet
- Set-top box

1.1 Part Numbers

Part Number	Package
FT313HQ-x	64 Pin QFN
FT313HL-x	64 Pin LQFP
FT313HP-x	64 Pin TQFP

Table 1-1 FT313H Numbers

Note: Packaging codes for x is:

-R: Taped and Reel, (QFN is 3000pcs, LQFP is 1000 pcs, TQFP is 2500pcs per reel)

-T: Tray packing, (QFN is 2600pcs, LQFP is 1600 pcs, TQFP is 2500pcs per tray)

For example: FT313HQ-R is 3000 QFN pcs in taped and reel packaging

1.2 USB Compliant

At the time of writing this datasheet, the FT313H was still to complete USB compliance testing.

2 FT313H Block Diagram

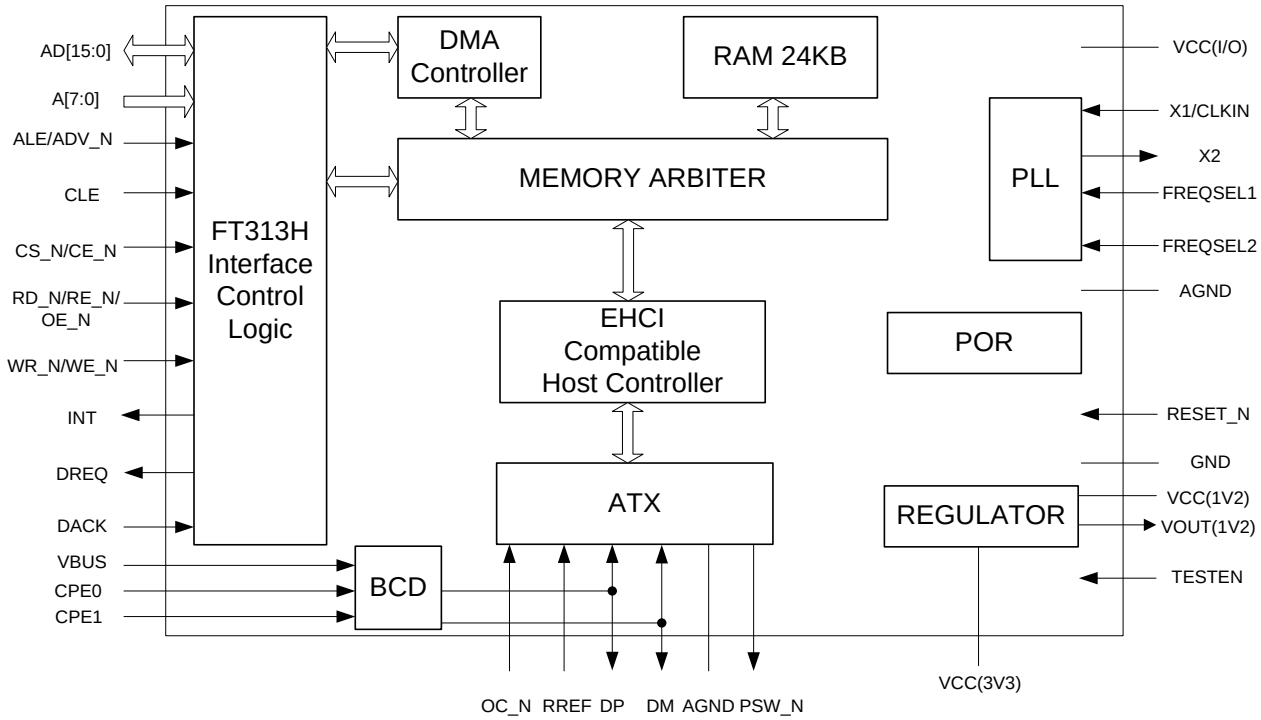

Figure 2-1 FT313H Block Diagram

For a description of each function please refer to Section 4.

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3 Device Pin Out and Signal Description

3.1 Pin Out – 64pin QFN

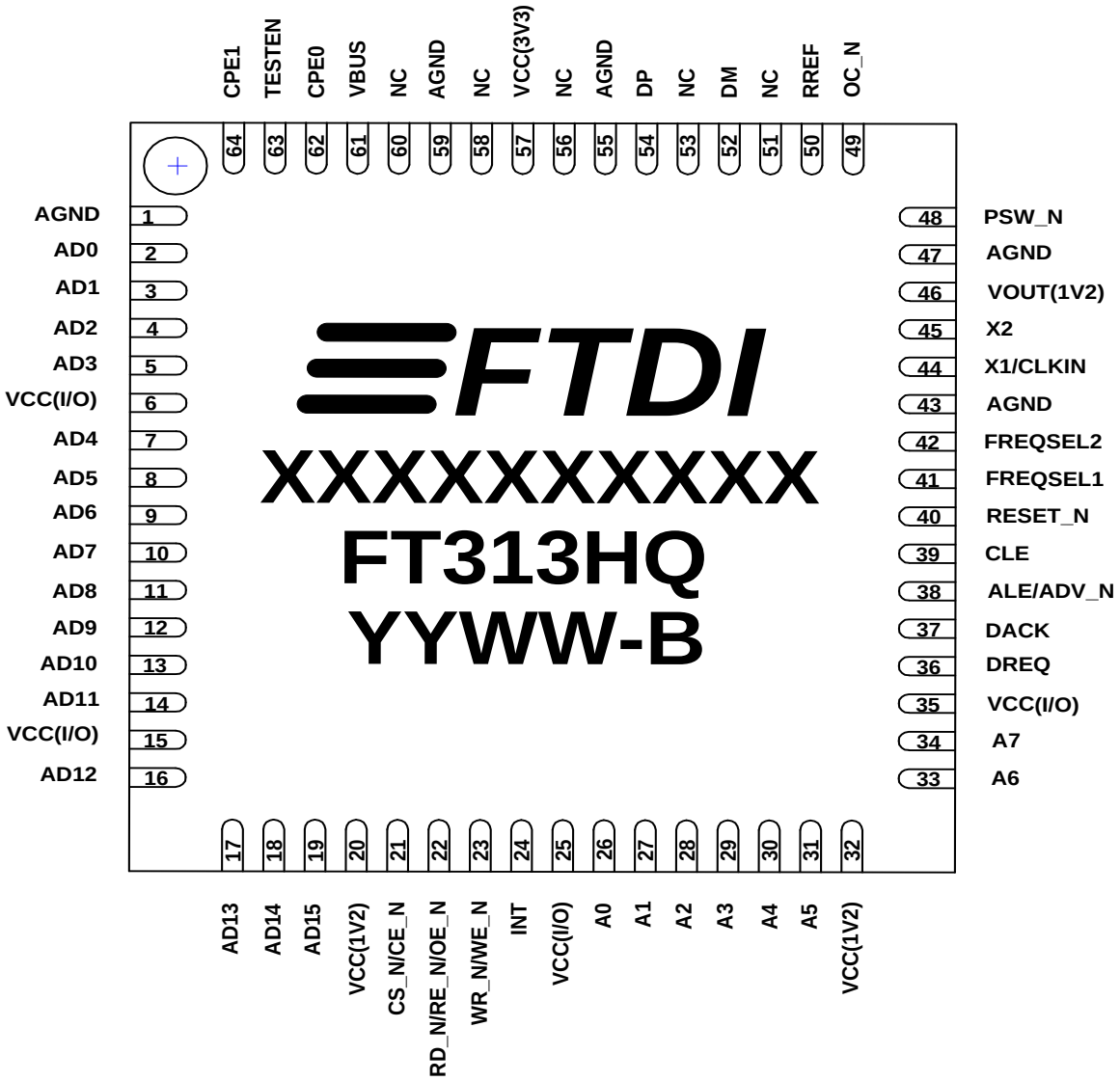


Figure 3-1 Pin Configuration QFN64 (top-down view)

3.2 Pin Out – 64pin LQFP

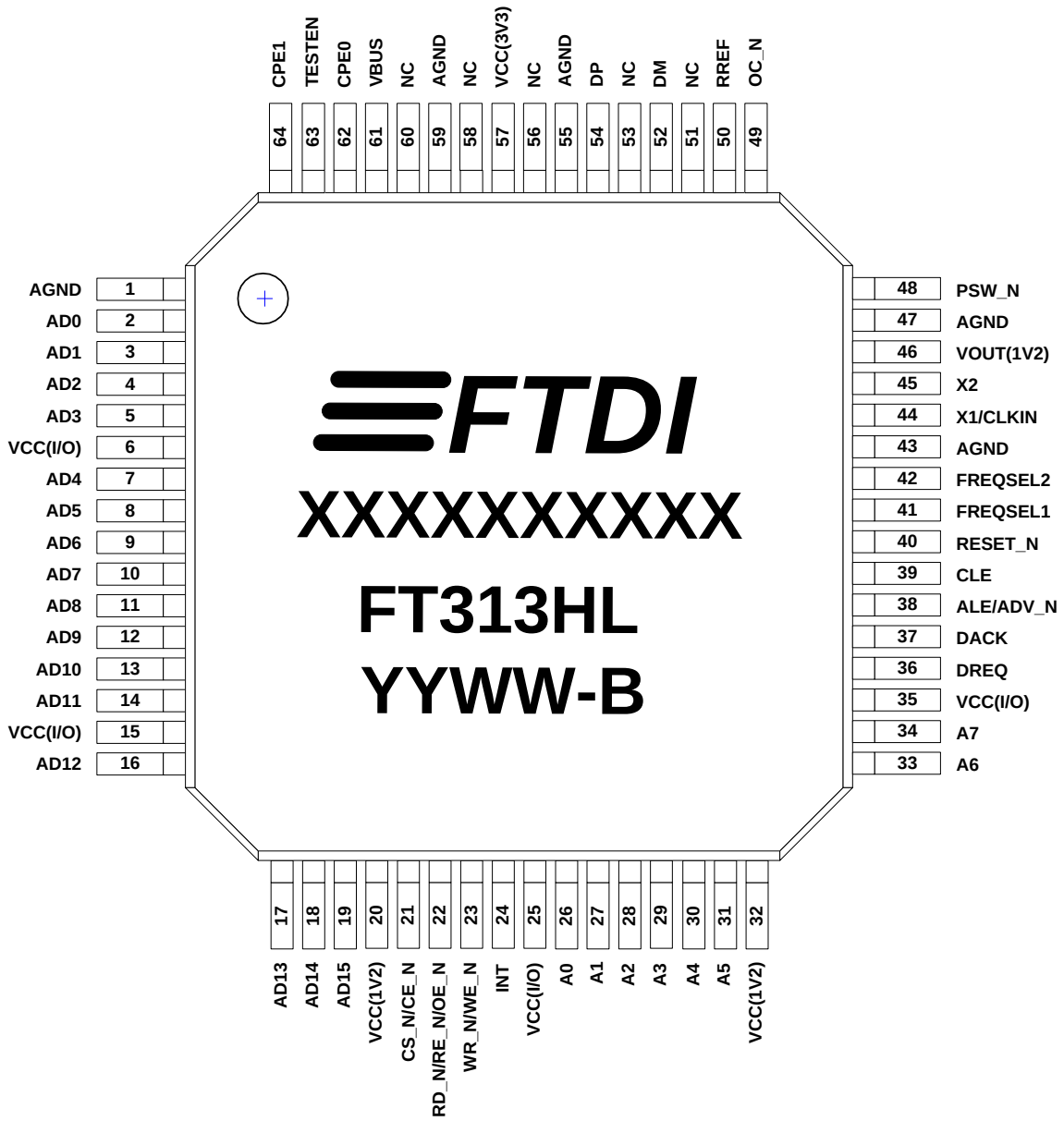


Figure 3-2 Pin Configuration LQFP64 (top-down view)

3.3 Pin Out – 64pin TQFP

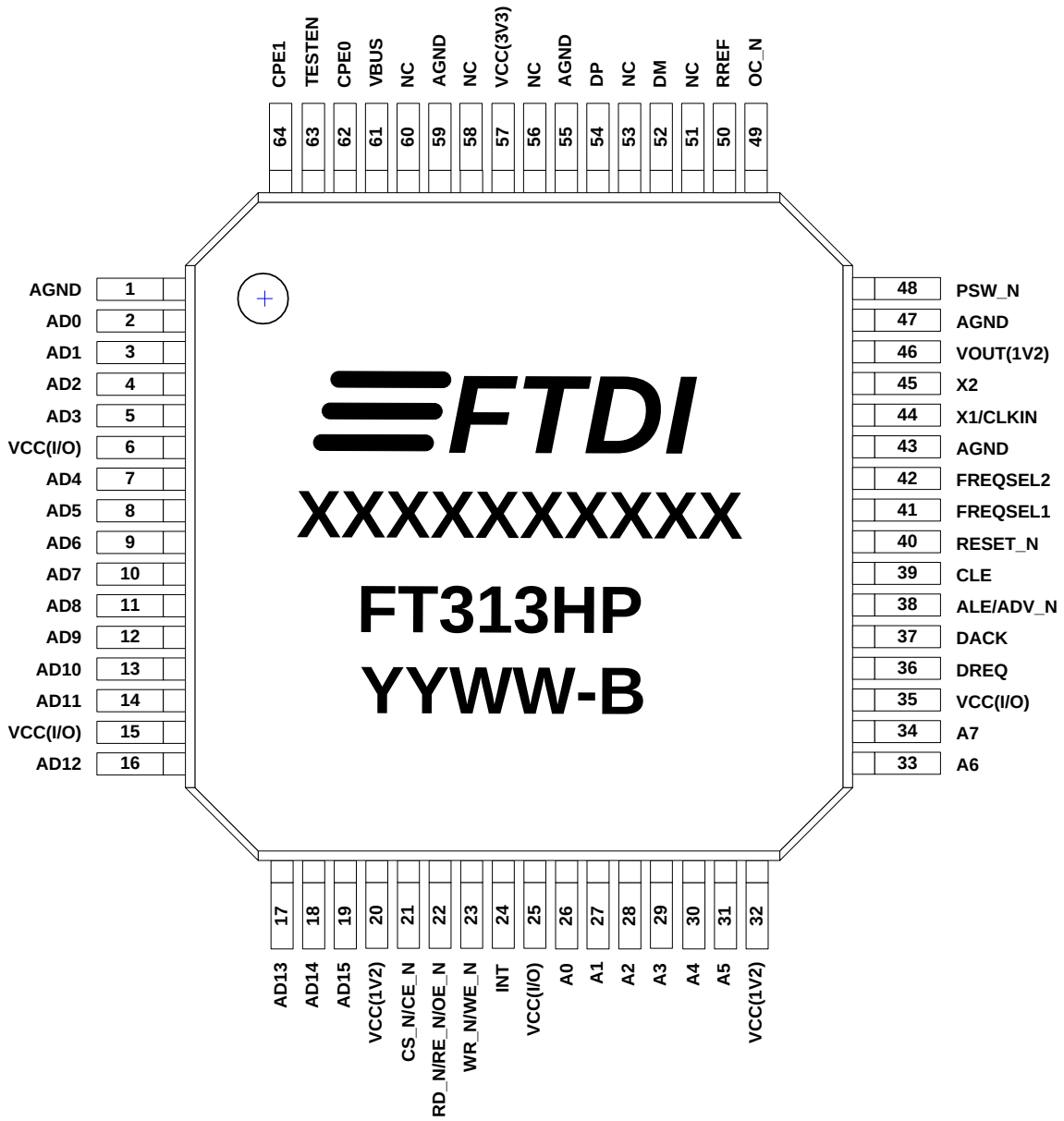


Figure 3-3 Pin Configuration TQFP64 (top-down view)

3.4 Pin Description

Pin No.	Name	Type	Description
1	AGND	P	Analog Ground
2	AD0	I/O	Bit 0 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
3	AD1	I/O	Bit 1 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
4	AD2	I/O	Bit 2 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
5	AD3	I/O	Bit 3 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
6	VCC(I/O)	P	I/O supply voltage; connect a 0.1uF decoupling capacitor 1.8V, 2.5V or 3.3V
7	AD4	I/O	Bit 4 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
8	AD5	I/O	Bit 5 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
9	AD6	I/O	Bit 6 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
10	AD7	I/O	Bit 7 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
11	AD8	I/O	Bit 8 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
12	AD9	I/O	Bit 9 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
13	AD10	I/O	Bit 10 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
14	AD11	I/O	Bit 11 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
15	VCC(I/O)	P	I/O supply voltage; connect a 0.1uF decoupling capacitor

Pin No.	Name	Type	Description
			1.8V, 2.5V or 3.3V
16	AD12	I/O	Bit 12 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
17	AD13	I/O	Bit 13 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
18	AD14	I/O	Bit 14 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
19	AD15	I/O	Bit 15 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
20	VCC(1V2)	P	Core power 1.2V input; for normal operation, this pin must be connected to pin 46. Connect a 0.1uF decoupling capacitor
21	CS_N/CE_N	I	Chip select; Input ; 3.3V tolerant
22	RD_N /RE_N/OE_N	I	Read enable, or read latch; when not in use, connect to VCC(I/O) Input; 3.3V tolerant
23	WR_N /WE_N	I	Write enable; when not in use, connect to VCC(I/O) Input; 3.3V tolerant
24	INT	O	Interrupt output Push-pull output; 3.3V tolerant
25	VCC(I/O)	P	I/O supply voltage; connect a 0.1uF decoupling capacitor 1.8V, 2.5V or 3.3V
26	A0	I	Bit 0 of the address bus; when not in use, connect to GND Input; 3.3V tolerant
27	A1	I	Bit 1 of the address bus; when not in use, connect to GND Input; 3.3V tolerant
28	A2	I	Bit 2 of the address bus; when not in use, connect to GND Input; 3.3V tolerant
29	A3	I	Bit 3 of the address bus; when not in use, connect to GND Input; 3.3V tolerant

Pin No.	Name	Type	Description
30	A4	I	Bit 4 of the address bus; when not in use, connect to GND Input; 3.3V tolerant
31	A5	I	Bit 5 of the address bus; when not in use, connect to GND Input; 3.3V tolerant
32	VCC (1V2)	P	Core power 1.2V input; for normal operation, this pin must be connected to pin 46. Connect a 0.1uF decoupling capacitor.
33	A6	I	Bit 6 of the address bus; when not in use, connect to GND Input; 3.3V tolerant
34	A7	I	Bit 7 of the address bus; when not in use, connect to GND Input; 3.3V tolerant
35	VCC(I/O)	P	I/O supply voltage; connect a 0.1uF decoupling capacitor 1.8V, 2.5V or 3.3V
36	DREQ	O	DMA request; Push-pull output; 3.3V tolerant
37	DACK	I	DMA acknowledge; Internal pull-down. Input; 3.3V tolerant
38	ALE/ADV_N	I	Address latch enable Input; 3.3V tolerant
39	CLE	I	Command latch enable Input; 3.3V tolerant
40	RESET_N	I	Chip reset; Internal pull-up. Input; 3.3V tolerant
41	FREQSEL1	I	Input clock frequency selection pin1 Input; 3.3V tolerant
42	FREQSEL2	I	Input clock frequency selection pin2 Input; 3.3V tolerant
43	AGND	P	Analog Ground
44	X1/CLKIN	AI	Crystal oscillator or clock input; 3.3V peak input allowed
45	X2	AO	Crystal oscillator output; leave open if an external clock is applied on pin X1/CLKIN
46	VOUT(1V2)	AO	Internal 1.2V regulator output; connect 4.7uF and

Pin No.	Name	Type	Description
			0.1uF decoupling capacitors to this pin.
47	AGND	P	Analog Ground
48	PSW_N	OD	Port power switch; when not in use, connect to VCC(3V3) through a 10kΩ resistor Open drain output; 5V tolerant
49	OC_N	I	Over current input; when not in use, connect to VCC(3V3) through a 10KΩ resistor Input; 5V tolerant
50	RREF	AI	Port reference resistor connection Connect 12 kΩ±1% resistor between RREF and GND
51	NC		No connect
52	DM	AI/O	Port DM; connect to the D- pin of the USB connector
53	NC		No connect
54	DP	AI/O	Port DP; connect to the D+ pin of the USB connector
55	AGND	P	Analog Ground
56	NC		No connect
57	VCC(3V3)	P	Supply 3.3V voltage; Connect 10uF and 0.1uF decoupling capacitors
58	NC		No connect
59	AGND	P	Analog Ground
60	NC		No connect
61	VBUS	OD	VBUS discharge. 5V tolerant
62	CPE0	I	Bit 0 to select charging port emulation type
63	TESTEN	I	Enable test mode. Internal pull-down. For normal operation leave floating.
64	CPE1	I	Bit 1 to select charging port emulation type

Table 3-1 FT313H pin description

Notes:

P : Power or ground
I : Input
O : Output
OD : Open drain output
I/O : Bi-direction Input and Output
AI : Analog Input
AO : Analog Output
AI/O : Analog Input / Output

4 Function Description

The FT313H is a USB2.0 compatible EHCI single port host controller which is mainly composed of the following:

- Microcontroller bus interface
- SRAM bus interface mode
- NOR bus interface mode
- General multiplex bus interface mode
- Interface mode lock
- DMA controller
- EHCI host controller
- System clock
- Power management
- BCD mode

The functions for each block are briefly described in the following subsections.

4.1 Microcontroller Bus Interface

The FT313H has a fast advance general purpose interface to communicate with most types of microcontrollers and microprocessors. This microcontroller interface is configured using pins ALE/ADV_N and CLE to accommodate most types of interfaces. The bus interface supports 8-bit and 16-bit, which can be configured using bit DATA_BUS_WIDTH. Three bus interface types are selected using inputs ALE/ADV_N and CLE during power up, the RD_N /RE_N/OE_N and CS_N/CE_N pins, or the RESET_N pin. Table 4.1 provides detail of bus configuration for each mode. Table 4.2 shows pinout information of each bus interface.

Bus Mode	ALE/ADV_N	CLE	DATA_BUS_WIDTH	Signal Description
SRAM 8-bit	HIGH	HIGH	1	• A[7:0]: 8-bit address bus • AD[7:0]: 8-bit data bus • Write (WR_N), read (RD_N), chip select (CS_N): control signals for normal SRAM mode • DACK: DMA acknowledge input • DREQ: DMA request output
SRAM 16-bit	HIGH	HIGH	0	• A[7:0]: 8-bit address bus • AD[15:0]: 16-bit data bus • Write (WR_N), read (RD_N), chip select (CS_N): control signals for normal SRAM mode • DACK: DMA acknowledge input • DREQ: DMA request output
NOR 8-bit	HIGH	LOW	1	• AD[7:0]: 8-bit data bus • ADV_N, write enable, output enable, chip select: control signals
NOR 16-bit	HIGH	LOW	0	• AD[15:0]: 16-bit data bus • ADV_N, write enable, output enable, chip select: control signals
General Multiplex 8-bit	LOW	HIGH	1	• AD[7:0]: 8-bit data bus • ALE, write(WR_N), read(RD_N), chip

Bus Mode	ALE/ADV_N	CLE	DATA_BUS_WIDTH	Signal Description
				select: control signals • DACK: DMA acknowledge input • DREQ: DMA request output
General Multiplex 16-bit	LOW	HIGH	0	• AD[15:0]: 16-bit data bus • ALE, write(WR_N), read(RD_N), chip select: control signals • DACK: DMA acknowledge input • DREQ: DMA request output

Table 4-1 Bus Configuration modes

SRAM mode	NOR mode	General Multiplex mode	Type	Description
AD[15:0]	AD[15:0]	AD[15:0]	I/O	Data or address bus
A[7:0]	-	-	I	Address bus
-	ADV_N	ALE	I	Address or command valid
CS_N	CS_N	CS_N	I	Chip select
RD_N/RE_N	OE_N	RD_N/RE_N	I	Read control
WR_N/WE_N	WE_N	WR_N/WE_N	I	Write control
INT	INT	INT	O	Interrupt request
DREQ	-	DREQ	O	DMA request
DACK	-	DACK	I	DMA acknowledge

Table 4-2 Pin information of the bus interface

4.2 SRAM bus interface mode

The bus interface will be in SRAM 16-bit mode if pins ALE/ADV_N and CLE are HIGH, when:

- The CS_N/CE_N pin goes LOW, and the RD_N /RE_N/OE_N pin goes LOW.

Then, if the DATA_BUS_WIDTH bit is set, the bus interface will be in SRAM 8-bit mode.

In SRAM mode, A[7:0] is the 8-bit address bus and AD[15:0] is the separate 16-bit data bus. The FT313H pins RD_N /RE_N/OE_N and WR_N/WE_N are the read and write strobes. The SRAM bus interface supports both 8-bit and 16-bit bus width that can be configured by setting or clearing bit DATA_BUS_WIDTH. The DMA transfer is also applicable to this interface.

4.3 NOR bus interface mode

The bus interface will be in NOR 16-bit mode, if pin ALE/ADV_N is HIGH and pin CLE is LOW, when:

- The CS_N/CE_N pin goes LOW, and the RD_N /RE_N/OE_N pin goes LOW.

Then, if the DATA_BUS_WIDTH bit is set, the bus interface will be in NOR 8-bit mode.

The NOR Flash interface access consists of two phases: address and data.

The address is valid when CS_N/CE_N and ADV_N are LOW, and the address is latched at the rising edge of ADV_N. For a read operation, WE_N must be HIGH. OE_N is the data output control. When active, the addressed register or the buffer data is driven to the I/O bus. The read operation is completed when CS_N/CE_N is de-asserted. For a write operation, OE_N must be HIGH. The WE_N assertion can start when ADV_N is de-asserted. WE_N is the data input strobe signal. When de-asserted, data will be written to the addressed register or the buffer. The write operation is completed when CS_N/CE_N is de-asserted.

4.4 General multiplex bus interface mode

The bus interface will be in general multiplex 16-bit mode, if pin ALE/ADV_N is LOW and pin CLE is HIGH, when:

- The CS_N/CE_N pin goes LOW, and the RD_N /RE_N/OE_N pin goes LOW.

Then, if the DATA_BUS_WIDTH bit is set, the bus interface will be in general multiplex 8-bit mode. The general multiplex bus interface supports most advance application processors.

The general multiplex interface access consists of two phases: address and data.

The address is valid when ALE/ADV_N goes HIGH, and the address is latched at the falling edge of ALE/ADV_N. For a read operation, WR_N/WE_N must be HIGH. RD_N /RE_N/OE_N is the data output control. When active, the addressed register or the buffer data is driven to the I/O bus. The read operation is completed when CS_N/CE_N is de-asserted. For a write operation, RD_N /RE_N/OE_N must be HIGH. The WR_N/WE_N assertion can start when ALE/ADV_N is de-asserted. WR_N/WE_N is the data input strobe signal. When de-asserted, data will be written to the addressed register or the buffer. The write operation is completed when CS_N/CE_N is de-asserted. The DMA transfer is also applicable to this interface.

4.5 Interface mode lock

The bus interface can be locked in any of the modes, SRAM, NOR, or general multiplex, using bit 3 of the HW Mode Control register. To lock the interface in a particular mode:

1. Read bits 7 and 6 of the SW Reset register.
2. Set bit 3 of the HW Mode Control register to logic 1.
3. Read bits 7 and 6 of the SW Reset register to ensure that the interface is locked in the desired mode.

Note: the default is 16-bit SRAM mode.

4.6 DMA controller

The DMA controller of the FT313H is used to transfer data between the system memory and local buffers. It shares data bus AD[15:0] and control signals WR_N/WE_N, RD_N /RE_N/OE_N, and CS_N/CE_N. The logic is dependent on the bus interface mode setting.

DREQ signal is from the FT313H to indicate the start of DMA transfer. DACK signal is used to differentiate if data transferred is for the DMA or PIO access. When DACK is asserted, it indicates that it is still in DMA mode. When DACK is de-asserted, it indicates that PIO is to be accessed. ALE/ADV_N and CLE are ignored in a DMA access cycle. Correct data will be captured only on the rising edge of WR_N/WE_N and RD_N /RE_N/OE_N.

The DMA controller of the FT313H has only one DMA channel. Therefore, only one DMA read or DMA write may take place at a time. Assign the DMA transfer length in the Data Session Length register for each DMA transfer. If the transfer length is larger than the burst counter, the DREQ signal will de-assert at the end of each burst transfer. DREQ will re-assert at the beginning of the each burst.

When DMA is transferring data from/to local buffer, if it wants to access local buffer content by PIO mode, can use auxiliary memory access registers AUX_MEMADDR and AUX_DATAPORT to read/write data from/to local buffer with single cycle.

For a 16-bit DMA transfer, the minimum burst length is 2 bytes. This means that the burst length is only one DMA cycle. Therefore, DREQ and DACK will assert and de-assert at each DMA cycle.

The FT313H will be asserted DMA EOT interrupt to indicate that the DMA transfer has either successfully completed or terminated.

4.7 EHCI host controller

The FT313H is a one-port EHCI-compatible host controller which supports all the USB 2.0 compliant Low-speed, Full-speed, and High-speed devices and split/preamble transactions for the HS/FS hub.

The EHCI host controller supports two categories of the transfer types, the periodic and asynchronous transfer types. The periodic transfer type includes the isochronous and interrupt transfers, while the asynchronous transfer type includes the control and bulk transfers.

The EHCI host controller has schedule interface that provides to the separate schedules for each category of the transfer type. The periodic schedule is based on a time-oriented frame list that represents a slide window of time of the host controller work items. All the ISO and INT transfers are serviced via the periodic schedule. The asynchronous schedule is a simple circular list of the schedule work items that provides a round robin service opportunity for all the asynchronous transfers.

The EHCI host controller contains the Isochronous Transfer Descriptor (iTD), Queue Head (qH) and Queue Element Transfer Descriptor (qTD), and Split Transaction Isochronous Transfer Descriptor (siTD) data structure interface to support the isochronous/interrupt/control/bulk transfers and split transaction.

The EHCI host controller internal buffer memory is 24KB. START_ADDR_MEM register is allocated from 0x0000 to 0x5FFF.

4.8 System clock

4.8.1 Phase Locked Loop (PLL) clock multiplier

The internal PLL supports 12MHz, 19.2MHz, or 24MHz input, which can be crystal or a clock already existing in system. The frequency selection can be done using the FREQSEL1 and FREQSEL2 pins. Table 4.3 provides clock frequency selection.

FREQSEL1	FREQSEL2	Clock Frequency
0	0	12MHz
1	0	19.2MHz
0	1	24MHz

Table 4-3 Clock frequency select

4.9 Power management

4.9.1 Power up and reset sequence

When VCC(I/O) and VCC(3V3) are on, an internal regulator will power on with VCC(3V3) on. An internal POR pulse will be generated during the regulator power on, so that internal circuits are in reset state until the regulator power is stable.

4.9.2 Power supply

Power supplies are defined in Table 4.4.

Symbol	Typical	Description
VCC(I/O)	1.8V, or 2.5V, or 3.3V	Supply for digital I/O pad
VCC(3V3)	3.3V	Supply for chip

Table 4-4 Power supply

4.9.3 ATX reference voltage

The ATX circuit provides a stable internal voltage reference (+1.2V) to bias the analog circuitry. This circuit requires an accurate external reference resistor. Connect 12kΩ±1% resistor between pins RREF and GND.

4.9.4 Power modes

Power management configuration defined in Table 4.5.

For each bit description, see CONFIG register.

OSC_EN	PLL_EN	HC_CLK_EN	Description
1	1	1	Operation mode
0	0	0	Suspend mode

Table 4-5 power management configuration

4.9.4.1 Operation mode

All power supplies are present. Host controller is active.

4.9.4.2 Suspend mode

All power supplies are present. Host controller goes to USB suspend.

The steps for the host suspend are as follows:

1. Clear the RS bit of the USBCMD register to stop the host controller from executing schedule.
2. Set the PO_SUSP bit of the PORTSC register to force the host controller to go into suspend.
3. Disable OSC_EN, PLL_EN and HC_CLK_EN bits of the CONFIG register to save power.
4. Clear the U_SUSP_U bit of the EOTTIME register to put the chip into suspend mode.

4.9.4.3 Wake up

The regulator will be in normal operating mode and the clock/oscillator/PLL will be enabled when either of these conditions is triggered:

1. Dummy read access with a LOW pulse on pins CS_N/CE_N and RD_N /RE_N/OE_N.
2. USB device connects or disconnects.
3. Remote wake up from external USB device.
4. Over current condition is triggered on OC_N if enabled by register.

After wake up automatically set corresponding bit of the CONFIG register, must set the U_SUSP_U bit of the EOTTIME register to wake up the chip.

4.10 BCD mode

The FT313H is an EHCI-compatible host controller with BCD block function, which follows the Battery Charging Specification Revision 1.2(BC1.2) by USB-IF. The block function that emulates USB host port as either Charging Downstream Port (CDP) or Dedicated Charging Port (DCP) which provides higher current source than Standard Downstream Port (SDP).

The BCD logic block will decode the mode of operation and choose by following setting:

1. BCD function is default enable by CONFIG register bit[5] setting.
2. BCD mode selection is default controlled by external pins configuration. Set CONFIG register bit[15] to take over BCD mode setting by software.
3. Same configuration by CONFIG register bit[14:13] to set BCD mode if software takes over control.

CPE1	CPE0	Mode	BCD_EN	Description
0	0	SDP	1	Standard downstream port, VBUS current limit ≤ 500mA
0	1	DCP	1	Dedicated charging port, USB host no functional on this port, VBUS current limit ≤ 1.5A
1	1	CDP	1	Charging downstream port alternative configuration, VBUS current limit ≤ 1.5A
X	X	X	0	BCD function disable

Table 4-6 BCD mode configuration

5 Host controller specific registers

5.1 Overview of registers

Table 5.1 shows the definitions of the FT313H host controller specific registers.

Address	Register	Reset value	Description
EHCI operational register			
00h	HCCAPLENGTH	0100 0010h	Capability register
04h	HCSPARAMS	0000 0001h	Structural parameter register
08h	HCCPARAMS	0000 0006h	Capability parameter register
10h	USBCMD	0008 0B00h	USB command register
14h	USBSTS	0000 1000h	USB status register
18h	USBINTR	0000 0000h	USB interrupt enable register
1Ch	FRINDEX	0000 0000h	Frame index register
24h	PERIODICLISTADDR	0000 0000h	Periodic frame list base address register
28h	ASYNCLISTADDR	0000 0000h	Current asynchronous list address register
30h	POSTSC	0000 0000h	Port status and control register
Configuration register			
34h	EOFTIME	0000 0041h	EOF time and asynchronous schedule sleep timer register
80h	CHIPID	0313 0001h	Chip ID register
84h	HWMODE	0000 0000h	HW mode control register
88h	EDGEINTC	0000 001Fh	Edge interrupt control register
8Ch	SWRESET	0000 0000h	SW reset register
90h	MEMADDR	0000h	Memory address register
92h	DATAPORT	0000h	Data port register
94h	DATASESSION	0000h	Data session length register
96h	CONFIG	1FA0h	Configuration register
98h	AUX_MEMADDR	0000h	Auxiliary memory address register
9Ah	AUX_DATAPORT	0000h	Auxiliary data port register
9Ch	SLEEPTIMER	0400h	Sleep timer register
Interrupt register			
A0h	HCINTSTS	0000h	Host controller interrupt status register

Address	Register	Reset value	Description
A4h	HCINTEN	0000h	Host controller interrupt enable register
USB testing register			
50h	TESTMODE	0000 0000h	Test mode register
70h	TESTPMSET1	0000 0000h	Test parameter setting 1 register
74h	TESTPMSET2	0000 0000h	Test parameter setting 2 register

Table 5-1 Overview of host controller specific registers

5.2 EHCI operational registers

5.2.1 HCCAPLENGTH register (address = 00h)

This register is used as an offset to add to register base to find the beginning of the operational register space. The high two bytes contain a BCD encoding of the EHCI revision number supported by this host controller. The most signification byte of this register represents a major revision and the least signification byte is the minor revision.

Bit	Name	Type	Default value	Description
[31:16]	HCIVERSION	RO	16'h0100	**Host Controller Interface Version Number** This register is a 2-byte register containing a BCD encoding of the EHCI revision number supported by the host controller.
[15:8]	Reserved	RO	8'h0	-
[7:0]	CAPLENGTH	RO	8'h10	**Capability Register Length** This register is used as an offset added to register base to find out the beginning of the Operational Register Space.

Table 5-2 Capability register

5.2.2 HCSPARAMS register (address = 04h)

This is a set of fields that are structural parameter: number of downstream ports, etc.

Bit	Name	Type	Default value	Description
[31:4]	Reserved	RO	28'h0	-
[3:0]	N_PORTS	RO	4'h1	**Number of Ports** This field specifies the number of the physical downstream ports implemented on the host controller.

Table 5-3 Structural parameter register

5.2.3 HCCPARAMS register (address = 08h)

This is multiple mode control (time base bit functionality) and addressing capability.

Bit	Name	Type	Default value	Description
[31:3]	Reserved	RO	29'h0	-
2	ASPC	RO	1'b1	**Asynchronous Schedule Park Capability** The host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. This feature can be disabled or enabled and set to a specific level by using the *Asynchronous Schedule Park Mode Enable* and *Asynchronous Schedule Park Mode Count* fields in the USBCMD register.
1	PFLF	RO	1'b1	**Programmable Frame List Flag** When this bit is set to 1b, the system software can specify and use a smaller frame list and configure the host controller via *Frame List Size* field of the USBCMD register. This requirement ensures that the frame list is always physically contiguous.
0	Reserved	RO	1'b0	-

Table 5-4 Capability parameter register

5.2.4 USBCMD register (address = 10h)

The command register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed.

Bit	Name	Type	Default value	Description
[31:24]	Reserved	RO	8'h0	-
[23:16]	INT_THRC	R/W	8'h08	**Interrupt Threshold Control** This field is used by the system software to select the maximum rate at which the host controller will issue the interrupts. The only valid values are described as below: Value Max Interrupt Interval for the high-speed 00h Reserved 01h No limited interval 02h 2 micro-frames 04h 4 micro-frames 08h 8 micro-frames (Default, equals to 1 ms) 10h 16 micro-frames (2 ms) 20h 32 micro-frames (4 ms) 40h 64 micro-frames (8 ms)

Bit	Name	Type	Default value	Description
				Note1: This is further gated by MIN_WIDTH bits of EDGEINTC register if edge trigger interrupt is used. Note2: In the full-speed mode, these registers are reserved.
[15:12]	Reserved	RO	4'b0	-
11	ASYN_PK_EN	R/W	1'b1	**Asynchronous Schedule Park Mode Enable** Software uses this register to enable or disable the Park mode. When this register is set to '1', the Park mode is enabled.
10	Reserved	RO	1'b0	-
[9:8]	ASYN_PK_CNT	R/W	2'b11	**Asynchronous Schedule Park Mode Count** This field contains a count for the number of successive transactions that the host controller is allowed to execute from a high-speed queue head on the asynchronous schedule.
7	Reserved	RO	1'b0	-
6	INT_OAAD	R/W	1'b0	**Interrupt on Asynchronous Advance Doorbell** This bit is used as a doorbell by software to ring the host controller to issue an interrupt at the next advance of the asynchronous schedule.
5	ASCH_EN	R/W	1'b0	**Asynchronous Schedule Enable** This bit controls whether the host controller skips the processing of asynchronous schedule. 0: Do not process the asynchronous schedule 1: Use the ASYNCLISTADDR register to access the asynchronous schedule
4	PSCH_EN	R/W	1'b0	**Periodic Schedule Enable** This bit controls whether the host controller skips the processing of the periodic schedule. 0: Do not process the periodic schedule 1: Use the PERIODICKISTBASE register to access the periodic schedule
[3:2]	FRL_SIZE	R/W	2'b00	**Frame List Size** This field specifies the size of the frame list. 00: 1024 elements (4096 bytes; default value) 01: 512 elements (2048 bytes) 10: 256 elements (1024 bytes) 11: Reserved
1	HC_RESET	R/W	1'b0	**Host Controller Reset** This control bit is used by the software to reset the host controller.

Bit	Name	Type	Default value	Description
0	RS	R/W	1'b0	**Run/Stop** When this bit is set to 1b, the host controller proceeds with the execution of schedule. 0: Stop 1: Run

Table 5-5 USB command register

5.2.5 USBSTS register (address = 14h)

This register indicates pending interrupts and various states of the Host Controller. The status resulting from a transaction on the serial bus is not indicated in this register. Software sets a bit to 0 in this register by writing a 1 to it.

Bit	Name	Type	Default value	Description
[31:16]	Reserved	RO	16'h0	-
15	ASCH_STS	RO	1'b0	**Asynchronous Schedule Status** This bit reports the actual status of the asynchronous schedule.
14	PSCH_STS	RO	1'b0	**Periodic Schedule Status** This bit reports the actual status of the periodic schedule.
13	Reclamation	RO	1'b0	**Reclamation** This is a read-only status bit, and used to detect an empty of the asynchronous schedule.
12	HCHalted	RO	1'b1	**Host Controller Halted** This bit is a zero whenever the Run/Stop bit is set to '1.' The host controller sets this bit to '1' after it has stopped the executing as a result of the Run/Stop bit being set to 0b.
[11:6]	Reserved	RO	6'b0	-
5	INT_OAA	R/WC	1'b0	**Interrupt on Asynchronous Advance** This status bit indicates the assertion of *interrupt on Async Advance Doorbell*.
4	H_SYSERR	R/WC	1'b0	**Host System Error** The Host Controller sets this bit to '1' when a serious error occurred during a host system access involving the host controller module.
3	FRL_ROL	R/WC	1'b0	**Frame List Rollover** The host controller sets this bit to '1' when the *Frame List Index* rolls over from its maximum value to zero.
2	PO_CHG_DET	R/WC	1'b0	**Port Change Detect** The host controller sets this bit to '1' when any port has a change bit transition from '0' to '1.' In addition, this bit is loaded with the OR of all of

Bit	Name	Type	Default value	Description
				the PORTSC change bits.
1	USBERR_INT	R/WC	1'b0	**USB Error Interrupt** The host controller sets this bit to '1' when the completion of a USB transaction results in an error condition.
0	USB_INT	R/WC	1'b0	**USB Interrupt** The host controller sets this bit to '1' upon the completion of a USB transaction.

Table 5-6 USB status register

5.2.6 USBINTR register (address = 18h)

This register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Interrupt sources that are disabled in this register still appear in the USBSTS to allow the software to poll for events.

Bit	Name	Type	Default value	Description
[31:6]	Reserved	RO	26'h0	-
5	INT_OAA_EN	R/W	1'b0	**Interrupt on Async Advance Enable** When this bit is set to '1,' and the *Interrupt on Async Advance* bit in the USBSTS register is set to '1' also, the host controller will issue an interrupt at the next interrupt threshold.
4	H_SYSERR_EN	R/W	1'b0	**Host System Error Enable** When this bit is set to '1,' and the *Host System Error Status* bit in the USBSTS register is set to '1' also, the host controller will issue an interrupt.
3	FRL_ROL_EN	R/W	1'b0	**Frame List Rollover Enable** When this bit is set to '1,' and the *Frame List Rollover* bit in the USBSTS register is set to '1' also, the host controller will issue an interrupt.
2	PO_CHG_DET_EN	R/W	1'b0	**Port Change Interrupt Enable** When this bit is set to '1,' and the *Port Change Detect* bit in the USBSTS register is set to '1' also, the host controller will issue an interrupt.
1	USBERR_INT_EN	R/W	1'b0	**USB Error Interrupt Enable** When this bit is set to '1,' and the USBERRINT bit in the USBSTS register is set to '1' also, the host controller will issue an interrupt at the next interrupt threshold.
0	USB_INT_EN	R/W	1'b0	**USB Interrupt Enable** When this bit is set to '1,' and the USBINT bit in the USBSTS register is a set to '1' also, the host controller will issue an interrupt at the next interrupt threshold. If set interrupt threshold to 01h, means that when interrupt event occurred, the INT signal will be toggled at once.

Table 5-7 USB interrupt enable register

5.2.7 FRINDEX register (address = 1Ch)

This register is used by the host controller to index into the periodic frame. The register updates very 125 microseconds (one each micro-frame).

Bit	Name	Type	Default value	Description
[31:14]	Reserved	RO	28'h0	-
[13:0]	FRINDEX	R/W	14'b0	**Frame Index** This register is used by the host controller to index the frame into the Periodic Frame List. It updates every 125 microseconds. This register cannot be written unless the host controller is at the halted state. Bits[N:3] are used for Frame List current index. This means that each location of the frame list is accessed 8 times before moving to the next index. USBCMD[Frame List Size] Number Elements N 00b (1024) 12 01b (512) 11 10b (256) 10 11b Reserved

Table 5-8 Frame index register

5.2.8 PERIODICLISTADDR register (address = 24h)

This 32-bit register contains the beginning address of the periodic frame list in the system memory.

Bit	Name	Type	Default value	Description
[31:12]	PERI_BASEADR	R/W	20'h0	**Periodic Frame List Base Address** This 32-bit register contains the beginning address of the Periodic Frame List in the system memory. These bits correspond to the memory address signals[31:12].
[11:0]	Reserved	RO	12'b0	-

Table 5-9 Periodic frame list base address register

5.2.9 ASYNCLISTADDR register (address = 28h)

This 32-bit register contains the address of the next asynchronous queue head to be executed.

Bit	Name	Type	Default value	Description
[31:5]	ASYNC_LADR	R/W	27'h0	**Current Asynchronous List Address** This 32-bit register contains the address of the next asynchronous queue head to be executed. These bits correspond to the memory address signals [31:5].
[4:0]	Reserved	RO	5'b0	-

Table 5-10 Current asynchronous list address register

5.2.10 POSTSC register (address = 30h)

The port status and control register is in the power well. It is only reset by hardware when the power is initially applied or in response to a host controller reset. The initial conditions of a port are:

- No peripheral connected
- Port disable

The software must not attempt to change the state of the port until the power is stable on the port. The host is required to have power stable to the port within 20 milliseconds of the zero to one transition.

When a peripheral device is attached, the port state transitions to the connected state and system software will process this as with any status change notification.

Bit	Name	Type	Default value	Description
[31:17]	Reserved	RO	15'h0	-
16	TST_FORCEEN	R/W	1'b0	**Test Force Enable** When this signal is written as '1,' the downstream facing port will be enabled in the high-speed mode. Then the Run/Stop bit must be transitioned to one in order to enable the transmission of the SOFs out of the port under test. This enables testing of the disconnect detection.
[15:12]	Reserved	RO	4'b0	-
[11:10]	LINE_STS	RO	2'b00	**Line Status** These bits reflect the current logical levels of the D+ and D- signal lines. Bits[11:10] USB state 00b SE0 10b J-state 01b K-state 11b Undefined
9	Reserved	RO	1'b0	-
8	PO_RESET	R/W	1'b0	**Port Reset** 1 = Port is in the reset state. 0 = Port is not in the reset state. When the software writes a '1' to this bit, the bus reset sequence as defined in the USB specification will start. Software writes a '0' to this bit to terminate the bus reset sequence. Software must keep this bit at a '1' long enough to ensure the reset sequence. Note: Reset signal which shall be followed by the USB2.0 chapter 7.1.7.5 Reset Signal requirement. If detected HS device, the software shall wait more than 200us for port reset clearing. Before setting this bit, RUN/STOP bit should be set to '0.'
7	PO_SUSP	R/W	1'b0	**Port Suspend** 1 = Port is in the suspend state 0 = Port is not in the suspend state.

Bit	Name	Type	Default value	Description
				The Port Enable Bit and Suspend Bit of this register define the port state as follows: Bits[Port Enable, Suspend] Port State 0X Disable 10 Enable 11 Suspend At the suspend state, the downstream propagation of the data is blocked on this port, except for the port reset. While at the suspend state, the port is sensitive to resume detection. Writing a '0' to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a '0' when: The software sets Force Port Resume bit to a '0' (From a one) The software sets Port Reset bit to a '1' (From a '0') Note: Before setting this bit, RUN/STOP bit should be set to 0.
6	F_PO_RESM	R/W	1'b0	**Force Port Resume** 1 = Resume detected/driven on port. 0 = No resume detected/driven on port. Software sets this bit to a '1' to resume signal. The host controller sets this bit to a '1' if a J-to-K transition is detected while the port is in the suspend state. When this bit transits to a '1' for the detection of a J-to-K transition, the Port Change Detect bit in USBSTS register is also set to a '1'.
[5:4]	Reserved	RO	2'b00	-
3	PO_EN_CHG	R/WC	1'b0	**Port Enable/Disable Change** 1 = Port enable/disable status has changed. 0 = No change
2	PO_EN	R/W	1'b0	**Port Enable/Disable** 1 = Enable 0 = Disable Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field.
1	CONN_CHG	R/WC	1'b0	**Connect Status Change** 1 = Change current connect status 0 = No change. This bit indicates a change has occurred in the current connect status of the port.
0	CONN_STS	RO	1'b0	**Current Connect Status** 1 = Device is presented on the port. 0 = No device is presented.

Bit	Name	Type	Default value	Description
				This value reflects the current state of the port, and may not correspond directly to cause the Connect Status Change bit to be set.

Table 5-11 Port status and control register

5.3 Configuration registers

5.3.1 EOTTIME register (address = 34h)

Bit	Name	Type	Default value	Description
[31:7]	Reserved	RO	25'h0	-
6	U_SUSP_N	R/W	1'b1	**Transceiver Suspend Mode** Active low Places the transceiver in the suspend mode that draws the minimal power from the power supplies. This is part of the power management.
[5:4]	EOF2_TIME	R/W	2'b00	**EOF 2 Timing Points** Control EOF2 timing point before next SOF. High-Speed EOF2 Time 00b 2 clocks (30 MHz) = 66 ns 01b 4 clocks (30 MHz) = 133 ns 10b 8 clocks (30 MHz) = 266 ns 11b 16 clocks (30 MHz) = 533 ns Full-Speed EOF2 Time 00b 20 clocks (30 MHz)=8 clocks (12 MHz) = 666 ns 01b 40 clocks (30 MHz)=16 clocks (12 MHz) = 1.333 µs 10b 80 clocks (30 MHz) = 32 clocks (12 MHz) = 2.66 µs 11b 160 clocks (30 MHz) = 64 clocks (12 MHz) = 5.3 µs Low-Speed EOF2 Time 00b 40 clocks (30 MHz) = 16 clocks (12 MHz) = 1.33 µs 01b 80 clocks (30 MHz) = 32 clocks (12 MHz) = 2.66 µs 10b 160 clocks (30 MHz) = 64 clocks (12 MHz) = 5.33 µs 11b 320 clocks (30 MHz) = 128 clocks (12 MHz) = 10.66 µs
[3:2]	EOF1_TIME	R/W	2'b00	**EOF 1 Timing Points** Controls the EOF1 timing point before next SOF. This value should be adjusted according to the maximum packet size. High-Speed EOF1 Time 00b 540 clocks (30 MHz) = 18 µs 01b 360 clocks (30 MHz) = 12 µs 10b 180 clocks (30 MHz) = 6 µs 11b 720 clocks (30 MHz) = 24 µs Full-Speed EOF1 Time 00b 1600 clocks (30 MHz) = 640 clocks (12 MHz) = 53.3 µs 01b 1400 clocks (30 MHz) = 560 clocks (12 MHz) = 46.6 µs 10b 1200 clocks (30 MHz) = 480 clocks (12 MHz) = 40 µs 11b 21000 clocks (30 MHz) = 8400 clocks (12 MHz)=700 µs Low-Speed EOF1 Time

Bit	Name	Type	Default value	Description
				00b 3750 clocks (30 MHz) = 1500 clocks (12 MHz) = 125 µs 01b 3500 clocks (30 MHz) = 1400 clocks (12 MHz) = 116 µs 10b 3250 clocks (30 MHz) = 1300 clocks (12 MHz) = 108 µs 11b 4000 clocks (30 MHz) = 1600 clocks (12 MHz) = 133 µs
[1:0]	ASYN_SCH_SLPT	R/W	2'b01	**Asynchronous Schedule Sleep Timer** Controls the Asynchronous Schedule sleep timer. 00b 5 µs 01b 10 µs 10b 15 µs 11b 20 µs

Table 5-12 EOF time and asynchronous schedule sleep timer register

5.3.2 CHIPID register (address = 80h)

This chip ID register contains the chip identification and hardware version numbers.

Bit	Name	Type	Default value	Description
[31:0]	CHIP_ID	RO	32'h03130001	**Chip ID**

Table **5-13 Chip ID register**

5.3.3 HWMODE register (address = 84h)

Bit	Name	Type	Default value	Description
[15: 8]	Reserved	RO	8'b0	-
[7: 6]	HOST_SPD_TYP	RO	2'b00	**Host Speed Type** Indicate the speed type of attached device 2'b10: HS 2'b00: FS 2'b01: LS 2'b11: Reserved
5	DACK_POL	R/W	1'b0	**DACK Polarity** 0: active LOW 1: active HIGH
4	DREQ_POL	R/W	1'b0	**DREQ Polarity** 0: active LOW 1: active HIGH
3	INTF_LOCK	R/W	1'b0	**Interface Lock** 0: Unlock the bus interface 1: Lock the bus interface

Bit	Name	Type	Default value	Description
2	INTR_POL	R/W	1'b0	**Interrupt Polarity** 0: active LOW 1: active HIGH
1	INTR_LEVEL	R/W	1'b0	**Interrupt Level** 0: level trigger 1: Edge trigged. The pulse width depends on the NO_OF_CLK bits in the EDGEINTC register.
0	GLOBAL_INTR_EN	R/W	1'b0	**Globe interrupt enable** 0: INT assertion disabled. INT will never be asserted, regardless of other settings or INT events. 1: INT assertion enabled. INT will be asserted according to the HCINTEN register, and event setting and occurrence.

Table 5-14 HW mode register

5.3.4 EDGEINTC register (address = 88h)

Bit	Name	Type	Default value	Description
[31:24]	MIN_WIDTH	R/W	8'b0	**Minimum Interval** Indicates the minimum interval between two edge interrupts in uSOFs (1 uSOF = 125us). This is not valid for level interrupts. A count of zero means that an interrupt occurs as when an event occurs.
[23:16]	Reserved	RO	8'b0	-
[15: 0]	NO_OF_CLK	R/W	16'b1F	**Number of clocks** Number of clocks that an Edge Interrupt must be kept asserted on the interface. The default INT pulse width is approximately 500ns. (N+1)*60MHz system clock.

Table 5-15 Edge interrupt control register

5.3.5 SWRESET register (address = 8Ch)

Bit	Name	Type	Default value	Description
[15: 8]	Reserved	RO	8'b0	-
[7: 6]	INTF_MODE	RO	2'b00	**Interface mode** 00b: Reserved 01b: Generic Multiplex mode

Bit	Name	Type	Default value	Description
				10b: NOR mode 11b: SRAM mode Write to these bits have no effect.
5	Reserved	RO	1'b0	-
4	DATA_BUS_WIDTH	R/W	1'b0	**Data bus width** 0: Defines a 16-bit data bus width. 1: Sets a 8-bit data bus width.
3	Reserved	RO	1'b0	-
2	RESET_ATX	R/W	1'b0	**Reset USB transceiver** 0: No reset 1: Enable reset When the software writes a '1' to this bit, the USB PHY reset sequence will start. Automatic clear zero.
1	RESET_HC	R/W	1'b0	**Reset host controller** 0: No reset 1: Enable reset When the software writes a '1' to this bit, the Host Controller reset sequence will start. Automatic clear zero.
0	RESET_ALL	R/W	1'b0	**Reset all system** 0: No reset 1: Enable reset When the software writes a '1' to this bit, the whole system reset sequence will start. Automatic clear zero.

Table 5-16 SW reset register

5.3.6 MEMADDR register (address = 90h)

Bit	Name	Type	Default value	Description
[15: 0]	START_ADDR_MEM	R/W	16'b0	**Start address for memory read / write** Internal 24K RAM memory address from 0x0000 to 0x5FFF. Used by PIO and DMA.

Table 5-17 Memory address register

5.3.7 DATAPORT register (address = 92h)

Bit	Name	Type	Default value	Description
[15: 0]	DATA_PORT	R/W	16'b0	**Data port** Read / write data from / to memory must go through this port. Used by PIO and DMA.

Table 5-18 Data port register

5.3.8 DATASESSION register (address = 94h)

Bit	Name	Type	Default value	Description
15	MEM_RW	R/W	1'b0	**Memory read or write** 0: Write data into memory 1: Read data from memory Used by PIO and DMA
[14: 0]	DATA_LEN	R/W	15'b0	**Data length for memory read or write** Preset the data length for memory read/write. The max data length is 24K. Used by PIO and DMA

Table 5-19 Data session length register

5.3.9 CONFIG register (address = 96h)

Bit	Name	Type	Default value	Description
15	BCD_MODE_CTRL	R/W	1'b0	**BCD Mode override control** 0: External CPE0 and CPE1 pins configuration take effect. 1: BCD_MODE [1:0] register bits take effect
[14:13]	BCD_MODE[1:0]	R/W	2'b00	**BCD Mode setting** 00: SDP Standard downstream port, VBUS current limit ≥ 500mA. 01: DCP

Bit	Name	Type	Default value	Description
				Dedicated charging port. USB host not functional on this port, VBUS current limit ≤ 1.5A. 10: Reserved 11: CDP Charging downstream port, VBUS current limit ≤ 1.5A.
12	Reserved	-	1'b1	-
11	OSC_EN	R/W	1'b1	**Oscillator enable** 0: Oscillator is not active 1: Oscillator is active
10	PLL_EN	R/W	1'b1	**Internal PLL enable** 0: PLL is disable 1: PLL is enable
9	Reserved	-	1'b1	**-**
8	HC_CLK_EN	R/W	1'b1	**Host controller clock enable** 0: clocks are disabled 1: clocks are enabled
7	VBUS_OFF	R/W	1'b1	**VBUS power switch** This bit controls the voltage on the VBUS on/off (default is "1") by switch external power switcher. 0: VBUS on, PSW_N signal is active LOW. 1: VBUS off, PSW_N signal is not active.
6	PORT_OC_EN	R/W	1'b0	**Port overcurrent enable** 0: disable over current detection 1: enable over current detection
5	BCD_EN	R/W	1'b1	**BCD module enable** 0: disable BCD module 1: enable BCD module
4	Reserved	RO	1'b0	**-**
[3: 2]	BURST_LEN	R/W	2'b00	**DMA burst length** 00: Single DMA burst 01: 4-cycle DMA burst 10: 8-cycle DMA burst 11: 16-cycle DMA burst
1	ENABLE_DMA	R/W	1'b0	**Enable DMA** 0: terminate DMA

Bit	Name	Type	Default value	Description
				1: enable DMA
0	DMA_ABORT	R/W	1'b0	**DMA abort** 0: DMA continuous running 1: DMA abort implement

Table 5-20 DMA configuration register

5.3.10 AUX_MEMADDR register (address = 98h)

Bit	Name	Type	Default value	Description
[15: 0]	AUX_START_ADDR_MEM	R/W	16'b0	**Auxiliary start address of memory read / write** When memory is occurred by DMA, use auxiliary start address for PIO memory access.

Table 5-21 AUX Memory address register

5.3.11 AUX_DATAPORT register (address = 9Ah)

Bit	Name	Type	Default value	Description
[15: 0]	AUX_DATA_PORT	R/W	16'b0	**Auxiliary data port** When memory is occurred by DMA, use auxiliary data port for PIO memory access.

Table 5-22 AUX data port register

5.3.12 SLEEPTIMER register (address = 9Ch)

Bit	Name	Type	Default value	Description
[15: 0]	SLEEP_TIMER	R/W	16'b0400	**Sleep timer** When host controller detected USB bus has no activity, the sleep timer will be started. When timer reduce to zero, the BUSINACTIVE interrupt will be generated, if the respective enable bit in the HCINTEN register is set. Default sleep timer is approximately 10ms.

Table 5-23 Sleep timer register

5.4 Interrupt registers

5.4.1 HCINTSTS register (address = A0h)

Bit	Name	Type	Default value	Description
[15: 8]	Reserved	RO	10'b0	-
7	WAKEUPINT	R/WC	1'b0	**Wake up interrupt on device connect or**

Bit	Name	Type	Default value	Description
				disconnect Indicates that wake up event is triggered. The INT line will be asserted if the respective enable bit in the HCINTEN register is set. 0: No wake up event has occurred on the port when device connects or disconnects. 1: Wake up event has occurred on the port when device connects or disconnects.
6	OCINT	R/WC	1'b0	**Overcurrent interrupt** Indicates that overcurrent event is triggered. The INT line will be asserted if the respective enable bit in the HCINTEN register is set. 0: No overcurrent event has occurred. 1: Overcurrent event has occurred.
5	CLKREADY	R/WC	1'b0	Clock ready Indicates that internal clock signals are running stable. The INT line will be asserted if the respective enable bit in the HCINTEN register is set. 0: No clock ready event has occurred. 1: Clock ready event has occurred.
4	BUSINACTIVE	R/WC	1'b0	**USB Bus inactive interrupt** Indicates that USB bus is inactive. The INT line will be asserted if the respective enable bit in the HCINTEN register is set. 0: USB bus is active. 1: USB bus is inactive.
3	REMOTEWKINT	R/WC	1'b0	**Remote Wake up interrupt** Indicates INT was generated when the host controller remote wakeup. The INT line will be asserted if the respective enable bit in the HCINTEN register is set. 0: No remote wake up. 1: Remote wake up event occurred.
2	DMAEOTINT	R/WC	1'b0	**DMA EOT interrupt** Indicates the DMA transfer completion. The INT line will be asserted if the respective enable bit in the HCINTEN register is set. 0: No DMA transfer is completed. 1: DMA transfer is completed.
1	SOFINT	R/WC	1'b0	**SOF interrupt** The INT line will be asserted if the respective bit enable is set.

Bit	Name	Type	Default value	Description
				0: No SOF event has occurred. 1: SOF event has occurred.
0	MSOFINT	R/WC	1'b0	**uSOF interrupt** The INT line will be asserted if the respective enable bit in the HCINTEN register is set. 0: No uSOF event has occurred. 1: uSOF event has occurred.

Table 5-24 HC interrupt status register

5.4.2 HCINTEN register (address = A4h)

Bit	Name	Type	Default value	Description
[15: 8]	Reserved	RO	10'b0	-
7	WAKEUPINT_EN	R/W	1'b0	**Wake up interrupt enable on device connect or disconnect** Control the INT generation when the device connects or disconnects as wake up events. 0: No INT will be generated when device connects or disconnects as wake up events. 1: INT will be asserted when device connects or disconnects as wake up events.
6	OCINT_EN	R/W	1'b0	**Overcurrent interrupt enable** Control the INT generation when the overcurrent event triggers 0: No INT will be generated after overcurrent event is triggered. 1: INT will be asserted after overcurrent event is triggered.
5	CLKREADY_EN	R/W	1'b0	**Clock ready enable** Control the INT generation when the internal clock signals are running stable 0: No INT will be generated after clock runs stable. 1: INT will be asserted after clock runs stable.
4	BUSINACTIVE_EN	R/W	1'b0	**USB Bus inactive enable** Control the INT generation when the USB bus is inactive 0: No INT will be generated when the USB bus is inactive. 1: INT will be asserted when the USB bus is inactive.
3		R/W	1'b0	**Remote wake up interrupt enable**

Bit	Name	Type	Default value	Description
	REMOTEWKINT_EN			Control the INT generation when the host controller supports remote wake up 0: No INT will be generated when remote wake up occurred. 1: INT will be asserted when remote wake up occurred.
2	DMAEOTINT_EN	R/W	1'b0	**DMA EOT interrupt enable** Control assertion of INT on the DMA transfer completion 0: No INT will be generated when a DMA transfer is completed. 1: INT will be asserted when a DMA transfer is completed.
1	SOFINT_EN	R/W	1'b0	**SOF interrupt enable** Control the INT generation at every SOF occurrence 0: No INT will be generated on SOF. 1: INT will be asserted at every SOF.
0	MSOFINT_EN	R/W	1'b0	**uSOF interrupt enable** Control the INT generation at every uSOF occurrence 0: No INT will be generated on uSOF. 1: INT will be asserted at every uSOF.

Table 5-25 HC interrupt status register

5.5 USB testing registers

5.5.1 TESTMODE register (address = 50h)

This register allows the firmware to set the DP and DM pins to predetermined states for testing purposes.

Once force one test mode on host, must use test device on port connection.

Note: Only one bit can be set to logic 1 at a time. After writing to this register, need add 150ns delay before writing this register again. The registers 70h and 74h both have same operation.

Bit	Name	Type	Default value	Description
[31:5]	Reserved	RO	27'b0	-
4	TST_LOOPBK	R/W	1'b0	Turn on the loop back mode. When this bit is set to '1', the host controller will enter the loop back mode.
3	Reserved	RO	1'b0	-
2	TST_PKT	R/W	1'b0	**TEST_PACKET** After entering the high speed and writing 1'b1 to this bit, users should command the DMA by the test parameter setting registers (0x70h and 0x74h) to move the packet data defined

Bit	Name	Type	Default value	Description
				in the USB2.0 specification from the memory to FIFO. Then, send the packet to the transceiver.
1	TST_KSTA	R/W	1'b0	**TEST_K** Upon writing a '1,' the D+/D- are set to the high-speed K state.
0	TST_JSTA	R/W	1'b0	**TEST_J** Upon writing a '1,' the D+/D- are set to the high-speed J state.

Table 5-26 Test mode register

5.5.2 TESTPMSET1 register (address = 70h)

This parameter setting register is only used by test packet mode.

Bit	Name	Type	Default value	Description
[31:25]	Reserved	RO	7'b0	-
[24: 8]	DMA_LEN	R/W	11'h000	**DMA Length** The total bytes of the DMA controller will move. The maximum length is 1024 – 1 Bytes.
[7: 2]	Reserved	RO	6'b0	-
1	DMA_TYPE	R/W	1'b0	**DMA Type** The transfer type of data moving 0: FIFO to Memory 1: Memory to FIFO
0	DMA_START	R/W	1'b0	**DMA Start** This bit informs the DMA controller to initiate the DMA transfer.

Table 5-27 Test mode parameter setting 1 register

5.5.3 TESTPMSET2 register (address = 74h)

This parameter setting register is only used by test packet mode.

Bit	Name	Type	Default value	Description
[31:0]	DMA_MADDR	R/W	32'b0	DMA Memory Address The starting address of memory to request the DMA transfer.

Table 5-28 Test parameter setting 2 register

6 Devices Characteristics and Ratings

6.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT313H device are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Temperature (Power Applied)	-40°C to 85°C	Degrees C
VCC Supply Voltage	0 to +5	V
VCC(I/O) Supply Voltage	0 to +5	V
DC Input Voltage – USBDP and USBDM	-0.5 to +5	V
DC Input Voltage – OC_N (5V tolerant)	-0.5 to +5.5	V
DC Input Voltage – All Other Inputs	-0.5 to +5	V

Table 6-1 Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

6.2 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC(I/O)	VCCIO operating supply voltage	1.62	1.8	1.98	V	Normal Operation
		2.25	2.5	2.75	V	
		2.97	3.3	3.63	V	
VCC(3V3)	VCC operating supply voltage	2.97	3.3	3.63	V	Normal Operation
Icc1	Idle current	-	20	-	mA	Idle
Icc2	Operating current	-	35	-	mA	Normal Operation High speed data transfer
Icc3	USB suspend	-	200	-	uA	USB suspend
VCC(1V2)	Core supply voltage	1.08	1.2	1.32	V	Normal Operation
VOUT(1V2)	Internal 1.2V regulator voltage	-	1.2	-	V	Normal Operation

Table 6-2 Operating Voltage and Current

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.4	3.3	-	V	Ioh=8mA
Vol	Output Voltage Low	-	-	0.4	V	Iol=8mA
Vih	Input High Voltage	2.0	-	-	V	-
Vil	Input Low Voltage	-	-	0.8	V	-
Vth	Schmitt Hysteresis Voltage	0.3	0.45	0.5	V	-
Ipu	Input pull-up current	25	42	60	uA	Vin = 0V
Rpu	Input pull-up resistance equivalent	120K	78K	60K	ohm	Vin = 0V
Ipd	Input pull-down current	25	42	60	uA	Vin = VCC(I/O)
Rpd	Input pull-down resistance equivalent	120K	78K	60K	ohm	Vin = VCC(I/O)
Iin	Input leakage current	-10	±1	10	uA	Vin = VCC(I/O) or 0
Ioz	Tri-state output leakage current	-10	±1	10	uA	-

Table 6-3 Digital I/O Pin Characteristics (VCC(I/O) = +3.3V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	VCC(I/O) -0.4	2.5	-	V	Ioh=6mA
Vol	Output Voltage Low	-	-	0.4	V	Iol=6mA
Vih	Input High Voltage	0.7VCC(I/O)	-	-	V	-
Vil	Input Low Voltage	-	-	0.3VCC(I/O)	V	-
Vth	Schmitt Hysteresis Voltage	0.28	0.39	0.5	V	-
Ipu	Input pull-up current	14	23	35	uA	Vin = 0
Rpu	Input pull-up resistance equivalent	160K	108K	78K	ohm	Vin = 0
Ipd	Input pull-down current	14	23	35	uA	Vin = VCC(I/O)
Rpd	Input pull-down resistance equivalent	160K	108K	78K	ohm	Vin = VCC(I/O)
Iin	Input leakage current	-10	±1	10	uA	Vin = VCC(I/O) or 0
Ioz	Tri-state output leakage current	-10	±1	10	uA	-

Table 6-4 Digital I/O Pin Characteristics (VCC(I/O) = +2.5V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	VCC(I/O) -0.4	1.8	-	V	Ioh=3.6mA
Vol	Output Voltage Low	-	-	0.4	V	Iol=3.6mA
Vih	Input High Voltage	0.7VCC(I/O)	-	-	V	-
Vil	Input Low Voltage	-	-	0.3VCC(I/O)	V	-
Vth	Schmitt Hysteresis Voltage	0.25	0.35	0.5	V	-
Ipu	Input pull-up current	6	10	15	uA	Vin = 0
Rpu	Input pull-up resistance equivalent	270K	180K	130K	ohm	Vin = 0
Ipd	Input pull-down current	6	10	15	uA	Vin = VCC(I/O)
Rpd	Input pull-down resistance equivalent	270K	180K	130K	ohm	Vin = VCC(I/O)
Iin	Input leakage current	-10	±1	10	uA	Vin = VCC(I/O) or 0
Ioz	Tri-state output leakage current	-10	±1	10	uA	-

Table 6-5 Digital I/O Pin Characteristics (VCC(I/O) = +1.8V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Input level for high speed						
Vhscm	Voltage of high speed data signal in the common mode	-50	-	500	mV	-
Vhssq	High speed squelch detection threshold	-	-	100	mV	Squelch is detected
		150	-	-	mV	Squelch is not detected
Vhsdsc	High speed disconnection detection threshold	625	-	-	mV	Disconnection is detected
		-	-	525	mV	Disconnection is not detected
Output level for high speed						
Vhsoi	High speed idle output voltage (Differential)	-10	-	10	mV	-
Vhsol	High speed low level output voltage (Differential)	-10	-	10	mV	-
Vhsoh	High speed high level output voltage (Differential)	-360	-	400	mV	-
Vchirpj	Chirp-J output voltage (Differential)	700	-	1100	mV	-
Vchirpk	Chirp-K output voltage (Differential)	-900	-	-500	mV	-
Input level for full speed and low speed						
Vdi	Differential input voltage sensitivity	0.2	-	-	V	|Vdp-Vdm|
Vcm	Differential common mode voltage	0.8	-	2.5	V	-
Vse	Single ended receiver threshold	0.8	-	2.0	V	-
Output level for full speed and low speed						
Vol	Low level output voltage	0	-	0.3	V	-
Voh	High level output voltage	2.8	-	3.6	V	-
Resistance						

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Rdrv	Driver output impedance	40.5	45	49.5	ohm	Equivalent resistance used as an internal chip

Table 6-6 USB I/O Pin (USBDP, USBDM) Characteristics

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.4	-	-	V	Ioh=2mA~16mA
Vol	Output Voltage Low	-	-	0.4	V	Iol=2mA~16mA
Vih	Input High Voltage	2.0	-	-	V	LVTTL
Vil	Input Low Voltage	-	-	0.8	V	LVTTL
Vopu*	Output pull up voltage for 5V tolerant I/Os	VCC(3V3)-0.9	-	-	V	Ipu = 1uA
Iin	Input leakage current	-	±1	-	uA	Vin = VCC(3V3) or 0
		-	±1	-	uA	Vin = 5V or 0
Cin	Input capacitor	-	2.3	-	pF	VCC(3V3) with 5V tolerant I/O

Table 6-7 5V Tolerant Pin (PSW_N, OC_N, VBUS) Characteristics

Note*: This parameter is to indicate that the pull up resistor for the 5V tolerant I/Os cannot reach VCC(3V3) DC level even without DC loading current.

6.3 AC Characteristics

AC Characteristics (Ambient Temperature = -40°C to +85°C)

System clock dynamic characteristics:

Parameter	Value			Unit
	Minimum	Typical	Maximum	
Crystal oscillator				
Clock frequency	-	12.00	-	MHz
	-	19.20	-	
	-	24.00	-	
External clock input				
external clock jitter	-	-	500	ps
clock duty cycle	45	50	55	%

Input voltage on pin X1/CLKIN	-	3.3	-	V

Recommended accuracy of the clock frequency is 50ppm for the crystal.

Table 6-8 System clock characteristics

Analog I/O pins (DP/DM) dynamic characteristics:

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Driver characteristic for high speed						
Thsr	High speed differential rise time	500	-	-	ps	-
Thsf	High speed differential fall time	500	-	-	ps	-
Driver characteristic for full speed						
Tfr	Rise time of DP/DM	4	-	20	ns	Cl=50pF 10%~90% of |Voh–Vol|
Tff	Fall time of DP/DM	4	-	20	ns	Cl=50pF 10%~90% of |Voh–Vol|
Tfrma	Differential rise/fall time matching	90	-	110	%	The first transition exclude from the idle mode
Driver characteristic for low speed						
Tlr	Rise time of DP/DM	75	-	300	ns	Cl=200pF~600pF 10%~90% of |Voh–Vol|
Tlf	Fall time of DP/DM	75	-	300	ns	Cl=200pF~600pF 10%~90% of |Voh–Vol|
Tlrma	Differential rise/fall time matching	80	-	125	%	The first transition exclude from the idle mode

Table 6-9 Analog I/O pins characteristics

6.4 Timing

6.4.1 PIO timing

SRAM PIO timing characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	VCC(I/O)=1.8V		VCC(I/O)=2.5V		VCC(I/O)=3.3V		Unit
		Min	Max	Min	Max	Min	Max	
Tcs	CS_N setup time before WR_N / RD_N low	0	-	0	-	0	-	ns
Tch	CS_N hold time after WR_N / RD_N high	0	-	0	-	0	-	ns
Tcp	CS_N pulse width for read	40	-	40	-	40	-	ns
	CS_N pulse width for write	40	-	40	-	40	-	ns
Tasrw	address setup time before WR_N / RD_N low	0	-	0	-	0	-	ns
Tahrw	Address Hold Time after WR_N/RD_N LOW	0	-	0	-	0	-	ns
Tap	Address Latch Pulse Width							ns
Twc	Write Cycle Time	80	-	79	-	78.5	-	ns
Twp	WR_N Pulse Width	40	-	40	-	40	-	ns
Tdh	RD_N High to Output Hi-Z	4	9	4	7	4	6	ns
	WR_N High to Input Hi-Z	0	-	0	-	0	-	ns
Tdadvh	DATA Setup Time before DATA Latch	6	-	6	-	6	-	ns
Toe	RD_N Low to DATA Output Enable	8	-	7	-	6	-	ns
Trp	RD_N Pulse Width	40	-	40	-	40	-	ns
Trc	Read Cycle Time	80	-	79.5	-	79	-	ns

Table 6-10 SRAM PIO timing

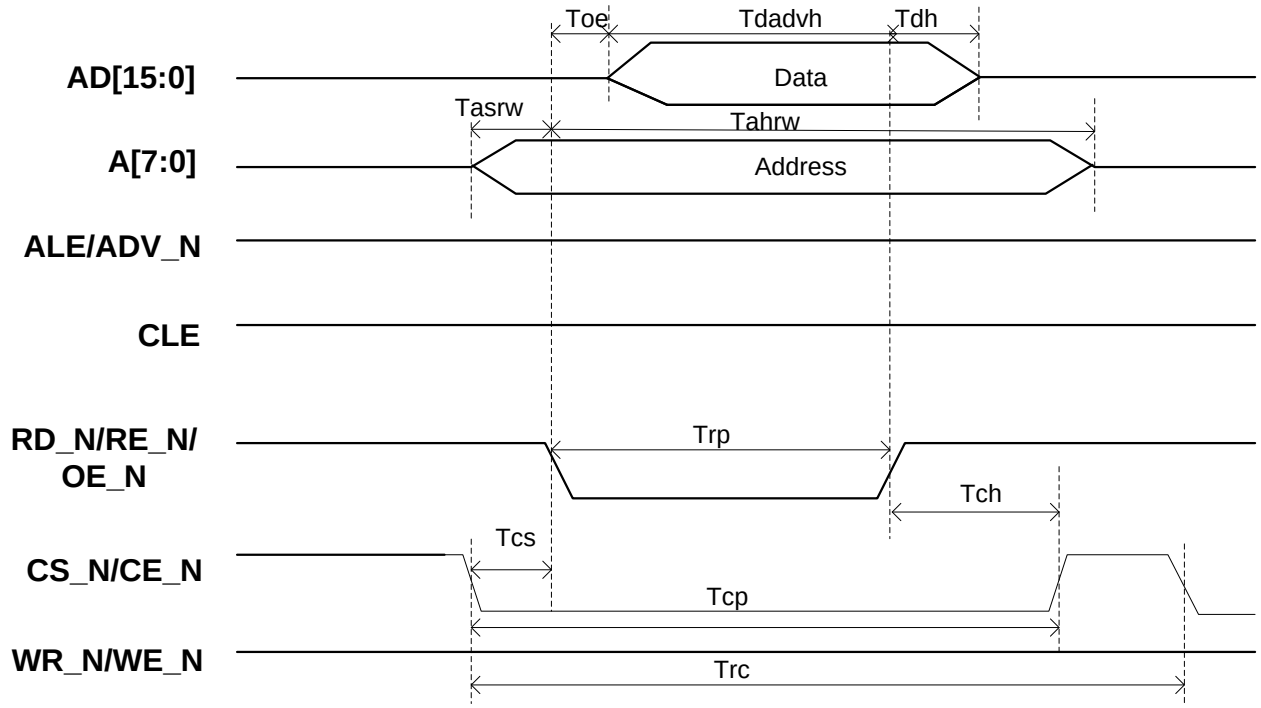


Figure 6-1 Read in SRAM mode

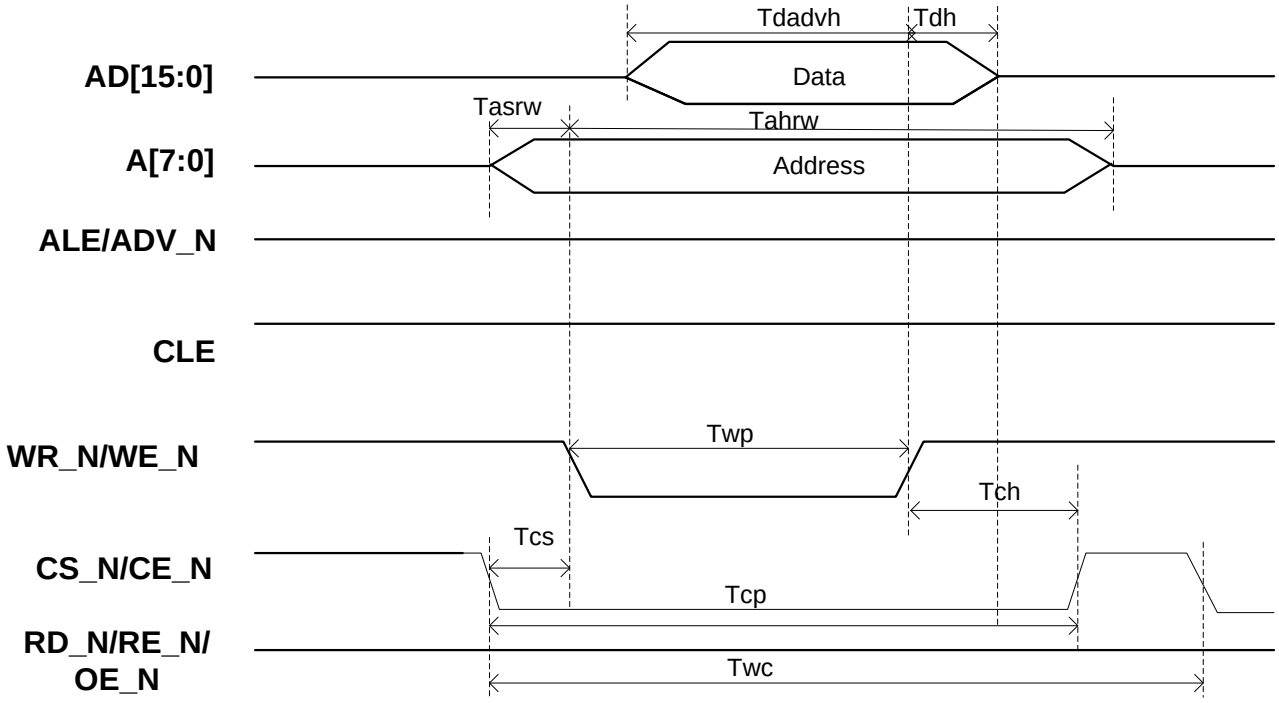


Figure 6-2 Write in SRAM mode

NOR PIO timing characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	VCC(I/O)=1.8V		VCC(I/O)=2.5V		VCC(I/O)=3.3V		Unit
		Min	Max	Min	Max	Min	Max	
Tch	CS_N hold time after WR_N / RD_N high	0	-	0	-	0	-	ns
Tcsadval	CS_N setup time before Address Latch	6.5	-	6.5	-	6	-	ns
Tah	Address Hold Time after Address Latch	0	-	0	-	0	-	ns
Tas	Address Setup Time before Address Latch	6	-	6	-	5	-	ns
Tap	Address Latch Pulse Width	10	-	10	-	10	-	ns
Twc	Write Cycle Time	80	-	78.5	-	78.5	-	ns
Twp	WR_N Pulse Width	40	-	40	-	40	-	ns
Tdh	RD_N High to Output Hi-Z	4	8	4	7	4	7	ns
	WR_N High to Input Hi-Z	0	-	0	-	0	-	ns
Tdadvh	DATA Setup Time before DATA Latch	6	-	5	-	5	-	ns
Toe	RD_N Low to DATA Output Enable	8	-	6	-	5	-	ns
Tbds	Ready to WR_N/RD_N Low	5	-	5	-	5	-	ns
Trp	RD_N Pulse Width	40	-	40	-	40	-	ns
Trc	Read Cycle Time	80	-	79	-	79	-	ns

Table 6-11 NOR PIO timing

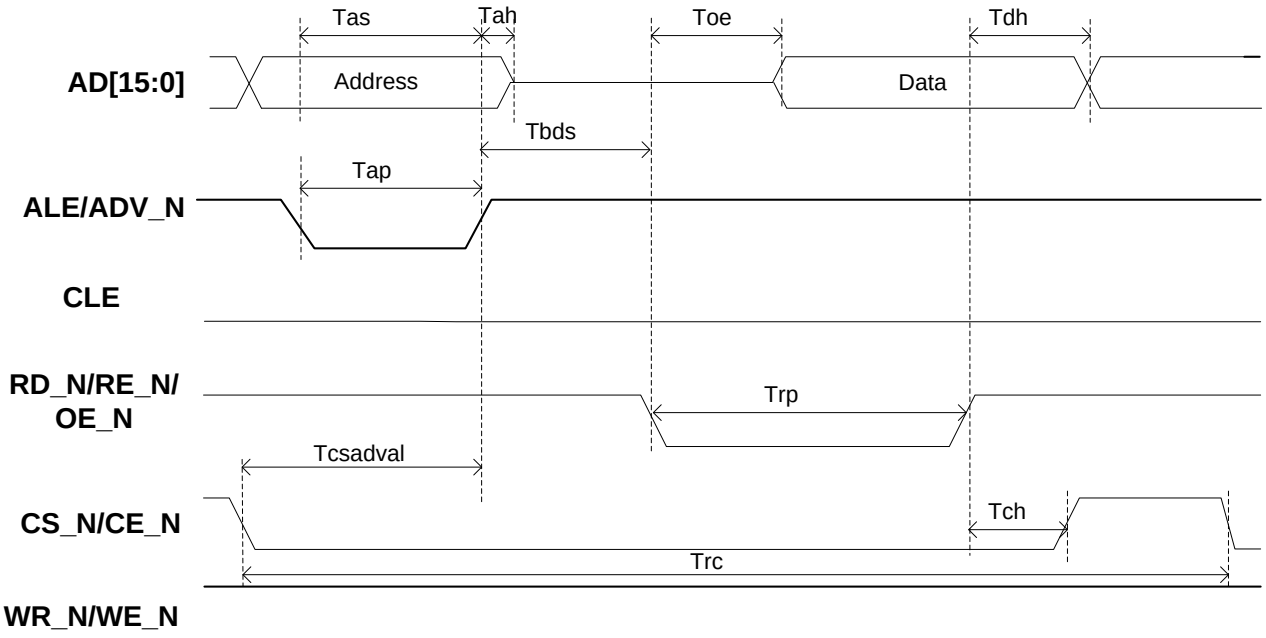


Figure 6-3 Read in NOR mode

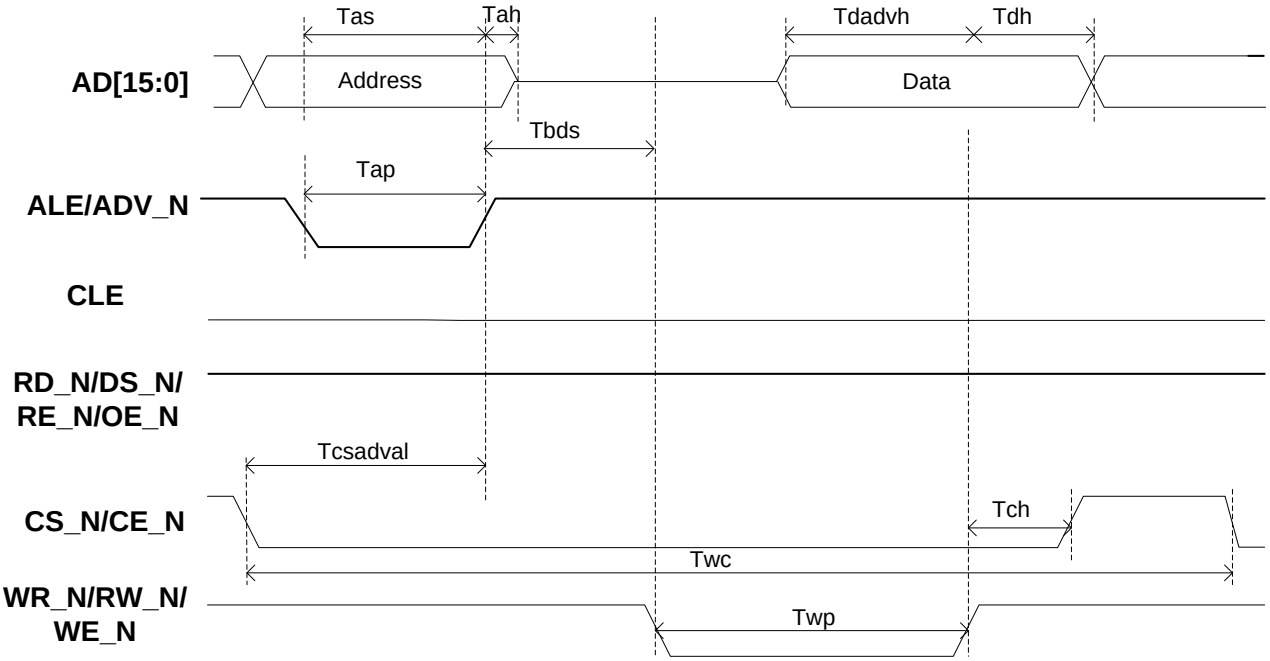


Figure 6-4 Write in NOR mode

General Multiplex PIO timing characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	VCC(I/O)=1.8V		VCC(I/O)=2.5V		VCC(I/O)=3.3V		Unit
		Min	Max	Min	Max	Min	Max	
Tch	CS_N hold time after WR_N / RD_N high	0	-	0	-	0	-	ns
Tcsadval	CS_N setup time before Address Latch	7.5	-	6.5	-	6.5	-	ns
Tah	Address Hold Time after Address Latch	0	-	0	-	0	-	ns
Tas	Address Setup Time before Address Latch	7	-	6	-	6	-	ns
Tap	Address Latch Pulse Width	10	-	10	-	10	-	ns
Twc	Write Cycle Time	80	-	78.5	-	78.5	-	ns
Twp	WR_N Pulse Width	40	-	40	-	40	-	ns
Tdh	RD_N High to Output Hi-Z	4	9	4	6.5	3.5	6	ns
	WR_N High to Input Hi-Z	0	-	0	-	0	-	ns
Tdadvh	DATA Setup Time before DATA Latch	6.5	-	5	-	5	-	ns
Toe	RD_N Low to DATA Output Enable	8	-	6	-	5	-	ns
Tbds	Ready to WR_N/RD_N Low	5	-	5	-	5	-	ns
Trp	RD_N Pulse Width	40	-	40	-	40	-	ns
Trc	Read Cycle Time	80	-	79	-	79	-	ns

Table 6-12 General Multiplex PIO timing

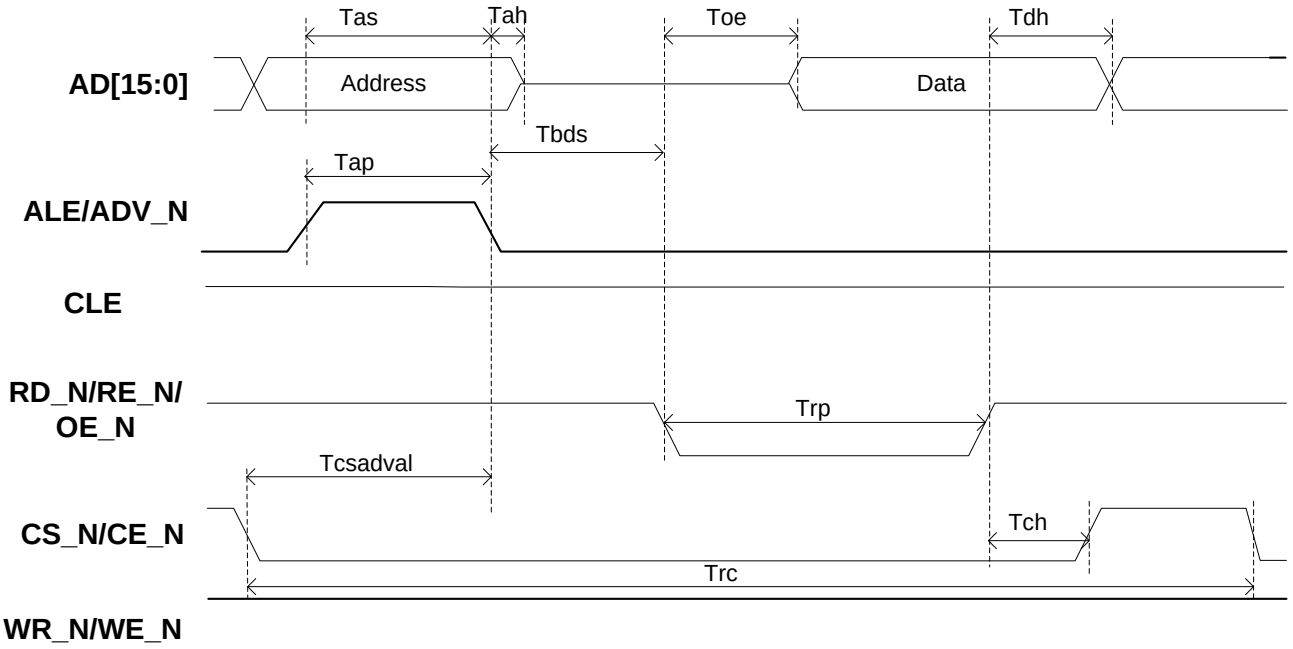


Figure 6-5 Read in General Multiplex mode

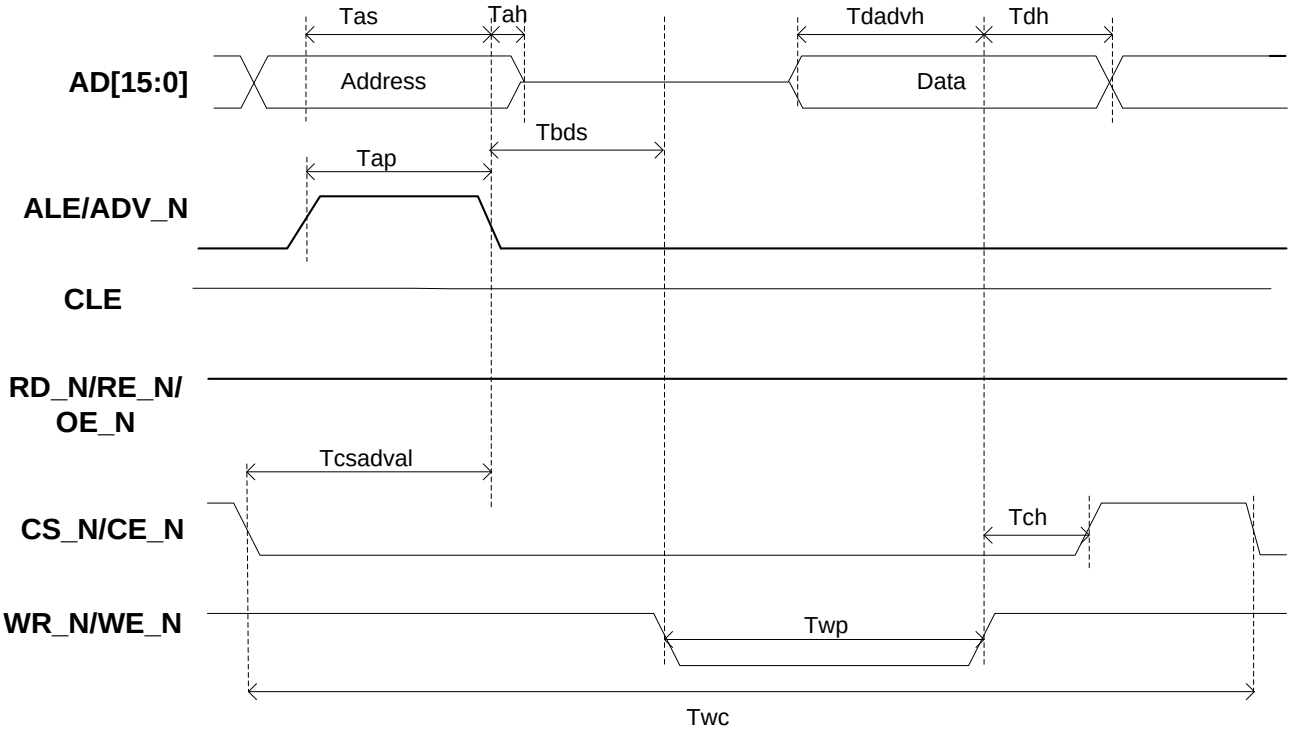


Figure 6-6 Write in General Multiplex mode

6.4.2 DMA timing

DMA timing characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Min	Max	Unit
$T_{sudreqdack}$	DREQ Set-up Time before DACK Assertion	0	-	ns
$T_{ddackdreq}$	DACK De-assertion to Next DREQ Assertion Time	18	-	ns
$T_{hdreqdack}$	DREQ Hold Time after Last Strobe Assertion	-	35	ns
T_{rwp}	RD_N/WR_N Pulse Width	40	-	ns
T_{oe}	Data Valid Time after RD_N Assertion	8	-	ns
T_{rdh}	Read Data Hold Time after RD_N De-asserts	4	9	ns
T_{wdh}	Write Data Hold Time after WR_N De-assertion	0	-	ns
T_{dadvh}	Write Data Set-up Time before WR_N De-assertion	6	-	ns
$T_{sudackrw}$	DACK Set-up Time before RD_N/WR_N Assertion	0	-	ns
T_{rwdack}	DACK De-assertion after RD_N/WR_N De-assertion	0	-	ns
T_{cyc}	DMA Read/Write Cycle Time	80	-	ns

Table 6-13 DMA timing

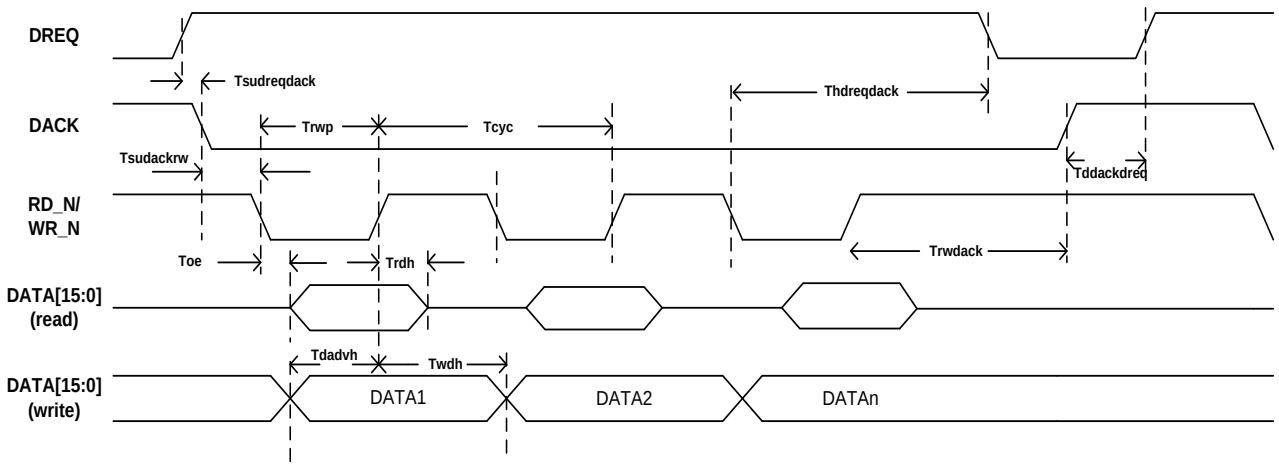
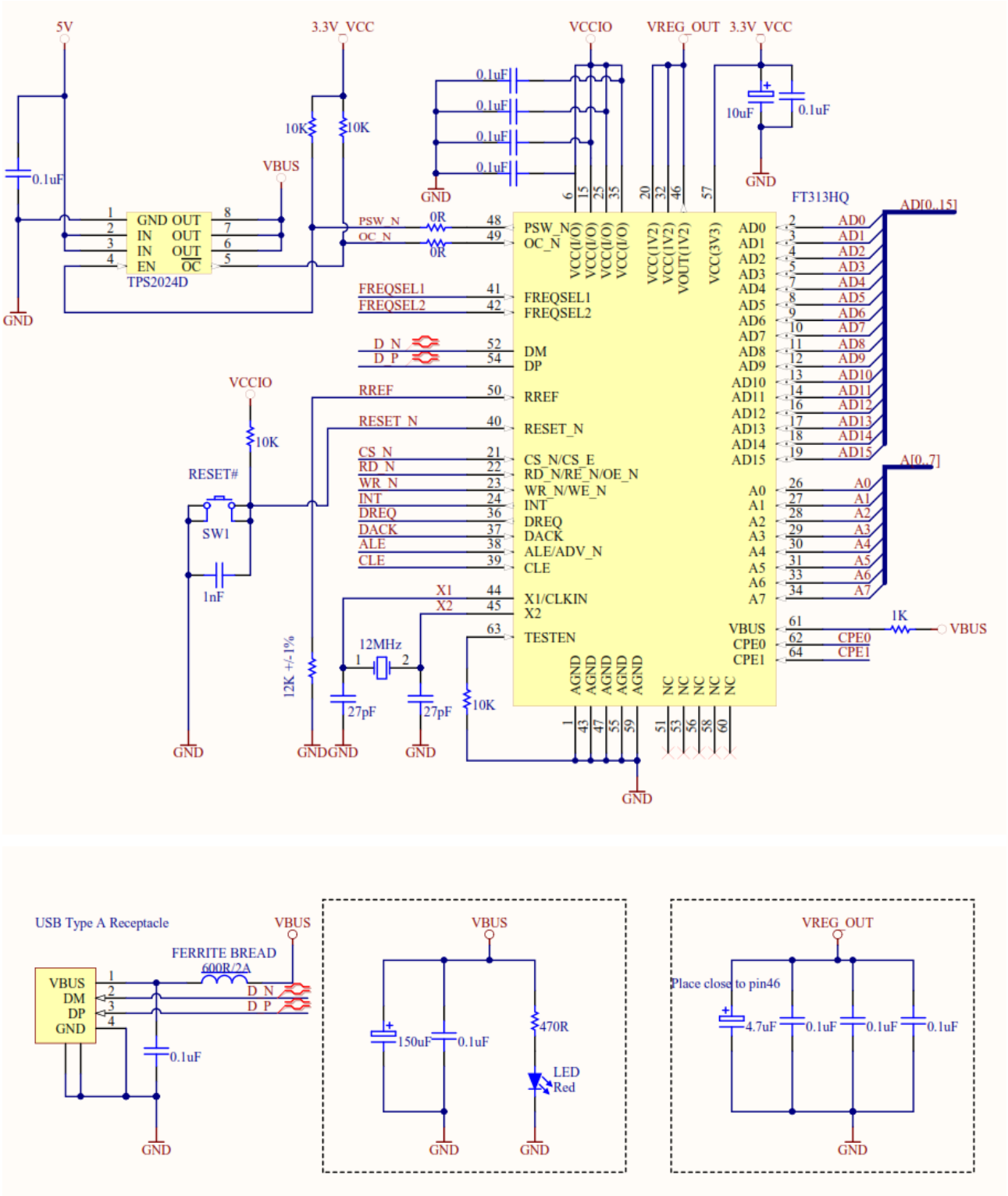


Figure 6-7 DMA read and write

7 Application Examples

FT313H can be configured to communicate with a microcontroller uses 16-bit/8-bit SRAM asynchronous bus interface, NOR interface, and General Multiplex interface. An example schematic is show in Figure 7.1.



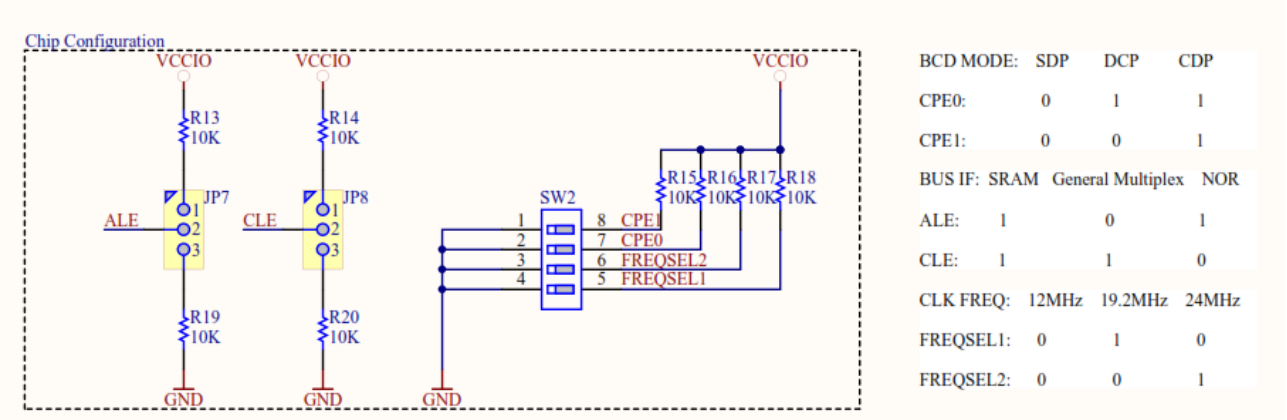
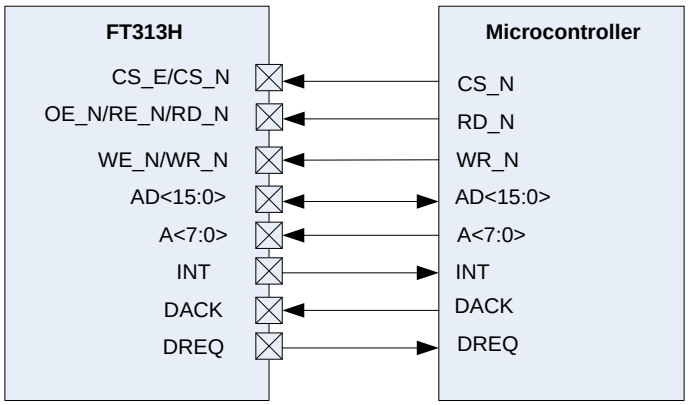


Figure 7-1 FT313H Chip Schematic

7.1 Examples of Bus Interface connection

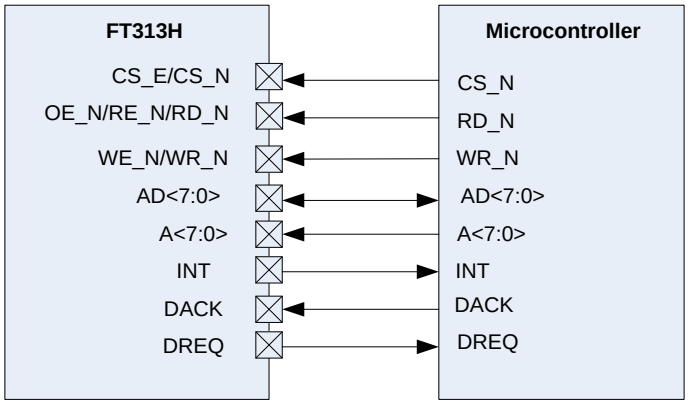
7.1.1 16-Bit SRAM asynchronous bus interface



If DMA transfers are not used the DACK and DREQ signals may be left floating or the DACK signal may be terminated with external 10k ohm pull-down resistor.

If the microcontroller has no AD<0> pin for 16-bit wide devices, the unused AD<0> signal with must be terminated with an external 10k ohm pull-down resistor.

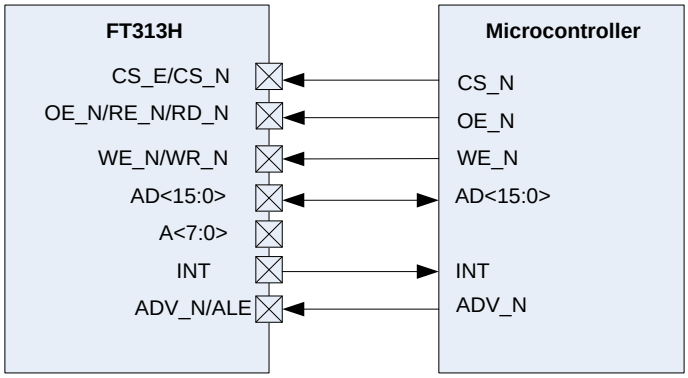
7.1.2 8-Bit SRAM asynchronous bus interface



8-Bit SRAM bus interface doesn't use high AD<15:8> data bus, must terminate AD<15:8> signals with external 10k ohm pull-down resistors.

If DMA transfers are not used the DACK and DREQ signals may be left floating or the DACK signal may be terminated with external 10k ohm pull-down resistor.

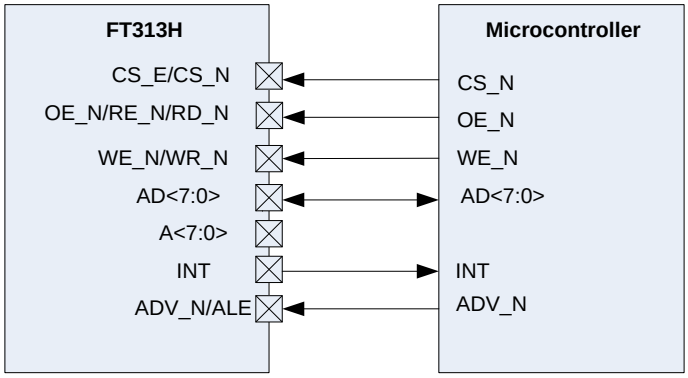
7.1.3 16-Bit NOR asynchronous bus interface



16-Bit NOR uses AD<15:0> signals as address and data bus. Unused A<7:0> address must be terminated with external 10k ohm pull-down resistor.

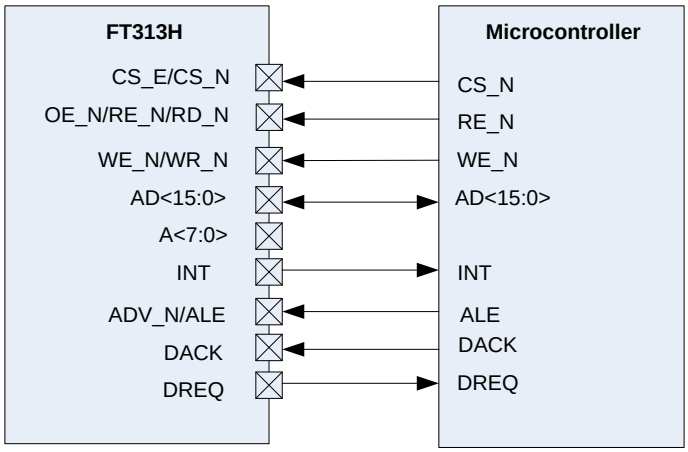
If the microcontroller has no AD<0> pin for 16-bit wide devices, the unused AD<0> signal with must be terminated with an external 10k ohm pull-down resistor.

7.1.4 8-Bit NOR asynchronous bus interface



8-Bit NOR uses AD<7:0> signals as address and data bus. The unused high data bus AD<15:8> and A<7:0> address bus must be terminated with external 10k ohm pull-down resistors.

7.1.5 16-Bit General Multiplex asynchronous bus interface

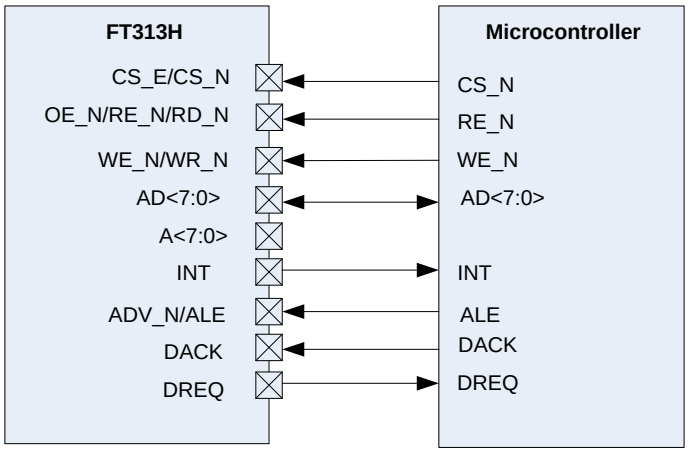


16-Bit General Multiplex uses AD<15:0> signals as address and data bus. Unused A<7:0> address must be terminated with external 10k ohm pull-down resistor.

If the microcontroller has no AD<0> pin for 16-bit wide devices, the unused AD<0> signal with must be terminated with an external 10k ohm pull-down resistor.

If DMA transfers are not used the DACK and DREQ signals may be left floating or the DACK signal may be terminated with external 10k ohm pull-down resistor.

7.1.6 8-Bit General Multiplex asynchronous bus interface



8-Bit General Multiplex uses AD<7:0> signals as address and data bus. The unused high data bus AD<15:8> and A<7:0> address bus must be terminated with external 10k ohm pull-down resistors.

If DMA transfers are not used the DACK and DREQ signals may be left floating or the DACK signal may be terminated with external 10k ohm pull-down resistor.

8 Package Parameters

The FT313H is available in three different packages. The FT313HQ is the QFN-64 package, the FT313HL is the LQFP-64 package and the FT313HP is the TQFP-64 package. The solder reflow profile for all packages is described in following sections.

8.1 FT313H Package Markings

8.1.1 QFN-64

An example of the markings on the QFN package are shown in Figure 8-1. The FTDI part number is too long for the 64 QFN package so in this case the last two digits are wrapped down onto the date code line.

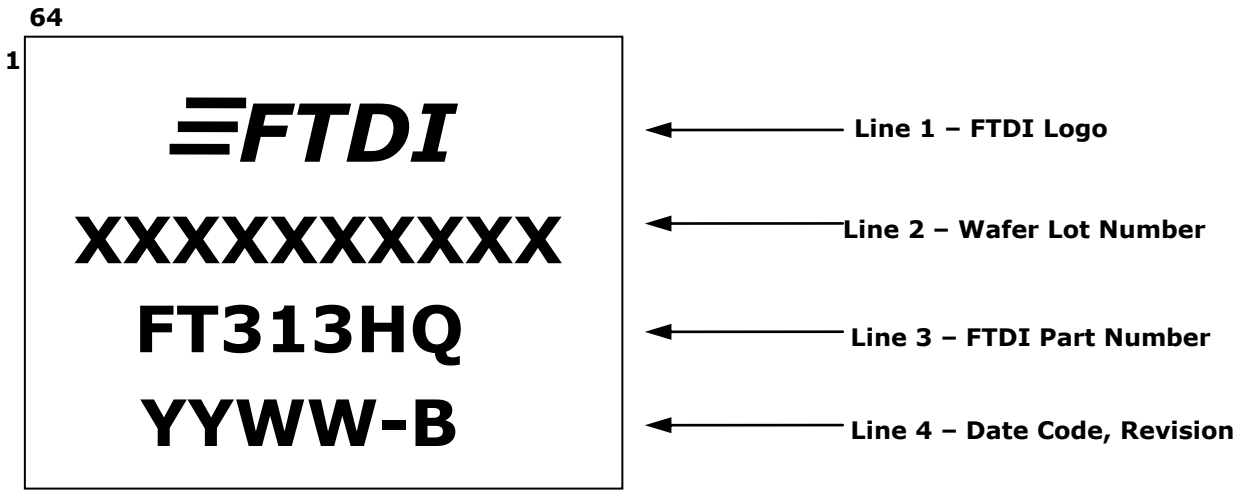


Figure 8-1 QFN Package Markings

Notes:

1. YYWW = Date Code, where YY is year and WW is week number
2. Marking alignment should be centre justified
3. Laser Marking should be used

8.1.2 LQFP-64

An example of the markings on the LQFP package are shown in Figure 8-2.

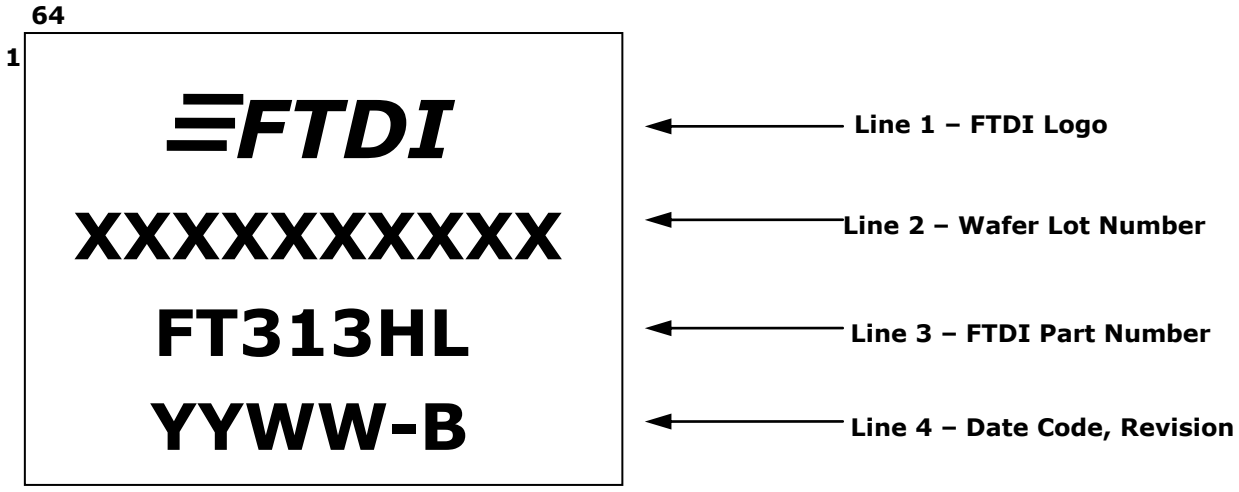


Figure 8-2 LQFP Package Markings

Notes:

1. YYWW = Date Code, where YY is year and WW is week number
2. Marking alignment should be centre justified
3. Laser Marking should be used

8.1.3 TQFP-64

An example of the markings on the TQFP package are shown in **Error! Reference source not found.**.

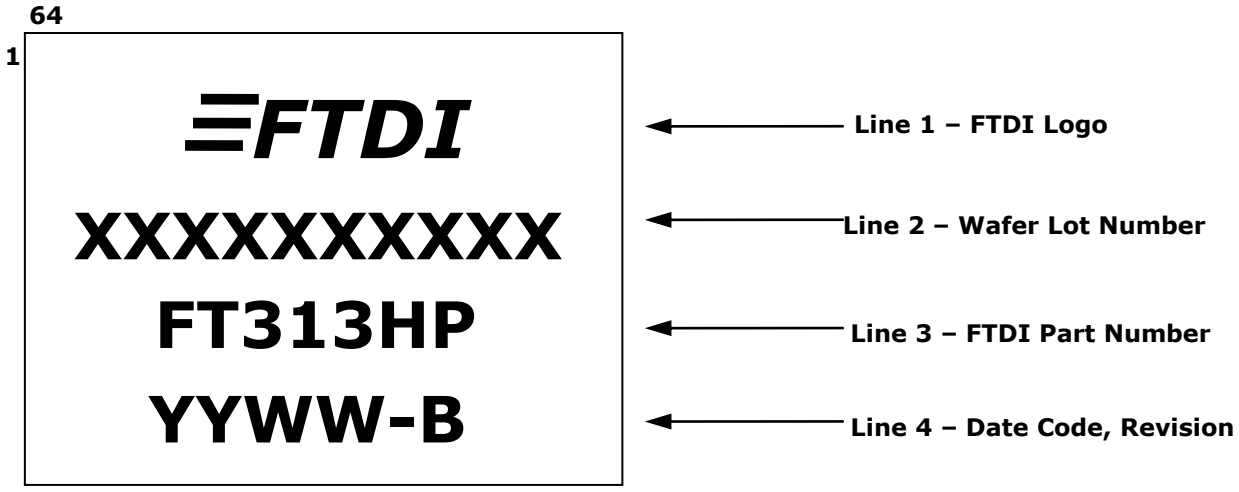
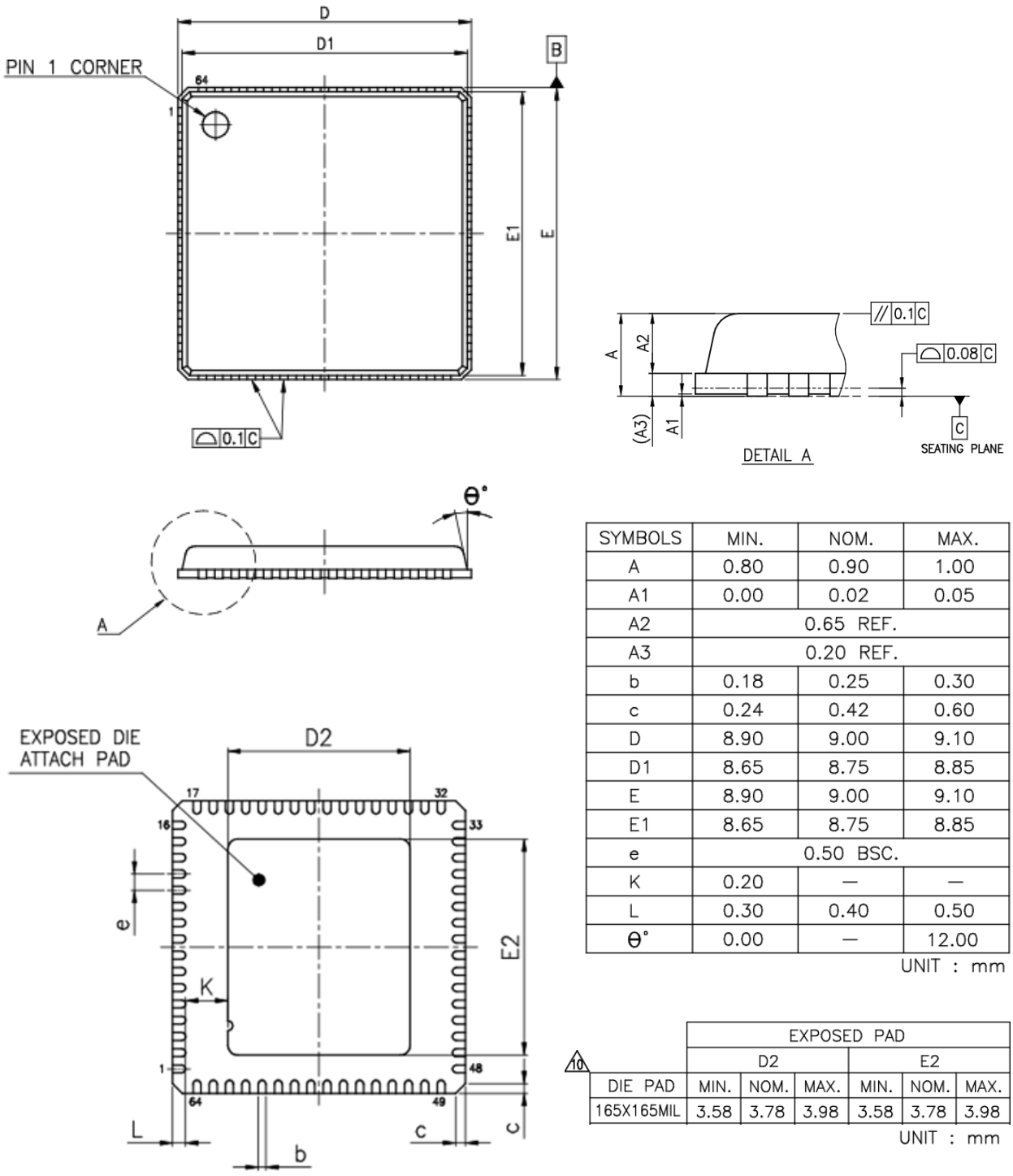


Figure 8-3 TQFP Package Markings

Notes:

1. YYWW = Date Code, where YY is year and WW is week number
2. Marking alignment should be centre justified
3. Laser Marking should be used

8.2 QFN-64 Package Dimensions



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.20 REF.	
b	0.18	0.25	0.30
c	0.24	0.42	0.60
D	8.90	9.00	9.10
D1	8.65	8.75	8.85
E	8.90	9.00	9.10
E1	8.65	8.75	8.85
e		0.50 BSC.	
K	0.20	—	—
L	0.30	0.40	0.50
θ°	0.00	—	12.00

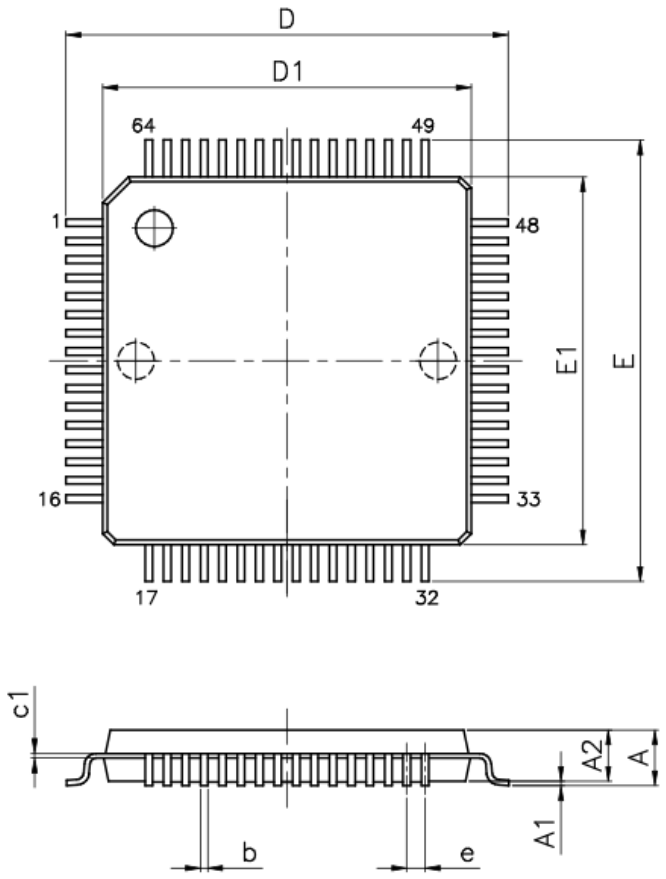
UNIT : mm

	EXPOSED PAD					
	D2			E2		
DIE PAD	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
165X165MIL	3.58	3.78	3.98	3.58	3.78	3.98

UNIT : mm

Figure 8-4 QFN-64 Package Markings

8.3 LQFP-64 Package Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c1	0.09	–	0.16
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20 REF		
θ	3.5° REF		
θ1	5.0° REF		
θ2	12° REF		
θ3	12° REF		
R1	0.16 REF		
R2	0.15 REF		

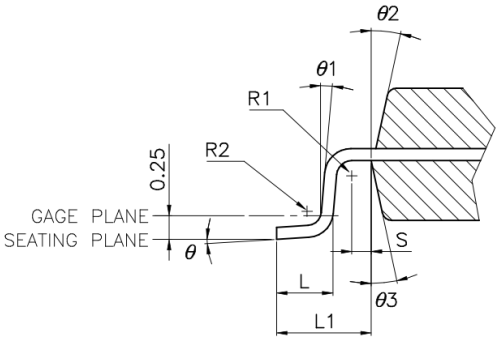
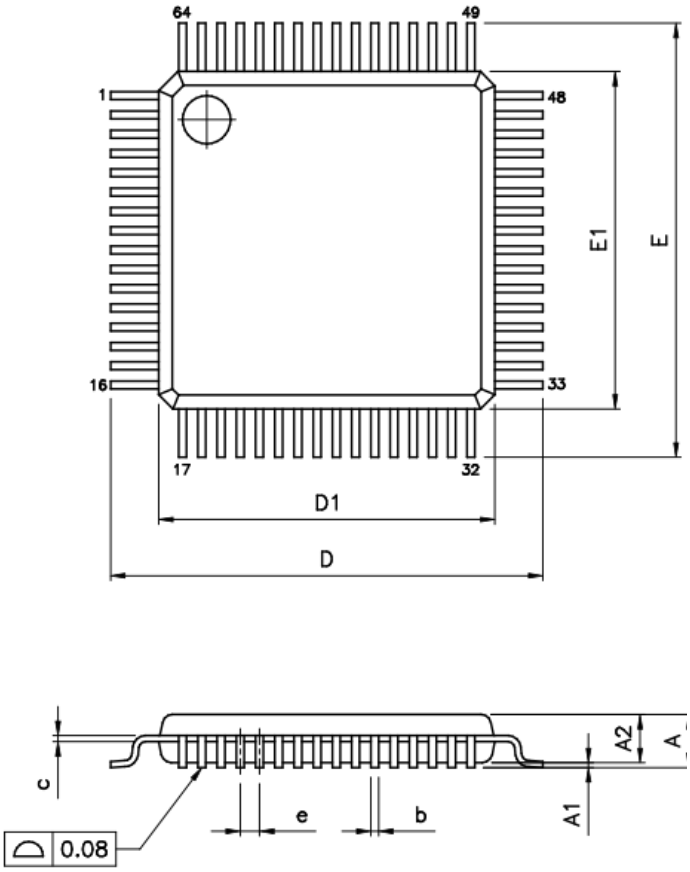


Figure 8-5 LQFP-64 Package Markings

8.4 TQFP-64 Package Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.20
A1	0.05	--	0.15
A2	0.95	1.00	1.05
b	0.13	0.18	0.23
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

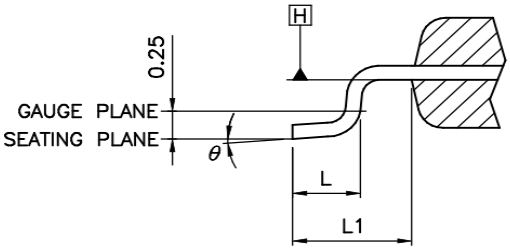


Figure 8-6 TQFP-64 Package Markings

8.5 Solder Reflow Profile

The FT313H is supplied in Pb free QFN-64, LQFP-64 and TQFP-64 packages. The recommended solder reflow profile for all package options is shown in

.

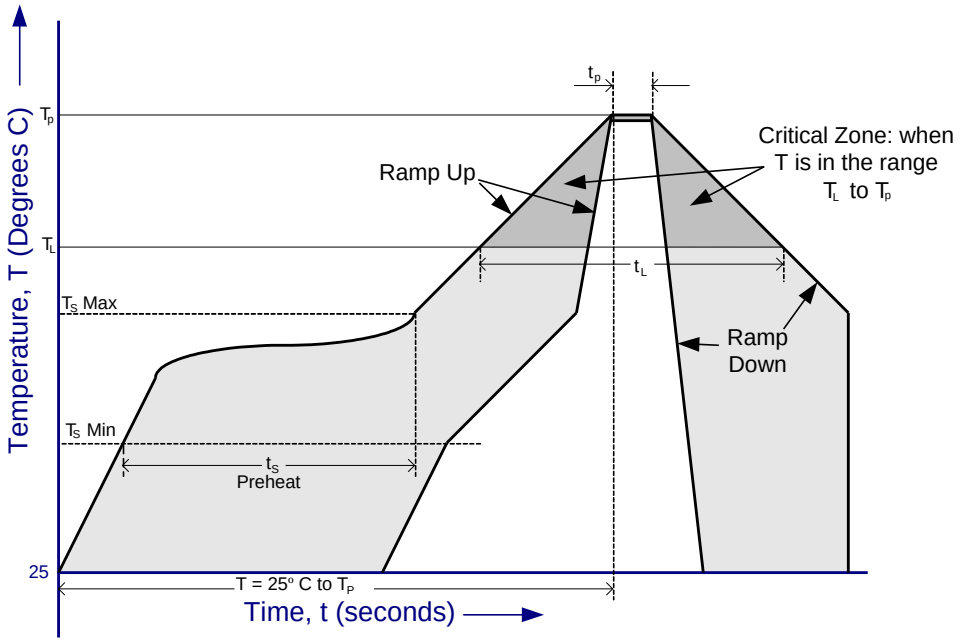


Figure 8-7 FT313H Solder Reflow Profile

The recommended values for the solder reflow profile are detailed in Table 8-1. Values are shown for both a completely Pb free solder process (i.e. the FT313H is used with Pb free solder), and for a non-Pb free solder process (i.e. the FT313H is used with non-Pb free solder).

Profile Feature	Pb Free Solder Process	Non-Pb Free Solder Process
Average Ramp Up Rate (T_s to T_p)	3°C / second Max.	3°C / Second Max.
Preheat - Temperature Min (T_s Min.) - Temperature Max (T_s Max.) - Time (t_s Min to t_s Max)	 150°C 200°C 60 to 120 seconds	 100°C 150°C 60 to 120 seconds
Time Maintained Above Critical Temperature T_L: - Temperature (T_L) - Time (t_L)	 217°C 60 to 150 seconds	 183°C 60 to 150 seconds
Peak Temperature (T_p)	260°C	240°C
Time within 5°C of actual Peak Temperature (t_p)	20 to 40 seconds	20 to 40 seconds
Ramp Down Rate	6°C / second Max.	6°C / second Max.
Time for T= 25°C to Peak Temperature, T_p	8 minutes Max.	6 minutes Max.

Table 8-1 Reflow Profile Parameter Values

9 FTDI Chip Contact Information

Head Office – Glasgow, UK

Unit 1, 2 Seaward Place, Centurion Business Park
Glasgow G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales) sales1@ftdichip.com
E-mail (Support) support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com

Branch Office – Tigard, Oregon, USA

7130 SW Fir Loop
Tigard, OR 97223
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-Mail (Sales) us.sales@ftdichip.com
E-Mail (Support) us.support@ftdichip.com
E-Mail (General Enquiries) us.admin@ftdichip.com

Branch Office – Taipei, Taiwan

2F, No. 516, Sec. 1, NeiHu Road
Taipei 114
Taiwan, R.O.C.
Tel: +886 (0) 2 8797 1330
Fax: +886 (0) 2 8751 9737

E-mail (Sales) tw.sales1@ftdichip.com
E-mail (Support) tw.support1@ftdichip.com
E-mail (General Enquiries) tw.admin1@ftdichip.com

Branch Office – Shanghai, China

Room 1103, No. 666 West Huaihai Road,
Changning District
Shanghai, 200052
China
Tel: +86 21 62351596
Fax: +86 21 62351595

E-mail (Sales) cn.sales@ftdichip.com
E-mail (Support) cn.support@ftdichip.com
E-mail (General Enquiries) cn.admin@ftdichip.com

Web Site

http://ftdichip.com

Appendix A – References

Useful Application Notes

Appendix B - List of Figures and Tables

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Appendix C - Revision History

Document Title:	USB Host IC FT313H
Document Reference No.:	FT_000589
Clearance No.:	FTDI# 318
Product Page:	http://www.ftdichip.com/FTProducts.htm
Document Feedback:	DS_FT313H

Version 1.0	Initial Release	OCT 2012
Version 1.1	Formatting tidy up	NOV 2012
Version 1.2	Add package markings	SEP 2013