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# FDMS5672

## N-Channel UltraFET Trench<sup>®</sup> MOSFET

60V, 22A, 11.5mΩ

### Features

- Max  $r_{DS(on)}$  = 11.5mΩ at  $V_{GS} = 10V$ ,  $I_D = 10.6A$
- Max  $r_{DS(on)}$  = 16.5mΩ at  $V_{GS} = 6V$ ,  $I_D = 8A$
- Typ Qg = 32nC at  $V_{GS} = 10V$
- Low Miller Charge
- Optimized Efficiency at High Frequencies
- RoHS Compliant

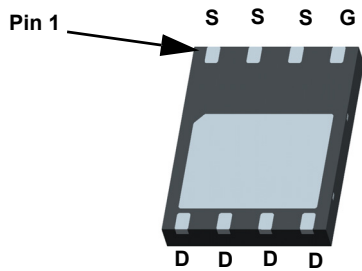


### General Description

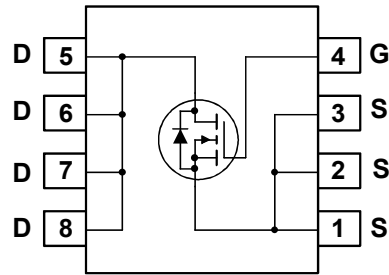
UltraFET devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for  $r_{DS(on)}$ , low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

### Application

- DC - DC Conversion



Power 56 (Bottom view)



### MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	60	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous	$T_C = 25^\circ C$ (Note 5)	65
	-Continuous	$T_C = 100^\circ C$ (Note 5)	39
	-Continuous	$T_A = 25^\circ C$ (Note 1a)	10.6
	-Pulsed	(Note 4)	176
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	337
$P_D$	Power Dissipation	$T_C = 25^\circ C$	78
	Power Dissipation	$T_A = 25^\circ C$ (Note 1a)	2.5
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.6	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS5672	FDMS5672	Power 56	13"	12mm	3000 units

FDMS5672 N-Channel UltraFET Trench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		59		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{V}, V_{GS} = 0\text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	3.2	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-11		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 10.6\text{A}$		9.4	11.5	m $\Omega$
		$V_{GS} = 6\text{V}, I_D = 8\text{A}$		13.0	16.5	
		$V_{GS} = 10\text{V}, I_D = 10.6\text{A}, T_J = 125^\circ\text{C}$		15.0	18.0	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 10.6\text{A}$		26		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		2100	2800	pF
$C_{oss}$	Output Capacitance			375	500	pF
$C_{rss}$	Reverse Transfer Capacitance			120	180	pF
$R_g$	Gate Resistance	$f = 1\text{MHz}$		1.2		$\Omega$

### Switching Characteristics

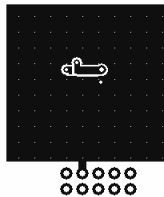
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{V}, I_D = 10.6\text{A}, V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$		16	29	ns
$t_r$	Rise Time			17	31	ns
$t_{d(off)}$	Turn-Off Delay Time			22	35	ns
$t_f$	Fall Time			8	16	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V		$V_{GS} = 0\text{V to } 10\text{V}$		32	45
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 30\text{V}, I_D = 10.6\text{A}$		10		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			8.3		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 10.6\text{A}$ (Note 2)		0.80	1.20	V
$t_{rr}$	Reverse Recovery Time	$I_F = 10.6\text{A}, di/dt = 100\text{A}/\mu\text{s}$		35	53	ns
$Q_{rr}$	Reverse Recovery Charge			42	63	nC

#### Notes:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



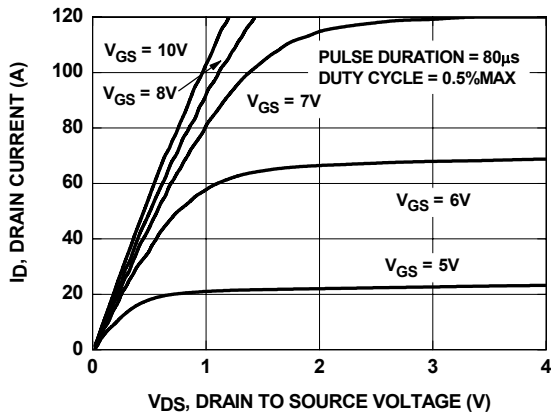
a.  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper



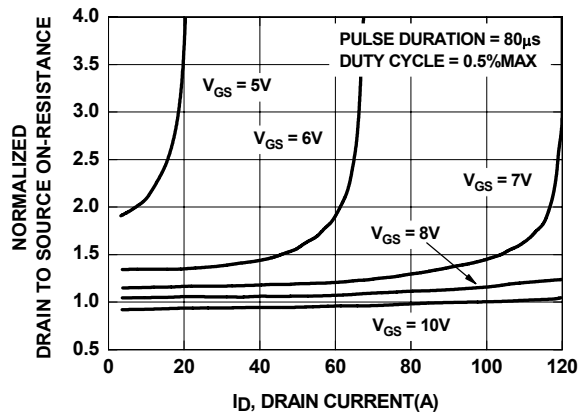
b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty cycle  $< 2.0\%$ .
- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{mH}$ ,  $I_{AS} = 15\text{A}$ ,  $V_{DD} = 60\text{V}$ ,  $V_{GS} = 10\text{V}$ .
- Pulsed  $I_d$  please refer to Fig 11 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

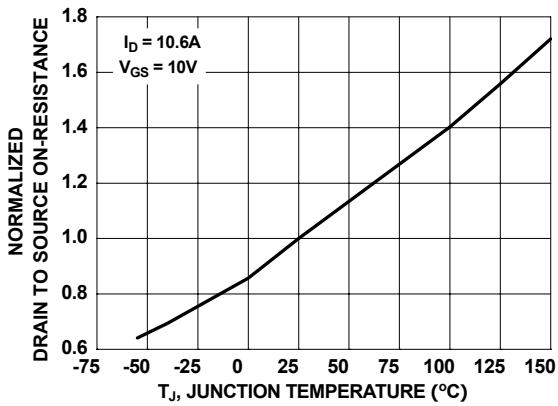
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



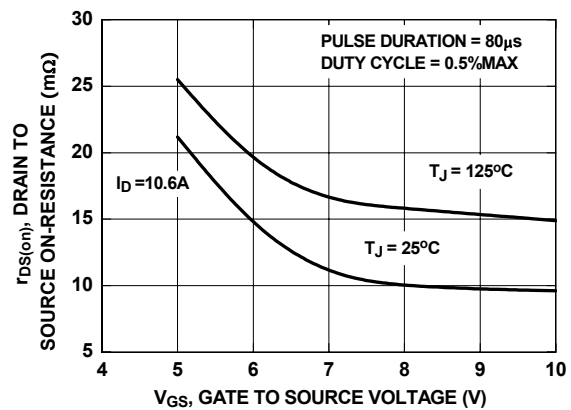
**Figure 1. On Region Characteristics**



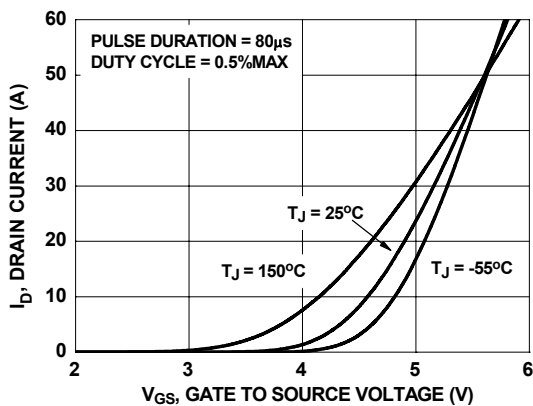
**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**



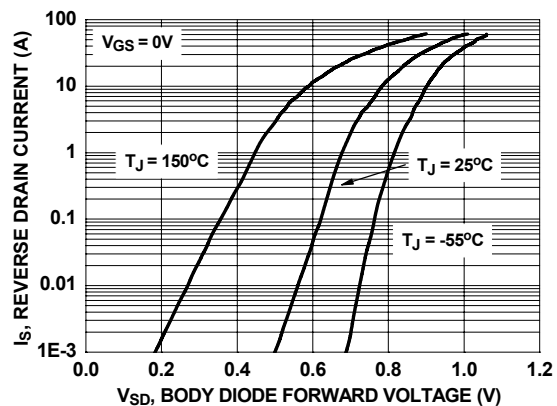
**Figure 3. Normalized On Resistance vs. Junction Temperature**



**Figure 4. On-Resistance vs. Gate to Source Voltage**



**Figure 5. Transfer Characteristics**



**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

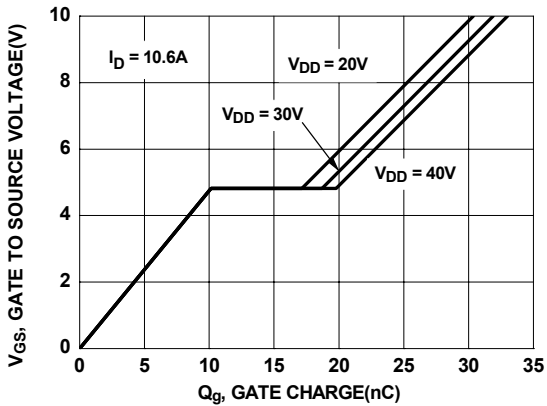


Figure 7. Gate Charge Characteristics

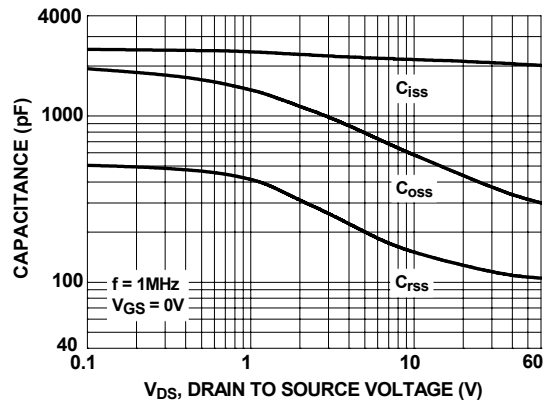


Figure 8. Capacitance vs. Drain to Source Voltage

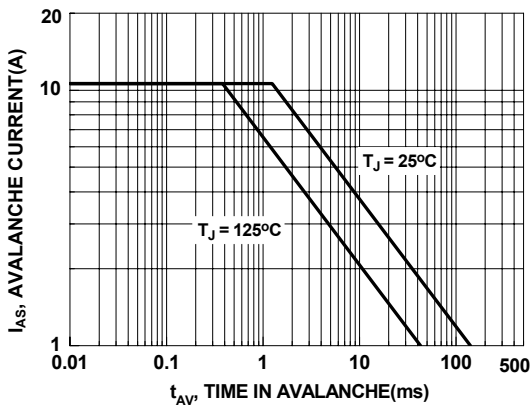


Figure 9. Unclamped Inductive Switching Capability

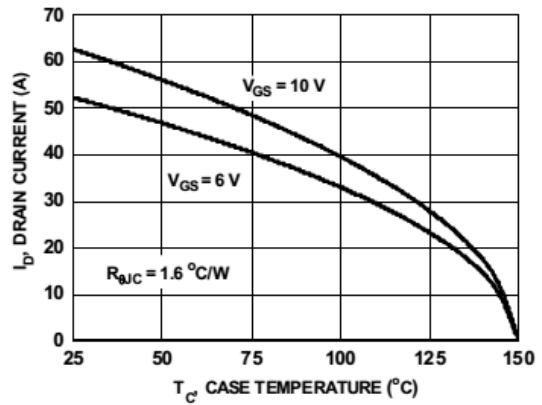


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

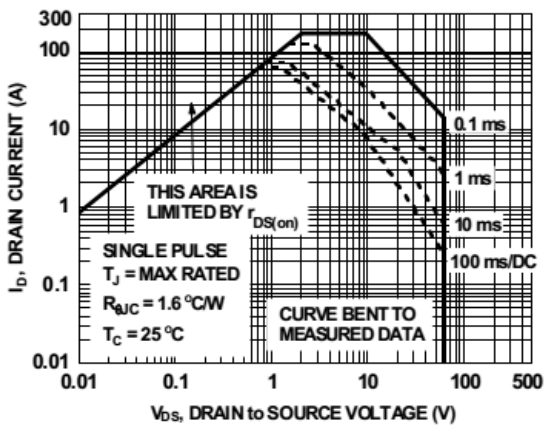


Figure 11. Forward Bias Safe Operating Area

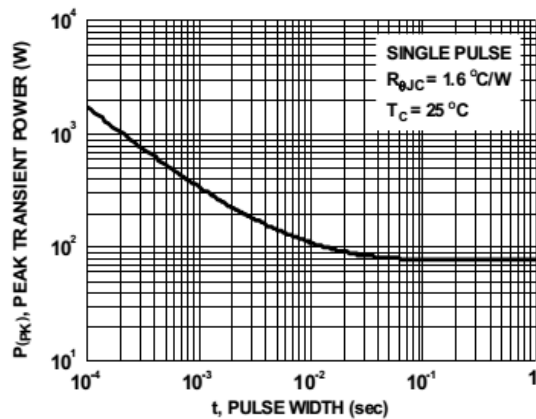


Figure 12. Single Pulse Maximum Power Dissipation

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

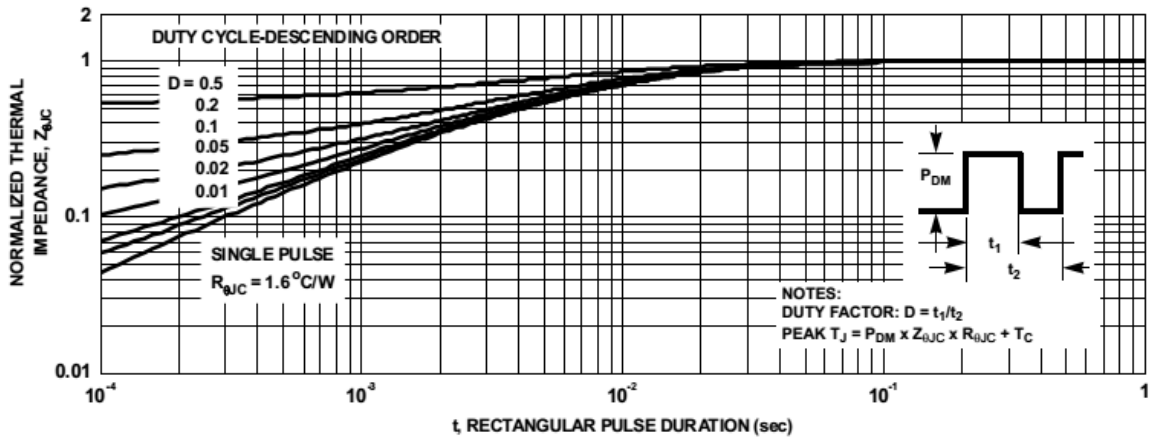
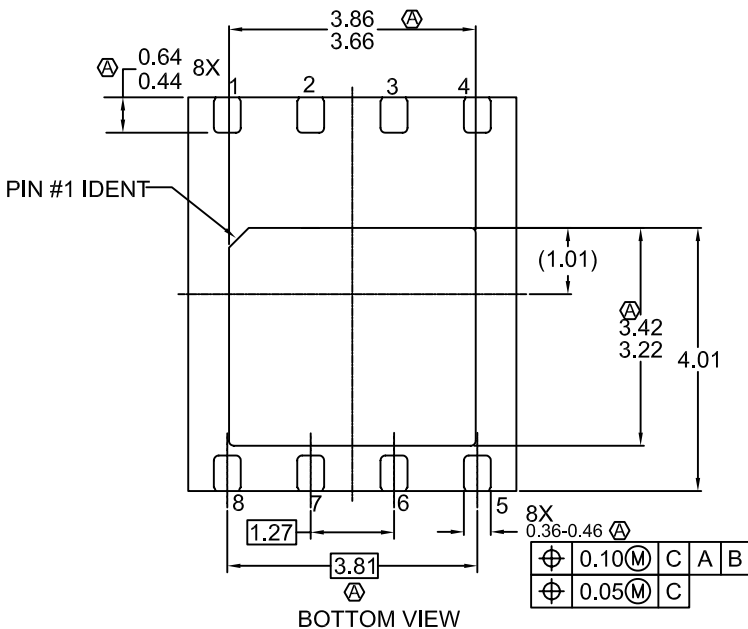
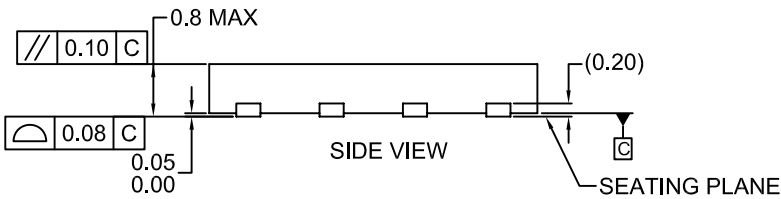
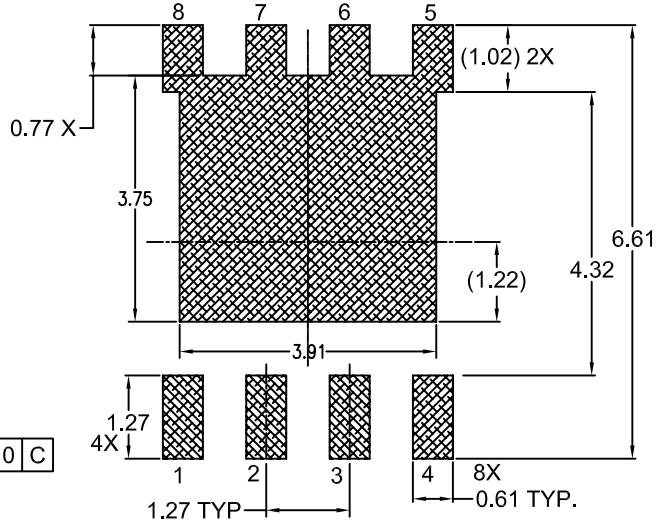
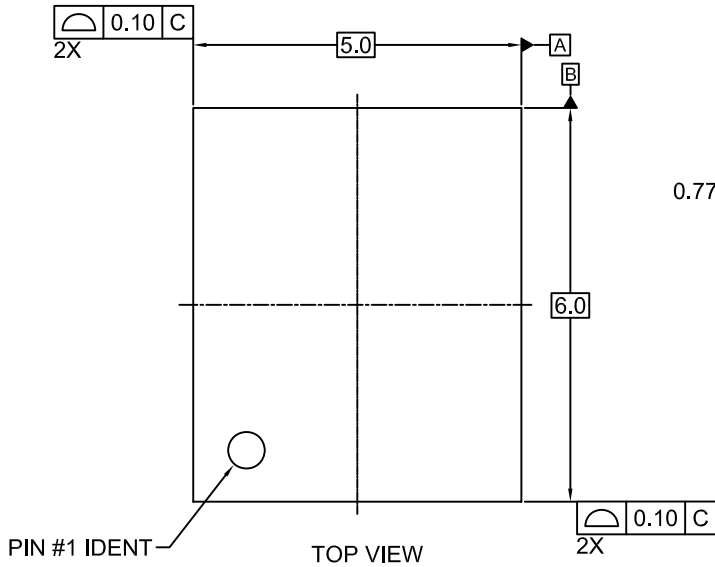


Figure 13. Transient Thermal Response Curve

REVISIONS			
NBR	DESCRIPTION	DATE	NAME/SITE
1	RELEASE TO DOCUMENT CONTROL	090305	David/FSPM
2	REVISE TO CORRECT DAP SIZE	080605	David/FSPM
3	I) REVISE TO CORRECT PKG THK II) REVISE THE PKG PROFILE TOLERANCE	210306	CK/FSPM
4	ADD IN LEAD LENGTH FOR LAND PATTERN	220908	LY/FSPM



NOTES:

- A DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. TERMINALS 5,6,7 AND 8 ARE TIED TO THE EXPOSED PADDLE
- E. LANDPATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY
- F. DRAWING FILENAME: MKT-MLP08Grev4

APPROVALS	DATE	FAIRCHILD SEMICONDUCTOR™			
DRAWN LY Lim	01 Nov 08	8LD, MLP, DUAL, NON-JEDEC, 5X6 MM BODY, TIED DAP			
DFTG. CHK. LY LIM	01 Nov 08				
ENGR. CHK. DAVID	01 Nov 08				
PROJECTION		SCALE N/A	SIZE N/A	DRAWING NUMBER MKT-MLP08G	REV 4
MM		DO NOT SCALE DRAWING		SHEET 1 of 1	

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