



# FAN23SV04T

## 4 A Synchronous Buck Regulator for DDR Termination

### Features

- $V_{IN}$  Range: 7 V to 18 V Using Internal Linear Regulator for Bias
- $V_{IN}$  Range: 4.5 V to 5.5 V with  $V_{IN}/P_{VIN}/P_{VCC}$  Connected to Bypass Internal Regulator
- High Efficiency
- Continuous Output Current: 4 A
- MOSFETs  $R_{DS,ON}$  (Typical): HS: 9.67 m $\Omega$ , LS: 5.46 m $\Omega$
- Internal Linear Bias Regulator
- Internal  $V_{DDQ}$  Resistor Divider
- Excellent Line and Load Transient Response
- Output Voltage Range: 0.5 to 1.5 V
- Programmable Frequency: 200 kHz to 1.5 MHz
- Programmable Soft-Start
- Low Shutdown Current
- Adjustable Sourcing Current Limit
- Internal Boot Diode
- Thermal Shutdown
- Halogen and Lead Free, RoHS Compliant

### Applications

- Bus Termination
- Servers and Desktop Computers
- NVDC Notebooks, Netbooks
- Game Consoles

### Description

The FAN23SV04T is a highly efficient, synchronous buck regulator for use in tracking applications, such as DDR termination rails. The  $V_{DDQ}$  input includes an internal 2:1 resistive voltage divider to reduce total circuit size and component count. The regulator operates with an input range from 7 V to 18 V and supports up to 4 A load currents. The device can operate from a 5 V rail ( $\pm 10\%$ ) if  $V_{IN}$ ,  $P_{VIN}$ , and  $P_{VCC}$  are connected together to bypass the internal linear regulator.

This device utilizes Fairchild's constant on-time control architecture to provide excellent transient response and to maintain a relatively constant switching frequency.

Switching frequency and sourcing over-current protection can be programmed to provide a flexible solution for various applications.

Output over-current, and thermal shutdown protections help prevent damage during fault conditions. A hysteresis feature restarts the device when normal operating temperature is reached.

### Ordering Information

Part Number	Configuration	Operating Temperature Range	Output Current	Package
FAN23SV04TMPX	PWM Mode with $V_{DDQ}$ Tracking Input	-40 to 125°C	4 A	34-Lead, PQFN, 5.5 mm x 5.0 mm

### Typical Application Diagrams

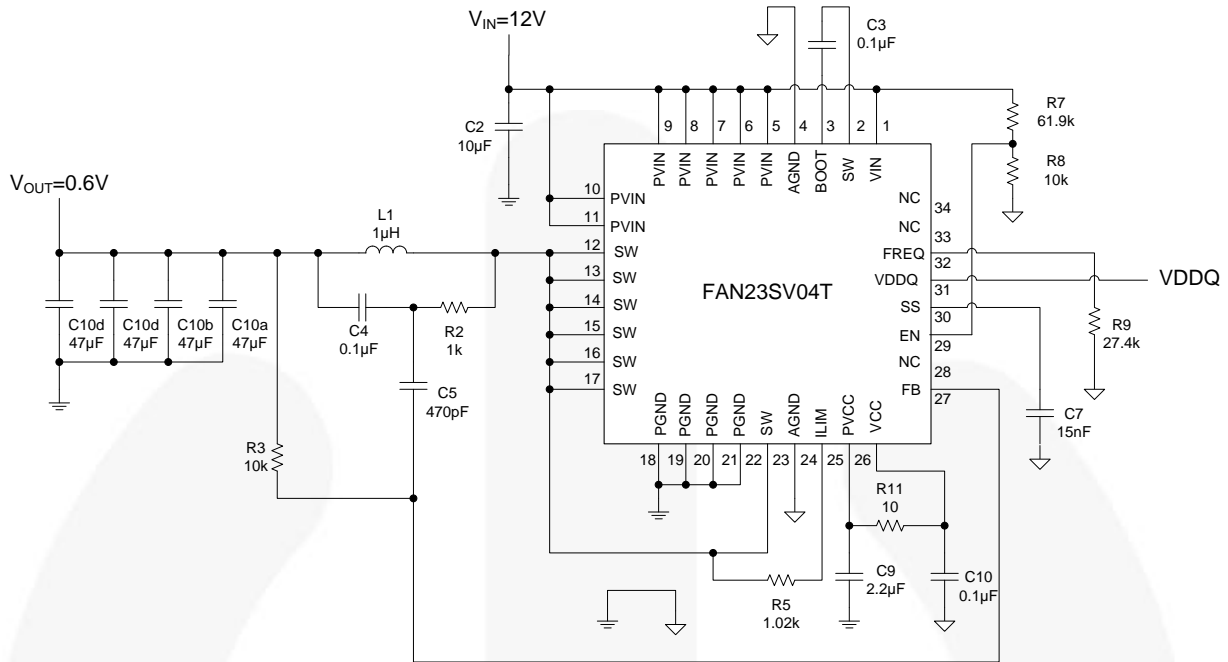


Figure 1. Typical Application with  $V_{IN} = 12\text{ V}$

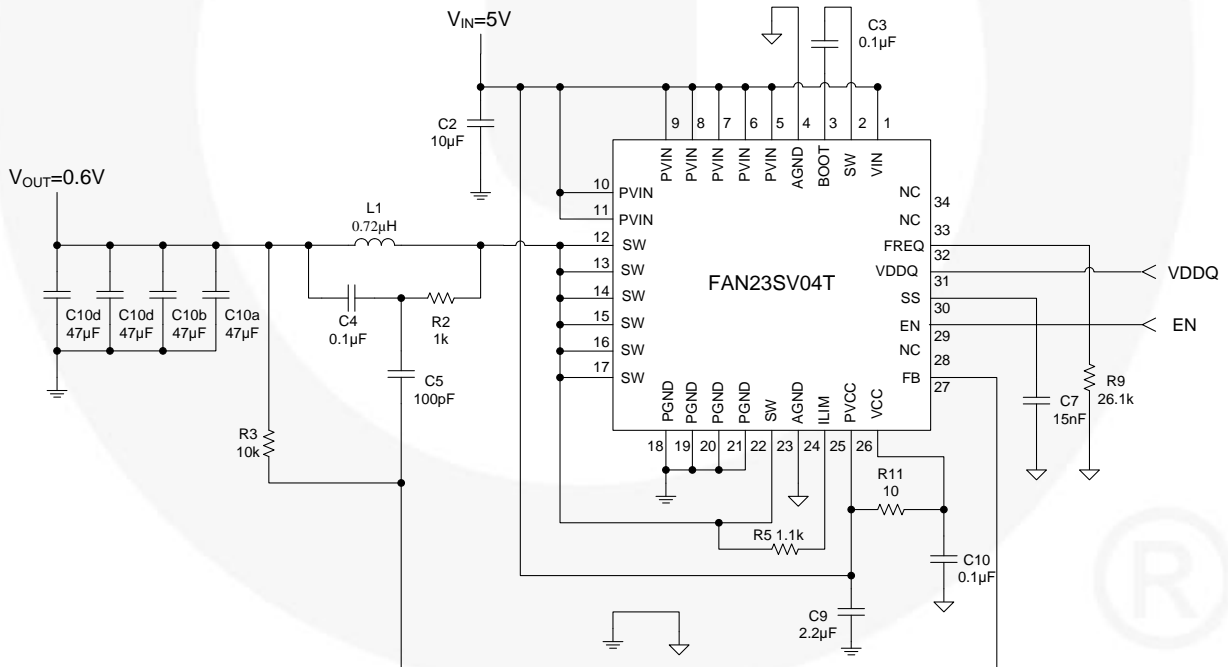


Figure 2. Typical Application with  $V_{IN} = 5\text{ V}$

### Functional Block Diagram

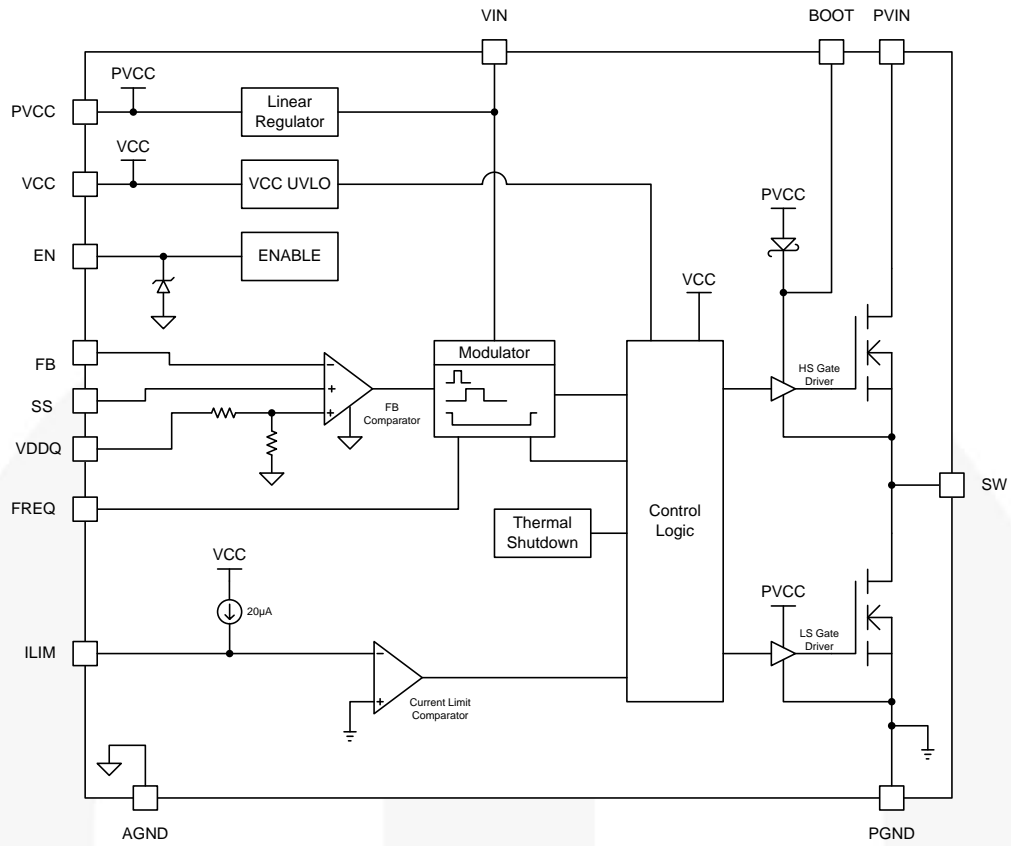


Figure 3. Block Diagram

## Pin Configuration

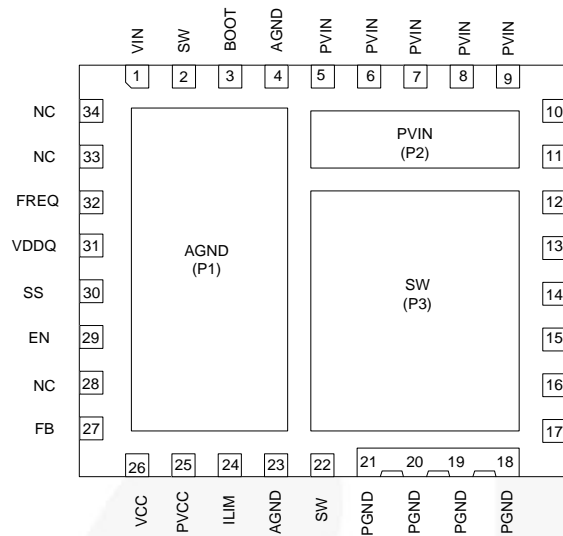


Figure 4. Bottom View

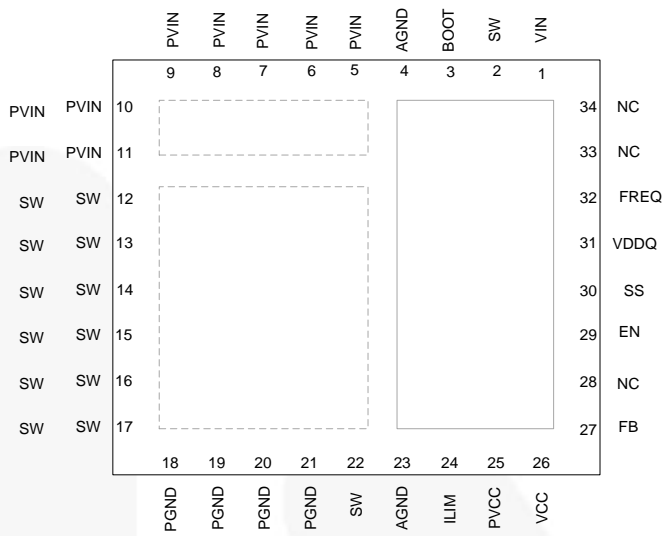


Figure 5. Top View

## Pin Definitions

Name	Pad / Pin	Description
PVIN	P2; 5-11	Power input for the power stage.
VIN	1	Power input to the linear regulator; used in the modulator for input voltage feed-forward.
PVCC	25	Power output of the linear regulator; directly supplies power for the low-side gate driver and boot diode. Can be connected to VIN and PVIN for operation from 5 V rail.
VCC	26	Power supply input for the controller.
PGND	18-21	Power ground for the low-side power MOSFET and for the low-side gate driver.
AGND	P1; 4, 23	Analog ground for the analog portions of the IC and for substrate.
SW	P3; 2, 12-17, 22	Switching node; junction between high-and low-side MOSFETs.
BOOT	3	Supply for high-side MOSFET gate driver. A capacitor from BOOT to SW supplies the charge to turn on the N-channel high-side MOSFET. During the freewheeling interval (low-side MOSFET on), the high-side capacitor is recharged by an internal diode connected to PVCC.
ILIM	24	Current limit. A resistor between ILIM and SW sets the current-limit threshold.
FB	27	Output voltage feedback to the modulator.
EN	29	Enable input to the IC. Pin must be driven logic high to enable, or logic low to disable.
SS	30	Soft-Start input to the modulator
VDDQ	31	External reference input to the modulator. The modulator regulates to half of the voltage at the VDDQ pin.
FREQ	32	On-time and frequency programming pin. Connect a resistor between FREQ and AGND to program on-time and switching frequency.
NC	28, 33-34	Leave pin open or connect to AGND.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Condition	Min.	Max.	Unit
V <sub>PVIN</sub>	Power Input	Referenced to PGND	-0.3	25.0	V
V <sub>IN</sub>	Modulator Input	Referenced to AGND	-0.3	25.0	V
V <sub>BOOT</sub>	Boot Voltage	Referenced to PVCC	-0.3	26.0	V
		Referenced to PVCC, <20 ns	-0.3	30.0	V
V <sub>SW</sub>	SW Voltage to GND	Referenced to PGND, AGND	-1	25	V
		Referenced to PGND, AGND < 20 ns	-5	25	V
V <sub>BOOT</sub>	Boot to SW Voltage	Referenced to SW	-0.3	6.0	V
	Boot to PGND	Referenced to PGND	-0.3	30	V
V <sub>PVCC</sub>	Gate Drive Supply Input	Referenced to PGND, AGND	-0.3	6.0	V
V <sub>VCC</sub>	Controller Supply Input	Referenced to PGND, AGND	-0.3	6.0	V
V <sub>ILIM</sub>	Current Limit Input	Referenced to AGND	-0.3	6.0	V
V <sub>FB</sub>	Output Voltage Feedback	Referenced to AGND	-0.3	6.0	V
V <sub>EN</sub>	Enable Input	Referenced to AGND	-0.3	6.0	V
V <sub>SS</sub>	Soft Start Input	Referenced to AGND	-0.3	6.0	V
V <sub>FREQ</sub>	Frequency Input	Referenced to AGND	-0.3	6.0	V
V <sub>DDQ</sub>	VDDQ Input	Referenced to AGND	-0.3	6.0	V
ESD	Electrostatic Discharge	Human Body Model, JESD22-A114 <sup>(1)</sup>		2000	V
		Charged Device Model, JESD22-C101 <sup>(2)</sup>		2500	V
T <sub>J</sub>	Junction Temperature			+150	°C
T <sub>STG</sub>	Storage Temperature		-55	+150	°C

### Note:

1. Exception for FB pin up to 350V
2. Exception for FB pin up to 500V

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Condition	Min.	Max.	Unit
V <sub>PVIN</sub>	Power Input	Referenced to PGND	7	18	V
V <sub>IN</sub>	Modulator Input	Referenced to AGND	7	18	V
T <sub>J</sub>	Junction Temperature		-40	+125	°C
I <sub>LOAD</sub>	Load Current	T <sub>A</sub> =25°C, No Airflow		6	A
V <sub>PVIN</sub> , V <sub>IN</sub> , V <sub>PVCC</sub>	PV <sub>IN</sub> , V <sub>IN</sub> , and Gate Drive Supply Input	V <sub>PVIN</sub> , V <sub>IN</sub> , V <sub>PVCC</sub> Connected for 5 V Rail Operation and Referenced to PGND, AGND	4.5	5.5	V

## Thermal Characteristics

The thermal characteristics were evaluated on a 4-layer pcb structure (1 oz/1 oz/1 oz/1 oz) measuring 7 cm x 7 cm).

Symbol	Parameter	Typ.	Unit
$\Theta_{JA}$	Thermal Resistance, Junction-to-Ambient	35	$^{\circ}\text{C}/\text{W}$
$\psi_{JC}$	Thermal Characterization Parameter, Junction-to-Top of Case	2.7	$^{\circ}\text{C}/\text{W}$
$\psi_{JPCB}$	Thermal Characterization Parameter, Junction-to-PCB	2.3	$^{\circ}\text{C}/\text{W}$

**Electrical Characteristics**Unless otherwise noted;  $V_{IN}=12\text{ V}$ ,  $V_{OUT}=0.6\text{ V}$ ,  $T_A=T_J=-40\text{ to }+125^\circ\text{C}$ .<sup>(5)</sup>

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Supply Current</b>						
$I_{VIN,SD}$	Shutdown Current	$E_N=0\text{ V}$			16	$\mu\text{A}$
$I_{VIN,Q}$	Quiescent Current	$E_N=5\text{ V}$ , Not Switching			1.8	$\text{mA}$
$I_{VIN,GateCharge}$	Gate Charge Current	$E_N=5\text{ V}$ , $f_{SW}=500\text{ kHz}$		10		$\text{mA}$
<b>Linear Regulator</b>						
$V_{REG}$	Regulator Output Voltage		4.75	5.00	5.25	$\text{V}$
$I_{REG}$	Regulator Current Limit		60			$\text{mA}$
<b>Reference, Feedback Comparator</b>						
$V_{FB}$	FB Voltage Threshold		590	596	602	$\text{mV}$
$V_{DDQ}$	$V_{DDQ}$ Pin Voltage Range		0		3	$\text{V}$
$I_{FB}$	FB Pin Bias Current		-100	0	100	$\text{nA}$
<b>Modulator</b>						
$t_{ON}$	On-Time Accuracy	$R_{FREQ}=56\text{ k}$ , $V_{IN}=10\text{ V}$ , $t_{ON}=250\text{ ns}$ , No Load	-20		20	%
$t_{OFF,MIN}$	Minimum SW Off-Time			320	374	$\text{ns}$
$D_{MIN}$	Minimum Duty Cycle	$FB=1\text{ V}$		0		%
<b>Soft-Start</b>						
$I_{SS}$	Soft-Start Current	$SS=0\text{ V}$	7	10	13	$\mu\text{A}$
<b>Current Limit</b>						
$I_{LIM}$	Valley Current Limit Accuracy	$T_A=T_J=25^\circ\text{C}$ , $I_{VALLEY}=4\text{ A}$	-10		10	%
$K_{LIM}$	$I_{LIM}$ Set-Point Scale Factor			233		
$I_{LIMTC}$	Temperature Coefficient			4000		$\text{ppm}/^\circ\text{C}$
<b>Enable</b>						
$V_{TH+}$	Rising Threshold		1.11	1.26	1.43	$\text{V}$
$V_{HYST}$	Hysteresis			122		$\text{mV}$
$V_{TH-}$	Falling Threshold		1.00	1.14	1.28	$\text{V}$
$V_{ENCLAMP}$	Enable Voltage Clamp	$I_{EN}=20\text{ }\mu\text{A}$	4.3	4.5		$\text{V}$
$I_{ENCLAMP}$	Clamp Current	$E_N=5\text{ V}$	24			$\mu\text{A}$
$I_{ENLK}$	Enable Pin Leakage	$E_N=1.2\text{ V}$			100	$\text{nA}$
$I_{ENLK}$	Enable Pin Leakage	$V_{EN}=5\text{ V}$			76	$\mu\text{A}$
<b>UVLO</b>						
$V_{ON}$	$V_{CC}$ Good Threshold Rising				4.4	$\text{V}$
$V_{HYS}$	Hysteresis Voltage			160		$\text{mV}$
<b>Thermal Shutdown</b>						
$T_{OFF}$	Thermal Shutdown Trip Point <sup>(3)</sup>			155		$^\circ\text{C}$
$T_{HYS}$	Hysteresis <sup>(3)</sup>			15		$^\circ\text{C}$
<b>Internal Bootstrap Diode</b>						
$V_{FBOOT}$	Forward Voltage	$I_F=10\text{ mA}$			0.6	$\text{V}$
$I_R$	Reverse Leakage	$V_R=5\text{ V}$			1000	$\mu\text{A}$
<b>MOSFETs</b>						
$R_{DS,ON,HS}$	Drain to Source On Resistance <sup>(4)</sup>	$V_{GS}=5\text{ V}$ , $I_D=30\text{ A}$ , $T_A=25^\circ\text{C}$		9.67		$\text{m}\Omega$
$R_{DS,ON,LS}$	Drain to Source On Resistance <sup>(4)</sup>	$V_{GS}=5\text{ V}$ , $I_D=30\text{ A}$ , $T_A=25^\circ\text{C}$		5.46		$\text{m}\Omega$

**Notes:**

- Guaranteed by design; not production tested.
- Typical  $R_{DS,ON}$  value is provided for reference only, and is derived from discrete MOSFET data.
- Device is 100% production tested at  $T_A=25^\circ\text{C}$ . Limits over that temperature are guaranteed by design.

## Typical Performance Characteristics

Tested using evaluation board circuit shown in Figure 1 with  $V_{IN}=12\text{ V}$ ,  $V_{OUT}=0.6\text{ V}$ ,  $f_{SW}=500\text{ kHz}$ ,  $T_A=25^\circ\text{C}$ , and no airflow; unless otherwise specified.

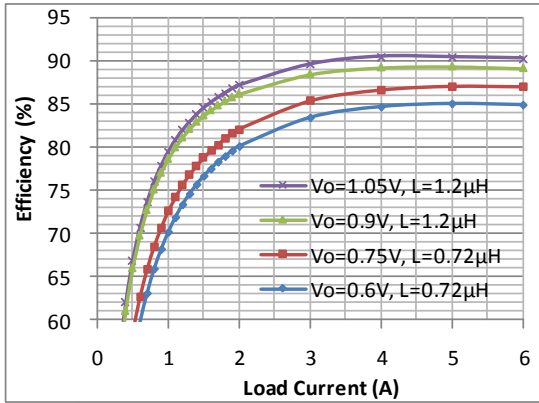


Figure 6. Efficiency vs. Load Current  $V_{IN}=12\text{ V}$  and  $f_{SW}=500\text{ kHz}$

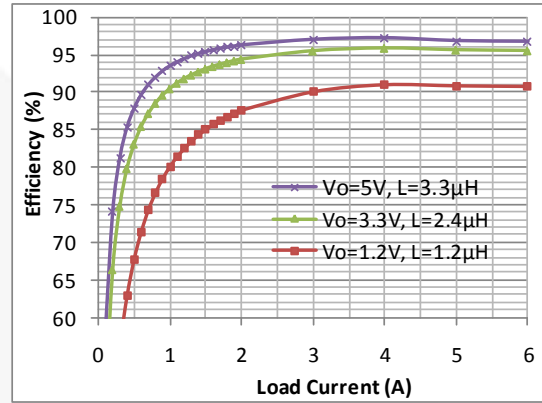


Figure 7. Efficiency vs. Load Current  $V_{IN}=12\text{ V}$  and  $f_{SW}=500\text{ kHz}$

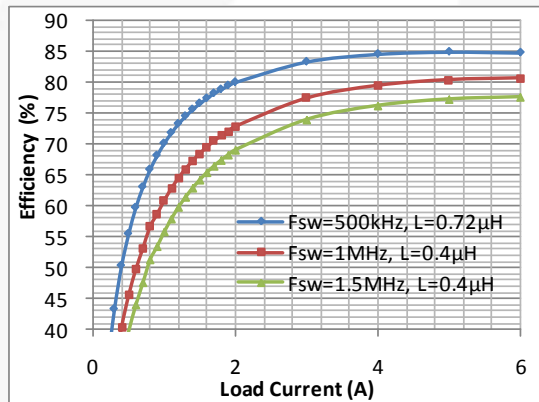


Figure 8. Efficiency vs. Load Current with  $V_{IN}=12\text{ V}$  and  $V_{OUT}=0.6\text{ V}$

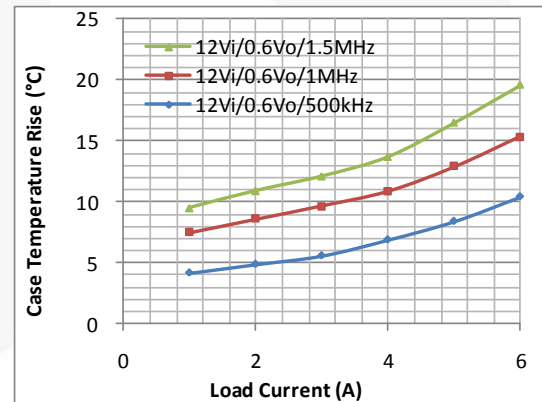


Figure 9. Case Temperature Rise vs. Load Current

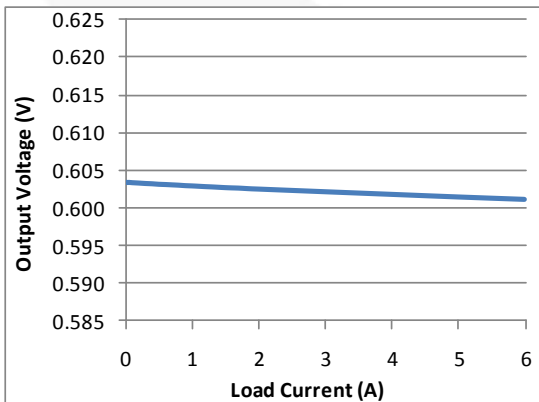


Figure 10. Load Regulation

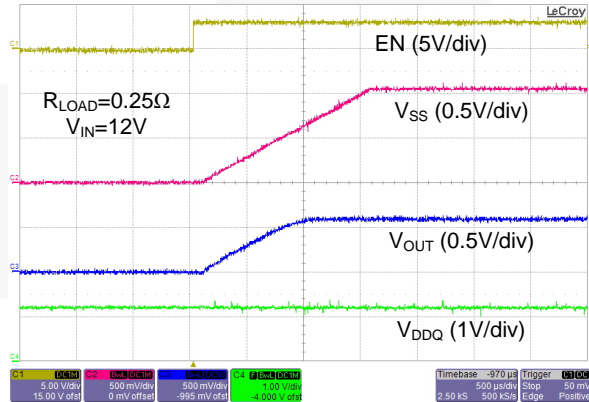


Figure 11. Startup Waveforms Using Soft-Start with 2.4 A Resistive Load



Typical Performance Characteristics (Continued)

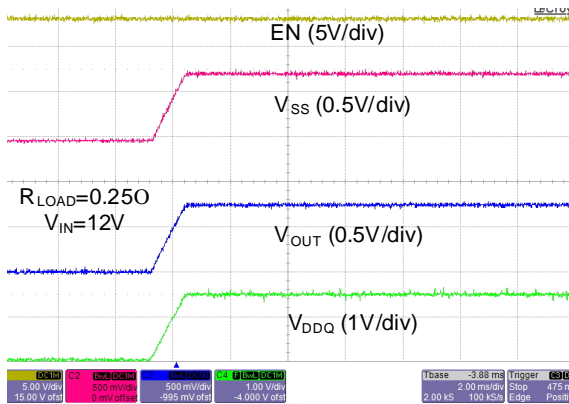


Figure 12. Startup Waveforms Tracking  $V_{DDQ}$  with 2.4 A Resistive Load

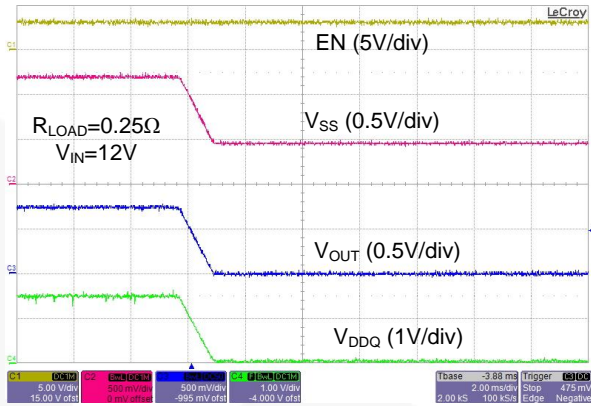


Figure 13. Shutdown Waveforms Tracking  $V_{DDQ}$  with 2.4 A Resistive Load

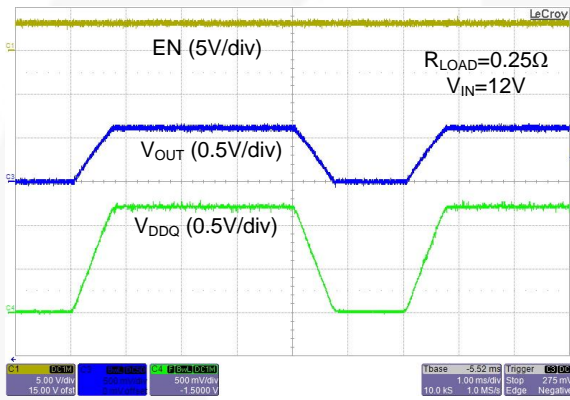


Figure 14. Tracking Operation with Variable  $V_{DDQ}$  Reference Input

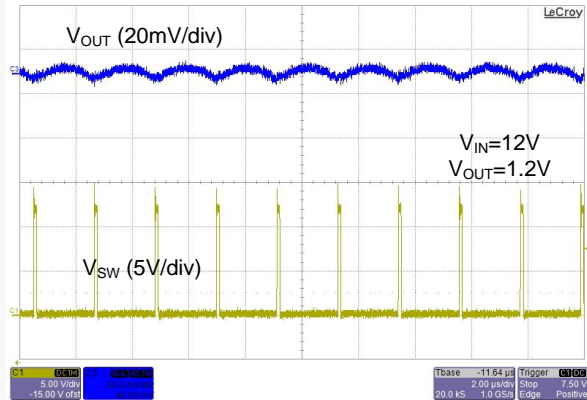


Figure 15. Static Output Ripple with No Load

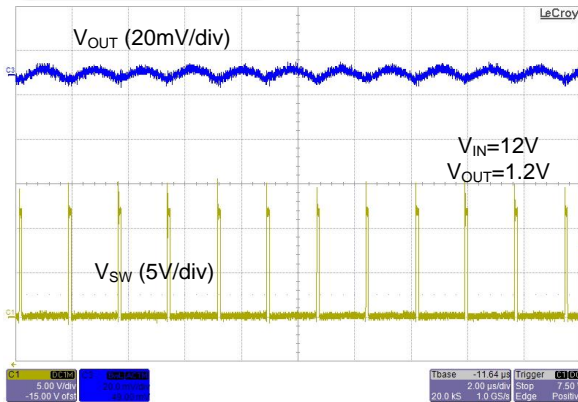


Figure 16. Static Output Ripple with 4 A Load Current

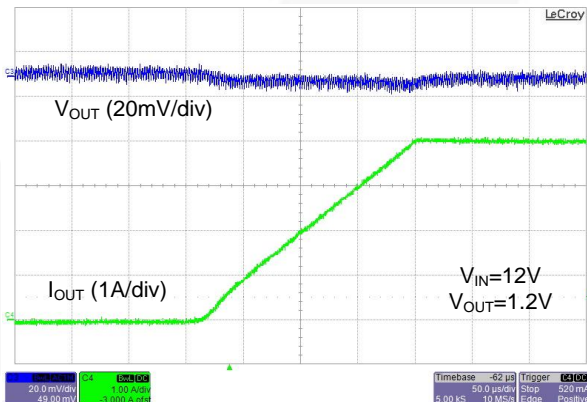
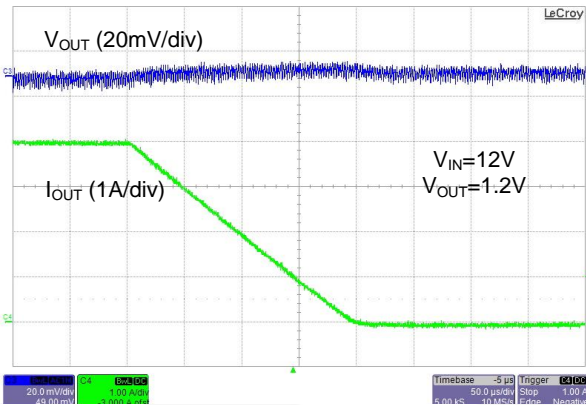
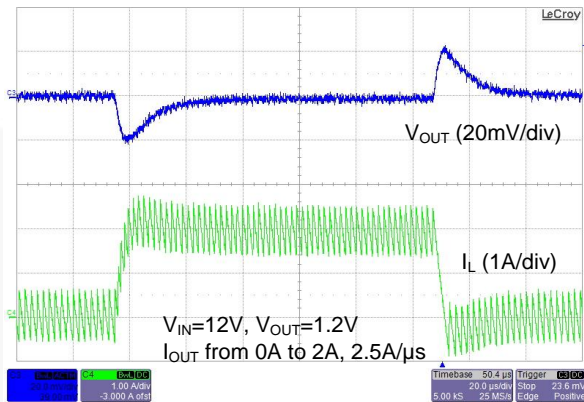


Figure 17. Operation as Load Changes from 0 A to 4 A

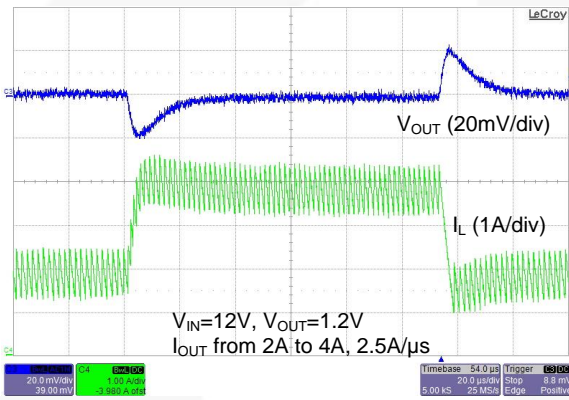
## Typical Performance Characteristics (Continued)



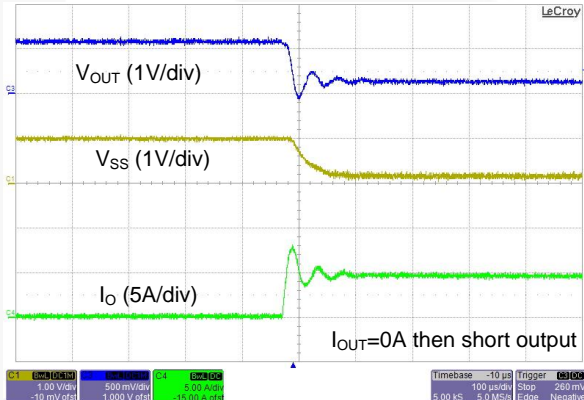
**Figure 18. Operation as Load Changes from 4 A to 0 A**



**Figure 19. Load Transient from 0% to 50% Load Current**



**Figure 20. Load Transient from 50% to 100% Load Current**



**Figure 21. Over-Current Protection with Heavy Load**

## Circuit Operation

The FAN23SV04T uses a constant-on-time modulation architecture with a  $V_{IN}$  feed-forward input to accommodate a wide  $V_{IN}$  range. This method provides fixed switching frequency ( $f_{SW}$ ) operation when the inductor operates in Continuous Conduction Mode (CCM). Additional benefits include excellent line and load transient response, cycle-by-cycle current limiting, and elimination of loop compensation requirements.

At the beginning of each cycle, FAN23SV04T turns on the high-side MOSFET (HS) for a fixed duration ( $t_{ON}$ ). At the end of  $t_{ON}$ , HS turns off for a duration ( $t_{OFF}$ ) determined by the operating conditions. Once the FB voltage ( $V_{FB}$ ) falls below the reference voltage ( $V_{REF}$ ), a new switching cycle begins.

The modulator provides a minimum off-time ( $t_{OFF-MIN}$ ) of 250 ns to provide a guaranteed interval for low-side MOSFET (LS) current sensing and PFM operation.  $t_{OFF-MIN}$  provides stability against multiple pulsing and limits maximum switching frequency during transient events.

### Enable

The enable pin can be driven with an external logic signal, connected to a resistive divider from  $PV_{IN}/V_{in}$  to ground to create an Under-Voltage Lockout (UVLO) based on the  $PV_{IN}/V_{IN}$  supply, or connected to  $PV_{IN}/V_{IN}$  through a single resistor to auto-enable while operating within the EN pin internal clamp current sink capability.

The EN pin can be directly driven by logic voltages of 5 V, 3.3 V, 2.5 V, etc. If the EN pin is driven by 5 V logic, a small current flows into the pin when the EN pin voltage exceeds the internal clamp voltage of 4.3 V. To eliminate clamp current flowing into the EN pin use a voltage divider to limit the EN pin voltage to < 4 V.

To implement the UVLO function based on  $PV_{IN}/V_{IN}$  voltage level, select values for R7 and R8 in Figure 1 such that the tap point reaches 1.26 V when  $V_{IN}$  reaches the desired startup level using the following equation:

$$R7 = R8 \left( \frac{V_{IN,on}}{V_{EN,on}} - 1 \right) \quad (1)$$

where  $V_{IN,on}$  is the input voltage for startup and  $V_{EN,on}$  is the EN pin rising threshold of 1.26 V. With R8 selected as 10 k $\Omega$ , and  $V_{IN,on}=9$  V the value of R7 is 61.9 k $\Omega$ .

The EN pin can be pulled high with a single resistor connected from  $V_{IN}$  to the EN pin. With  $V_{IN} > 5.5$  V a series resistor is required to limit the current flow into the EN pin clamp to less than 24  $\mu$ A to keep the internal clamp within normal operating range. The resistor value can be calculated from the following equation:

$$R_{EN} > \frac{V_{IN,max} - V_{EN,clamp,min}}{22\mu A} \quad (2)$$

### Constant On-Time Modulation

The FAN23SV04T uses a constant on-time modulation technique, in which the HS MOSFET is turned on for a fixed time, set by the modulator, in response to the input

voltage and the frequency-setting resistor. This on-time is proportional to the desired output voltage, divided by the input voltage. With this proportionality, the frequency is essentially constant over the load range where inductor current is continuous.

For a buck converter in Continuous-Conduction Mode (CCM), the switching frequency  $f_{SW}$  is expressed as:

$$f_{SW} = \frac{V_{OUT}}{V_{IN} \cdot t_{ON}} \quad (3)$$

The on-time generator sets the on-time ( $t_{ON}$ ) for the high-side MOSFET, which results in the switching frequency of the regulator during steady-state operation. To maintain a relatively constant switching frequency over a wide range of input conditions, the input voltage information is fed into the on-time generator.

$t_{ON}$  is determined by:

$$t_{ON} = \frac{C_{LON}}{I_{LON}} \cdot 2V \quad (4)$$

where  $I_{LON}$  is:

$$I_{LON} = \frac{1}{10} \cdot \frac{V_{IN}}{R_{FREQ}} \quad (5)$$

where  $R_{FREQ}$  is the frequency-setting resistor described in the Setting Switching Frequency section;  $C_{LON}$  is the internal 2.2 pF capacitor; and  $I_{LON}$  is the  $V_{IN}$  feed-forward current that generates the on-time.

The FAN23SV04T implements open-circuit detection on the FREQ pin to protect the output from an infinitely long on-time. In the event the FREQ pin is left floating, switching of the regulator is disabled. The FAN23SV04T is designed for a  $V_{IN}$  input range 7 to 18 V and  $f_{SW}$  from 200 kHz to 1.5 MHz, resulting in an  $I_{LON}$  ratio of 1 to 16.

As the ratio of  $V_{OUT}$  to  $V_{IN}$  increases,  $t_{OFF,min}$  introduces a limit on the maximum switching frequency as calculated in the following equation, where the factor 1.2 is included in the denominator to provide some headroom for transient operation:

$$f_{SW} < \frac{\left(1 - \frac{V_{OUT}}{V_{IN,min}}\right)}{1.2 \cdot t_{OFF,min}} \quad (6)$$

### VDDQ

This pin is connected to the  $V_{DDQ}$  supply, which the FAN23SV04T must track during startup and produce an output ( $V_{TT}$ ) equal to half of  $V_{DDQ}$  in steady-state conditions. To accomplish this, the  $V_{DDQ}$  pin has an internal resistor divider to AGND that provides a reference voltage equal to  $V_{DDQ}/2$  at the positive input of the FB comparator.

### Soft-Start (SS)

A conventional soft-start ramp is implemented to provide a controlled startup sequence of the output voltage. A current is generated on the SS pin to charge an external capacitor. The lesser of the voltage on the SS pin and the reference voltage is used for output regulation.

During normal operation, the SS voltage is clamped to 400 mV above the FB voltage. The clamp voltage drops to 40 mV during an overload condition (when  $V_{FB}$  is  $\leq$  400 mV) to allow the converter to recover using the soft-start ramp once the overload condition is removed. There is no on-time modulation during normal soft-start or when recovering from an overload condition.

The nominal startup time is programmable through an internal current source charging the external soft-start capacitor  $C_{SS}$ :

$$C_{SS} = \frac{I_{SS} \cdot t_{SS}}{V_{REF}} \quad (7)$$

where:

$C_{SS}$  = External soft-start programming capacitor;

$I_{SS}$  = Internal soft-start charging current source, 10  $\mu$ A;

$t_{SS}$  = Soft-start time; and

$V_{REF}$  = VDDQ/2.

For example; for 1 ms startup time,  $C_{SS}$ =15 nF.

The soft-start option can be used for ratiometric tracking.

When EN is LOW, the soft-start capacitor is discharged.

### Internal Linear Regulator

The FAN23SV04T includes a linear regulator to facilitate single-supply operation for self-biased applications. PVCC is the linear regulator output and supplies power to the internal gate drivers. The PVCC pin should be bypassed with a 2.2  $\mu$ F ceramic capacitor. The device can operate from a 5 V rail if the  $V_{IN}$ ,  $P_{VIN}$ , and  $P_{VCC}$  pins are connected together to bypass the internal linear regulator.

### V<sub>CC</sub> Bias Supply and UVLO

The  $V_{CC}$  rail supplies power to the controller. It is generally connected to the PVCC rail through a low-pass filter of a 10  $\Omega$  resistor and 0.1  $\mu$ F capacitor to minimize any noise sources from the driver supply.

An Under-Voltage Lockout (UVLO) circuit monitors the  $V_{CC}$  voltage to ensure proper operation. Once the  $V_{CC}$  voltage is above the UVLO threshold, the part begins operation after an initialization routine of 50  $\mu$ s. There is no UVLO circuitry on either the PVCC or  $V_{IN}$  rails.

### Over-Current Protection (OCP)

The FAN23SV04T uses current information through the LS to implement valley-current limiting. While an OC event is detected, the HS is prevented from turning on and the LS is kept on until the current falls below the user-defined set point. Once the current is below the set point, the HS is allowed to turn on.

The ILIM pin has an open detection circuit to provide protection against operation without a current limit.

### Over-Temperature Protection (OTP)

FAN23SV04T incorporates an over-temperature protection circuit that disables the converter when the die temperature reaches 155°C. The IC restarts when the die temperature falls below 140°C.

## Application Information

### Stability

Constant on-time stability consists of two parameters: stability criterion and sufficient signal at  $V_{FB}$ .

Stability criterion is given by:

$$R_{ESR} \cdot C_{OUT} \gg \frac{t_{ON}}{2} \quad (8)$$

Sufficient signal requirement is given by:

$$\Delta I_{IND} \cdot R_{ESR} > \Delta V_{FB} \quad (9)$$

where  $\Delta I_{IND}$  is the inductor current ripple and  $\Delta V_{FB}$  is the ripple voltage on  $V_{FB}$ , which should be  $\geq$ 12 mV.

In certain applications, especially designs utilizing only ceramic output capacitors, there may not be sufficient ripple magnitude available on the feedback pin for stable operation. In this case, an external circuit, such as R2-C4-C5 shown in Figure 1, can be added to inject ripple voltage into the FB pin.

There are some specific considerations when selecting the RCC ripple injector circuit. For typical applications, the value of C4 can be selected as 0.1  $\mu$ F and approximate values for R2 and C5 can be determined using the following equations.

R2 must be small enough to develop 12 mV of ripple:

$$R2 < \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN} \cdot 0.012V \cdot C4 \cdot f_{SW}} \quad (10)$$

R2 must also be selected such that the R2C4 time constant enables stable operation:

$$R2 < \frac{0.33 \cdot 2\pi \cdot f_{SW} \cdot L_{OUT} \cdot C_{OUT}}{C4} \quad (11)$$

The minimum value of C5 can be selected to minimize the capacitive component of ripple appearing on the feedback pin:

$$C5_{MIN} = \frac{L_{OUT} \cdot C_{OUT}}{R2 \cdot R3 \cdot C4} \quad (12)$$

Using the minimum value of C5 generally offers the best transient response, and 100 pF is a good initial value in many applications. However, under some operating conditions excessive pulse jitter may be observed. To reduce jitter and improve stability, the value of C5 can be increased:

$$C5 \geq 2 \cdot C5_{MIN} \quad (13)$$

### 5 V PV<sub>CC</sub>

The PV<sub>CC</sub> is the output of the internal regulator that supplies power to the drivers and  $V_{CC}$ . It is crucial to keep this pin decoupled to PGND with a  $\geq$ 1  $\mu$ F X5R or X7R ceramic capacitor. Because  $V_{CC}$  powers the internal analog circuit, it is filtered from PV<sub>CC</sub> with a 10  $\Omega$  resistor and 0.1  $\mu$ F X7R decoupling ceramic capacitor to AGND.

## Setting the Output Voltage ( $V_{OUT}$ )

The output voltage,  $V_{OUT}$ , is regulated by initiating a high-side MOSFET on-time interval when the valley of the divided output voltage appearing at the FB pin reaches  $V_{REF}$ . Since this method regulates at the valley of the output ripple voltage, the actual DC output voltage on  $V_{OUT}$  is offset from the programmed output voltage by the average value of the output ripple voltage. The output  $V_{OUT}$  setting of the regulator can be determined using the following equation:

$$V_{OUT} = \frac{V_{DDQ}}{2} \quad (14)$$

where  $V_{DDQ}$  is the voltage applied to pin 31.

For example; if  $V_{DDQ}=1.2\text{ V}$  then  $V_{OUT}=600\text{ mV}$ .  $V_{FB}$  is trimmed to a value of 596 mV when  $V_{DDQ}=V_{REF}=600\text{ mV}$ . The final output voltage, including the effect of the output ripple voltage, can be approximated by:

$$V_{OUT} = V_{FB} * \left[ \frac{V_{rip}}{2} \right] \quad (15)$$

## Setting the Switching Frequency ( $f_{sw}$ )

$f_{sw}$  is programmed through external  $R_{FREQ}$  as follows:

$$R_{FREQ} = \frac{V_{OUT}}{20 * C_{TON} * f_{sw}} \quad (16)$$

where  $C_{TON}=2.2\text{ pF}$ . For example; for  $f_{sw}=500\text{ kHz}$  and  $V_{OUT}=0.6\text{ V}$ , then select a standard resistor value for  $R_{FREQ}=27.4\text{ k}\Omega$ .

## Inductor Selection

The inductor is typically selected based on the ripple current ( $\Delta I_L$ ), which is approximately 25% to 45% of the maximum DC load. The inductor current rating should be selected such that the saturation and heating current ratings exceed the intended currents encountered in the application over the expected temperature range of operation. Regulators that require fast transient response use smaller inductance and higher current ripple; while regulators that require higher efficiency keep ripple current on the low side.

The inductor value is given by:

$$L = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{\Delta I_L \cdot f_{sw}} \quad (17)$$

For example: for 12 V  $V_{IN}$ , 0.6 V  $V_{OUT}$ , 4 A load, 25%  $I_L$ , and 500 kHz  $f_{sw}$ ; L is calculated to be 1.1  $\mu\text{H}$  and a standard value of 1  $\mu\text{H}$  is selected.

## Input Capacitor Selection

Input capacitor  $C_{IN}$  is selected based on voltage rating, RMS current  $I_{CIN(RMS)}$  rating, and capacitance. For capacitors with DC voltage bias derating, such as ceramic capacitors, higher rating is strongly recommended. RMS current rating is given by:

$$I_{CIN(RMS)} = I_{LOAD-MAX} \cdot \sqrt{D \cdot (1 - D)} \quad (18)$$

where  $I_{LOAD-MAX}$  is the maximum load current and D is the duty cycle  $V_{OUT}/V_{IN}$ . The maximum  $I_{CIN(RMS)}$  occurs at 50% duty cycle.

The capacitance is given by:

$$C_{IN} = \frac{I_{LOAD-MAX} \cdot D \cdot (1 - D)}{f_{sw} \cdot \Delta V_{IN}} \quad (19)$$

where  $\Delta V_{IN}$  is input voltage ripple, normally 1% of  $V_{IN}$ .

For example: for  $V_{IN}=12\text{ V}$ ,  $\Delta V_{IN}=120\text{ mV}$ ,  $V_{OUT}=0.6\text{ V}$ , 4 A load, and  $f_{sw}=950\text{ kHz}$ ; then  $C_{IN}$  is calculated as 1.7  $\mu\text{F}$ , select a single 10  $\mu\text{F}$ , 25 V-rated ceramic capacitor with X7R or similar dielectric, recognizing that the capacitor DC bias characteristic indicates that the capacitance value falls approximately 40% at  $V_{IN}=12\text{ V}$ .

## Output Capacitor Selection

Output capacitor  $C_{OUT}$  is also selected based on voltage rating, RMS current  $I_{CIN}$  (RMS) rating, and capacitance. For capacitors with DC voltage bias derating, such as ceramic capacitors, higher rating is recommended.

When calculating  $C_{OUT}$ , usually the dominant requirement is the current load step transient. If the unloading transient requirement ( $I_{OUT}$  transitioning from HIGH to LOW), is satisfied, the load transient ( $I_{OUT}$  transitioning LOW to HIGH), is also usually satisfied. The unloading  $C_{OUT}$  calculation, assuming  $C_{OUT}$  has negligible parasitic resistance and inductance in the circuit path, is given by:

$$C_{OUT} = L \cdot \frac{I_{LEVEL1}^2 - I_{LEVEL2}^2}{(V_{OUT} + \Delta V_{OUT})^2 - V_{OUT}^2} \quad (20)$$

where  $I_{level1}$  and  $I_{level2}$  are current levels before and after load steps, and  $\Delta V_{OUT}$  is the voltage overshoot, usually specified at 3 to 5%.

For example: for  $V_{IN}=12\text{ V}$ ,  $V_{OUT}=0.6\text{ V}$ ,  $I_{LEVEL1}=3\text{ A}$ ,  $I_{LEVEL2}=2\text{ A}$ ,  $f_{sw}=500\text{ kHz}$ ,  $L_{OUT}=1\text{ }\mu\text{H}$ , and 4.0%  $\Delta V_{OUT}$  overshoot of 24 mV; the  $C_{OUT}$  value is calculated to be 170  $\mu\text{F}$ , and four 47  $\mu\text{F}$ , 6.3 V-rated X5R ceramic capacitors may be used. This equation assumes that the load current rises instantaneously; with reduced current slew rate, the value for  $C_{OUT}$  can be reduced.

## Setting the Current Limit

Current limit is implemented by sensing the inductor valley current across the LS  $R_{DS(ON)}$  during the LS on-time. The current-limit comparator prevents a new on-time from starting until the valley current is less than the current limit.

The set point is configured by connecting a resistor from the ILIM pin to the SW pin. A trimmed current of approximately 20  $\mu\text{A}$  is output onto the ILIM pin, which creates a voltage across the resistor. When the voltage on ILIM goes negative, an over-current condition is detected.

The current flowing out of the ILIM pin through  $R_{ILIM}$  is trimmed to compensate for both the  $R_{DS(ON)}$  of the LS MOSFET and the offset voltage of the current limit comparator.  $R_{ILIM}$  is calculated by:

$$R_{ILIM} = 1.02 * K_{ILIM} * I_{VALLEY} \quad (21)$$

where  $K_{ILIM}$  is the current source scale factor equal to the average  $R_{DS,ON}$  of the LS MOSFET divided by the average ILIM pin current of 20  $\mu$ A, and  $I_{VALLEY}$  is the inductor valley current when the current limit threshold is reached. The factor 1.01 accounts for the temperature offset of the LS MOSFET compared to control circuit (approximately 5°C), and the approximate increase in the  $R_{DS,on}$  of the LS MOSFET of 4000 ppm/°C.

With the constant on-time architecture, HS is always turned on for a fixed on-time. This determines the peak-to-peak inductor current.

Current ripple  $\Delta I$  is given by:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) * t_{ON}}{L} \quad (22)$$

From the equation above, the worst-case ripple occurs during an output short circuit (where  $V_{OUT}$  is 0 V). This should be taken into account when selecting the current limit set point.

The FAN23SV04T uses valley-current sensing. The current limit ( $I_{ILIM}$ ) set point is the valley ( $I_{VALLEY}$ ).

The valley current level for calculating  $R_{ILIM}$  is given by:

$$I_{VALLEY} = I_{LOAD(CL)} - \frac{\Delta I_L}{2} \quad (23)$$

where  $I_{LOAD(CL)}$  is the DC load current when the current limit threshold is reached.

For example: in a converter designed for 4 A steady-state operation and 1 A current ripple, the current-limit threshold could be selected at 120% of  $I_{LOAD(SS)}$  to accommodate transient operation and inductor value decrease under loading. As a result;  $I_{LOAD(SS)}$  is 4.8 A,  $I_{VALLEY}$ =4.3 A, and  $R_{ILIM}$  is selected as the standard value of 1.02 k $\Omega$ .

## Boot Resistor

In some applications, especially with higher input voltage, the  $V_{SW}$  ring voltage may exceed the derating guidelines of 80% to 90% of absolute rating for  $V_{SW}$ . In this situation, a resistor can be connected in series with the boot capacitor (C3 in Figure 1) to reduce the turn-on speed of the high-side MOSFET to reduce the amplitude of the  $V_{SW}$  ring voltage.

## PCB (Printed Circuit Board) Layout Guidelines

The following should be considered before beginning a PCB layout using the FAN23SV04T. A sample PCB layout from the evaluation board following the layout guidelines is shown in Figure 22 - Figure 25.

Power components consisting of the input capacitors, output capacitors, inductor, and FAN23SV04T device should be on a common side of the PCB in close proximity to each other and connected using surface copper.

Sensitive analog components; including SS, FB, ILIM, FREQ, and EN; should be placed away from the high-voltage switching circuits, such as SW and BOOT, and connected to their respective pins with short traces.

The inner PCB layer closest to the FAN23SV04T device should have Power Ground (PGND) under the power-processing portion of the device (PVIN, SW, and PGND). This inner PCB layer should have a separate Analog Ground (AGND) under the P1 pad and the associated analog components. AGND and PGND should be connected together near the IC between PGND pins 18-21 and AGND pin 23, which connects to P1 thermal pad.

The AGND thermal pad (P1) should be connected to AGND plane on the inner layer using four 0.25 mm vias spread under the pad. No vias are included under PVIN (P2) and SW (P3) to maintain the PGND plane under the power circuitry intact.

Power circuit loops that carry high currents should be arranged to minimize the loop area. Primary focus should be directed to minimize the loop for current flow from the input capacitor to PVIN, through the internal MOSFETs, and returning to the input capacitor. The input capacitor should be placed as close to the PVIN terminals as possible.

The current return path from PGND at the low-side MOSFET source to the negative terminal of the input capacitor can be routed under the inductor and also through vias that connect the input capacitor and low-side MOSFET source to the PGND region under the power portion of the IC.

The SW node trace that connects the source of the high-side MOSFET and the drain of the low-side MOSFET to the inductor should be short and wide.

To control the voltage across the output capacitor, the output voltage divider should be located close to the FB pin, with the upper FB voltage divider resistor connected to the positive side of the output capacitor, and the bottom resistor should be connected to the AGND portion of the FAN23SV04T device.

When using ceramic capacitor solutions with external ramp injection circuitry (R2, C4, C5 in Figure 1), R2 and C4 should be connected near the inductor and coupling capacitor C5 should be placed near the FB pin to minimize FB pin trace length.

Decoupling capacitors for PVCC and VCC should be located close to their respective device pins.

SW node connections to BOOT, ILIM, and ripple injection resistor R2 should be through separate traces.

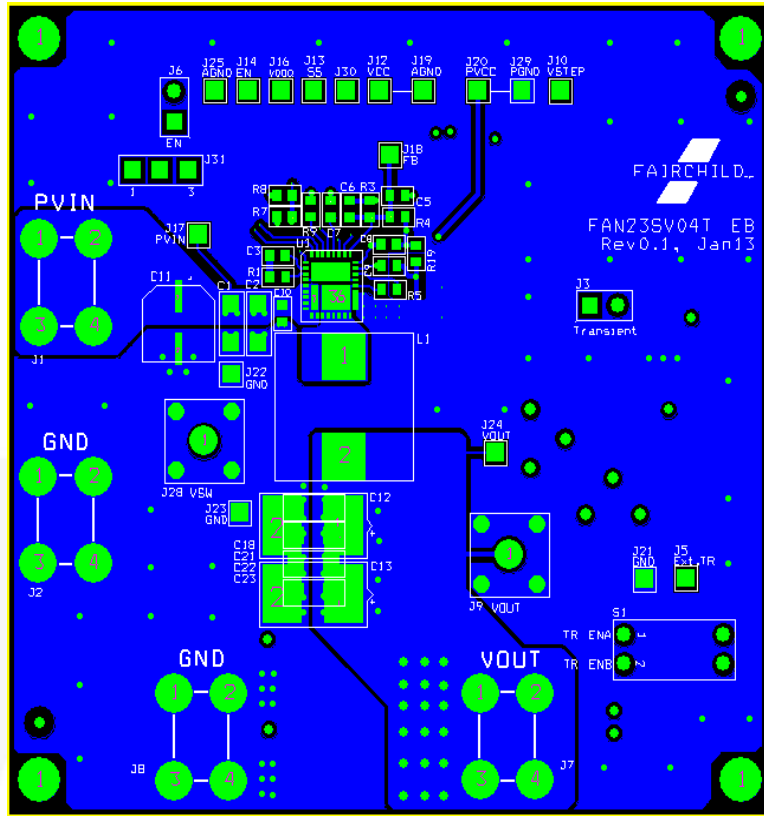


Figure 22. Evaluation Board Top Layer Copper

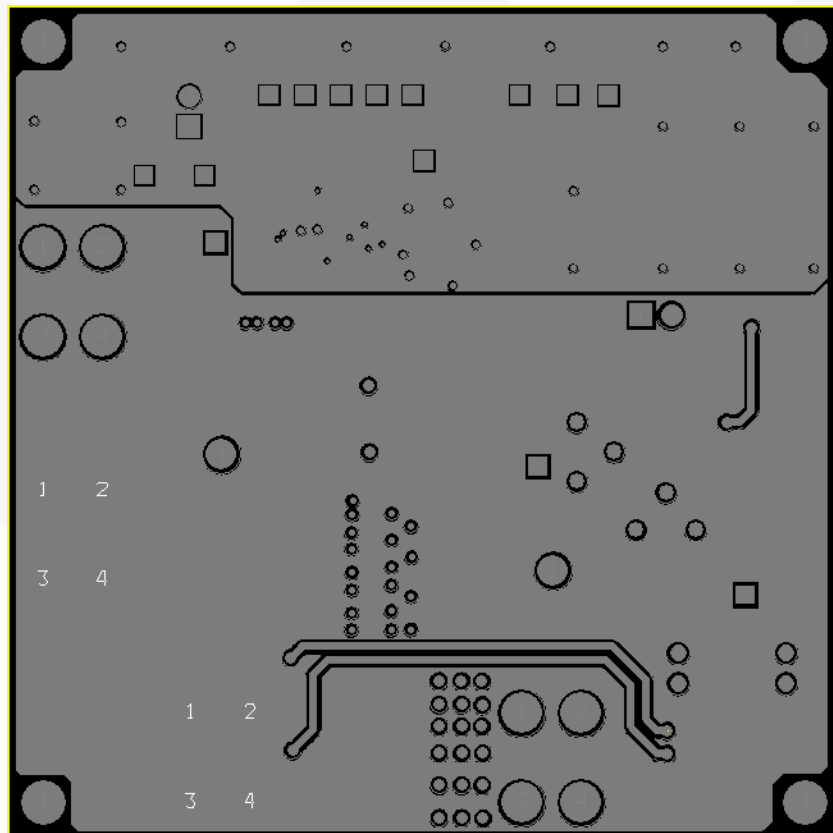


Figure 23. Evaluation Board Inner Layer 1 Copper

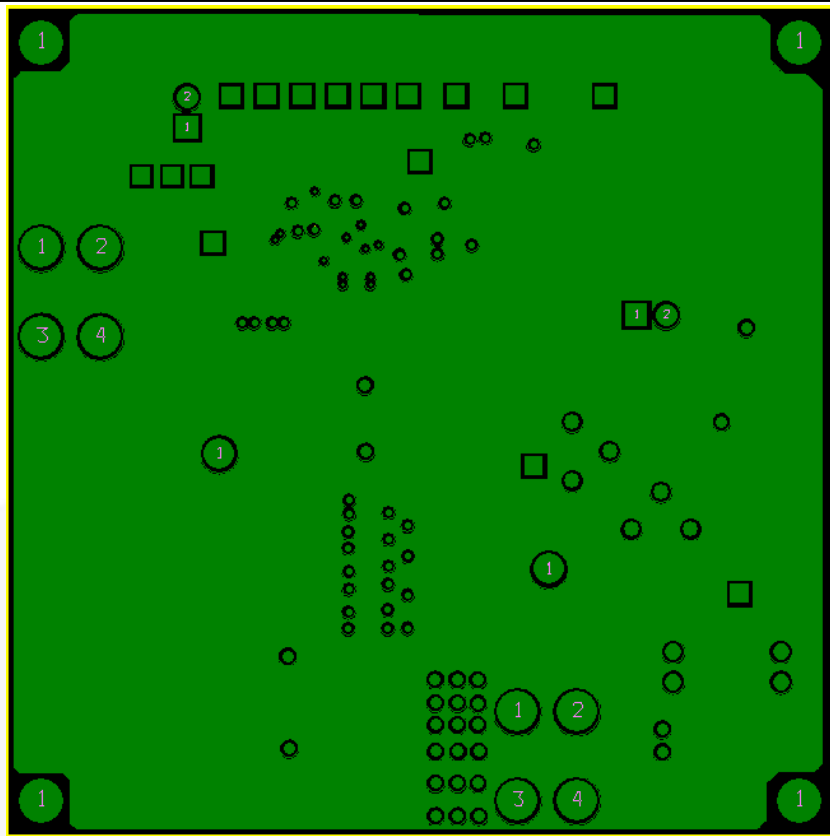


Figure 24. Evaluation Board Inner Layer 2 Copper

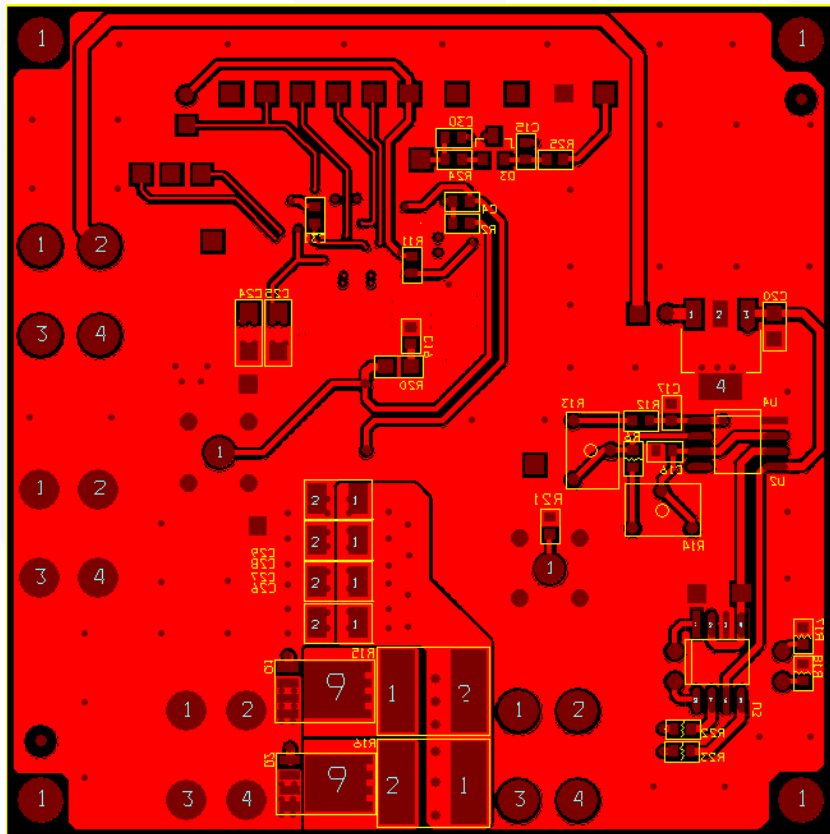
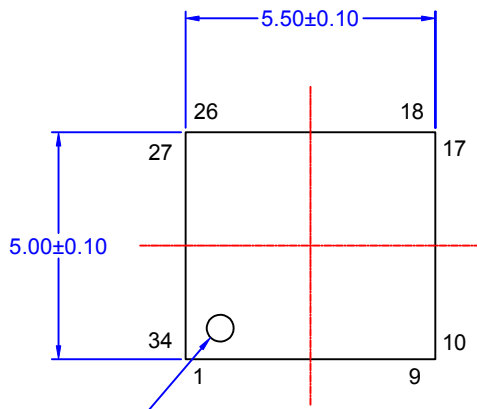


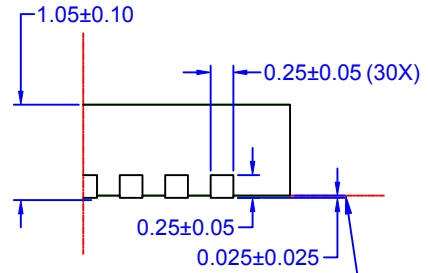
Figure 25. Evaluation Board Bottom Layer Copper





PIN#1  
INDICATOR

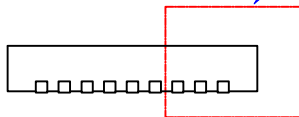
**TOP VIEW**



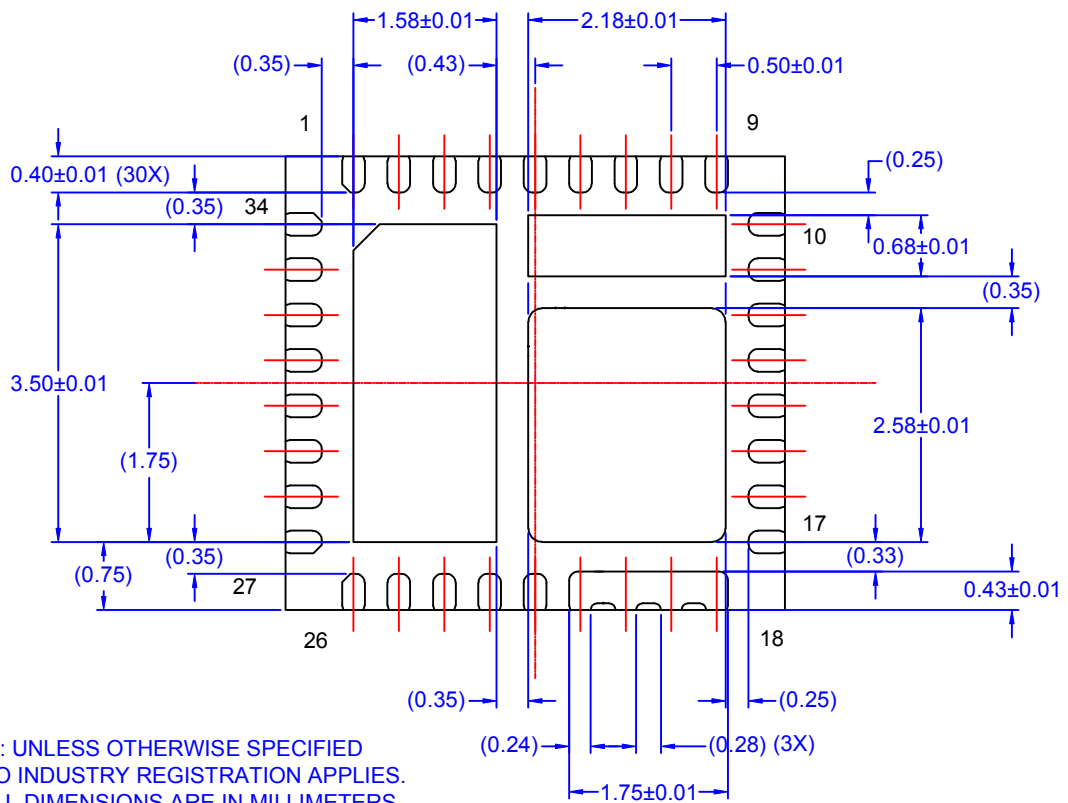
**DETAIL 'A'**  
SCALE: 2:1

SEATING  
PLANE

SEE  
DETAIL 'A'

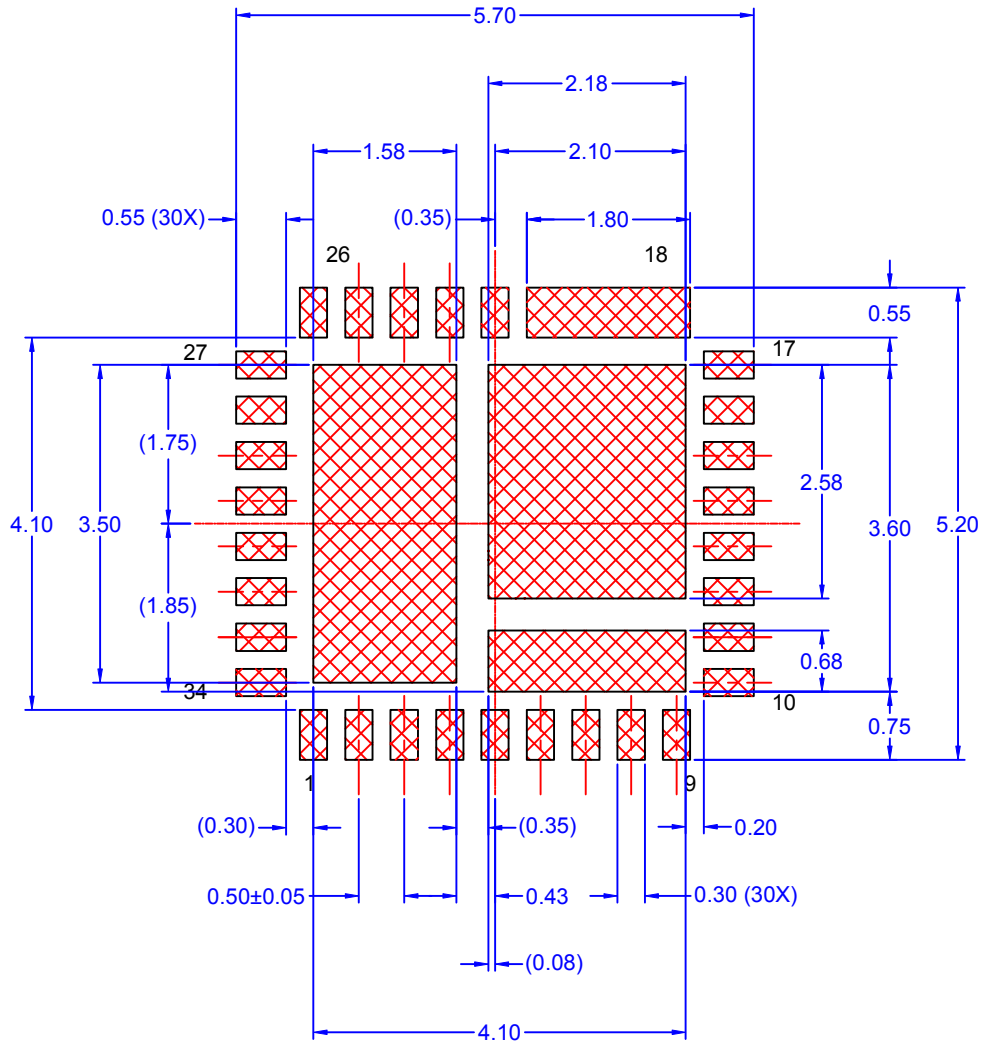


**FRONT VIEW**



**BOTTOM VIEW**

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) NO INDUSTRY REGISTRATION APPLIES.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - E) DRAWING FILE NAME: MKT-PQFN34AREV2
  - F) FAIRCHILD SEMICONDUCTOR



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| EfficientMax™            | MicroPak™                                      | SPM®                                  | Ultra FRFET™     |
| ESBC™                    | MicroPak2™                                     | STEALTH™                              | UniFET™          |
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| Fairchild Semiconductor® | MotionGrid®                                    | SuperSOT™-6                           | VoltagePlus™     |
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| FACT®                    | MTX®   | SupreMOS®                             | Xsens™           |
| FAST®                    | MVN®   | SyncFET™                              | 仙童™              |
| FastvCore™               | mWSaver®                                       | Sync-Lock™                            |                  |
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