

74AC74, 74ACT74

Dual D-Type Positive Edge-Triggered Flip-Flop

Features

- I_{CC} reduced by 50%
- Output source/sink 24mA
- ACT74 has TTL-compatible inputs

General Description

The AC/ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, \bar{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.


Asynchronous Inputs:

- LOW input to \bar{S}_D (Set) sets Q to HIGH level
- LOW input to \bar{C}_D (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} HIGH

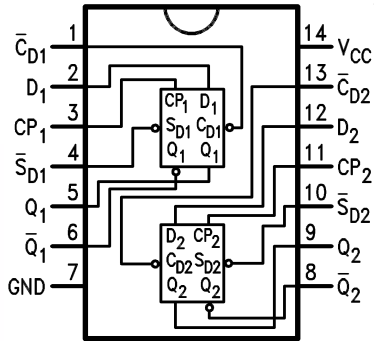
Ordering Information

| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| 74AC74SC | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74AC74SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74AC74MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74AC74PC | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| 74ACT74SC | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
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| 74ACT74PC | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

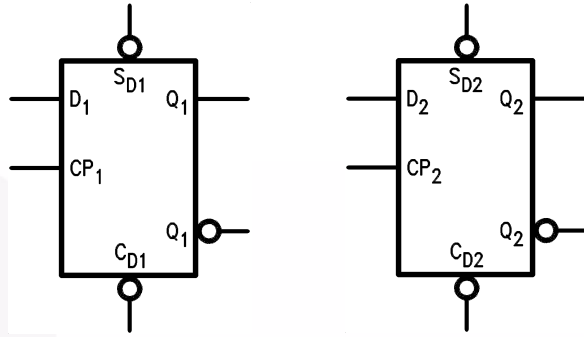
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



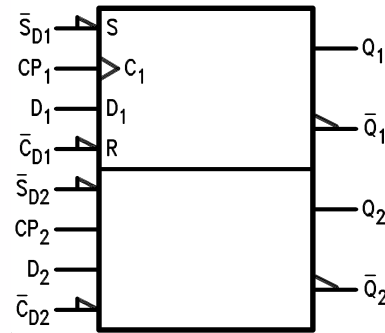
Logic Symbols



Pin Descriptions

| Pin Names | Description |
|----------------------------------|---------------------|
| D_1, D_2 | Data Inputs |
| CP_1, CP_2 | Clock Pulse Inputs |
| $\bar{C}_{D1}, \bar{C}_{D2}$ | Direct Clear Inputs |
| $\bar{S}_{D1}, \bar{S}_{D2}$ | Direct Set Inputs |
| $Q_1, \bar{Q}_1, Q_2, \bar{Q}_2$ | Outputs |

IEEE/IEC



Truth Table

(Each Half)

| Inputs | | | | Outputs | |
|-------------|-------------|----|---|---------|-------------|
| \bar{S}_D | \bar{C}_D | CP | D | Q | \bar{Q} |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |
| H | H | ↗ | H | H | L |
| H | H | ↗ | L | L | H |
| H | H | L | X | Q_0 | \bar{Q}_0 |

H = HIGH Voltage Level

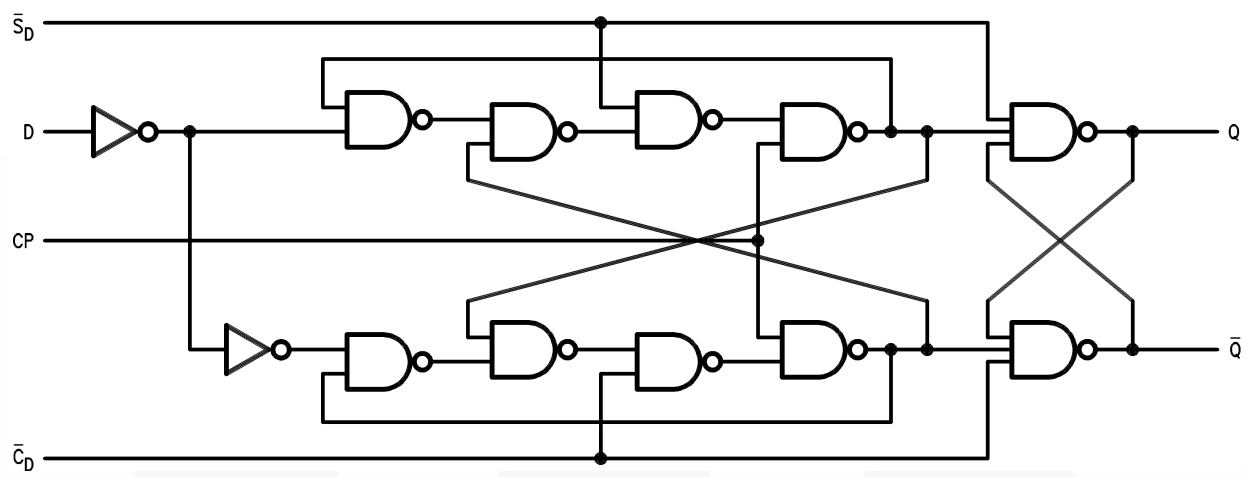
L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

$Q_0 (\bar{Q}_0)$ = Previous Q (\bar{Q}) before LOW-to-HIGH Transition of Clock

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|-----------------------|--|--------------------------|
| V_{CC} | Supply Voltage | -0.5V to +7.0V |
| I_{IK} | DC Input Diode Current $V_I = -0.5V$ | -20mA |
| | $V_I = V_{CC} + 0.5$ | +20mA |
| V_I | DC Input Voltage | -0.5V to $V_{CC} + 0.5V$ |
| I_{OK} | DC Output Diode Current $V_O = -0.5V$ | -20mA |
| | $V_O = V_{CC} + 0.5V$ | +20mA |
| V_O | DC Output Voltage | -0.5V to $V_{CC} + 0.5V$ |
| I_O | DC Output Source or Sink Current | $\pm 50mA$ |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current per Output Pin | $\pm 50mA$ |
| T_{STG} | Storage Temperature | -65°C to +150°C |
| T_J | Junction Temperature | 140°C |

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|-----------------------|--|----------------|
| V_{CC} | Supply Voltage AC | 2.0V to 6.0V |
| | ACT | 4.5V to 5.5V |
| V_I | Input Voltage | 0V to V_{CC} |
| V_O | Output Voltage | 0V to V_{CC} |
| T_A | Operating Temperature | -40°C to +85°C |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC} , V_{CC} @ 3.3V, 4.5V, 5.5V | 125mV/ns |
| $\Delta V / \Delta t$ | Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V | 125mV/ns |

DC Electrical Characteristics for AC

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | T _A = -40°C to +85°C | | Units |
|--------------------------------|---|------------------------|--|------------------------|-------------------|---------------------------------|--|-------|
| | | | | Typ. | Guaranteed Limits | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 3.0 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 2.1 | 2.1 | | V |
| | | 4.5 | | 2.25 | 3.15 | | | |
| | | 5.5 | | 2.75 | 3.85 | | | |
| V _{IL} | Maximum LOW Level Input Voltage | 3.0 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 0.9 | 0.9 | | V |
| | | 4.5 | | 2.25 | 1.35 | | | |
| | | 5.5 | | 2.75 | 1.65 | | | |
| V _{OH} | Minimum HIGH Level Output Voltage | 3.0 | I _{OUT} = -50μA | 2.99 | 2.9 | 2.9 | | V |
| | | 4.5 | | 4.49 | 4.4 | | | |
| | | 5.5 | | 5.49 | 5.4 | | | |
| | | 3.0 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -12mA | | 2.56 | 2.46 | | |
| | | 4.5 | | | 3.86 | 3.76 | | |
| | | 5.5 | | | 4.86 | 4.76 | | |
| V _{OL} | Maximum LOW Level Output Voltage | 3.0 | I _{OUT} = 50μA | 0.002 | 0.1 | 0.1 | | V |
| | | 4.5 | | 0.001 | 0.1 | | | |
| | | 5.5 | | 0.001 | 0.1 | | | |
| | | 3.0 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 12mA | | 0.36 | 0.44 | | |
| | | 4.5 | | | 0.36 | 0.44 | | |
| | | 5.5 | | | 0.36 | 0.44 | | |
| I _{IN} ⁽³⁾ | Maximum Input Leakage Current | 5.5 | V _I = V _{CC} , GND | | ±0.1 | ±1.0 | | μA |
| I _{OLD} | Minimum Dynamic Output Current ⁽²⁾ | 5.5 | V _{OLD} = 1.65V Max. | | | 75 | | mA |
| I _{OHD} | | 5.5 | V _{OHD} = 3.85V Min. | | | -75 | | mA |
| I _{CC} ⁽³⁾ | Maximum Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | | 2.0 | 20.0 | | μA |

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = +25°C | | T _A = -40°C to +85°C | | Units |
|------------------|---|------------------------|---|--|-------------------|---------------------------------|------|-------|
| | | | | Typ. | Guaranteed Limits | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 4.5 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 2.0 | 2.0 | | V |
| | | 5.5 | | 1.5 | 2.0 | 2.0 | | |
| V _{IL} | Maximum LOW Level Input Voltage | 4.5 | V _{OUT} = 0.1V or V _{CC} - 0.1V | 1.5 | 0.8 | 0.8 | | V |
| | | 5.5 | | 1.5 | 0.8 | 0.8 | | |
| V _{OH} | Minimum HIGH Level Output Voltage | 4.5 | I _{OUT} = -50μA | 4.49 | 4.4 | 4.4 | | V |
| | | 5.5 | | 5.49 | 5.4 | 5.4 | | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA | | 3.86 | 3.76 | | |
| | | 5.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OH} = -24mA ⁽⁴⁾ | | 4.86 | 4.76 | |
| V _{OL} | Maximum LOW Level Output Voltage | 4.5 | I _{OUT} = 50μA | 0.001 | 0.1 | 0.1 | | V |
| | | 5.5 | | 0.001 | 0.1 | 0.1 | | |
| | | 4.5 | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA | | 0.36 | 0.44 | | |
| | | 5.5 | | V _{IN} = V _{IL} or V _{IH} , I _{OL} = 24mA ⁽⁴⁾ | | 0.36 | 0.44 | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | V _I = V _{CC} , GND | | ±0.1 | ±1.0 | | μA |
| I _{CCT} | Maximum I _{CC} /Input | 5.5 | V _I = V _{CC} - 2.1V | 0.6 | | 1.5 | | mA |
| I _{OLD} | Minimum Dynamic Output Current ⁽⁵⁾ | 5.5 | V _{OLD} = 1.65V Max. | | | 75 | | mA |
| | | 5.5 | V _{OHD} = 3.85V Min. | | | -75 | | mA |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | | 2.0 | 20.0 | | μA |

Notes:

4. All outputs loaded; thresholds on input associated with output under test.

AC Electrical Characteristics for AC

| Symbol | Parameter | V_{CC} (V) ⁽⁶⁾ | $T_A = +25^\circ\text{C}$, $C_L = 50\text{pF}$ | | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $C_L = 50\text{pF}$ | | Units |
|-----------|---|-----------------------------|--|------|------|--|------|-------|
| | | | Min. | Typ. | Max. | Min. | Max. | |
| f_{MAX} | Maximum Clock Frequency | 3.3 | 100 | 125 | | 95 | | MHz |
| | | 5.0 | 140 | 160 | | 125 | | |
| t_{PLH} | Propagation Delay, \overline{C}_{Dn} or \overline{S}_{Dn} to Q_n or \overline{Q}_n | 3.3 | 3.5 | 8.0 | 12.0 | 2.5 | 13.0 | ns |
| | | 5.0 | 2.5 | 6.0 | 9.0 | 2.0 | 10.0 | |
| t_{PHL} | Propagation Delay, \overline{C}_{Dn} or \overline{S}_{Dn} to Q_n or \overline{Q}_n | 3.3 | 4.0 | 10.5 | 12.0 | 3.5 | 13.5 | ns |
| | | 5.0 | 3.0 | 8.0 | 9.5 | 2.5 | 10.5 | |
| t_{PLH} | Propagation Delay, CP_n to Q_n or \overline{Q}_n | 3.3 | 4.5 | 8.0 | 13.5 | 4.0 | 16.0 | ns |
| | | 5.0 | 3.5 | 6.0 | 10.0 | 3.0 | 10.5 | |
| t_{PHL} | Propagation Delay, CP_n to Q_n or \overline{Q}_n | 3.3 | 3.5 | 8.0 | 14.0 | 3.5 | 14.5 | ns |
| | | 5.0 | 2.5 | 6.0 | 10.0 | 2.5 | 10.5 | |

Note:

5. Voltage range 3.3 is $3.3\text{V} \pm 0.3\text{V}$. Voltage range 5.0 is $5.0\text{V} \pm 0.5\text{V}$.

AC Operating Requirements for AC

| Symbol | Parameter | V_{CC} (V) ⁽⁷⁾ | $T_A = +25^\circ\text{C}$, $C_L = 50\text{pF}$ | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $C_L = 50\text{pF}$ | | Units |
|-----------|--|-----------------------------|--|--------------------|--|--|-------|
| | | | Typ. | Guaranteed Minimum | | | |
| t_S | Set-up Time, HIGH or LOW, D_n to CP_n | 3.3 | 1.5 | 4.0 | 4.5 | | ns |
| | | 5.0 | 1.0 | 3.0 | 3.0 | | |
| t_H | Hold Time, HIGH or LOW, D_n to CP_n | 3.3 | -2.0 | 0.5 | 0.5 | | ns |
| | | 5.0 | -1.5 | 0.5 | 0.5 | | |
| t_W | CP_n or \overline{C}_{Dn} or \overline{S}_{Dn} Pulse Width | 3.3 | 3.0 | 5.5 | 7.0 | | ns |
| | | 5.0 | 2.5 | 4.5 | 5.0 | | |
| t_{rec} | Recovery Time, \overline{C}_{Dn} or \overline{S}_{Dn} to CP | 3.3 | -2.5 | 0 | 0 | | ns |
| | | 5.0 | -2.0 | 0 | 0 | | |

Note:

6. Voltage range 3.3 is $3.3\text{V} \pm 0.3\text{V}$. Voltage range 5.0 is $5.0\text{V} \pm 0.5\text{V}$.

AC Electrical Characteristics for ACT

| Symbol | Parameter | V _{CC} (V) ⁽⁸⁾ | T _A = +25°C, C _L = 50pF | | | T _A = -40°C to +85°C, C _L = 50pF | | Units |
|------------------|--|------------------------------------|--|------|------|---|------|-------|
| | | | Min. | Typ. | Max. | Min. | Max. | |
| f _{MAX} | Maximum Clock Frequency | 5.0 | 145 | 210 | | 125 | | MHz |
| t _{PLH} | Propagation Delay, \overline{C}_{Dn} or \overline{S}_{Dn} to Q _n or \overline{Q}_n | 5.0 | 3.0 | 5.5 | 9.5 | 2.5 | 10.5 | ns |
| t _{PHL} | Propagation Delay, \overline{C}_{Dn} or \overline{S}_{Dn} to Q _n or \overline{Q}_n | 5.0 | 3.0 | 6.0 | 10.0 | 3.0 | 11.5 | ns |
| t _{PLH} | Propagation Delay, CP _n to Q _n or \overline{Q}_n | 5.0 | 4.0 | 7.5 | 11.0 | 4.0 | 13.0 | ns |
| t _{PHL} | Propagation Delay, CP _n to Q _n or \overline{Q}_n | 5.0 | 3.5 | 6.0 | 10.0 | 3.0 | 11.5 | ns |

Note:

7. Voltage range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements for ACT

| Symbol | Parameter | V _{CC} (V) ⁽⁹⁾ | T _A = +25°C, C _L = 50pF | | T _A = -40°C to +85°C, C _L = 50pF | | Units |
|------------------|---|------------------------------------|--|--------------------|---|--|-------|
| | | | Typ. | Guaranteed Minimum | | | |
| t _S | Set-up Time, HIGH or LOW, D _n to CP _n | 5.0 | 1.0 | 3.0 | 3.5 | | ns |
| t _H | Hold Time, HIGH or LOW, D _n to CP _n | 5.0 | -0.5 | 1.0 | 1.0 | | ns |
| t _W | CP _n or \overline{C}_{Dn} or \overline{S}_{Dn} Pulse Width | 5.0 | 3.0 | 5.0 | 6.0 | | ns |
| t _{rec} | Recovery Time, \overline{C}_{Dn} or \overline{S}_{Dn} to CP | 5.0 | -2.5 | 0 | 0 | | ns |

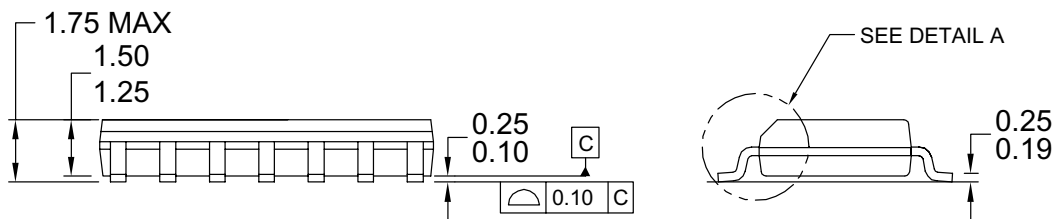
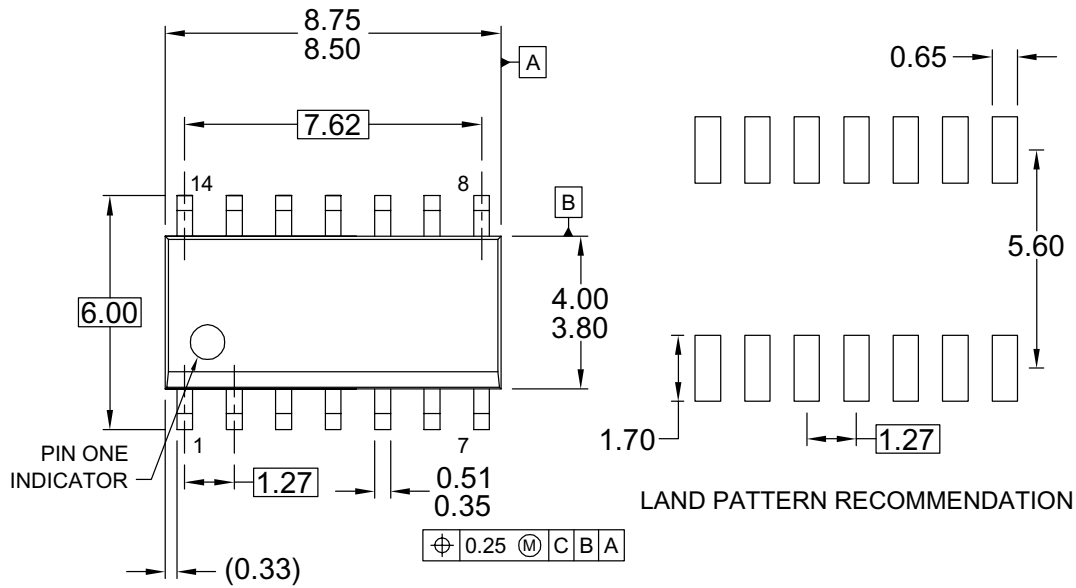
Note:

8. Voltage range 5.0 is 5.0V ± 0.5V.

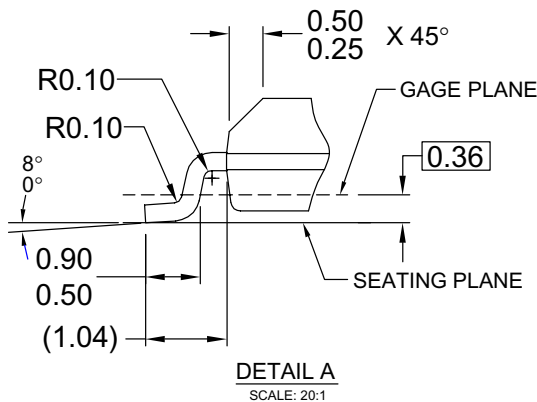
Capacitance

| Symbol | Parameter | Conditions | Typ. | Units |
|-----------------|-------------------------------|------------------------|------|-------|
| C _{IN} | Input Capacitance | V _{CC} = OPEN | 4.5 | pF |
| C _{PD} | Power Dissipation Capacitance | V _{CC} = 5.0V | 35.0 | pF |

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED



- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

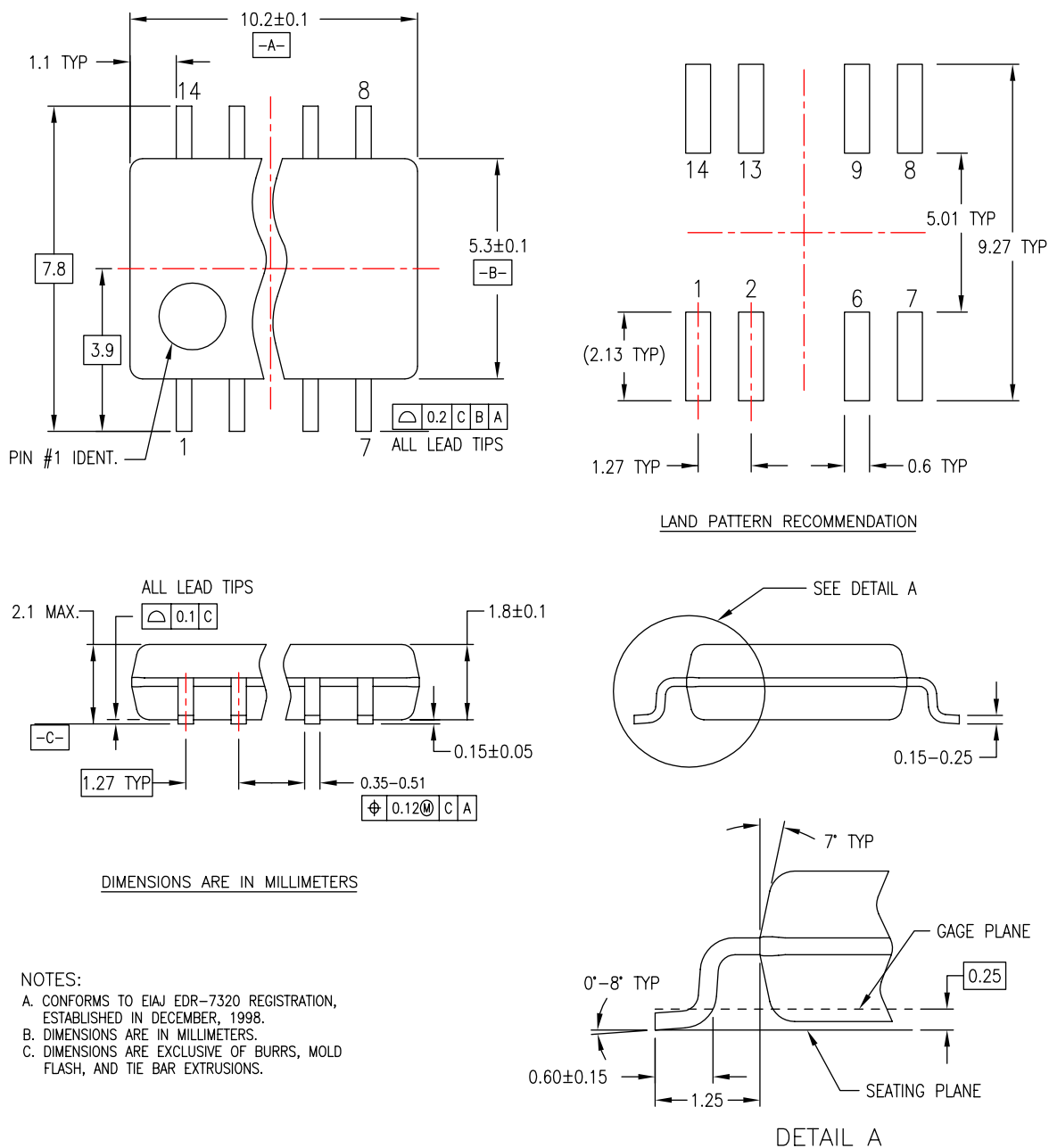
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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Physical Dimensions (Continued)



- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DREVC

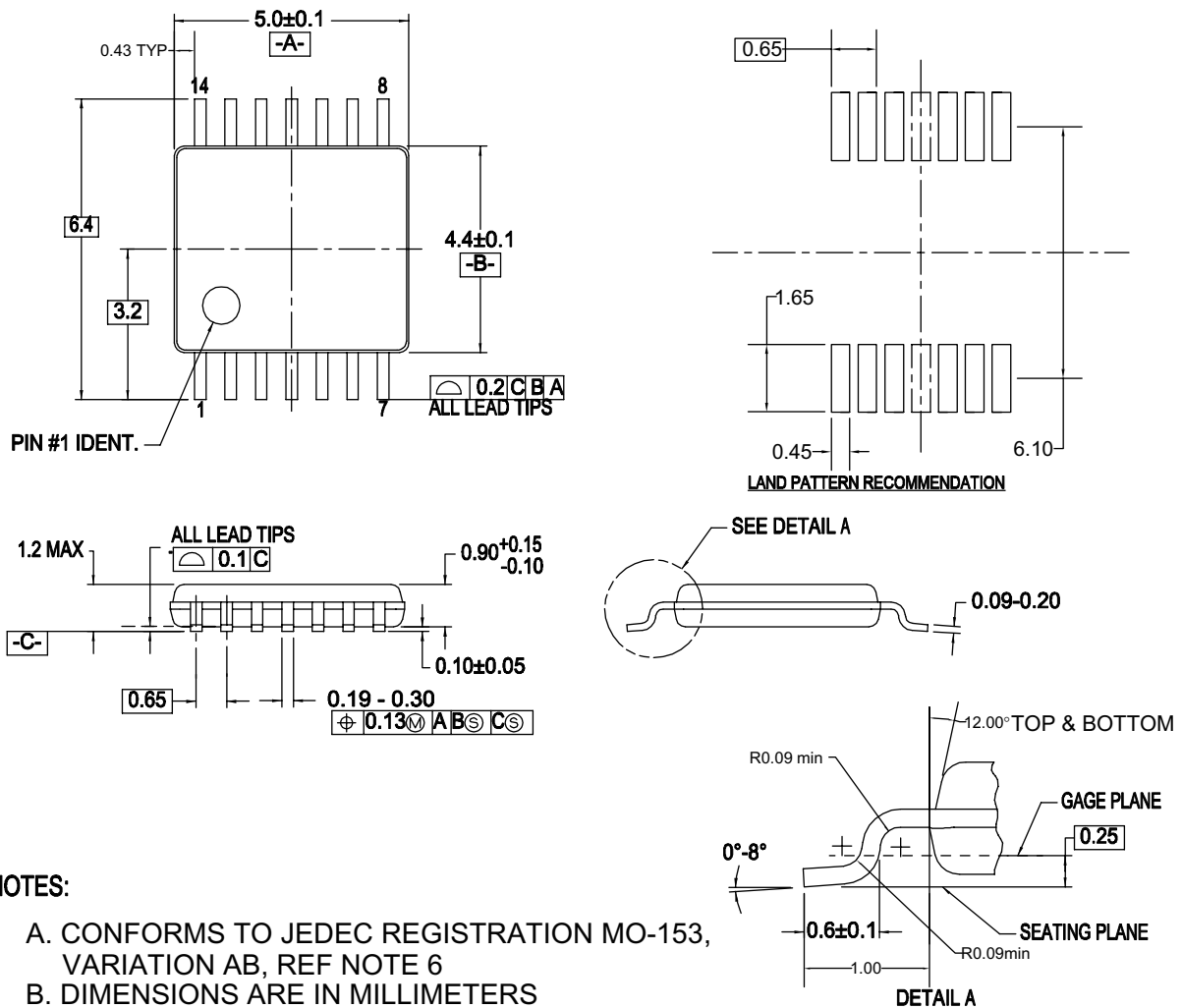
Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)



NOTES:

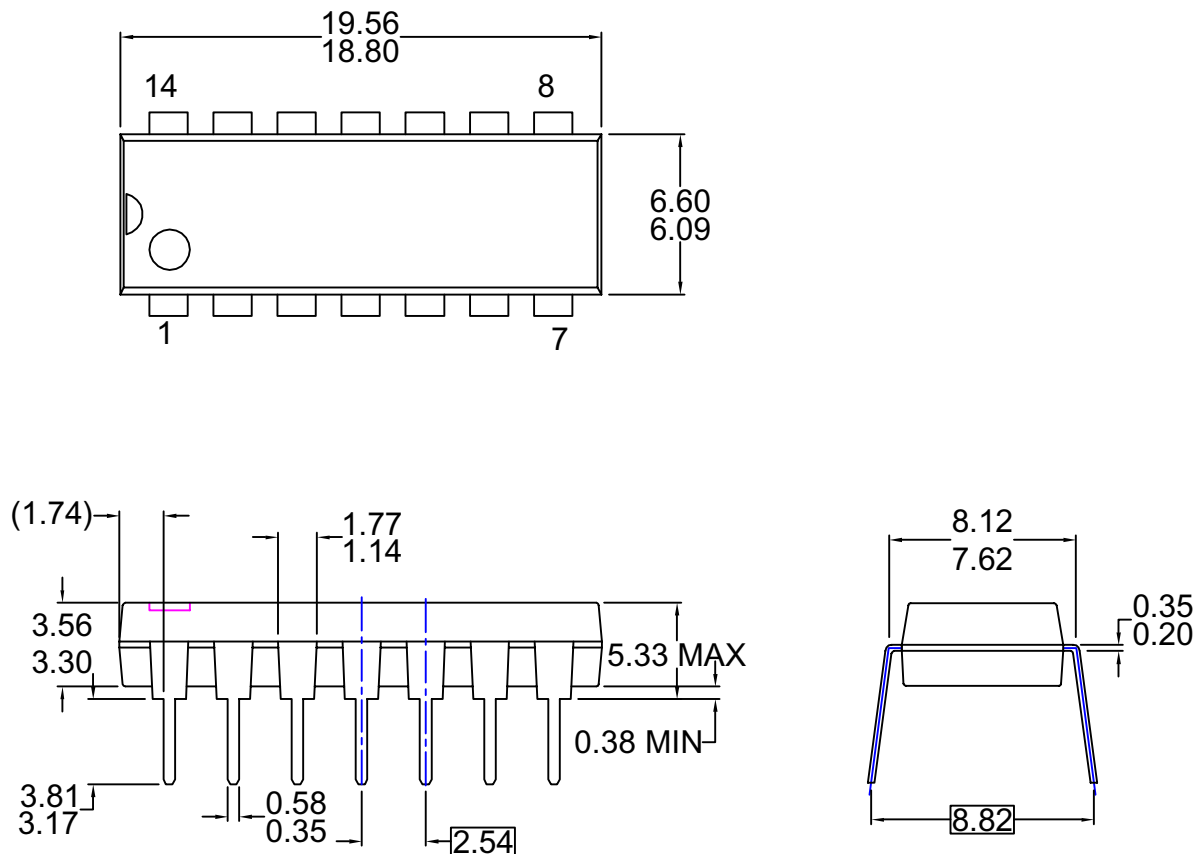
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Physical Dimensions (Continued)

- NOTES: UNLESS OTHERWISE SPECIFIED**
- THIS PACKAGE CONFORMS TO
 - A) JEDEC MS-001 VARIATION BA
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - D) DIMENSIONS AND TOLERANCES PER ASME Y14.5-1994
 - E) DRAWING FILE NAME: MKT-N14AREV7

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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

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| FAST [®] | Motion-SPM [™] | STEALTH [™] | UHC [®] |
| FastvCore [™] * | OPTOLOGIC [®] | SuperFET [™] | Ultra FRFET [™] |
| FlashWriter [®] * | OPTOPLANAR [®] | SuperSOT [™] -3 | UniFET [™] |
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PRODUCT STATUS DEFINITIONS

Definition of Terms

| Datasheet Identification | Product Status | Definition |
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Rev. I32