

MM74HC4066 Quad Analog Switch

Features

- Typical switch enable time: 15ns
- Wide analog input voltage range: 0V–12V
- Low “ON” resistance: 30 typ. (MM74HC4066)
- Low quiescent current: 80µA maximum (74HC)
- Matched switch characteristics
- Individual switch controls


General Description

The MM74HC4066 devices are digitally controlled analog switches utilizing advanced silicon-gate CMOS technology. These switches have low “ON” resistance and low “OFF” leakages. They are bidirectional switches, thus any analog input may be used as an output and visa-versa. Also the MM74HC4066 switches contain linearization circuitry which lowers the “ON” resistance and increases switch linearity. The MM74HC4066 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when LOW. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

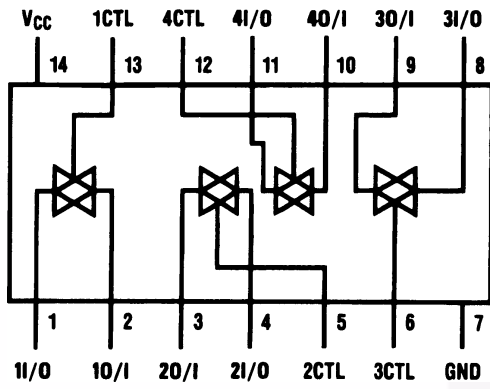
Ordering Information

Order Number	Package Number	Package Description
MM74HC4066M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4066SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4066MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4066N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

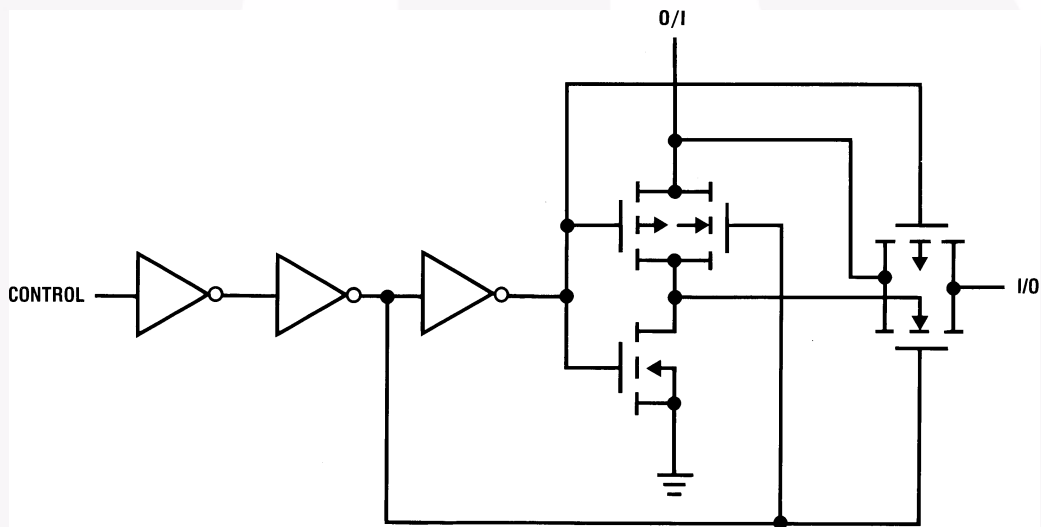


Top View

Truth Table

Input	Switch
CTL	I/O-O/I
L	"OFF"
H	"ON"

Schematic Diagram



Absolute Maximum Ratings⁽¹⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5 to +15V
V_{IN}	DC Control Input Voltage	-1.5 to $V_{CC}+1.5V$
V_{OUT}	DC Switch I/O Voltage	$V_{EE}-0.5$ to $V_{CC}+0.5V$
I_{IK}, I_{OK}	Clamp Diode Current	$\pm 20mA$
I_{OUT}	DC Output Current, per pin	$\pm 25mA$
I_{CC}	DC V_{CC} or GND Current, per pin	$\pm 50mA$
T_{STG}	Storage Temperature Range	-65°C to +150°C
P_D	Power Dissipation Note 2	600mW
	S.O. Package only	500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Notes:

1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating — plastic “N” package: -12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	2	12	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	-40	+85	°C
t_r, t_f	Input Rise or Fall Times $V_{CC} = 2.0V$		1000	ns
	$V_{CC} = 4.5V$		500	ns
	$V_{CC} = 6.0V$		400	ns

DC Electrical Characteristics⁽³⁾

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C		T _A = -40°C to 85°C	T _A = -55°C to 125°C	Units
				Typ.	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	2.0			1.5	1.5	1.5	V
		4.5			3.15	3.15	3.15	
		9.0			6.3	5.3	6.3	
		12.0			8.4	8.4	8.4	
V _{IL}	Maximum LOW Level Input Voltage	2.0			0.5	0.5	0.5	V
		4.5			1.35	1.35	1.35	
		9.0			2.7	2.7	2.7	
		12.0			3.6	3.6	3.6	
R _{ON}	Maximum "ON" Resistance ⁽⁴⁾	4.5	V _{CTL} = V _{IH} , I _S = 2.0mA, V _{IS} = V _{CC} to GND (Figure 1)	100	170	200	220	Ω
		9.0		50	85	105	110	
		12.0		30	70	85	90	
		2.0	V _{CTL} = V _{IH} , I _S = 2.0mA, V _{IS} = V _{CC} or GND (Figure 1)	120	180	215	240	
		4.5		50	80	100	120	
		9.0		35	60	75	80	
		12.0		20	40	60	70	
R _{ON}	Maximum "ON" Resistance Matching	4.5	V _{CTL} = V _{IH} , V _{IS} = V _{CC} to GND	10	15	20	20	Ω
		9.0		5	10	15	15	
		12.0		5	10	15	15	
I _{IN}	Maximum Control Input Current		V _{IN} = V _{CC} or GND, V _{CC} = 2–6V		±0.1	±1.0	±1.0	μA
I _{IZ}	Maximum Switch "OFF" Leakage Current	6.0	V _{OS} = V _{CC} or GND, V _{IS} = GND or V _{CC} , V _{CTL} = V _{IL} (Figure 3)	10	±60	±600	±600	nA
		9.0		15	±80	±800	±800	
		12.0		20	±100	±1000	±1000	
I _{IZ}	Maximum Switch "ON" Leakage Current	6.0	V _{IS} = V _{CC} to GND, V _{CTL} = V _{IH} , V _{OS} = OPEN (Figure 2)	10	±40	±150	±150	nA
		9.0		15	±50	±200	±200	
		12.0		20	±60	±300	±300	
I _{CC}	Maximum Quiescent Supply Current	6.0	V _{IN} = V _{CC} or GND, I _{OUT} = 0μA		2.0	20	40	μA
		9.0			4.0	40	80	
		12.0			8.0	80	160	

Notes:

- For a power supply of 5V ±10% the worst case on resistance (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.
- At supply voltages (V_{CC}–GND) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

$V_{CC} = 2.0V-6.0V$ $V_{EE} = 0V-12V$, $C_L = 50pF$ (unless otherwise specified)

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25^\circ C$				Units
				Typ.	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out	2.0V		25	50	30	75	ns
		4.5V		5	10	13	15	
		9.0V		4	8	10	12	
		12.0V		3	7	11	13	
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	2.0V	$R_L = 1k\Omega$	30	100	125	150	ns
		4.5V		12	20	25	30	
		9.0V		6	12	15	18	
		12.0V		5	10	13	15	
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay	2.0V	$R_L = 1k\Omega$	60	168	210	252	ns
		4.5V		25	36	45	54	
		9.0V		20	32	40	48	
		12.0V		15	30	38	45	
f_{MAX}	Minimum Frequency Response (Figure 7) $20 \log (V_O/V_I) = -3dB$	4.5V	$R_L = 600\Omega$, $V_{IS} = 2 V_{PP}$ at $(V_{CC}/2)^{(5)(6)}$	40				MHz
		9.0V		100				
	Crosstalk Between any Two Switches (Figure 8)	4.5V	$R_L = 600\Omega$, $F = 1MHz^{(6)(7)}$	-52				dB
		9.0V		-50				
	Peak Control to Switch Feedthrough Noise (Figure 9)	4.5V	$R_L = 600\Omega$, $F = 1MHz$, $C_L = 50pF$	100				mV
		9.0V		250				
	Switch OFF Signal Feedthrough Isolation (Figure 10)	4.5V	$R_L = 600\Omega$, $F = 1MHz$, $V_{(CT)}V_{IL}^{(6)(7)}$	-42				dB
		9.0V		-44				
THD	Total Harmonic Distortion (Figure 11)	4.5V	$R_L = 10k\Omega$, $C_L = 50pF$, $F = 1kHz$, $V_{IS} = 4 V_{PP}$, $V_{IS} = 8 V_{PP}$.013				%
		9.0V		.008				
C_{IN}	Maximum Control Input Capacitance			5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance			20				pF
C_{IN}	Maximum Feedthrough Capacitance		$V_{CTL} = GND$	0.5				pF
C_{PD}	Power Dissipation Capacitance			15				pF

Notes:

- Adjust 0dBm for $F = 1kHz$ (Null R_L/R_{ON} Attenuation).
- V_{IS} is centered at $V_{CC}/2$.
- Adjust input for 0dBm.

AC Test Circuits and Switching Time Waveforms

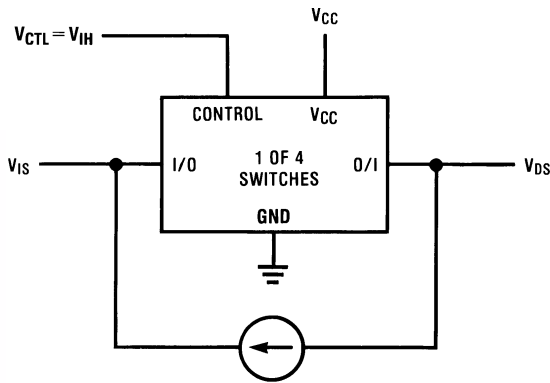


Figure 1. "ON" Resistance

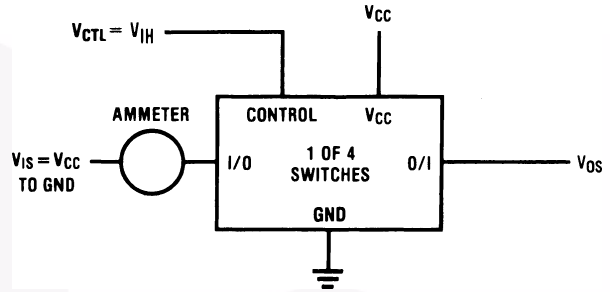


Figure 2. "ON" Channel Leakage Current

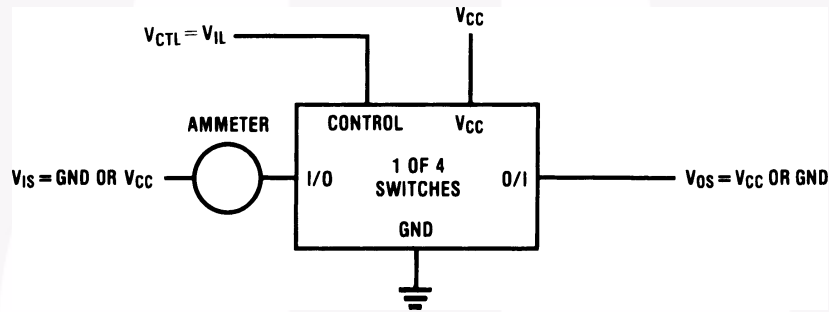


Figure 3. "OFF" Channel Leakage Current

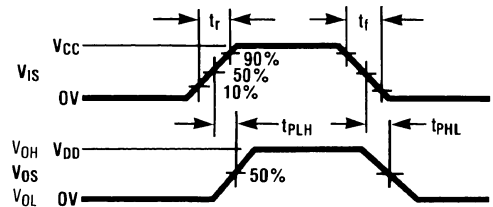
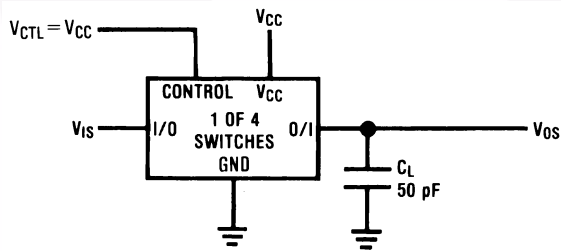


Figure 4. t_{PHL} , t_{PLH} Propagation Delay Time Signal Input to Signal Output

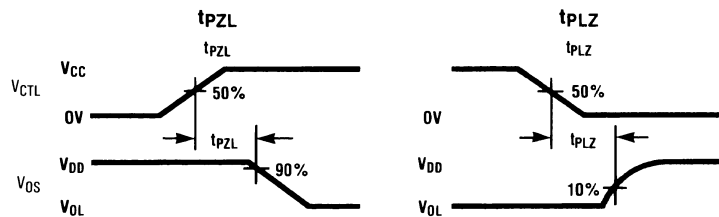
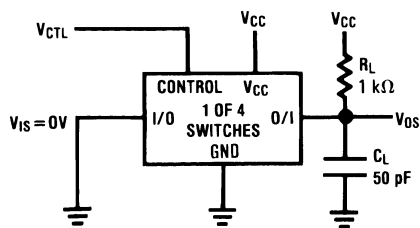


Figure 5. t_{PZL} , t_{PLZ} Propagation Delay Time Control to Signal Output

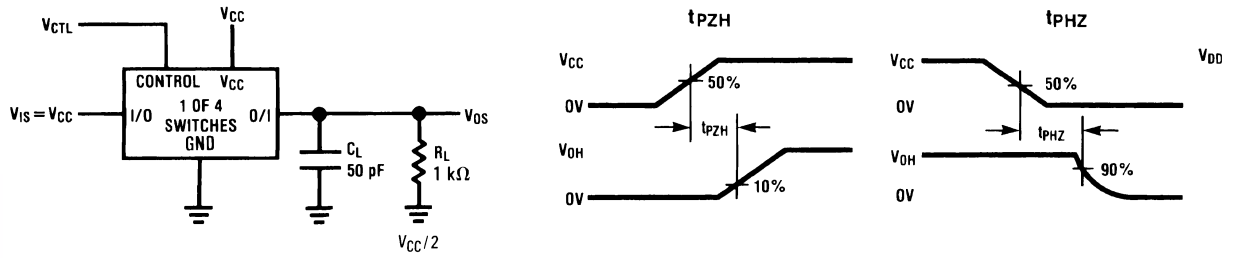


Figure 6. t_{PZH} , t_{PHZ} Propagation Delay Time Control to Signal Output

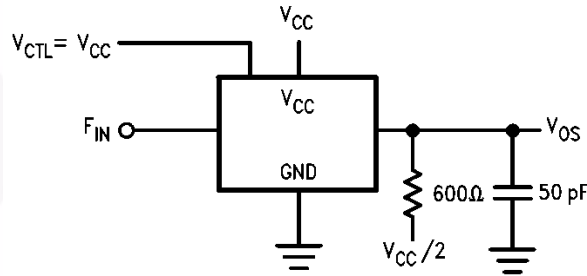


Figure 7. Frequency Response

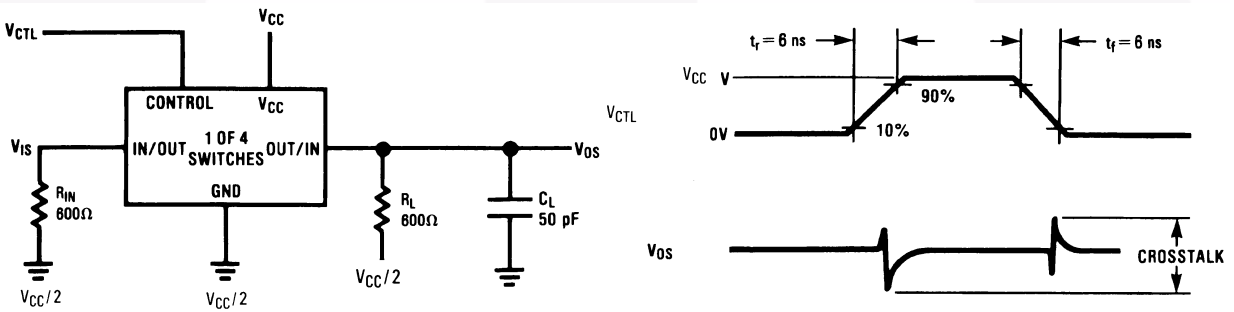


Figure 8. Crosstalk: Control Input to Signal Output

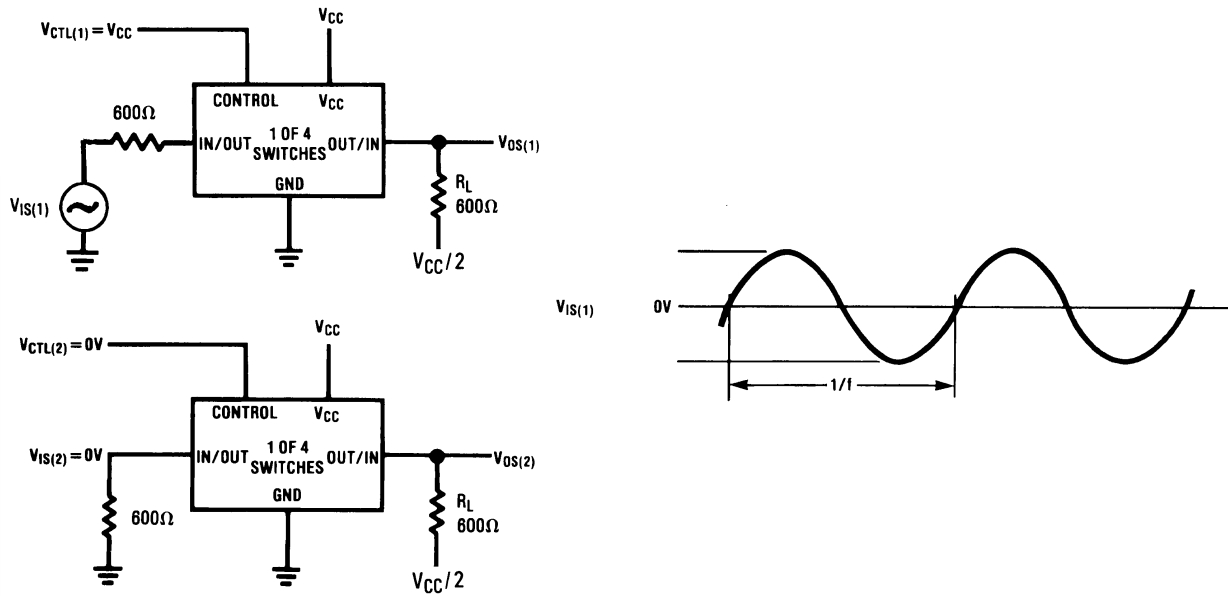


Figure 9. Crosstalk Between Any Two Switches

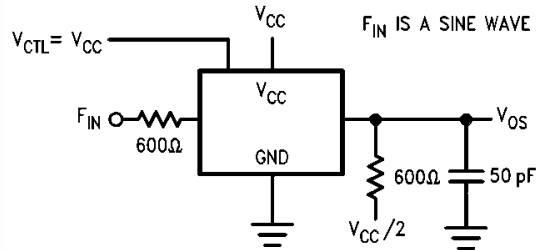


Figure 10. Switch OFF Signal Feedthrough Isolation

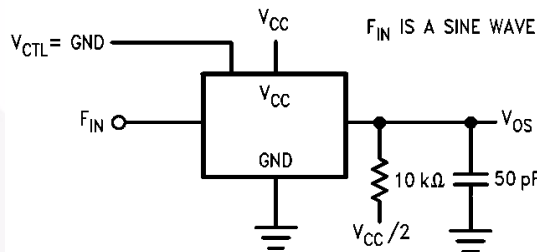
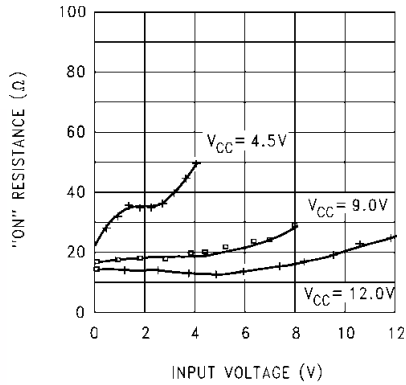


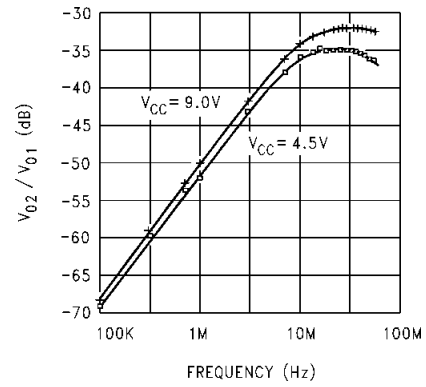
Figure 11. Sinewave Distortion

Typical Performance Characteristics

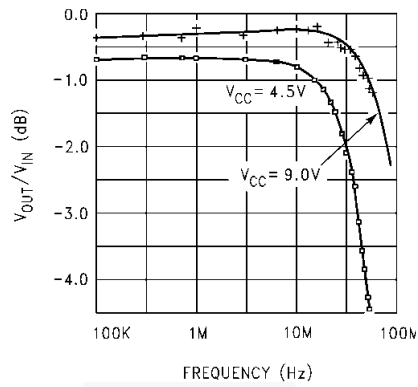
Typical "ON" Response



Typical Crosstalk Between Any Two Switches



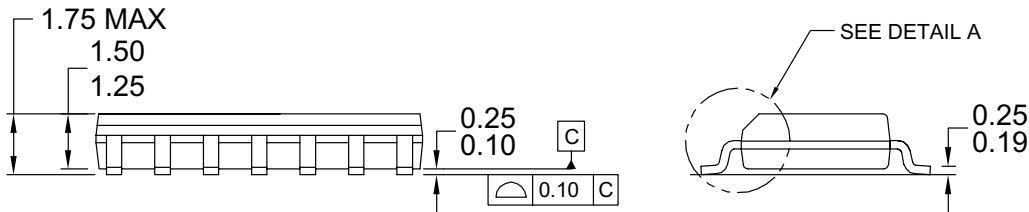
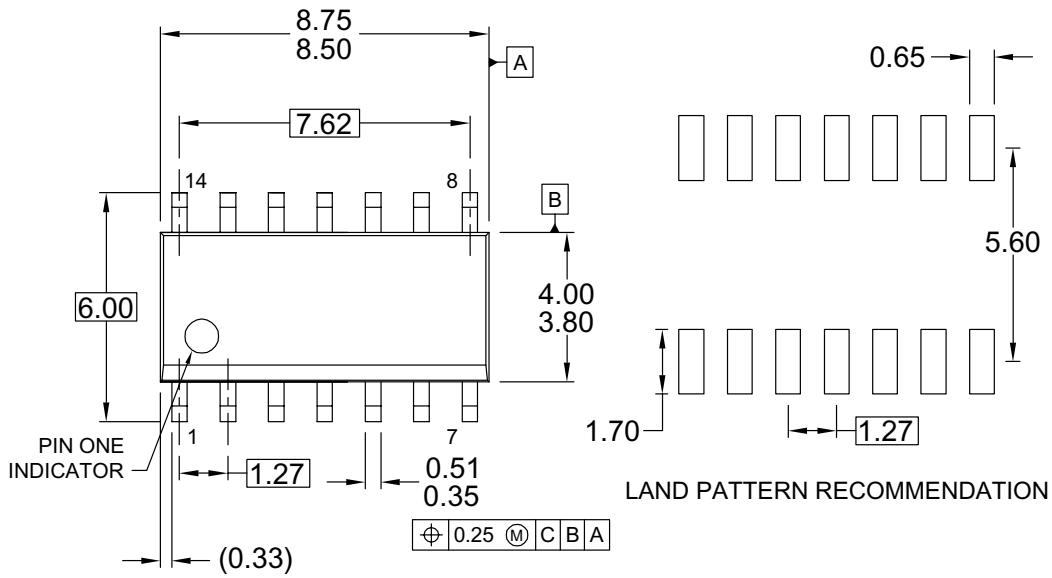
Typical Frequency Response



Special Considerations

In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the ON resistance).

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

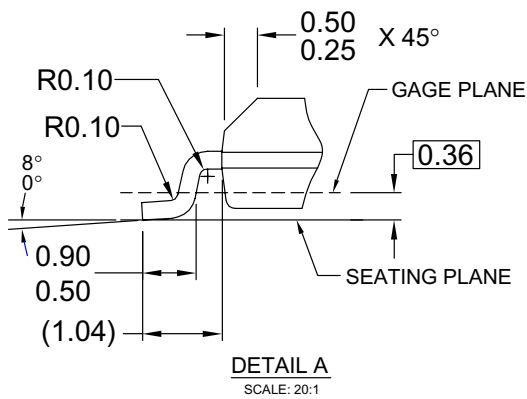


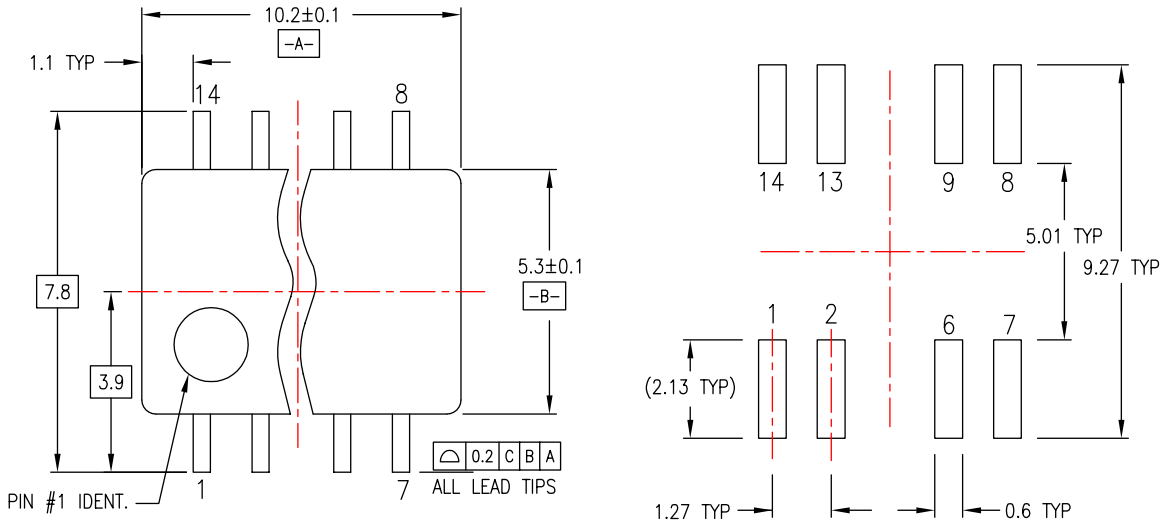
Figure 12. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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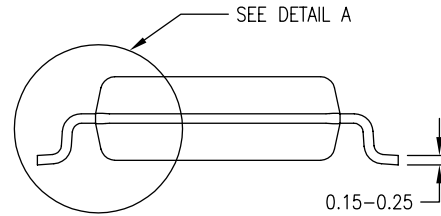
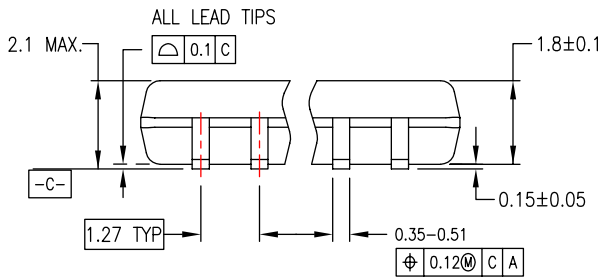
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Physical Dimensions (Continued)



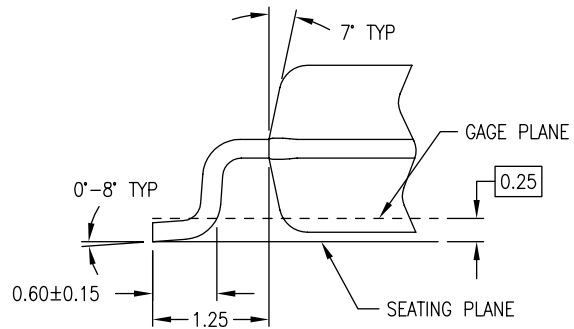
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
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- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



DETAIL A

M14DREVC

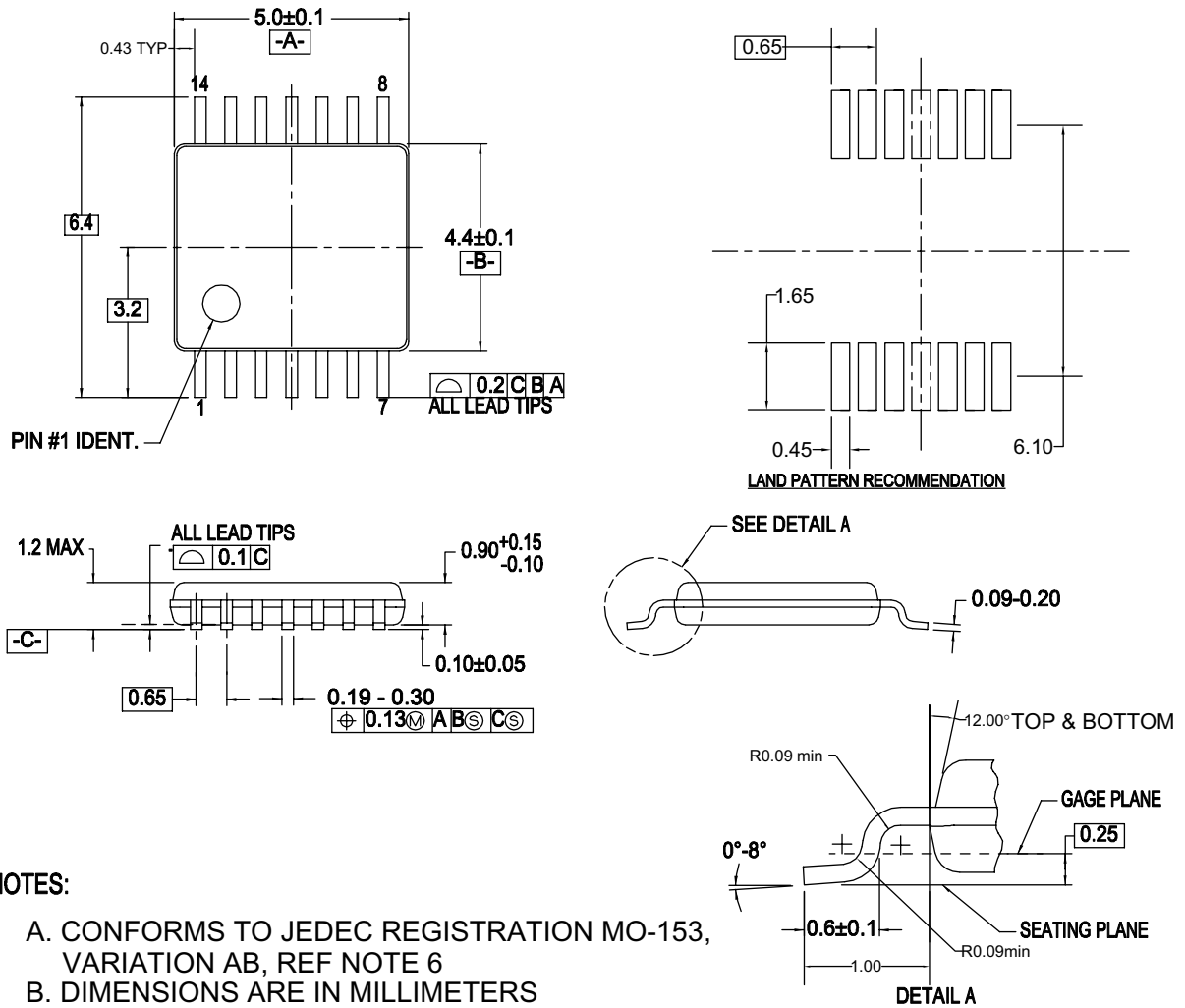
Figure 13. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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NOTES:

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- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

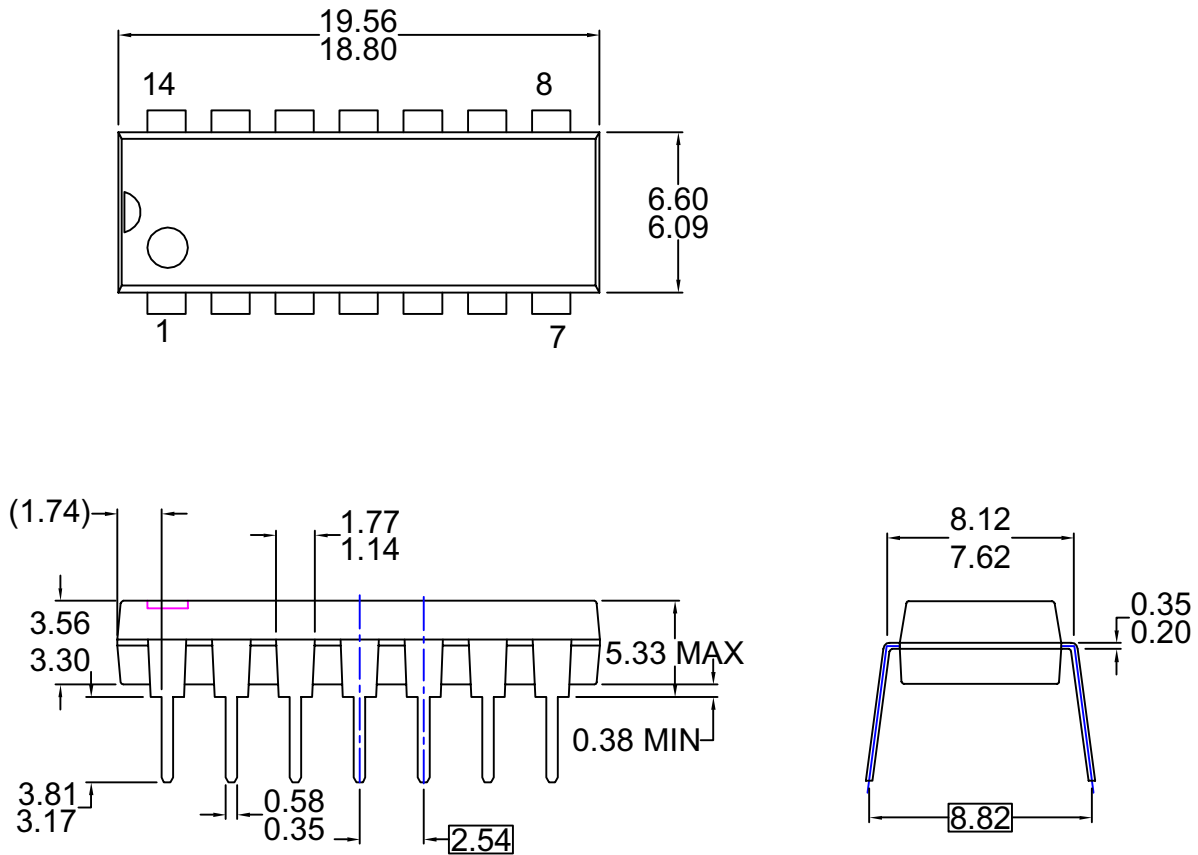
Figure 14. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Physical Dimensions (Continued)



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 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - D) DIMENSIONS AND TOLERANCES PER ASME Y14.5-1994
 - E) DRAWING FILE NAME: MKT-N14AREV7

Figure 15. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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