FAIRCHILD SEMICONDUCTOR®

November 2013

FCM8531 — MCU Embedded and Configurable 3-Phase PMSM / BLDC Motor Controller

Features

Advanced Motor Controller (AMC)

- Configurable Processing Core
  - Sensorless Field-Oriented Control (FOC) with Speed Integral Method
  - Sensorless FOC with Sliding Mode
  - Hall Interface
- Space Vector Modulation (SVM)
- Sine-Wave & Square-Wave Generator
- Programmable Current Leading Phase Control
- Programmable Soft-Switching Control (Dead Time)
- FCM8531RQY Certified by UL for IEC-60730-1 Class B Compliance with recognized marking:

Embedded MCU

- MCS® 51 Compatible
- 63% of Instructions' Execution Cycle <3 System Clocks (3T)
- Memory Size:
  - 12 KB Flash Program Memory
  - 256 +1 KB SRAM Data Memory
- Extended16-Bit Multiplication / Division Unit (MDU)
- ≤17 General-Purpose Input / Output (GPIO) Pins
- Full Duplex Serial Interface (UART)
- I^2C Interface
- Serial Peripheral Interface (SPI)
- Three External Interrupts
- Three 16-Bit Timers
- Programmable 15-Bit Watchdog Timer (WDT)
- Built-in Power-On Reset (POR)
- Built-in Clock Generator
- Two-Level Program Memory Lock

ADC and DAC

- 8-Channel, 10-Bit ADC
  - Auto-Trigger Sample & Hold
  - Four Trigger Mode Selections
  - Three Pre-AMP Gain Selections
- 1-Channel, 8-Bit DAC

Protections

- Three Levels of Over-Current Protection (OCP)

Power Management

- Idle Mode, Stop Mode, Sleep Mode

Development Supports

- In System Programming (ISP)
  On-Chip Debug Support (OCDS)

Description

The FCM8531 is an application-specific parallel-core processor for motor control that consists of an Advanced Motor Controller (AMC) processor and a MCS® 51-compatible MCU processor. The AMC is the core processor specifically designed for motor control. It integrates a configurable processing core and peripheral circuits to perform FOC and "Sensorless" motor control. System control, user interface, communication interface, and input/output interface can be programmed through the embedded MCS® 51 for different motor applications.

The advantage of FCM8531's parallel-core processors is that the two processors can work independently and complement each other. The AMC processes the tasks dedicated for motor controls, such as the motor control algorithms, PWM controls, current sensing, real-time over-current protection, and motor angle calculation. The embedded MCU provides motor control commands to the AMC to perform motor control activities through a communication interface. This approach reduces the software burden and simplifies the control system program because complex motor control algorithms are executed in the AMC. Fairchild provides the Motor Control Development System (MCDS) IDE and MCDS Programming Kit for users to develop software, compile programs, and perform online debugging.

To meet IEC 60730-1 Class B safety standard for household appliances, FCM8531 has FCM8531RQY version in its family that has been certificated by UL for the compliance. Users can directly utilize the UL certificated AMC to quicken product development cycle for electronic controlled PMSM/BLDC motor.

Applications

- Sensorless IPM / SPM, BLDC / PMSM Motor
- Fan, Blower, Pump, Compressor, etc.

Related Resources

- *AN-8202 — FCM8531 User Manual - Hardware Description*
- *AN-8203 — FCM8531 User Manual - Instruction Set*
- *User Guide for FCM8531 Evaluation Board*

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FCM8531QY	-40°C to 85°C	32-Lead, LQFP, JEDEC MS-026, Variation BBA, 7 mm Square	Tray
FCM8531RQY	-40°C to 85°C	32-Lead, LQFP, JEDEC MS-026, Variation BBA, 7 mm Square	Tray

Application Diagram

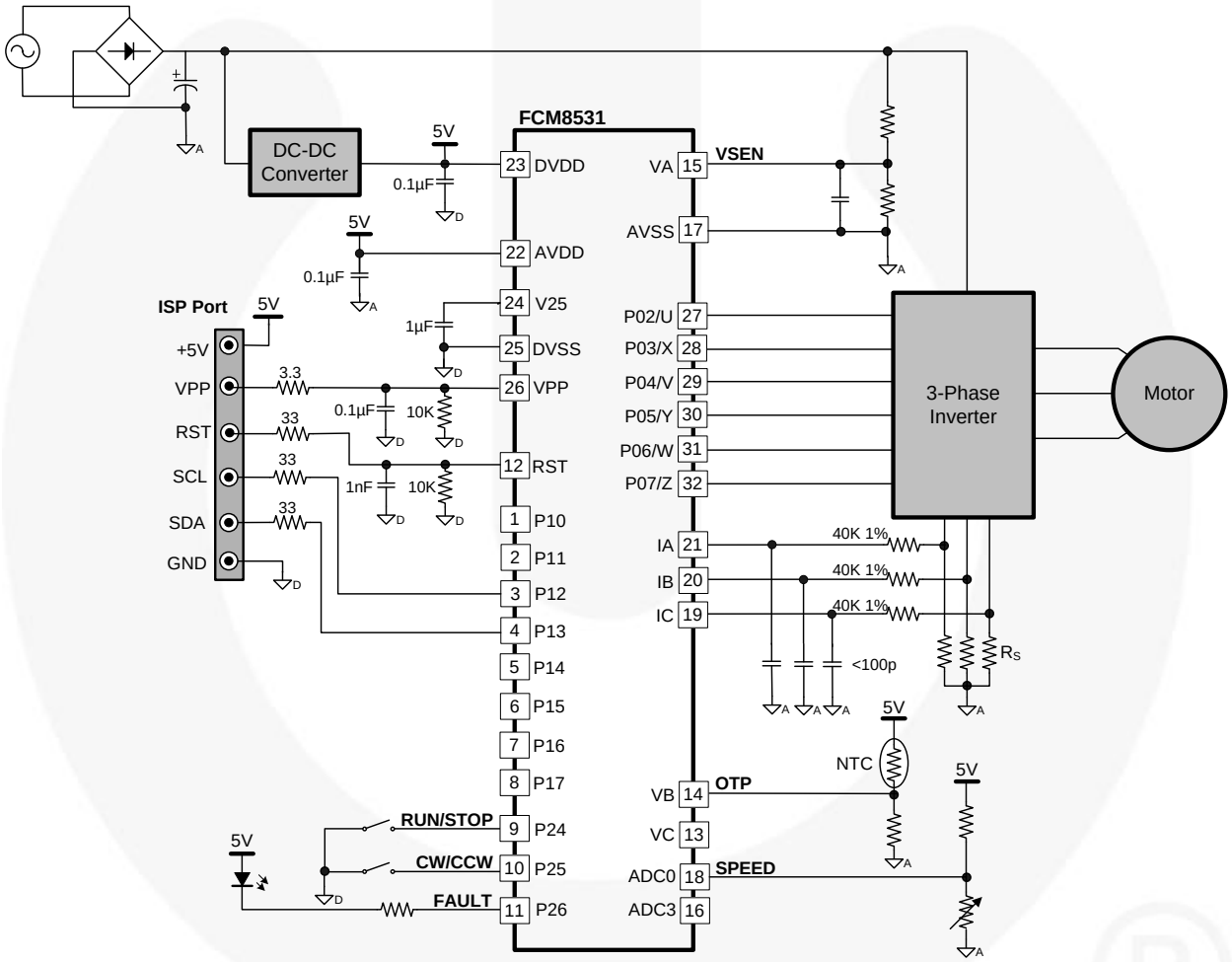


Figure 1. Typical Application Circuit

Block Diagram

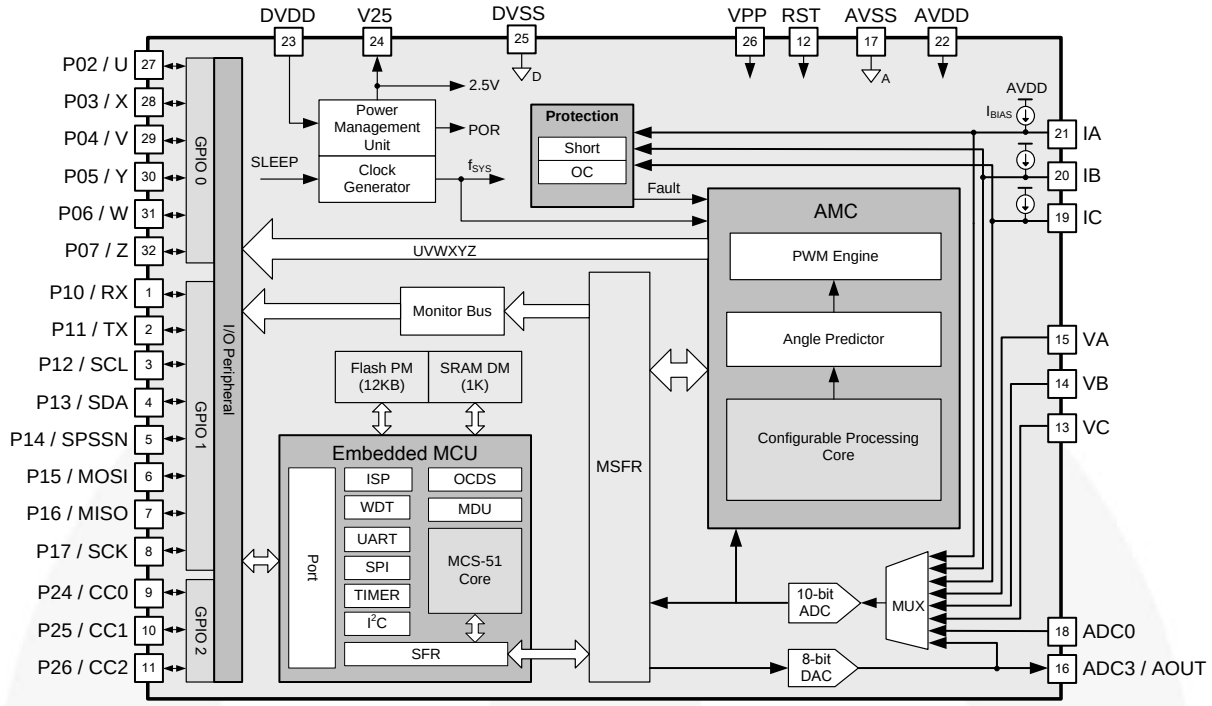
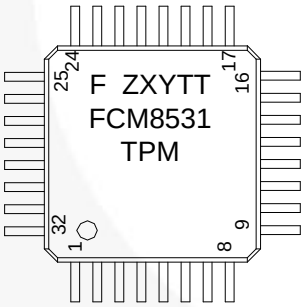


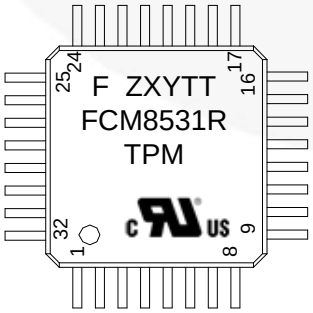
Figure 2. Block Diagram

Marking Information



F- Fairchild Logo
Z- Plant Code
X-1-Digit Year Code
Y- 1-Digit Week Code
TT: 2-Digit Die Run Code
T:Package Type (Q=LQFP)
P: Y=Green Package
M: Die Run Code

Figure 3. FCM8531 Top Mark



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R: UL60730 Certification
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Figure 4. FCM8531R Top Mark

Pin Configuration

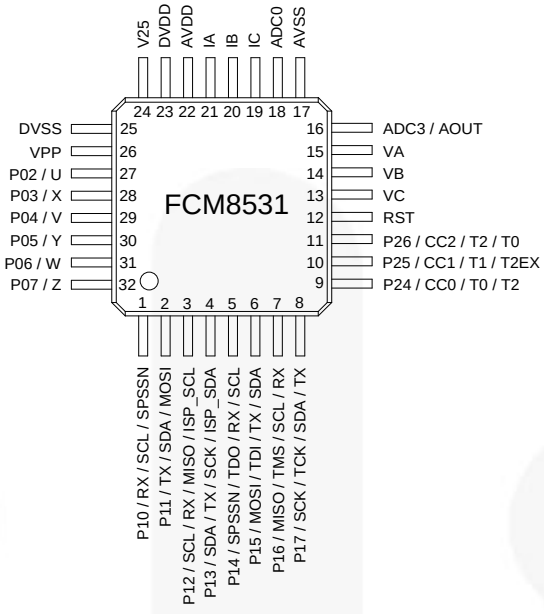

Figure 5. Pin Configuration

Pin Definitions

Pin #	Name	Type	Description
1	P10	I/O	**Bit 0 of Port 1**. General-purpose input/output pin with internal pull-up resistor.
	RX	I	**Data Receive (UART)**
	SCL	I/O	**Serial Clock (I^2C)**
	SPSSN	I/O	**SPI Slave Select (SPI)**
2	P11	I/O	**Bit 1 of Port 1**. General-purpose input/output pin with internal pull-up resistor.
	TX	O	**Serial Data Transmit (UART)**
	SDA	I/O	**Serial Data (I^2C)**
	MOSI	I/O	**Master Data Output and Slave Data Input (SPI)**
3	P12	I/O	**Bit 2 of Port 1**. General-purpose input/output pin with internal pull-up resistor.
	SCL	I/O	**Serial Clock (I^2C)**
	RX	I	**Data Receive (UART)**
	MISO	I/O	**Master Data Input and Slave Data Output (SPI)**
	ISP_SCL	I	**ISP Serial Clock**. Serial clock input in ISP Mode.
4	P13	I/O	**Bit 3 of Port 1**. General-purpose input/output pin with internal pull-up resistor.
	SDA	I/O	**Serial Data (I^2C)**
	TX	O	**Serial Data Transmit (UART)**
	SCK	I/O	**Serial Clock (SPI)**
	ISP_SDA	I/O	**ISP Serial Data**. Serial data input/output pin in ISP Mode.
5	P14	I/O	**Bit 4 of Port 1**. General-purpose input/output pin with internal pull-up resistor.
	SPSSN	I/O	**SPI Slave Select (SPI)**
	RX	I	**Data Receive (UART)**
	SCL	I/O	**Serial Clock (I^2C)**
	TDO	O	**Test Data Output**. Test data output in OCDS Mode.

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Pin Definitions (Continued)

Pin #	Name	Type	Description
6	P15	I/O	**Bit 5 of Port 1**. General-purpose input/output pin with internal pull-up resistor.
	MOSI	I/O	**Master Data Output and Slave Data Input (SPI)**
	TX	O	**Serial Data Transmit (UART)**
	SDA	I/O	**Serial Data (I^2C)**
	TDI	I	**Test Data Input**. Test data input in OCDS Mode.
7	P16	I/O	**Bit 6 of Port 1**. General-purpose input/output pin with internal pull-up resistor.
	MISO	I/O	**Master Data Input and Slave Data Output (SPI)**
	SCL	I/O	**Serial Clock (I^2C)**
	RX	I	**Data Receive (UART)**
	TMS	I	**Test Mode Select**. Test mode select in OCDS Mode.
8	P17	I/O	**Bit 7 of Port 1**. General-purpose input/output pin with internal pull-up resistor.
	SCK	I/O	**Serial Clock (SPI)**
	SDA	I/O	**Serial Data (I^2C)**
	TX	O	**Serial Data Transmit (UART)**
	TCK	I	**Test Clock**. Test clock input in OCDS Mode.
9	P24	I/O	**Bit 4 of Port 2**. General-purpose input/output pin with internal pull-up resistor.
	CC0	I/O	**TIMER2 Compare/Capture Channel 0**
	T0	I	**TIMER0 External Input**
	T2	I	**TIMER2 External Input**
10	P25	I/O	**Bit 5 of Port 2**. General-purpose input/output pin with internal pull-up resistor.
	CC1	I/O	**TIMER2 Compare/Capture Channel 1**
	T1	I	**TIMER1 External Input**
	T2EX	I	**TIMER2 External Trigger**
11	P26	I/O	**Bit 6 of Port 2**. General-purpose input/output pin with internal pull-up resistor.
	CC2	I/O	**TIMER2 Compare/Capture Channel 2**
	T2	I	**TIMER2 External Input**
	T0	I	**TIMER0 External Input**
12	RST	I	**System Reset**. Hardware reset input, active HIGH.
13	VC	AI	**Analog Input**. 10-bit ADC input (middle sampling rate). The ADC result stores in VCL and VCH registers (2Ch, 2Dh) of MSFR.
14	VB	AI	**Analog Input**. 10-bit ADC input (middle sampling rate). The ADC result stores in VBL and VBH registers (2Ah, 2Bh) of MSFR.
15	VA	AI	**Analog Input**. 10-bit ADC input (middle sampling rate). The ADC result stores in VAL and VAH registers (28h, 29h) of MSFR.
16	ADC3	AI	**Analog Input**. 10-bit ADC input (low sampling rate).The ADC result stores in ADC3L and ADC3H registers (36h, 37h) of MSFR.
	AOUT	AO	**Analog Output**. 8-bit DAC output set by DAC3 register (47h) of MSFR.
17	AVSS	P	**Analog Ground**
18	ADC0	AI	**Analog Input**. 10-bit ADC input (low sampling rate). The ADC result stores in ADC0L and ADC0H registers (30h, 31h) of MSFR.
19	IC	AI	**Phase C Current Input**. 10-bit ADC input (high sampling rate). The ADC result stores in ICL and ICH registers (24h, 25h) of MSFR.

Continued on the following page…

Pin Definitions (Continued)

Pin #	Name	Type	Description
20	IB	AI	**Phase B Current Input**. 10-bit ADC input (high sampling rate). The ADC result stores in IBL and IBH registers (22h, 23h) of MSFR.
21	IA	AI	**Phase A Current Input**. 10-bit ADC input (High sampling rate). The ADC result stores in IAL and IAH registers (20h, 21h) of MSFR.
22	AVDD	P	**5.0 V Analog Voltage Input**. A 0.1 µF (minimum) capacitor should be connected between this pin and AVSS.
23	DVDD	P	**5.0 V Digital Voltage Input**. A 0.1 µF (minimum) capacitor should be connected between this pin and DVSS.
24	V25	O	**2.5 V Voltage Regulator Output**. A 0.1 µF (minimum) capacitor should be connected between this pin and DVSS.
25	DVSS	P	**Digital Ground**
26	VPP	P	**Programming Supply Voltage**. V_{PP} = 12 V for flash memory programming.
27	U	O	**PWM Output**. High-side gate control signal of phase A.
	P02	I/O	**Bit 2 of Port 0**. General-purpose input/output pin with internal pull-down resistor.
28	X	O	**PWM Output**. Low-side gate control signal of phase A.
	P03	I/O	**Bit 3 of Port 0**. General-purpose input/output pin with internal pull-down resistor.
29	V	O	**PWM Output**. High-side gate control signal of phase B.
	P04	I/O	**Bit 4 of Port 0**. General-purpose input/output pin with internal pull-down resistor.
30	Y	O	**PWM Output**. Low-side gate control signal of phase B.
	P05	I/O	**Bit 5 of Port 0**. General-purpose input/output pin with internal pull-down resistor.
31	W	O	**PWM Output**. High-side gate control signal of phase C.
	P06	I/O	**Bit 6 of Port 0**. General-purpose input/output pin with internal pull-down resistor.
32	Z	O	**PWM Output**. Low-side gate control signal of phase C.
	P07	I/O	**Bit 7 of Port 0**. General-purpose input/output pin with internal pull-down resistor.

Notes:

1. Type P: power pin.
2. Type I: digital input pin.
3. Type O: digital output pin.
4. Type I/O: bidirectional input/output pin.
5. Type AI: analog input pin.
6. Type AO: analog output pin.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{PP}	Programming Supply Voltage		-0.7	13	V
V_{DD}	Supply Voltage		-0.7	7	V
V_{VIH}	Voltage of I/O Pin and RST Pin with Respect to GND		-0.2	V_{DD}+0.2	V
V_{AN}	Analog Input Voltage		-0.2	V_{DD}+0.2	V
Θ_{JA}	Thermal Resistance (Junction-to-Air)			80	°C/W
T_A	Operating Ambient Temperature Range		-40	85	°C
T_{STG}	Storage Temperature Range		-65	150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		3,000	V
		Charged Device Model, JESD22-C101		1,250	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{PP}	Programming Supply Voltage	11.8	12.0	12.2	V

Electrical Characteristics

V_{DD}=5 V, and T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SYS}	System Frequency		29.4	30.0	30.6	MHz
f_{SYS}	System Frequency	At -40°C	28.5		31.5	MHz
Power Management						
V_{DD_ON}	Turn-On Voltage				4.5	V
V_{DD_OFF}	Turn-Off Voltage		3.2			V
V_{OUT}	V25 Output Voltage Range	Load Current < 10 mA	2.35	2.50	2.65	V
I_{DD_OPER}	V_{DD} Current at Operation Mode	20 kHz PWM Output	20	29	35	mA
I_{DD_SLEEP}[7]	V_{DD} Current at Sleep Mode	Wake-up Period = 37 ms			500	µA
t_{SLEEP}[7]	Sleep Mode Period	Initial Setting		40		ms
Flash Memory[7]						
V_{PP}	Program/Erase Supply Voltage		11.8	12.0	12.2	V
I_{VPP}	Mass Program Current				8	mA
t_{WRITE}	Page Write Time			1.55		ms
t_{ERASE}	Erase Time		500		600	ms
	Endurance	Erase + Write	1000			cycle
	Data Retention		100			year
10-Bit ADC[7]						
R_I	Input Impedance			3		MΩ
V_{I_MIN}	Minimum Conversion Voltage	Code 000h		0		V
V_{I_MAX}	Maximum Conversion Voltage	Code 3FFh		4		V
DNL	Differential Nonlinearity			±2.0		LSB
INL	Integral Nonlinearity			±2.0		LSB
Err_{ADC}	Offset Error			±3.0		LSB
8-Bit DAC[7]						
R_O	Output Impedance	W/I, W/O Current Bias		10		kΩ
V_{O_MIN}	Minimum Conversion Voltage	Code 00h		50		mV
V_{O_MAX}	Maximum Conversion Voltage	Code FFh		4		V
DNL	Differential Nonlinearity			±1.0		LSB
INL	Integral Nonlinearity			±2.0		LSB
Current Limit						
V_{OCL_OFFSET}	OCL Comparator Offset	OCL = 10h	-50		50	mV
V_{OCH_OFFSET}	OCH Comparator Offset	OCH = C0h	-50		50	mV
V_{SHORT_OFFSET}	SHORT Comparator Offset	SHORT = C0h	-50		50	mV
V_{OCL_RNG}[7]	OCL Comparator Operation Range		0		3.5	V
V_{OCH_RNG}[7]	OCH Comparator Operation Range		1		4	V
V_{SHORT_RNG}[7]	SHORT Comparator Operation Range		1		4	V
I_{BIAS}	Current Source of IA/IB/IC		47.5	50.0	52.5	µA
I_{BIAS}[7]	Current Source of IA/IB/IC	At -40°C	46		51	µA

Continued on the following page…

Electrical Characteristics

V_{DD}=5 V, and T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
GPIO						
V_{IH}	Input High Voltage		3.3			V
V_{IL}	Input Low Voltage				1.8	V
R_{UP}[7]	P1, P2 Pull-Up Resistor			40		kΩ
R_{DOWN}[7]	P0, RST Pull-Down Resistor			45		kΩ
I_{OL}	Low Level Output Current	V_{OL} = 0.4 V	2.3			mA
I_{OH}	High Level Output Current	V_{OH} = 0.8 x V_{DD}	2.5			mA
SPI[7,9]						
$t_{R(SCK)}$	SPI Clock Rising Time	Master Mode, C_L = 20 pF		60		ns
$t_{F(SCK)}$	SPI Clock Falling Time	Master Mode, C_L = 20 pF		60		ns
t_{SCK}	SPI Clock Cycle Time		t_{SYS} x 8			ns
t_{ENS}	SSN Setup Time		t_{SYS} x 3			ns
t_{HS}	SSN Hold Time	Slave Mode	t_{SYS} x 3			ns
t_{DS}	Data Input Setup Time	Master Mode		t_{SYS}		ns
		Slave Mode		t_{SYS}		ns
$t_{DH(MO)}$	Data Output Hold Time	Master Mode		t_{SYS}		ns
$t_{DH(SO)}$	Data Output Hold Time	Slave Mode		t_{SYS}		ns
$t_{DH(MI)}$	Data Input Hold Time	Master Mode		t_{SYS}		ns
$t_{DH(SI)}$	Data Input Hold Time	Slave Mode		t_{SYS}		ns
$t_{DIS(SO)}$	Data Output Disable Time	Slave Mode	t_{SYS} x 3			ns
I^2C Interface[7,10]						
t_{SCL}	I^2C Clock Cycle Time		t_{SYS} x 120			ns
t_{START}	I^2C Start Bit Setup Time			t_{SCL} / 2		ns
t_{STOP}	I^2C Stop Bit Setup Time			t_{SCL} / 2		ns
t_{SETUP}	I^2C Data Setup Time			t_{SYS}		ns
t_{HOLD}	I^2C Data Hold Time			t_{SYS}		ns

Notes:

7. These parameters are not tested in manufacturing.
8. t_{SYS} = 1 / f_{SYS} = 33.33 ns.
9. SPI timing diagrams as Figure 6 and Figure 7.
10. I^2C timing diagram as Figure 8.

Timing Diagrams

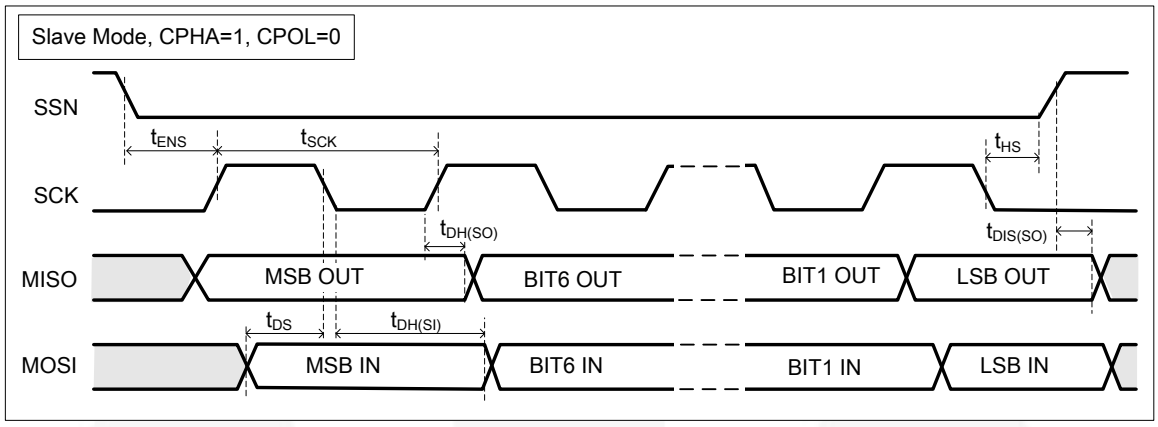


Figure 6. SPI Timing Diagram– Slave Mode

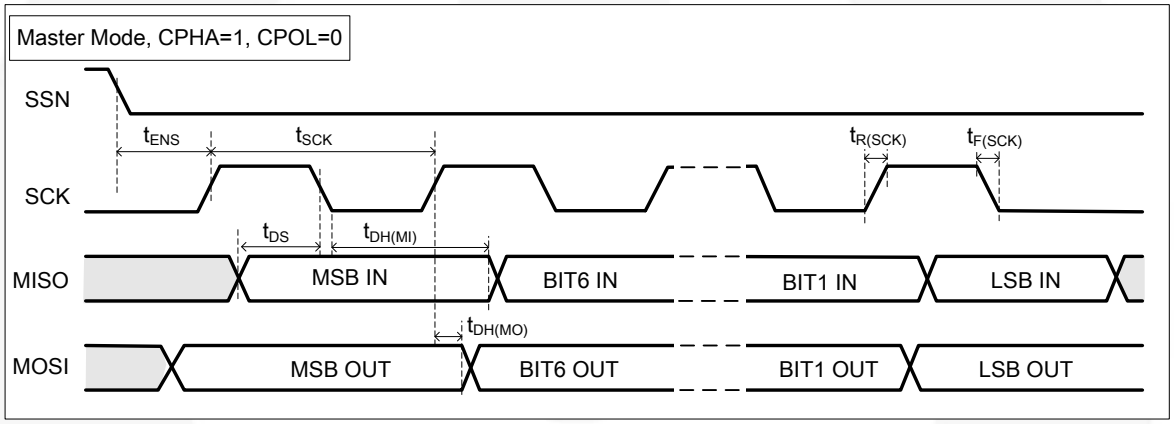


Figure 7. SPI Timing Diagram – Master Mode

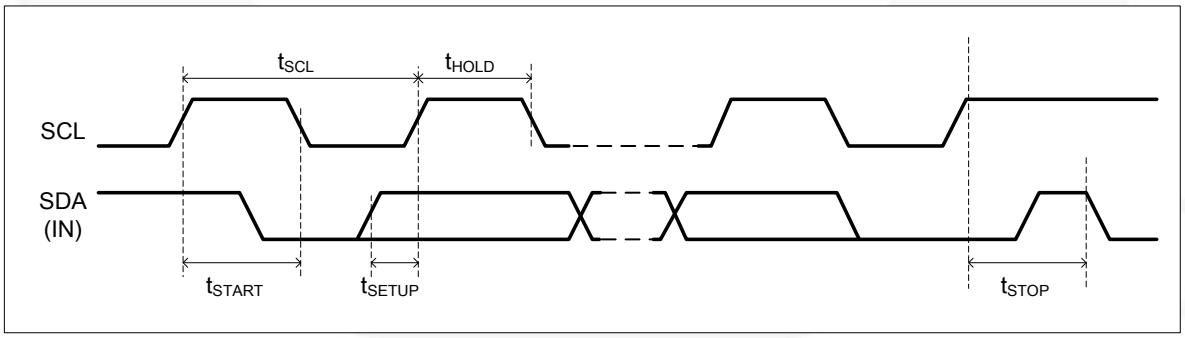


Figure 8. I^2C interface Timing Diagram

Typical Performance Characteristics

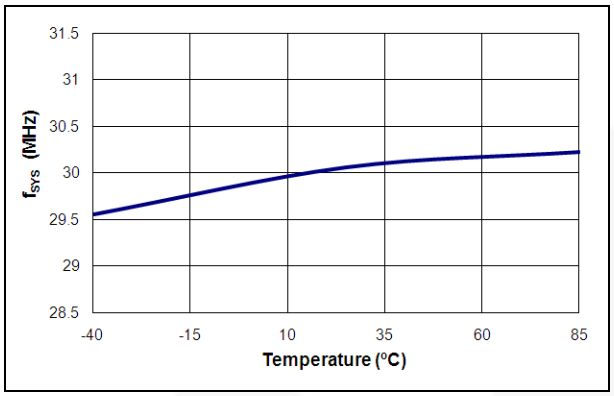


Figure 9. System Frequency (f_{SYS}) vs. Temperature

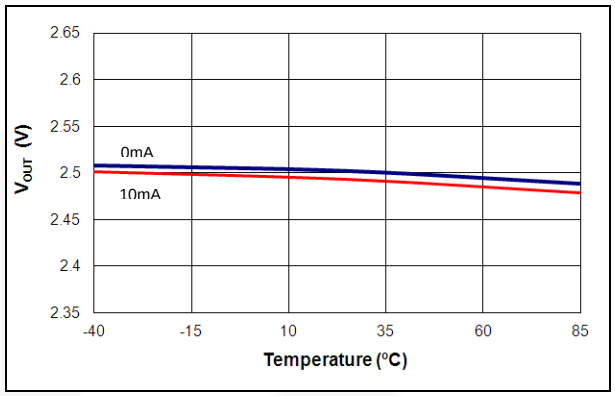


Figure 10. V25 Output Voltage (V_{OUT}) vs. Temperature

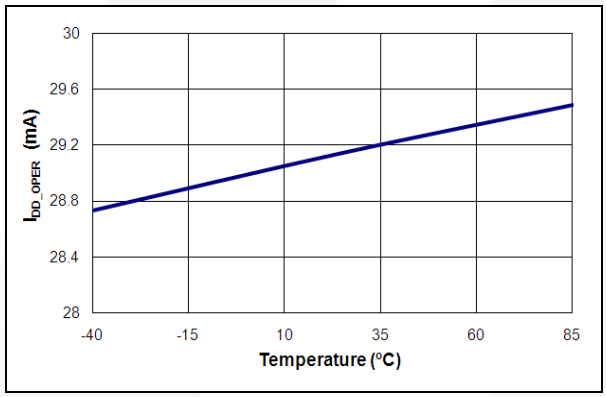


Figure 11. V_{DD} Operation Current (I_{DD_OPPER}) vs. Temperature

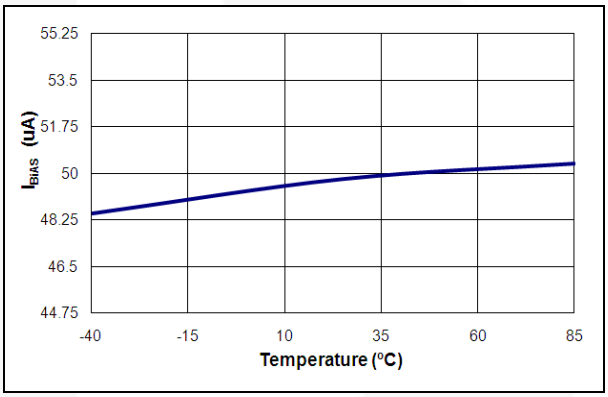


Figure 12. Current Source of IA/IB/IC (I_{BIAS}) vs. Temperature

Functional Description

Advanced Motor Controller (AMC)

The AMC is used for motor driving. It consists of several motor control modules; such as configurable processing core, PWM engine, and angle predictor. Depending on the application, the configurable processing core can be configured with suitable AMC library to perform different motor control algorithms, such as Field-Oriented Control (FOC) or sensorless control.

For example, if the Sensorless library is used as the control algorithm, the configurable processing core obtains the motor current via the internal ADC to estimate the rotor angle. After that, a PWM engine is used to provide the PWM output drive signal to set the correct rotor angle.

If the configurable processing core is configured with the Hall Interface library, the rotor position information is input by GPIO and the rotor angle is estimated using the angle predictor. The PWM engine can provide the appropriate PWM output drive signals for motor driving.

IEC 60730 Safety Functions

The FCM8531RQY is certified to meet the IEC 60730-1 Class-B standards; which cover mechanical, electrical, and electronic appliances. To achieve IEC 60730-1 Class-B requirements, the safety functions are included in the AMC of FCM8531RQY and in compliance with the following structures:

- Single channel using functional test.
- Single channel using periodic functional test.

Follow the procedures recommended in the related application notes to comply with IEC 60730 certification in application designs.

Configurable Processing Core

The AMC can be configured with different libraries, depending on the application, via the Motor Control Development System (MCDS) Integrated Development Environment (IDE). For example: Speed Integral, Sliding Mode, or Hall Interface libraries can be activated.

Speed Integral: this is a sensorless FOC library where D-axis phase error is compensated by a large integrator to achieve more stable speed response. Fewer parameters are required to set with Speed Integral. Applications with static load, such as fans, can adopt this library.

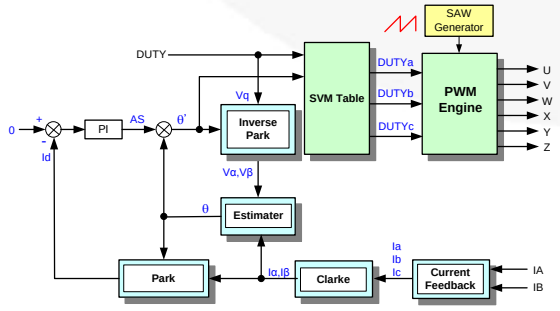


Figure 13. Speed Integral Block Diagram

Sliding Mode: this is a Sensorless FOC library with more parameters to adjust and set. Applications with dynamic loads; such as water pumps, oil pumps, and compressors; can adopt this library.

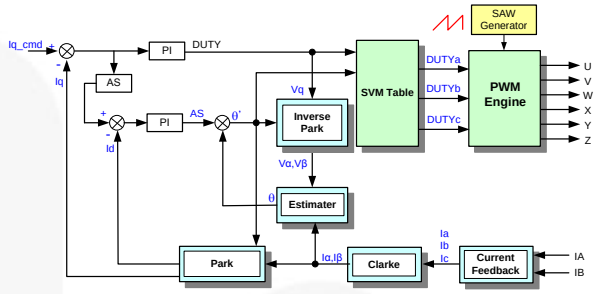


Figure 14. Sliding Mode Block Diagram

Hall Interface: this library is used in Hall sensor motor control systems with square / sinusoidal wave drive.

For more information, please see:

AMC Library User Guide - Speed Integral for FCM8531

AMC Library User Guide - Sliding Mode for FCM8531

AMC Library User Guide - Hall Interface for FCM8531

PWM Engine

The PWM engine includes four circuit modules: saw generator, square-wave PWM generator, sine-wave PWM generator, and PWM MUX.

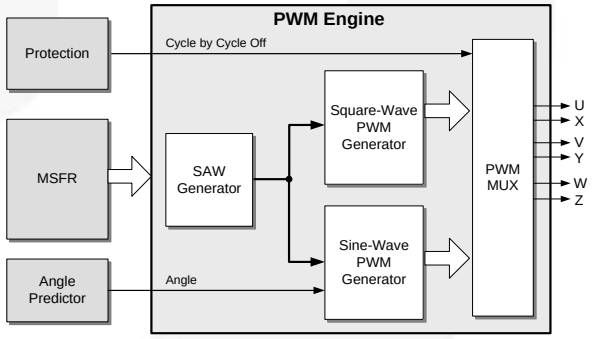


Figure 15. PWM Engine Block Diagram

The saw generator determines the PWM waveform and carrier frequency. There are three modes of carrier waveforms; UP, DOWN, and UP-DOWN; set using the SAWMOD bit in the SAWCNTL register in MSFR (Motor Special Function Registers) (*see* **Error! Reference source not found.**).

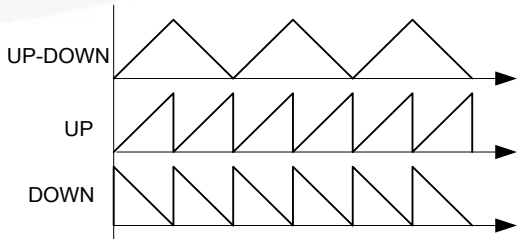


Figure 16. SAW Output Mode

The PWM carrier frequency is decided by the PRESCAL and the POSSCAL in the SPRDH/L and SAWCNTL registers in MSFR. The PWM frequency, when SAW is in the UP-DOWN Mode, can be obtained using the following formula:

$$f_{PWM} = \frac{f_{SYS}}{PRESCAL[1:0] \times POSSCAL[2:0] \times SPRDH/L[10:0] \times 2} \quad (1)$$

The PWM frequency formula for SAW in the UP and DOWN modes is calculated by:

$$f_{PWM} = \frac{f_{SYS}}{PRESCAL[1:0] \times POSSCAL[2:0] \times SPRDH/L[10:0]} \quad (2)$$

Please refer to AN-8202—FCM8531 User Manual - Hardware Description for details.

SAW Generator

The **Square-Wave PWM Generator** generates square-wave PWM signals with a default pattern based on a built-in table of default square-waves (*see Table 1*). Corresponding PWM output signals are determined by the pattern of Hall input signals or the Hall register, while direction is determined by the CW setting.

In addition to generating default square-wave PWM output waveforms, a customizable user-defined square-wave table is also provided. This enables users to define special square-wave output waveforms according to application requirements.

Table 1. Default Square-Wave Table

CW	Hall	Hall	U-V-W	X-Y-Z
X	0 0 0	0	0 0 0	0 0 0
X	1 1 1	7	0 0 0	0 0 0
1	0 0 1	1	P 0 0	Pb 1 0
1	0 1 1	3	0 0 P	0 1 Pb
1	0 1 0	2	0 0 P	1 0 Pb
1	1 1 0	6	0 P 0	1 Pb 0
1	1 0 0	4	0 P 0	0 Pb 1
1	1 0 1	5	P 0 0	Pb 0 1
0	1 0 1	5	0 0 P	1 0 Pb
0	1 0 0	4	0 0 P	0 1 Pb
0	1 1 0	6	P 0 0	Pb 1 0
0	0 1 0	2	P 0 0	Pb 0 1
0	0 1 1	3	0 P 0	0 Pb 1
0	0 0 1	1	0 P 0	1 Pb 0

Notes:

11. X: don't care.
12. P: PWM.
13. Pb: PWM inverse.

In square-wave mode, the PWM duty is determined by the DUTYA and DUTYAL registers in MSFR, with a total of 11 bits (*see Figure 17*).

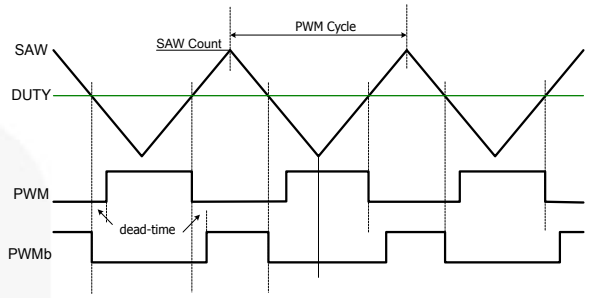


Figure 17. PWM Output

The **Sine-Wave PWM Generator** includes a Space Vector Modulation (SVM) circuit responsible for generating sine-wave PWM output waveforms. In addition to built-in sinusoidal waveform modulation, which is popular in many applications, a table allows users to customize PWM output waveforms.

In sine-wave mode, the PWM duty is determined by the DUTYA register in MSFR. When using the Hall interface library, the PWM engine starts the motor in square-wave mode. After the angle predictor can accurately predict angles, the PWM engine automatically shifts to sine-wave mode. As shown in Figure 18 (CW=0) and Figure 19 (CW=1), corresponding PWM signals are generated based on the angle estimated from Hall input signals.

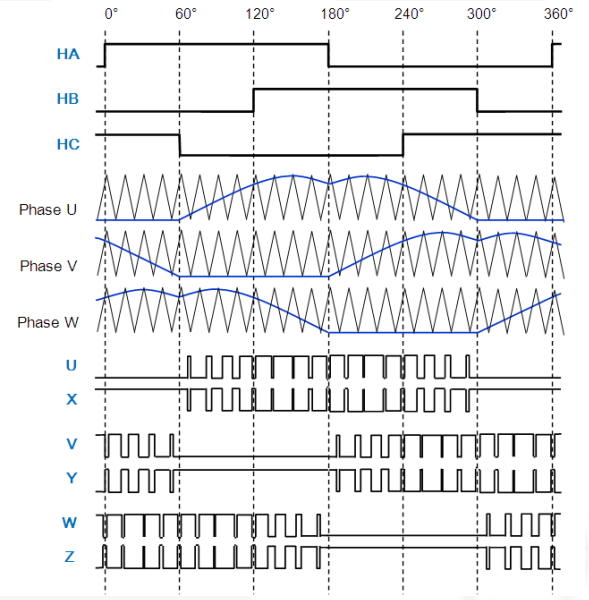


Figure 18. Default Sine-Wave PWM Output (CW=0)

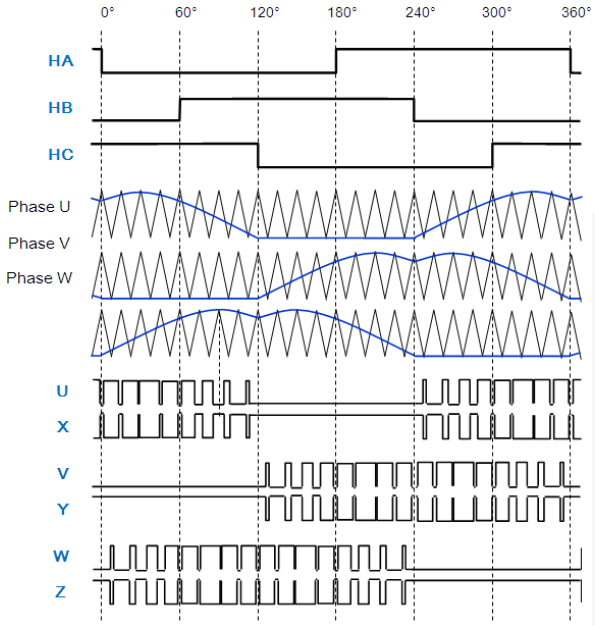


Figure 19. Default Sine-Wave PWM Output (CW=1)

Angle Predictor

When using Hall sensors for sine-wave control, the Hall signals are used to accurately predict the rotor position of the motor. This information is provided to the SVM circuit to calculate the space vector. Two circuits are included in the angle predictor: Hall signal filter and leading-angle shifter.

The Hall signal filter is responsible for Hall signal debounce, blanking, regulation, and inversion.

The rotor position can be adjusted using the leading-angle shifter. This can compensate for the current lag caused by motor winding inductance and further improve the motor efficiency.

Embedded MCU

System flow control, user interface, input/output, and communication interface can be programmed and set in the embedded MCU. The instruction set is fully compatible with MCS®51; therefore, a standard 805x assembler and compiler can be used for development.

Since FCM8531 uses advanced instruction architecture that only needs one system clock per instruction set, its computation speed is greatly improved compared with the conventional 8051 MCU, which needs 12 system clocks per instruction set.

In addition to the normal 8051 MCU functions; such as GPIO, TIMER0/1/2, ISR, and UART; other communication interfaces; such as SPI, I^2C, and Watchdog Timer (WDT) functions; are also integrated into the embedded MCU.

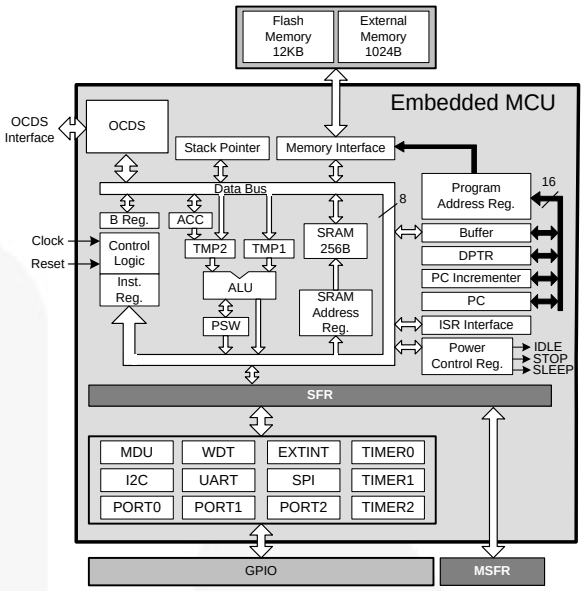


Figure 20. Embedded MCU Block Diagram

Memory Map

The 12KB flash program memory is divided into two parts. In the first section of the memory area, addresses 0000h~2EFFh, are used to store programs. Addresses higher than 2EFFh are in the special area, including two groups of user-definable wave tables and one lock byte. When 0 is written into the highest bit of the lock byte, the OCDS function is disabled. When 0 is written into any other bit, the flash memory is encrypted to secure the program code.

Flash memory must first be erased and then re-written.

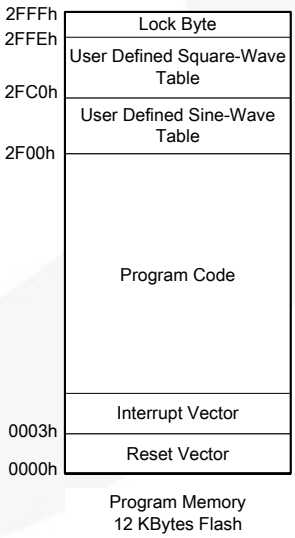


Figure 21. Program Memory Map

Four groups of register banks are provided in the 256-byte internal SRAM data memory. The first 128 bytes (00h~7Fh) of the internal data memory can be read by immediate addressing or indirect addressing. The latter 128 bytes (80h~FFh) in the memory are overlapped with SFR. Accessing data in SRAM must use indirect addressing, while SFR uses immediate addressing to read and write.

The 1024 bytes of external SRAM data memory are addressed by a 16-bit DPTR and use an MOVX instruction for accessing.

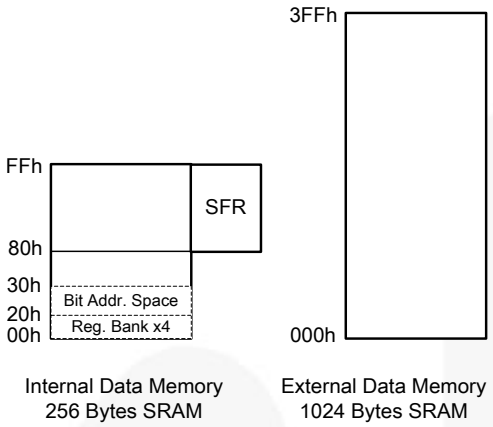


Figure 22. Data Memory Map

Multiplication-Division Unit (MDU)

The MDU, used for parallel calculations, can process 32-bit division, 16-bit multiplication, and 32-bit displacement and normalization calculations.

After setting the calculation model, the MDU begins to execute calculation. Meanwhile, MCU are freed to continue the subsequent flow without pausing. After calculation is completed, the result is stored in SFR.

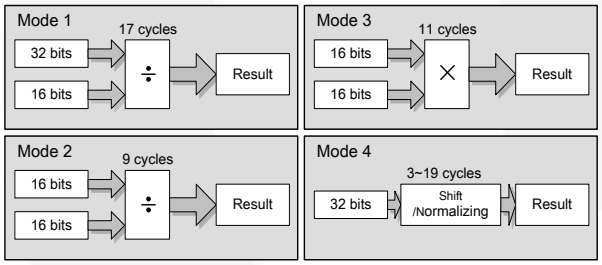


Figure 23. MDU Mode

GPIO (General-Purpose Input / Output)

The FCM8531 has three GPIO ports: P0[7:2], P1[7:0], and P2[6:4]. The output can be set to direct drive or open drain through DIR0, DIR1, and DIR2 of the SFR. Inside the FCM8531, P0[7:2] is pulled down to GND by internal resistors and other digital IOs are pulled up to 5 V with internal resistors.

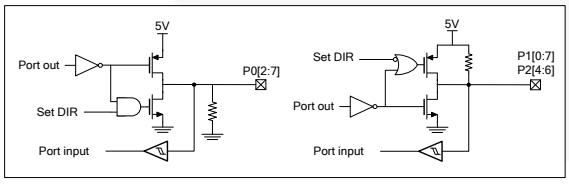


Figure 24. GPIO Driver & Buffer

P0[7:2] can be defined as a GPIO or PWM output signal (U, V, W, X, Y, and Z) by using P0_CFG of the SFR. After reset, P0[7:2] is pre-set to a PWM output signal and the other DIO pins are pre-set as GPIO (*see Table 2*).

The multi-function pins P1[7:0] and P2[6:4] can be set through IO_CFG (F9h) of the SFR (*see Table 3 and Table 4).*

Table 2. Port 0 Function Configuration

P0_CFG	0 (Default)	1
Bit 7	PWM Z Channel	P07
Bit 6	PWM W Channel	P06
Bit 5	PWM Y Channel	P05
Bit 4	PWM V Channel	P04
Bit 3	PWM X Channel	P03
Bit 2	PWM U Channel	P02

Table 3. Port 1 Function Configuration

Pin	IO_CFG[1:0]			
	00 (Default)	01	10	11
P10	RX	SCL	SPSSN	SPSSN
P11	TX	SDA	MOSI	MOSI
P12	SCL	RX	MISO	MISO
P13	SDA	TX	SCK	SCK
P14	SPSSN	SPSSN	RX	SCL
P15	MOSI	MISO	TX	SDA
P16	MISO	MISO	SCL	RX
P17	SCK	SCK	SDA	TX

Table 4. Port 2 Function Configuration

Pin	IO_CFG[3:2]			
	00 (Default)	01	10	11
P24	CC0	CC0	T0	T2
P25	CC1	CC1	T1	T2EX
P26	CC2	CC2	T2	T0

Interrupt

The FCM8531 provides 16 interrupt sources *(see Table 5)* that can be divided into five priority groups and four priority levels.

Most of the interrupt settings are identical to the standard MCS51, except for the following:

- The external interrupt 0 input source pin can be assigned to P24 or P26 through IO_CFG of the SFR (Special Function Registers). The interrupt trigger mode can be set to low-level trigger and falling-edge trigger.
- External interrupt 1 is input via P25. The interrupt trigger mode can be set to low-level trigger and falling-edge trigger.
- The external interrupt 12 input signal can be assigned to P1[6:0]. When an interrupt occurs, INT12_STA can be used to inspect which pin has been triggered. The interrupt trigger mode can be set to low-level trigger and falling-edge trigger.

- The other interrupt sources include: V_{DD} low-voltage warnings, ADC transformation completion trigger, Hall signal trigger, slow Hall signal, Hall signal error, and short-circuit sensing. These can be used for developing the motor control system.
- When an interrupt occurs, the int$_{er}$rupt service executes interrupt service programs at the specified interrupt vector addresses. During an interrupt, another interrupt is only permitted if an interrupt source with a higher priority level occurs.

Table 5. Interrupt Vector

Interrupt Source	Interrupt Vector	Symbol	Trigger
External Interrupt 0	0003h	EX0	Fall, Low
Timer 0 Overflow	000Bh	ET0	
External Interrupt 1	0013h	EX1	Fall, Low
Timer 1 Overflow	001Bh	ET1	
Serial	0023h	ES0	
Timer2	002Bh	ET2	
I^2C	0043h	EX7	
SPI	004Bh	EX2	
COM0	0053h	EX3	Rise, Fall
COM1	005Bh	EX4	Rise
COM2	0063h	EX5	Rise
FAULT	008Bh	EX8	
ADC Ready Trigger	0093h	EX9	
Hall Edge	009Bh	EX10	Rise, Fall, Rise & Fall
AMC	00A3h	EX11	Rise
External Interrupt 12	00ABh	EX12	Rise, Fall, Rise & Fall

Watchdog Timer (WDT)

The watchdog timer is a 15-bit counter that increases every 384 or 6144 system cycles. If there are software or hardware abnormalities, it resets automatically.

When the watchdog timer is set in WDTREL of the SFR, it begins to count when the SWDT bit of SFR IEN1 is set to 1. When it counts to 7FFCh and a timeout occurs, it internally resets.

The watchdog timer must be refreshed before timeout. If unexpected errors occur, the watchdog timer is not refreshed. After timeout, the program restarts.

Motor Special Function Registers (MSFRs)

MSFRs are registers used exclusively for motor control modules. They are accessed through MCU SFRs.

Parameters such as motor control, Hall signal configure, waveform type, PWM engine, and over-current protection level can be set in MSFRs.

The ADC and controller status (e.g., Fault status, Hall status, and PWM status) can be obtained via MSFRs.

ADC and DAC

The analog signal input pins (IA, IB, IC, VA, VB, VC, ADC0, and ADC3/AOUT) can be programmed for current sensing, voltage feedback, speed control, over-temperature protection, or other analog signal inputs; depending on the application. The ADC3/AOUT pin location can be used as 0~4 V analog output. The output voltage is set via the DAC in the MSFR.

The internal ADC is divided into three groups according to the speed of the sampling rate (*see Table 6*).

Table 6. ADC Sampling Rate

Sampling Rate Speed	Channel	Convert Period
High	IA, IB, IC	1 ADC Trigger
Mid	VA, VB, VC	4 ADC Trigger
Low	ADC0, ADC3	16 ADC Trigger

Pins IA, IB, and IC are preset as current-sensing input.

When ADC trigger signals occur, the sample-and-hold circuits retrieve the voltage to be converted. Then it goes through a pre-amplifier to a 10-bit A-D converter. After conversion, it is stored in MSFR and generates an ADC-ready interrupt.

ADC trigger mode has four sub-modes: SAW peak, SAW valley, Timer0, and manual trigger.

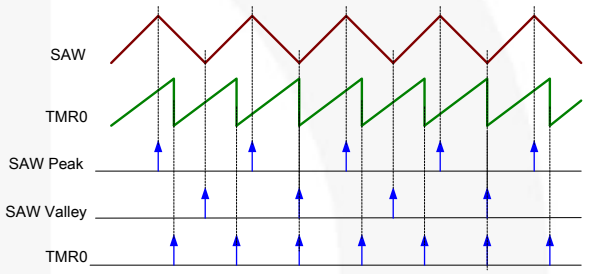


Figure 25. ADC Trigger Mode

Protections

Protection functions are provided for Hall signal error protection and over-current (cycle-by-cycle) protection.

When a Hall signal error occurs, the PWM pulse is turned off until the error status is released.

Cycle-by-cycle over-current protection (OCP) monitors every PWM cycle. If over-current is detected, the PWM is turned off until the next cycle.

In addition to the cycle-by-cycle OCP, other protections generate interrupts.

Table 7. Fault and Protection

Type	Condition	Action
Hall Slow	Hall Period Overflow	Interrupt 8
Short A	IA > I_{SHORT}	Interrupt 8
Short B	IB > I_{SHORT}	Interrupt 8
Short C	IC > I_{SHORT}	Interrupt 8
Hall Error	Hall Sensor = 111 or 000	Interrupt 8 PWM Off
OC High	IA / IB / IC > I_{OCH}	PWM Off
OC Low	IA / IB / IC < I_{OCL}	PWM off

Current Protections

There are three methods of current protection: negative over current, positive over current, and short-circuit sensing. The protection points can be set via the OCL, OCH, and SHORT of MSFR. After a protection is triggered, PWM is immediately turned off until the next cycle (cycle-by-cycle).

When the input voltage is higher than the SHORT voltage, an EX8 interrupt is generated. Corresponding measures can be executed to protect system based on requirements of application systems.

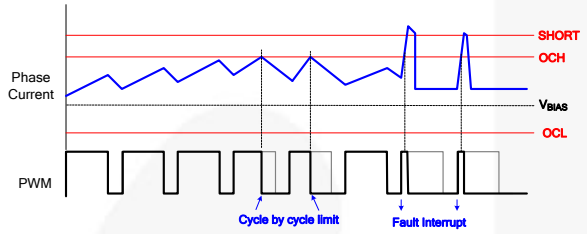


Figure 26. Current Protection (Square-Wave)

Each current-sensing pin (IA, IB, and IC) has an output of 50 µA of bias current. The recommended setting for the bias voltage is 2.0 V (R_{BIAS}= 40 kΩ).

$$V_{BIAS} = I_{BIAS} \times R_{BIAS} \quad (3)$$

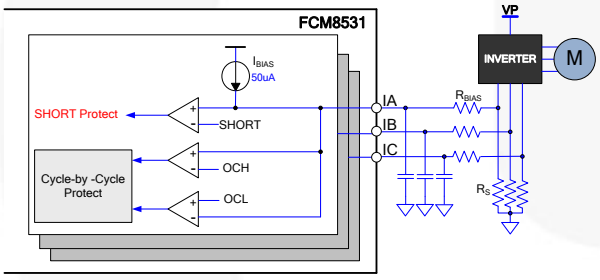


Figure 27. Current Feedback Circuit

Power Management

If V_{DD} is > VDD_{ON}, the reset status takes about 2 ms to be released.

FCM8531 provides three kinds of power-saving modes:

- In IDLE mode; execution of MCU programs pauses, but the peripheral I/O circuits continue to work (e.g. PWM, external interrupt, timing, serial output, etc.).
- In STOP mode; execution of programs, digital I/O interfaces, and all digital circuits pause. This mode continues until the occurrence of an EX0/EX1 external interrupt or a system reset.
- In SLEEP mode, the MCU and AMC are both turned off. At this moment, the alarm timer begins to count. After a timeout, the MCU and AMC are turned on again.

Development Supports

Fairchild provides the Motor Control Development System (MCDS) Integrated Development Environment (IDE). On Microsoft® Windows platforms, functions such as project building, program code generation, compilation, In-System Programming (ISP), and On-Chip Debug Support (OCDS) are supported. This facilitates software development and debugging.

For detailed information please see: *User Guide for MCDS IDE of FCM8531.*

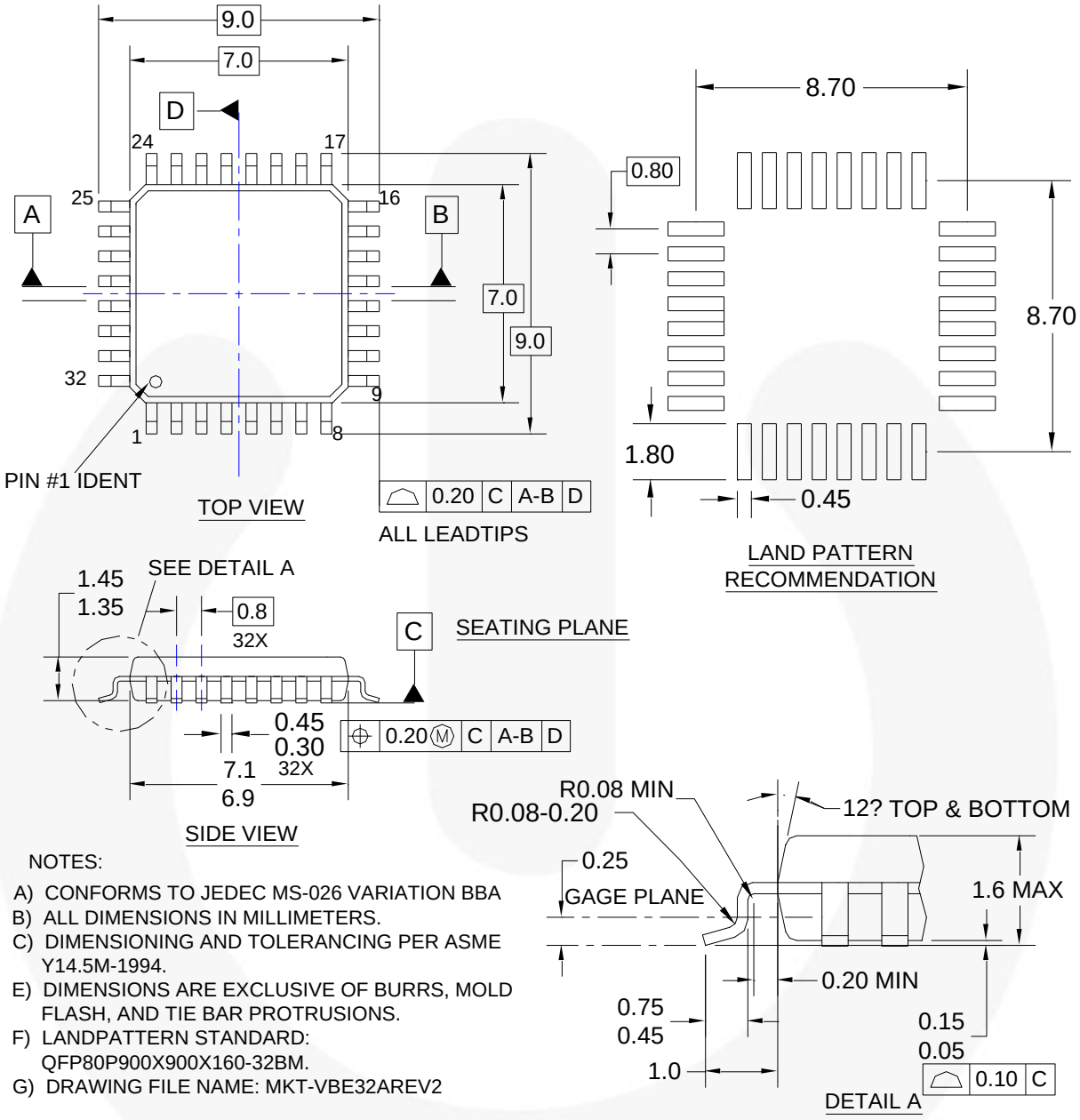
Table 8. SFRs (Special Function Registers) Map

Hex	X000	X001	X010	X011	X100	X101	X110	X111	Hex
F8	P0_CFG	IO_CFG	INT12_CFG	INT12_STA	DIR0	DIR1	DIR2		**FF**
F0	B							SRST	**F7**
E8		MD0	MD1	MD2	MD3	MD4	MD5	ARCON	**EF**
E0	ACC	SPSTA	SPCON	SPDAT	SPSSN				**E7**
D8	ADCON		I2CDAT	I2CADR	I2CCON	I2CSTA			**DF**
D0	PSW								**D7**
C8	T2CON		CRCL	CRCH	TL2	TH2			**CF**
C0	IRCON	CCEN	CCL1	CCH1	CCL2	CCH2			**C7**
B8	IEN1	IP1	SRELH					IRCON2	**BF**
B0	MTX0	MTX1	MTX2	MTX3	MRX0	MRX1	MRX2	MRX3	**B7**
A8	IEN0	IP0	SRELL						**AF**
A0	P2								**A7**
98	SCON	SBUF	IEN2						**9F**
90	P1		DPS	DPC			MSFRADR	MSFRDAT	**97**
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON		**8F**
80	P0	SP	DPL	DPH	DPL1	DPH1	WDTREL	PCON	**87**

Table 9. MSFRs (Motor Special Function Registers) Map

Hex	X000	X001	X010	X011	X100	X101	X110	X111	Hex
78									**7F**
70									**78**
68									**6F**
60									**67**
58									**5F**
50									**57**
48									**4F**
40	MBUSCTL	PT01	PT23	SLEEP	OCH	OCL	SHORT	DACO	**47**
38	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ANGLE	MSTAT	**3F**
30	ADC0L	ADC0H					ADC3L	ADC3H	**37**
28	VAL	VAH	VBL	VBH	VCL	VCH	ADCINX	BAK	**2F**
20	IAL	IAH	IBL	IBH	ICL	ICH	OCCNTL	OCSTA	**27**
18	HALMXU	HALFLT	HALSTA	HALINT	HPERL	HPERM	HPERH	ADCCFG	**1F**
10	Reserved	Reserved		Reserved	Reserved	Reserved	Reserved	Reserved	**17**
08	PWMCFG	SAWCNTL	SPRDL	SPRDH	SDLYBL	SDLYBH	SDLYCL	SDLYCH	**0F**
00	MCNTL	ANGCTL	AS	ANGDET	DUTYAL	DUTYA	DUTYB	DUTYC	**07**

Physical Dimensions



NOTES:

A) CONFORMS TO JEDEC MS-026 VARIATION BBA
B) ALL DIMENSIONS IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
E) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR PROTRUSIONS.
F) LANDPATTERN STANDARD: QFP80P900X900X160-32BM.
G) DRAWING FILE NAME: MKT-VBE32AREV2

Figure 28. 32-Low-Profile, Quad, Flat Pack Package (LQFP)

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SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
TinyBoost®
TinyBuck®
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
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ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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