

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

Designed for broadband commercial and industrial applications with frequencies up to 1000 MHz. The high gain and broadband performance of this device make it ideal for large-signal, common-source amplifier applications in 28 volt base station equipment.

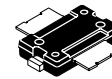
- Typical Performance at 945 MHz, 28 Volts
 - Output Power — 45 Watts PEP
 - Power Gain — 19 dB
 - Efficiency — 41% (Two Tones)
 - IMD — -31 dBc
- Integrated ESD Protection
- Guaranteed Ruggedness @ Load VSWR = 5:1, @ 28 Vdc, 945 MHz, 45 Watts CW Output Power

Features

- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Dual-Lead Bolt-down Plastic Package Can Also Be Used As Surface Mount.
- 200°C Capable Plastic Package
- N Suffix Indicates Lead-Free Terminations. RoHS Compliant.
- TO-270-2 Available in Tape and Reel. R1 Suffix = 500 Units per 24 mm, 13 inch Reel.

MRF9045NR1

**945 MHz, 45 W, 28 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFET**



**CASE 1265-09, STYLE 1
TO-270-2
PLASTIC**

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	- 0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	- 0.5, + 15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	177 1.18	W W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.85	$^\circ\text{C}/\text{W}$

Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	$^\circ\text{C}$

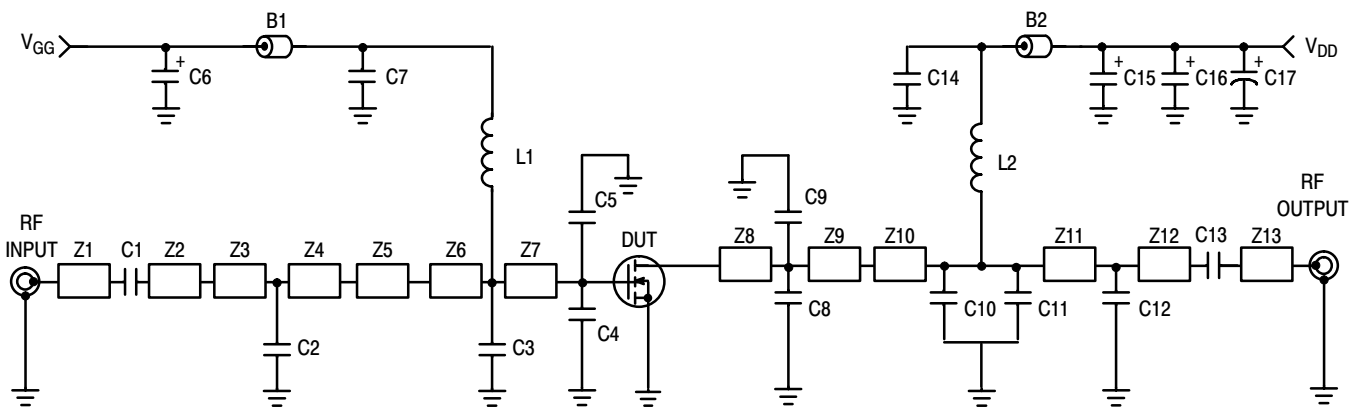
1. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

NOT RECOMMENDED FOR NEW DESIGN

NOT RECOMMENDED FOR NEW DESIGN

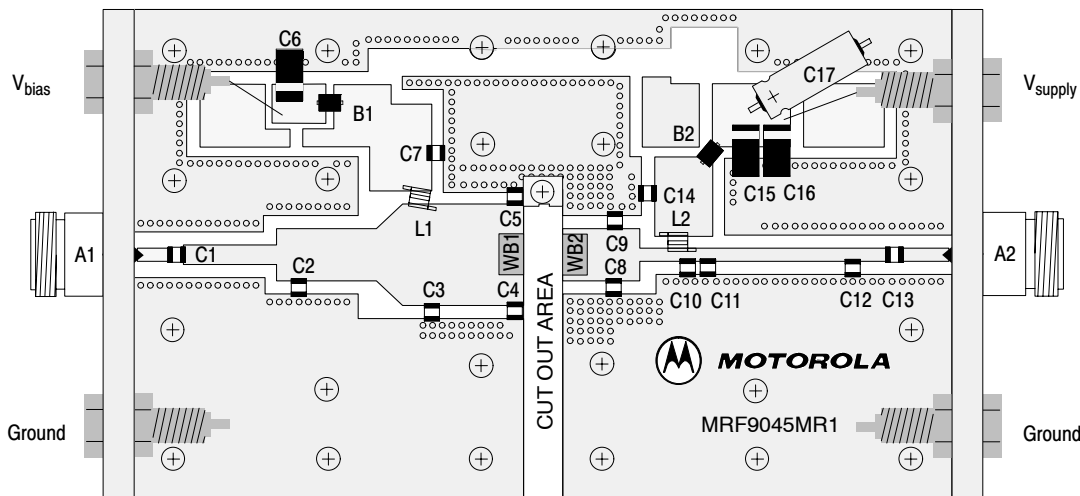
Table 5. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 150\ \mu\text{Adc}$)	$V_{GS(th)}$	2	2.8	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_D = 350\ \text{mA}$)	$V_{GS(Q)}$	3	3.7	5	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1\ \text{A}$)	$V_{DS(on)}$	—	0.22	0.4	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 3\ \text{A}$)	g_{fs}	—	4	—	S
Dynamic Characteristics					
Input Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{iss}	—	70	—	pF
Output Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{oss}	—	38	—	pF
Reverse Transfer Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	1.7	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\ \text{mA}$, $f_1 = 945.0\ \text{MHz}$, $f_2 = 945.1\ \text{MHz}$)	G_{ps}	17	19	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\ \text{mA}$, $f_1 = 945.0\ \text{MHz}$, $f_2 = 945.1\ \text{MHz}$)	η	38	41	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\ \text{mA}$, $f_1 = 945.0\ \text{MHz}$, $f_2 = 945.1\ \text{MHz}$)	IMD	—	-31	-28	dBc
Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\ \text{mA}$, $f_1 = 945.0\ \text{MHz}$, $f_2 = 945.1\ \text{MHz}$)	IRL	—	-14	-9	dB
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\ \text{mA}$, $f_1 = 930.0\ \text{MHz}$, $f_2 = 930.1\ \text{MHz}$ and $f_1 = 960.0\ \text{MHz}$, $f_2 = 960.1\ \text{MHz}$)	G_{ps}	—	19	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\ \text{mA}$, $f_1 = 930.0\ \text{MHz}$, $f_2 = 930.1\ \text{MHz}$ and $f_1 = 960.0\ \text{MHz}$, $f_2 = 960.1\ \text{MHz}$)	η	—	41	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\ \text{mA}$, $f_1 = 930.0\ \text{MHz}$, $f_2 = 930.1\ \text{MHz}$ and $f_1 = 960.0\ \text{MHz}$, $f_2 = 960.1\ \text{MHz}$)	IMD	—	-31	—	dBc
Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 45\text{ W PEP}$, $I_{DQ} = 350\ \text{mA}$, $f_1 = 930.0\ \text{MHz}$, $f_2 = 930.1\ \text{MHz}$ and $f_1 = 960.0\ \text{MHz}$, $f_2 = 960.1\ \text{MHz}$)	IRL	—	-13	—	dB



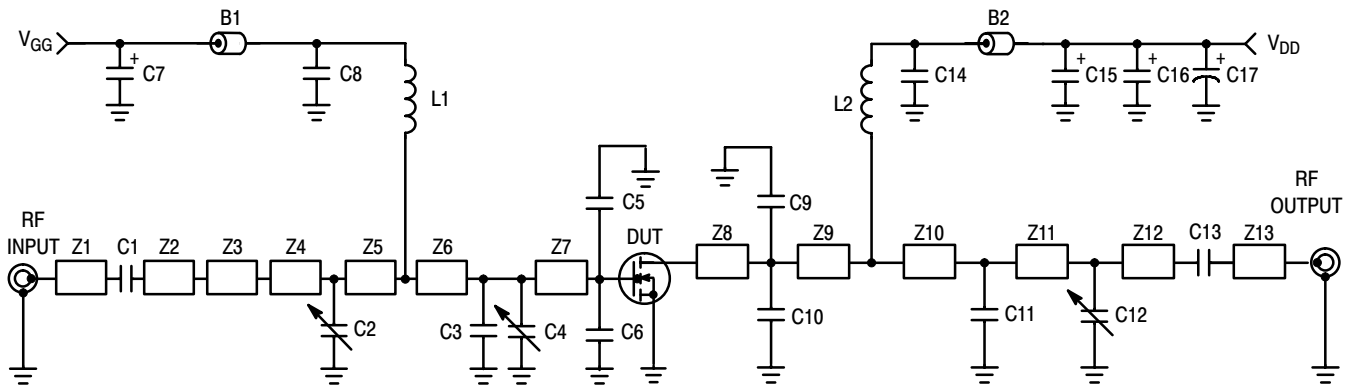
B1, B2	Short Ferrite Beads, Surface Mount	Z3	0.14" x 0.32" Microstrip
C1, C7, C13, C14	47 pF Chip Capacitors	Z4	0.47" x 0.32" Microstrip
C2, C8	2.7 pF Chip Capacitors	Z5	0.16" x 0.32" x 0.62" Taper
C3	3.9 pF Chip Capacitor	Z6	0.18" x 0.62" Microstrip
C4, C5, C8, C9	10 pF Chip Capacitors	Z7	0.56" x 0.62" Microstrip
C6, C15, C16	10 μ F, 35 V Tantalum Surface Mount Capacitors	Z8	0.33" x 0.32" Microstrip
C10	2.2 pF Chip Capacitor	Z9	0.14" x 0.32" Microstrip
C11	4.7 pF Chip Capacitor	Z10	0.36" x 0.08" Microstrip
C12	1.2 pF Chip Capacitor	Z11	1.01" x 0.08" Microstrip
C17	220 μ F, 50 V Electrolytic Capacitor	Z12	0.15" x 0.08" Microstrip
L1, L2	12.5 nH Inductors	Z13	0.29" x 0.08" Microstrip
Z1	0.20" x 0.08" Microstrip		
Z2	0.57" x 0.12" Microstrip		

Figure 1. MRF9045NR1 930-960 MHz Broadband Test Circuit Schematic



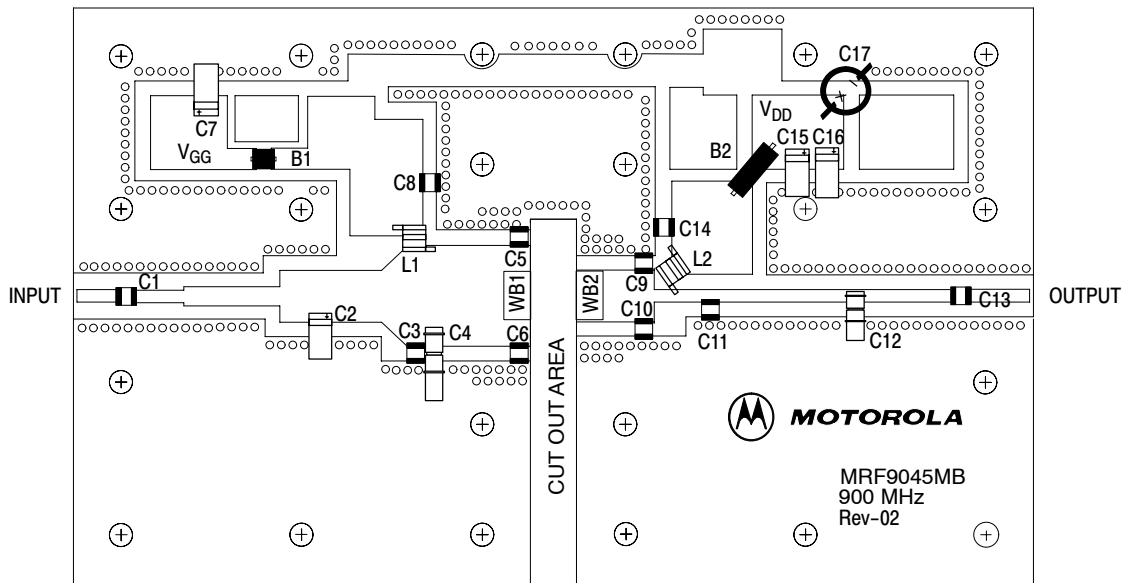
Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. MRF9045NR1 930-960 MHz Broadband Test Circuit Component Layout



B1	Short Ferrite Bead	Z1	0.260" x 0.060" Microstrip
B2	Long Ferrite Bead	Z2	0.240" x 0.060" Microstrip
C1, C8, C13, C14	47 pF Chip Capacitors	Z3	0.500" x 0.100" Microstrip
C2	0.4 - 2.5 pF Variable Capacitor, Johanson Gigatrim	Z4	0.215" x 0.270" Microstrip
C3	3.6 pF Chip Capacitor	Z5	0.315" x 0.270" Microstrip
C4	0.8 - 8.0 pF Variable Capacitor, Johanson Gigatrim	Z6	0.160" x 0.270" x 0.520" Taper
C5, C6, C9, C10	10 pF Chip Capacitors	Z7	0.285" x 0.520" Microstrip
C7, C15, C16	10 μF, 35 V Tantalum Chip Capacitors	Z8	0.140" x 0.270" Microstrip
C11	7.5 pF Chip Capacitor	Z9	0.450" x 0.270" Microstrip
C12	0.6 - 4.5 pF Variable Capacitor, Johanson Gigatrim	Z10	0.250" x 0.060" Microstrip
C17	220 μF Electrolytic Chip Capacitor	Z11	0.720" x 0.060" Microstrip
L1, L2	12.5 nH Surface Mount Inductors	Z12	0.490" x 0.060" Microstrip
WB1, WB2	10 mil Brass Wear Blocks	Z13	0.290" x 0.060" Microstrip
		Board	Taconic RF-35-0300, ε _r = 3.5

Figure 3. MRF9045NR1 930-960 MHz Broadband Test Circuit Schematic



Freescle has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescle Semiconductor signature/logo. PCBs may have either Motorola or Freescle markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 4. MRF9045NR1 930-960 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

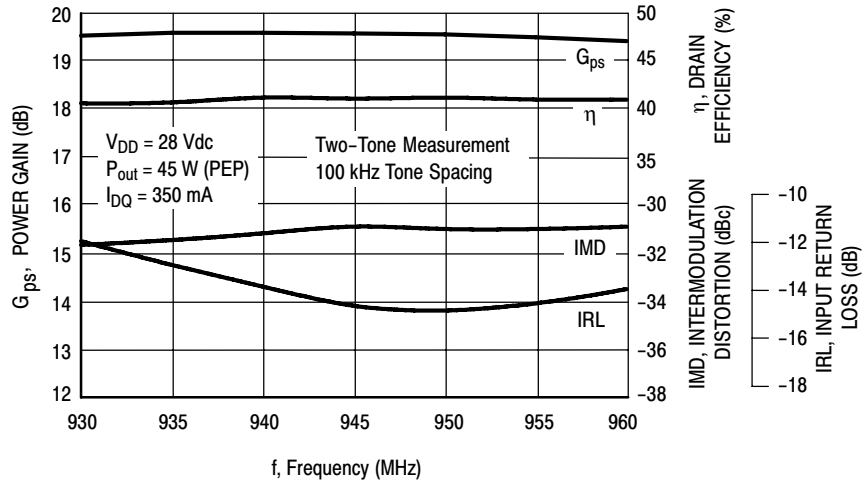


Figure 5. Class AB Broadband Circuit Performance

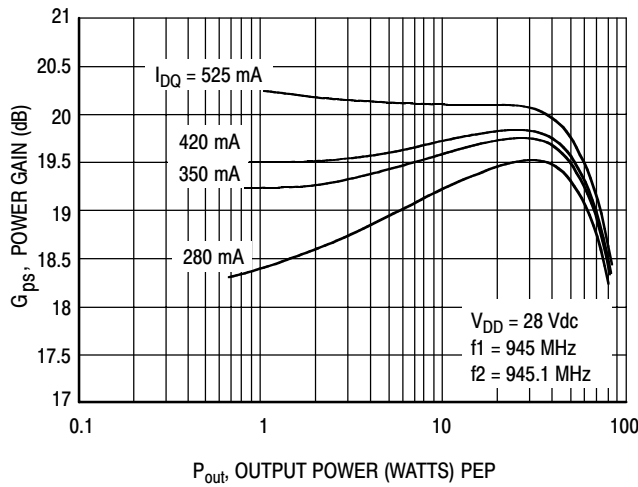


Figure 6. Power Gain versus Output Power

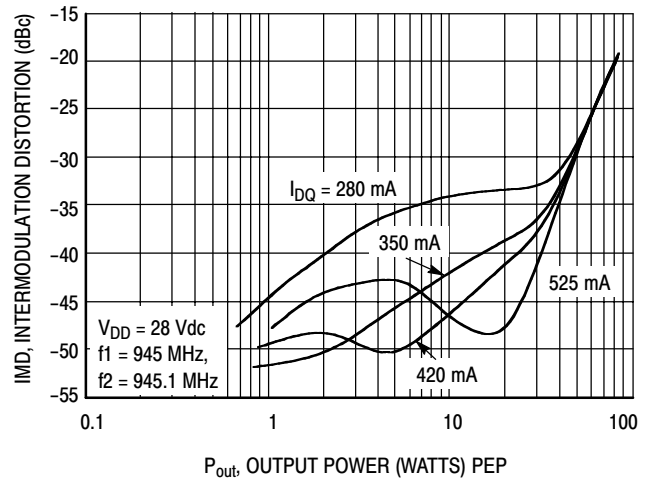


Figure 7. Intermodulation Distortion versus Output Power

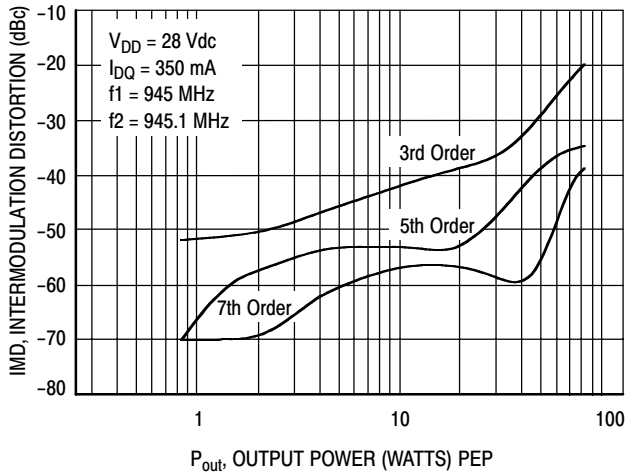


Figure 8. Intermodulation Distortion Products versus Output Power

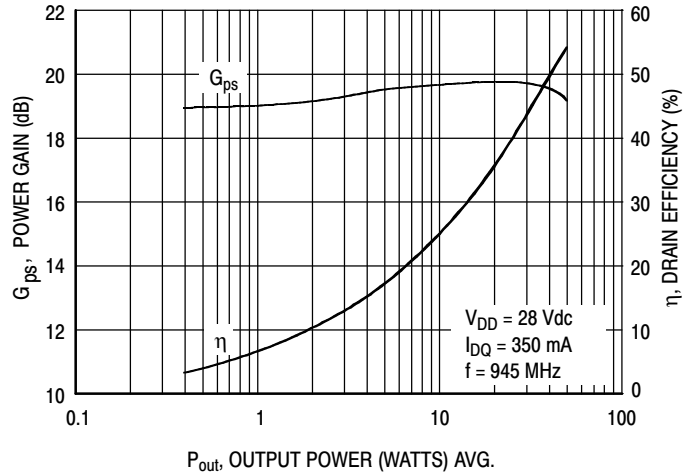


Figure 9. Power Gain and Efficiency versus Output Power

TYPICAL CHARACTERISTICS

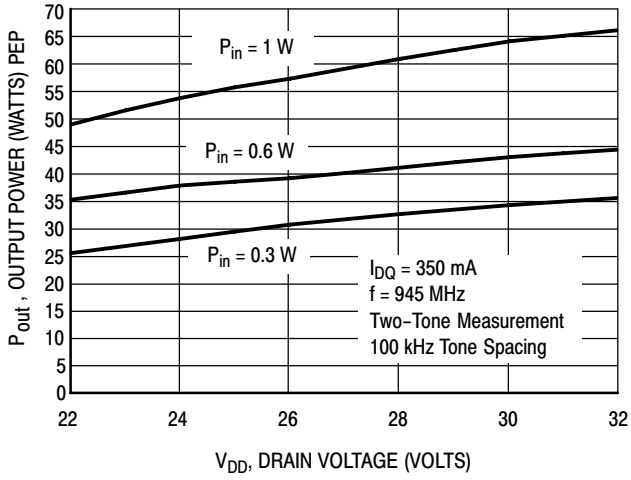
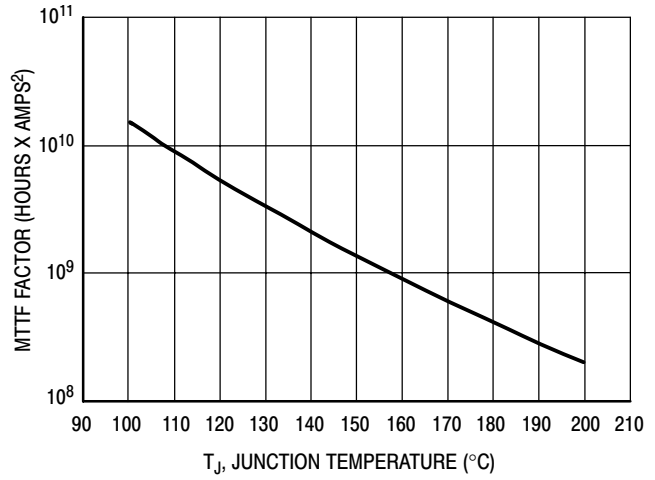
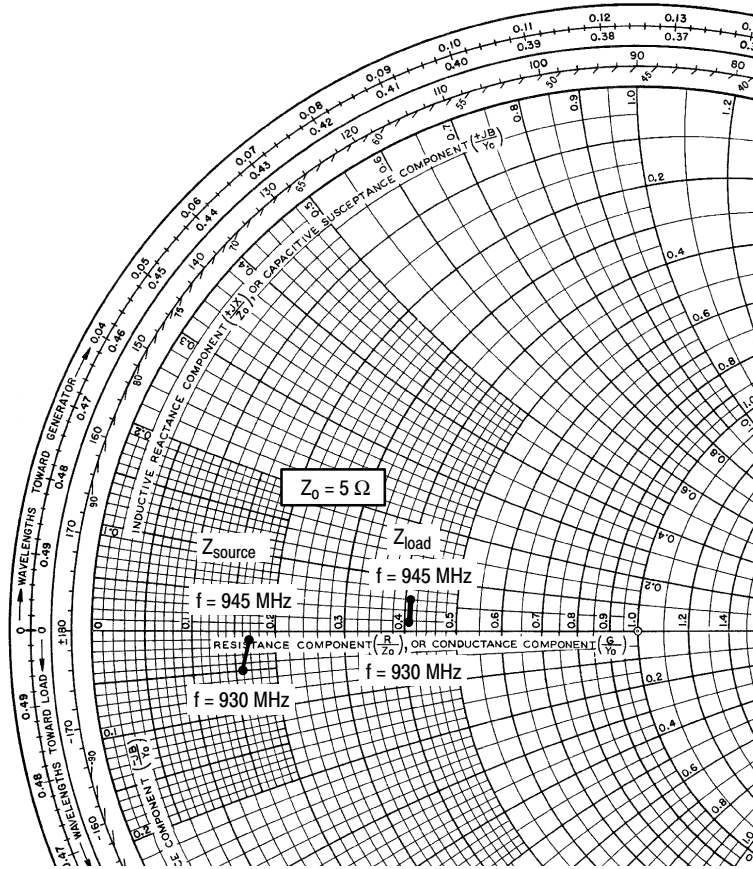


Figure 10. Output Voltage versus Supply Voltage



This above graph displays calculated MTTF in hours x ampere² drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by I_D² for MTTF in a particular application.

Figure 11. MTTF Factor versus Junction Temperature



$V_{DD} = 28\text{ V}$, $I_{DQ} = 350\text{ mA}$, $P_{out} = 45\text{ W (PEP)}$

f MHz	Z_{source} Ω	Z_{load} Ω
930	$0.81 - j0.25$	$2.03 + j0.09$
945	$0.85 - j0.05$	$2.03 + j0.28$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

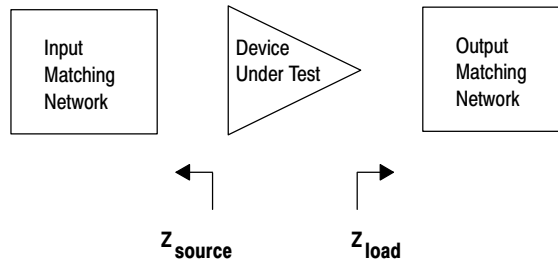
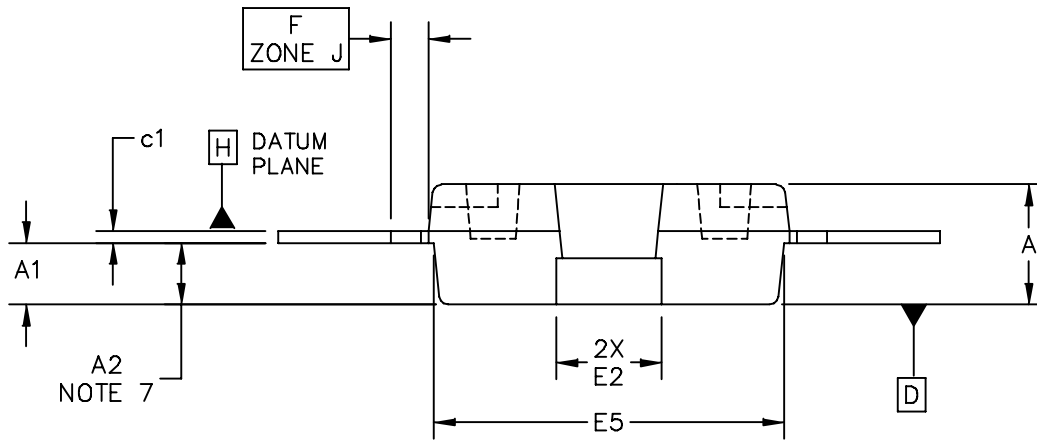
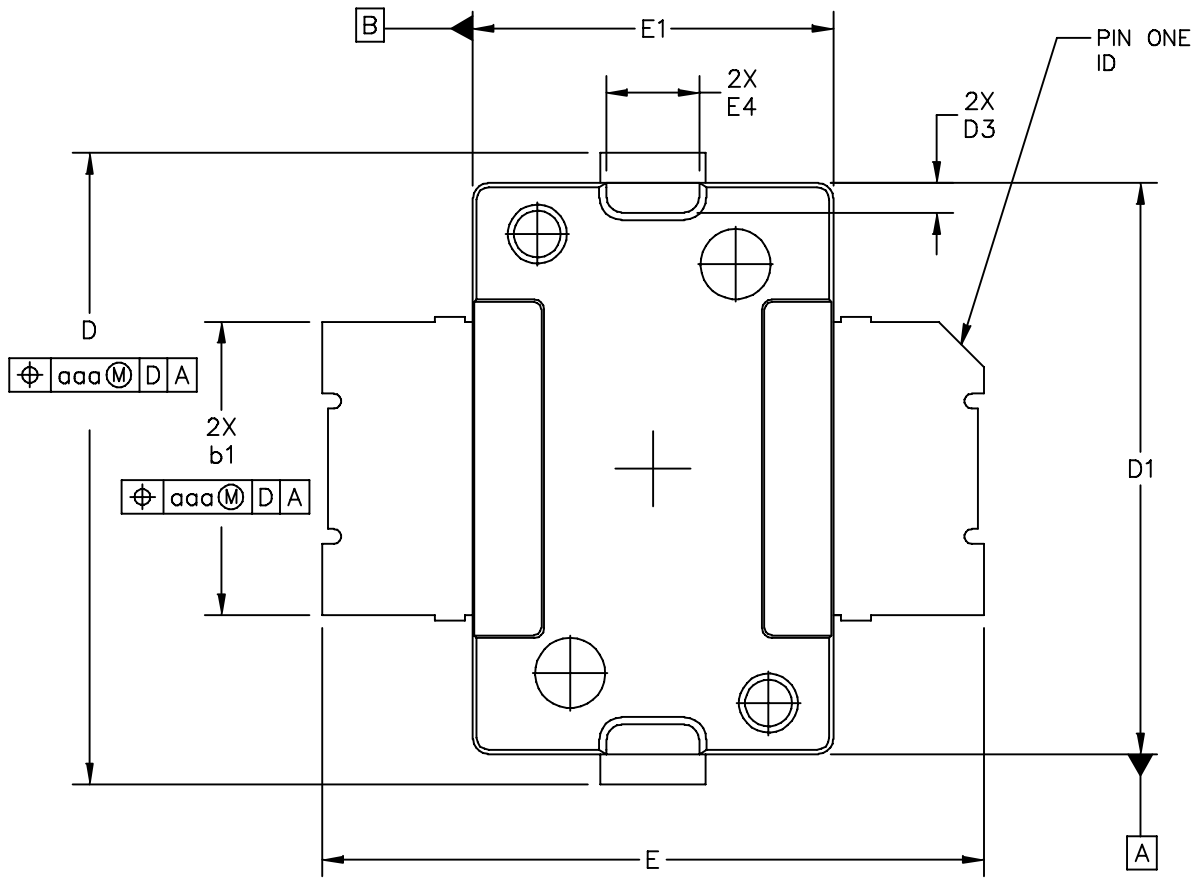


Figure 12. Series Equivalent Source and Load Impedance

NOT RECOMMENDED FOR NEW DESIGN

PACKAGE DIMENSIONS

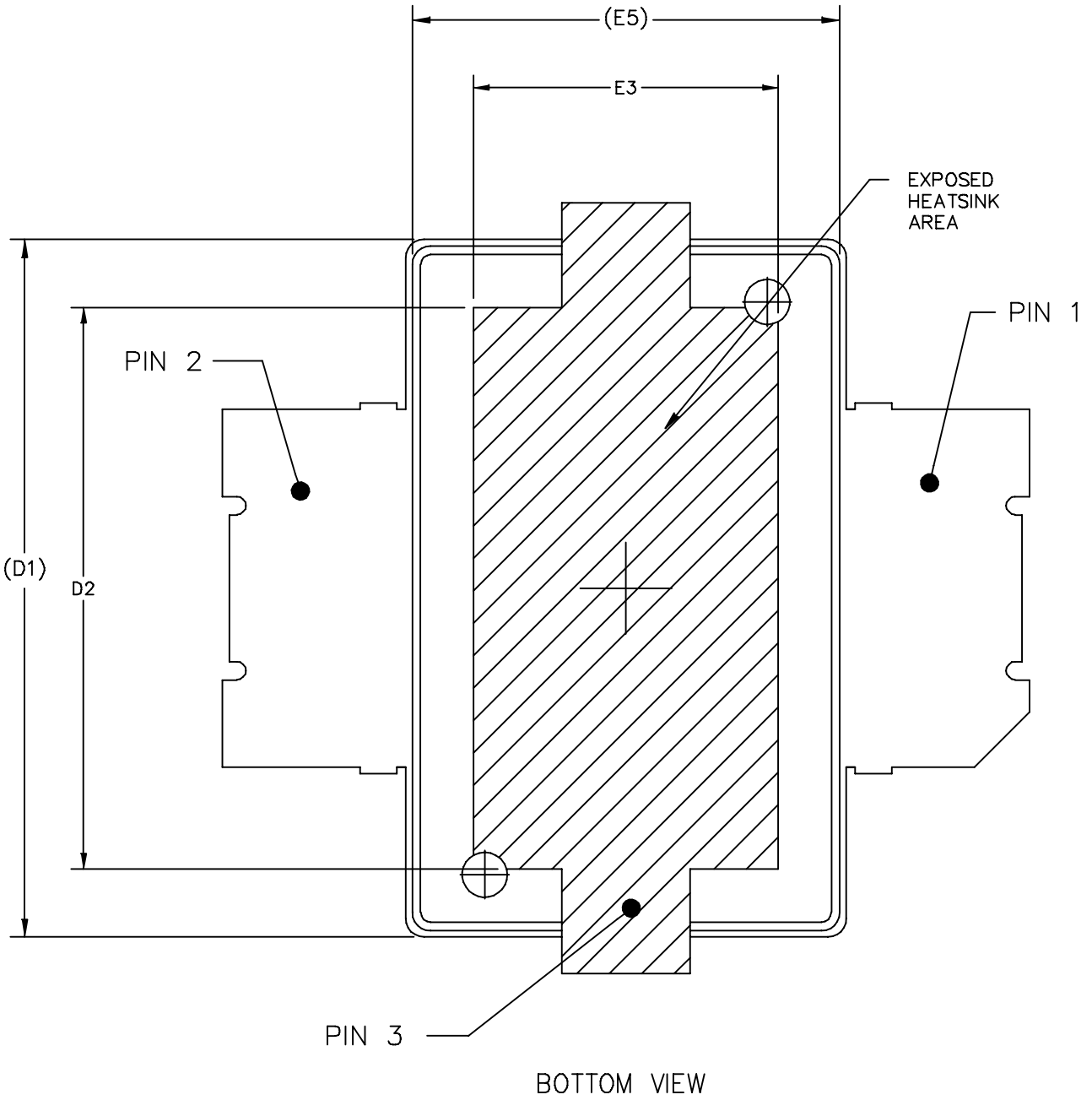


NOT RECOMMENDED FOR NEW DESIGN

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270 SURFACE MOUNT	DOCUMENT NO: 98ASH98117A	REV: K	
	CASE NUMBER: 1265-09	29 JUN 2007	
	STANDARD: JEDEC TO-270 AA		

NOT RECOMMENDED FOR NEW DESIGN

NOT RECOMMENDED FOR NEW DESIGN



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270 SURFACE MOUNT	DOCUMENT NO: 98ASH98117A	REV: K	
	CASE NUMBER: 1265-09	29 JUN 2007	
	STANDARD: JEDEC TO-270 AA		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D1" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION "A2" APPLIES WITHIN ZONE "J" ONLY.
8. DIMENSIONS "D" AND "E2" DO NOT INCLUDE MOLD PROTRUSION. OVERALL LENGTH INCLUDING MOLD PROTRUSION SHOULD NOT EXCEED 0.430 INCH FOR DIMENSION "D" AND 0.080 INCH FOR DIMENSION "E2". DIMENSIONS "D" AND "E2" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -D-.

STYLE 1:
 PIN 1 - DRAIN
 PIN 2 - GATE
 PIN 3 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.078	.082	1.98	2.08	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.193	.199	4.90	5.06
A2	.040	.042	1.02	1.07	c1	.007	.011	0.18	0.28
D	.416	.424	10.57	10.77	aaa	.004		0.10	
D1	.378	.382	9.60	9.70					
D2	.290	----	7.37	----					
D3	.016	.024	0.41	0.61					
E	.436	.444	11.07	11.28					
E1	.238	.242	6.04	6.15					
E2	.066	.074	1.68	1.88					
E3	.150	----	3.81	----					
E4	.058	.066	1.47	1.68					
E5	.231	.235	5.87	5.97					

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: TO-270 SURFACE MOUNT		DOCUMENT NO: 98ASH98117A		REV: K	
		CASE NUMBER: 1265-09		29 JUN 2007	
		STANDARD: JEDEC TO-270 AA			

NOT RECOMMENDED FOR NEW DESIGN

NOT RECOMMENDED FOR NEW DESIGN

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
12	Sept. 2008	<ul style="list-style-type: none">• Data sheet revised to reflect part status change, including use of applicable overlay.• Replaced Case Outline 1265-08 with 1265-09, Issue K, p. 1, 8-10. Corrected cross hatch pattern in bottom view and changed its dimensions (D2 and E3) to minimum value on source contact (D2 changed from Min-Max .290-.320 to .290 Min; E3 changed from Min-Max .150-.180 to .150 Min). Added JEDEC Standard Package Number.• Added Product Documentation and Revision History, p. 11

NOT RECOMMENDED FOR NEW DESIGN

NOT RECOMMENDED FOR NEW DESIGN

How to Reach Us:**Home Page:**

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2008. All rights reserved.

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.

