

# 2 Mbit / 4 Mbit (x8) Small-Sector Flash

GLS29SF020 / GLS29SF040

GLS29VF020 / GLS29VF040



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## FEATURES:

- **Organized as 256K x8 / 512K x8**
- **Single Voltage Read and Write Operations**
  - 4.5-5.5V for GLS29SF020/040
  - 2.7-3.6V for GLS29VF020/040
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 10 mA (typical)
  - Standby Current:
    - 30  $\mu$ A (typical) for GLS29SF020/040
    - 1  $\mu$ A (typical) for GLS29VF020/040
- **Sector-Erase Capability**
  - Uniform 128 Byte sectors
- **Fast Read Access Time:**
  - 55 ns for GLS29SF020/040
  - 70 ns for GLS29VF020/040
- **Latched Address and Data**
- **Fast Erase and Byte-Program:**
  - Sector-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 70 ms (typical)
  - Byte-Program Time: 14  $\mu$ s (typical)
  - Chip Rewrite Time:
    - 4 seconds (typical) for GLS29SF/VF020
    - 8 seconds (typical) for GLS29SF/VF040
- **Automatic Write Timing**
  - Internal  $V_{PP}$  Generation
- **End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **TTL I/O Compatibility for GLS29SF020/040**
- **CMOS I/O Compatibility for GLS29VF020/040**
- **JEDEC Standard**
  - Flash EEPROM Pinouts and command sets
- **Packages Available**
  - 32-lead PLCC
  - 32-lead TSOP (8mm x 14mm)
- **All non-Pb (lead-free) devices are RoHS compliant**

## PRODUCT DESCRIPTION

The GLS29SF020/040 and GLS29VF020/040 are 256K x8 / 512K x8 CMOS Small-Sector Flash (SSF) manufactured with high-performance SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The GLS29SF020/040 devices write (Program or Erase) with a 4.5-5.5V power supply. The GLS29VF020/040 devices write (Program or Erase) with a 2.7-3.6V power supply. These devices conform to JEDEC standard pin assignments for x8 memories.

Featuring high performance Byte-Program, the GLS29SF020/040 and GLS29VF020/040 devices provide a maximum Byte-Program time of 20  $\mu$ sec. To protect against inadvertent write, they have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed endurance of at least 10,000 cycles. Data retention is rated at greater than 100 years.

The GLS29SF020/040 and GLS29VF020/040 devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, they significantly improve performance and reliability, while lowering power consumption. They inherently use less energy during Erase and Program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. They also improve flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times independent of the number of Erase/Program cycles that have occurred. Therefore, the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

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To meet high density, surface mount requirements, the GLS29SF020/040 and GLS29VF020/040 devices are offered in 32-lead PLCC and 32-lead TSOP packages. The pin assignments are shown in Figures 2 and 3.

## Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

## Read

The Read operation of the GLS29SF020/040 and GLS29VF020/040 devices are controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram in Figure 4 for further details.

## Byte-Program Operation

The GLS29SF020/040 and GLS29VF020/040 devices are programmed on a byte-by-byte basis. Before programming, the sector where the byte exists must be fully erased. The Program operation is accomplished in three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed, within 20  $\mu$ s. See Figures 5 and 6 for WE# and CE# controlled Program operation timing diagrams and Figure 16 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

## Sector-Erase Operation

The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The GLS29SF020/040 and GLS29VF020/040 offer Sector-Erase mode. The sector architecture is based on uniform sector size of 128 Bytes. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (20H) and sector address (SA) in the last bus cycle. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (20H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit methods. For timing waveforms, see Figure 9. Any commands issued during the Sector-Erase operation are ignored.

## Chip-Erase Operation

The GLS29SF020/040 and GLS29VF020/040 devices provide a Chip-Erase operation, which allows the user to erase the entire memory array to the “1s” state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Chip-Erase command (10H) with address 555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 10 for the timing diagram, and Figure 19 for the flowchart. Any commands written during the Chip-Erase operation will be ignored.

## Write Operation Status Detection

The GLS29SF020/040 and GLS29VF020/040 devices provide two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ<sub>7</sub>) and Toggle Bit (DQ<sub>6</sub>). The End-of-Write detection mode is enabled after the rising edge of WE# which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ<sub>7</sub> or DQ<sub>6</sub>. In order to pre-

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vent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

## Data# Polling (DQ<sub>7</sub>)

When the GLS29SF020/040 and GLS29VF020/040 devices are in the internal Program operation, any attempt to read DQ<sub>7</sub> will produce the complement of the true data. Once the Program operation is completed, DQ<sub>7</sub> will produce true data. Note that even though DQ<sub>7</sub> may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1  $\mu$ s. During internal Erase operation, any attempt to read DQ<sub>7</sub> will produce a '0'. Once the internal Erase operation is completed, DQ<sub>7</sub> will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7 for Data# Polling timing diagram and Figure 17 for a flow-chart.

## Toggle Bit (DQ<sub>6</sub>)

During the internal Program or Erase operation, any consecutive attempts to read DQ<sub>6</sub> will produce alternating '0's and '1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 8 for Toggle Bit timing diagram and Figure 17 for a flowchart.

## Data Protection

The GLS29SF020/040 and GLS29VF020/040 devices provide both hardware and software features to protect nonvolatile data from inadvertent writes.

## Hardware Data Protection

**Noise/Glitch Protection:** A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

**V<sub>DD</sub> Power Up/Down Detection:** The Write operation is inhibited when V<sub>DD</sub> is less than 2.5V for GLS29SF020/040. The Write operation is inhibited when V<sub>DD</sub> is less than 1.5V for GLS29VF020/040.

**Write Inhibit Mode:** Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

## Software Data Protection (SDP)

The GLS29SF020/040 and GLS29VF020/040 provide the JEDEC approved Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three- byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of a six-byte load sequence. These devices are shipped with the Software Data Protection permanently enabled. The specific software command codes are shown in Table 4. During SDP command sequence, invalid commands will abort the device to read mode, within T<sub>RC</sub>.

## Product Identification

The Product Identification mode identifies the devices as GLS29SF020, GLS29SF040 and GLS29VF020, GLS29VF040 and manufacturer as Greenliant. This mode may be accessed by software operations. Users may use the Software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Table 4 for

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software operation, Figure 11 for the Software ID Entry and Read timing diagram, and Figure 18 for the Software ID Entry command sequence flowchart.

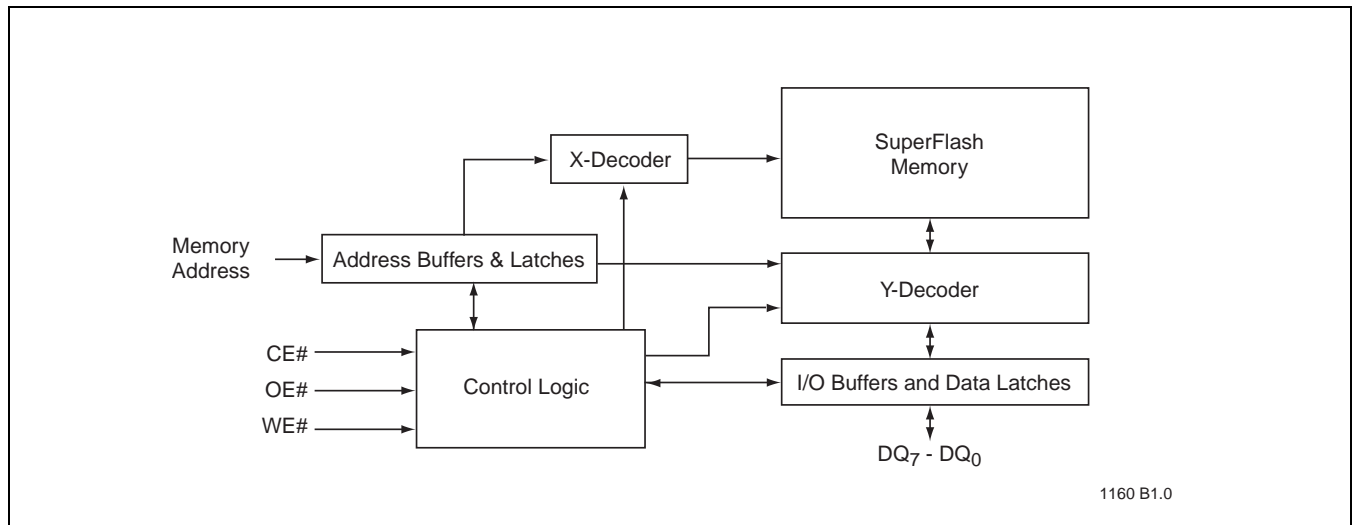
**TABLE 1: Product Identification**

|                   | Address | Data |
|-------------------|---------|------|
| Manufacturer's ID | 0000H   | BFH  |
| Device ID         |         |      |
| GLS29SF020        | 0001H   | 24H  |
| GLS29VF020        | 0001H   | 25H  |
| GLS29SF040        | 0001H   | 13H  |
| GLS29VF040        | 0001H   | 14H  |

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## Product Identification Mode Exit/Reset

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read operation. Please note that the Software ID Exit command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 12 for timing waveform, and Figure 18 for a flowchart.



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**FIGURE 1: Functional Block Diagram**

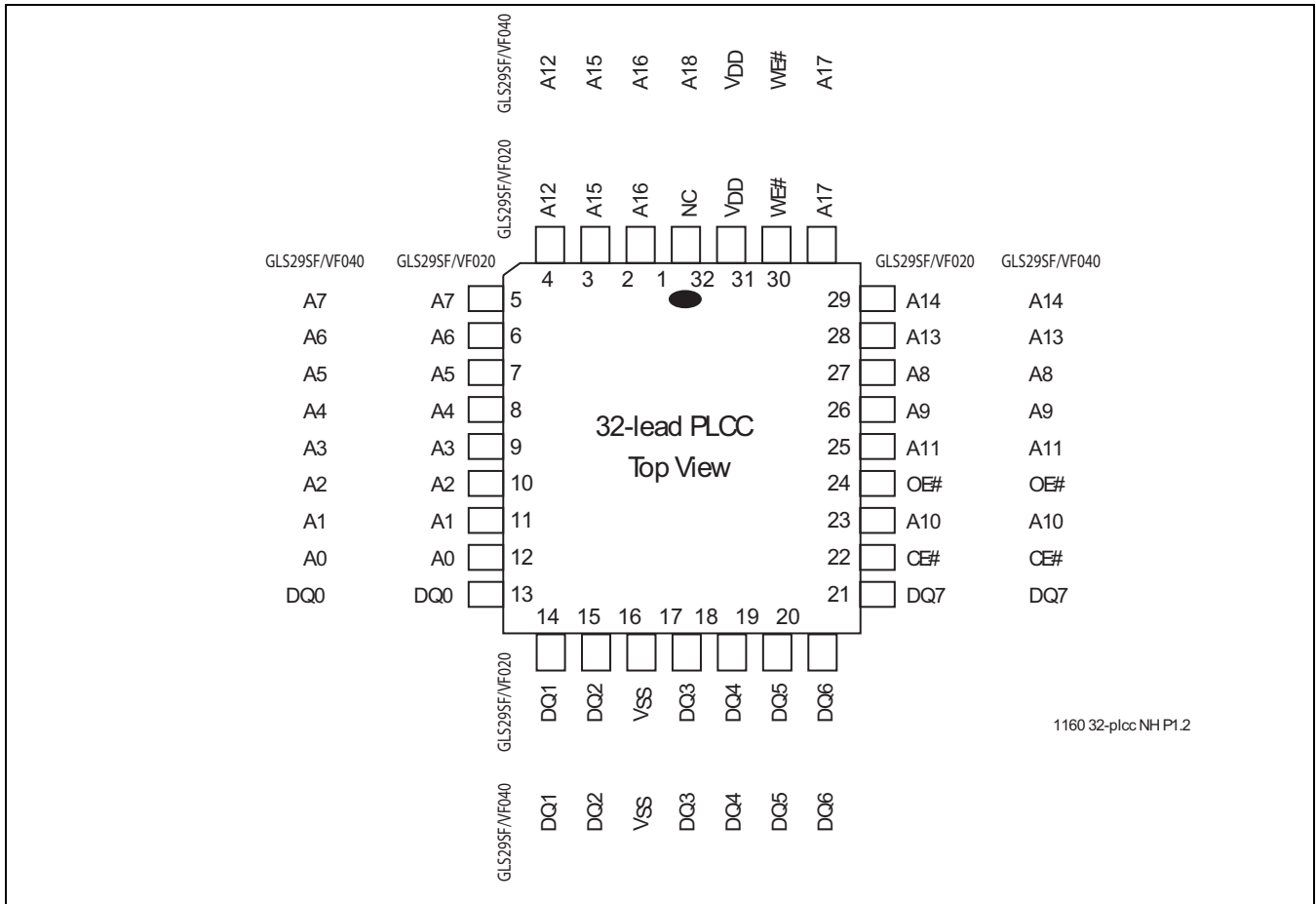
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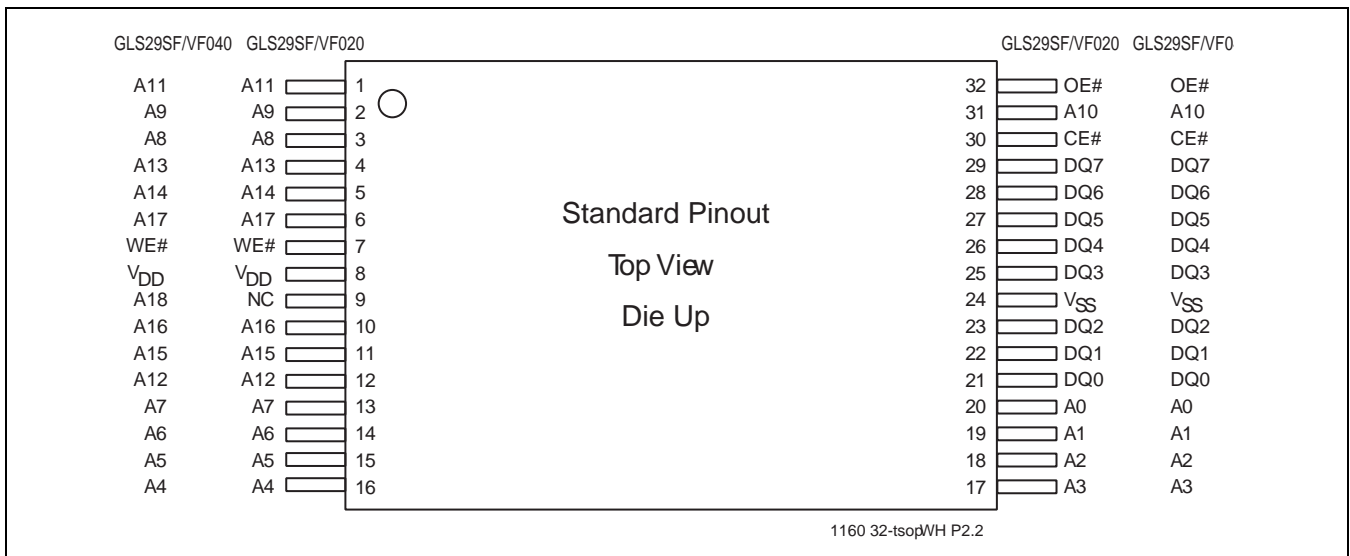
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**FIGURE 2: Pin Assignments for 32-lead PLCC**



**FIGURE 3: Pin Assignments for 32-lead TSOP (8mm x 14mm)**

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**TABLE 2: Pin Description**

| Symbol                           | Pin Name          | Functions  |
|----------------------------------|-------------------|--|
| $A_{MS}^1-A_0$                   | Address Inputs    | To provide memory addresses. During Sector-Erase $A_{MS}-A_8$ address lines will select the sector.  |
| DQ <sub>7</sub> -DQ <sub>0</sub> | Data Input/output | To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high. |
| CE#                              | Chip Enable       | To activate the device when CE# is low.  |
| OE#                              | Output Enable     | To gate the data output buffers.   |
| WE#                              | Write Enable      | To control the Write operations.   |
| V <sub>DD</sub>                  | Power Supply      | To provide power supply voltage: 4.5-5.5V for GLS29SF020/040<br>2.7-3.6V for GLS29VF020/040  |
| V <sub>SS</sub>                  | Ground            |  |
| NC                               | No Connection     | Pin not connected internally   |

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1.  $A_{MS}$  = Most significant address  
 $A_{MS}$  = A<sub>17</sub> for GLS29SF/VF020 and A<sub>18</sub> for GLS29SF/VF040

**TABLE 3: Operation Modes Selection**

| Mode                   | CE#             | OE#             | WE#             | DQ                       | Address                               |
|------------------------|-----------------|-----------------|-----------------|--------------------------|---------------------------------------|
| Read                   | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | D <sub>OUT</sub>         | A <sub>IN</sub>                       |
| Program                | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | D <sub>IN</sub>          | A <sub>IN</sub>                       |
| Erase                  | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | X <sup>1</sup>           | Sector address,<br>XXH for Chip-Erase |
| Standby                | V <sub>IH</sub> | X               | X               | High Z                   | X                                     |
| Write Inhibit          | X               | V <sub>IL</sub> | X               | High Z/ D <sub>OUT</sub> | X                                     |
|                        | X               | X               | V <sub>IH</sub> | High Z/ D <sub>OUT</sub> | X                                     |
| Product Identification |                 |                 |                 |                          |                                       |
| Software Mode          | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> |                          | See Table 4                           |

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1. X can be V<sub>IL</sub> or V<sub>IH</sub>, but no other value.

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**TABLE 4: Software Command Sequence**

| Command Sequence                 | 1st Bus Write Cycle |      | 2nd Bus Write Cycle |      | 3rd Bus Write Cycle |      | 4th Bus Write Cycle |      | 5th Bus Write Cycle |      | 6th Bus Write Cycle          |      |
|----------------------------------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|------------------------------|------|
|                                  | Addr <sup>1</sup>   | Data | Addr <sup>1</sup>   | Data | Addr <sup>1</sup>   | Data | Addr <sup>1</sup>   | Data | Addr <sup>1</sup>   | Data | Addr <sup>1</sup>            | Data |
| Byte-Program                     | 555H                | AAH  | 2AAH                | 55H  | 555H                | A0H  | BA <sup>2</sup>     | Data |                     |      |                              |      |
| Sector-Erase                     | 555H                | AAH  | 2AAH                | 55H  | 555H                | 80H  | 555H                | AAH  | 2AAH                | 55H  | SA <sub>X</sub> <sup>3</sup> | 20H  |
| Chip-Erase                       | 555H                | AAH  | 2AAH                | 55H  | 555H                | 80H  | 555H                | AAH  | 2AAH                | 55H  | 555H                         | 10H  |
| Software ID Entry <sup>4,5</sup> | 555H                | AAH  | 2AAH                | 55H  | 555H                | 90H  |                     |      |                     |      |                              |      |
| Software ID Exit <sup>6</sup>    | XXH                 | F0H  |                     |      |                     |      |                     |      |                     |      |                              |      |
| Software ID Exit <sup>6</sup>    | 555H                | AAH  | 2AAH                | 55H  | 555H                | F0H  |                     |      |                     |      |                              |      |

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- Address format A<sub>14</sub>-A<sub>0</sub> (Hex).  
Addresses A<sub>15</sub>-A<sub>MS</sub> can be V<sub>IL</sub> or V<sub>IH</sub>, but no other value, for the Command sequence for GLS29SF/VF020/040.  
A<sub>MS</sub> = Most significant address  
A<sub>MS</sub> = A<sub>17</sub> for GLS29SF/VF020 and A<sub>18</sub> for GLS29SF/VF040.
- BA = Program Byte address
- SA<sub>X</sub> for Sector-Erase; uses A<sub>MS</sub>-A<sub>7</sub> address lines for GLS29SF/VF020/040
- The device does not remain in Software Product ID mode if powered down.
- With A<sub>MS</sub>-A<sub>1</sub> = 0; Greenliant Manufacturer's ID = BFH, is read with A<sub>0</sub> = 0,  
GLS29SF020 Device ID = 24H, is read with A<sub>0</sub> = 1  
GLS29VF020 Device ID = 25H, is read with A<sub>0</sub> = 1  
GLS29SF040 Device ID = 13H, is read with A<sub>0</sub> = 1  
GLS29VF040 Device ID = 14H, is read with A<sub>0</sub> = 1
- Both Software ID Exit operations are equivalent

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**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

|  |                                |
|--|--------------------------------|
| Temperature Under Bias                                       | -55°C to +125°C                |
| Storage Temperature  | -65°C to +150°C                |
| D. C. Voltage on Any Pin to Ground Potential                 | -0.5V to V <sub>DD</sub> +0.5V |
| Transient Voltage (<20 ns) on Any Pin to Ground Potential    | -2.0V to V <sub>DD</sub> +2.0V |
| Voltage on A <sub>9</sub> Pin to Ground Potential            | -0.5V to 13.2V                 |
| Package Power Dissipation Capability (T <sub>A</sub> = 25°C) | 1.0W                           |
| Through Hole Lead Soldering Temperature (10 Seconds)         | 300°C                          |
| Surface Mount Solder Reflow Temperature <sup>1</sup>         | 260°C for 10 seconds           |
| Output Short Circuit Current <sup>2</sup>                    | 50 mA                          |

1. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

#### Operating Range for GLS29SF020/040

| Range      | Ambient Temp   | V <sub>DD</sub> |
|------------|----------------|-----------------|
| Commercial | 0°C to +70°C   | 4.5-5.5V        |
| Industrial | -40°C to +85°C | 4.5-5.5V        |

#### Operating Range for GLS29VF020/040

| Range      | Ambient Temp   | V <sub>DD</sub> |
|------------|----------------|-----------------|
| Commercial | 0°C to +70°C   | 2.7-3.6V        |
| Industrial | -40°C to +85°C | 2.7-3.6V        |

#### AC Conditions of Test

|                            |                                   |
|----------------------------|-----------------------------------|
| Input Rise/Fall Time       | 5 ns                              |
| Output Load                | C <sub>L</sub> = 30 pF for 55 ns  |
| Output Load                | C <sub>L</sub> = 100 pF for 70 ns |
| See Figures 13, 14, and 15 |                                   |

**TABLE 5: DC Operating Characteristics V<sub>DD</sub> = 4.5-5.5V for GLS29SF020/040**

| Symbol           | Parameter                                    | Limits               |     |       | Test Conditions   |
|------------------|--|----------------------|-----|-------|---|
|                  |  | Min                  | Max | Units |   |
| I <sub>DD</sub>  | Power Supply Current                         |                      |     |       | Address input=V <sub>IL</sub> /V <sub>IH</sub> , at f=1/T <sub>RC</sub> Min<br>V <sub>DD</sub> =V <sub>DD</sub> Max |
|                  | Read   |                      | 25  | mA    | CE#=OE#=V <sub>IL</sub> , WE#=V <sub>IH</sub> , all I/Os open   |
|                  | Write  |                      | 30  | mA    | CE#=WE#=V <sub>IL</sub> , OE#=V <sub>IH</sub>   |
| I <sub>SB1</sub> | Standby V <sub>DD</sub> Current (TTL input)  |                      | 3   | mA    | CE#=V <sub>IH</sub> , V <sub>DD</sub> =V <sub>DD</sub> Max  |
| I <sub>SB2</sub> | Standby V <sub>DD</sub> Current (CMOS input) |                      | 100 | µA    | CE#=V <sub>IHC</sub> , V <sub>DD</sub> =V <sub>DD</sub> Max   |
| I <sub>LI</sub>  | Input Leakage Current                        |                      | 1   | µA    | V <sub>IN</sub> =GND to V <sub>DD</sub> , V <sub>DD</sub> =V <sub>DD</sub> Max                                      |
| I <sub>LO</sub>  | Output Leakage Current                       |                      | 10  | µA    | V <sub>OUT</sub> =GND to V <sub>DD</sub> , V <sub>DD</sub> =V <sub>DD</sub> Max                                     |
| V <sub>IL</sub>  | Input Low Voltage                            |                      | 0.8 | V     | V <sub>DD</sub> =V <sub>DD</sub> Min  |
| V <sub>IH</sub>  | Input High Voltage                           | 2.0                  |     | V     | V <sub>DD</sub> =V <sub>DD</sub> Max  |
| V <sub>IHC</sub> | Input High Voltage (CMOS)                    | V <sub>DD</sub> -0.3 |     | V     | V <sub>DD</sub> =V <sub>DD</sub> Max  |
| V <sub>OL</sub>  | Output Low Voltage                           |                      | 0.4 | V     | I <sub>OL</sub> =2.1 µA, V <sub>DD</sub> =V <sub>DD</sub> Min   |
| V <sub>OH</sub>  | Output High Voltage                          | 2.4                  |     | V     | I <sub>OH</sub> =-400 µA, V <sub>DD</sub> =V <sub>DD</sub> Min  |

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**TABLE 6: DC Operating Characteristics  $V_{DD} = 2.7-3.6V$  for GLS29VF020/040**

| Symbol    | Parameter                 | Limits       |     |         | Test Conditions   |
|-----------|---------------------------|--------------|-----|---------|---|
|           |                           | Min          | Max | Units   |   |
| $I_{DD}$  | Power Supply Current      |              |     |         | Address input= $V_{IL}/V_{IH}$ , at $f=1/T_{RC}$ Min<br>$V_{DD}=V_{DD}$ Max |
|           | Read                      |              | 25  | mA      | $CE\#=OE\#=V_{IL}$ , $WE\#=V_{IH}$ , all I/Os open                          |
|           | Write                     |              | 30  | mA      | $CE\#=WE\#=V_{IL}$ , $OE\#=V_{IH}$  |
| $I_{SB}$  | Standby $V_{DD}$ Current  |              | 30  | $\mu A$ | $CE\#=V_{IHC}$ , $V_{DD}=V_{DD}$ Max  |
| $I_{LI}$  | Input Leakage Current     |              | 1   | $\mu A$ | $V_{IN}=GND$ to $V_{DD}$ , $V_{DD}=V_{DD}$ Max                              |
| $I_{LO}$  | Output Leakage Current    |              | 10  | $\mu A$ | $V_{OUT}=GND$ to $V_{DD}$ , $V_{DD}=V_{DD}$ Max                             |
| $V_{IL}$  | Input Low Voltage         |              | 0.8 | V       | $V_{DD}=V_{DD}$ Min   |
| $V_{IH}$  | Input High Voltage        | $0.7V_{DD}$  |     | V       | $V_{DD}=V_{DD}$ Max   |
| $V_{IHC}$ | Input High Voltage (CMOS) | $V_{DD}-0.3$ |     | V       | $V_{DD}=V_{DD}$ Max   |
| $V_{OL}$  | Output Low Voltage        |              | 0.2 | V       | $I_{OL}=100 \mu A$ , $V_{DD}=V_{DD}$ Min                                    |
| $V_{OH}$  | Output High Voltage       | $V_{DD}-0.2$ |     | V       | $I_{OH}=-100 \mu A$ , $V_{DD}=V_{DD}$ Min                                   |

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**TABLE 7: Recommended System Power-up Timings**

| Symbol           | Parameter                           | Minimum | Units   |
|------------------|-------------------------------------|---------|---------|
| $T_{PU-READ}^1$  | Power-up to Read Operation          | 100     | $\mu s$ |
| $T_{PU-WRITE}^1$ | Power-up to Program/Erase Operation | 100     | $\mu s$ |

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 8: Capacitance ( $T_A = 25^\circ C$ ,  $f=1$  Mhz, other pins open)**

| Parameter   | Description         | Test Condition | Maximum |
|-------------|---------------------|----------------|---------|
| $C_{I/O}^1$ | I/O Pin Capacitance | $V_{I/O} = 0V$ | 12 pF   |
| $C_{IN}^1$  | Input Capacitance   | $V_{IN} = 0V$  | 6 pF    |

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 9: Reliability Characteristics**

| Symbol      | Parameter      | Minimum Specification | Units  | Test Method         |
|-------------|----------------|-----------------------|--------|---------------------|
| $N_{END}^1$ | Endurance      | 10,000                | Cycles | JEDEC Standard A117 |
| $T_{DR}^1$  | Data Retention | 100                   | Years  | JEDEC Standard A103 |
| $I_{LTH}^1$ | Latch Up       | $100 + I_{DD}$        | mA     | JEDEC Standard 78   |

T9.2 1160

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

# 2 Mbit / 4 Mbit Small-Sector Flash

GLS29SF020 / GLS29SF040

GLS29VF020 / GLS29VF040



Data Sheet

## AC CHARACTERISTICS

**TABLE 10: Read Cycle Timing Parameters**

$V_{DD} = 4.5-5.5V$  for GLS29SF020/040 and  $2.7-3.6V$  for GLS29VF020/040

| Symbol      | Parameter                       | GLS29SF020/040-55 |     | GLS29VF020/040-70 |     | Units |
|-------------|---------------------------------|-------------------|-----|-------------------|-----|-------|
|             |                                 | Min               | Max | Min               | Max |       |
| $T_{RC}$    | Read Cycle Time                 | 55                |     | 70                |     | ns    |
| $T_{CE}$    | Chip Enable Access Time         |                   | 55  |                   | 70  | ns    |
| $T_{AA}$    | Address Access Time             |                   | 55  |                   | 70  | ns    |
| $T_{OE}$    | Output Enable Access Time       |                   | 30  |                   | 35  | ns    |
| $T_{CLZ}^1$ | CE# Low to Active Output        | 0                 |     | 0                 |     | ns    |
| $T_{OLZ}^1$ | OE# Low to Active Output        | 0                 |     | 0                 |     | ns    |
| $T_{CHZ}^1$ | CE# High to High-Z Output       |                   | 20  |                   | 25  | ns    |
| $T_{OHZ}^1$ | OE# High to High-Z Output       |                   | 20  |                   | 25  | ns    |
| $T_{OH}^1$  | Output Hold from Address Change | 0                 |     | 0                 |     | ns    |

T10.10 1160

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

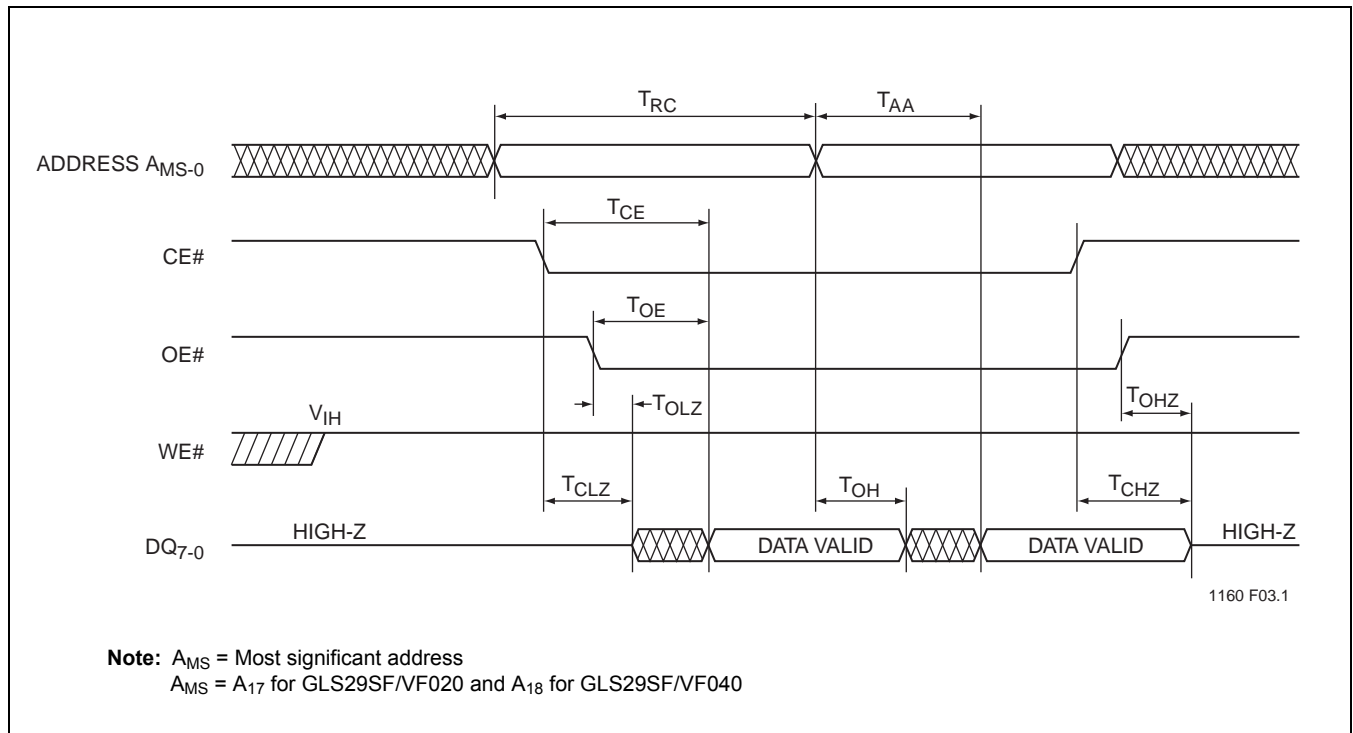
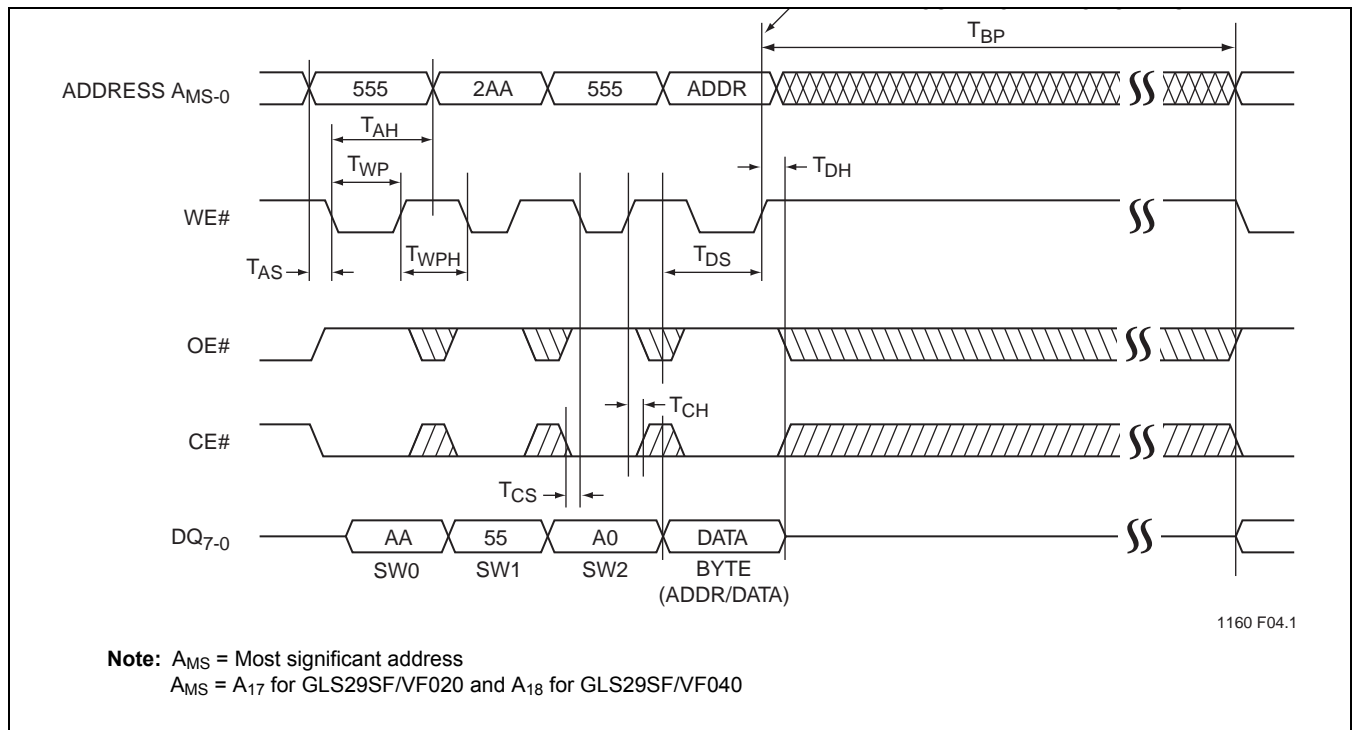
**TABLE 11: Program/Erase Cycle Timing Parameters**

$V_{DD} = 4.5-5.5V$  for GLS29SF020/040 and  $2.7-3.6V$  for GLS29VF020/040

| Symbol      | Parameter                        | Min | Max | Units   |
|-------------|----------------------------------|-----|-----|---------|
| $T_{BP}$    | Byte-Program Time                |     | 20  | $\mu s$ |
| $T_{AS}$    | Address Setup Time               | 0   |     | ns      |
| $T_{AH}$    | Address Hold Time                | 30  |     | ns      |
| $T_{CS}$    | WE# and CE# Setup Time           | 0   |     | ns      |
| $T_{CH}$    | WE# and CE# Hold Time            | 0   |     | ns      |
| $T_{OES}$   | OE# High Setup Time              | 0   |     | ns      |
| $T_{OEH}$   | OE# High Hold Time               | 10  |     | ns      |
| $T_{CP}$    | CE# Pulse Width                  | 40  |     | ns      |
| $T_{WP}$    | WE# Pulse Width                  | 40  |     | ns      |
| $T_{WPH}^1$ | WE# Pulse Width High             | 30  |     | ns      |
| $T_{CPH}^1$ | CE# Pulse Width High             | 30  |     | ns      |
| $T_{DS}$    | Data Setup Time                  | 40  |     | ns      |
| $T_{DH}^1$  | Data Hold Time                   | 0   |     | ns      |
| $T_{IDA}^1$ | Software ID Access and Exit Time |     | 150 | ns      |
| $T_{SE}$    | Sector-Erase                     |     | 25  | ms      |
| $T_{SCE}$   | Chip-Erase                       |     | 100 | ms      |

T11.9 1160

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**Data Sheet**

**FIGURE 4: Read Cycle Timing Diagram**

**FIGURE 5: WE# Controlled Program Cycle Timing Diagram**

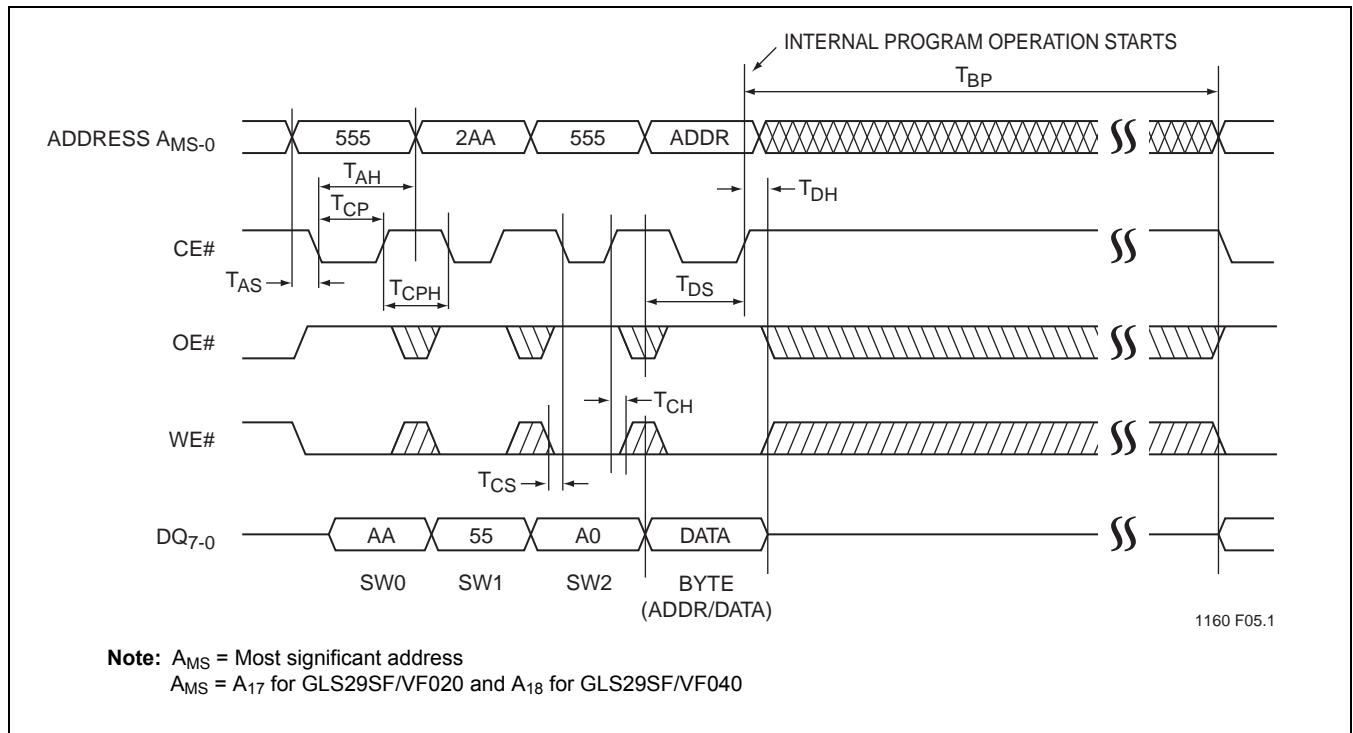
# 2 Mbit / 4 Mbit Small-Sector Flash

GLS29SF020 / GLS29SF040

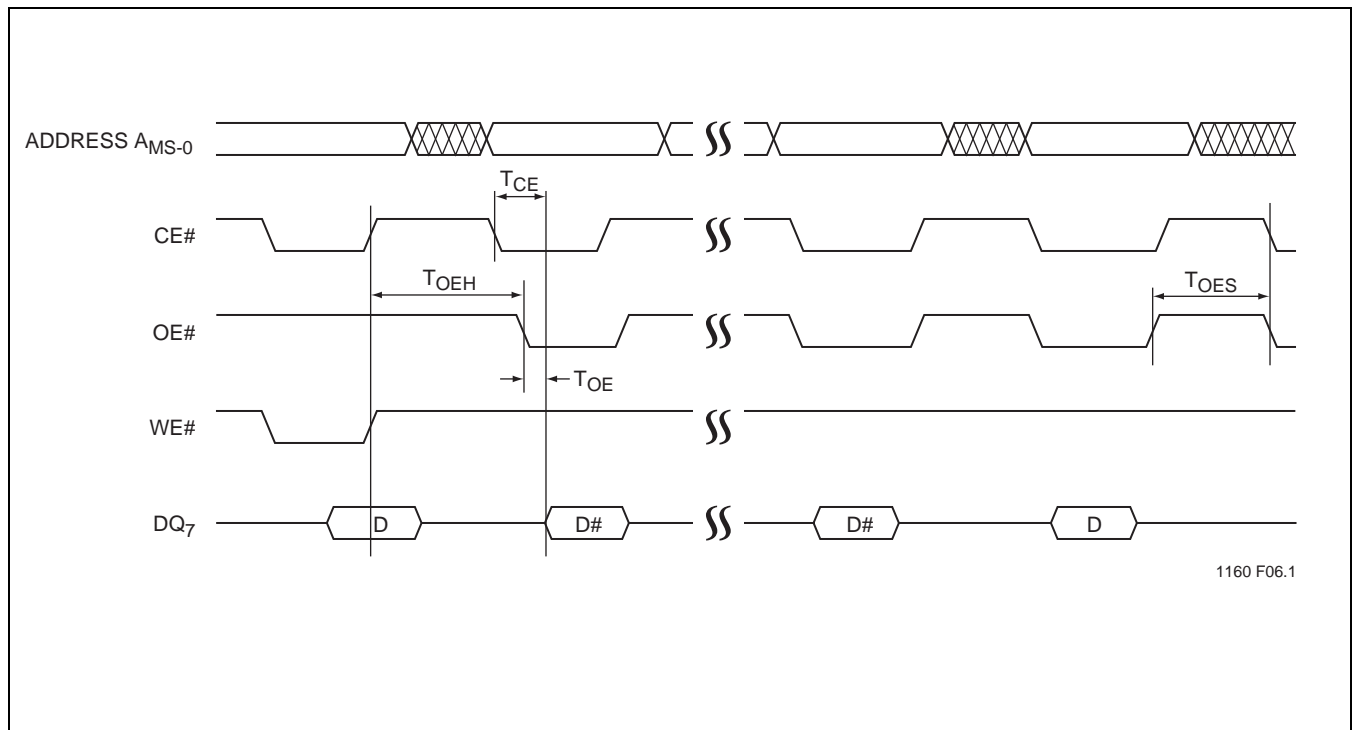
GLS29VF020 / GLS29VF040



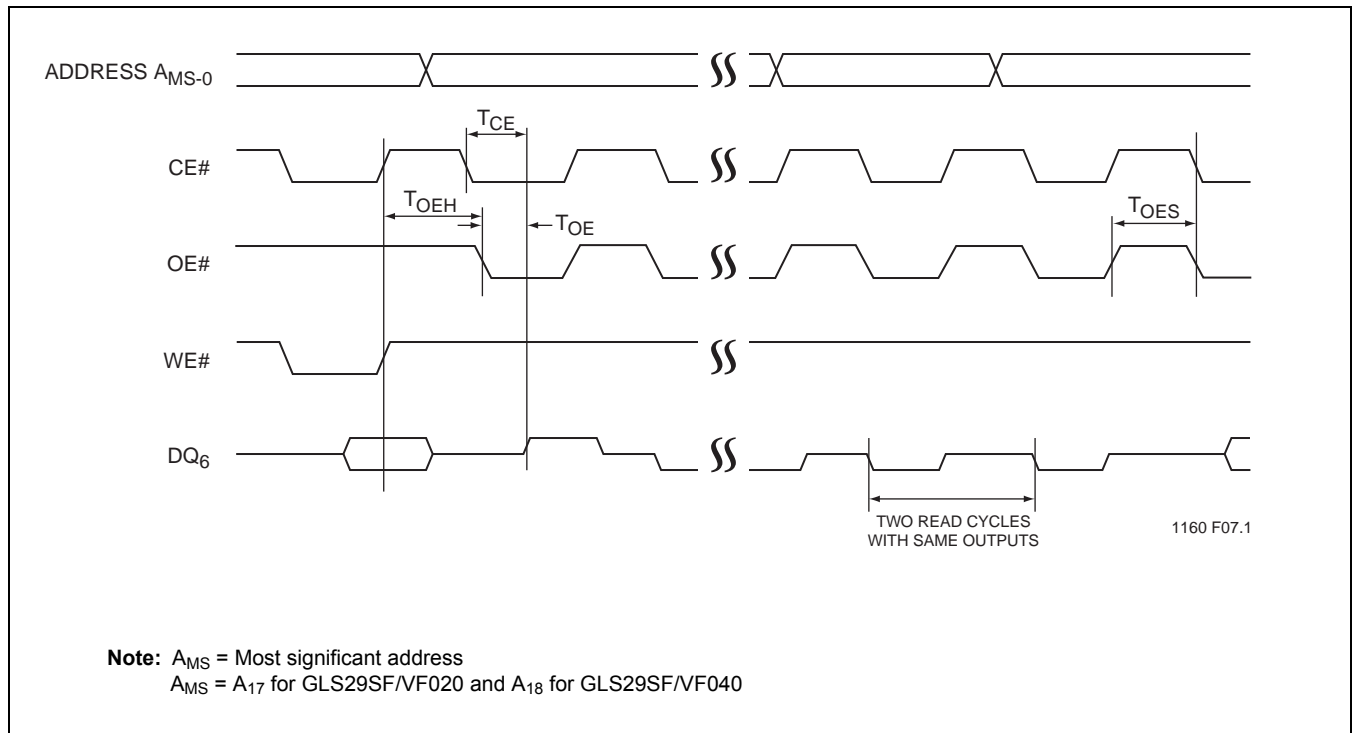
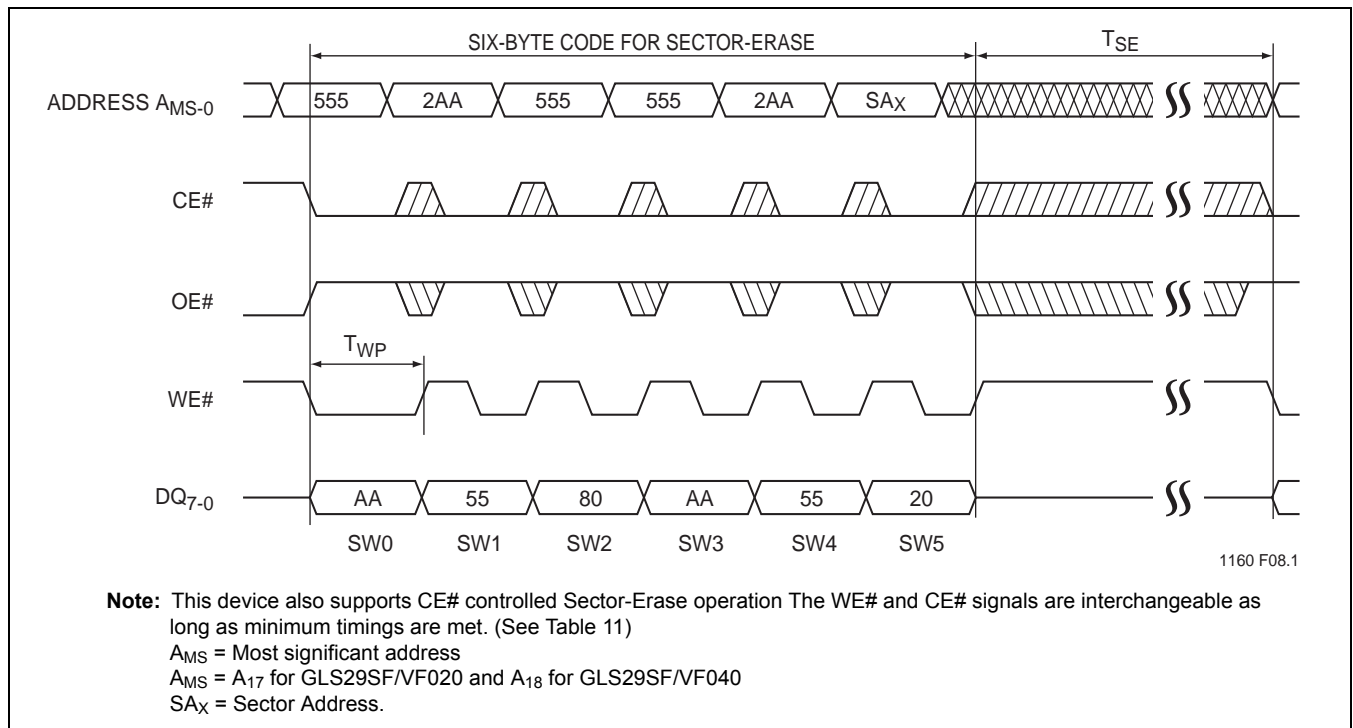
Data Sheet



**FIGURE 6: CE# Controlled Program Cycle Timing Diagram**



**FIGURE 7: Data# Polling Timing Diagram**

**Data Sheet**

**FIGURE 8: Toggle Bit Timing Diagram**

**FIGURE 9: WE# Controlled Sector-Erase Timing Diagram**

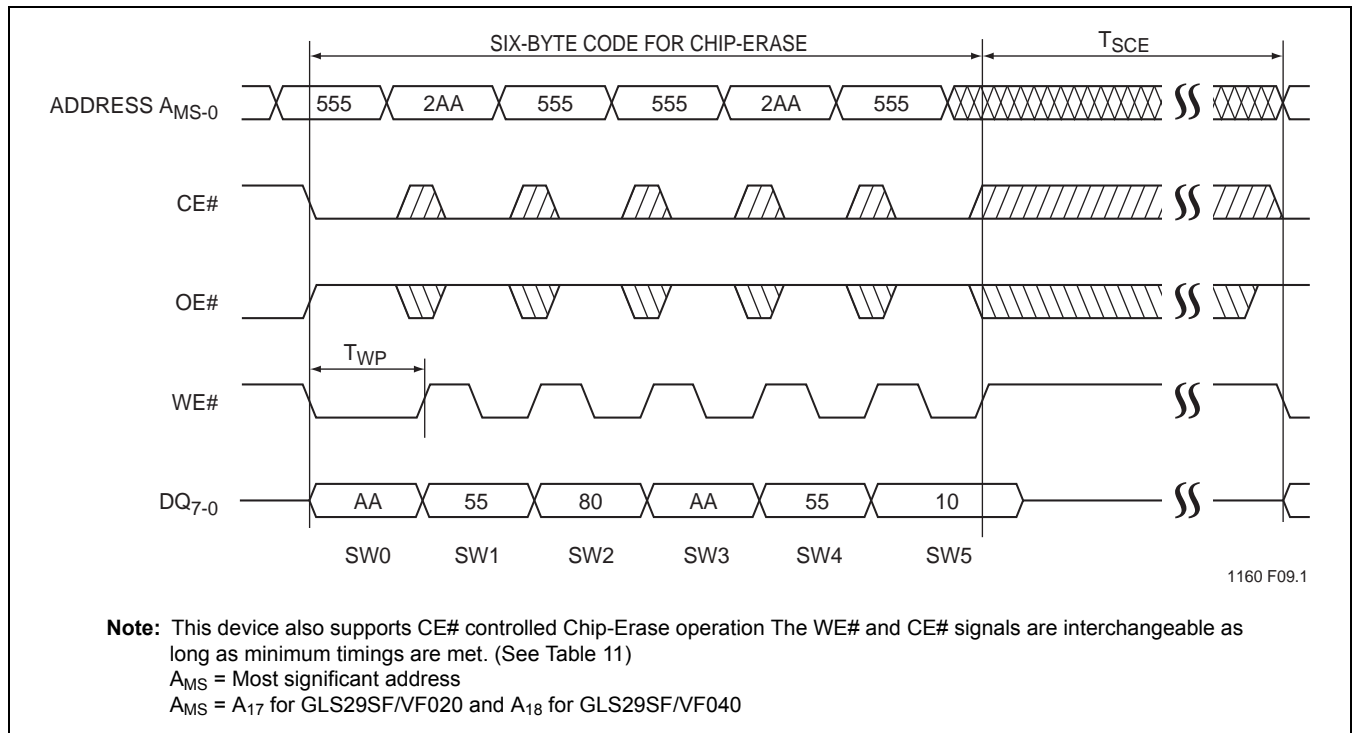
# 2 Mbit / 4 Mbit Small-Sector Flash

GLS29SF020 / GLS29SF040

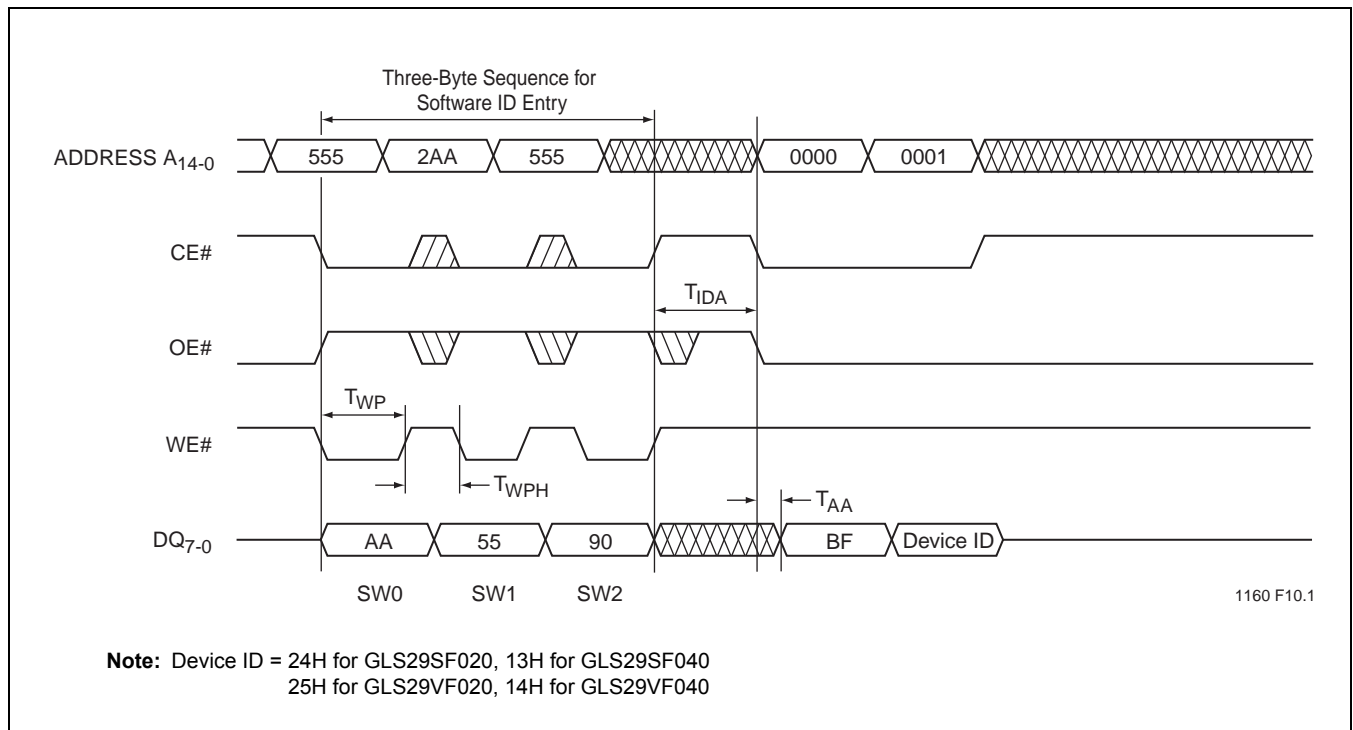
GLS29VF020 / GLS29VF040



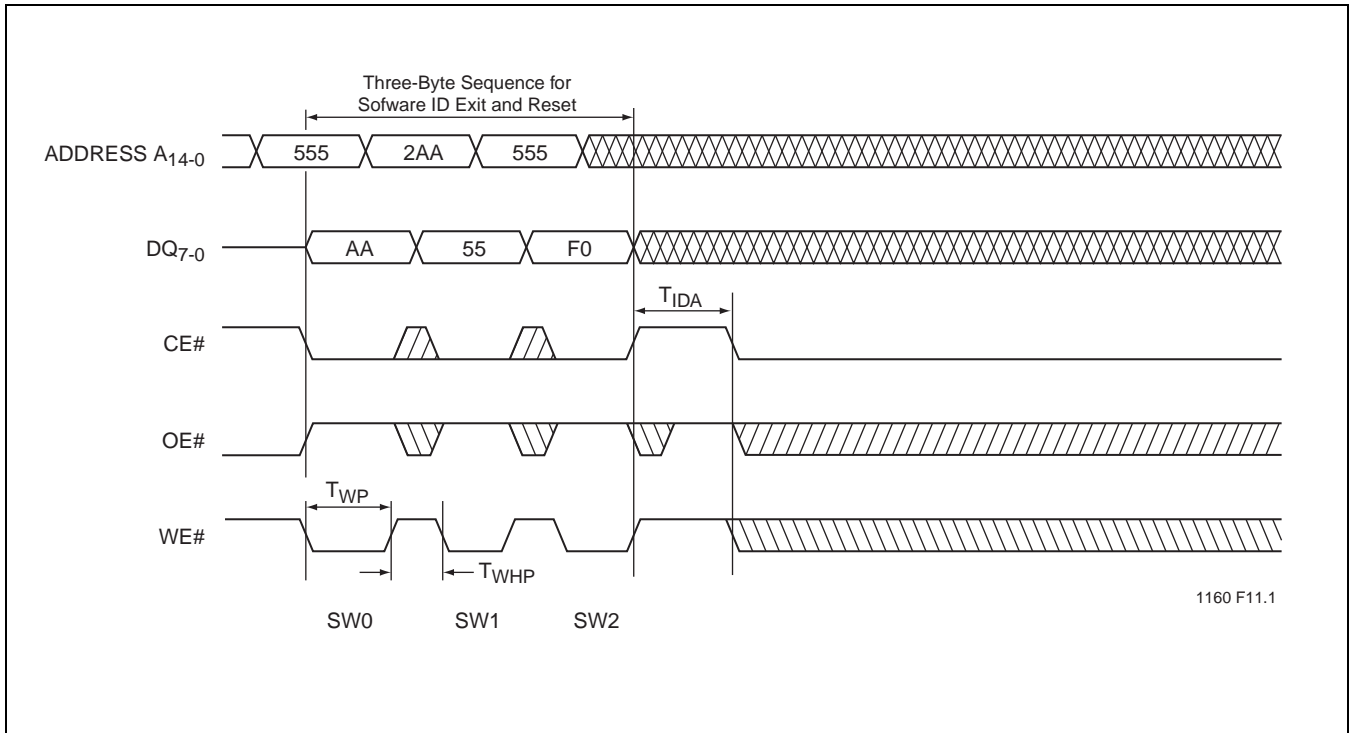
Data Sheet



**FIGURE 10: WE# Controlled Chip-Erase Timing Diagram**



**FIGURE 11: Software ID Entry and Read**

**Data Sheet**

**FIGURE 12: Software ID Exit and Reset**



# 2 Mbit / 4 Mbit Small-Sector Flash

GLS29SF020 / GLS29SF040

GLS29VF020 / GLS29VF040



Data Sheet

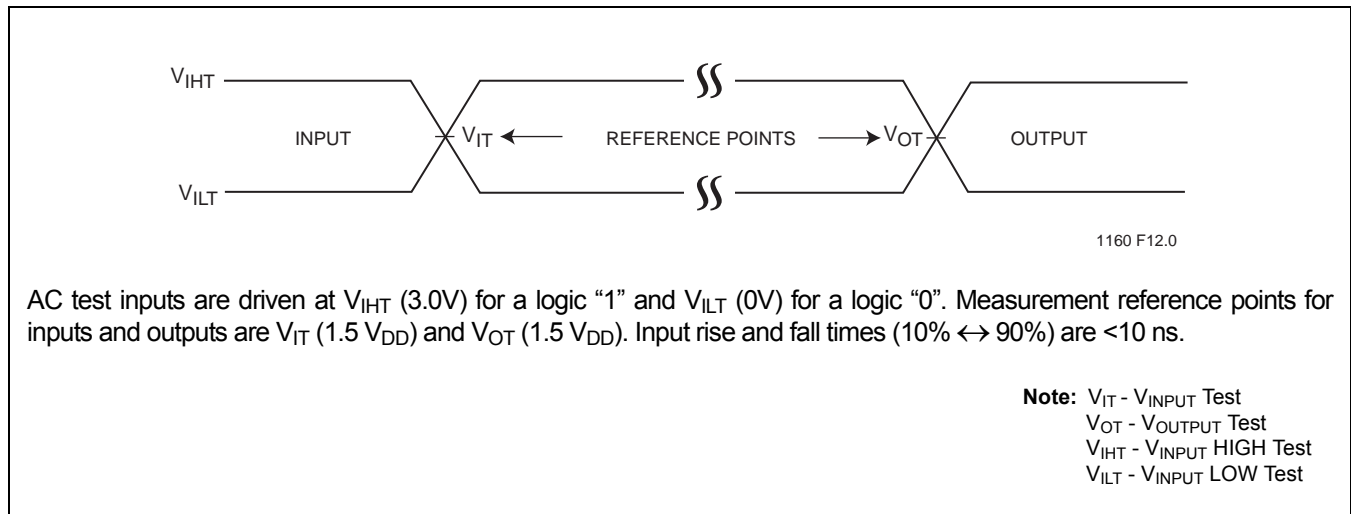


FIGURE 13: AC Input/Output Reference Waveforms for GLS29SF020/040

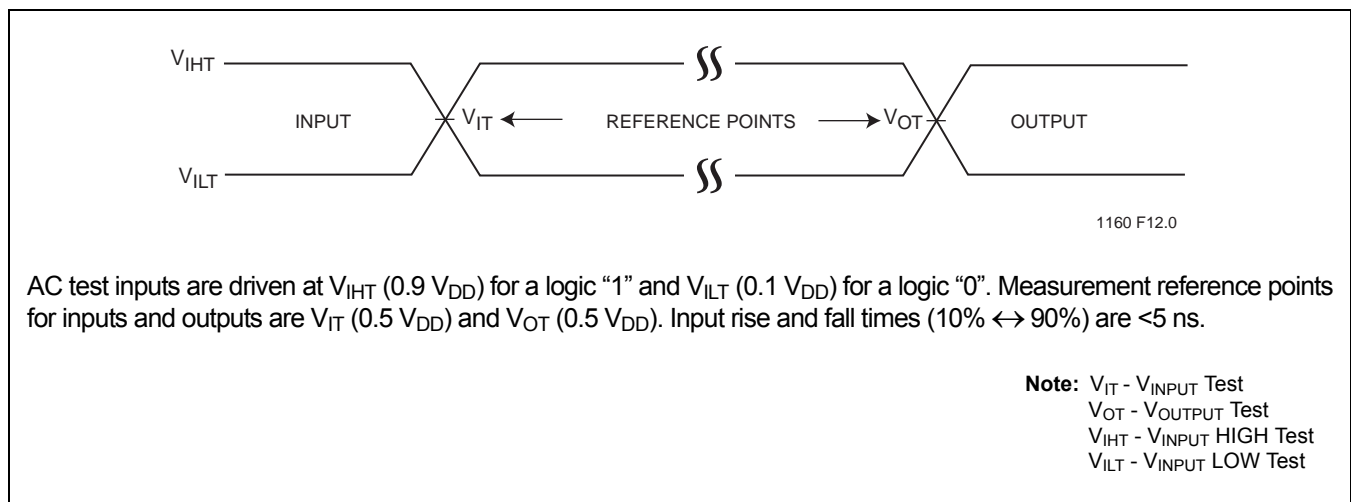
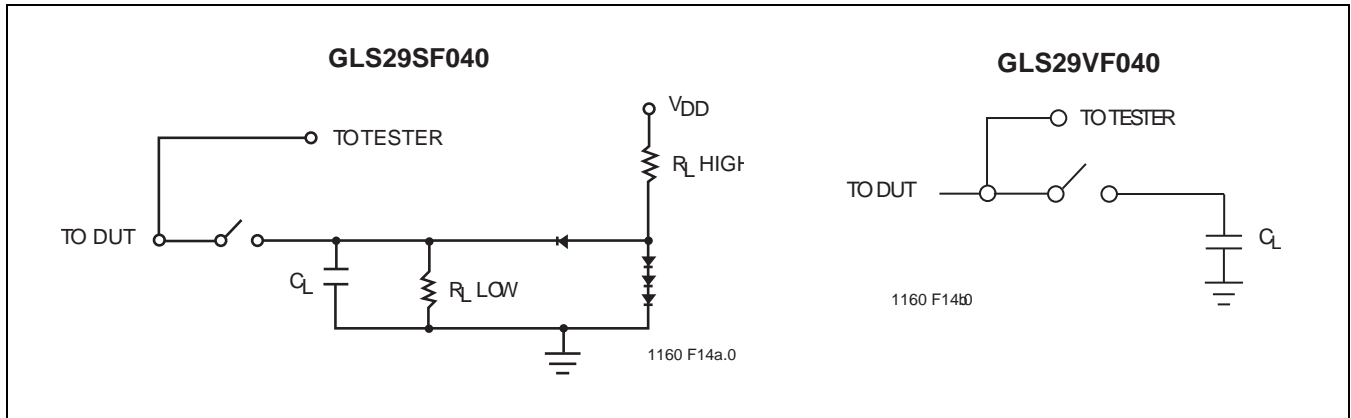


FIGURE 14: AC Input/Output Reference Waveforms for GLS29VF020/040

Data Sheet



**FIGURE 15: Test Load Examples**

# 2 Mbit / 4 Mbit Small-Sector Flash

GLS29SF020 / GLS29SF040

GLS29VF020 / GLS29VF040



Data Sheet

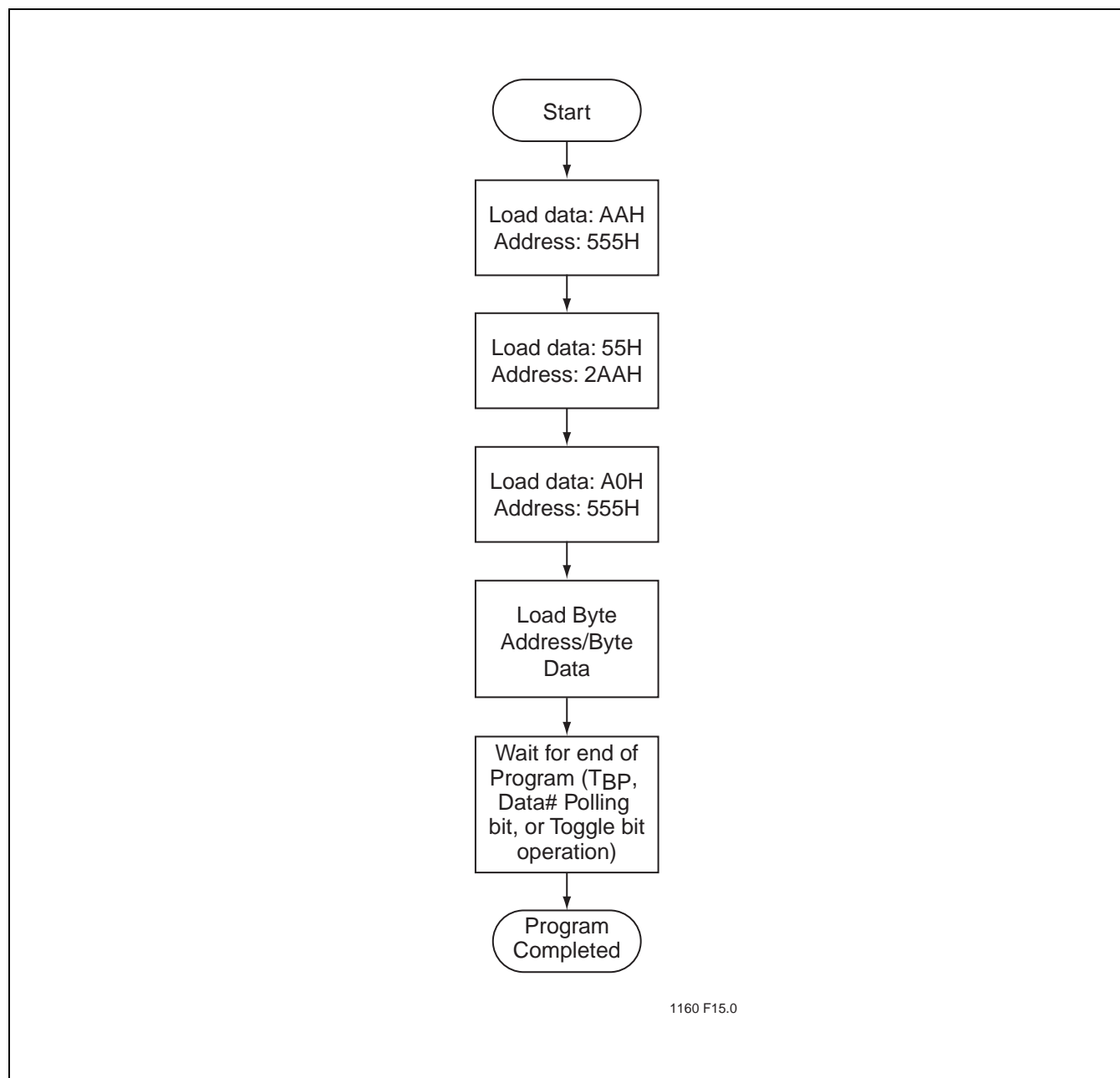
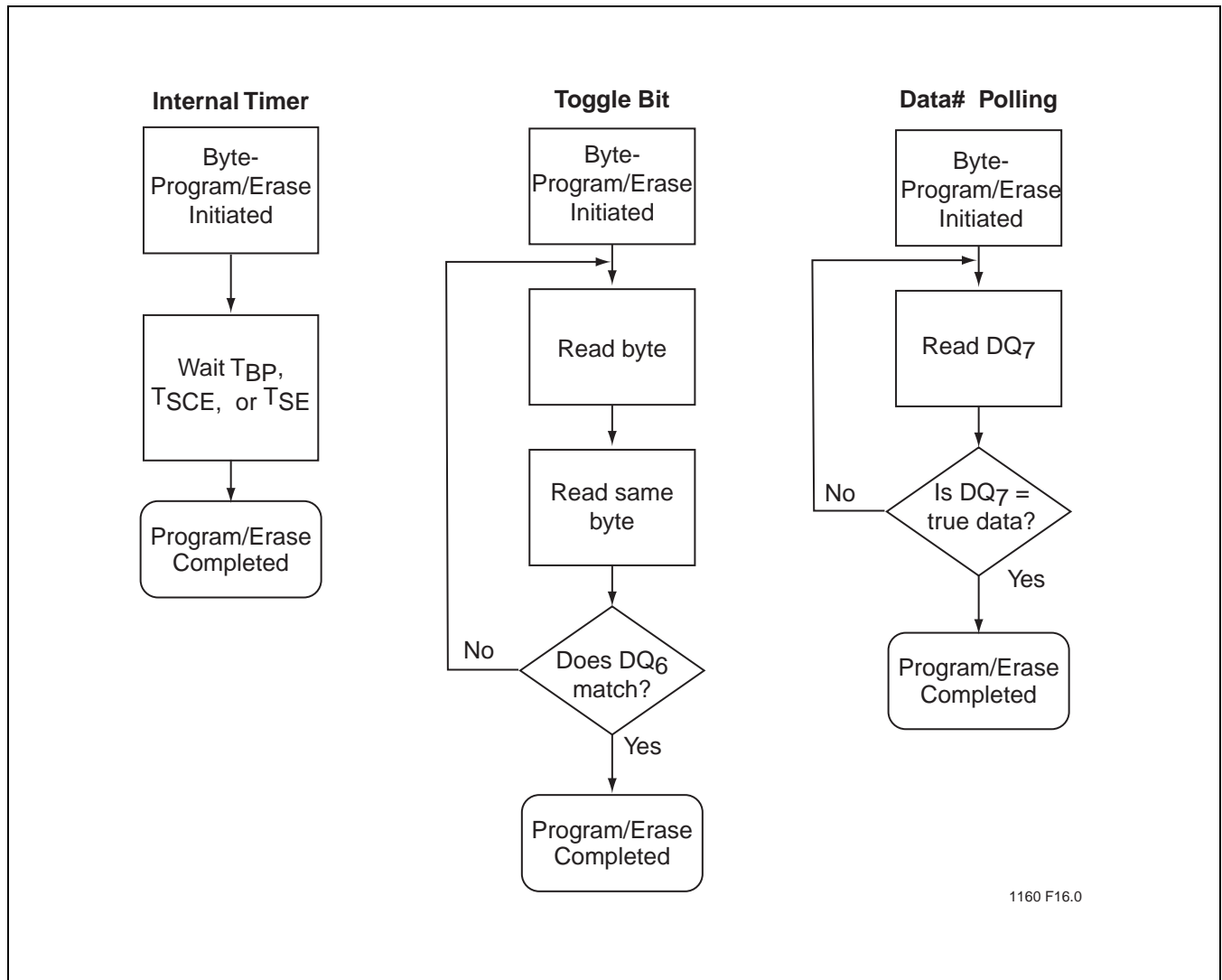


FIGURE 16: Byte-Program Algorithm

## Data Sheet


**FIGURE 17: Wait Options**

# 2 Mbit / 4 Mbit Small-Sector Flash

GLS29SF020 / GLS29SF040

GLS29VF020 / GLS29VF040



Data Sheet

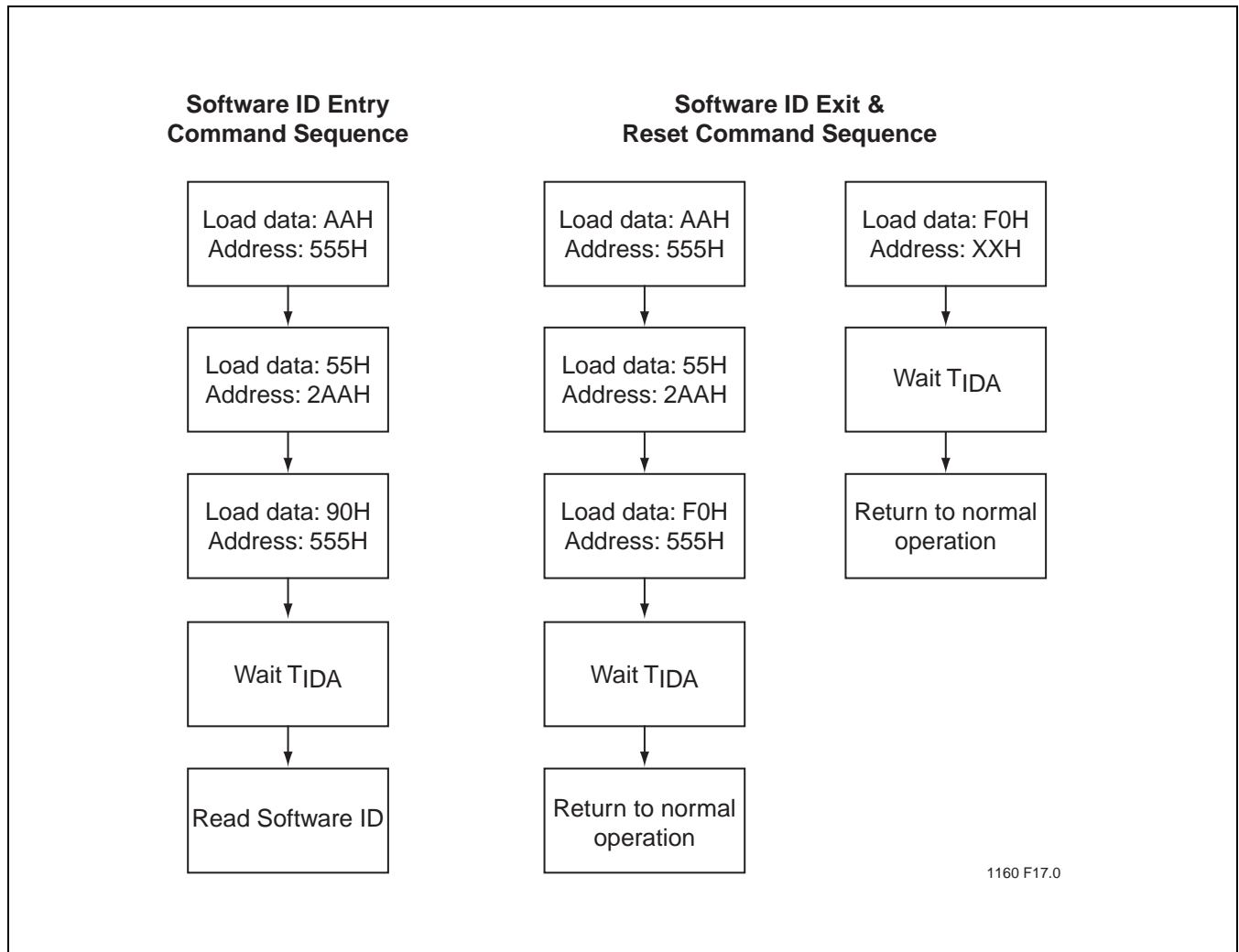
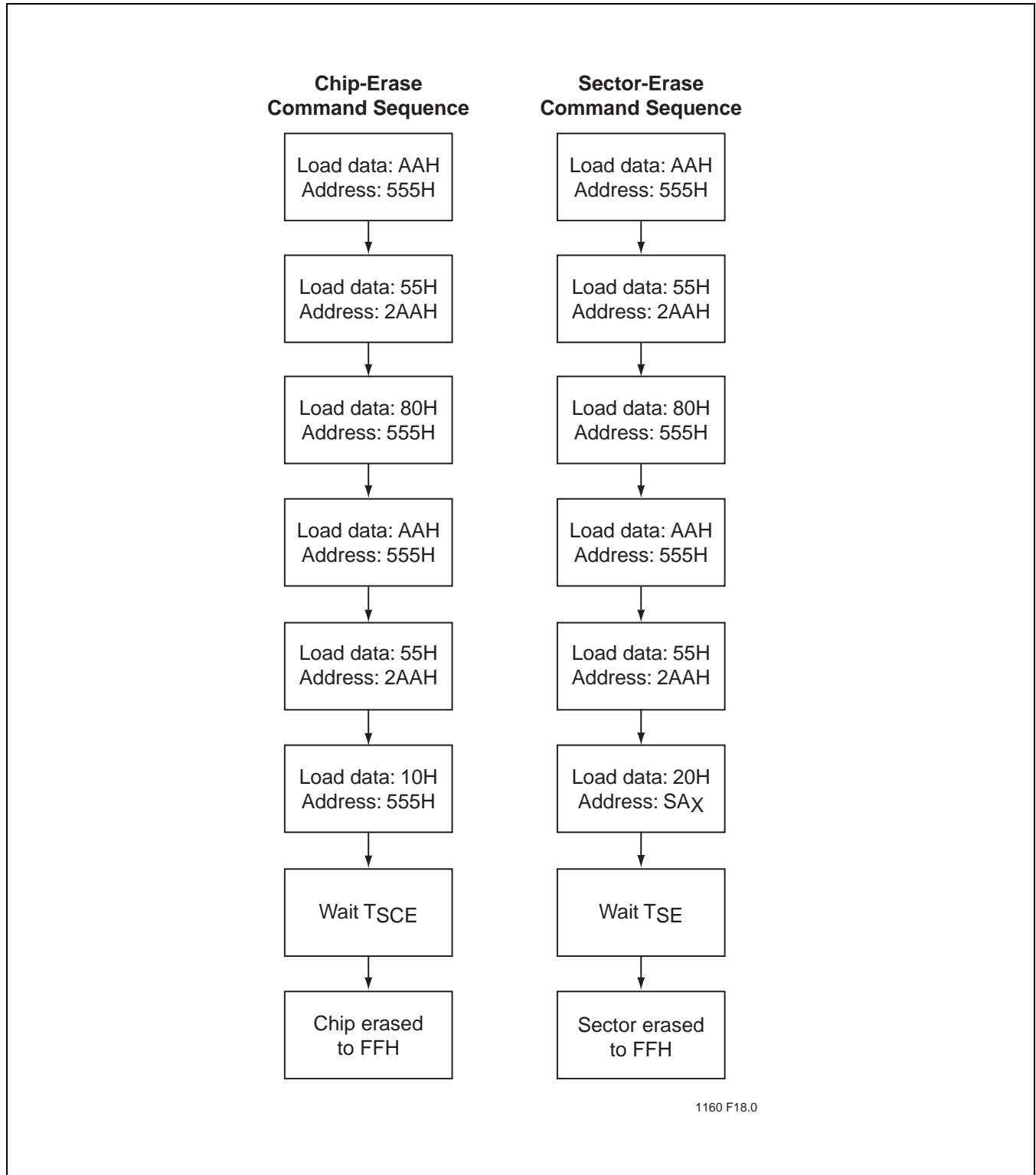


FIGURE 18: Software ID Command Flowcharts

**Data Sheet**


1160 F18.0

**FIGURE 19: Erase Command Sequence**

# 2 Mbit / 4 Mbit Small-Sector Flash

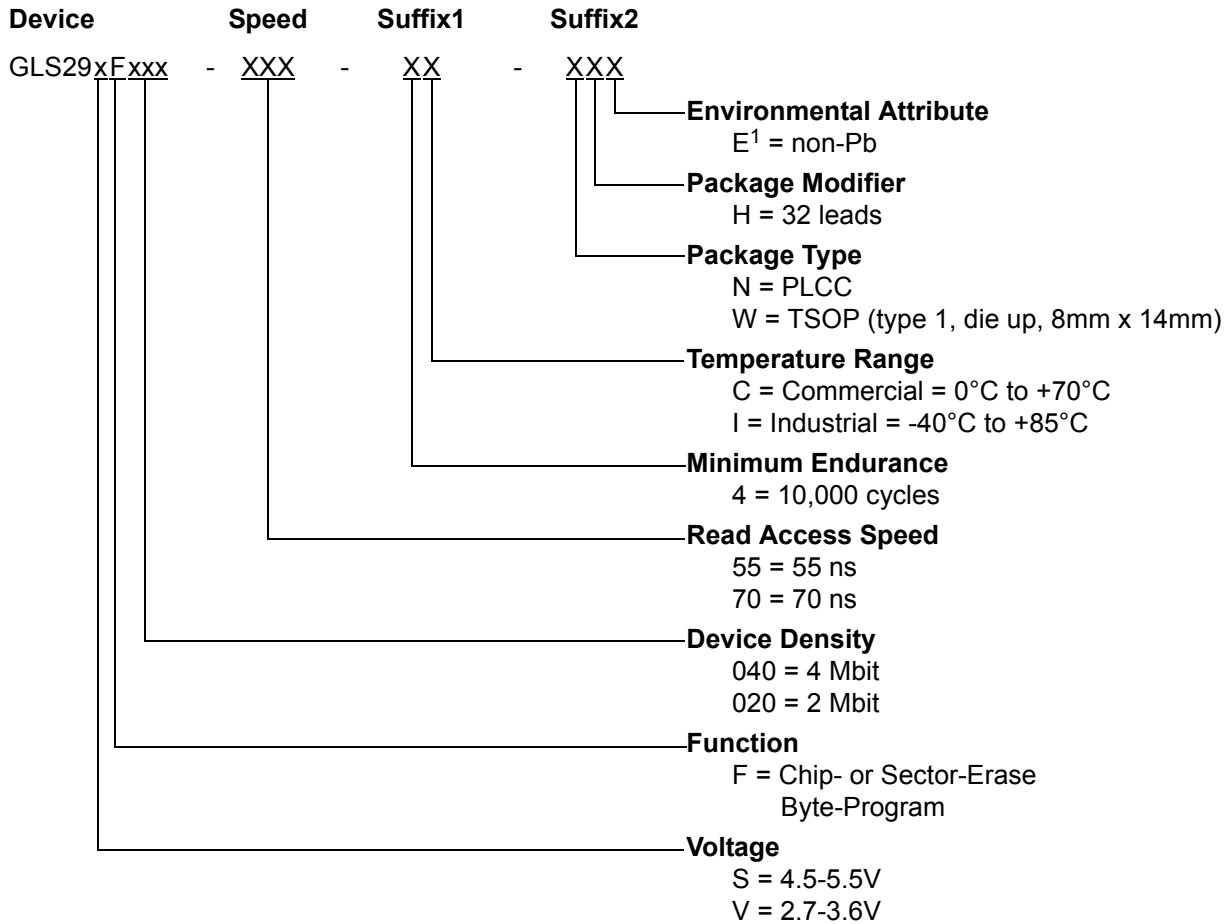
GLS29SF020 / GLS29SF040

GLS29VF020 / GLS29VF040



Data Sheet

## PRODUCT ORDERING INFORMATION



1. Environmental suffix "E" denotes non-Pb solder.  
Greenliant non-Pb solder devices are "RoHS Compliant".

## Data Sheet

**Valid combinations for GLS29SF020**

GLS29SF020-55-4C-NHE    GLS29SF020-55-4C-WHE

GLS29SF020-55-4I-NHE    GLS29SF020-55-4I-WHE

**Valid combinations for GLS29VF020**

GLS29VF020-70-4C-NHE    GLS29VF020-70-4C-WHE

GLS29VF020-70-4I-NHE    GLS29VF020-70-4I-WHE

**Valid combinations for GLS29SF040**

GLS29SF040-55-4C-NH    GLS29SF040-55-4C-WH

GLS29SF040-55-4C-NHE    GLS29SF040-55-4C-WHE

GLS29SF040-55-4I-NH    GLS29SF040-55-4I-WH

GLS29SF040-55-4I-NHE    GLS29SF040-55-4I-WHE

**Valid combinations for GLS29VF040**

GLS29VF040-70-4C-NH    GLS29VF040-70-4C-WH

GLS29VF040-70-4C-NHE    GLS29VF040-70-4C-WHE

GLS29VF040-70-4I-NH    GLS29VF040-70-4I-WH

GLS29VF040-70-4I-NHE    GLS29VF040-70-4I-WHE

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your Greenliant sales representative to confirm availability of valid combinations and to determine availability of new combinations.



# 2 Mbit / 4 Mbit Small-Sector Flash

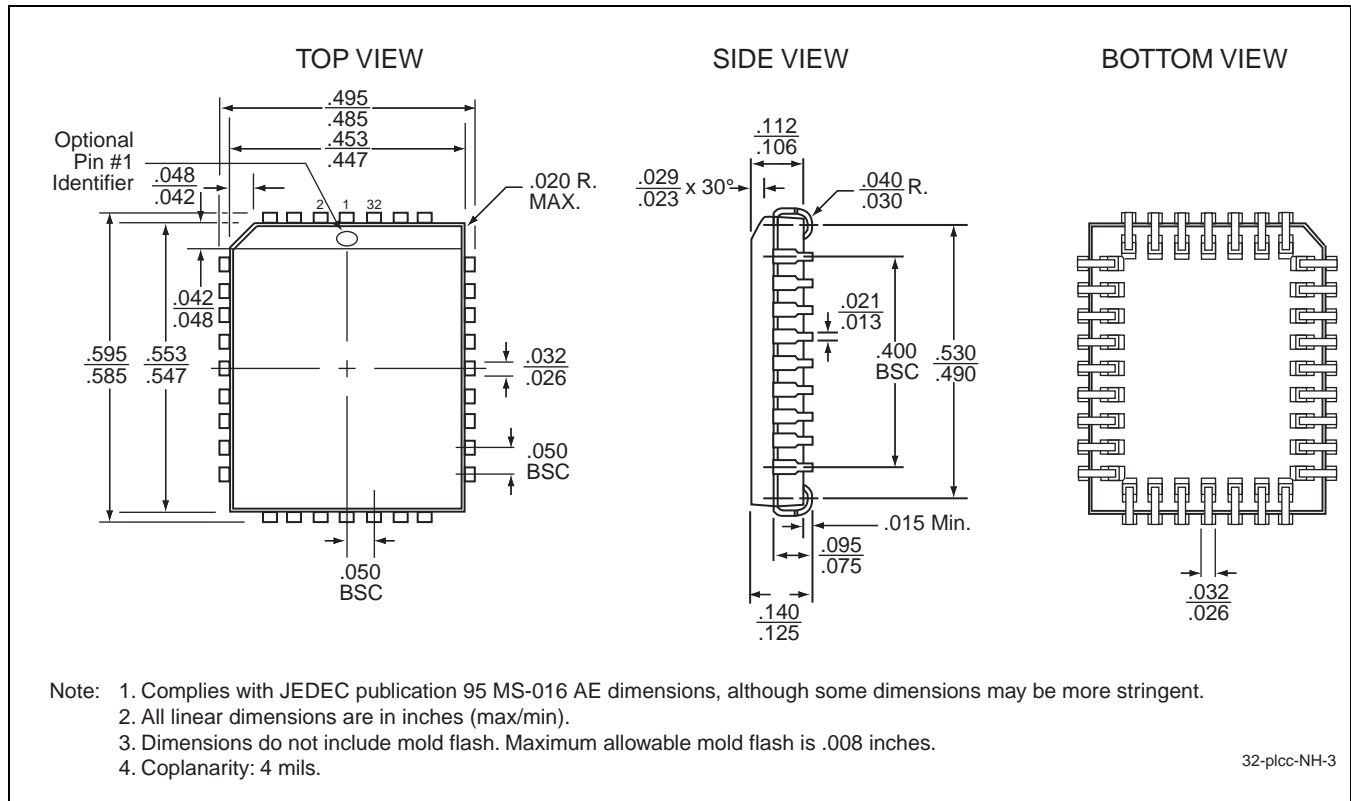
GLS29SF020 / GLS29SF040

GLS29VF020 / GLS29VF040



Data Sheet

## PACKAGING DIAGRAMS

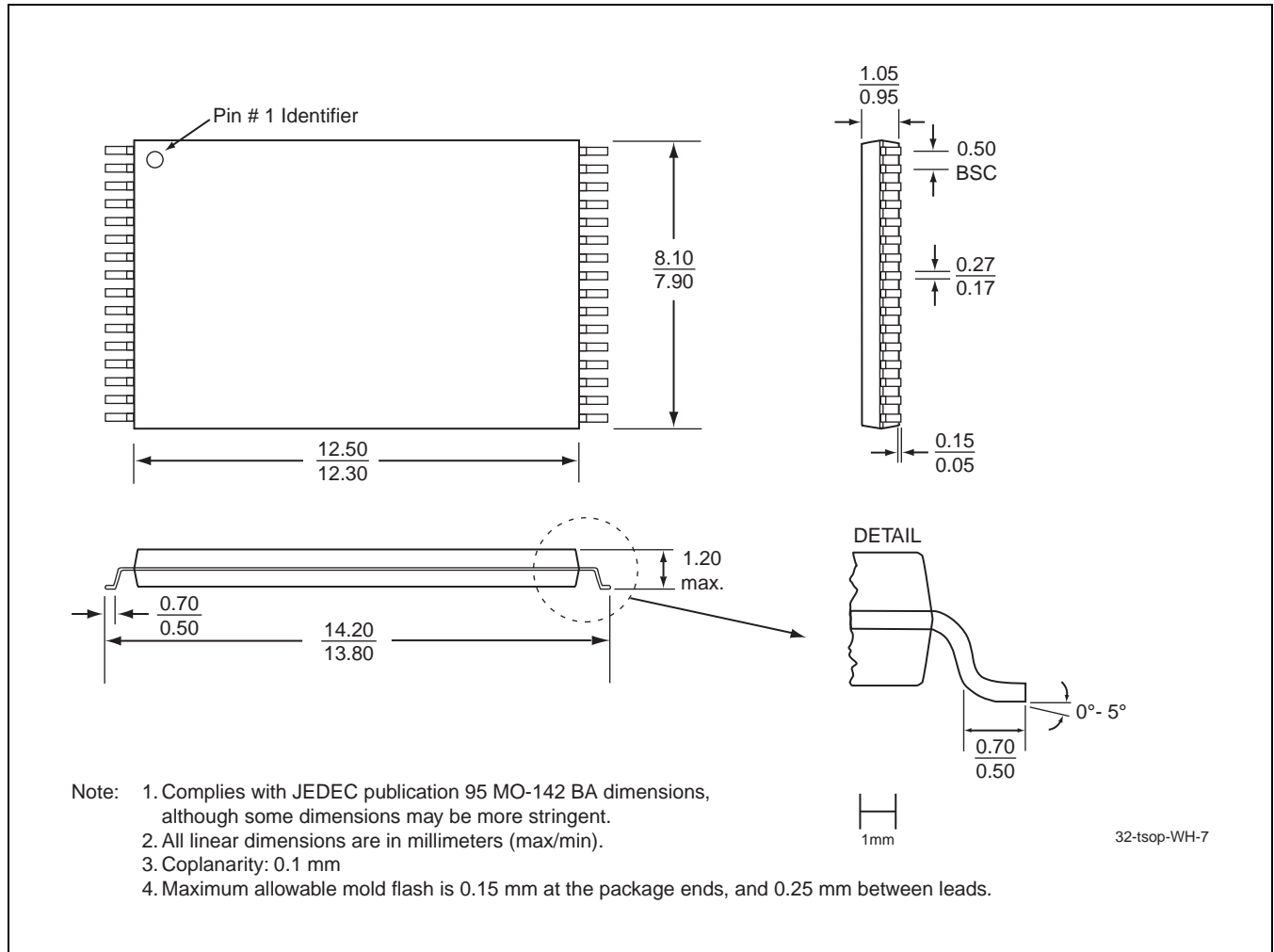


**FIGURE 20: 32-lead Plastic Lead Chip Carrier (PLCC)**  
**Greenliant Package Code: NH**

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**Data Sheet**


**FIGURE 21: 32-lead Thin Small Outline Package (TSOP) 8mm x 14mm  
 Greenliant Package Code: WH**

# 2 Mbit / 4 Mbit Small-Sector Flash

GLS29SF020 / GLS29SF040

GLS29VF020 / GLS29VF040



Data Sheet

TABLE 12: Revision History

| Number | Description   | Date     |
|--------|---|----------|
| 05     | <ul style="list-style-type: none"><li>2002 Data Book</li></ul>  | May 2002 |
| 06     | <ul style="list-style-type: none"><li>Removed 512 Kbit, 1 Mbit, and 2 Mbit parts</li><li>Commercial temperature and 70 ns parts removed</li><li>PH package is no longer offered</li><li>Part number changes - see page 24 for additional information</li><li>Changes to Tables 5 and 6 on page 8 and page 10:<ul style="list-style-type: none"><li>Clarified Test Conditions for Power Supply Current and Read parameters</li><li>Clarified I<sub>DD</sub> Write to be Program and Erase</li><li>Corrected I<sub>DD</sub> Program and Erase from 20 mA to 30 mA</li><li>Corrected I<sub>DD</sub> Read from 20 mA to 25 mA</li></ul></li><li>Clarified measurement reference points V<sub>IT</sub> and V<sub>OT</sub> to be 1.5V instead of 1.5V<sub>DD</sub></li><li>Corrected the V<sub>OL</sub> test condition I<sub>OL</sub> to be 2.1 mA instead of 2.1 μA in Table 5 on page 8</li></ul> | Mar 2003 |
| 07     | <ul style="list-style-type: none"><li>Corrected the Test Conditions for the Read Parameter in Table 5 on page 8</li></ul>   | Apr 2003 |
| 08     | <ul style="list-style-type: none"><li>Added Commercial temperatures for all packages (See page 24 for details)</li></ul>  | Aug 2003 |
| 09     | <ul style="list-style-type: none"><li>2004 Data Book</li><li>Changed status to "Data Sheet"</li></ul>   | Dec 2003 |
| 10     | <ul style="list-style-type: none"><li>Added 70 ns technical data and MPNs for SST29VF040 only</li></ul>   | Feb 2004 |
| 11     | <ul style="list-style-type: none"><li>Added RoHS compliance information on page 1 and in the "Product Ordering Information" on page 23</li><li>Reinstated 512 Kbit, 1 Mbit, and 2 Mbit devices and MPNs (excluding the PDIP package)</li><li>Removed 55 ns technical data and MPNs for SST29VF040</li><li>Added non-Pb MPNs for all devices</li><li>Clarified the solder temperature profile under "Absolute Maximum Stress Ratings" on page 8</li></ul>  | Mar 2005 |
| 12     | <ul style="list-style-type: none"><li>Removed all entries related to SST29SF/VF512 and SST29SF/VF010</li><li>Removed leaded parts for 020 products.</li></ul>   | Nov 2005 |
| 13     | <ul style="list-style-type: none"><li>Changed I<sub>DD</sub> Read from 20mA to 25mA, and Changed I<sub>DD</sub> Write from 20mA to 30mA in Table 5 on page 8 and Table 6 on page 10</li></ul>   | Oct 2006 |
| 14     | <ul style="list-style-type: none"><li>Changed I<sub>SB</sub> from 15 to 30 μA in Table 6 on page 10.</li></ul>  | Oct 2008 |
| 15     | <ul style="list-style-type: none"><li>Transferred from SST to Greenliant</li></ul>  | May 2010 |

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