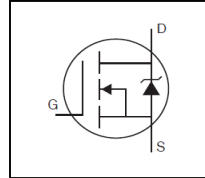


**Features**

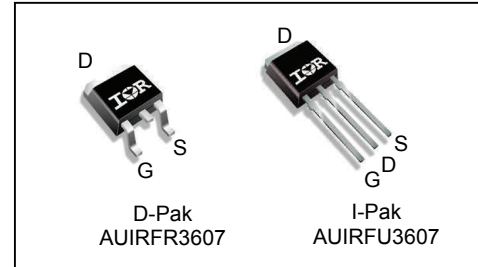
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified \*



$V_{DS}$		<b>75V</b>
$R_{DS(on)}$	typ.	<b>7.34mΩ</b>
	max.	<b>9.0mΩ</b>
$I_D$ (Silicon Limited)		<b>80A</b> ①
$I_D$ (Package Limited)		<b>56A</b>

**Description**

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRFU3607	I-Pak	Tube	75	AUIRFU3607
AUIRFR3607	D-Pak	Tube	75	AUIRFR3607
		Tape and Reel Left	3000	AUIRFR3607TRL

**Absolute Maximum Ratings**

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	80①	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	56①	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	56	
$I_{DM}$	Pulsed Drain Current ②	310	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	140	W
	Linear Derating Factor	0.96	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ③	120	mJ
$I_{AR}$	Avalanche Current ②	46	A
$E_{AR}$	Repetitive Avalanche Energy ⑤	14	mJ
dv/dt	Peak Diode Recovery dv/dt④	27	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	1.045	°C/W
$R_{\theta JA}$	Junction-to-Ambient ( PCB Mount) ⑥	—	50	
$R_{\theta JA}$	Junction-to-Ambient ⑥	—	110	

HEXFET® is a registered trademark of Infineon.

\*Qualification standards can be found at [www.infineon.com](http://www.infineon.com)

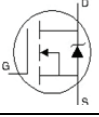
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	75	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.096	—	V/°C	Reference to 25°C, I <sub>D</sub> = 5mA ②
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	7.34	9.0	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 46A ⑤
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA
g <sub>fs</sub>	Forward Trans conductance	115	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 46A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 75V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V

**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

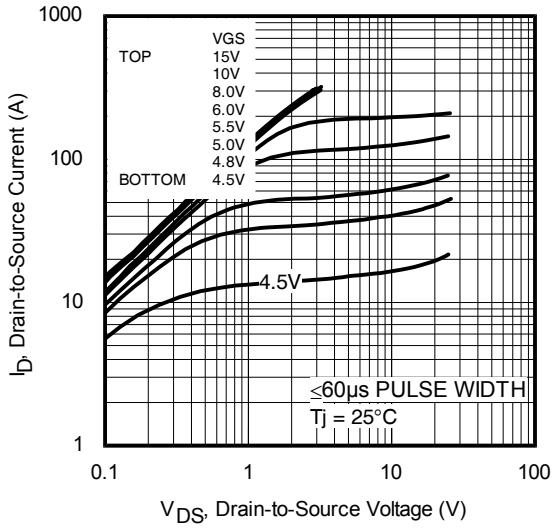
Q <sub>g</sub>	Total Gate Charge	—	56	84	nC	I <sub>D</sub> = 46A V <sub>DS</sub> = 38V V <sub>GS</sub> = 10V ⑤
Q <sub>gs</sub>	Gate-to-Source Charge	—	13	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	16	—		
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )	—	40	—		
R <sub>G</sub>	Gate Resistance	—	0.55	—	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	16	—	ns	V <sub>DD</sub> = 49V I <sub>D</sub> = 46A R <sub>G</sub> = 6.8Ω V <sub>GS</sub> = 10V ⑤
t <sub>r</sub>	Rise Time	—	110	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	43	—		
t <sub>f</sub>	Fall Time	—	96	—		
C <sub>iss</sub>	Input Capacitance	—	3070	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 50V f = 1.0MHz V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 60V ⑧ V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 60V ⑨
C <sub>oss</sub>	Output Capacitance	—	280	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	130	—		
C <sub>oss eff. (ER)</sub>	Effective Output Capacitance (Energy Related)	—	380	—		
C <sub>oss eff. (TR)</sub>	Effective Output Capacitance (Time Related)	—	610	—		

**Diode Characteristics**

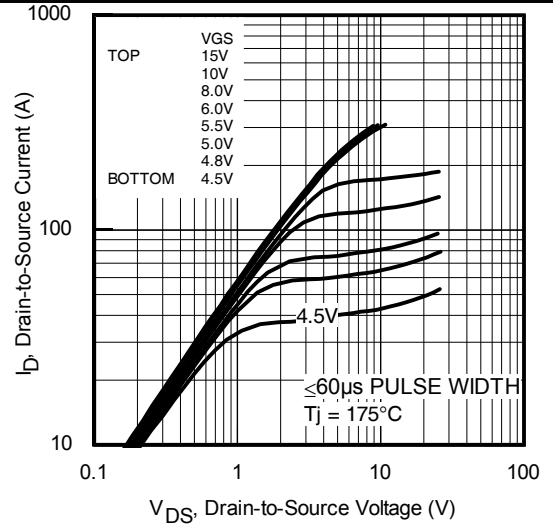
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	80 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	310		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 46A, V <sub>GS</sub> = 0V ⑤
t <sub>rr</sub>	Reverse Recovery Time	—	33	50	ns	T <sub>J</sub> = 25°C — V <sub>R</sub> = 64V, T <sub>J</sub> = 125°C — I <sub>F</sub> = 46A
Q <sub>rr</sub>	Reverse Recovery Charge	—	32	48		
I <sub>RRM</sub>	Reverse Recovery Current	—	1.9	—	A	T <sub>J</sub> = 25°C
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

**Notes:**

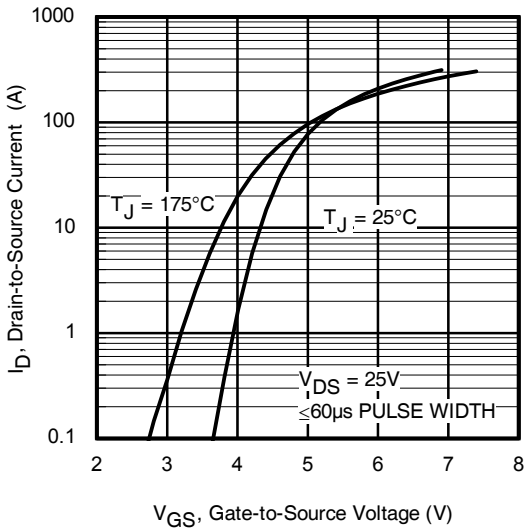
- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 56A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ③ Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.12mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 46A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ④ I<sub>SD</sub> ≤ 46A, di/dt ≤ 1920A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑥ C<sub>oss eff. (TR)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑦ C<sub>oss eff. (ER)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑨ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C.



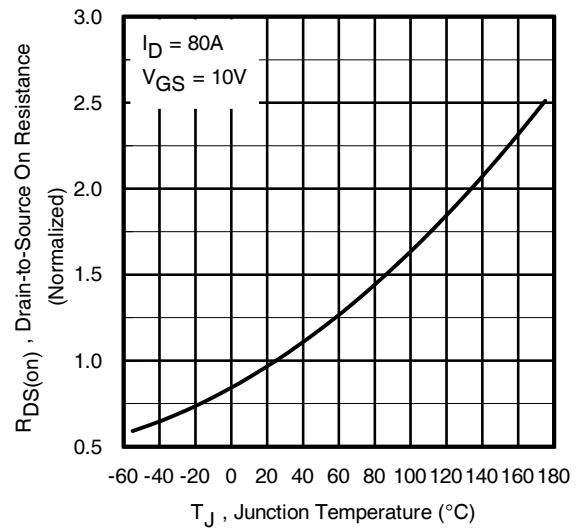
**Fig. 1 Typical Output Characteristics**



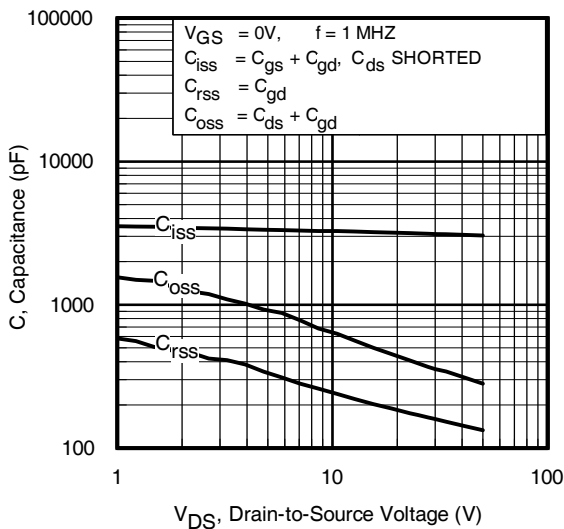
**Fig. 2 Typical Output Characteristics**



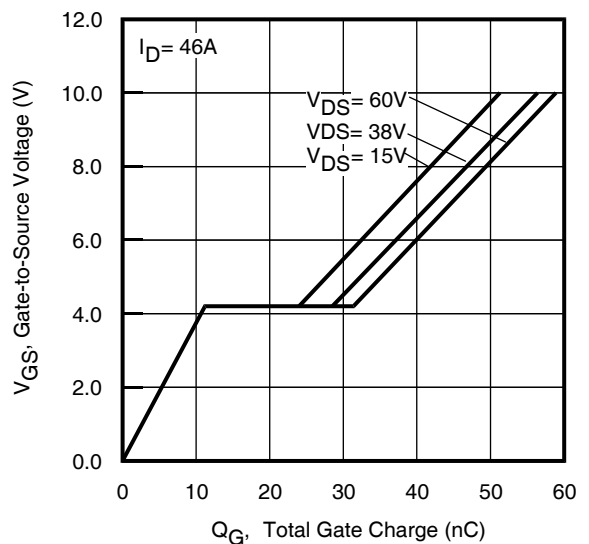
**Fig. 3 Typical Transfer Characteristics**



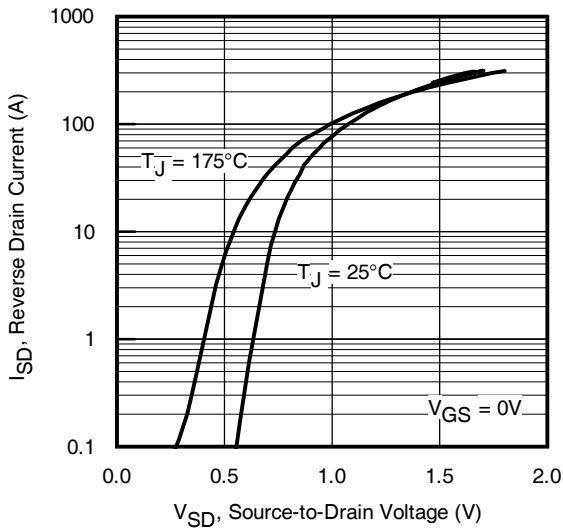
**Fig. 4 Normalized On-Resistance vs. Temperature**



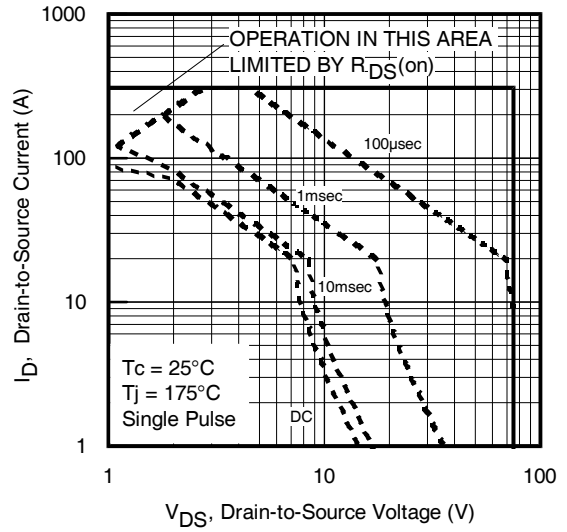
**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**



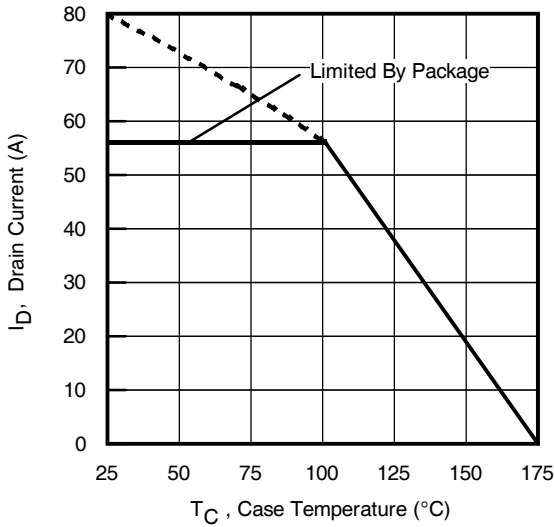
**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**



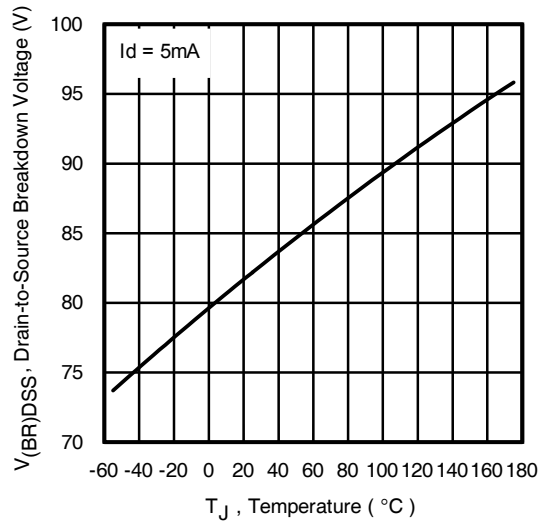
**Fig. 7** Typical Source-to-Drain Diode Forward Voltage



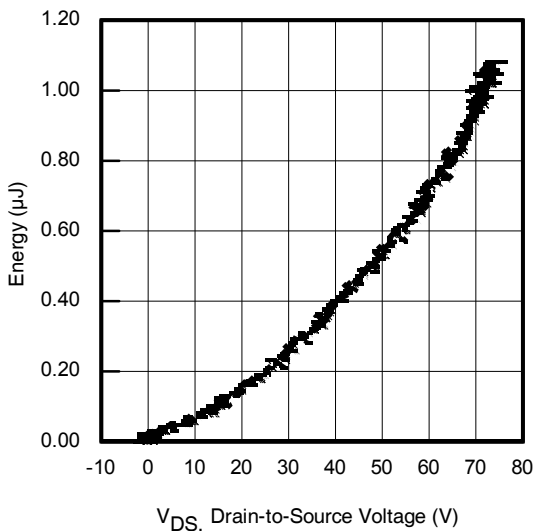
**Fig 8.** Maximum Safe Operating Area



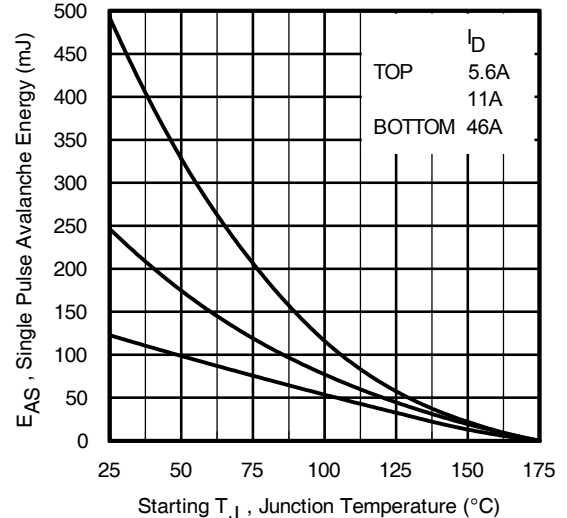
**Fig. 9** Maximum Drain Current vs. Case Temperature



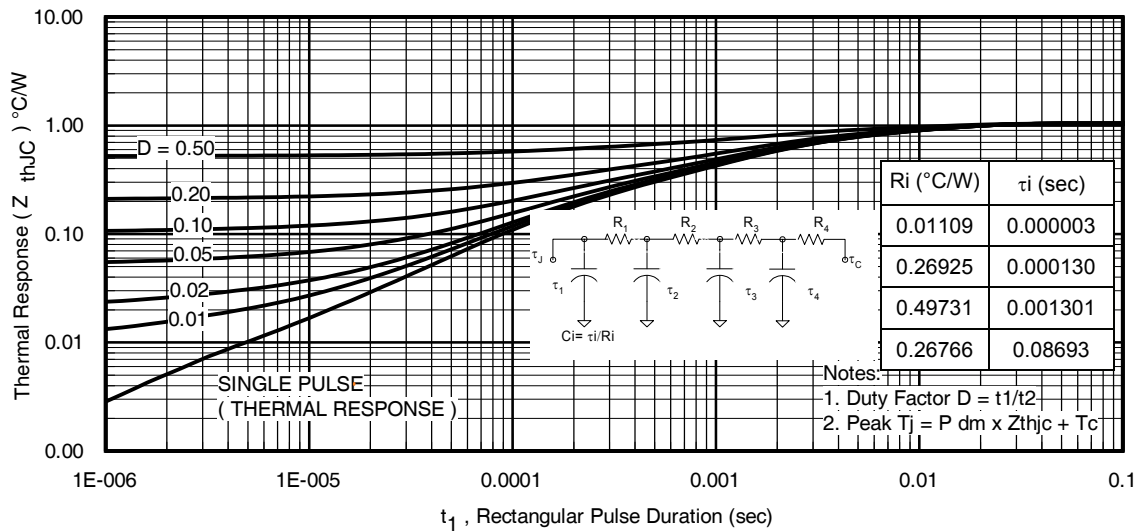
**Fig 10.** Drain-to-Source Breakdown Voltage



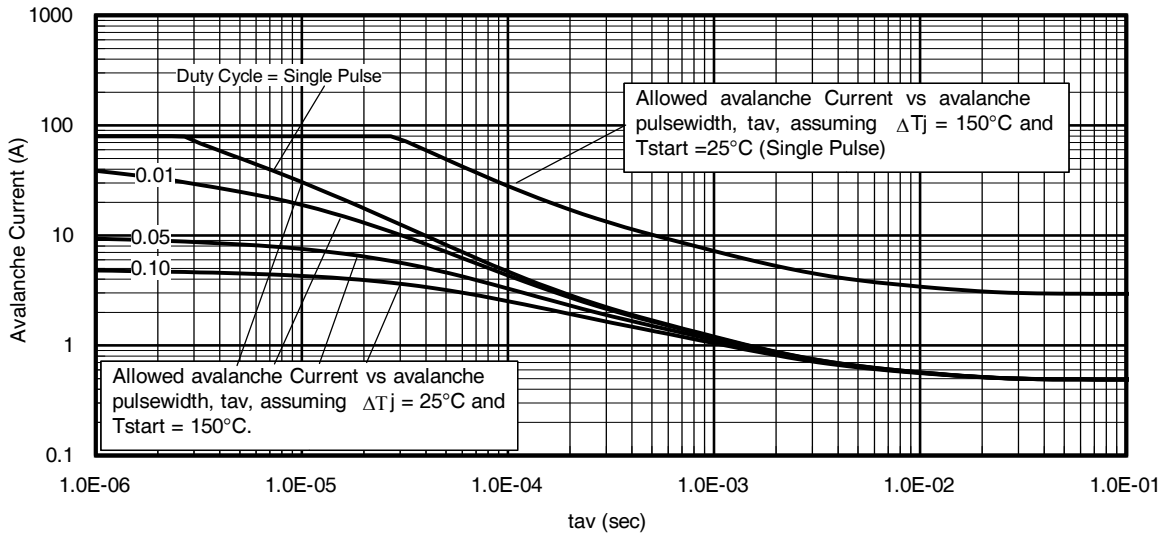
**Fig. 11** Typical Coss Stored Energy



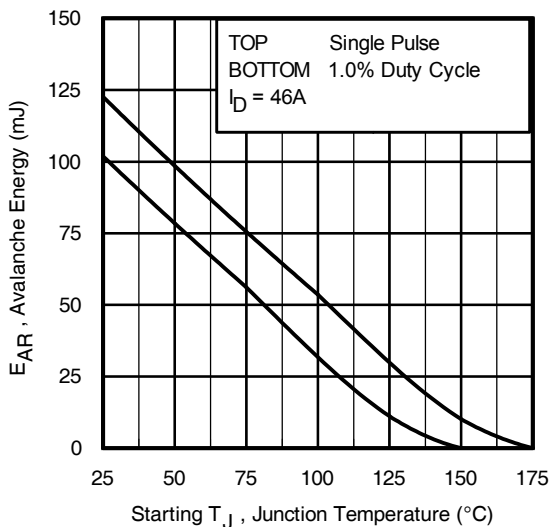
**Fig 12.** Maximum Avalanche Energy vs. Drain Current



**Fig 13.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



**Fig 14.** Typical Avalanche Current Vs. Pulse width



**Notes on Repetitive Avalanche Curves , Figures 14, 15:**  
**(For further info, see AN-1005 at [www.infineon.com](http://www.infineon.com))**

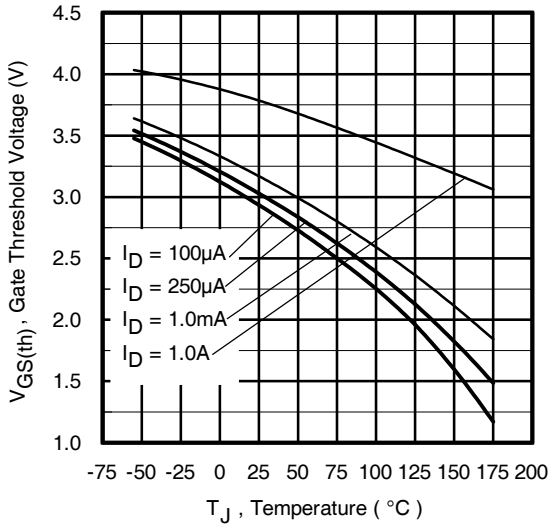
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 13, 14).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thjc}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thjc}$$

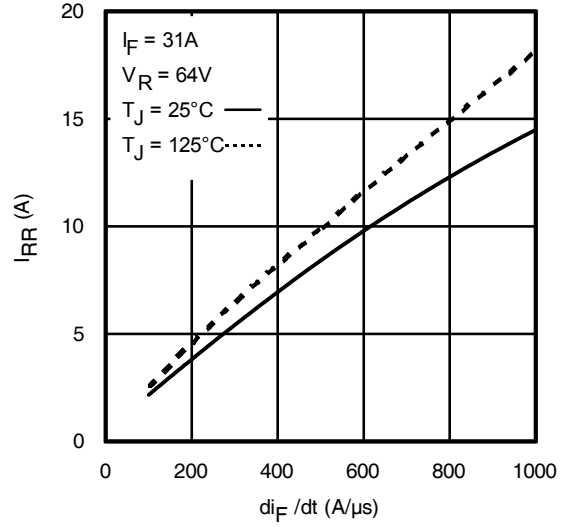
$$I_{av} = 2\Delta T / [ 1.3 \cdot BV \cdot Z_{thjc} ]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

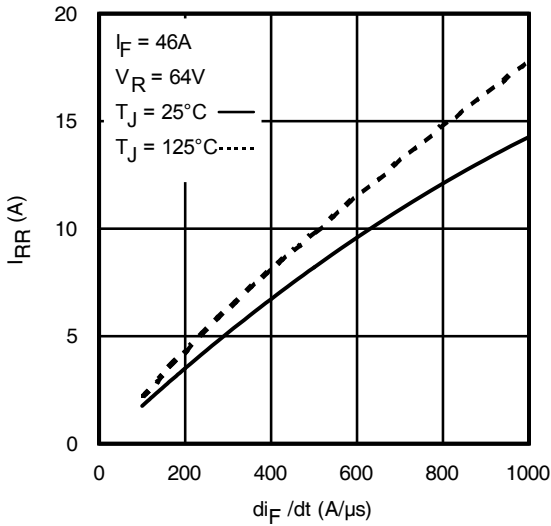
**Fig 15.** Maximum Avalanche Energy Vs. Temperature



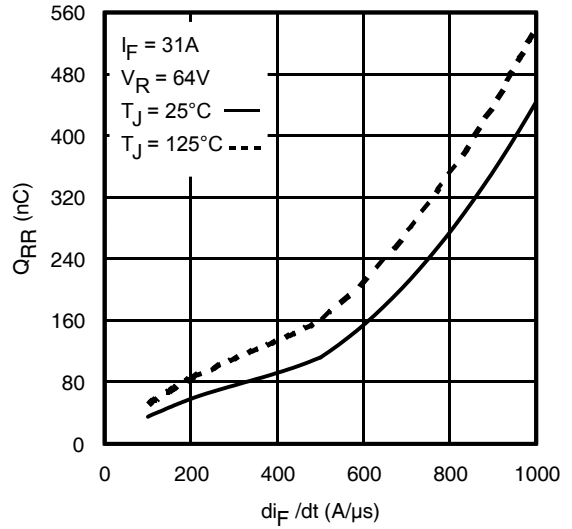
**Fig 16.** Threshold Voltage vs. Temperature



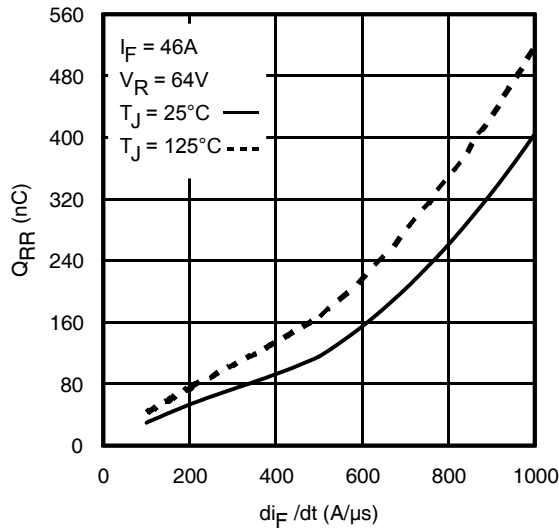
**Fig. 17 -** Typical Recovery Current vs. di/dt



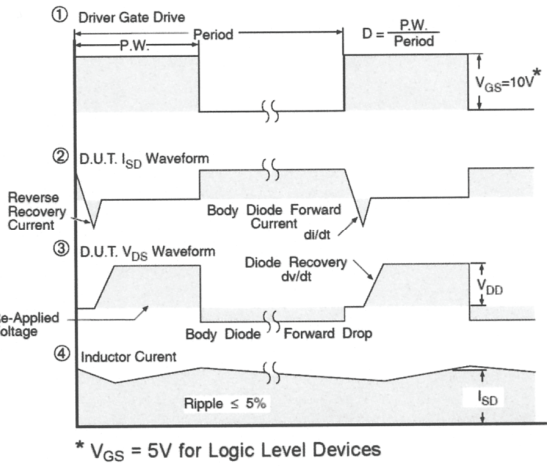
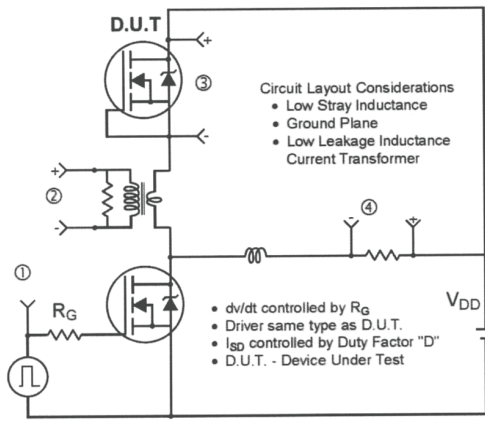
**Fig. 18 -** Typical Recovery Current vs. di/dt



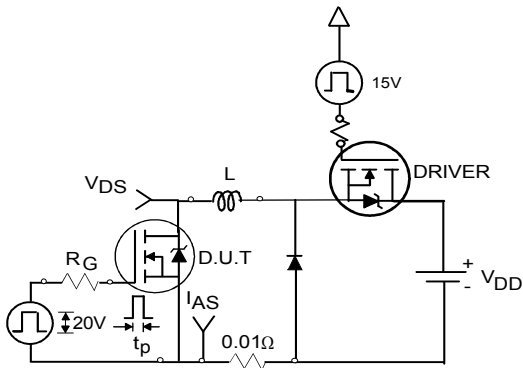
**Fig. 19 -** Typical Stored Charge vs. di/dt



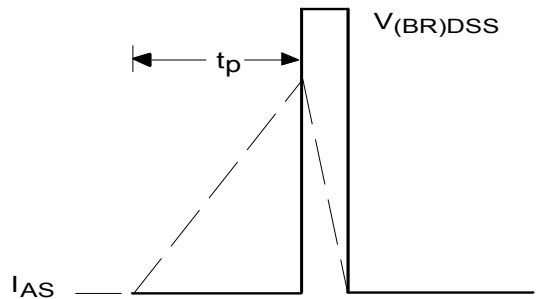
**Fig. 20 -** Typical Stored Charge vs. di/dt



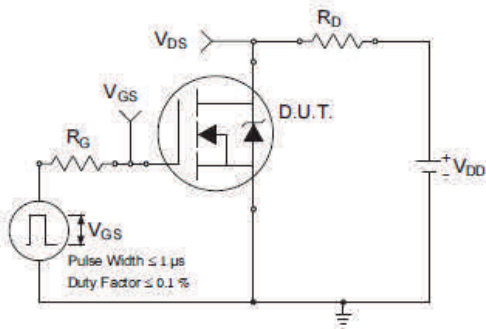
**Fig 20.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



**Fig 21a.** Unclamped Inductive Test Circuit



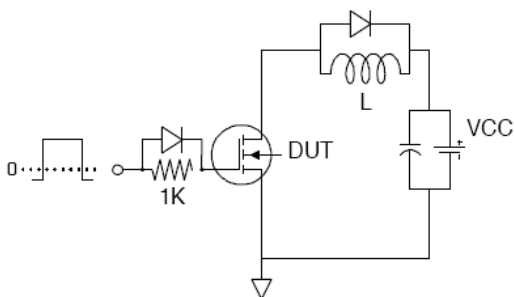
**Fig 21b.** Unclamped Inductive Waveforms



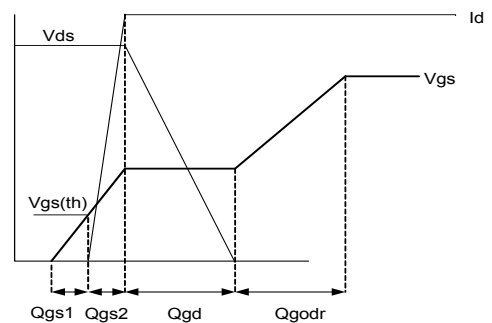
**Fig 22a.** Switching Time Test Circuit



**Fig 22b.** Switching Time Waveforms



**Fig 23a.** Gate Charge Test Circuit



**Fig 23b.** Gate Charge Waveform

## D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))



**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
φ	0"	10"	0"	10"	
φ1	0"	15"	0"	15"	
φ2	25"	35"	25"	35"	

LEAD ASSIGNMENTS

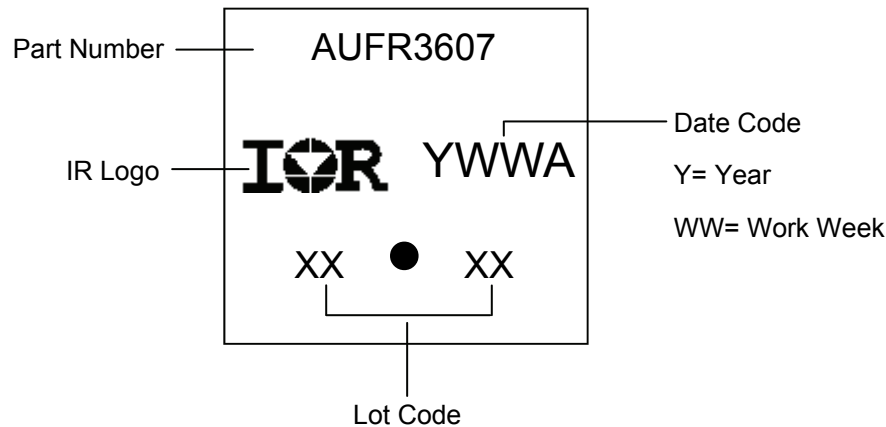
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

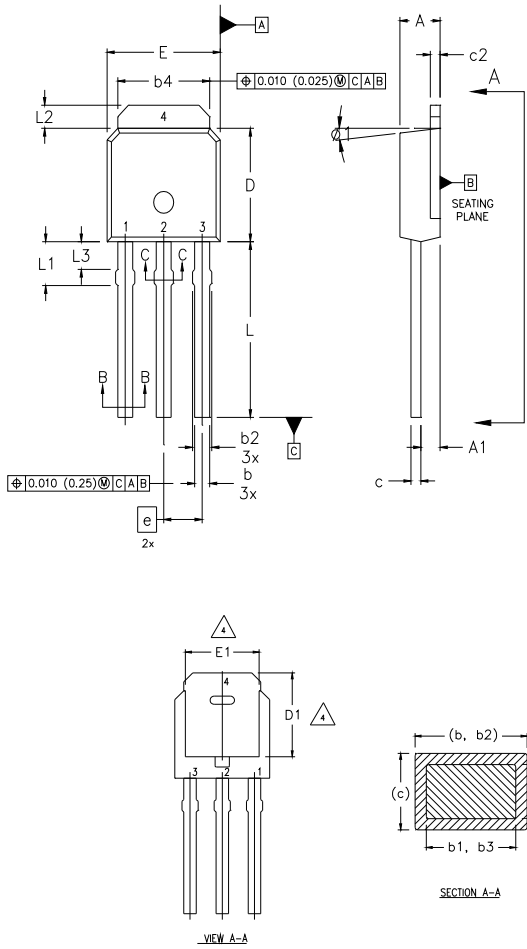
## D-Pak (TO-252AA) Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



## I-Pak (TO-251AA) Package Outline (Dimensions are shown in millimeters (inches))



**NOTES:**

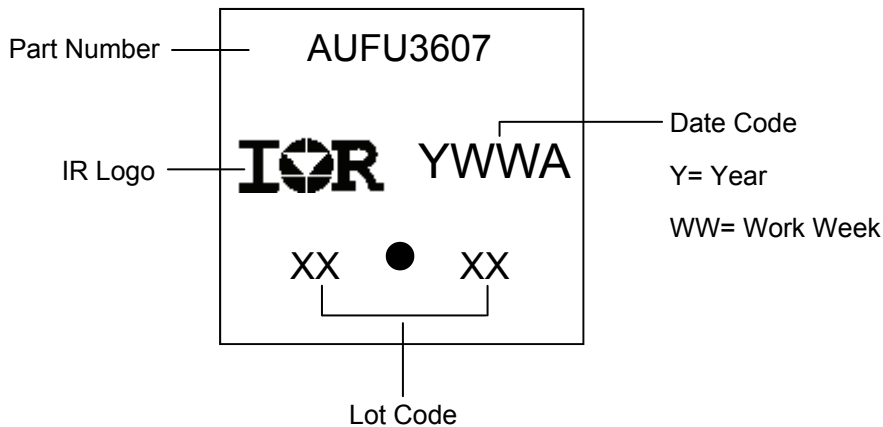
- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

LEAD ASSIGNMENTS

- HEXFET
- 1.- GATE
  - 2.- DRAIN
  - 3.- SOURCE
  - 4.- DRAIN

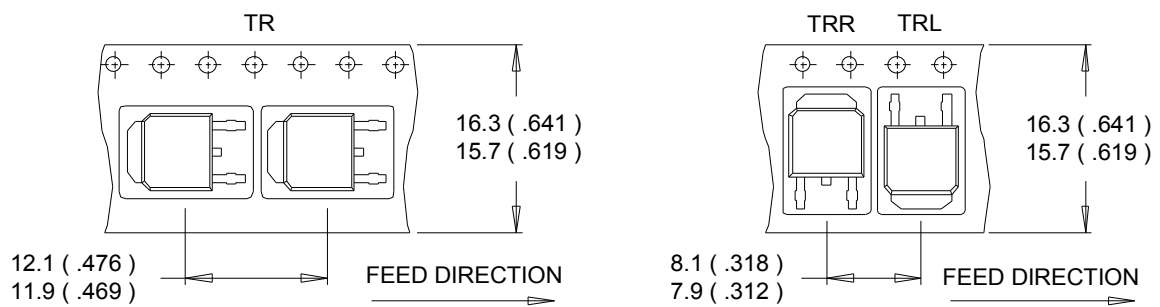
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	0"	15"	0"	15"	

## I-Pak (TO-251AA) Part Marking Information



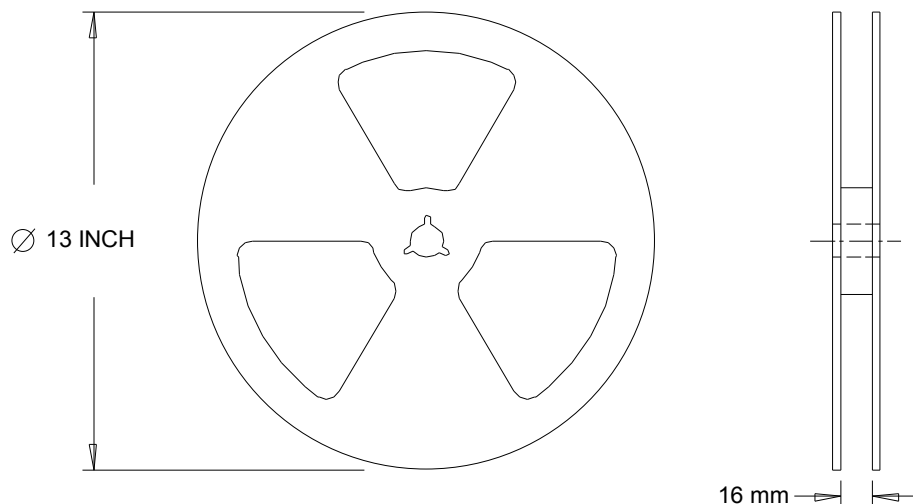
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D-Pak (TO-252AA) Tape & Reel Information** (Dimensions are shown in millimeters (inches))



**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information**

<b>Qualification Level</b>		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		D-Pak	MSL1
		I-Pak	
<b>ESD</b>	Machine Model	Class M4 (+/- 600V) <sup>†</sup> AEC-Q101-002	
	Human Body Model	Class H1C (+/- 2000V) <sup>†</sup> AEC-Q101-001	
	Charged Device Model	Class C4 (+/- 1000V) <sup>†</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

† Highest passing voltage.

**Revision History**

Date	Comments
10/12/2015	<ul style="list-style-type: none"> <li>Updated datasheet with corporate template</li> <li>Corrected ordering table on page 1.</li> </ul>

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