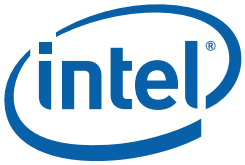

Mobile Intel® Atom™ Processor N270 Single Core

Datasheet

May 2008

Document Number: 320032-001

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Revision History

Document Number	Revision Number	Description	Revision Date
320032	001	Initial release.	May 2008

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1 Introduction

The Intel® Atom™ Processor N270 (code named Mobile Diamondville) is built on 45-nanometer process technology — the first generation of low-power IA-32 micro-architecture specially designed for Netbook'08 Platform. In this platform, the processor supports Intel® 945GSE chipset with the I/O Controller Hub - Intel 82801GBM.

Note: Throughout this document, the Intel® Atom™ Processor N270 is referred as processor.

1.1 Major Features

The following list provides some of the key features on this processor:

- New single-core processor for mobile devices
- On-die, primary 32-kB instructions cache and 24-kB write-back data cache
- 533-MHz source-synchronous front side bus (FSB)
- 2-Threads support
- On-die 512-kB, 8-way L2 cache
- Support for IA 32-bit architecture
- Intel® Streaming SIMD Extensions-2 and -3 (Intel® SSE2 and Intel® SSE3) support and Supplemental Streaming SIMD Extension 3 (SSSE3) support
- Micro-FCBGA8 packaging technologies
- Thermal management support via Intel® Thermal Monitor 1 and Intel Thermal Monitor 2
- FSB Lane Reversal for flexible routing
- Supports C0/C1(e)/C2(e)/C4(e)
- L2 Dynamic Cache Sizing
- Advanced power management features including Enhanced Intel SpeedStep® Technology
- Execute Disable Bit support for enhanced security

1.2 Terminology

Term	Definition
#	A "#" symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a non-maskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as address or data), the "#" symbol implies that the signal is inverted. For example, D [3:0] = "HLHL" refers to a hex 'A', and D [3:0]# = "LHLH" also refers to a hex "A" (H= High logic level, L= Low logic level).
Front Side Bus (FSB)	Refers to the interface between the processor and system core logic (also known as the GMCH chipset components).
AGTL+	Advanced Gunning Transceiver Logic. Used to refer to Assisted GTL+ signaling technology on some Intel processors.
CMOS	Complementary metal-Oxide semiconductor.
Storage Conditions	Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased, or receive any clocks. Upon exposure to "free air" (i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
Enhanced Intel SpeedStep® Technology	Technology that provides power management capabilities to low power devices.
Processor Core	Processor core die with integrated L1 and L2 cache. All AC timing and signal integrity specifications are at the pads of the processor core.
TDP	Thermal Design Power
V_{CC}	The processor core power supply
VR	Voltage Regulator
V_{SS}	The processor ground
V_{CC}HFM	V_{CC} at Highest Frequency Mode (HFM).
V_{CC}LFM	V_{CC} at Lowest Frequency Mode (LFM).

Term	Definition
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up.
V_{CCP}	AGTL+ Termination Voltage.
V_{CCA}	PLL Supply voltage.
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep (C4).
V_{CCF}	Fuse Power Supply.
I_{CCDES}	I_{CC} for Mobile Intel® Atom™ Processor N270 Recommended Design Target (Estimated).
I_{CC}	I_{CC} for Mobile Intel® Atom™ Processor N270 is the number that can be use as a reflection on a battery life estimates.
$I_{AH,}$	I_{CC} Auto-Halt
I_{SGNT}	I_{CC} Stop-Grant.
I_{DSLP}	I_{CC} Deep Sleep.
$dI_{CC/dt}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin (Estimated).
I_{CCA}	I_{CC} for V_{CCA} Supply.
P_{AH}	Auto Halt Power.
P_{SGNT}	Stop Grant Power.
P_{DPRSLP}	Deeper Sleep Power.
T_J	Junction Temperature.

1.3 References

Material and concepts available in the following documents may be beneficial when reading this document.

Table 1. References

Document	Document No./Location
Intel® 64 and IA-32 Architectures Software Developer's Manuals • *Intel® 64 and IA-32 Architectures Software Developer's Manual Volume 1: Basic Architecture* • *Intel® 64 and IA-32 Architectures Software Developer's Manual Volume 2A: Instruction Set Reference, A-M* • *Intel® 64 and IA-32 Architectures Software Developer's Manual Volume 2B: Instruction Set Reference, N-Z* • *Intel® 64 and IA-32 Architectures Software Developer's Manual Volume 3A: System Programming Guide* • *Intel® 64 and IA-32 Architectures Software Developer's Manual Volume 3B: System Programming Guide*	http://www.intel.com/products/processor/manuals/
Mobile Intel® 945 Express Chipset Family Datasheet	309219
Mobile Intel® 945 Express Chipset Family Specification Update	309220
Intel® I/O Controller Hub 7 (ICH7) Family Datasheet	307013
Intel® I/O Controller Hub 7 (ICH7) Family Specification Update	307014
AP-485, Intel® Processor Identification and CPUID Instruction Application Note	241618

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2 Low Power Features

2.1 Clock Control and Low-power States

The processor supports low power states at the thread level and the package level. A thread may independently enter the C1/AutoHALT, C1/MWAIT, C2, C3, and C4 low power states. Package low power states include Normal, Stop Grant, Stop Grant Snoop, Sleep and Deep Sleep. When both threads are in a common low-power state the central power management logic ensures the entire processor enters the respective package low power state by initiating a P_LVLx (P_LVL2 and P_LVL3) I/O read to the chipset.

The processor implements two software interfaces for requesting low power states, MWAIT instruction extensions with sub-state hints and P_LVLx reads to the ACPI P_BLK register block mapped in the processor's I/O address space. The P_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor and do not directly result in I/O reads on the processor FSB. The monitor address does not need to be setup before using the P_LVLx I/O read interface. The sub-state hints used for each P_LVLx read can be configured in a software programmable MSR. If a thread encounters a chipset break event while STPCLK# is asserted, then it asserts the PBE# output signal. Assertion of PBE# when STPCLK# is asserted indicates to system logic that individual threads should return to the C0 state and the processor should return to the Normal state.

Figure 1 shows the thread low-power states. Figure 2 shows the package low-power states. Table 2 provides a mapping of thread low-power states to package low power states.

Figure 1. Thread Low-power States

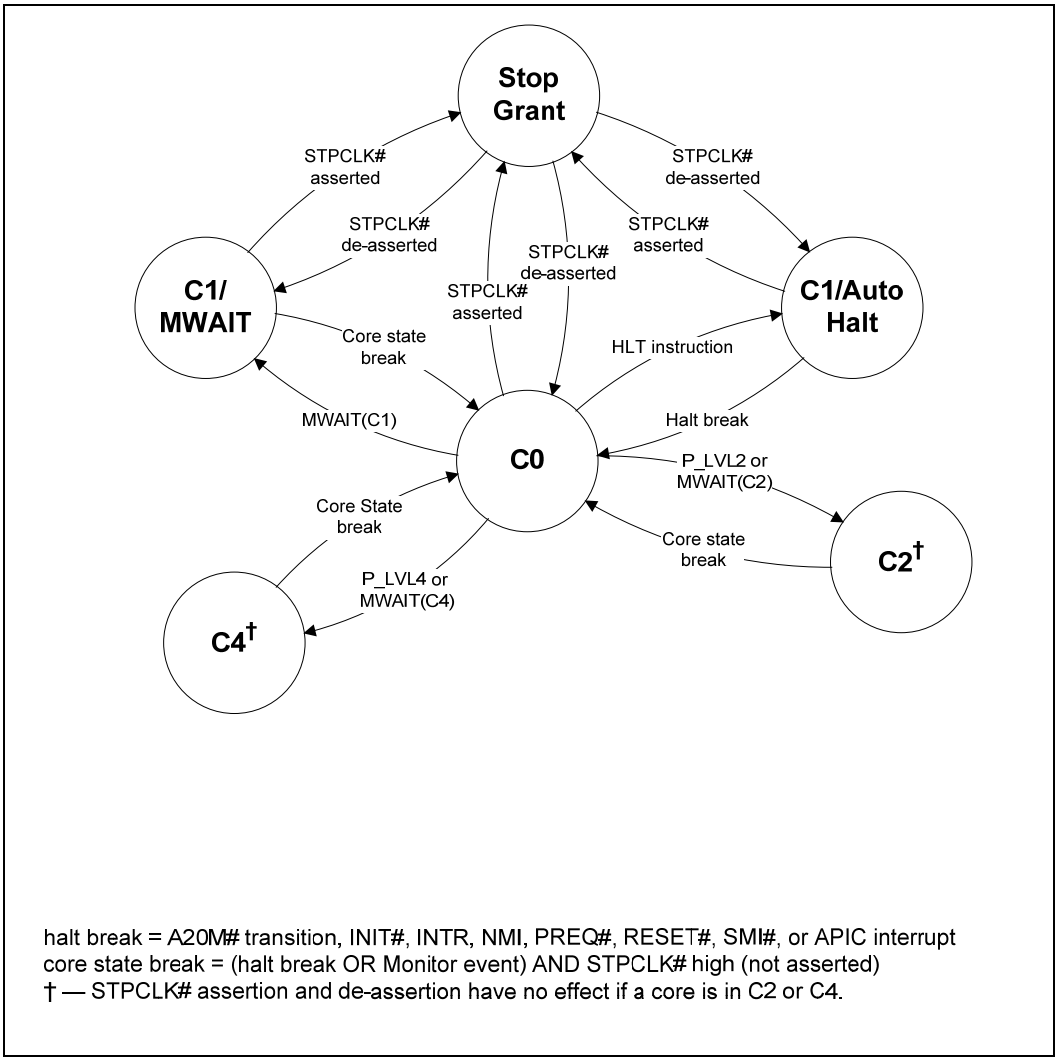

Figure 2. Package Low-power States

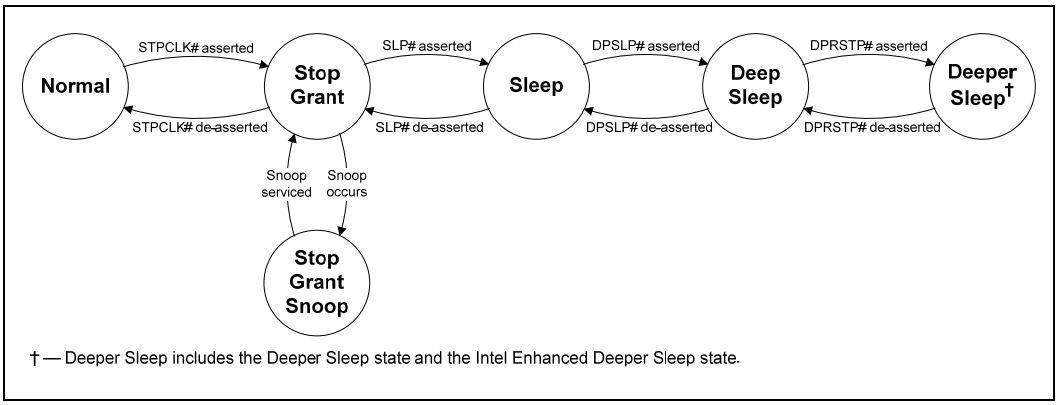

Table 2. Coordination of Thread Low-power States at the Package Level

Thread State	Package State[2]			
	C0	C1[1]	C2	C4
C0	Normal	Normal	Normal	Normal
C1[1]	Normal	AutoHalt	AutoHalt	AutoHalt
C2	Normal	AutoHalt	Stop-Grant	Stop-Grant
C4	Normal	AutoHalt	Stop-Grant	Deeper Sleep /Intel® Enhanced Deeper Sleep

NOTES:
1. AutoHALT or MWAIT/C1.
2. To enter a package state, both threads must be in a common low power state. If the threads are not in a common low power state, the package state will resolve to the highest power C state.

2.1.1 Thread Low-power State Descriptions

2.1.1.1 Thread C0 State

This is the normal operating state for threads in the processor.

2.1.1.2 Thread C1/AutoHALT Power-down State

C1/AutoHALT is a low-power state entered when a thread executes the HALT instruction. The processor thread will transition to the C0 state upon occurrence of SMI#, INIT#, LINT [1:0] (NMI, INTR), or FSB interrupt messages. RESET# will cause the processor to immediately initialize itself.

A System Management Interrupt (SMI) handler will return execution to either Normal state or the AutoHALT Power-down state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 3A/3B: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Power-down state. When the system de-asserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT Power-down state, the processor threads will process bus snoops and snoops from the other thread. The processor will enter a snoopable sub-state (not shown in Figure 1) to process the snoop and then return to the AutoHALT Power-down state.

2.1.1.3 Thread C1/MWAIT Power-down State

C1/MWAIT is a low-power state entered when the processor thread executes the MWAIT(C1) instruction. Processor behavior in the MWAIT state is identical to the AutoHALT state except that Monitor events can cause the processor to return to the C0 state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 2A: Instruction Set Reference, A-M* and *Volume 2B: Instruction Set Reference, N-Z*, for more information.

2.1.1.4 Thread C2 State

Individual threads of the dual-threaded processor can enter the C2 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C2) instruction, but the processor will not issue a Stop-Grant Acknowledge special bus cycle unless the STPCLK# pin is also asserted.

While in the C2 state, the processor will process bus snoops and snoops from the other thread. The processor thread will enter a snoopable sub-state (not shown in Figure 1) to process the snoop and then return to the C2 state.

2.1.1.5 Thread C4 State

Individual threads of the processor can enter the C4 state by initiating a P_LVL4 I/O read to the P_BLK or an MWAIT(C4) instruction. If both processor threads are in C4, the central power management logic will request that the entire processor enter the Deeper Sleep package low-power state (see Section 2.1.2.6).

To enable the package level Intel Enhanced Deeper Sleep state, Dynamic Cache Sizing and Intel Enhanced Deeper Sleep state fields must be configured in the software programmable MSR bit.

2.1.2 Package Low-power State Descriptions

The following state descriptions assume that both threads are in a common low power state. For cases when only one thread is in a low power state (see Section 2.1.1).

2.1.2.1 Normal State

This is the normal operating state for the processor. The processor remains in the Normal state when the threads are in the C0, C1/AutoHALT, or C1/MWAIT state.

2.1.2.2 Stop-Grant State

When the STPCLK# pin is asserted, each thread of the processors enters the Stop-Grant state within 1384 bus clocks after the response phase of the processor-issued Stop-Grant Acknowledge special bus cycle. When the STPCLK# pin is de-asserted, the core returns to its previous low-power state.

Since the AGTL+ signal pins receive power from the FSB, these pins should not be driven (allowing the level to return to V_{CCP}) for minimum power drawn by the

termination resistors in this state. In addition, all other input pins on the FSB should be driven to the inactive state.

RESET# causes the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. When RESET# is asserted by the system, the STPCLK#, SLP#, DPSLP#, and DPRSTP# pins must be de-asserted prior to RESET# de-assertion. When re-entering the Stop-Grant state from the Sleep state, STPCLK# should be de-asserted after the de-assertion of SLP#.

While in Stop-Grant state, the processor will service snoops and latch interrupts delivered on the FSB. The processor will latch SMI#, INIT# and LINT [1:0] interrupts and will service only one of each upon return to the Normal state.

The PBE# signal may be driven when the processor is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt or Monitor event latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that the entire processor should return to the Normal state.

A transition to the Stop-Grant Snoop state occurs when the processor detects a snoop on the FSB (see Section 2.1.2.3). A transition to the Sleep state (see Section 2.1.2.4) occurs with the assertion of the SLP# signal.

2.1.2.3 Stop-Grant Snoop State

The processor responds to snoop or interrupt transactions on the FSB while in Stop-Grant state by entering the Stop-Grant Snoop state. The processor will stay in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB) or the interrupt has been latched. The processor returns to the Stop-Grant state once the snoop has been serviced or the interrupt has been latched.

2.1.2.4 Sleep State

The Sleep state is a low-power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and stops all internal clocks. The Sleep state is entered through assertion of the SLP# signal while in the Stop-Grant state. The SLP# pin should only be asserted when the processor is in the Stop-Grant state. SLP# assertion while the processor is not in the Stop-Grant state is out of specification and may result in unapproved operation.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP#, DPSLP#, or RESET#) are allowed on the FSB while the processor is in Sleep state. Snoop events that occur while in Sleep state or during a transition into or out of Sleep state will cause unpredictable behavior. Any transition on an input signal before the processor has returned to the Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant state. If RESET# is driven active while the processor is in the Sleep state, the SLP# and STPCLK# signals should be de-asserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering an even lower power state, the Deep Sleep state, by asserting the DPSLP# pin (see Section 2.1.2.5). While the processor is in the Sleep state, the SLP# pin must be de-asserted if another asynchronous FSB event needs to occur.

2.1.2.5 Deep Sleep State

The Deep Sleep state is entered through assertion of the DPSLP# pin while in the Sleep state. BCLK may be stopped during the Deep Sleep state for additional platform level power savings. BCLK stop/restart timings on appropriate chipset-based platforms with the CK505 clock chip are as follows:

- **Deep Sleep entry:** the system clock chip may stop/tri-state BCLK within 2 BCLKs of DPSLP# assertion. It is permissible to leave BCLK running during Deep Sleep.
- **Deep Sleep exit**: the system clock chip must start toggling BCLK within 10 BCLK periods within DPSLP# de-assertion.

To re-enter the Sleep state, the DPSLP# pin must be de-asserted. BCLK can be re-started after DPSLP# de-assertion as described above. A period of 15 microseconds (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep state. Once in the Sleep state, the SLP# pin must be de-asserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions of signals are allowed on the FSB while the processor is in Deep Sleep state. When the processor is in Deep Sleep state, it will not respond to interrupts or snoop transactions. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

2.1.2.6 Deeper Sleep State

The Deeper Sleep state is similar to the Deep Sleep state but further reduces core voltage levels. One of the potential lower core voltage levels is achieved by entering the base Deeper Sleep state. The Deeper Sleep state is entered through assertion of the DPRSTP# pin while in the Deep Sleep state. The following lower core voltage level is achieved by entering the Intel Enhanced Deeper Sleep state which is a sub-state of Deeper Sleep state. Intel Enhanced Deeper Sleep state is entered through assertion of the DPRSTP# pin while in the Deep Sleep only when the L2 cache has been completely shut down. Refer to Section 2.1.2.6.1 for further details on reducing the L2 cache and entering Intel Enhanced Deeper Sleep state.

In response to entering Deeper Sleep, the processor drives the VID code corresponding to the Deeper Sleep core voltage on the VID [6:0] pins.

Exit from Deeper Sleep or Intel Enhanced Deeper Sleep state is initiated by DPRSTP# de-assertion when the core requests a package state other than C4 or the core requests a processor performance state other than the lowest operating point.

2.1.2.6.1 Intel Enhanced Deeper Sleep State

Intel Enhanced Deeper Sleep state is a sub-state of Deeper Sleep that extends power saving capabilities by allowing the processor to further reduce core voltage once the

L2 cache has been reduced to zero ways and completely shut down. The following events occur when the processor enters Intel Enhanced Deeper Sleep state:

- The processor issues a P_LVL4 I/O read or an MWAIT(C4) instruction and then progressively reduces the L2 cache to zero.
- The processor drives the VID code corresponding to the Intel Enhanced Deeper Sleep state core voltage on the VID [6:0] pins.

2.2 Dynamic Cache Sizing

Dynamic Cache Sizing allows the processor to flush and disable a programmable number of L2 cache ways upon each Deeper Sleep entry under the following conditions:

- The C0 timer that tracks continuous residency in the Normal package state, has not expired. This timer is cleared during the first entry into Deeper Sleep to allow consecutive Deeper Sleep entries to shrink the L2 cache as needed.
- The FSB speed to processor core speed ratio is below the predefined L2 shrink threshold.

If the FSB speed to processor core speed ratio is above the predefined L2 shrink threshold, then L2 cache expansion will be requested. If the ratio is zero, then the ratio will not be taken into account for Dynamic Cache Sizing decisions.

Upon STPCLK# de-assertion, the core exiting Intel Enhanced Deeper Sleep state will expand the L2 cache to two ways and invalidate previously disabled cache ways. If the L2 cache reduction conditions stated above still exist when the core returns to C4 then package enters Intel Enhanced Deeper Sleep state, then the L2 will be shrunk to zero again. If the core requests a processor performance state resulting in a higher ratio than the predefined L2 shrink threshold, the C0 timer expires, then the whole L2 will be expanded upon the next interrupt event.

L2 cache shrink prevention may be enabled as needed on occasion through an MWAIT(C4) sub-state field. If shrink prevention is enabled, the processor does not enter Intel Enhanced Deeper Sleep state since the L2 cache remains valid and in full size.

2.3 Enhanced Intel SpeedStep® Technology

The processor features Enhanced Intel SpeedStep Technology. Following are the key features of Enhanced Intel SpeedStep Technology:

- Multiple voltage and frequency operating points provide optimal performance at the lowest power.
- Voltage and frequency selection is software controlled by writing to processor MSRs:
  - If the target frequency is higher than the current frequency, V_{CC} is ramped up in steps by placing new values on the VID pins and the PLL then locks to the new frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the new frequency and the V_{CC} is changed through the VID pin mechanism.
  - Software transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition completes.
- The processor controls voltage ramp rates internally to ensure glitch free transitions.
- Low transition latency and large number of transitions possible per second:
  - Processor core (including L2 cache) is unavailable for up to 10 µs during the frequency transition.
  - The bus protocol (BNR# mechanism) is used to block snooping.
- Improved Intel® Thermal Monitor mode:
  - When the on-die thermal sensor indicates that the die temperature is too high, the processor can automatically perform a transition to a lower frequency and voltage specified in a software programmable MSR.
  - The processor waits for a fixed time period. If the die temperature is down to acceptable levels, an up transition to the previous frequency and voltage point occurs.
  - An interrupt is generated for the up and down Intel Thermal Monitor transitions enabling better system level thermal management.
- Enhanced thermal management features:
  - Digital Thermal Sensor and Out of Specification detection
  - Intel Thermal Monitor-1 in addition to Intel Thermal Monitor-2 in case of unsuccessful Intel Thermal Monitor-2 transition.

2.4 Enhanced Low-Power States

Enhanced low-power states (C1E, C2E, C4E) optimize for power by forcibly reducing the performance state of the processor when it enters a package low-power state. Instead of directly transitioning into the package low-power state, the enhanced package low-power state first reduces the performance state of the processor by performing an Enhanced Intel SpeedStep Technology transition down to the lowest operating point. Upon receiving a break event from the package low-power state, control will be returned to software while an Enhanced Intel SpeedStep Technology transition up to the initial operating point occurs. The advantage of this feature is that it significantly reduces leakage while in the Stop-Grant and Deeper Sleep states.

Note: Long-term reliability cannot be assured unless all the Enhanced Low-Power States are enabled.

The processor implements two software interfaces for requesting enhanced package low-power states: MWAIT instruction extensions with sub-state hints and via BIOS by configuring a software programmable MSR bit to automatically promote package low-power states to enhanced package low-power states.

Enhanced Intel SpeedStep Technology transitions are multi-step processes that require clocked control. These transitions cannot occur when the processor is in the Sleep or Deep Sleep package low-power states since processor clocks are not active in these states. Enhanced Deeper Sleep is an exception to this rule when the Hard C4E configuration is enabled in a software programmable MSR bit. This Enhanced Deeper Sleep state configuration will lower core voltage to the Deeper Sleep level while in Deeper Sleep and, upon exit, will automatically transition to the lowest operating voltage and frequency to reduce snoop service latency. The transition to the lowest operating point or back to the original software requested point may not be instantaneous. Furthermore, upon very frequent transitions between active and idle states, the transitions may lag behind the idle state entry resulting in the processor either executing for a longer time at the lowest operating point or running idle at a high operating point. Observations and analyses show this behavior should not significantly impact total power savings or performance score while providing power benefits in most other cases.

2.5 FSB Low Power Enhancements

The processor incorporates FSB low power enhancements:

- BPRI# control for address and control input buffers
- Dynamic Bus Parking
- Dynamic On Die Termination disabling
- Low VCCP (I/O termination voltage)

The processor incorporates the DPWR# signal that controls the data bus input buffers on the processor. The DPWR# signal disables the buffers when not used and activates them only when data bus activity occurs, resulting in significant power savings with no performance impact. BPRI# control also allows the processor address and control input buffers to be turned off when the BPRI# signal is inactive. Dynamic Bus Parking allows a reciprocal power reduction in chipset address and control input buffers when the processor de-asserts its BR0# pin. The on-die termination on the processor FSB buffers is disabled when the signals are driven low, resulting in additional power savings. The low I/O termination voltage is on a dedicated voltage plane independent of the core voltage, enabling low I/O switching power at all times.

2.5.1 Front Side Bus

The processor has only one signaling mode, where the data and address buses and the strobe signals are operating in GTL mode. The reason to use GTL is to improve signal integrity.

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3 Electrical Specifications

3.1 Power and Ground Pins

For clean, on-chip power distribution, the processor will have a large number of VCC (power) and VSS (ground) inputs. All power pins must be connected to V_{CC} power planes while all VSS pins must be connected to system ground planes. Use of multiple power and ground planes is recommended to reduce I*R drop. The processor VCC pins must be supplied the voltage determined by the VID (Voltage ID) pins.

3.2 FSB Clock (BCLK [1:0]) and Processor Clocking

BCLK [1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous generation processors, the processor core frequency is a multiple of the BCLK [1:0] frequency. The processor uses a differential clocking implementation.

3.3 Voltage Identification

The processor uses seven voltage identification pins (VID [6:0]) to support automatic selection of power supply voltages. The VID pins for the processor are CMOS outputs driven by the processor VID circuitry. Table 3 specifies the voltage level corresponding to the state of VID [6:0]. A “1” in this refers to a high-voltage level and a “0” refers to low-voltage level.

Table 3. Voltage Identification Definition

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000

3.4 Catastrophic Thermal Protection

The processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. Even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough such that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of 125°C (maximum), or if the THERMTRIP# signal is asserted, the VCC supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway of the processor. THERMTRIP# functionality is not ensured if the PWRGOOD signal is not asserted.

3.5 Reserved and Unused Pins

All other RSVD signals can be left as No Connect. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Section 4.2 for a pin listing of the processor and the location of all RSVD pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active low AGTL+ inputs may be left as no connects if AGTL+ termination is provided on the processor silicon. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected.

3.6 FSB Frequency Select Signals (BSEL [2:0])

The BSEL [2:0] signals are used to select the frequency of the processor input clock (BCLK [1:0]). These signals should be connected to the clock chip and the appropriate chipset on the platform. The BSEL encoding for BCLK [1:0] is shown in Table 4.

Table 4. BSEL [2:0] Encoding for BCLK Frequency

BSEL [2]	BSEL [1]	BSEL [0]	BCLK Frequency
L	L	H	133 MHz

3.7 FSB Signal Groups

To simplify the following discussion, the FSB signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals which are dependent upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asynchronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 5 identifies which signals are common clock, source synchronous, and asynchronous.

Table 5. FSB Pin Groups

Signal Group	Type	Signals1
AGTL+ Common Clock Input	Synchronous to BCLK [1:0]	BPRI#, DEFER#, PREQ#4, RESET#, RS [2:0]#, TRDY#, DPWR#
AGTL+ Common Clock I/O	Synchronous to BCLK [1:0]	ADS#, BNR#, BPM [3:0]#, BR0#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, PRDY#
AGTL+ Source Synchronous I/O	Synchronous to assoc. strobe	**Signals** / **Associated Strobe**: REQ [4:0]#, A [16:3]# — ADSTB0# A [31:17]# — ADSTB1# D [15:0]# — DSTBP0#, DSTBN0# D [31:16]# — DSTBP1#, DSTBN1# D [47:32]# — DSTBP2#, DSTBN2# D [63:48]# — DSTBP3#, DSTBN3#
AGTL+ Strobes	Synchronous to BCLK [1:0]	ADSTB [1:0]#, DSTBP [3:0]#, DSTBN [3:0]#
CMOS Input	Asynchronous	DPRSTP#, DPSLP#, IGNNE#, INIT#, LINT0/INTR, LINT1/ NMI, PWRGOOD, SMI#, SLP#, STPCLK#
Open Drain Output	Asynchronous	FERR#, THERMTRIP#, IERR#
Open Drain I/O	Asynchronous	PROCHOT#3
CMOS Output	Asynchronous	VID [6:0], BSEL [2:0]
CMOS Input	Synchronous to TCK	TCK, TDI, TMS, TRST#

Signal Group	Type	Signals1
Open Drain Output	Synchronous to TCK	TDO
FSB Clock	Clock	BCLK [1:0]
Power/Other		COMP [3:0], HFPLL (old name is DBR#2), CMREF, GTLREF, TEST2/Dclk, TEST1/Aclk, THERMDA, THERMDC, VCC, VCCA, VCCP, VCC_SENSE, VSS, VSS_SENSE, VCCQ [1:0], VCCPC6

NOTES:

1. Refer to Chapter 4 for signal descriptions and termination requirements.
2. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
3. PROCHOT# signal type is open drain output and CMOS input.

3.8 CMOS Asynchronous Signals

CMOS input signals are shown in Table 5. Legacy output FERR#, IERR# and other non- AGTL+ signals (THERMTRIP# and PROCHOT#) use Open Drain output buffers. These signals do not have setup or hold time specifications in relation to BCLK [1:0]. However, all of the CMOS signals are required to be asserted for more than 5 BCLKs for the processor to recognize them. See Section 3.10 for the DC specifications for the CMOS signal groups.

3.9 Maximum Ratings

Table 6 specifies absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 6. Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes[1,5]
$T_{STORAGE}$	Processor Storage Temperature	-40	85	°C	2
$V_{CC, VCCP}$	Any Processor Supply Voltage with Respect to V_{SS}	-0.3	1.10	V	1
VinAGTL+	AGTL+ Buffer DC Input Voltage with Respect to V_{SS}	-0.1	1.10	V	1, 2
VinAsynch_CMOS	CMOS Buffer DC Input Voltage with Respect to V_{SS}	-0.1	1.10	V	1, 2

NOTES:
1. This rating applies to the processor and does not include any tray or packaging.
2. Contact Intel for storage requirements in excess of one year.

3.10 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise. See Chapter 4 for the pin signal definitions and signal pin assignments. Most of the signals on the FSB are in the AGTL+ signal group. The DC specifications for these signals are listed in Table 9. DC specifications for the CMOS group are listed in Table 10.

Table 9 through Table 11 list the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. The Highest Frequency Mode (HFM) and Lowest Frequency Mode (LFM) refer to the highest and lowest core operating frequencies supported on the processor. Active mode load line specifications apply in all states except in the Deep Sleep and Deeper Sleep states. $V_{CC,BOOT}$ is the default voltage driven by the voltage regulator at power up in order to set the VID values. Unless specified otherwise, all specifications for the processor are at T_J = 90°C.

Note: Care should be taken to read all notes associated with each parameter.

Table 7. Voltage and Current Specifications for the Processors

Symbol	Parameter		Min	Typ	Max	Unit	Notes[13]
FSB Frequency	BCLK Frequency		132.63	133.33	133.37	MHz	
V_{CC}HFM	V_{CC} at Highest Frequency Mode (HFM)		AVID	-	1.10	V	1, 2, 11
V_{CC}LFM	V_{CC} at Lowest Frequency Mode (LFM)		0.75	—	AVID	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up		—	1.20	—	V	2, 6
V_{CCP}	AGTL+ Termination Voltage		1.00	1.05	1.10	V	
V_{CCA}	PLL Supply voltage		1.425	1.5	1.575	V	
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep (C4)		0.75	—	1.0	V	1, 2
V_{CCF}	Fuse Power Supply		1.00	1.05	1.10	V	
I_{CCDES}	I_{CC} for Processors Recommended Design Target (Estimated)		—	—	4.0	A	
I_{CC}	I_{CC} for Processors		—	—	—	—	—
	Processor Number	Core Frequency/Voltage	—	—	—	—	—
	N270	1.6GHz / 1.10V	—	—	3	A	3, 4
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant HFM: 1.6 GHz @ 1.10 Volts LFM: 0.8 – 1.2 GHz @ 0.75 – 1.00 Volts		— —	— —	2.2 1.5	A	3, 4
I_{DSLP}	I_{CC} Deep Sleep HFM: 1.6 GHz @ 1.10 Volts LFM: 0.8 GHz @ 0.75 – 1.00 Volts		— —	— —	1.4 0.6	A	At 50°C 3, 4
I_{DPRSLP}	I_{CC} Deeper Sleep (C4)		—	—	0.2	A	At 50°C 3, 4
$dI_{CC/dt}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin (Estimated)		—	—	2.5	A/µs	5, 7
I_{CCA}	I_{CC} for V_{CCA} Supply		—	—	130	mA	
I_{CCP}	I_{CCP} before V_{CC} Stable		—	—	2.5	A	8
I_{CCP}	I_{CCP} after V_{CC} Stable		—	—	1.5	A	9

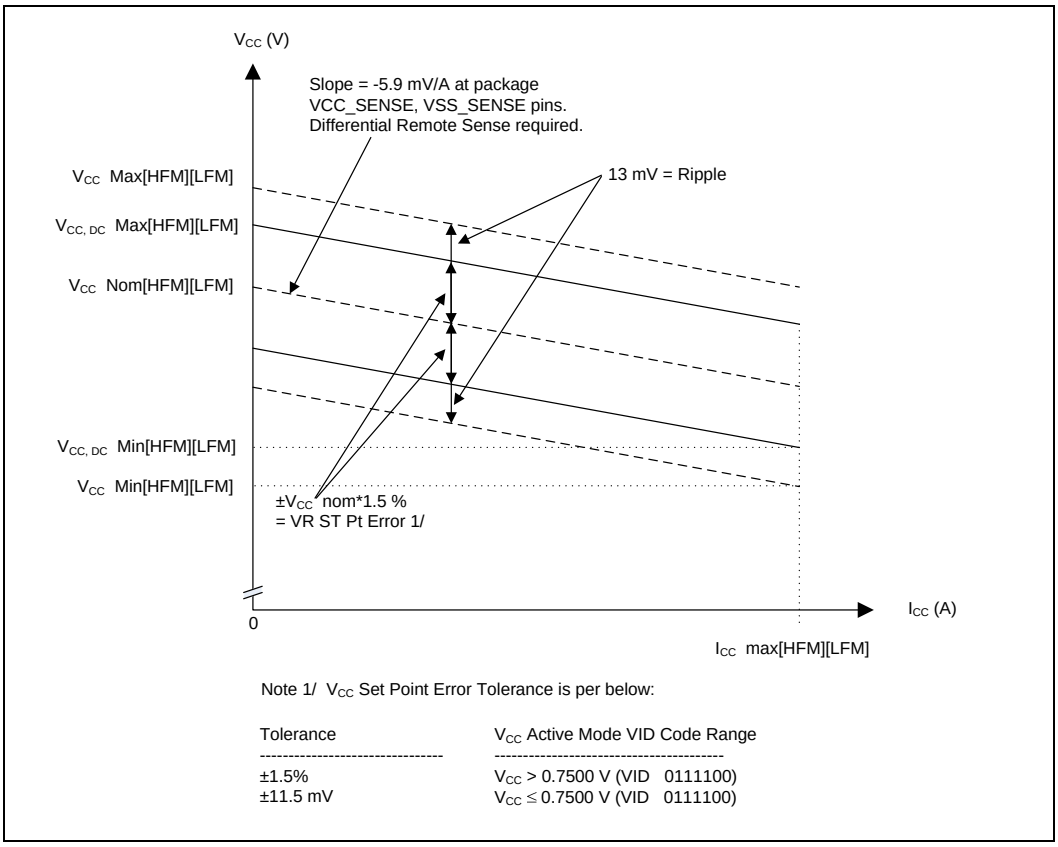
NOTES:

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and can not be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Thermal Monitor 2, Enhanced Intel SpeedStep technology, or Enhanced Halt State). Typical AVID range is 0.8 V to 0.85 V.
2. The voltage specifications are assumed to be measured across VCC_SENSE and VSS_SENSE pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum

impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.

3. Specified at 90°C T_J.
4. Specified at the nominal V_{CC}.
5. Measured at the bulk capacitors on the motherboard.
6. $V_{CC,BOOT}$ tolerance is shown in Figure 3 and Figure 4.
7. Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal V_{CC}. Not 100% tested.
8. This is a power-up peak current specification, which is applicable when V_{CCP} is high and V_{CC_CORE} is low.
9. This is a steady-state I_{CC} current specification, which is applicable when both V_{CCP} and V_{CC_CORE} are high.
10. The V_{CC} max supported by the process is 1.1 V but the parameter can change (burnin voltage is higher).
11. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.

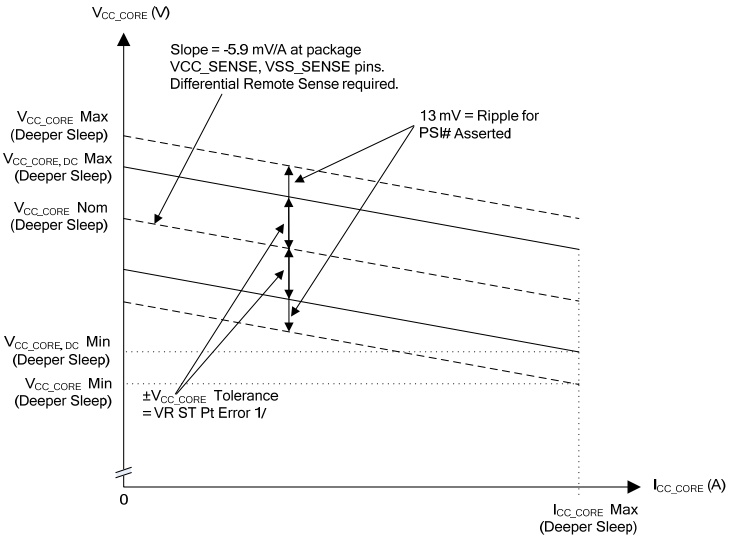
Figure 3. Active VCC and ICC Processor Loadline



Note 1/ V_{CC} Set Point Error Tolerance is per below:

Tolerance	V_{CC} Active Mode VID Code Range
±1.5%	V_{CC} > 0.7500 V (VID 0111100)
±11.5 mV	$V_{CC} \leq$ 0.7500 V (VID 0111100)

Figure 4. Deeper Sleep VCC and ICC Processor Loadline



Note 1/ Deeper Sleep VCC_CORE Set Point Error Tolerance is per below:

Tolerance – PSI# Ripple	V_{CC_CORE} VID Voltage Range
± [(VID*1.5%) – 3 mV]	V_{CC_CORE} > 0.7500 V
± (11.5 mV) – 3 mV]	0.7500 V ≤ V_{CC_CORE} ≤ 0.5000 V
± (25 mV) – 3 mV]	0.5000 V < V_{CC_CORE} ≤ 0.4125 V

Table 8. FSB Differential BCLK Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes[1]
V_{IH}	Input High Voltage	—	—	1.15	V		7, 8
V_{OH}	Input Low Voltage	—	—	-0.3	V		7, 8
V_{CROSS}	Crossing Voltage	0.3	—	0.55	V		2, 7, 9
ΔV_{CROSS}	Range of Crossing Points	—	—	140	mV		2, 7, 5
V_{SWING}	Differential Output Swing	300	—	—	mV		6
I_{LI}	Input Leakage Current	-5	—	+5	µA		3
Cpad	Pad Capacitance	1.2	1.45	2.0	pF		4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as absolute voltage where rising edge of BCLK0 is equal to the falling edge of BCLK1.
3. For Vin between 0 V and V_{IH}.
4. Cpad includes die capacitance only. No package parasitics are included.
5. ΔV_{CROSS} is defined as the total variation of all crossing voltages as defined in note 2.
6. Measurement taken from differential waveform.
7. Measurement taken from single-ended waveform.
8. “Steady state” voltage, not including Overshoots or Undershoots.
9. Only applies to the differential rising edge (BCLK0 rising and BCLK1 falling).

Table 9. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CCP}	I/O Voltage	1.00	1.05	1.10	V	
GTLREF	GTL Reference Voltage	—	2/3 V_{CCP}	—	V	6
R_{COMP}	Compensation Resistor	27.23	27.5	27.78	Ω	10
R_{ODT}	Termination Resistor	—	55	—	Ω	11
V_{IH}	Input High Voltage	GTLREF+0.10	V_{CCP}	V_{CCP}+0.10	V	3,6
V_{IL}	Input Low Voltage	-0.10	0	GTLREF–0.10	V	2,4
V_{OH}	Output High Voltage	V_{CCP}–0.10	V_{CCP}	V_{CCP}	V	6
R_{TT}	Termination Resistance	46 [SS] 46 [CC]	55	61 [SS] 64 [CC]	Ω	7, 12
R_{ON} (GTL mode)	GTL Buffer on Resistance	21	25	29	Ω	5
I_{LI}	Input Leakage Current	—	—	±100	µA	8
Cpad	Pad Capacitance	1.8	2.1	2.75	pF	9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{CCP}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull-down driver resistance.
6. GTLREF should be generated from VCCP with a 1% tolerance resistor divider.
7. RTT is the on-die termination resistance measured at VOL of the AGTL+ output driver.
8. Specified with on-die RTT and RON are turned off.
9. Cpad includes die capacitance only. No package parasitics are included.
10. There are external resistor on the comp0 and comp2 pins.
11. On-die termination resistance, measured at 0.33*V_{CCP}.
12. SS: source synchronous pins such as quad-pumped data bus and double-pumped address bus which require a clock strobe. CC: Common clock pins.

Table 10. Legacy CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CCP}	I/O Voltage	1.00	1.05	1.10	V	
V_{IH}	Input High Voltage	0.7*V_{CCP}	V_{CCP}	VCCP+0.1	V	2
V_{IL}	Input Low Voltage CMOS	-0.10	0.00	0.3*V_{CCP}	V	2, 3
V_{OH}	Output High Voltage	0.9*V_{CCP}	V_{CCP}	V_{CCP}+0.1	V	2
V_{OL}	Output Low Voltage	-0.10	0	0.1*V_{CCP}	V	2
I_{OH}	Output High Current	1.5	—	4.1	mA	5
I_{OL}	Output Low Current	1.5	—	4.1	mA	4
I_{LI}	Input Leakage Current	—	—	± 100	µA	6
Cpad1	Pad Capacitance	1.6	2.1	2.55	pF	7
Cpad2	Pad Capacitance for CMOS Input	0.95	1.2	1.45		8

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{CCP} referred to in these specifications refers to instantaneous V_{CCP}.
3. Reserved.
4. Measured at 0.1*V_{CCP}.
5. Measured at 0.9*V_{CCP}.
6. For Vin between 0V and V_{CCP}. Measured when the driver is tri-stated.
7. Cpad1 includes die capacitance only for DPRSTP#, DPSLP#, PWRGOOD. No package parasitics are included.
8. Cpad2 includes die capacitance for all other CMOS input signals. No package parasitics are included.

Table 11. Open Drain Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{OH}	Output High Voltage	V_{CCP}–5%	V_{CCP}	V_{CCP}+5%	V	3
V_{OL}	Output Low Voltage	0	—	0.20	V	
I_{OL}	Output Low Current	16	—	50	mA	2
I_{LO}	Output Leakage Current	—	—	±200	µA	4
Cpad	Pad Capacitance	1.9	2.2	2.45	pF	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Measured at 0.2 V_{CCP}.
3. V_{OH} is determined by value of the external pull-up resistor to V_{CCP}.
4. For Vin between 0 V and V_{OH}.
5. Cpad includes die capacitance only. No package parasitics are included.

§

4 Package Mechanical Specifications and Pin Information

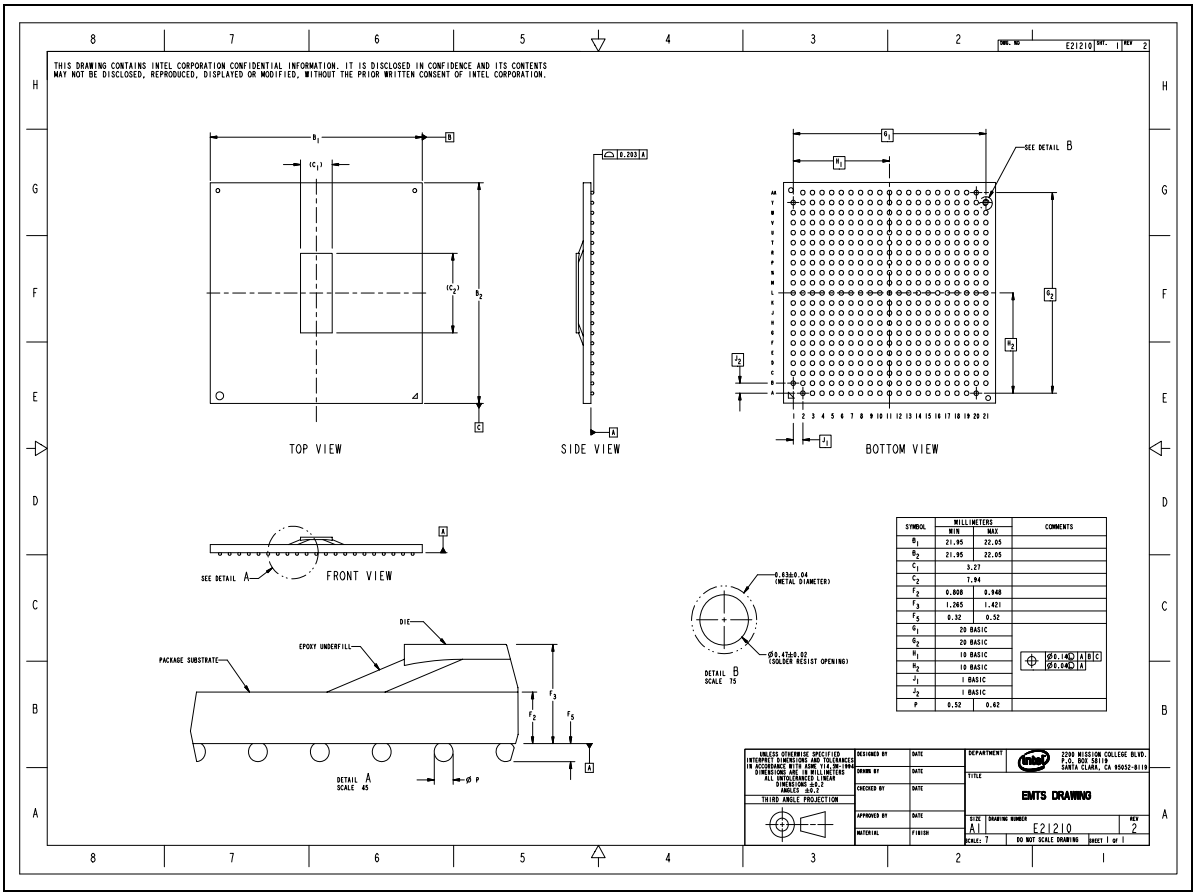
This chapter provides the package specifications, pin-out assignments, and signal description.

4.1 Package Mechanical Specifications

The processor is available in 512 KB, 437 pins in FCBGA8 package. The package dimensions are shown in Figure .

4.1.1 Package Mechanical Drawings

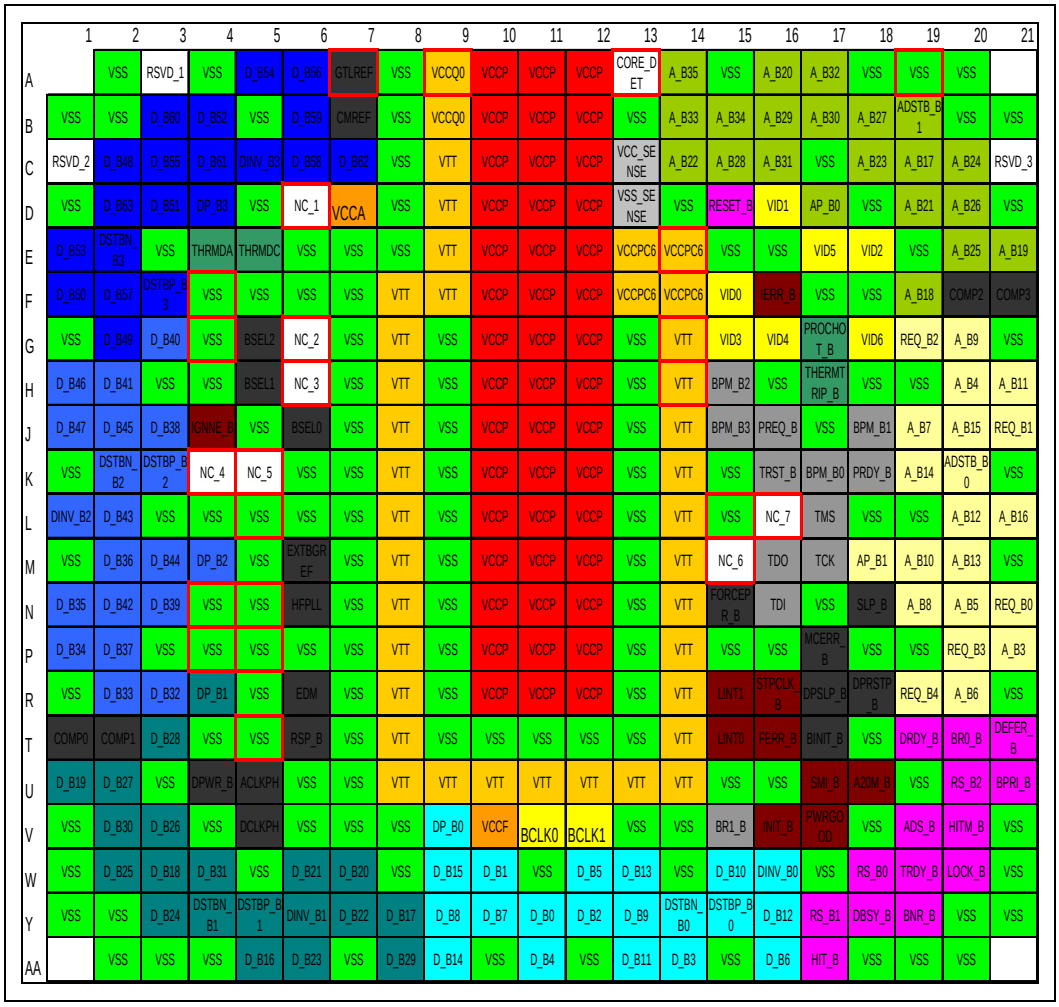
Figure 5. Package Mechanical Drawing



4.2 Processor Pin-out Assignment

Figure are graphic representations of the processor pin-out assignments. Table 12 lists the pin-out by signal name.

Figure 6. Pin-out Diagram (Top View, Left Side)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
A		VSS	RSVD_1	VSS	D_B54	D_B56	GTLREF	VSS	VCCQ0	VCCP	VCCP	VCCP	CORE_DET	A_B35	VSS	A_B20	A_B32	VSS	VSS	VSS	
B	VSS	VSS	D_B60	D_B52	VSS	D_B59	CMREF	VSS	VCCQ0	VCCP	VCCP	VCCP	VSS	A_B33	A_B34	A_B29	A_B30	A_B27	ADSTB_B1	VSS	VSS
C	RSVD_2	D_B48	D_B55	D_B61	DINV_B3	D_B58	D_B62	VSS	VTT	VCCP	VCCP	VCCP	VCC_SENSE	A_B22	A_B28	A_B31	VSS	A_B23	A_B17	A_B24	RSVD_3
D	VSS	D_B63	D_B51	DP_B3	VSS	NC_1	VCCA	VSS	VTT	VCCP	VCCP	VCCP	VSS_SENSE	VSS	RESET_B	VID1	AP_B0	VSS	A_B21	A_B26	VSS
E	D_B53	DSTBN_B3	VSS	THRMDA	THRMDC	VSS	VSS	VSS	VTT	VCCP	VCCP	VCCP	VCCPC6	VCCPC6	VSS	VSS	VID5	VID2	VSS	A_B25	A_B19
F	D_B50	D_B57	DSTBP_B3	VSS	VSS	VSS	VSS	VTT	VTT	VCCP	VCCP	VCCP	VCCPC6	VCCPC6	VID0	IERR_B	VSS	VSS	A_B18	COMP2	COMP3
G	VSS	D_B49	D_B40	VSS	BSEL2	NC_2	VSS	VTT	VSS	VCCP	VCCP	VCCP	VSS	VTT	VID3	VID4	PROCHOT_B	VID6	REQ_B2	A_B9	VSS
H	D_B46	D_B41	VSS	VSS	BSEL1	NC_3	VSS	VTT	VSS	VCCP	VCCP	VCCP	VSS	VTT	BPM_B2	VSS	THERMTRIP_B	VSS	VSS	A_B4	A_B11
J	D_B47	D_B45	D_B38	IGNNE_B	VSS	BSEL0	VSS	VTT	VSS	VCCP	VCCP	VCCP	VSS	VTT	BPM_B3	PREQ_B	VSS	BPM_B1	A_B7	A_B15	REQ_B1
K	VSS	DSTBN_B2	DSTBP_B2	NC_4	NC_5	VSS	VSS	VTT	VSS	VCCP	VCCP	VCCP	VSS	VTT	VSS	TRST_B	BPM_B0	PRDY_B	A_B14	ADSTB_B0	VSS
L	DINV_B2	D_B43	VSS	VSS	VSS	VSS	VSS	VTT	VSS	VCCP	VCCP	VCCP	VSS	VTT	VSS	NC_7	TMS	VSS	VSS	A_B12	A_B16
M	VSS	D_B36	D_B44	DP_B2	VSS	EXTBGREF	VSS	VTT	VSS	VCCP	VCCP	VCCP	VSS	VTT	NC_6	TDO	TCK	AP_B1	A_B10	A_B13	VSS
N	D_B35	D_B42	D_B39	VSS	VSS	HFPLL	VSS	VTT	VSS	VCCP	VCCP	VCCP	VSS	VTT	FORCEPR_B	TDI	VSS	SLP_B	A_B8	A_B5	REQ_B0
P	D_B34	D_B37	VSS	VSS	VSS	VSS	VSS	VTT	VSS	VCCP	VCCP	VCCP	VSS	VTT	VSS	VSS	MCERR_B	VSS	VSS	REQ_B3	A_B3
R	VSS	D_B33	D_B32	DP_B1	VSS	EDM	VSS	VTT	VSS	VCCP	VCCP	VCCP	VSS	VTT	LINT1	STPCLK_B	DPSLP_B	DPRSTP_B	REQ_B4	A_B6	VSS
T	COMP0	COMP1	D_B28	VSS	VSS	RSP_B	VSS	VTT	VSS	VSS	VSS	VSS	VSS	VTT	LINT0	FERR_B	BINIT_B	VSS	DRDY_B	BR0_B	DEFER_B
U	D_B19	D_B27	VSS	DPWR_B	ACLKPH	VSS	VSS	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VSS	VSS	SMI_B	A20M_B	VSS	RS_B2	BPRI_B
V	VSS	D_B30	D_B26	VSS	DCLKPH	VSS	VSS	VSS	DP_B0	VCCF	BCLK0	BCLK1	VSS	VSS	BR1_B	INIT_B	PWRGOOD	VSS	ADS_B	HITM_B	VSS
W	VSS	D_B25	D_B18	D_B31	VSS	D_B21	D_B20	VSS	D_B15	D_B1	VSS	D_B5	D_B13	VSS	D_B10	DINV_B0	VSS	RS_B0	TRDY_B	LOCK_B	VSS
Y	VSS	VSS	D_B24	DSTBN_B1	DSTBP_B1	DINV_B1	D_B22	D_B17	D_B8	D_B7	D_B0	D_B2	D_B9	DSTBN_B0	DSTBP_B0	D_B12	RS_B1	DBSY_B	BNR_B	VSS	VSS
AA		VSS	VSS	VSS	D_B16	D_B23	VSS	D_B29	D_B14	VSS	D_B4	VSS	D_B11	D_B3	VSS	D_B6	HIT_B	VSS	VSS	VSS	

Table 12. Pin-out Arranged by Signal Name

Signal Name	Ball #
A [10]#	M19
A [11]#	H21
A [12]#	L20
A [13]#	M20
A [14]#	K19
A [15]#	J20
A [16]#	L21
A [17]#	C19
A [18]#	F19
A [19]#	E21
A [20]#	A16
A [21]#	D19
A [22]#	C14
A [23]#	C18
A [24]#	C20
A [25]#	E20
A [26]#	D20
A [27]#	B18
A [28]#	C15
A [29]#	B16
A [3]#	P21
A [30]#	B17
A [31]#	C16
A [32]#	A17
A [33]#	B14
A [34]#	B15
A [35]#	A14
A [4]#	H20
A [5]#	N20
A [6]#	R20

Signal Name	Ball #
A [7]#	J19
A [8]#	N19
A [9]#	G20
A20M#	U18
ACLKPH	U5
ADS#	V19
ADSTB [0]#	K20
ADSTB [1]#	B19
BCLK [0]	V11
BCLK [1]	V12
BNR#	Y19
BPM [0]#	K17
BPM [1]#	J18
BPM [2]#	H15
BPM [3]#	J15
BPRI#	U21
BR0#	T20
BR1#	V15
BSEL [0]	J6
BSEL [1]	H5
BSEL [2]	G5
COMP [0]	T1
COMP [1]	T2
COMP [2]	F20
COMP [3]	F21
D [0]#	Y11
D [1]#	W10
D [10]#	W15
D [11]#	AA13
D [12]#	Y16

Signal Name	Ball #
D [13]#	W13
D [14]#	AA9
D [15]#	W9
D [16]#	AA5
D [17]#	Y8
D [18]#	W3
D [19]#	U1
D [2]#	Y12
D [20]#	W7
D [21]#	W6
D [22]#	Y7
D [23]#	AA6
D [24]#	Y3
D [25]#	W2
D [26]#	V3
D [27]#	U2
D [28]#	T3
D [29]#	AA8
D [3]#	AA14
D [30]#	V2
D [31]#	W4
D [32]#	R3
D [33]#	R2
D [34]#	P1
D [35]#	N1
D [36]#	M2
D [37]#	P2
D [38]#	J3
D [39]#	N3
D [4]#	AA11

Signal Name	Ball #
D [40]#	G3
D [41]#	H2
D [42]#	N2
D [43]#	L2
D [44]#	M3
D [45]#	J2
D [46]#	H1
D [47]#	J1
D [48]#	C2
D [49]#	G2
D [5]#	W12
D [50]#	F1
D [51]#	D3
D [52]#	B4
D [53]#	E1
D [54]#	A5
D [55]#	C3
D [56]#	A6
D [57]#	F2
D [58]#	C6
D [59]#	B6
D [6]#	AA16
D [60]#	B3
D [61]#	C4
D [62]#	C7
D [63]#	D2
D [7]#	Y10
D [8]#	Y9
D [9]#	Y13
DBSY#	Y18
DCLKPH	V5

Signal Name	Ball #
DEFER#	T21
DINV [0]#	W16
DINV [1]#	Y6
DINV [2]#	L1
DINV [3]#	C5
DPRSTP#	R18
DPWR#	U4
DRDY#	T19
DSTBN [0]#	Y14
DSTBN [1]#	Y4
DSTBN [2]#	K2
DSTBN [3]#	E2
DSTBP [0]#	Y15
DSTBP [1]#	Y5
DSTBP [2]#	K3
DSTBP [3]#	F3
FERR#	T16
FORCEPR#	N15
GTLREF	A7
HIT#	AA17
HITM#	V20
IERR#	F16
IGNNE#	J4
INIT#	V16
LINT0	T15
LINT1	R15
LOCK#	W20
MCERR#	P17
NC	D6
NC	G6
NC	H6

Signal Name	Ball #
NC	K4
NC	K5
NC	M15
NC	L16
PRDY#	K18
PREQ#	J16
PROCHOT#	G17
PWRGOOD	V17
REQ [0]#	N21
REQ [1]#	J21
REQ [2]#	G19
REQ [3]#	P20
REQ [4]#	R19
RESET#	D15
RS [0]#	W18
RS [1]#	Y17
RS [2]#	U20
AP#0	D17
DPSLP#	R17
AP#1	M18
BNT#	T17
CMREF	B7
CORE_DET	A13
EDM	R6
HPPLL	N6
RSP#	T6
RSVD	A3
RSVD	C1
RSVD	C21
VCCPC61	E13
VCCPC62	E14

Signal Name	Ball #
VCCPC63	F13
VCCPC64	F14
SLP#	N18
SMI#	U17
STPCLK#	R16
TCK	M17
TDI	N16
TDO	M16
EXTREF	M6
THERMTRIP#	H17
THRMDA	E4
THRMDC	E5
TMS	L17
TRDY#	W19
TRST#	K16
VCC	A10
VCC	A11
VCC	A12
VCC	B10
VCC	B11
VCC	B12
VCC	C10
VCC	C11
VCC	C12
VCC	D10
VCC	D11
VCC	D12
VCC	E10
VCC	E11
VCC	E12
VCC	F10

Signal Name	Ball #
VCC	F11
VCC	F12
VCC	G10
VCC	G11
VCC	G12
VCC	H10
VCC	H11
VCC	H12
VCC	J10
VCC	J11
VCC	J12
VCC	K10
VCC	K11
VCC	K12
VCC	L10
VCC	L11
VCC	L12
VCC	M10
VCC	M11
VCC	M12
VCC	N10
VCC	N11
VCC	N12
VCC	P10
VCC	P11
VCC	P12
VCC	R10
VCC	R11
VCC	R12
VCCA	D7
VCCF	V10

Signal Name	Ball #
VCCQ0	A9
VCCQ0	B9
VCCSENSE	C13
VID [0]	F15
VID [1]	D16
VID [2]	E18
VID [3]	G15
VID [4]	G16
VID [5]	E17
VID [6]	G18
VSS	A2
VSS	A4
VSS	A8
VSS	A15
VSS	A18
VSS	A19
VSS	A20
VSS	B1
VSS	B2
VSS	B5
VSS	B8
VSS	B13
VSS	B20
VSS	B21
VSS	C8
VSS	C17
VSS	D1
VSS	D5
VSS	D8
VSS	D14
VSS	D18

Signal Name	Ball #
VSS	D21
VSS	E3
VSS	E6
VSS	E7
VSS	E8
VSS	E15
VSS	E16
VSS	E19
VSS	F4
VSS	F5
VSS	F6
VSS	F7
VSS	F17
VSS	F18
VSS	G1
VSS	G4
VSS	G7
VSS	G9
VSS	G13
VSS	G21
VSS	H3
VSS	H4
VSS	H7
VSS	H9
VSS	H13
VSS	H16
VSS	H18
VSS	H19
VSS	J5
VSS	J7
VSS	J9

Signal Name	Ball #
VSS	J13
VSS	J17
VSS	K1
VSS	K6
VSS	K7
VSS	K9
VSS	K13
VSS	K15
VSS	K21
VSS	L3
VSS	L4
VSS	L5
VSS	L6
VSS	L7
VSS	L9
VSS	L13
VSS	L15
VSS	L18
VSS	L19
VSS	M1
VSS	M5
VSS	M7
VSS	M9
VSS	M13
VSS	M21
VSS	N4
VSS	N5
VSS	N7
VSS	N9
VSS	N13
VSS	N17

Signal Name	Ball #
VSS	P3
VSS	P4
VSS	P5
VSS	P6
VSS	P7
VSS	P9
VSS	P13
VSS	P15
VSS	P16
VSS	P18
VSS	P19
VSS	R1
VSS	R5
VSS	R7
VSS	R9
VSS	R13
VSS	R21
VSS	T4
VSS	T5
VSS	T7
VSS	T9
VSS	T10
VSS	T11
VSS	T12
VSS	T13
VSS	T18
VSS	U3
VSS	U6
VSS	U7
VSS	U15
VSS	U16

Signal Name	Ball #
VSS	U19
VSS	V1
VSS	V4
VSS	V6
VSS	V7
VSS	V8
VSS	V13
VSS	V14
VSS	V18
VSS	V21
VSS	W1
VSS	W5
VSS	W8
VSS	W11
VSS	W14
VSS	W17
VSS	W21
VSS	Y1
VSS	Y2
VSS	Y20
VSS	Y21
VSS	AA2
VSS	AA3

Signal Name	Ball #
VSS	AA4
VSS	AA7
VSS	AA10
VSS	AA12
VSS	AA15
VSS	AA18
VSS	AA19
VSS	AA20
VSSSENSE	D13
VTT	C9
VTT	D9
VTT	E9
VTT	F8
VTT	F9
VTT	G8
VTT	G14
VTT	H8
VTT	H14
VTT	J8
VTT	J14
VTT	K8
VTT	K14
VTT	L8

Signal Name	Ball #
VTT	L14
VTT	M8
VTT	M14
VTT	N8
VTT	N14
VTT	P8
VTT	P14
VTT	R8
VTT	R14
VTT	T8
VTT	T14
VTT	U8
VTT	U9
VTT	U10
VTT	U11
VTT	U12
VTT	U13
VTT	U14
DP#0	V9
DP#1	R4
DP#2	M4
DP#3	D4

4.3 Signal Description

Table 13. Signal Description

Signal Name	Type	Description
A [31:3]#	I/O	A [31:3]# (Address) defines a 2^{32}-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the processor FSB. A [31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB [1:0]#. Address signals are used as straps which are sampled before RESET# is de-asserted.
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an input/output write instruction, it must be valid along with the TRDY# assertion of the corresponding input/output Write bus transaction.
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A [31:3]# and REQ [4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal loop, or deferred reply ID match operations associated with the new transaction.
ADSTB [1:0]#	I/O	Address strobes are used to latch A [31:3]# and REQ [4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** — **Associated Strobe** REQ [4:0]#, A [16:3]# — ADSTB [0]# A [31:17]# — ADSTB [1]#
BCLK [1:0]	I	The differential pair BCLK (Bus Clock) determines the FSB frequency. All FSB agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing VCROSS.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

<table>
<tr><th>Signal Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BPM [0]#</td><td>O</td><td rowspan="4">BPM [3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM [3:0]# should connect the appropriate pins of all FSB agents. This includes debug or performance monitoring tools.</td></tr>
<tr><td>BPM [1]#</td><td>I/O</td></tr>
<tr><td>BPM [2]#</td><td>O</td></tr>
<tr><td>BPM [3]#</td><td>I/O</td></tr>
<tr><td>BPRI#</td><td>I</td><td>BPRI# (Bus Priority Request) is used to arbitrate for ownership of the FSB. It must connect the appropriate pins of both FSB agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed then releases the bus by de-asserting BPRI#.</td></tr>
<tr><td>BR0#</td><td>I/O</td><td>BR0# is used by the processor to request the bus. The arbitration is done between the processor (Symmetric Agent) and Intel 945GSE (High Priority Agent).</td></tr>
<tr><td>BSEL [2:0]</td><td>O</td><td>BSEL [2:0] (Bus Select) are used to select the processor input clock frequency. Table 4 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. For Intel® Atom™ processor N270, the BSEL is fixed to operat at 133-MHz BCLK frequency.</td></tr>
<tr><td>COMP [3:0]</td><td>PWR</td><td>COMP [3:0] must be terminated on the system board using precision (1% tolerance) resistors.</td></tr>
<tr><td>D [63:0]#</td><td>I/O</td><td>D [63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the FSB agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer.

D [63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D [63:0]# are latched off the falling edge of both DSTBP [3:0]# and DSTBN [3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#.
<table>
<tr><th>Quad-Pumped Signal Groups Data Group</th><th>DSTBN#/DSTBP#</th><th>DINV#</th></tr>
<tr><td>D [15:0]#</td><td>0</td><td>0</td></tr>
<tr><td>D [31:16]#</td><td>1</td><td>1</td></tr>
<tr><td>D [47:32]#</td><td>2</td><td>2</td></tr>
<tr><td>D [63:48]#</td><td>3</td><td>3</td></tr>
</table>
Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.</td></tr>
</table>

<table>
<tr><th>Signal Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DBSY#</td><td>I/O</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the FSB to indicate that the data bus is in use. The data bus is released after DBSY# is de-asserted. This signal must connect the appropriate pins on both FSB agents.</td></tr>
<tr><td>DEFER#</td><td>I</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both FSB agents.</td></tr>
<tr><td>DINV [3:0]#</td><td>I</td><td>DINV [3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D [63:0]# signals. The DINV [3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. DINV [3:0]# assignment to data bus signals is shown below.
<table>
<tr><th>Bus Signal</th><th>Data Bus Signals</th></tr>
<tr><td>DINV [3]#</td><td>D [63:48]#</td></tr>
<tr><td>DINV [2]#</td><td>D [47:32]#</td></tr>
<tr><td>DINV [1]#</td><td>D [31:16]#</td></tr>
<tr><td>DINV [0]#</td><td>D [15:0]#</td></tr>
</table>
</td></tr>
<tr><td>DPRSTP#</td><td>I</td><td>DPRSTP# when asserted on the platform causes the processor to transition from the Deep Sleep State to the Deeper Sleep state. In order to return to the Deep Sleep State, DPRSTP# must be de-asserted. DPRSTP# is driven by the South Bridge chipset.</td></tr>
<tr><td>DPSLP#</td><td>I</td><td>DPSLP# when asserted on the platform causes the processor to transition from the Sleep State to the Deep Sleep state. In order to return to the Sleep State, DPSLP# must be de-asserted. DPSLP# is driven by the South Bridge chipset.</td></tr>
<tr><td>DPWR#</td><td>I</td><td>DPWR# is a control signal from the Intel 945GSE chipset used to reduce power on the processor data bus input buffers.</td></tr>
<tr><td>DRDY#</td><td>I/O</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be de-asserted to insert idle clocks. This signal must connect the appropriate pins of both FSB agents.</td></tr>
<tr><td>DSTBN [3:0]#</td><td>I/O</td><td>Data strobe used to latch in D [63:0]#
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D [15:0]#</td><td>DINV [0]#, DSTBN [0]#</td></tr>
<tr><td>D [31:16]#</td><td>DINV [1]#, DSTBN [1]#</td></tr>
<tr><td>D [47:32]#</td><td>DINV [2]#, DSTBN [2]#</td></tr>
<tr><td>D [63:48]#</td><td>DINV [3]#, DSTBN [3]#</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Signal Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DSTBP [3:0]#</td><td>I/O</td><td>Data strobe used to latch in D [63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D [15:0]#</td><td>DINV [0]#, DSTBP [0]#</td></tr>
<tr><td>D [31:16]#</td><td>DINV [1]#, DSTBP [1]#</td></tr>
<tr><td>D [47:32]#</td><td>DINV [2]#, DSTBP [2]#</td></tr>
<tr><td>D [63:48]#</td><td>DINV [3]#, DSTBP [3]#</td></tr>
</table></td></tr>
<tr><td>FERR#/PBE#</td><td>O</td><td>FERR# (Floating-point Error)PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified with STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MSDOS*- type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is de-asserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event.

For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volume 3 of the Intel® 64 and IA-32 Architectures Software Developer's Manuals and the Intel® Processor Identification and CPUID Instruction Application Note.

For termination requirements please contact your Intel representative.</td></tr>
<tr><td>CMREF</td><td>PWR</td><td>CMREF determines the signal reference level for CMOS input pins. CMREF should be set at 1/2 V_{CCP}. CMREF is used by the CMOS receivers to determine if a signal is a logical-0 or logical-1.

NOTE: Because of not using CMOS, CMREF and GTLREF should be provided with 2/3 V_{CCP}.</td></tr>
<tr><td>GTLREF</td><td>PWR</td><td>GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical-0 or logical-1.</td></tr>
<tr><td>HIT#
HITM#</td><td>I/O</td><td>HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.</td></tr>
</table>

Signal Name	Type	Description
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is de-asserted, the processor generates an exception on a non-control floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register-0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both FSB agents. If INIT# is sampled active on the active to inactive transition of RESET#, the processor reverses its FSB data and address signals internally to ease motherboard layout for systems where the chipset is on the other side of the motherboard. D [63:0] => D [0:63] A [31:3] => A [3:31] DINV [3:0]# is also reversed.
LINT [1:0]	I	LINT [1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT [1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT [1:0] is the default configuration.

Signal Name	Type	Description
LOCK#	I/O	Lock# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the FSB, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the FSB throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	O	Probe Ready signal used by debug tools to request debug operation of the processor. Please contact your Intel representative for more implementation details.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor. Please contact your Intel representative for more implementation details.
PROCHOT#	I/O, O (DP)	As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system de-asserts PROCHOT#. This signal may require voltage translation on the motherboard. Please contact your Intel representative for more implementation details.
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. ‘Clean’ implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification, and be followed by a 2-ms (minimum) RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. For termination requirements, please contact your Intel representative for more implementation details.
REQ [4:0]#	I/O	REQ [4:0]# (Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB [0] #.

Signal Name	Type	Description
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, both FSB agents will de-assert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is de-asserted. Please contact your Intel representative for more implementation details.
RS [2:0]#	I	RS [2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both FSB agents.
RSVD	Reserved	All other RSVD signals can be left as No Connects.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, de-assertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is de-asserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the de-assertion of RESET# the processor will tri-state its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is de-asserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port). Please contact your Intel representative for more implementation details.
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support. Please contact your Intel representative for more implementation details.

Signal Name	Type	Description
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support. Please contact your Intel representative for more implementation details.
TEST[1:4]		Refer to the appropriate platform design guide for further TEST1, TEST2, TEST3, and TEST4 termination requirements and implementation details. All TEST signals can be left as No Connects.
THRMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This condition is signaled to the system by the THERMTRIP# (Thermal Trip) pin. For termination requirements, please contact your Intel representative for more implementation details.
THRMDA	PWR	Thermal Diode - Anode
THRMDC	PWR	Thermal Diode - Cathode
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools. Please contact your Intel representative for more implementation details.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. Please contact your Intel representative for more implementation details.
VCCA	PWR	VCCA provides isolated power for the internal processor core PLLs. Please contact your Intel representative for more implementation details.
VCC	PWR	Processor core power supply
VSS	GND	Processor core ground node.
VSS / NCTF	GND	Non Critical to Function
VID [6:0]	O	VID [6:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (V_{CC}). Unlike some previous generations of processors, these are CMOS signals that are driven by the processor. The voltage supply for these pins must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See Table 3 for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself.
VCCP	PWR	Processor I/O Power Supply

Signal Name	Type	Description
VCC_SENSE	O	VCCSENSE is an isolated low impedance connection to processor core power (V_{CC}). It can be used to sense or measure power near the silicon with little noise. Please contact your Intel representative for more implementation details.
VSS_SENSE	O	VSS_SENSE is an isolated low impedance connection to processor core V_{SS}. It can be used to sense or measure ground near the silicon with little noise. Please contact your Intel representative for more implementation details.

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5 Thermal Specifications and Design Considerations

The processor requires a thermal solution to maintain temperatures within operating limits. A complete thermal solution includes both component and system level thermal management features.

The system/processor thermal solution should be designed such that the processor remains within the minimum and maximum junction temperature (T_J) specifications at the corresponding thermal design power (TDP) value listed in Table 14 through Table 16. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system.

Attempts to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system.

Table 14. Power Specifications for the Processor

Symbol	Processor Number	Core Frequency and Voltage	Thermal Design Power			Unit	Notes
TDP	N270	1.6 GHz HFM V_{CC}	2.5W			W	At 90°C 1, 4
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
PAH, PSGNT	Auto Halt, Stop Grant Power at HFM V_{CC} at LFM V_{CC}		—	—	 1.0 0.7	 W W	At 70°C 2
PDSLP	Deep Sleep Power		—	—	0.5	W	At 50°C 2, 5
PDPRSLP	Deeper Sleep Power		—	—	0.5	W	At 50°C 2, 5
TJ	Junction Temperature		0	—	90	°C	3, 4

NOTES:

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section **Error! Reference source not found.** for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Deep Sleep state is mapped to Deeper Sleep State.

The processor incorporates three methods of monitoring die temperature: the Digital Thermal Sensor, Intel Thermal Monitor, and the Thermal Diode. The Intel Thermal Monitor (detailed in Section 5.2) must be used to determine when the maximum specified processor junction temperature has been reached.

5.1 Thermal Diode

The processor incorporates an on-die PNP transistor whose base emitter junction is used as a thermal “diode”, with its collector shorted to ground. The thermal diode can be read by an off-die analog/digital converter (a thermal sensor) located on the motherboard or a stand-alone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but is not a reliable indication that the maximum operating temperature of the processor has been reached. When using the thermal diode, a temperature offset value must be read from a processor MSR and applied. See Section 5.2 for more details. See Section 5.3 for thermal diode usage recommendation when the PROCHOT# signal is not asserted.

The reading of the external thermal sensor (on the motherboard) connected to the processor thermal diode signals will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the external thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time based variations in the die temperature measurement. Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the T_J temperature can change.

Offset between the thermal diode based temperature reading and the Intel Thermal Monitor reading may be characterized using the Intel Thermal Monitor’s Automatic mode activation of the thermal control circuit. This temperature offset must be taken into account when using the processor thermal diode to implement power management events. This offset is different than the diode T_{offset} value programmed into the processor Model Specific Register (MSR).

Table 15 and Table 16 provide the diode interface and specifications. Transistor model parameters shown in Table 16 provide more accurate temperature measurements when the diode ideality factor is closer to the maximum or minimum limits. Contact your external sensor supplier for their recommendation. The thermal diode is separate from the Thermal Monitor’s thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Table 15. Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
THERMDA	E4	Thermal diode anode
THERMDC	E5	Thermal diode cathode

Table 16. Thermal Diode Parameters using Transistor Model

Symbol	Parameter	Min	Typ	Max	Unit	Notes
IFW	Forward Bias Current	5	—	200	µA	1
IE	Emitter Current	5	—	200	µA	1
nQ	Transistor Ideality	0.997	1.001	1.015		2,3,4
Beta		0.25	—	0.65		2,3
R_T	Series Resistance	2.79	4.52	6.24	Ω	2,5

NOTES:

1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized across a temperature range of 50–100°C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, nQ, represents the deviation from ideal transistor model behavior as exemplified by the equation for the collector current:

   $$I_c = I_s * (e^{qV_{BE}/n_QkT} - 1)$$

   where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the transistor base emitter junction (same nodes as VD), k = Boltzmann Constant, and T = absolute temperature (Kelvin).

5. The series resistance, R_T, provided in the Diode Model Table (Table 16) can be used for more accurate readings as needed.

When calculating a temperature based on the thermal diode measurements, a number of parameters must be either measured or assumed. Most devices measure the diode ideality and assume a series resistance and ideality trim value, although are capable of also measuring the series resistance. Calculating the temperature is then accomplished using the equation listed under Table 16. In most sensing devices, an expected value for the diode ideality is designed-in to the temperature calculation equation. If the designer of the temperature sensing device assumes a perfect diode, the ideality value (also called n_{trim}) will be 1.000. Given that most diodes are not perfect, the designers usually select an n_{trim} value that more closely matches the behavior of the diodes in the processor. If the processor diode ideality deviates from that of the n_{trim}, each calculated temperature will be offset by a fixed amount. This temperature offset can be calculated with the equation:

$$T_{error(nf)} = Tmeasured * (1 - n_{actual}/n_{trim})$$

Where $T_{error(nf)}$ is the offset in degrees C, $T_{measured}$ is in Kelvin, n_{actual} is the measured ideality of the diode, and n_{trim} is the diode ideality assumed by the temperature sensing device.

5.2 Intel® Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks or by initiating an Enhanced Intel SpeedStep Technology transition when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: automatic mode and on-demand mode. If both modes are activated, automatic mode takes precedence.

There are two automatic modes called Intel Thermal Monitor-1 and Intel Thermal Monitor-2. These modes are selected by writing values to the MSRs of the processor. After automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

The Intel Thermal Monitor automatic mode must be enabled through BIOS for the processor to be operating within specifications. Intel recommends Intel Thermal Monitor-1 and Intel Thermal Monitor-2 be enabled on the processor.

When Intel Thermal Monitor-1 is enabled and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

When Intel Thermal Monitor-2 is enabled and a high temperature situation exists, the processor will perform an Enhanced Intel SpeedStep Technology transition to the LFM. When the processor temperature drops below the critical level, the processor will make an Enhanced Intel SpeedStep Technology transition to the last requested operating point. The processor also supports Enhanced Multi Threaded Thermal Monitoring (EMTTM). EMTTM is a processor feature that enhances Intel Thermal Monitor-2 with a processor throttling algorithm known as Adaptive Intel Thermal Monitor-2. Adaptive Intel Thermal Monitor-2 transitions to intermediate operating points, rather than directly to the LFM, once the processor has reached its thermal

limit and subsequently searches for the highest possible operating point. Please ensure this feature is enabled and supported in the BIOS. **Also with EMTTM enabled, the operating system can request the processor to throttling to any point between Intel Dynamic Acceleration frequency and Super LFM frequency as long as these features are enabled in the BIOS and supported by the processor.**

The Intel Thermal Monitor automatic mode and Enhanced Multi Threaded Thermal Monitoring must be enabled through BIOS for the processor to be operating within specifications. Intel recommends Intel Thermal Monitor-1 and Intel Thermal Monitor-2 be enabled on the processors.

Intel Thermal Monitor-1, Intel Thermal Monitor-2, and EMTTM features are collectively referred to as Adaptive Thermal Monitoring features.

Intel Thermal Monitor-1 and Intel Thermal Monitor-2 can co-exist within the processor. If both Intel Thermal Monitor-1 and Intel Thermal Monitor-2 bits are enabled in the auto-throttle MSR, Intel Thermal Monitor-2 will take precedence over Intel Thermal Monitor-1. However, if Force Intel Thermal Monitor-1 over Intel Thermal Monitor-2 is enabled in MSRs via BIOS and Intel Thermal Monitor-2 is not sufficient to cool the processor below the maximum operating temperature, then Intel Thermal Monitor-1 will also activate to help cool down the processor.

If a processor load based Enhanced Intel SpeedStep Technology transition (through MSR write) is initiated when a Intel Thermal Monitor-2 period is active, there are two possible results:

- If the processor load based Enhanced Intel SpeedStep technology transition target frequency is **higher** than the Intel Thermal Monitor-2 transition based target frequency, the processor load-based transition will be deferred until the Intel Thermal Monitor-2 event has been completed.
- If the processor load-based Enhanced Intel SpeedStep technology transition target frequency is **lower** than the Intel Thermal Monitor-2 transition based target frequency, the processor will transition to the processor load-based Enhanced Intel SpeedStep technology target frequency point.

The TCC may also be activated via on-demand mode. If bit 4 of the ACPI Intel Thermal Monitor control register is written to a 1, the TCC will be activated immediately independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in on-demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-demand mode may be used at the same time automatic mode is enabled; however, if the system tries to enable the TCC via on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three MSR, and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel

Thermal Monitor feature. The Intel Thermal Monitor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#.

PROCHOT# will not be asserted when the processor is in the Stop Grant, Sleep, Deep Sleep, and Deeper Sleep low power states; hence, the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within maximum specification. If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above low power states with PROCHOT# already asserted, PROCHOT# will remain asserted until the processor exits the low power state and the processor junction temperature drops below the thermal trip point.

If Intel Thermal Monitor automatic mode is disabled, the processor will be operating out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125°C. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in Chapter 3.

5.3 Digital Thermal Sensor

The processor also contains an on-die Digital Thermal Sensor (DTS) that is read via an MSR (no I/O interface). The DTS is only valid while the processor is in the normal operating state (the Normal package level low power state).

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor (T_{J_max}). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the DTS will always be at or below T_{J_max}. Catastrophic temperature conditions are detectable via an Out Of Spec status bit. This bit is also part of the DTS MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not ensured once the activation of the “Out of Spec” status bit is set.

The DTS-relative temperature readout corresponds to the Intel Thermal Monitor-1 and Intel Thermal Monitor -2 trigger point. When the DTS indicates maximum processor core temperature has been reached, the Intel Thermal Monitor-1 or Intel Thermal Monitor-2 hardware thermal control mechanism will activate. The DTS and Intel Thermal Monitor-1/Intel Thermal Monitor-2 temperature may not correspond to the thermal diode reading since the thermal diode is located in a separate portion of the die and thermal gradient between the individual core DTS. Additionally, the thermal gradient from DTS to thermal diode can vary substantially due to changes in processor power, mechanical and thermal attach, and software application. The system designer is required to use the DTS to ensure proper operation of the processor within its temperature operating specifications.

Changes to the temperature can be detected via two programmable thresholds located in the processor MSRs. These thresholds have the capability of generating interrupts via the core's local APIC.

Note: The digital thermal sensor (DTS) accuracy is in the order of -5°C ~ +10°C around 90°C; it deteriorates to ±10°C at 50°C. The DTS temperature reading saturates at some temperature below 50°C. Any DTS reading below 50°C should be considered to indicate only a temperature below 50°C and not a specific temperature. External thermal sensor with “BJT” model is required to read thermal diode temperature.

5.3.1 Out of Specification Detection

Overheat detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shut down before the THERMTRIP# is activated. If the processor’s Intel Thermal Monitor-1 or Intel Thermal Monitor-2 are triggered and the temperature remains high, an “Out Of Spec” status and sticky bit are latched in the status MSR register and generates thermal interrupt.

5.3.2 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If Intel Thermal Monitor-1 or Intel Thermal Monitor-2 is enabled, then the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#.

The processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from overheating situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

Only a single PROCHOT# pin exists at a package level of the processor. When the core's thermal sensor trips, the PROCHOT# signal will be driven by the processor package. If only Intel Thermal Monitor-1 is enabled, PROCHOT# will be asserted and only the core that is above TCC temperature trip point will have its core clocks modulated. If Intel Thermal Monitor-2 is enabled and the core is above TCC temperature trip point, it will enter the lowest programmed Intel Thermal Monitor-2 performance state. It is important to note that Intel recommends both Intel Thermal Monitor-1 and Intel Thermal Monitor-2 to be enabled.

When PROCHOT# is driven by an external agent and if only Intel Thermal Monitor-1 is enabled on the core, then the processor core will have the clocks modulated. If Intel Thermal Monitor-2 is enabled, then the processor core will enter the lowest programmed Intel Thermal Monitor-2 performance state. It should be noted that Force Intel Thermal Monitor-1 on Intel Thermal Monitor-2, enabled via BIOS, does not have any effect on external PROCHOT#. If PROCHOT# is driven by an external agent when Intel Thermal Monitor-1, Intel Thermal Monitor-2, and Force Intel Thermal Monitor-1 on Intel Thermal Monitor-2 are all enabled, then the processor will still apply only Intel Thermal Monitor-2.

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR will cool down as a result of reduced processor power

consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP. With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss.

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