2nd Generation Intel® Core™ Processor Family Mobile and Intel® Celeron® Processor Family Mobile

Datasheet, Volume 1

Supporting Intel® Core™ i7 Mobile Extreme Edition Processor Series and Intel® Core™ i5 and i7 Mobile Processor Series

Supporting Intel® Celeron® Mobile Processor Series

This is Volume 1 of 2

September 2012

Document Number: 324692-006

All products, platforms, dates, and figures specified are preliminary based on current expectations, and are subject to change without notice. All dates specified are target dates, are provided for planning purposes only and are subject to change.

This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local sales office that you have the latest datasheet before finalizing a design.

Enabling Execute Disable Bit functionality requires a PC with a processor with Execute Disable Bit capability and a supporting operating system. Check with your PC manufacturer on whether your system delivers Execute Disable Bit functionality.

Enhanced Intel SpeedStep® Technology; See the Processor Spec Finder or contact your Intel representative for more information.

64-bit computing on Intel architecture requires a computer system with a processor, chipset, BIOS, operating system, device drivers and applications enabled for Intel® 64 architecture. Performance will vary depending on your hardware and software configurations. Consult with your system vendor for more information.

No computer system can provide absolute security under all conditions. Intel® Trusted Execution Technology (Intel® TXT) requires a computer system with Intel® Virtualization Technology, an Intel TXT-enabled processor, chipset, BIOS, Authenticated Code Modules and an Intel TXT-compatible measured launched environment (MLE). The MLE could consist of a virtual machine monitor, an OS or an application. In addition, Intel TXT requires the system to contain a TPM v1.2, as defined by the Trusted Computing Group and specific software for some uses. For more information, see http://www.intel.com/technology/security/

Intel® Virtualization Technology requires a computer system with an enabled Intel® processor, BIOS, virtual machine monitor (VMM) and, for some uses, certain computer system software enabled for it. Functionality, performance or other benefits will vary depending on hardware and software configurations and may require a BIOS update. Software applications may not be compatible with all operating systems. Please check with your application vendor.

Intel® Active Management Technology requires the computer system to have an Intel® AMT-enabled chipset, network hardware and software, as well as connection with a power source and a corporate network connection. Setup requires configuration by the purchaser and may require scripting with the management console or further integration into existing security frameworks to enable certain functionality. It may also require modifications of implementation of new business processes. With regard to notebooks, Intel AMT may not be available or certain capabilities may be limited over a host OS-based VPN or when connecting wirelessly, on battery power, sleeping, hibernating or powered off. For more information, see http://www.intel.com/technology/platform-technology/intel-amt/

Intel® Turbo Boost Technology requires a PC with a processor with Intel Turbo Boost Technology capability. Intel Turbo Boost Technology performance varies depending on hardware, software and overall system configuration. Check with your PC manufacturer on whether your system delivers Intel Turbo Boost Technology.For more information, see http://www.intel.com/technology/turboboost.

Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. See www.intel.com/products/processor_number for details.

Code names featured are used internally within Intel to identify products that are in development and not yet publicly announced for release. Customers, licensees and other third parties are not authorized by Intel to use code names in advertising, promotion or marketing of any product or services and any such use of Intel's internal code names is at the sole risk of the user.

Contents

Figures

Tables

Revision History

Revision Number	Description	Date
001	• Initial Release	January 2011
002	• Added Intel® Core™ i7-2677M, i7-2637M, and i5-2557M processors • Added Intel® Celeron® B800 and 847 processors	June 2011
003	• Added Intel® Celeron® 787 and 857 processors	July 2011
004	• Added Intel® Celeron® B710 processor	July 2011
005	• Added Intel® Core™ i7-2960XM, i7-2860QM, i7-2760QM, and i7-2640M processors • Added Intel® Celeron® B840 processor	September 2011
006	• Added Intel® Celeron® B830, 887 processors	September 2012

§ §

1 Introduction

The 2nd Generation Intel® Core™ processor family mobile and Intel® Celeron® processor family mobile are the next generation of 64-bit, multi-core mobile processor built on 32- nanometer process technology. Based on a new micro-architecture, the processor is designed for a two-chip platform. The two-chip platform consists of a processor and Platform Controller Hub (PCH). The platform enables higher performance, lower cost, easier validation, and improved x-y footprint. The processor includes Integrated Display Engine, Processor Graphics and Integrated Memory Controller and is designed for mobile platforms. The processor comes with either 6 or 12 Processor Graphics execution units (EU). The processor may be offered in a rPGA988B, BGA1224 or BGA1023 package. Figure 1-1 shows an example platform block diagram.

This document provides DC electrical specifications, signal integrity, differential signaling specifications, pinout and signal definitions, interface functional descriptions, thermal specifications, and additional feature information pertinent to the implementation and operation of the processor on its respective platform.

Note: Throughout this document, the 2nd Generation Intel® Core™ processor family mobile and Intel® Celeron® processor family mobile may be referred to simply as “processor”.

Note: Throughout this document, the Intel® Core™ i7 Extreme Edition mobile processor series refers to the Intel® Core™ i7-2920XM processor.

Note: Throughout this document, the Intel® Core™ i7 mobile processor series refers to the Intel® Core™ i7-2960XM, i7-2860QM, i7-2820QM, i7-2760QM, i7-2720QM, i7-2677M, i7-2640M, i7-2637M, and i7-2620M processors.

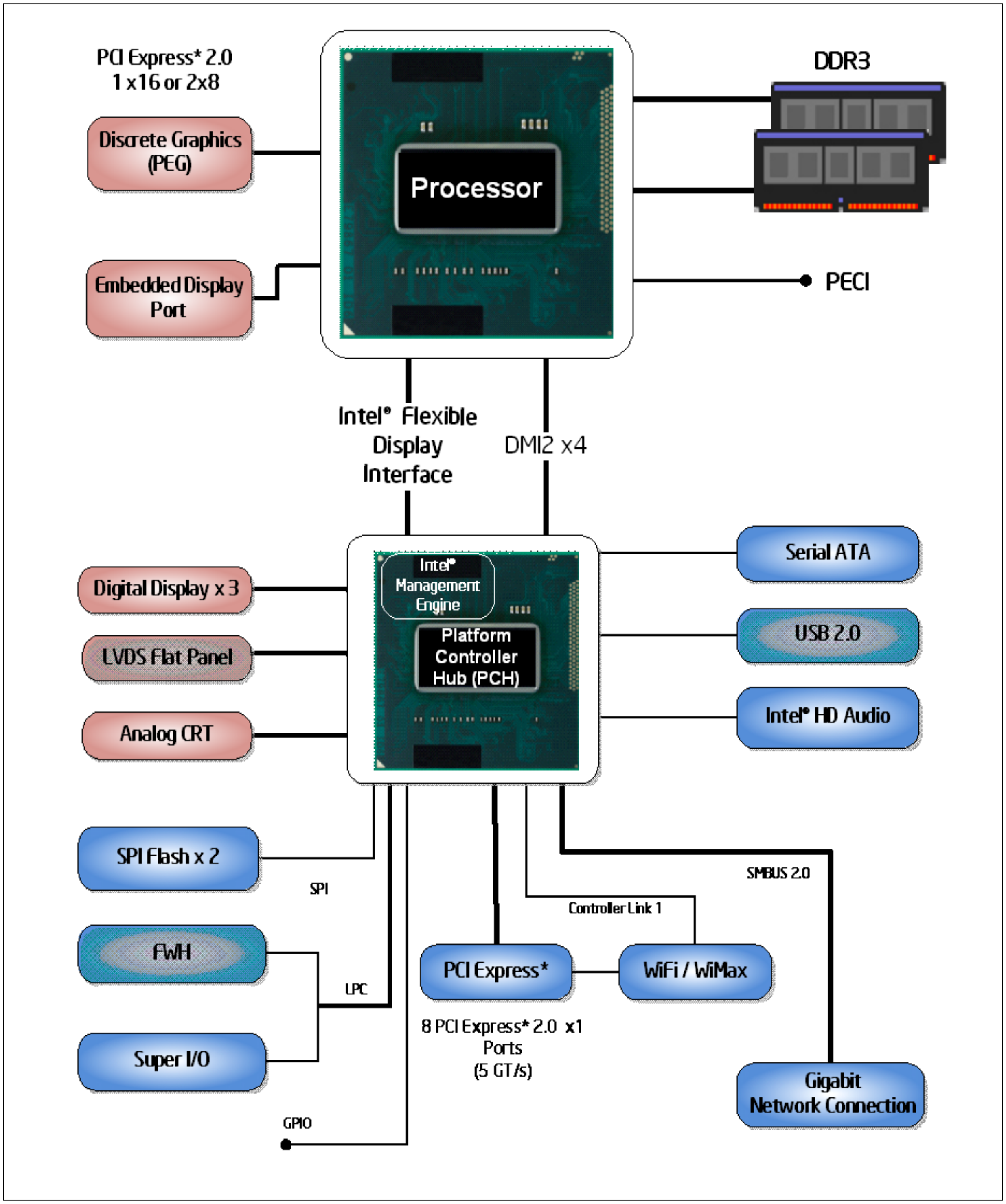
Note: Throughout this document, the Intel® Core™ i5 mobile processor series refers to the Intel® Core™ i5-2557M, i5-2540M, and i5-2520M processors.

Note: Throughout this document, the Intel® Celeron® processor family mobile refers to the Intel® Celeron® B830, B800, B710, 887, 857, 847, B840, and 787 processors.

Note: Throughout this document, the Intel® 6 Series Chipset Platform Controller Hub may also be referred to as “PCH”.

Note: Some processor features are not available on all platforms. Refer to the processor specification update for details.

Figure 1-1. Mobile Platform System Block Diagram Example



1.1 Processor Feature Details

- Four or two execution cores
- A 32-KB instruction and 32-KB data first-level cache (L1) for each core
- A 256-KB shared instruction/data second-level cache (L2) for each core
- Up to 8-MB shared instruction/data third-level cache (L3), shared among all cores

1.1.1 Supported Technologies

- Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d)
- Intel® Virtualization Technology (Intel® VT) for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x)
- Intel® Active Management Technology 7.0 (Intel® AMT 7.0)
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® Streaming SIMD Extensions 4.1 (Intel® SSE4.1)
- Intel® Streaming SIMD Extensions 4.2 (Intel® SSE4.2)
- Intel® Hyper-Threading Technology (Intel® HT Technology)
- Intel® 64 Architecture
- Execute Disable Bit
- Intel® Turbo Boost Technology
- Intel® Advanced Vector Extensions (Intel® AVX)
- Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)
- PCLMULQDQ Instruction

1.2 Interfaces

1.2.1 System Memory Support

- Two channels of DDR3 memory with a maximum of one SO-DIMM per channel
- Single-channel and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- Memory DDR3 data transfer rates of 1066 MT/s, 1333 MT/s, and 1600 MT/s
- 64-bit wide channels
- DDR3 I/O Voltage of 1.5 V
- Non-ECC, unbuffered DDR3 SO-DIMMs only
- Theoretical maximum memory bandwidth of
  - 17.1 GB/s in dual-channel mode assuming DDR3 1066 MT/s
  - 21.3 GB/s in dual-channel mode assuming DDR3 1333 MT/s
  - 25.6 GB/s in dual-channel mode assuming DDR3 1600 MT/s
- 1Gb, 2Gb, and 4Gb DDR3 DRAM technologies are supported for x8 and x16 devices
  - Using 4Gb device technologies, the largest memory capacity possible is 16 GB, assuming dual-channel mode with two x8, dual-ranked, un-buffered, non-ECC, SO-DIMM memory configuration.
- Up to 32 simultaneous open pages, 16 per channel (assuming 4 Ranks of 8 Bank Devices)

- Memory organizations
  - Single-channel modes
  - Dual-channel modes - Intel® Flex Memory Technology:
    - Dual-channel symmetric (Interleaved)
- Command launch modes of 1n/2n
- On-Die Termination (ODT)
- Asynchronous ODT
- Intel® Fast Memory Access (Intel® FMA)
  - Just-in-Time Command Scheduling
  - Command Overlap
  - Out-of-Order Scheduling

1.2.2 PCI Express*

- PCI Express* port(s) are fully-compliant with the *PCI Express Base Specification, Revision 2.0*.
- Processor with mobile PCH supported configurations

Table 1-1. PCI Express* Supported Configurations in Mobile Products

Configuration	Organization	Mobile
1	1x8	Graphics
	2x4	I/O
2	2x8	Graphics, I/O
3	1x16	Graphics, I/O

- The port may negotiate down to narrower widths
  - Support for x16/x8/x4/x1 widths for a single PCI Express mode
- 2.5 GT/s and 5.0 GT/s PCI Express* frequencies are supported
- Gen1 Raw bit-rate on the data pins of 2.5 GT/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface. This also does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on the interface of 4 GB/s in each direction simultaneously, for an aggregate of 8 GB/s when x16 Gen 1
- Gen 2 Raw bit-rate on the data pins of 5.0 GT/s, resulting in a real bandwidth per pair of 500 MB/s given the 8b/10b encoding used to transmit data across this interface. This also does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on the interface of 8 GB/s in each direction simultaneously, for an aggregate of 16 GB/s when x16 Gen 2
- Hierarchical PCI-compliant configuration mechanism for downstream devices
- Traditional PCI style traffic (asynchronous snooped, PCI ordering)
- PCI Express* extended configuration space. The first 256 bytes of configuration space aliases directly to the PCI Compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.
- PCI Express* Enhanced Access Mechanism; accessing the device configuration space in a flat memory mapped fashion
- Automatic discovery, negotiation, and training of link out of reset

- Traditional AGP style traffic (asynchronous non-snooped, PCI-X Relaxed ordering)
- Peer segment destination posted write traffic (no peer-to-peer read traffic) in Virtual Channel 0
  - DMI -> PCI Express* Port 0
  - DMI -> PCI Express* Port 1
  - PCI Express* Port 0 -> DMI
  - PCI Express* Port 1 -> DMI
- 64-bit downstream address format, but the processor never generates an address above 64 GB (Bits 63:36 will always be zeros)
- 64-bit upstream address format, but the processor responds to upstream read transactions to addresses above 64 GB (addresses where any of Bits 63:36 are nonzero) with an Unsupported Request response. Upstream write transactions to addresses above 64 GB will be dropped.
- Re-issues Configuration cycles that have been previously completed with the Configuration Retry status
- PCI Express* reference clock is 100-MHz differential clock
- Power Management Event (PME) functions
- Dynamic width capability
- Message Signaled Interrupt (MSI and MSI-X) messages
- Polarity inversion
- Dynamic lane numbering reversal as defined by the *PCI Express Base Specification*.
- Static lane numbering reversal
  - Does not support dynamic lane reversal, as defined (optional) by the *PCI Express Base Specification.*
- Supports Half Swing “low-power/low-voltage” mode.

Note: The processor does not support PCI Express* Hot-Plug.

1.2.3 Direct Media Interface (DMI)

- DMI 2.0 support
- Four lanes in each direction
- 5 GT/s point-to-point DMI interface to PCH is supported
- Raw bit-rate on the data pins of 5.0 GB/s, resulting in a real bandwidth per pair of 500 MB/s given the 8b/10b encoding used to transmit data across this interface. Does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on interface of 2 GB/s in each direction simultaneously, for an aggregate of 4 GB/s when DMI x4
- Shares 100-MHz PCI Express* reference clock
- 64-bit downstream address format, but the processor never generates an address above 64 GB (Bits 63:36 will always be zeros)
- 64-bit upstream address format, but the processor responds to upstream read transactions to addresses above 64 GB (addresses where any of Bits 63:36 are nonzero) with an Unsupported Request response. Upstream write transactions to addresses above 64 GB will be dropped.

- Supports the following traffic types to or from the PCH
  - DMI -> DRAM
  - DMI -> processor core (Virtual Legacy Wires (VLWs), Resetwarn, or MSIs only)
  - Processor core -> DMI
- APIC and MSI interrupt messaging support
  - Message Signaled Interrupt (MSI and MSI-X) messages
- Downstream SMI, SCI and SERR error indication
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive, and LPC bus masters
- DC coupling – no capacitors between the processor and the PCH
- Polarity inversion
- PCH end-to-end lane reversal across the link
- Supports Half Swing “low-power/low-voltage”

1.2.4 Platform Environment Control Interface (PECI)

The PECI is a one-wire interface that provides a communication channel between a PECI client (the processor) and a PECI master. The processors support the PECI 3.0 Specification.

1.2.5 Processor Graphics

- The Processor Graphics contains a refresh of the sixth generation graphics core enabling substantial gains in performance and lower power consumption. Up to 12 EU Support.
- Next Generation Intel Clear Video Technology HD support is a collection of video playback and enhancement features that improve the end user’s viewing experience.
  - Encode/transcode HD content
  - Playback of high definition content including Blu-ray Disc*
  - Superior image quality with sharper, more colorful images
  - Playback of Blu-ray disc S3D content using HDMI (V.1.4 with 3D)
- DirectX* Video Acceleration (DXVA) support for accelerating video processing
  - Full AVC/VC1/MPEG2 HW Decode
- Advanced Scheduler 2.0, 1.0, XPDM support
- Windows* 7, XP, Windows Vista*, OSX, Linux OS Support
- DX10.1, DX10, DX9 support
- OGL 3.0 support

1.2.6 Embedded DisplayPort* (eDP)

- Stand alone dedicated port (unlike previous generation processor that shared pins with PCIe interface)

1.2.7 Intel® Flexible Display Interface (Intel® FDI)

- For SKUs with graphics, Intel FDI carries display traffic from the Processor Graphics in the processor to the legacy display connectors in the PCH
- Based on DisplayPort standard
- Two independent links – one for each display pipe
- Four unidirectional downstream differential transmitter pairs
    - Scalable down to 3X, 2X, or 1X based on actual display bandwidth requirements
    - Fixed frequency 2.7 GT/s data rate
- Two sideband signals for Display synchronization
    - FDI_FSYNC and FDI_LSYNC (Frame and Line Synchronization)
- One Interrupt signal used for various interrupts from the PCH
    - FDI_INT signal shared by both Intel FDI Links
- PCH supports end-to-end lane reversal across both links
- Common 100-MHz reference clock

1.3 Power Management Support

1.3.1 Processor Core

- Full support of Advanced Configuration and Power Interface (ACPI) C-states as implemented by the following processor C-states
    - C0, C1, C1E, C3, C6, C7
- Enhanced Intel SpeedStep® Technology

1.3.2 System

- S0, S3, S4, S5

1.3.3 Memory Controller

- Conditional self-refresh (Intel® Rapid Memory Power Management (Intel® RMPM))
- Dynamic power-down

1.3.4 PCI Express*

- L0s and L1 ASPM power management capability

1.3.5 Direct Media Interface (DMI)

- L0s and L1 ASPM power management capability

1.3.6 Processor Graphics Controller

- Intel® Rapid Memory Power Management (Intel® RMPM) – CxSR
- Intel® Graphics Performance Modulation Technology (Intel® GPMT)
- Intel Smart 2D Display Technology (Intel S2DDT)
- Graphics Render C-State (RC6)
- Intel Seamless Display Refresh Rate Switching with Embedded DisplayPort*

1.4 Thermal Management Support

- Digital Thermal Sensor
- Intel Adaptive Thermal Monitor
- THERMTRIP# and PROCHOT# support
- On-Demand Mode
- Open and Closed Loop Throttling
- Memory Thermal Throttling
- External Thermal Sensor (TS-on-DIMM and TS-on-Board)
- Render Thermal Throttling
- Fan speed control with DTS

1.5 Package

- The processor is available on two packages:
  - A 37.5 x 37.5 mm rPGA package (rPGA988B)
  - A 31 x 24 mm BGA package (BGA1023 or BGA1224)

1.6 Terminology

Table 1-2. Terminology (Sheet 1 of 3)

Term	Description
ACPI	Advanced Configuration and Power Interface
BLT	Block Level Transfer
CRT	Cathode Ray Tube
DDR3	Third-generation Double Data Rate SDRAM memory technology
DMA	Direct Memory Access
DMI	Direct Media Interface
DP	DisplayPort*
DTS	Digital Thermal Sensor
eDP*	Embedded DisplayPort*
Enhanced Intel SpeedStep® Technology	Technology that provides power management capabilities to laptops.
EU	Execution Unit

Table 1-2. Terminology (Sheet 2 of 3)

Term	Description
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
IMC	Integrated Memory Controller
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture
Intel® DPST	Intel® Display Power Saving Technology
Intel® FDI	Intel® Flexible Display Interface
Intel® TXT	Intel® Trusted Execution Technology
Intel® Virtualization Technology	Processor virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
Intel® VT-d	Intel® Virtualization Technology (Intel® VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or OS) control, for enabling I/O device virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.
IOV	I/O Virtualization
ITPM	Integrated Trusted Platform Module
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signaling. A high speed, low power data transmission standard used for display connections to LCD panels.
NCTF	Non-Critical to Function. NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
PCH	Platform Controller Hub. The new, 2009 chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security and storage features.
PECI	Platform Environment Control Interface
PEG	PCI Express* Graphics. External Graphics using PCI Express* Architecture. A high-speed serial interface whose configuration is software compatible with the existing PCI specifications.
Processor	The 64-bit, single-core or multi-core component (package).
Processor Core	The term "processor core" refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache.
Processor Graphics	Intel® Processor Graphics
Rank	A unit of DRAM corresponding four to eight devices in parallel. These devices are usually, but not always, mounted on a single side of a SO-DIMM.
SCI	System Control Interrupt. Used in ACPI protocol.
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
TAC	Thermal Averaging Constant.
TAP	Test Access Point
TDP	Thermal Design Power.
V_{AXG}	Graphics core power supply.

Table 1-2. Terminology (Sheet 3 of 3)

Term	Description
V_{CC}	Processor core power supply.
V_{CCIO}	High Frequency I/O logic power supply
V_{CCPLL}	PLL power supply
V_{CCSA}	System Agent (memory controller, DMI, PCIe controllers, and display engine) power supply
V_{DDQ}	DDR3 power supply.
VLD	Variable Length Decoding.
V_{SS}	Processor ground.
x1	Refers to a Link or Port with one Physical Lane.
x16	Refers to a Link or Port with sixteen Physical Lanes.
x4	Refers to a Link or Port with four Physical Lanes.
x8	Refers to a Link or Port with eight Physical Lanes.

1.7 Related Documents

Refer to Table 1-3 for additional information.

Table 1-3. Related Documents

Document	Document Number/ Location
2nd Generation Intel® Core™ Processor Family Mobile and Intel® Celeron® Processor Family Mobile Datasheet, Volume 2	www.intel.com/Assets/PDF/datasheet/324803.pdf
2nd Generation Intel® Core™ Processor Family Mobile and Intel® Celeron® Processor Family Mobile Specification Update	www.intel.com/Assets/PDF/specupdate/324693.pdf
Intel® 6 Series Chipset and Intel® C200 Series Chipset Datasheet	www.intel.com/Assets/PDF/datasheet/324645.pdf
Intel® 6 Series Chipset and Intel® C200 Series Chipset Thermal Mechanical Specifications and Design Guidelines	www.intel.com/Assets/PDF/designguide/324647.pdf
Advanced Configuration and Power Interface Specification 3.0	http://www.acpi.info/
PCI Local Bus Specification 3.0	http://www.pcisig.com/specifications
Intel® TXT Measured Launched Environment Developer's Guide	http://www.intel.com/technology/security
Intel® 64 Architecture x2APIC Specification	http://www.intel.com/products/processor/manuals/
PCI Express Base Specification 2.0*	http://www.pcisig.com
DDR3 SDRAM Specification	http://www.jedec.org
DisplayPort Specification*	http://www.vesa.org
Intel® 64 and IA-32 Architectures Software Developer's Manuals	http://www.intel.com/products/processor/manuals/index.htm
Volume 1: Basic Architecture	253665
Volume 2A: Instruction Set Reference, A-M	253666
Volume 2B: Instruction Set Reference, N-Z	253667
Volume 3A: System Programming Guide	253668
Volume 3B: System Programming Guide	253669

§ §

2 Interfaces

This chapter describes the interfaces supported by the processor.

2.1 System Memory Interface

2.1.1 System Memory Technology Supported

The Integrated Memory Controller (IMC) supports DDR3 protocols with two independent, 64-bit wide channels each accessing one DIMM. It supports a maximum of one unbuffered non-ECC DDR3 DIMM per-channel; thus, allowing up to two device ranks per-channel.

- DDR3 Data Transfer Rates
  - 1066 MT/s (PC3-8500), 1333 MT/s (PC3-10600), 1600 MT/s (PC-12800)
- DDR3 SO-DIMM Modules
  - Raw Card A – Dual Ranked x16 unbuffered non-ECC
  - Raw Card B – Single Ranked x8 unbuffered non-ECC
  - Raw Card C – Single Ranked x16 unbuffered non-ECC
  - Raw Card F – Dual Ranked x8 (planar) unbuffered non-ECC
- DDR3 DRAM Device Technology

Standard 1-Gb, 2-Gb, and 4-Gb technologies and addressing are supported for x16 and x8 devices. There is no support for memory modules with different technologies or capacities on opposite sides of the same memory module. If one side of a memory module is populated, the other side is either identical or empty.

Table 2-1. Supported SO-DIMM Module Configurations[1,2]

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Physical Device Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
A	1 GB	1 Gb	64 M x 16	8	2	13/10	8	8K
	2 GB	2 Gb	128 M x 16	8	2	14/10	8	8K
B	1 GB	1 Gb	128 M x 8	8	1	14/10	8	8K
	2 GB	2 Gb	256 M x 8	8	1	15/10	8	8K
C	512 MB	1 Gb	64 M x 16	4	1	13/10	8	8K
	1 GB	2 Gb	128 M x 16	4	1	14/10	8	8K
F	2 GB	1 Gb	128 M x 8	16	2	14/10	8	8K
	4 GB	2 Gb	256 M x 8	16	2	15/10	8	8K
	8 GB	4 Gb	512 M x 8	16	2	16/ 10	8	8K

Notes:
1. System memory configurations are based on availability and are subject to change.
2. Interface does not support ULV/LV memory modules or ULV/LV DIMMs.

2.1.2 System Memory Timing Support

The IMC supports the following DDR3 Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- t_{CL} = CAS Latency
- t_{RCD} = Activate Command to READ or WRITE Command delay
- t_{RP} = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes = 1n indicates a new command may be issued every clock and 2n indicates a new command may be issued every 2 clocks. Command launch mode programming depends on the transfer rate and memory configuration.

Table 2-2. DDR3 System Memory Timing Support

Segment	Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRP (tCK)	CWL (tCK)	CMD Mode	Notes[1]
Extreme Edition (XE) and Quad Core SV	1066	7	7	7	6	1n/2n	
	1333	9	9	9	7	1n/2n	
	1600	11	11	11	8	1n/2n	
Dual Core SV, Low voltage and Ultra low voltage	1066	7	7	7	6	1n/2n	
		8	8	8	6	1n/2n	
	1333	9	9	9	7	1n/2n	

Notes:
1. System memory timing support is based on availability and is subject to change.

2.1.3 System Memory Organization Modes

The IMC supports two memory organization modes—single-channel and dual-channel. Depending upon how the DIMM Modules are populated in each memory channel, a number of different configurations can exist.

2.1.3.1 Single-Channel Mode

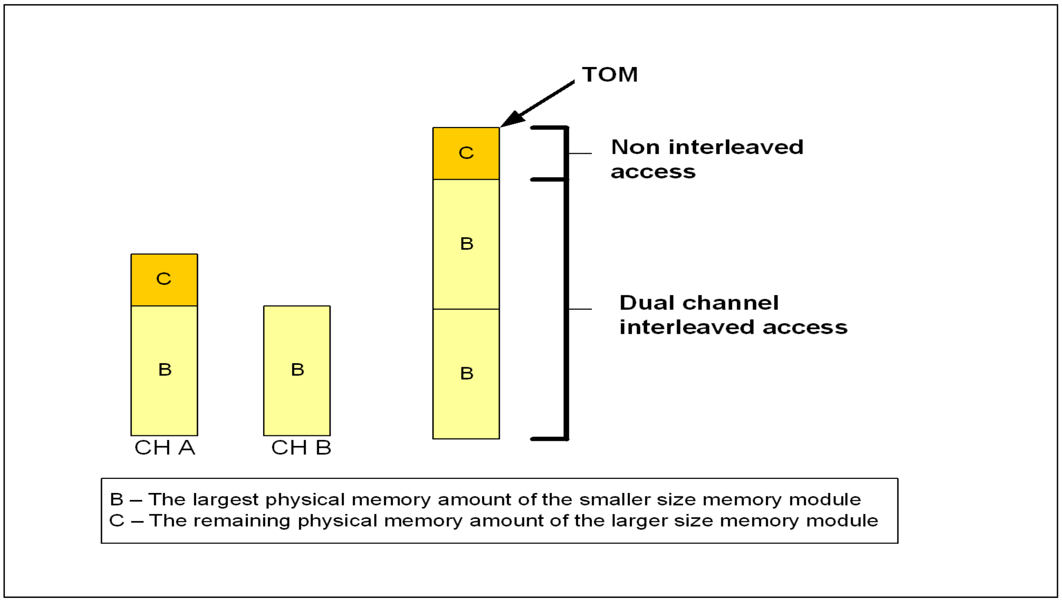
In this mode, all memory cycles are directed to a single-channel. Single-channel mode is used when either Channel A or Channel B DIMM connectors are populated in any order, but not both.

2.1.3.2 Dual-Channel Mode – Intel® Flex Memory Technology Mode

The IMC supports Intel Flex Memory Technology Mode. Memory is divided into a symmetric and an asymmetric zone. The symmetric zone starts at the lowest address in each channel and is contiguous until the asymmetric zone begins or until the top address of the channel with the smaller capacity is reached. In this mode, the system runs with one zone of dual-channel mode and one zone of single-channel mode, simultaneously, across the whole memory array.

Note: Channels A and B can be mapped for physical channels 0 and 1 respectively or vice versa; however, channel A size must be greater or equal to channel B size.

Figure 2-1. Intel® Flex Memory Technology Operation



2.1.3.2.1 Dual-Channel Symmetric Mode

Dual-Channel Symmetric mode, also known as interleaved mode, provides maximum performance on real world applications. Addresses are ping-ponged between the channels after each cache line (64-byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously since they are ensured to be on opposite channels. Use Dual-Channel Symmetric mode when both Channel A and Channel B DIMM connectors are populated in any order, with the total amount of memory in each channel being the same.

When both channels are populated with the same memory capacity and the boundary between the dual channel zone and the single channel zone is the top of memory, IMC operates completely in Dual-Channel Symmetric mode.

Note: The DRAM device technology and width may vary from one channel to the other.

2.1.4 Rules for Populating Memory Slots

In all modes, the frequency of system memory is the lowest frequency of all memory modules placed in the system, as determined through the SPD registers on the memory modules. The system memory controller supports only one DIMM connector per channel. The usage of DIMM modules with different latencies is allowed. For dual-channel modes, both channels must have an DIMM connector populated. For single-channel mode, only a single-channel can have a DIMM connector populated.

2.1.5 Technology Enhancements of Intel® Fast Memory Access (Intel® FMA)

The following sections describe the Just-in-Time Scheduling, Command Overlap, and Out-of-Order Scheduling Intel FMA technology enhancements.

2.1.5.1 Just-in-Time Command Scheduling

The memory controller has an advanced command scheduler where all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just-in-Time to make optimal use of Command Overlapping. Thus, instead of having all memory access requests go individually through an arbitration mechanism forcing requests to be executed one at a time, they can be started without interfering with the current request allowing for concurrent issuing of requests. This allows for optimized bandwidth and reduced latency while maintaining appropriate command spacing to meet system memory protocol.

2.1.5.2 Command Overlap

Command Overlap allows the insertion of the DRAM commands between the Activate, Precharge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. Multiple commands can be issued in an overlapping manner, increasing the efficiency of system memory protocol.

2.1.5.3 Out-of-Order Scheduling

While leveraging the Just-in-Time Scheduling and Command Overlap enhancements, the IMC continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back to back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the IMC to further reduce latency and increase bandwidth efficiency.

2.1.6 Memory Type Range Registers (MTRRs) Enhancement

The processor has 2 additional MTRRs (total 10 MTRRs). These additional MTRRs are specially important in supporting larger system memory beyond 4 GB.

2.1.7 Data Scrambling

The memory controller incorporates a DDR3 Data Scrambling feature to minimize the impact of excessive di/dt on the platform DDR3 VRs due to successive 1s and 0s on the data bus. Past experience has demonstrated that traffic on the data bus is not random and can have energy concentrated at specific spectral harmonics creating high di/dt that is generally limited by data patterns that excite resonance between the package inductance and on-die capacitances. As a result, the memory controller uses a data scrambling feature to create pseudo-random patterns on the DDR3 data bus to reduce the impact of any excessive di/dt.

2.1.8 DRAM Clock Generation

Every supported DIMM has two differential clock pairs. There are a total of four clock pairs driven directly by the processor to two DIMMs.

2.2 PCI Express* Interface

This section describes the PCI Express interface capabilities of the processor. See the *PCI Express Base Specification* for details of PCI Express.

The processor has one PCI Express controller that can support one external x16 PCI Express Graphics Device. The primary PCI Express Graphics port is referred to as PEG 0.

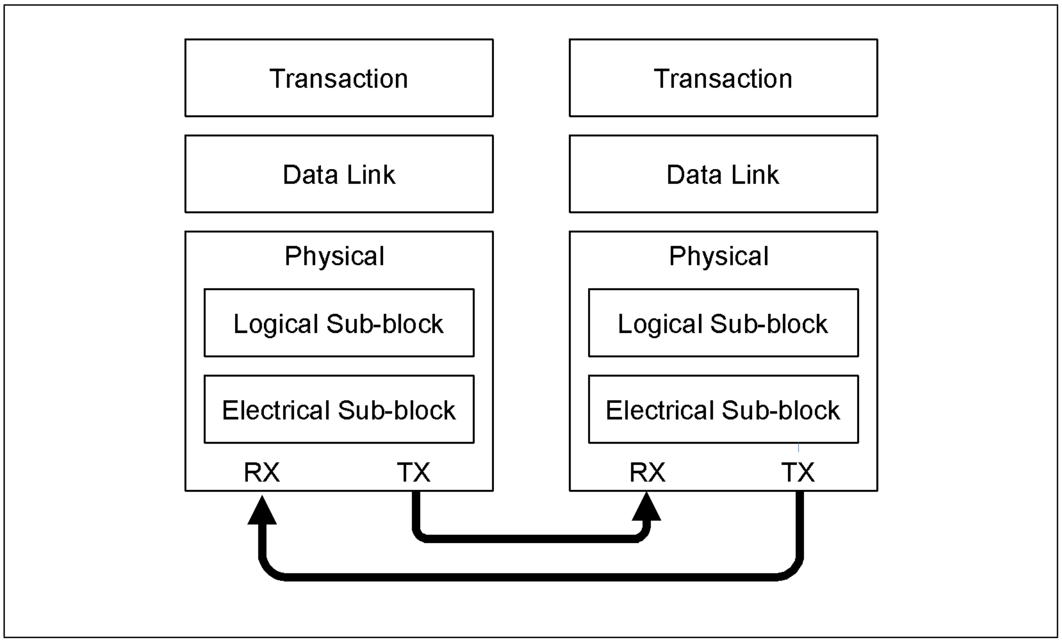
2.2.1 PCI Express* Architecture

Compatibility with the PCI addressing model is maintained to ensure that all existing applications and drivers operate unchanged.

The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The initial recovered clock speed of 1.25 GHz results in 2.5 Gb/s/direction that provides a 250 MB/s communications channel in each direction (500 MB/s total). That is close to twice the data rate of classic PCI. The fact that 8b/10b encoding is used accounts for the 250 MB/s where quick calculations would imply 300 MB/s. The external graphics ports support Gen2 speed as well. At 5.0 GT/s, Gen 2 operation results in twice as much bandwidth per lane as compared to Gen 1 operation. When operating with two PCIe controllers, each controller can be operating at either 2.5 GT/s or 5.0 GT/s.

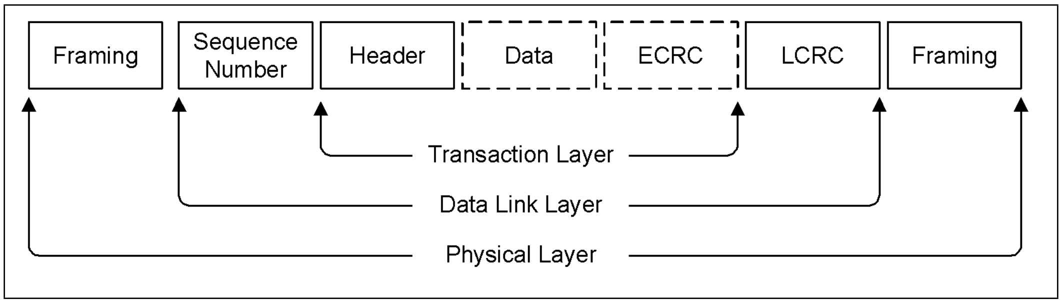
The PCI Express architecture is specified in three layers—Transaction Layer, Data Link Layer, and Physical Layer. The partitioning in the component is not necessarily along these same boundaries. Refer to Figure 2-2 for the PCI Express Layering Diagram.

Figure 2-2. PCI Express* Layering Diagram



PCI Express uses packets to communicate information between components. Packets are formed in the Transaction and Data Link Layers to carry the information from the transmitting component to the receiving component. As the transmitted packets flow through the other layers, they are extended with additional information necessary to handle packets at those layers. At the receiving side, the reverse process occurs and packets get transformed from their Physical Layer representation to the Data Link Layer representation and finally (for Transaction Layer Packets) to the form that can be processed by the Transaction Layer of the receiving device.

Figure 2-3. Packet Flow through the Layers



2.2.1.1 Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The Transaction Layer also manages flow control of TLPs.

2.2.1.2 Data Link Layer

The middle layer in the PCI Express stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

The transmission side of the Data Link Layer accepts TLPs assembled by the Transaction Layer, calculates and applies data protection code and TLP sequence number, and submits them to Physical Layer for transmission across the Link. The receiving Data Link Layer is responsible for checking the integrity of received TLPs and for submitting them to the Transaction Layer for further processing. On detection of TLP error(s), this layer is responsible for requesting retransmission of TLPs until information is correctly received, or the Link is determined to have failed. The Data Link Layer also generates and consumes packets that are used for Link management functions.

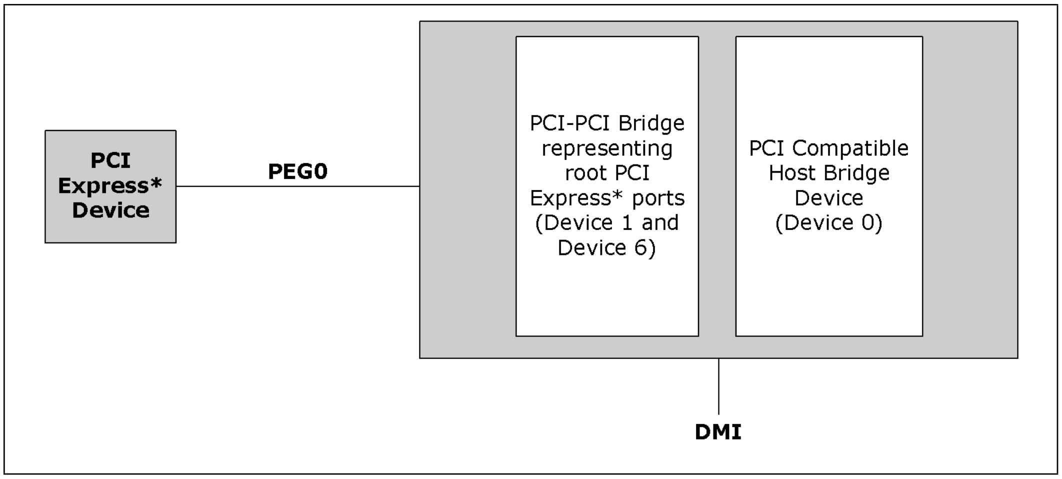
2.2.1.3 Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry. It also includes logical functions related to interface initialization and maintenance. The Physical Layer exchanges data with the Data Link Layer in an implementation-specific format, and is responsible for converting this to an appropriate serialized format and transmitting it across the PCI Express Link at a frequency and width compatible with the remote device.

2.2.2 PCI Express* Configuration Mechanism

The PCI Express (external graphics) link is mapped through a PCI-to-PCI bridge structure.

Figure 2-4. PCI Express* Related Register Structures in the Processor



PCI Express extends the configuration space to 4096 bytes per-device/function, as compared to 256 bytes allowed by the Conventional PCI Specification. PCI Express configuration space is divided into a PCI-compatible region (that consists of the first 256 bytes of a logical device's configuration space) and an extended PCI Express region (that consists of the remaining configuration space). The PCI-compatible region can be accessed using either the mechanisms defined in the PCI specification or using the enhanced PCI Express configuration access mechanism described in the PCI Express Enhanced Configuration Mechanism section.

The PCI Express Host Bridge is required to translate the memory-mapped PCI Express configuration space accesses from the host processor to PCI Express configuration cycles. To maintain compatibility with PCI configuration addressing mechanisms, it is recommended that system software access the enhanced configuration space using 32-bit operations (32-bit aligned) only. See the *PCI Express Base Specification* for details of both the PCI-compatible and PCI Express Enhanced configuration mechanisms and transaction rules.

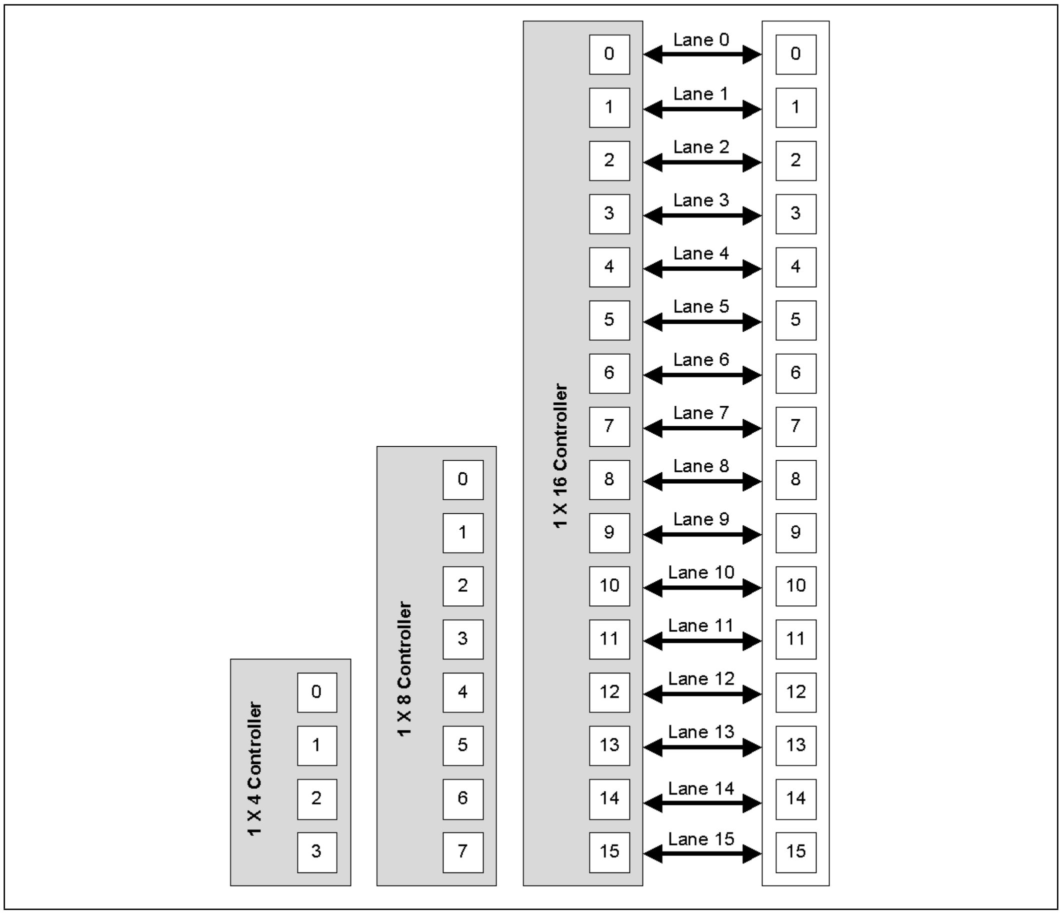
2.2.3 PCI Express Graphics

The external graphics attach (PEG) on the processor is a single, 16-lane (x16) port. The PEG port is compliant with the *PCI Express Base Specification, Revision 2.0.*

2.2.4 PCI Express* Lanes Connection

Figure 2-5 demonstrates the PCIe lanes mapping.

Figure 2-5. PCI Express* Typical Operation 16 lanes Mapping



2.3 Direct Media Interface (DMI)

Direct Media Interface (DMI) connects the processor and the PCH. Next generation DMI2 is supported.

Note: Only DMI x4 configuration is supported.

2.3.1 DMI Error Flow

DMI can only generate SERR in response to errors, never SCI, SMI, MSI, PCI INT, or GPE. Any DMI related SERR activity is associated with Device 0.

2.3.2 Processor / PCH Compatibility Assumptions

The processor is compatible with the Intel® 6 Series Chipset PCH. The processor is not compatible with any previous PCH products.

2.3.3 DMI Link Down

The DMI link going down is a fatal, unrecoverable error. If the DMI data link goes to data link down, after the link was up, then the DMI link hangs the system by not allowing the link to retrain to prevent data corruption. This link behavior is controlled by the PCH.

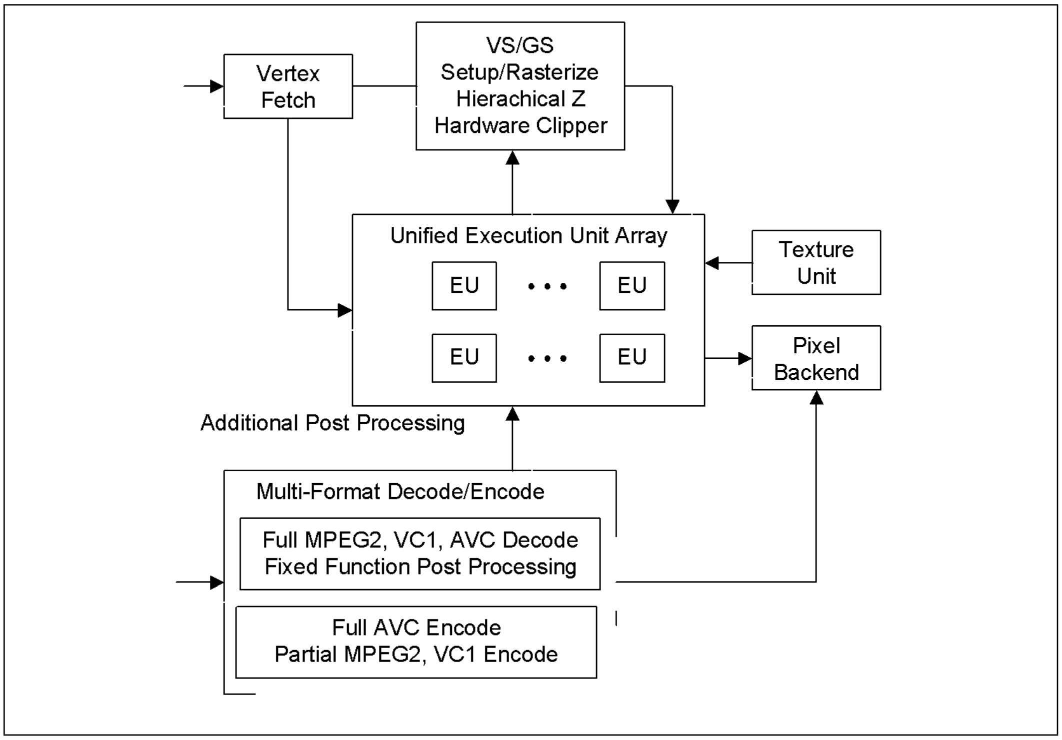
Downstream transactions that had been successfully transmitted across the link prior to the link going down may be processed as normal. No completions from downstream, non-posted transactions are returned upstream over the DMI link after a link down event.

2.4 Processor Graphics Controller (GT)

New Graphics Engine Architecture includes 3D compute elements, Multi-format hardware-assisted decode/encode Pipeline, and Mid-Level Cache (MLC) for superior high definition playback, video quality, and improved 3D performance and Media.

Display Engine in the Uncore handles delivering the pixels to the screen. GSA (Graphics in System Agent) is the primary Channel interface for display memory accesses and "PCI-like" traffic in and out.

Figure 2-6. Processor Graphics Controller Unit Block Diagram



2.4.1 3D and Video Engines for Graphics Processing

The 3D graphics pipeline architecture simultaneously operates on different primitives or on different portions of the same primitive. All the cores are fully programmable, increasing the versatility of the 3D Engine. The Gen 6.0 3D engine provides the following performance and power-management enhancements:

- Up to 12 Execution units (EUs)
- Hierarchal-Z
- Video quality enhancements

2.4.1.1 3D Engine Execution Units

- Supports up to 12 EUs. The EUs perform 128-bit wide execution per clock.
- Support SIMD8 instructions for vertex processing and SIMD16 instructions for pixel processing.

2.4.1.2 3D Pipeline

2.4.1.2.1 Vertex Fetch (VF) Stage

The VF stage executes 3DPRIMITIVE commands. Some enhancements have been included to better support legacy D3D APIs as well as SGI OpenGL*.

2.4.1.2.2 Vertex Shader (VS) Stage

The VS stage performs shading of vertices output by the VF function. The VS unit produces an output vertex reference for every input vertex reference received from the VF unit, in the order received.

2.4.1.2.3 Geometry Shader (GS) Stage

The GS stage receives inputs from the VS stage. Compiled application-provided GS programs, specifying an algorithm to convert the vertices of an input object into some output primitives. For example, a GS shader may convert lines of a line strip into polygons representing a corresponding segment of a blade of grass centered on the line. Or it could use adjacency information to detect silhouette edges of triangles and output polygons extruding out from the edges.

2.4.1.2.4 Clip Stage

The Clip stage performs general processing on incoming 3D objects. However, it also includes specialized logic to perform a Clip Test function on incoming objects. The Clip Test optimizes generalized 3D Clipping. The Clip unit examines the position of incoming vertices, and accepts/rejects 3D objects based on its Clip algorithm.

2.4.1.2.5 Strips and Fans (SF) Stage

The SF stage performs setup operations required to rasterize 3D objects. The outputs from the SF stage to the Windower stage contain implementation-specific information required for the rasterization of objects and also supports clipping of primitives to some extent.

2.4.1.2.6 Windower/IZ (WIZ) Stage

The WIZ unit performs an early depth test, which removes failing pixels and eliminates unnecessary processing overhead.

The Windower uses the parameters provided by the SF unit in the object-specific rasterization algorithms. The WIZ unit rasterizes objects into the corresponding set of pixels. The Windower is also capable of performing dithering, whereby the illusion of a higher resolution when using low-bpp channels in color buffers is possible. Color dithering diffuses the sharp color bands seen on smooth-shaded objects.

2.4.1.3 Video Engine

The Video Engine handles the non-3D (media/video) applications. It includes support for VLD and MPEG2 decode in hardware.

2.4.1.4 2D Engine

The 2D Engine contains BLT (Block Level Transfer) functionality and an extensive set of 2D instructions. To take advantage of the 3D during engine’s functionality, some BLT functions make use of the 3D renderer.

2.4.1.4.1 Processor Graphics VGA Registers

The 2D registers consists of original VGA registers and others to support graphics modes that have color depths, resolutions, and hardware acceleration features that go beyond the original VGA standard.

2.4.1.4.2 Logical 128-Bit Fixed BLT and 256 Fill Engine

This BLT engine accelerates the GUI of Microsoft Windows* operating systems. The 128-bit BLT engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The BLT engine can be used for the following:

- Move rectangular blocks of data between memory locations
- Data alignment
- To perform logical operations (raster ops)

The rectangular block of data does not change, as it is transferred between memory locations. The allowable memory transfers are between: cacheable system memory and frame buffer memory, frame buffer memory and frame buffer memory, and within system memory. Data to be transferred can consist of regions of memory, patterns, or solid color fills. A pattern is always 8 x 8 pixels wide and may be 8, 16, or 32 bits per pixel.

The BLT engine expands monochrome data into a color depth of 8, 16, or 32 bits. BLTs can be either opaque or transparent. Opaque transfers move the data specified to the destination. Transparent transfers compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source memory location, the BLT engine specifies which area in memory to begin the BLT transfer. Hardware is included for all 256 raster operations (source, pattern, and destination) defined by Microsoft, including transparent BLT.

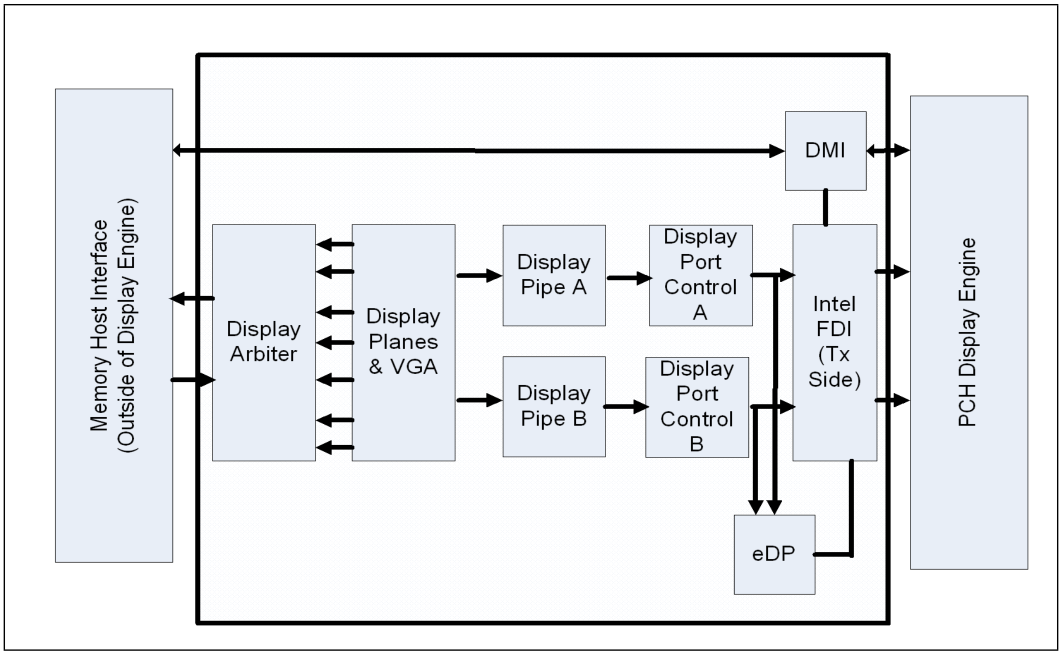
The BLT engine has instructions to invoke BLT and stretch BLT operations, permitting software to set up instruction buffers and use batch processing. The BLT engine can perform hardware clipping during BLTs.

2.4.2 Processor Graphics Display

The Processor Graphics controller display pipe can be broken down into three components:

- Display Planes
- Display Pipes
- Embedded DisplayPort* and Intel® FDI

Figure 2-7. Processor Display Block Diagram



2.4.2.1 Display Planes

A display plane is a single displayed surface in memory and contains one image (desktop, cursor, overlay). It is the portion of the display hardware logic that defines the format and location of a rectangular region of memory that can be displayed on display output device and delivers that data to a display pipe. This is clocked by the Core Display Clock.

2.4.2.1.1 Planes A and B

Planes A and B are the main display planes and are associated with Pipes A and B respectively. The two display pipes are independent, allowing for support of two independent display streams. They are both double-buffered, which minimizes latency and improves visual quality.

2.4.2.1.2 Sprite A and B

Sprite A and Sprite B are planes optimized for video decode, and are associated with Planes A and B respectively. Sprite A and B are also double-buffered.

2.4.2.1.3 Cursors A and B

Cursors A and B are small, fixed-sized planes dedicated for mouse cursor acceleration, and are associated with Planes A and B respectively. These planes support resolutions up to 256 x 256 each.

2.4.2.1.4 Video Graphics Array (VGA)

VGA is used for boot, safe mode, legacy games, etc. It can be changed by an application without OS/driver notification, due to legacy requirements.

2.4.2.2 Display Pipes

The display pipe blends and synchronizes pixel data received from one or more display planes and adds the timing of the display output device upon which the image is displayed. This is clocked by the Display Reference clock inputs.

The display pipes A and B operate independently of each other at the rate of 1 pixel per clock. They can attach to any of the display ports. Each pipe sends display data to the PCH over the Intel Flexible Display Interface (Intel FDI).

2.4.2.3 Display Ports

The display ports consist of output logic and pins that transmit the display data to the associated encoding logic and send the data to the display device (that is, LVDS, HDMI*, DVI, SDVO, and so on). All display interfaces connecting external displays are now repartitioned and driven from the PCH with the exception of the DisplayPort.

2.4.2.4 Embedded DisplayPort*

The Processor Graphics supports the Embedded DisplayPort* (eDP) interface, intended for display devices that are integrated into the system (such as laptop LCD panel).

The DisplayPort (abbreviated DP) is different than the generic term display port. The DisplayPort specification is a VESA standard. DisplayPort consolidates internal and external connection methods to reduce device complexity, support cross industry applications, and provide performance scalability. The eDP interface supports link-speeds of 1.62 Gbps and 2.7 Gbps on 1, 2, or 4 data lanes. The eDP supports -0.5% SSC and non-SSC clock settings.

2.4.3 Intel® Flexible Display Interface (Intel® FDI)

The Intel Flexible Display Interface (Intel® FDI) is a proprietary link for carrying display traffic from the Processor Graphics controller to the PCH display I/Os. Intel® FDI supports two independent channels—one for pipe A and one for pipe B.

- Each channel has four transmit (Tx) differential pairs used for transporting pixel and framing data from the display engine.
- Each channel has one single-ended LineSync and one FrameSync input (1-V CMOS signaling).
- One display interrupt line input (1-V CMOS signaling).
- Intel® FDI may dynamically scalable down to 2X or 1X based on actual display bandwidth requirements.
- Common 100-MHz reference clock.
- Each channel transports at a rate of 2.7 Gbps.
- PCH supports end-to-end lane reversal across both channels (no reversal support required in the processor).

2.4.4 Multi-Graphics Controller Multi-Monitor Support

The processor supports simultaneous use of the Processor Graphics Controller (GT) and a x16 PCI Express Graphics (PEG) device.

The processor supports a maximum of 2 displays connected to the PEG card in parallel with up to 2 displays connected to the processor and PCH.

Note: When supporting Multi Graphics controllers Multi-Monitors, "drag and drop" between monitors and the 2x8 PEG is not supported.

2.5 Platform Environment Control Interface (PECI)

The PECI is a one-wire interface that provides a communication channel between a PECI client (processor) and a PECI master. The processor implements a PECI interface to:

- Allow communication of processor thermal and other information to the PECI master.
- Read averaged Digital Thermal Sensor (DTS) values for fan speed control.

2.6 Interface Clocking

2.6.1 Internal Clocking Requirements

Table 2-3. Reference Clock

Reference Input Clock	Input Frequency	Associated PLL
BCLK/BCLK#	100 MHz	Processor/Memory/Graphics/PCIe/DMI/FDI
DPLL_REF_CLK/DPLL_REF_CLK#	120 MHz	Embedded DisplayPort (eDP)

§ §

3 Technologies

This chapter provides a high-level description of Intel technologies implemented in the processor.

The implementation of the features may vary between the processor SKUs.

Details on the different technologies of Intel processors and other relevant external notes are located at the Intel technology web site: http://www.intel.com/technology/

3.1 Intel® Virtualization Technology (Intel® VT)

Intel Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel Virtualization Technology (Intel VT-x) added hardware support in the processor to improve the virtualization performance and robustness. Intel Virtualization Technology for Directed I/O (Intel VT-d) adds chipset hardware implementation to support and improve I/O virtualization performance and robustness.

Intel VT-x specifications and functional descriptions are included in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B* and is available at:

http://www.intel.com/products/processor/manuals/index.htm

The Intel VT-d specification and other VT documents can be referenced at:

http://www.intel.com/technology/virtualization/index.htm

3.1.1 Intel® Virtualization Technology (Intel® VT) for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) Objectives

Intel VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel VT-x features to provide improved a reliable virtualized platform. By using Intel VT-x, a VMM is:

- **Robust:** VMMs no longer need to use paravirtualization or binary translation. This means that they will be able to run off-the-shelf OSs and applications without any special steps.
- **Enhanced:** Intel VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- **More reliable:** Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.
- **More secure:** The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system.

3.1.2 Intel® Virtualization Technology (Intel® VT) for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) Features

The processor core supports the following Intel VT-x features:

- Extended Page Tables (EPT)
  - EPT is hardware assisted page table virtualization
  - It eliminates VM exits from guest OS to the VMM for shadow page-table maintenance
- Virtual Processor IDs (VPID)
  - Ability to assign a VM ID to tag processor core hardware structures (such as TLBs)
  - This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
- Guest Preemption Timer
  - Mechanism for a VMM to preempt the execution of a guest OS after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest
  - The feature aids VMM developers in flexibility and Quality of Service (QoS) assurances
- Descriptor-Table Exiting
  - Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).
  - A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.

3.1.3 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) Objectives

The key Intel VT-d objectives are domain-based isolation and hardware-based virtualization. A domain can be abstractly defined as an isolated environment in a platform to which a subset of host physical memory is allocated. Virtualization allows for the creation of one or more partitions on a single system. This could be multiple partitions in the same operating system, or there can be multiple operating system instances running on the same system – offering benefits such as system consolidation, legacy migration, activity partitioning, or security.

3.1.4 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) Features

The processor supports the following Intel VT-d features:

- Memory controller and Processor Graphics comply with Intel® VT-d 1.2 specification.
- Two VT-d DMA remap engines.
    - iGraphics DMA remap engine
    - DMI/PEG
- Support for root entry, context entry, and default context
- 39-bit guest physical address and host physical address widths
- Support for 4K page sizes only
- Support for register-based fault recording only (for single entry only) and support for MSI interrupts for faults
- Support for both leaf and non-leaf caching
- Support for boot protection of default page table
- Support for non-caching of invalid page table entries
- Support for hardware based flushing of translated but pending writes and pending reads, on IOTLB invalidation
- Support for page-selective IOTLB invalidation
- MSI cycles (MemWr to address FEEx_xxxxh) not translated
    - Translation faults result in cycle forwarding to VBIOS region (byte enables masked for writes). Returned data may be bogus for internal agents, PEG/DMI interfaces return unsupported request status
- Interrupt Remapping is supported
- Queued invalidation is supported.
- VT-d translation bypass address range is supported (Pass Through)

Note: Intel VT-d Technology may not be available on all SKUs.

3.1.5 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) Features Not Supported

The following features are not supported by the processor with Intel VT-d:

- No support for PCISIG endpoint caching (ATS)
- No support for Intel VT-d read prefetching/snarfing (that is, translations within a cacheline are not stored in an internal buffer for reuse for subsequent translations).
- No support for advance fault reporting
- No support for super pages
- No support for Intel VT-d translation bypass address range (such usage models need to be resolved with VMM help in setting up the page tables correctly)

3.2 Intel® Trusted Execution Technology (Intel® TXT)

Intel Trusted Execution Technology (Intel TXT) defines platform-level enhancements that provide the building blocks for creating trusted platforms.

The Intel TXT platform helps to provide the authenticity of the controlling environment such that those wishing to rely on the platform can make an appropriate trust decision. The Intel TXT platform determines the identity of the controlling environment by accurately measuring and verifying the controlling software.

Another aspect of the trust decision is the ability of the platform to resist attempts to change the controlling environment. The Intel TXT platform will resist attempts by software processes to change the controlling environment or bypass the bounds set by the controlling environment.

Intel TXT is a set of extensions designed to provide a measured and controlled launch of system software that will then establish a protected environment for itself and any additional software that it may execute.

These extensions enhance two areas:

- The launching of the Measured Launched Environment (MLE)
- The protection of the MLE from potential corruption

The enhanced platform provides these launch and control interfaces using Safer Mode Extensions (SMX).

The SMX interface includes the following functions:

- Measured/Verified launch of the MLE
- Mechanisms to ensure the above measurement is protected and stored in a secure location
- Protection mechanisms that allow the MLE to control attempts to modify itself

For more information, refer to the *Intel® TXT Measured Launched Environment Developer's Guide* in http://www.intel.com/technology/security*.*

3.3 Intel® Hyper-Threading Technology (Intel® HT Technology)

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology), that allows an execution core to function as two logical processors. While some execution resources (such as caches, execution units, and buses) are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support.

Intel recommends enabling Intel HT Technology with Microsoft Windows 7*, Microsoft Windows Vista*, Microsoft Windows* XP Professional/Windows* XP Home, and disabling Intel HT Technology using the BIOS for all previous versions of Windows operating systems. For more information on Intel HT Technology, see http://www.intel.com/technology/platform-technology/hyper-threading/.

3.4 Intel® Turbo Boost Technology

Compared with previous generation products, Intel Turbo Boost Technology will increase the ratio of application power to TDP. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at the maximum power limit for significant periods of time.

Note: Intel Turbo Boost Technology may not be available on all SKUs.

Intel Turbo Boost Technology is a feature that allows the processor to opportunistically and automatically run faster than its rated operating core and/or render clock frequency when there is sufficient power headroom, and the product is within specified temperature and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads. The processor supports a Turbo mode where the processor can use the thermal capacity associated with package and run at power levels higher than TDP power for short durations. This improves the system responsiveness for short, bursty usage conditions. The turbo feature needs to be properly enabled by BIOS for the processor to operate with maximum performance. Since the turbo feature is configurable and dependent on many platform design limits outside of the processor control, the maximum performance cannot be ensured.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment, and system design.

3.4.1 Intel® Turbo Boost Technology Frequency

The processor's rated frequency assumes that all execution cores are active and are at the sustained thermal design power (TDP). However, under typical operation not all cores are active or at executing a high power workload. Therefore, most applications are consuming less than the TDP at the rated frequency. Intel Turbo Boost Technology takes advantage of the available TDP headroom and active cores are able to increase their operating frequency.

To determine the highest performance frequency amongst active cores, the processor takes the following into consideration to recalculate turbo frequency during runtime:

- The number of cores operating in the C0 state.
- The estimated core current consumption.
- The estimated package prior and present power consumption.
- The package temperature.

Any of these factors can affect the maximum frequency for a given workload. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

Note: Intel Turbo Technology processor frequencies are only active if the operating system is requesting the P0 state. For more information on P-states and C-states refer to Chapter 4, “Power Management”.

3.4.2 Intel® Turbo Boost Technology Graphics Frequency

The graphics render frequency is selected dynamically based on graphics workload demand as permitted by the processor turbo control. The processor can optimize both processor and Processor Graphics performance through power sharing. The processor cores and the processor graphics core share a package power limit. If the graphics core is not consuming enough power to reach the package power limit, the cores can increase frequency to take advantage of the unused thermal power headroom. The opposite can happen when the processor cores are not consuming enough power to reach the package power limit. For the Processor Graphics, this could mean an increase in the render core frequency (above its rated frequency) and increased graphics performance. Both the processor core(s) and the graphics render core can increase frequency higher than possible without power sharing.

Note: Processor utilization of turbo graphic frequencies requires that the Intel Graphics driver to be properly installed. Turbo graphic frequencies are not dependent on the operating system processor P-state requests and may turbo while the processor is in any processor P-states.

3.5 Intel® Advanced Vector Extensions (Intel® AVX)

Intel Advanced Vector Extensions (Intel AVX) is the latest expansion of the Intel instruction set. It extends the Intel Streaming SIMD Extensions (Intel SSE) from 128-bit vectors into 256-bit vectors. Intel AVX addresses the continued need for vector floating-point performance in mainstream scientific and engineering numerical applications, visual processing, recognition, data-mining/synthesis, gaming, physics, cryptography and other areas of applications. The enhancement in Intel AVX allows for improved performance due to wider vectors, new extensible syntax, and rich functionality including the ability to better manage, rearrange, and sort data. For more information on Intel AVX, see http://www.intel.com/software/avx

3.6 Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)

The processor supports Advanced Encryption Standard New Instructions (Intel AES-NI) that are a set of Single Instruction Multiple Data (SIMD) instructions that enable fast and secure data encryption and decryption based on the Advanced Encryption Standard (AES). Intel AES-NI are valuable for a wide range of cryptographic applications; such as, applications that perform bulk encryption/decryption, authentication, random number generation, and authenticated encryption. AES is broadly accepted as the standard for both government and industry applications, and is widely deployed in various protocols.

Intel AES-NI consists of six Intel SSE instructions. Four instructions, AESENC, AESENCLAST, AESDEC, and AESDELAST facilitate high performance AES encryption and decryption. The other two, AESIMC and AESKEYGENASSIST, support the AES key expansion procedure. Together, these instructions provide a full hardware for supporting AES, offering security, high performance, and a great deal of flexibility.

3.6.1 PCLMULQDQ Instruction

The processor supports the carry-less multiplication instruction, PCLMULQDQ. PCLMULQDQ is a Single Instruction Multiple Data (SIMD) instruction that computes the 128-bit carry-less multiplication of two, 64-bit operands without generating and propagating carries. Carry-less multiplication is an essential processing component of several cryptographic systems and standards. Hence, accelerating carry-less multiplication can significantly contribute to achieving high speed secure computing and communication.

3.7 Intel® 64 Architecture x2APIC

The x2APIC architecture extends the xAPIC architecture that provides a key mechanism for interrupt delivery. This extension is intended primarily to increase processor addressability.

Specifically, x2APIC:

- Retains all key elements of compatibility to the xAPIC architecture
    - delivery modes
    - interrupt and processor priorities
    - interrupt sources
    - interrupt destination types
- Provides extensions to scale processor addressability for both the logical and physical destination modes
- Adds new features to enhance performance of interrupt delivery
- Reduces complexity of logical destination mode interrupt delivery on link based architectures

The key enhancements provided by the x2APIC architecture over xAPIC are the following:

- Support for two modes of operation to provide backward compatibility and extensibility for future platform innovations
    - In xAPIC compatibility mode, APIC registers are accessed through a memory mapped interface to a 4 KB page, identical to the xAPIC architecture.
    - In x2APIC mode, APIC registers are accessed through Model Specific Register (MSR) interfaces. In this mode, the x2APIC architecture provides significantly increased processor addressability and some enhancements on interrupt delivery.
- Increased range of processor addressability in x2APIC mode
    - Physical xAPIC ID field increases from 8 bits to 32 bits, allowing for interrupt processor addressability up to 4G-1 processors in physical destination mode. A processor implementation of x2APIC architecture can support fewer than 32-bits in a software transparent fashion.
    - Logical xAPIC ID field increases from 8 bits to 32 bits. The 32-bit logical x2APIC ID is partitioned into two sub-fields—a 16-bit cluster ID and a 16-bit logical ID within the cluster. Consequently, ((2^20) -16) processors can be addressed in logical destination mode. Processor implementations can support fewer than 16 bits in the cluster ID sub-field and logical ID sub-field in a software agnostic fashion.

- More efficient MSR interface to access APIC registers
  - To enhance inter-processor and self directed interrupt delivery as well as the ability to virtualize the local APIC, the APIC register set can be accessed only through MSR based interfaces in the x2APIC mode. The Memory Mapped IO (MMIO) interface used by xAPIC is not supported in the x2APIC mode.
- The semantics for accessing APIC registers have been revised to simplify the programming of frequently-used APIC registers by system software. Specifically, the software semantics for using the Interrupt Command Register (ICR) and End Of Interrupt (EOI) registers have been modified to allow for more efficient delivery and dispatching of interrupts.

The x2APIC extensions are made available to system software by enabling the local x2APIC unit in the “x2APIC” mode. To benefit from x2APIC capabilities, a new Operating System and a new BIOS are both needed, with special support for the x2APIC mode.

The x2APIC architecture provides backward compatibility to the xAPIC architecture and forward extendibility for future Intel platform innovations.

Note: Intel x2APIC technology may not be available on all processor SKUs.

For more information, refer to the *Intel® 64 Architecture x2APIC Specification* at http://www.intel.com/products/processor/manuals/

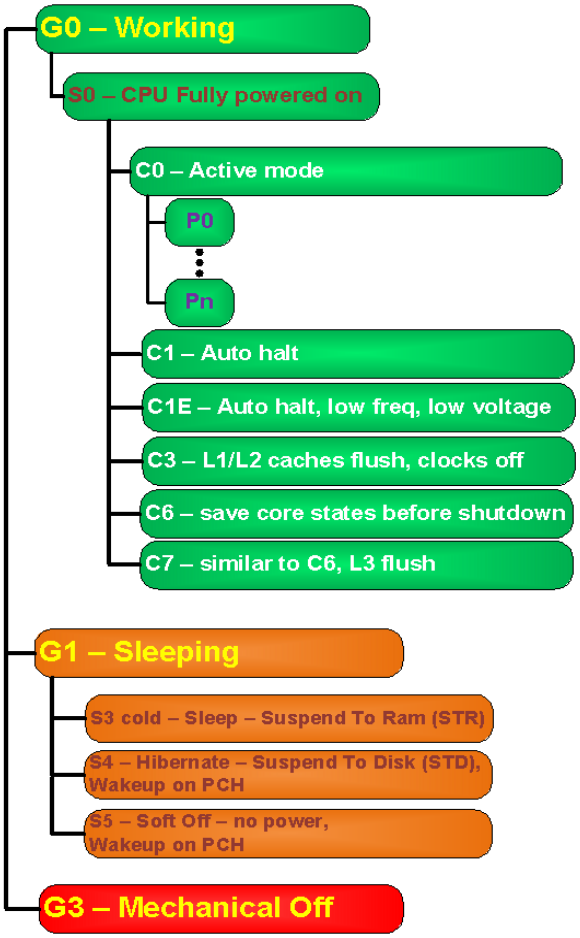
§ §

4 Power Management

This chapter provides information on the following power management topics:

- Advanced Configuration and Power Interface (ACPI) States
- Processor Core
- Integrated Memory Controller (IMC)
- PCI Express*
- Direct Media Interface (DMI)
- Processor Graphics Controller

Figure 4-1. Power States



* Note: Power states availability may vary between the different SKUs

4.1 Advanced Configuration and Power Interface (ACPI) States Supported

The ACPI states supported by the processor are described in this section.

4.1.1 System States

Table 4-1. System States

State	Description
G0/S0	Full On
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot is not supported by the processor).
G1/S4	Suspend-to-Disk (STD). All power lost (except wakeup on PCH).
G2/S5	Soft off. All power lost (except wakeup on PCH). Total reboot.
G3	Mechanical off. All power (AC and battery) removed from system.

4.1.2 Processor Core / Package Idle States

Table 4-2. Processor Core / Package State Support

State	Description
C0	Active mode, processor executing code
C1	AutoHALT state
C1E	AutoHALT state with lowest frequency and voltage operating point
C3	Execution cores in C3 flush their L1 instruction cache, L1 data cache, and L2 cache to the L3 shared cache. Clocks are shut off to each core.
C6	Execution cores in this state save their architectural state before removing core voltage.
C7	Execution cores in this state behave similarly to the C6 state. If all execution cores request C7, L3 cache ways are flushed until it is cleared.

4.1.3 Integrated Memory Controller States

Table 4-3. Integrated Memory Controller States

State	Description
Power up	CKE asserted. Active mode
Pre-charge Power-down	CKE de-asserted (not self-refresh) with all banks closed
Active Power-Down	CKE de-asserted (not self-refresh) with minimum one bank active
Self-Refresh	CKE de-asserted using device self-refresh

4.1.4 PCI Express* Link States

Table 4-4. PCI Express* Link States

State	Description
L0	Full on – Active transfer state
L0s	First Active Power Management low power state – Low exit latency
L1	Lowest Active Power Management – Longer exit latency
L3	Lowest power state (power-off) – Longest exit latency

4.1.5 Direct Media Interface (DMI) States

Table 4-5. Direct Media Interface (DMI) States

State	Description
L0	Full on – Active transfer state
L0s	First Active Power Management low power state – Low exit latency
L1	Lowest Active Power Management – Longer exit latency
L3	Lowest power state (power-off) – Longest exit latency

4.1.6 Processor Graphics Controller States

Table 4-6. Processor Graphics Controller States

State	Description
D0	Full on, display active
D3 Cold	Power-off

4.1.7 Interface State Combinations

Table 4-7. G, S, and C State Combinations

Global (G) State	Sleep (S) State	Processor Package (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt
G0	S0	C3	Deep Sleep	On	Deep Sleep
G0	S0	C6/C7	Deep Power-down	On	Deep Power-down
G1	S3	Power off		Off, except RTC	Suspend to RAM
G1	S4	Power off		Off, except RTC	Suspend to Disk
G2	S5	Power off		Off, except RTC	Soft Off
G3	NA	Power off		Power off	Hard off

Table 4-8. D, S, and C State Combination

Graphics Adapter (D) State	Sleep (S) State	Package (C) State	Description
D0	S0	C0	Full On, Displaying
D0	S0	C1/C1E	Auto-Halt, Displaying
D0	S0	C3	Deep sleep, Displaying
D0	S0	C6/C7	Deep Power Down, Displaying
D3	S0	Any	Not displaying
D3	S3	N/A	Not displaying, Graphics Core is powered off
D3	S4	N/A	Not displaying, suspend to disk

4.2 Processor Core Power Management

While executing code, Enhanced Intel SpeedStep Technology optimizes the processor's frequency and core voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, lower power C-states have longer entry and exit latencies.

4.2.1 Enhanced Intel® SpeedStep® Technology

The following are the key features of Enhanced Intel SpeedStep Technology:

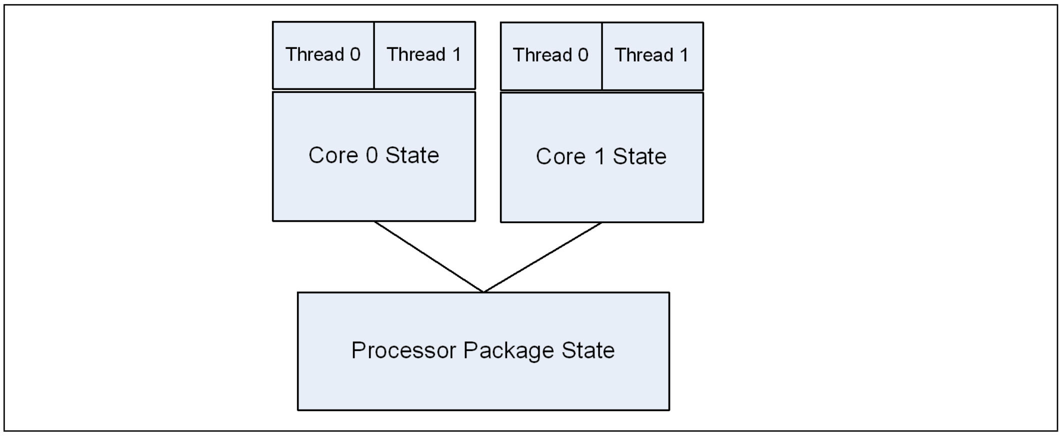
- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency and the number of active processor cores.
  - If the target frequency is higher than the current frequency, V_{CC} is ramped up in steps to an optimized voltage. This voltage is signaled by the SVID bus to the voltage regulator. Once the voltage is established, the PLL locks on to the target frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the target frequency, then transitions to a lower voltage by signaling the target voltage on SVID bus.
  - All active processor cores share the same frequency and voltage. In a multi-core processor, the highest frequency P-state requested amongst all active cores is selected.
  - Software-requested transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition is completed.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Because there is low transition latency between P-states, a significant number of transitions per-second are possible.

4.2.2 Low-Power Idle States

When the processor is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, higher C-states have longer exit and entry latencies. Resolution of C-states occur at the thread, processor core, and processor package level. Thread-level C-states are available if Intel HT Technology is enabled.

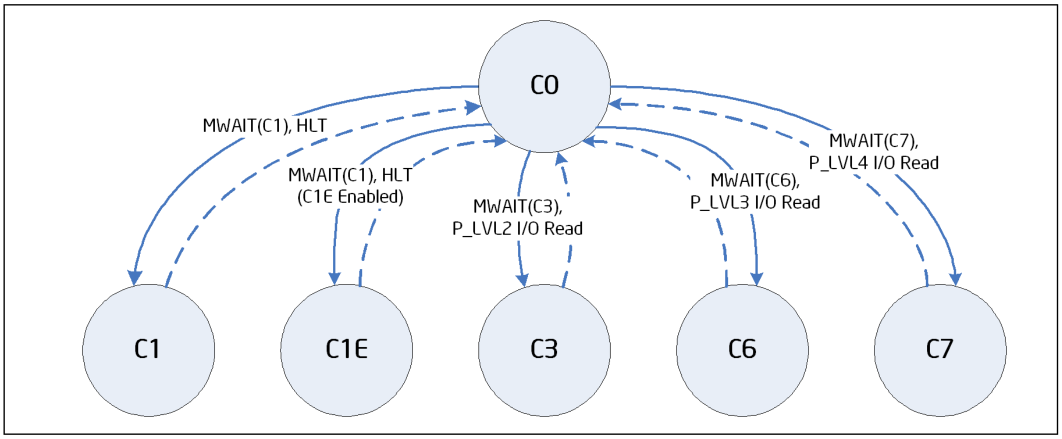
Caution: Long term reliability cannot be assured unless all the Low Power Idle States are enabled.

Figure 4-2. Idle Power Management Breakdown of the Processor Cores



Entry and exit of the C-States at the thread and core level are shown in Figure 4-3.

Figure 4-3. Thread and Core C-State Entry and Exit



While individual threads can request low power C-states, power saving actions only take place once the core C-state is resolved. Core C-states are automatically resolved by the processor. For thread and core C-states, a transition to and from C0 is required before entering any other C-state.

Table 4-9. Coordination of Thread Power States at the Core Level

Processor Core C-State		Thread 1				
		C0	**C1**	**C3**	**C6**	**C7**
Thread 0	**C0**	C0	C0	C0	C0	C0
	C1	C0	C1[1]	C1[1]	C1[1]	C1[1]
	C3	C0	C1[1]	C3	C3	C3
	C6	C0	C1[1]	C3	C6	C6
	C7	C0	C1[1]	C3	C6	C7

Note: If enabled, the core C-state will be C1E if all cores have resolved a core C1 state or higher.

4.2.3 Requesting Low-Power Idle States

The primary software interfaces for requesting low power idle states are through the MWAIT instruction with sub-state hints and the HLT instruction (for C1 and C1E). However, software may make C-state requests using the legacy method of I/O reads from the ACPI-defined processor clock control registers, referred to as P_LVLx. This method of requesting C-states provides legacy support for operating systems that initiate C-state transitions using I/O reads.

For legacy operating systems, P_LVLx I/O reads are converted within the processor to the equivalent MWAIT C-state request. Therefore, P_LVLx reads do not directly result in I/O reads to the system. The feature, known as I/O MWAIT redirection, must be enabled in the BIOS.

Note: The P_LVLx I/O Monitor address needs to be set up before using the P_LVLx I/O read interface. Each P-LVLx is mapped to the supported MWAIT(Cx) instruction as shown in Table 4-10.

Table 4-10. P_LVLx to MWAIT Conversion

P_LVLx	MWAIT(Cx)	Notes
P_LVL2	MWAIT(C3)	
P_LVL3	MWAIT(C6)	C6. No sub-states allowed.
P_LVL4	MWAIT(C7)	C7. No sub-states allowed.
P_LVL5+	MWAIT(C7)	C7. No sub-states allowed.

The BIOS can write to the C-state range field of the PMG_IO_CAPTURE MSR to restrict the range of I/O addresses that are trapped and emulate MWAIT like functionality. Any P_LVLx reads outside of this range does not cause an I/O redirection to MWAIT(Cx) like request. They fall through like a normal I/O instruction.

Note: When P_LVLx I/O instructions are used, MWAIT substates cannot be defined. The MWAIT substate is always zero if I/O MWAIT redirection is used. By default, P_LVLx I/O redirections enable the MWAIT 'break on EFLAGS.IF’ feature that triggers a wakeup on an interrupt, even if interrupts are masked by EFLAGS.IF.

4.2.4 Core C-states

The following are general rules for all core C-states, unless specified otherwise:

- A core C-State is determined by the lowest numerical thread state (such as Thread 0 requests C1E while Thread 1 requests C3, resulting in a core C1E state). See Table 4-7.
- A core transitions to C0 state when:
  - — An interrupt occurs
  - — There is an access to the monitored address if the state was entered using an MWAIT instruction
- For core C1/C1E, core C3, and core C6/C7, an interrupt directed toward a single thread wakes only that thread. However, since both threads are no longer at the same core C-state, the core resolves to C0.
- A system reset re-initializes all processor cores.

4.2.4.1 Core C0 State

The normal operating state of a core where code is being executed.

4.2.4.2 Core C1/C1E State

C1/C1E is a low power state entered when all threads within a core execute a HLT or MWAIT(C1/C1E) instruction.

A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1/C1E state. See the *Intel® 64 and IA-32 Architecture Software Developer's Manual, Volume 3A/3B: System Programmer's Guide for more information.*

While a core is in C1/C1E state, it processes bus snoops and snoops from other threads. For more information on C1E, see Section 4.2.5.2.

4.2.4.3 Core C3 State

Individual threads of a core can enter the C3 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C3) instruction. A core in C3 state flushes the contents of its L1 instruction cache, L1 data cache, and L2 cache to the shared L3 cache, while maintaining its architectural state. All core clocks are stopped at this point. Because the core's caches are flushed, the processor does not wake any core that is in the C3 state when either a snoop is detected or when another core accesses cacheable memory.

4.2.4.4 Core C6 State

Individual threads of a core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering core C6, the core will save its architectural state to a dedicated SRAM. Once complete, a core will have its voltage reduced to zero volts. During exit, the core is powered on and its architectural state is restored.

4.2.4.5 Core C7 State

Individual threads of a core can enter the C7 state by initiating a P_LVL4 I/O read to the P_BLK or by an MWAIT(C7) instruction. The core C7 state exhibits the same behavior as the core C6 state unless the core is the last one in the package to enter the C7 state. If it is, that core is responsible for flushing L3 cache ways. The processor supports the C7s substate. When an MWAIT(C7) command is issued with a C7s sub-state hint, the entire L3 cache is flushed in one step as opposed to flushing the L3 cache in multiple steps.

4.2.4.6 C-State Auto-Demotion

In general, deeper C-states such as C6 or C7 have long latencies and have higher energy entry/exit costs. The resulting performance and energy penalties become significant when the entry/exit frequency of a deeper C-state is high. Therefore, incorrect or inefficient usage of deeper C-states have a negative impact on battery life idle. To increase residency and improve battery life idle in deeper C-states, the processor supports C-state auto-demotion.

There are two C-State auto-demotion options:

- C7/C6 to C3
- C7/C6/C3 To C1

The decision to demote a core from C6/C7 to C3 or C3/C6/C7 to C1 is based on each core's immediate residency history. Upon each core C6/C7 request, the core C-state is demoted to C3 or C1 until a sufficient amount of residency has been established. At that point, a core is allowed to go into C3/C6 or C7. Each option can be run concurrently or individually.

This feature is disabled by default. BIOS must enable it in the PMG_CST_CONFIG_CONTROL register. The auto-demotion policy is also configured by this register.

4.2.5 Package C-States

The processor supports C0, C1/C1E, C3, C6, and C7 power states. The following is a summary of the general rules for package C-state entry. These apply to all package C-states unless specified otherwise:

- A package C-state request is determined by the lowest numerical core C-state amongst all cores.
- A package C-state is automatically resolved by the processor depending on the core idle power states and the status of the platform components.
  - Each core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
  - The platform may allow additional power savings to be realized in the processor.
  - For package C-states, the processor is not required to enter C0 before entering any other C-state.

The processor exits a package C-state when a break event is detected. Depending on the type of break event, the processor does the following:

- If a core break event is received, the target core is activated and the break event message is forwarded to the target core.
  - If the break event is not masked, the target core enters the core C0 state and the processor enters package C0.
- If the break event was due to a memory access or snoop request.
  - But the platform did not request to keep the processor in a higher package C-state, the package returns to its previous C-state.
  - And the platform requests a higher power C-state, the memory access or snoop request is serviced and the package remains in the higher power C-state.

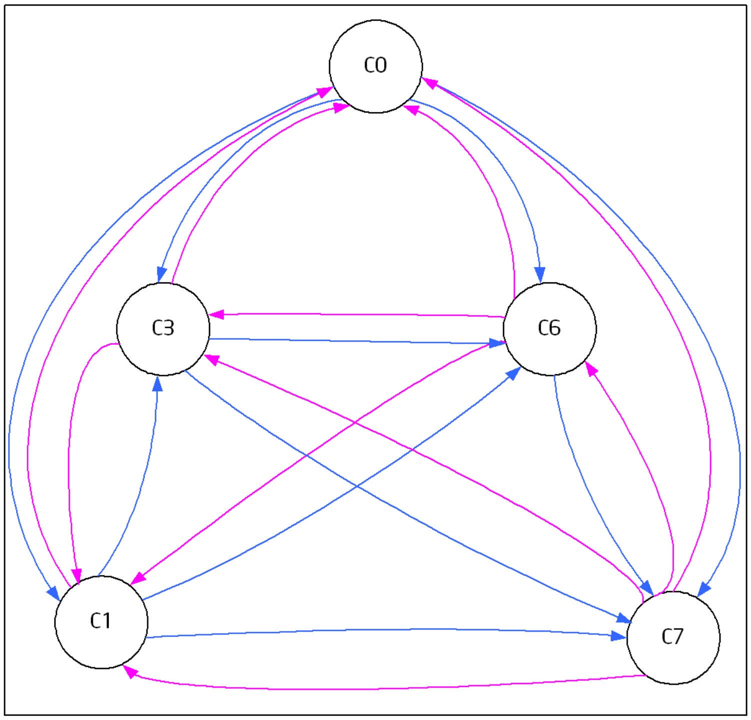
Table 4-11 shows package C-state resolution for a dual-core processor. Figure 4-4 summarizes package C-state transitions.

Table 4-11. Coordination of Core Power States at the Package Level

Package C-State		Core 1				
		C0	**C1**	**C3**	**C6**	**C7**
Core 0	**C0**	C0	C0	C0	C0	C0
	C1	C0	C1[1]	C1[1]	C1[1]	C1[1]
	C3	C0	C1[1]	C3	C3	C3
	C6	C0	C1[1]	C3	C6	C6
	C7	C0	C1[1]	C3	C6	C7

Note: If enabled, the package C-state will be C1E if all cores have resolved a core C1 state or higher.

Figure 4-4. Package C-State Entry and Exit



4.2.5.1 Package C0

This is the normal operating state for the processor. The processor remains in the normal state when at least one of its cores is in the C0 or C1 state or when the platform has not granted permission to the processor to go into a low power state. Individual cores may be in lower power idle states while the package is in C0.

4.2.5.2 Package C1/C1E

No additional power reduction actions are taken in the package C1 state. However, if the C1E sub-state is enabled, the processor automatically transitions to the lowest supported core clock frequency, followed by a reduction in voltage.

The package enters the C1 low power state when:

- At least one core is in the C1 state.
- The other cores are in a C1 or lower power state.

The package enters the C1E state when:

- All cores have directly requested C1E using MWAIT(C1) with a C1E sub-state hint.
- All cores are in a power state lower that C1/C1E but the package low power state is limited to C1/C1E using the PMG_CST_CONFIG_CONTROL MSR.
- All cores have requested C1 using HLT or MWAIT(C1) and C1E auto-promotion is enabled in IA32_MISC_ENABLES.

No notification to the system occurs upon entry to C1/C1E.

4.2.5.3 Package C3 State

A processor enters the package C3 low power state when:

- At least one core is in the C3 state.
- The other cores are in a C3 or lower power state, and the processor has been granted permission by the platform.
- The platform has not granted a request to a package C6/C7 state but has allowed a package C6 state.

In package C3-state, the L3 shared cache is valid.

4.2.5.4 Package C6 State

A processor enters the package C6 low power state when:

- At least one core is in the C6 state.
- The other cores are in a C6 or lower power state, and the processor has been granted permission by the platform.
- The platform has not granted a package C7 request but has allowed a C6 package state.

In package C6 state, all cores have saved their architectural state and have had their core voltages reduced to zero volts. The L3 shared cache is still powered and snoopable in this state. The processor remains in package C6 state as long as any part of the L3 cache is active.

4.2.5.5 Package C7 State

The processor enters the package C7 low power state when all cores are in the C7 state and the L3 cache is completely flushed. The last core to enter the C7 state begins to shrink the L3 cache by N-ways until the entire L3 cache has been emptied. This allows further power savings.

Core break events are handled the same way as in package C3 or C6. However, snoops are not sent to the processor in package C7 state because the platform, by granting the package C7 state, has acknowledged that the processor possesses no snoopable information. This allows the processor to remain in this low power state and maximize its power savings.

Upon exit of the package C7 state, the L3 cache is not immediately re-enabled. It re-enables once the processor has stayed out of C6 or C7 for an preset amount of time. Power is saved since this prevents the L3 cache from being re-populated only to be immediately flushed again.

4.2.5.6 Dynamic L3 Cache Sizing

Upon entry into the package C7 state, the L3 cache is reduced by N-ways until it is completely flushed. The number of ways, N, is dynamically chosen per concurrent C7 entry. Similarly, upon exit, the L3 cache is gradually expanded based on internal heuristics.

4.3 Integrated Memory Controller (IMC) Power Management

The main memory is power managed during normal operation and in low-power ACPI Cx states.

4.3.1 Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a memory module connector in which it is not connected to any actual memory devices (such as SO-DIMM connector is unpopulated, or is single-sided) is tri-stated. The benefits of disabling unused SM signals are:

- Reduced power consumption.
- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated, the corresponding chip select and CKE signals are not driven.

At reset, all rows must be assumed to be populated, until it can be proven that they are not populated. This is due to the fact that when CKE is tristated with an SO-DIMM present, the SO-DIMM is not ensured to maintain data integrity.

SCKE tri-state should be enabled by BIOS where appropriate, since at reset all rows must be assumed to be populated.

4.3.2 DRAM Power Management and Initialization

The processor implements extensive support for power management on the SDRAM interface. There are four SDRAM operations associated with the Clock Enable (CKE) signals that the SDRAM controller supports. The processor drives four CKE pins to perform these operations.

The CKE is one of the power-save means. When CKE is off the internal DDR clock is disabled and the DDR power is reduced. The power-saving differs according the selected mode and the DDR type used. For more information, please refer to the IDD table in the DDR specification.

The DDR specification defines 3 levels of power-down that differ in power-saving and in wakeup time:

1. **Active power-down (APD):** This mode is entered if there are open pages when de-asserting CKE. In this mode the open pages are retained. Power-saving in this mode is the lowest. Power consumption of DDR is defined by IDD3P. Exiting this mode is fined by tXP – small number of cycles.
2. **Precharged power-down (PPD):** This mode is entered if all banks in DDR are precharged when de-asserting CKE. Power-saving in this mode is intermediate – better than APD, but less than DLL-off. Power consumption is defined by IDD2P1. Exiting this mode is defined by tXP. Difference from APD mode is that when waking-up all page-buffers are empty
3. **DLL-off:** In this mode the data-in DLLs on DDR are off. Power-saving in this mode is the best among all power-modes. Power consumption is defined by IDD2P1. Exiting this mode is defined by tXP, but also tXPDLL (10 – 20 according to DDR type) cycles until first data transfer is allowed.

The processor supports 5 different types of power-down. The different modes are the power-down modes supported by DDR3 and combinations of these. The type of CKE power-down is defined by the configuration. The are options are:

1. No power-down
2. APD: The rank enters power-down as soon as idle-timer expires, no matter what is the bank status
3. PPD: When idle timer expires the MC sends PRE-all to rank and then enters power-down
4. DLL-off: same as option (2) but DDR is configured to DLL-off
5. APD, change to PPD (APD-PPD): Begins as option (1), and when all page-close timers of the rank are expired, it wakes the rank, issues PRE-all, and returns to PPD APD, change to DLL-off (APD_DLLoff) – Begins as option (1), and when all page-close timers of the rank are expired, it wakes the rank, issues PRE-all and returns to DLL-off power-down

The CKE is determined per rank when it is inactive. Each rank has an idle-counter. The idle-counter starts counting as soon as the rank has no accesses, and if it expires, the rank may enter power-down while no new transactions to the rank arrive to queues. The idle-counter begins counting at the last incoming transaction arrival.

It is important to understand that since the power-down decision is per rank, the MC can find many opportunities to power-down ranks even while running memory intensive applications, and savings are significant (may be a few watts, according to the DDR specification). This is significant when each channel is populated with more ranks.

Selection of power modes should be according to power-performance or thermal trade-offs of a given system:

- When trying to achieve maximum performance and power or thermal consideration is not an issue: use no power-down.
- In a system that tries to minimize power-consumption, try to use the deepest power-down mode possible – DLL-off or APD_DLLoff.
- In high-performance systems with dense packaging (that is, complex thermal design) the power-down mode should be considered in order to reduce the heating and avoid DDR throttling caused by the heating.

Control of the power-mode through CRB-BIOS: The BIOS selects by default no-power-down. There are knobs to change the power-down selected mode.

Another control is the idle timer expiration count. This is set through PM_PDWN_config bits 7:0 (MCHBAR +4CB0). As this timer is set to a shorter time, the MC will have more opportunities to put DDR in power-down. The minimum recommended value for this register is 15. There is no BIOS hook to set this register. Customers who choose to change the value of this register can do it by changing the BIOS. For experiments, this register can be modified in real time if BIOS did not lock the MC registers.

Note: In APD, APD-PPD, and APD-DLLoff there is no point in setting the idle-counter in the same range of page-close idle timer.

Another option associated with CKE power-down is the S_DLL-off. When this option is enabled, the SBR I/O slave DLLs go off when all channel ranks are in power-down. (Do **not** confuse it with the DLL-off mode, in which the **DDR** DLLs are off). This mode requires to define the I/O slave DLL wakeup time.

4.3.2.1 Initialization Role of CKE

During power-up, CKE is the only input to the SDRAM that has its level recognized (other than the DDR3 reset pin) once power is applied. It must be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during power-up. CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is ensured to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.

4.3.2.2 Conditional Self-Refresh

Intel Rapid Memory Power Management (Intel RMPM) conditionally places memory into self-refresh in the package C3, C6, and C7 low-power states. Intel RMPM functionality depends on the graphics/display state (relevant only when processor graphics is being used), as well as memory traffic patterns generated by other connected I/O devices. The target behavior is to enter self-refresh as long as there are no memory requests to service.

When entering the S3 – Suspend-to-RAM (STR) state or S0 conditional self-refresh, the processor core flushes pending cycles and then enters all SDRAM ranks into self-refresh. The CKE signals remain LOW so the SDRAM devices perform self-refresh.

Table 4-12. Targeted Memory State Conditions

Mode	Memory State with Processor Graphics	Memory State with External Graphics
C0, C1, C1E	Dynamic memory rank power down based on idle conditions.	Dynamic memory rank power down based on idle conditions.
C3, C6, C7	If the Processor Graphics engine is idle and there are no pending display requests, then enter self-refresh. Otherwise, use dynamic memory rank power down based on idle conditions.	If there are no memory requests, then enter self-refresh. Otherwise, use dynamic memory rank power down based on idle conditions.
S3	Self-Refresh Mode.	Self-Refresh Mode.
S4	Memory power down (contents lost).	Memory power down (contents lost)

4.3.2.3 Dynamic Power-down Operation

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power-down state. The processor core controller can be configured to put the devices in *active power-down* (CKE de-assertion with open pages) or *precharge power-down* (CKE de-assertion with all pages closed). Precharge power-down provides greater power savings but has a bigger performance impact, since all pages will first be closed before putting the devices in power-down mode.

If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

4.3.2.4 DRAM I/O Power Management

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel. Clocks can be controlled on a per SO-DIMM basis. Exceptions are made for per SO-DIMM control signals such as CS#, CKE, and ODT for unpopulated SO-DIMM slots.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path must be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).

4.4 PCI Express* Power Management

- Active power management support using L0s, and L1 states.
- All inputs and outputs disabled in L2/L3 Ready state.

Note: PEG interface does not support Hot Plug.

Note: Power impact may be observed when PEG link disable power management state is used.

4.5 Direct Media Interface (DMI) Power Management

- Active power management support using L0s/L1 state.

4.6 Graphics Power Management

4.6.1 Intel® Rapid Memory Power Management (Intel® RMPM) (also known as CxSR)

The Intel Rapid Memory Power Management puts rows of memory into self refresh mode during C3/C6/C7 to allow the system to remain in the lower power states longer. Mobile processors routinely save power during runtime conditions by entering the C3, C6, or C7 state. Intel RMPM is an indirect method of power saving that can have a significant effect on the system as a whole.

4.6.2 Intel® Graphics Performance Modulation Technology (Intel® GPMT)

Intel Graphics Power Modulation Technology (Intel GPMT) is a method for saving power in the graphics adapter while continuing to display and process data in the adapter. This method will switch the render frequency and/or render voltage dynamically between higher and lower power states supported on the platform based on render engine workload. When the system is running in battery mode, and if the end user launches applications such as 3D or Video, the graphics software may switch the render frequency dynamically between higher and lower power/performance states depending on the render engine workload.

In products where Intel® Graphics Dynamic Frequency (also known as Turbo Boost Technology) is supported and enabled, the functionality of Intel GPMT will be maintained by Intel® Graphics Dynamic Frequency (also known as Turbo Boost Technology).

4.6.3 Graphics Render C-State

Render C-State (RC6) is a technique designed to optimize the average power to the graphics render engine during times of idleness of the render engine. Render C-state is entered when the graphics render engine, blitter engine and the video engine have no workload being currently worked on and no outstanding graphics memory transactions. When the idleness condition is met, the Integrated Graphics will program the VR into a low voltage state (~0.4 V) through the SVID bus.

Render C-State (RC6) is a technique designed to optimize the average power to the graphics render engine during times of idleness of the render engine. Render C-state is entered when the graphics render engine, blitter engine and the video engine have no workload being currently worked on and no outstanding graphics memory transactions. When the idleness condition is met, the Processor Graphics will program the VR into a low voltage state (0-~0.4 V) through the SVID bus.

4.6.4 Intel® Smart 2D Display Technology (Intel® S2DDT)

Intel S2DDT reduces display refresh memory traffic by reducing memory reads required for display refresh. Power consumption is reduced by less accesses to the IMC. S2DDT is only enabled in single pipe mode.

Intel S2DDT is most effective with:

- Display images well suited to compression, such as text windows, slide shows, and so on. Poor examples are 3D games.
- Static screens such as screens with significant portions of the background showing 2D applications, processor benchmarks, and so on, or conditions when the processor is idle. Poor examples are full-screen 3D games and benchmarks that flip the display image at or near display refresh rates.

4.6.5 Intel® Graphics Dynamic Frequency

Intel® Graphics Dynamic Frequency Technology is the ability of the processor and graphics cores to opportunistically increase frequency and/or voltage above the ensured processor and graphics frequency for the given part. Intel® Graphics Dynamic Frequency Technology is a performance feature that makes use of unused package power and thermals to increase application performance. The increase in frequency is determined by how much power and thermal budget is available in the package, and the application demand for additional processor or graphics performance. The processor core control is maintained by an embedded controller. The graphics driver dynamically adjusts between P-States to maintain optimal performance, power, and thermals. The graphics driver will always place the graphics engine in its lowest possible P-State; thereby, acting in the same capacity as Intel GPMT.

4.6.6 Display Power Savings Technology 6.0 (DPST)

This is a mobile only supported power management feature.

The Intel® DPST technique achieves backlight power savings while maintaining a good visual experience. This is accomplished by adaptively enhancing the displayed image while decreasing the backlight brightness simultaneously. The goal of this technique is to provide equivalent end-user-perceived image quality at a decreased backlight power level.

1. The original (input) image produced by the operating system or application is analyzed by the Intel® DPST subsystem. An interrupt to Intel® DPST software is generated whenever a meaningful change in the image attributes is detected. (A meaningful change is when the Intel® DPST software algorithm determines that enough brightness, contrast, or color change has occurred to the displaying images that the image enhancement and backlight control needs to be altered.)
2. Intel® DPST subsystem applies an image-specific enhancement to increase image contrast, brightness, and other attributes.
3. A corresponding decrease to the backlight brightness is applied simultaneously to produce an image with similar user-perceived quality (such as brightness) as the original image.

Intel® DPST 5.0 has improved the software algorithms and has minor hardware changes to better handle backlight phase-in and ensures the documented and validated method to interrupt hardware phase-in.

4.6.7 Automatic Display Brightness (ADB)

This is a mobile only supported power management feature.

Intel® Automatic Display Brightness feature dynamically adjusts the backlight brightness based upon the current ambient light environment. This feature requires an additional sensor to be on the panel front. The sensor receives the changing ambient light conditions and sends the interrupts to the Intel Graphics driver. As per the change in Lux, (current ambient light illuminance), the new backlight setting can be adjusted through BLC (see section 11). The converse applies for a brightly lit environment. Intel® Automatic Display Brightness increases the back light setting.

4.6.8 Intel® Seamless Display Refresh Rate Switching Technology (Intel® SDRRS Technology)

This is a mobile only supported power management feature.

When a Local Flat Panel (LFP) supports multiple refresh rates, the Intel® Display Refresh Rate Switching power conservation feature can be enabled. The higher refresh rate will be used when on plugged in power or when the end user has not selected/enabled this feature. The graphics software will automatically switch to a lower refresh rate for maximum battery life when the notebook is on battery power and when the user has selected/enabled this feature.

There are two distinct implementations of Intel® DRRS—static and seamless. The static Intel® Display Refresh Rate Switching Technology (Intel® DRRS Technology) method uses a mode change to assign the new refresh rate. The seamless Intel® Seamless Display Refresh Rate Switching Technology (Intel® SDRRS Technology) method is able to accomplish the refresh rate assignment without a mode change and therefore does not experience some of the visual artifacts associated with the mode change (SetMode) method.

4.7 Thermal Power Management

See Section 4.6 for all graphics thermal power management-related features.

§ §

5 Thermal Management

The thermal solution provides both the component-level and the system-level thermal management. To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed so that the processor:

- Remains below the maximum junction temperature ($T_{j,Max}$) specification at the maximum thermal design power (TDP).
- Conforms to system constraints, such as system acoustics, system skin-temperatures, and exhaust-temperature requirements.

Caution: Thermal specifications given in this chapter are on the component and package level and apply specifically to the 2nd Generation Intel® Core™ processor family mobile and Intel® Celeron® processor family mobile. Operating the processor outside the specified limits may result in permanent damage to the processor and potentially other components in the system.

5.1 Thermal Design Power (TDP) and Junction Temperature (Tj)

The processor TDP is the maximum sustained power that should be used for design of the processor thermal solution. TDP represents an expected maximum sustained power from realistic applications. TDP may be exceeded for short periods of time or if running a “power virus” workload. Due to Intel Turbo Boost Technology, applications are expected to run closer to TDP more often as the processor attempts to take advantage of available headroom in the platform to maximize performance.

The processor may also exceed the TDP for short durations after a period of lower power operation due to its turbo feature. This feature is intended to take advantage of available thermal capacitance in the thermal solution for momentary high power operation. The duration and time of such operation can be limited by platform runtime configurable registers within the processor.

The processor integrates multiple processor and graphics cores on a single die. This may result in differences in the power distribution across the die and must be considered when designing the thermal solution.

5.2 Thermal Considerations

Intel Turbo Boost Technology allows processor cores and Processor Graphics cores to run faster than the baseline frequency. During a turbo event, the processor can exceed its TDP power for brief periods. Turbo is invoked opportunistically and automatically as long as the processor is conforming to its temperature, power delivery, and current specification limits. Thus, thermal solutions and platform cooling that are designed to be less than thermal design guidance may experience thermal and performance issues since more applications will tend to run at or near the maximum power limit for significant periods of time.

5.2.1 Intel® Turbo Boost Technology Power Control and Reporting

When operating in the turbo mode, the processor will monitor its own power and adjust the turbo frequency to maintain the average power within limits over a thermally significant time period. The package, processor core, and graphic core powers are estimated using architectural counters and do not rely on any input from the platform.

The behavior of turbo is dictated by the following controls that are accessible using MSR, MMIO, or PECI interfaces:

- **POWER_LIMIT_1**: TURBO_POWER_LIMIT, MSR 610h, bits 14:0. This value sets the exponentially weighted moving average power limit over a long time period. This is normally aligned to the TDP of the part and steady-state cooling capability of the thermal solution. This limit may be set lower than TDP, real-time, for specific needs, such as responding to a thermal event. If set lower than TDP, the processor may not be able to honor this limit for all workloads since this control only applies in the turbo frequency range; a very high powered application may exceed POWER_LIMIT_1, even at non-turbo frequencies. The default value is the TDP for the SKU.
- **POWER_LIMIT_1_TIME**: TURBO _POWER_LIMIT, MSR 610h, bits 23:17. This value is a time parameter that adjusts the algorithm behavior. The exponentially weighted moving average turbo algorithm will use this parameter to maintain time averaged power at or below POWER_LIMIT_1. The default value is 1 second; however, 28 seconds is recommended for most mobile applications.
- **POWER_LIMIT_2**: TURBO_POWER_LIMIT, MSR 610h, bits 46:32. This value establishes the upper power limit of turbo operation above TDP, primarily for platform power supply considerations. Power may exceed this limit for up to 10 mS. The default for this limit is 1.25 x TDP.

The following considerations and limitations apply to the power monitoring feature:

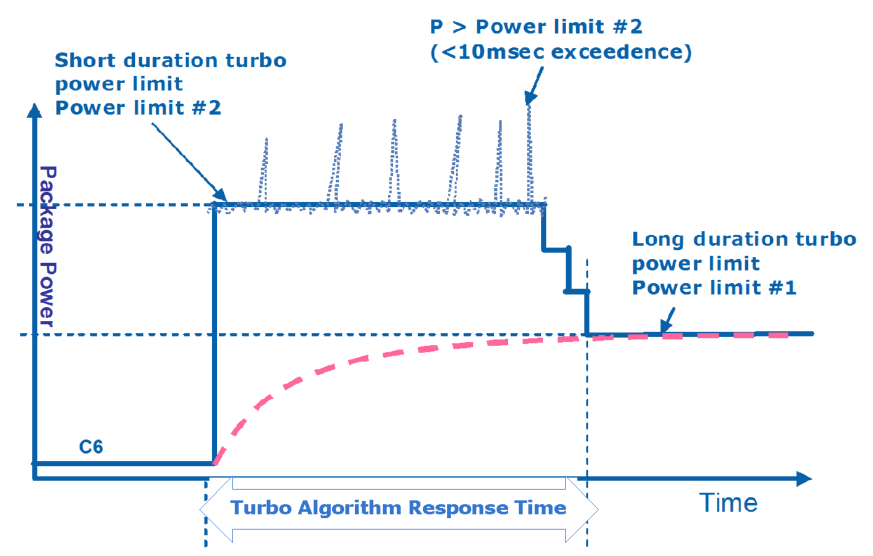
- Calibration applies to the processor family and is not conducted on a part-by-part basis. Therefore, some difference between actual and reported power may be observed.
- Power monitoring is calibrated with a variety of common, realistic workloads near Tj_max. Workloads with power characteristic markedly different from those used during the calibration process or lower temperatures may result in increased differences between actual and estimated power.
- In the event an uncharacterized workload or power “virus” application were to result in exceeding programmed power limits, the processor Thermal Control Circuitry (TCC) will protect the processor when properly enabled. Adaptive Thermal Monitor must be enabled for the processor to remain within specification.

Illustration of Intel Turbo Boost Technology power control is shown in the following sections and figures. Multiple controls operate simultaneously allowing for customization for multiple system thermal and power limitations. These controls allow for turbo optimizations within system constraints.

5.2.2 Package Power Control

The package power control allows for customization to implement optimal turbo within platform power delivery and package thermal solution limitations.

Figure 5-1. Package Power Control



5.2.3 Power Plane Control

The processor core and graphics core power plane controls allow for customization to implement optimal turbo within voltage regulator thermal limitations. It is possible to use these power plane controls to protect the voltage regulator from overheating due to extended high currents. Power limiting per plane cannot be ensured in all usages. This function is similar to the package level long duration window control.

5.2.4 Turbo Time Parameter

'Turbo Time Parameter' is a mathematical parameter (units in seconds) that controls the processor turbo algorithm using an exponentially weighted moving average of energy usage. During a maximum power turbo event of about 1.25 x TDP, the processor could sustain Power_Limit_2 for up to approximately 1.5 the Turbo Time Parameter. If the power value and/or ‘Turbo Time Parameter’ is changed during runtime, it may take a period of time (possibly up to approximately 3 to 5 times the ‘Turbo Time Parameter’, depending on the magnitude of the change and other factors) for the algorithm to settle at the new control limits.

5.3 Thermal and Power Specifications

The following notes apply to Table 5-1, Table 5-2, Table 5-3, and Table 5-4.

Notes	Description
1	The TDPs given are not the maximum power the processor can generate. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained periods of time.
2	TDP workload may consist of a combination of a CPU-core intensive and a graphics-core intensive applications.
3	The thermal solution needs to ensure that the processor temperature does not exceed the maximum junction temperature (Tj,max) limit, as measured by the DTS and the critical temperature bit.
4	The processor junction temperature is monitored by Digital Temperature Sensors (DTS). For DTS accuracy, refer to Section 5.4.1.2.1.
5	Digital Thermal Sensor (DTS) based fan speed control is required to achieve optimal thermal performance. Intel recommends full cooling capability well before the DTS reading reaches Tj,Max. An example of this is Tj,Max – 10 ºC.
6	The idle power specifications are not 100% tested. These power specifications are determined by the characterization at higher temperatures and extrapolating the values for the junction temperature indicated.
7	At Tj of Tj,max
8	At Tj of 50 ºC
9	At Tj of 35 ºC
10	Can be modified at runtime by MSR writes, with MMIO and with PECI commands
11	'Turbo Time Parameter' is a mathematical parameter (unit in seconds) that controls the processor turbo algorithm using a moving average of energy usage. Avoid setting the Turbo Time Parameter to a value less than 0.1 seconds. Refer to Section 5.2.4 for further information.
12	Shown limit is a time averaged power, based upon the Turbo Time Parameter. Absolute product power may exceed the set limits for short durations or under virus or uncharacterized workloads.
13	Processor will be controlled to specified power limit as described in Section 5.2.1. If the power value and/or 'Turbo Time Parameter' is changed during runtime, it may take a short period of time (approximately 3 to 5 times the 'Turbo Time Parameter') for the algorithm to settle at the new control limits.
14	This is a hardware default setting and not a behavioral characteristic of the part.
15	For controllable turbo workloads, the limit may be exceeded for up to 10 ms
16	Tjmax for some Dual Core SV SKUs in rPGA package will be 85 °C. Refer to Dear Customer Letters (DCLs) or contact your field representative to get details of SKUs that have Tjmax of 85 °C.

Table 5-1. Thermal Design Power (TDP) Specifications

Segment	State	CPU Core Frequency	Processor Graphics Core frequency	Thermal Design Power	Units	Notes
Extreme Edition (XE)	HFM	2.5 GHz up to 3.5 GHz	650 MHz up to 1300 MHz	55	W	1, 2, 7
	LFM	800 MHz	650 MHz up to 1300 MHz	36		
Quad Core SV	HFM	2.2 GHz up to 3.4 GHz	650 MHz up to 1300 MHz	45	W	1, 2, 7
	LFM	800 MHz	650 MHz up to 1300 MHz	33		
Dual Core SV	HFM	2.5 GHz up to 3.4 GHz	650 MHz up to 1300 MHz	35	W	1, 2, 7
	LFM	800 MHz	650 MHz up to 1300 MHz	26		
Low Voltage	HFM	2.1 GHz up to 3.2 GHz	500 MHz up to 1100 MHz	25	W	1, 2, 7
	LFM	800 MHz	500 MHz up to 1100 MHz	12		
Ultra Low Voltage	HFM	1.4 GHz up to 2.7 GHz	350 MHz up to 1000 MHz	17	W	1, 2, 7
	LFM	800 MHz	350 MHz up to 1000 MHz	10		

Table 5-2. Junction Temperature Specification

Segment	Symbol	Package Turbo Parameter	Min	Default	Max	Units	Notes
Extreme Edition (XE)	T_J	Junction temperature limit	0	—	100	°C	3, 4, 5,
Quad Core SV	T_J	Junction temperature limit	0	—	100	°C	3, 4, 5,
Dual Core SV	T_J	Junction temperature limit	0	—	100	°C	3, 4, 5, 16
Low Voltage	T_J	Junction temperature limit	0	—	100	°C	3, 4, 5
Ultra Low Voltage	T_J	Junction temperature limit	0	—	100	°C	3, 4, 5

Table 5-3. Package Turbo Parameters (Sheet 1 of 2)

Segment	Symbol	Package Turbo Parameter	Min	H/W Default	Max	Units	Notes
Extreme Edition (XE)	Turbo Time Parameter (package)	Processor turbo long duration time window (POWER_LIMIT_1_TIME in TURBO_POWER_LIMIT MSR 0610h bits [23:17])	N/A	1	N/A	s	10, 11, 14
	Long P (package)	'Long duration' turbo power limit (POWER_LIMIT_1 in TURBO_POWER_LIMIT MSR 0610h bits [14:0])	N/A	55	N/A	W	10,12,13, 14
	Short P (package)	'Short duration' turbo power limit (POWER_LIMIT_2 in TURBO_POWER_LIMIT MSR 0610h bits [46:32])	N/A	1.25 x 55	N/A	W	10, 14, 15

Table 5-3. Package Turbo Parameters (Sheet 2 of 2)

Segment	Symbol	Package Turbo Parameter	Min	H/W Default	Max	Units	Notes
Quad Core SV	Turbo Time Parameter (package)	Processor turbo long duration time window (POWER_LIMIT_1_TIME in TURBO_POWER_LIMIT MSR 0610h bits [23:17])	0.001	1	64	S	10, 11, 14
	Long P (package)	'Long duration' turbo power limit (POWER_LIMIT_1 in TURBO_POWER_LIMIT MSR 0610h bits [14:0])	40	45	48	W	10,12,13, 14
	Short P (package)	'Short duration' turbo power limit (POWER_LIMIT_2 in TURBO_POWER_LIMIT MSR 0610h bits [46:32])	40	1.25 x 45	60	W	10, 14, 15
Dual Core SV	Turbo Time Parameter (package)	Processor turbo long duration time window (POWER_LIMIT_1_TIME in TURBO_POWER_LIMIT MSR 0610h bits [23:17])	0.001	1	64	S	10, 11, 14
	Long P (package)	'Long duration' turbo power limit (POWER_LIMIT_1 in TURBO_POWER_LIMIT MSR 0610h bits [14:0])	28	35	36	W	10, 12, 13, 14
	Short P (package)	'Short duration' turbo power limit (POWER_LIMIT_2 in TURBO_POWER_LIMIT MSR 0610h bits [46:32])	28	1.25 x 35	44	W	10, 14, 15
Low Voltage	Turbo Time Parameter (package)	Processor turbo long duration time window (POWER_LIMIT_1_TIME in TURBO_POWER_LIMIT MSR 0610h bits [23:17])	0.001	1	32	S	10, 11, 14
	Long P (package)	'Long duration' turbo power limit (POWER_LIMIT_1 in TURBO_POWER_LIMIT MSR 0610h bits [14:0])	24	25	28	W	10, 12, 13, 14
	Short P (package)	'Short duration' turbo power limit (POWER_LIMIT_2 in TURBO_POWER_LIMIT MSR 0610h bits [46:32])	24	1.25 x 25	36	W	10, 14, 15
Ultra Low Voltage	Turbo Time Parameter (package)	Processor turbo long duration time window (POWER_LIMIT_1_TIME in TURBO_POWER_LIMIT MSR 0610h bits [23:17])	0.001	1	32	S	10,11,14
	Long P (package)	'Long duration' turbo power limit (POWER_LIMIT_1 in TURBO_POWER_LIMIT MSR 0610h bits [14:0])	—	17	—	W	10,12, 13, 14
	Short P (package)	'Short duration' turbo power limit (POWER_LIMIT_2 in TURBO_POWER_LIMIT MSR 0610h bits [46:32])	—	1.25 x 17	—	W	10,14,15

Table 5-4. Idle Power Specifications

Segment	Symbol	Idle Parameter	Min	Typ	Max	Units	Notes
Extreme Edition (XE)	P_{C1E}	Idle power in the Package C1e state	—	—	12.5	W	6, 8
	P_{C6}	Idle power in the Package C6 state	—	—	4	W	6, 9
	P_{C7}	Idle power in the Package C7state	—	—	3.85	W	6, 9
Quad Core SV	P_{C1E}	Idle power in the Package C1e state	—	—	11	W	6, 8
	P_{C6}	Idle power in the Package C6 state	—	—	3.9	W	6, 9
	P_{C7}	Idle power in the Package C7state	—	—	3.8	W	6, 9
Dual Core SV	P_{C1E}	Idle power in the Package C1e state	—	—	8.8	W	6, 8
	P_{C6}	Idle power in the Package C6 state	—	—	3.1	W	6, 9
	P_{C7}	Idle power in the Package C7state	—	—	2.95	W	6, 9
Low Voltage	P_{C1E}	Idle power in the Package C1e state	—	—	6.4	W	6, 8
	P_{C6}	Idle power in the Package C6 state	—	—	2.5	W	6, 9
	P_{C7}	Idle power in the Package C7state	—	—	2.35	W	6, 9
Ultra Low Voltage	P_{C1E}	Idle power in the Package C1e state	—	—	5.8	W	6, 8
	P_{C6}	Idle power in the Package C6 state	—	—	2.3	W	6, 9
	P_{C7}	Idle power in the Package C7state	—	—	2.2	W	6, 9

5.4 Thermal Management Features

This section covers thermal management features for the processor.

5.4.1 Processor Package Thermal Features

This section covers thermal management features for the entire processor complex (including the processor core, the graphics core, and integrated memory controller hub), and will be referred to as processor package, or by simply the package.

Occasionally the package will operate in conditions that exceed its maximum allowable operating temperature. This can be due to internal overheating or due to overheating in the entire system. To protect itself and the system from thermal failure, the package is capable of reducing its power consumption and thereby its temperature to attempt to remain within normal operating limits using the Adaptive Thermal Monitor.

The Adaptive Thermal Monitor can be activated when any package temperature, monitored by a digital thermal sensor (DTS), meets or exceeds its maximum junction temperature specification ($T_{J,max}$) and asserts PROCHOT#. The thermal control circuit (TCC) can be activated prior to $T_{J,max}$ by use of the TCC activation offset. The assertion of PROCHOT# activates the thermal control circuit (TCC), and causes both the processor core and graphics core to reduce frequency and voltage adaptively. The TCC will remain active as long as any package temperature exceeds its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated.

Note: Adaptive Thermal Monitor protection is always enabled.

5.4.1.1 Adaptive Thermal Monitor

The purpose of the Adaptive Thermal Monitor is to reduce processor core power consumption and temperature until it operates at or below its maximum operating temperature (according for TCC activation offset). Processor core power reduction is achieved by:

- Adjusting the operating frequency (using the core ratio multiplier) and input voltage (using the SVID bus).
- Modulating (starting and stopping) the internal processor core clocks (duty cycle).

The temperature at which the Adaptive Thermal Monitor activates the Thermal Control Circuit is factory calibrated and is not user configurable. The default value is software visible in the TEMPERATURE_TARGET (1A2h) MSR, Bits 23:16. The Adaptive Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines. The Adaptive Thermal Monitor is not intended as a mechanism to maintain processor TDP. The system design should provide a thermal solution that can maintain TDP within its intended usage range.

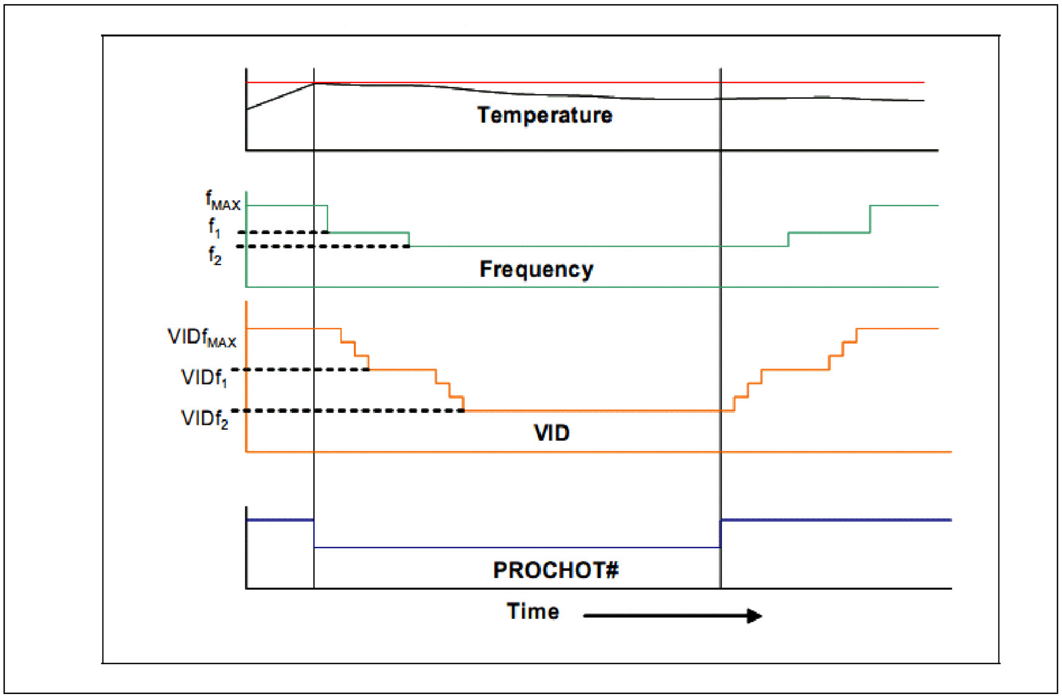
5.4.1.1.1 Frequency / Voltage Control

Upon TCC activation, the processor core attempts to dynamically reduce processor core power by lowering the frequency and voltage operating point. The operating points are automatically calculated by the processor core itself and do not require the BIOS to program them as with previous generations of Intel processors. The processor core will scale the operating points such that:

- The voltage will be optimized according to the temperature, the core bus ratio, and number of cores in deep C-states.
- The core power and temperature are reduced while minimizing performance degradation.

A small amount of hysteresis has been included to prevent an excessive amount of operating point transitions when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature the operating frequency and voltage will transition back to the normal system operating point. This is illustrated in Figure 5-2.

Figure 5-2. Frequency and Voltage Ordering



Once a target frequency/bus ratio is resolved, the processor core will transition to the new target automatically.

- On an upward operating point transition, the voltage transition precedes the frequency transition.
- On a downward transition, the frequency transition precedes the voltage transition.

When transitioning to a target core operating voltage, a new VID code to the voltage regulator is issued. The voltage regulator must support dynamic VID steps to support this method.

During the voltage change:

- It will be necessary to transition through multiple VID steps to reach the target operating voltage.
- Each step is 5 mV for Intel MVP-7.0 compliant VRs.
- The processor continues to execute instructions. However, the processor will halt instruction execution for frequency transitions.

If a processor load-based Enhanced Intel SpeedStep Technology / P-state transition (through MSR write) is initiated while the Adaptive Thermal Monitor is active, there are two possible outcomes:

- If the P-state target frequency is higher than the processor core optimized target frequency, the p-state transition will be deferred until the thermal event has been completed.
- If the P-state target frequency is lower than the processor core optimized target frequency, the processor will transition to the P-state operating point.

5.4.1.1.2 Clock Modulation

If the frequency/voltage changes are unable to end an Adaptive Thermal Monitor event, the Adaptive Thermal Monitor will use clock modulation. Clock modulation is done by alternately turning the clocks off and on at a duty cycle (ratio between clock "on" time and total time) specific to the processor. The duty cycle is factory configured to 25% on and 75% off and cannot be modified. The period of the duty cycle is configured to 32 microseconds when the TCC is active. Cycle times are independent of processor frequency. A small amount of hysteresis has been included to prevent excessive clock modulation when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases. Clock modulation is automatically engaged as part of the TCC activation when the frequency/voltage targets are at their minimum settings. Processor performance will be decreased by the same amount as the duty cycle when clock modulation is active. Snooping and interrupt processing are performed in the normal manner while the TCC is active.

5.4.1.2 Digital Thermal Sensor

Each processor execution core has an on-die Digital Thermal Sensor (DTS) that detects the core's instantaneous temperature. The DTS is the preferred method of monitoring processor die temperature because:

- It is located near the hottest portions of the die.
- It can accurately track the die temperature and ensure that the Adaptive Thermal Monitor is not excessively activated.

Temperature values from the DTS can be retrieved through:

- A software interface using processor Model Specific Register (MSR).
- A processor hardware interface as described in Section 5.4.4.

Note: When temperature is retrieved by processor MSR, it is the instantaneous temperature of the given core. When temperature is retrieved using PECI, it is the average of the highest DTS temperature in the package over a 256 ms time window. Intel recommends using the PECI reported temperature for platform thermal control that benefits from averaging, such as fan speed control. The average DTS temperature may not be a good indicator of package Adaptive Thermal Monitor activation or rapid increases in temperature that triggers the Out of Specification status bit within the PACKAGE_THERM_STATUS MSR 01B1h and IA32_THERM_STATUS MSR 19Ch.

Code execution is halted in C1–C7. Therefore, temperature cannot be read using the processor MSR without bringing a core back into C0. However, temperature can still be monitored through PECI in lower C-states except for C7.

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor ($T_{j,max}$), regardless of TCC activation offset. It is the responsibility of software to convert the relative temperature to an absolute temperature. The absolute reference temperature is readable in the TEMPERATURE_TARGET MSR 1A2h. The temperature returned by the DTS is an implied negative integer indicating the relative offset from $T_{j,max}$. The DTS does not report temperatures greater than $T_{j,max}$.

The DTS-relative temperature readout directly impacts the Adaptive Thermal Monitor trigger point. When a package DTS indicates that it has reached the TCC activation (a reading of 0h, except when the TCC activation offset is changed), the TCC will activate and indicate a Adaptive Thermal Monitor event. A TCC activation will lower both IA core and graphics core frequency, voltage or both.

Changes to the temperature can be detected using two programmable thresholds located in the processor thermal MSRs. These thresholds have the capability of generating interrupts using the core's local APIC. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.

5.4.1.2.1 Digital Thermal Sensor Accuracy (Taccuracy)

The error associated with DTS measurement will not exceed ±5 °C at Tj,max. The DTS measurement within the entire operating range will meet a ±5 °C accuracy.

5.4.1.3 PROCHOT# Signal

PROCHOT# (processor hot) is asserted when the processor core temperature has reached its maximum operating temperature ($T_{j,max}$). See Figure 5-2 for a timing diagram of the PROCHOT# signal assertion relative to the Adaptive Thermal Response. Only a single PROCHOT# pin exists at a package level. When any core arrives at the TCC activation point, the PROCHOT# signal will be asserted. PROCHOT# assertion policies are independent of Adaptive Thermal Monitor enabling.

Note: Bus snooping and interrupt latching are active while the TCC is active.

5.4.1.3.1 Bi-Directional PROCHOT#

By default, the PROCHOT# signal is defined as an output only. However, the signal may be configured as bi-directional. When configured as a bi-directional signal, PROCHOT# can be used for thermally protecting other platform components should they overheat as well. When PROCHOT# is driven by an external device:

- the package will immediately transition to the minimum operation points (voltage and frequency) supported by the processor and graphics cores. This is contrary to the internally-generated Adaptive Thermal Monitor response.
- Clock modulation is not activated.

The TCC will remain active until the system de-asserts PROCHOT#. The processor can be configured to generate an interrupt upon assertion and de-assertion of the PROCHOT# signal.

Note: Toggling PROCHOT# more than once in 1.5ms period will result in constant Pn state of the processor.

5.4.1.3.2 Voltage Regulator Protection

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR will cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target thermal design current (I_{CCTDC}) instead of maximum current. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. Overall, the system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP.

5.4.1.3.3 Thermal Solution Design and PROCHOT# Behavior

With a properly designed and characterized thermal solution, it is anticipated that PROCHOT# will only be asserted for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable.

However, an under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may:

- Cause a noticeable performance loss.
- Result in prolonged operation at or above the specified maximum junction temperature and affect the long-term reliability of the processor.
- May be incapable of cooling the processor even when the TCC is active continuously (in extreme situations).

5.4.1.3.4 Low-Power States and PROCHOT# Behavior

If the processor enters a low-power package idle state such as C3 or C6/C7 with PROCHOT# asserted, PROCHOT# will remain asserted until:

- The processor exits the low-power state
- The processor junction temperature drops below the thermal trip point.

For the package C7 state, PROCHOT# may de-assert for the duration of C7 state residency even if the processor enters the idle state operating at the TCC activation temperature. The PECI interface is fully operational during all C-states and it is expected that the platform continues to manage processor (“package”) core thermals even during idle states by regularly polling for thermal data over PECI.

5.4.1.3.5 THERMTRIP# Signal

Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the package will automatically shut down when the silicon has reached an elevated temperature that risks physical damage to the product. At this point the THERMTRIP# signal will go active.

5.4.1.3.6 Critical Temperature Detection

Critical Temperature detection is performed by monitoring the package temperature. This feature is intended for graceful shutdown before the THERMTRIP# is activated; however, the processor execution is not ensured between critical temperature and THERMTRIP#. If the package's Adaptive Thermal Monitor is triggered and the temperature remains high, a critical temperature status and sticky bit are latched in the PACKAGE_THERM_STATUS MSR 1B1h and also generates a thermal interrupt if enabled. For more details on the interrupt mechanism, refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals.*

5.4.2 Processor Core Specific Thermal Features

5.4.2.1 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption using clock modulation. This mechanism is referred to as "On-Demand" mode and is distinct from Adaptive Thermal Monitor and bi-directional PROCHOT#. The processor platforms must not rely on software usage of this mechanism to limit the processor temperature. On-Demand Mode can be done using processor MSR or chipset I/O emulation.

On-Demand Mode may be used in conjunction with the Adaptive Thermal Monitor. However, if the system software tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode. If the I/O based and MSR-based On-Demand modes are in conflict, the duty cycle selected by the I/O emulation-based On-Demand mode will take precedence over the MSR-based On-Demand Mode.

5.4.2.1.1 MSR Based On-Demand Mode

If Bit 4 of the IA32_CLOCK_MODULATION MSR is set to a 1, the processor will immediately reduce its power consumption using modulation of the internal core clock, independent of the processor temperature. The duty cycle of the clock modulation is programmable using Bits 3:1 of the same IA32_CLOCK_MODULATION MSR. In this mode, the duty cycle can be programmed in either 12.5% or 6.25% increments (discoverable using CPU ID). Thermal throttling using this method will modulate each processor core's clock independently.

5.4.2.1.2 I/O Emulation-Based On-Demand Mode

I/O emulation-based clock modulation provides legacy support for operating system software that initiates clock modulation through I/O writes to ACPI defined processor clock control registers on the chipset (PROC_CNT). Thermal throttling using this method will modulate all processor cores simultaneously.

5.4.3 Memory Controller Specific Thermal Features

The memory controller provides the ability to initiate memory throttling based upon memory temperature. The memory temperature can be provided to the memory controller using PECI or can be estimated by the memory controller based upon memory activity. The temperature trigger points are programmable by memory mapped IO registers.

5.4.3.1 Programmable Trip Points

This memory controller provides programmable critical, hot and warm trip points. Crossing a critical trip point forces a system shutdown. Crossing a hot or warm trip point will initiate throttling. The amount of memory throttle at each trip point is programmable.

5.4.4 Platform Environment Control Interface (PECI)

The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices. The processor implements a PECI interface to allow communication of processor thermal information to other devices on the platform. The processor provides a digital thermal sensor (DTS) for fan speed control. The DTS is calibrated at the factory to provide a digital representation of relative processor temperature. Averaged DTS values are read using the PECI interface.

The PECI physical layer is a self-clocked one-wire bus that begins each bit with a driven, rising edge from an idle level near zero volts. The duration of the signal driven high depends on whether the bit value is a Logic 0 or Logic 1. PECI also includes variable data transfer rate established with every message. The single wire interface provides low board routing overhead for the multiple load connections in the congested routing area near the processor and chipset components. Bus speed, error checking, and low protocol overhead provides adequate link bandwidth and reliability to transfer critical device operating conditions and configuration information.

5.4.4.1 Fan Speed Control with Digital Thermal Sensor

Digital Thermal Sensor based fan speed control (T_{FAN}) is a recommended feature to achieve optimal thermal performance. At the T_{FAN} temperature, Intel recommends full cooling capability well before the DTS reading reaches $T_{j,max}$. An example of this would be $T_{FAN} = T_{j,max} - 10$ ºC.

§ §

6 Signal Description

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The following notations are used to describe the signal type.

Notations	Signal Type
I	Input Pin
O	Output Pin
I/O	Bi-directional Input/Output Pin

The signal description also includes the type of buffer used for the particular signal (see Table 6-1).

Table 6-1. Signal Description Buffer Types

Signal	Description
PCI Express*	PCI Express interface signals. These signals are compatible with PCI Express* 2.0 Signalling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Refer to the PCIe specification.
eDP	Embedded Display Port interface signals. These signals are compatible with VESA Revision 1.0 DP specifications and the interface is AC coupled. The buffers are not 3.3-V tolerant.
FDI	Intel Flexible Display interface signals. These signals are based on PCI Express* 2.0 Signaling Environment AC Specifications (2.7 GT/s), but are DC coupled. The buffers are not 3.3-V tolerant.
DMI	Direct Media Interface signals. These signals are based on PCI Express* 2.0 Signaling Environment AC Specifications (5 GT/s), but are DC coupled. The buffers are not 3.3-V tolerant.
CMOS	CMOS buffers. 1.1-V tolerant
DDR3	DDR3 buffers: 1.5-V tolerant
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation
Ref	Voltage reference signal
Asynchronous[1]	Signal has no timing relationship with any reference clock.

Notes:

1. Qualifier for a buffer type.

6.1 System Memory Interface Signals

Table 6-2. Memory Channel A Signals

Signal Name	Description	Direction/ Buffer Type
SA_BS[2:0]	**Bank Select:** These signals define which banks are selected within each SDRAM rank.	O DDR3
SA_WE#	**Write Enable Control Signal:** This signal is used with SA_RAS# and SA_CAS# (along with SA_CS#) to define the SDRAM Commands.	O DDR3
SA_RAS#	**RAS Control Signal:** This signal is used with SA_CAS# and SA_WE# (along with SA_CS#) to define the SRAM Commands.	O DDR3
SA_CAS#	**CAS Control Signal:** This signal is used with SA_RAS# and SA_WE# (along with SA_CS#) to define the SRAM Commands.	O DDR3
SA_DQS[7:0] SA_DQS#[7:0]	**Data Strobes:** SA_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS[7:0] and its SA_DQS#[7:0] during read and write transactions.	I/O DDR3
SA_DQ[63:0]	**Data Bus:** Channel A data signal interface to the SDRAM data bus.	I/O DDR3
SA_MA[15:0]	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.	O DDR3
SA_CK[1:0]	**SDRAM Differential Clock:** Channel A SDRAM Differential clock signal pair. The crossing of the positive edge of SA_CK and the negative edge of its complement SA_CK# are used to sample the command and control signals on the SDRAM.	O DDR3
SA_CK#[1:0]	**SDRAM Inverted Differential Clock:** Channel A SDRAM Differential clock signal-pair complement.	O DDR3
SA_CKE[1:0]	**Clock Enable:** (1 per rank). These signals are used to: • Initialize the SDRAMs during power-up • Power-down SDRAM ranks • Place all SDRAM ranks into and out of self-refresh during STR	O DDR3
SA_CS#[1:0]	**Chip Select:** (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O DDR3
SA_ODT[1:0]	**On Die Termination:** Active Termination Control.	O DDR3

Table 6-3. Memory Channel B Signals

Signal Name	Description	Direction/ Buffer Type
SB_BS[2:0]	**Bank Select:** These signals define which banks are selected within each SDRAM rank.	O DDR3
SB_WE#	**Write Enable Control Signal:** This signal is used with SB_RAS# and SB_CAS# (along with SB_CS#) to define the SDRAM Commands.	O DDR3
SB_RAS#	**RAS Control Signal:** This signal is used with SB_CAS# and SB_WE# (along with SB_CS#) to define the SRAM Commands.	O DDR3
SB_CAS#	**CAS Control Signal:** This signal is used with SB_RAS# and SB_WE# (along with SB_CS#) to define the SRAM Commands.	O DDR3
SB_DQS[7:0] SB_DQS#[7:0]	**Data Strobes:** SB_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQS[8:0] and its SB_DQS#[7:0] during read and write transactions.	I/O DDR3
SB_DQ[63:0]	**Data Bus:** Channel B data signal interface to the SDRAM data bus.	I/O DDR3
SB_MA[15:0]	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.	O DDR3
SB_CK[1:0]	**SDRAM Differential Clock:** Channel B SDRAM Differential clock signal pair. The crossing of the positive edge of SB_CK and the negative edge of its complement SB_CK# are used to sample the command and control signals on the SDRAM.	O DDR3
SB_CK#[1:0]	**SDRAM Inverted Differential Clock:** Channel B SDRAM Differential clock signal-pair complement.	O DDR3
SB_CKE[1:0]	**Clock Enable:** (1 per rank). These signals are used to: • Initialize the SDRAMs during power-up. • Power-down SDRAM ranks. • Place all SDRAM ranks into and out of self-refresh during STR.	O DDR3
SB_CS#[1:0]	**Chip Select:** (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O DDR3
SB_ODT[1:0]	**On Die Termination:** Active Termination Control.	O DDR3

6.2 Memory Reference and Compensation Signals

Table 6-4. Memory Reference and Compensation

Signal Name	Description	Direction/ Buffer Type
SM_RCOMP[2:0]	**System Memory Impedance Compensation:**	I A
SM_VREF	**DDR3 Reference Voltage:** This provides reference voltage to the DDR3 interface and is defined as $V_{DDQ}/2$.	I A

6.3 Reset and Miscellaneous Signals

Table 6-5. Reset and Miscellaneous Signals

Signal Name	Description	Direction/ Buffer Type
CFG[17:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. • **CFG[1:0]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal — 1 = Normal operation — 0 = Lane numbers reversed • **CFG[3]:** Reserved • **CFG[4]:** eDP enable — 1 = Disabled — 0 = Enabled • **CFG[6:5]:** PCI Express Bifurcation — 00 = 1 x8, 2 x4 PCI Express — 01 = Reserved — 10 = 2 x8 PCI Express — 11 = 1 x16 PCI Express • **CFG[17:7]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I CMOS
PM_SYNC	**Power Management Sync**: A sideband signal to communicate power management status from the platform to the processor.	I CMOS
RESET#	Platform Reset pin driven by the PCH	I CMOS
RSVD RSVD_TP RSVD_NCTF	**RESERVED:** All signals that are RSVD and RSVD_NCTF must be left unconnected on the board. However, Intel recommends that all RSVD_TP signals have using test points.	No Connect Test Point Non-Critical to Function
SM_DRAMRST#	**DDR3 DRAM Reset:** Reset signal from processor to DRAM devices. One common to all channels.	O CMOS

6.4 PCI Express*-Based Interface Signals

Table 6-6. PCI Express* Graphics Interface Signals

Signal Name	Description	Direction/ Buffer Type
PEG_ICOMPI	**PCI Express Input Current Compensation**	I A
PEG_ICOMPO	**PCI Express Current Compensation**	I A
PEG_RCOMPO	**PCI Express Resistance Compensation**	I A
PEG_RX[15:0] PEG_RX#[15:0]	**PCI Express Receive Differential Pair**	I PCI Express
PEG_TX[15:0] PEG_TX#[15:0]	**PCI Express Transmit Differential Pair**	O PCI Express

6.5 Embedded DisplayPort* (eDP) Signals

Table 6-7. Embedded DisplayPort* Signals

Signal Name	Description	Direction/ Buffer Type
eDP_TX[3:0] eDP_TX#[3:0]	**Embedded DisplayPort Transmit Differential Pair**	O Diff
eDP_AUX eDP_AUX#	**Embedded DisplayPort Auxiliary Differential Pair**	I/O Diff
eDP_HPD#	**Embedded DisplayPort Hot Plug Detect:**	I Asynchronous CMOS
eDP_COMPIO	**Embedded DisplayPort Current Compensation**	I A
eDP_ICOMPO	**Embedded DisplayPort Current Compensation**	I A

6.6 Intel® Flexible Display Interface (Intel® FDI) Signals

Table 6-8. Intel® Flexible Display Interface (Intel® FDI)

Signal Name	Description	Direction/ Buffer Type
FDI0_TX[3:0] FDI0_TX#[3:0]	**Intel® Flexible Display Interface Transmit Differential Pair** – Pipe A	O FDI
FDI0_FSYNC[0]	**Intel® Flexible Display Interface Frame Sync** – Pipe A	I CMOS
FDI0_LSYNC[0]	**Intel® Flexible Display Interface Line Sync** – Pipe A	I CMOS
FDI1_TX[3:0] FD1I_TX#[3:0]	**Intel® Flexible Display Interface Transmit Differential Pair** – Pipe B	O FDI
FDI1_FSYNC[1]	**Intel® Flexible Display Interface Frame Sync** – Pipe B	I CMOS
FDI1_LSYNC[1]	**Intel® Flexible Display Interface Line Sync** – Pipe B	I CMOS
FDI_INT	**Intel® Flexible Display Interface Hot Plug Interrupt**	I Asynchronous CMOS

6.7 Direct Media Interface (DMI) Signals

Table 6-9. Direct Media Interface (DMI) Signals – Processor to PCH Serial Interface

Signal Name	Description	Direction/ Buffer Type
DMI_RX[3:0] DMI_RX#[3:0]	**DMI Input from PCH:** Direct Media Interface receive differential pair.	I DMI
DMI_TX[3:0] DMI_TX#[3:0]	**DMI Output to PCH:** Direct Media Interface transmit differential pair.	O DMI

6.8 Phase Lock Loop (PLL) Signals

Table 6-10. Phase Lock Loop (PLL) Signals

Signal Name	Description	Direction/ Buffer Type
BCLK BCLK#	Differential bus clock input to the processor	I Diff Clk
DPLL_REF_CLK **DPLL_REF_CLK#**	Embedded Display Port PLL Differential Clock In: 120 MHz.	I Diff Clk

6.9 Test Access Points (TAP) Signals

Table 6-11. Test Access Points (TAP) Signals

Signal Name	Description	Direction/ Buffer Type
BPM#[7:0]	**Breakpoint and Performance Monitor Signals:** These signals are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O CMOS
BCLK_ITP BCLK_ITP#	These pins are connected in parallel to the top side debug probe to enable debug capacities.	I
DBR#	DBR# is used only in systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset.	O
PRDY#	PRDY# is a processor output used by debug tools to determine processor debug readiness.	O Asynchronous CMOS
PREQ#	PREQ# is used by debug tools to request debug operation of the processor.	I Asynchronous CMOS
TCK	**TCK (Test Clock):** This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). TCK must be driven low or allowed to float during power on Reset.	I CMOS
TDI	**TDI (Test Data In):** This signal transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.	I CMOS
TDO	**TDO (Test Data Out):** This signal transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.	O Open Drain
TMS	**TMS (Test Mode Select):** A JTAG specification support signal used by debug tools.	I CMOS
TRST#	**TRST# (Test Reset):** This signal resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.	I CMOS

6.10 Error and Thermal Protection Signals

Table 6-12. Error and Thermal Protection Signals (Sheet 1 of 2)

Signal Name	Description	Direction/ Buffer Type
CATERR#	**Catastrophic Error:** This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this for non-recoverable machine check errors or other unrecoverable internal errors. On the processor, CATERR# is used for signaling the following types of errors: • Legacy MCERRs – CATERR# is asserted for 16 BCLKs. • Legacy IERRs – CATERR# remains asserted until warm or cold reset.	O CMOS
PECI	**PECI (Platform Environment Control Interface):** A serial sideband interface to the processor, it is used primarily for thermal, power, and error management.	I/O Asynchronous
PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	CMOS Input/ Open-Drain Output

Table 6-12. Error and Thermal Protection Signals (Sheet 2 of 2)

Signal Name	Description	Direction/ Buffer Type
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin.	O Asynchronous CMOS

6.11 Power Sequencing Signals

Table 6-13. Power Sequencing Signals

Signal Name	Description	Direction/ Buffer Type
SM_DRAMPWROK	**SM_DRAMPWROK Processor Input:** Connects to PCH DRAMPWROK.	I Asynchronous CMOS
UNCOREPWRGOOD	The processor requires this input signal to be a clean indication that the V_{CCSA}, V_{CCIO}, V_{AXG}, and V_{DDQ}, power supplies are stable and within specifications. This requirement applies, regardless of the S-state of the processor. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. This is connected to the PCH PROCPWRGD signal.	I Asynchronous CMOS
SKTOCC# **(rPGA only)** **PROC_DETECT# (BGA)**	**SKTOCC# (Socket Occupied)/PROC_DETECT (Processor Detect):** Pulled down directly (0 Ohms) on the processor package to ground. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.	

6.12 Processor Power Signals

Table 6-14. Processor Power Signals (Sheet 1 of 2)

Signal Name	Description	Direction/ Buffer Type
VCC	Processor core power rail	Ref
VCCIO	Processor power for I/O	Ref
VDDQ	Processor I/O supply voltage for DDR3	Ref
VAXG	Graphics core power supply.	Ref
VCCPLL	VCCPLL provides isolated power for internal processor PLLs	Ref
VCCSA	System Agent power supply	Ref
VCCPQE (BGA Only)	Filtered, low noise derivative of VCCIO	Ref

Table 6-14. Processor Power Signals (Sheet 2 of 2)

Signal Name	Description	Direction/ Buffer Type
VCCDQ (BGA Only)	Filtered, low noise derivative of VDDQ	Ref
VIDSOUT VIDSCLK VIDALERT#	VIDALERT#, VIDSCLK, and VIDSCLK comprise a three signal serial synchronous interface used to transfer power management information between the processor and the voltage regulator controllers. This serial VID interface replaces the parallel VID interface on previous processors.	I/O O I CMOS
VCCSA_VID[1]	**Voltage selection for VCCSA**: This pin must have a pull down resistor to ground.	O CMOS

6.13 Sense Signals

Table 6-15. Sense Signals

Signal Name	Description	Direction/ Buffer Type
VCC_SENSE VSS_SENSE	VCC_SENSE and VSS_SENSE provide an isolated, low impedance connection to the processor core voltage and ground. They can be used to sense or measure voltage near the silicon.	O Analog
VAXG_SENSE VSSAXG_SENSE	VAXG_SENSE and VSSAXG_SENSE provide an isolated, low impedance connection to the V_{AXG} voltage and ground. They can be used to sense or measure voltage near the silicon.	O Analog
VCCIO_SENSE VSS_SENSE_VCCIO	VCCIO_SENSE and VSS_SENSE_VCCIO provide an isolated, low impedance connection to the processor V_{CCIO} voltage and ground. They can be used to sense or measure voltage near the silicon.	O Analog
VDDQ_SENSE VSS_SENSE_VDDQ	VDDQ_SENSE and VSS_SENSE_VDDQ provides an isolated, low impedance connection to the V_{DDQ} voltage and ground. They can be used to sense or measure voltage near the silicon.	O Analog
VCCSA_SENSE	VCCSA_SENSE provide an isolated, low impedance connection to the processor system agent voltage. It can be used to sense or measure voltage near the silicon.	O Analog
VCC_DIE_SENSE	**Die Validation Sense:**	O Analog
VCC_VAL_SENSE VSS_VAL_SENSE	**V_{CC} Validation Sense:**	O Analog
VAXG_VAL_SENSE VSSAXG_VAL_SENSE	**V_{AXG} Validation Sense:**	O Analog

6.14 Ground and Non-Critical to Function (NCTF) Signals

Table 6-16. Ground and Non-Critical to Function (NCTF) Signals

Signal Name	Description	Direction/ Buffer Type
VSS	Processor ground node	GND
VSS_NCTF (BGA Only)	**Non-Critical to Function:** These pins are for package mechanical reliability.	
DC_TEST_xx#	**Daisy Chain-** These pins are for solder joint reliability and non-critical to function. For BGA only.	

6.15 Future Compatibility Signals

Table 6-17. Future Compatibility Signals

Signal Name	Description	Direction/ Buffer Type
PROC_SELECT#	This pin is for compatibility with future platforms. A pull-up resistor to V_{CPLL} is required if connected to the DF_TVS strap on the PCH.	
SA_DIMM_VREFDQ SB_DIMM_VREFDQ	**Memory Channel A/B DIMM DQ Voltage Reference:** These signals are not used by the processors and are for future compatibility only. No connection is required.	
VCCIO_SEL	**Voltage selection for VCCIO**: This pin must be pulled high on the motherboard, when using dual rail voltage regulator, which will be used for future compatibility.	
VCCSA_VID[0]	**Voltage selection for VCCSA**: This pin must have a pull down resistor to ground.	

6.16 Processor Internal Pull-Up / Pull-Down Resistors

Table 6-18. Processor Internal Pull-Up / Pull-Down Resistors

Signal Name	Pull-Up / Pull-Down	Rail	Value
BPM[7:0]	Pull Up	VCCIO	65–165 Ω
PRDY#	Pull Up	VCCIO	65–165 Ω
PREQ#	Pull Up	VCCIO	65–165 Ω
TCK	Pull Down	VSS	5–15 kΩ
TDI	Pull Up	VCCIO	5–15 kΩ
TMS	Pull Up	VCCIO	5–15 kΩ
TRST#	Pull Up	VCCIO	5–15 kΩ
CFG[17:0]	Pull Up	VCCIO	5–15 kΩ

§ §

7 Electrical Specifications

7.1 Power and Ground Pins

The processor has VCC, VCCIO, VDDQ, VCCPLL, VCCSA, VAXG and VSS (ground) inputs for on-chip power distribution. All power pins must be connected to their respective processor power planes, while all VSS pins must be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop. The VCC pins and VAXG pins must be supplied with the voltage determined by the processor **S**erial **V**oltage **ID**entification (SVID) interface. Table 7-1 specifies the voltage level for the various VIDs.

7.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low- and full-power states. To keep voltages within specification, output decoupling must be properly designed.

Caution: Design the board to ensure that the voltage provided to the processor remains within the specifications listed in Table 7-3. Failure to do so can result in timing violations or reduced lifetime of the processor.

7.2.1 Voltage Rail Decoupling

The voltage regulator solution must:

- provide sufficient decoupling to compensate for large current swings generated during different power mode transitions.
- provide low parasitic resistance from the regulator to the socket.
- meet voltage and current specifications as defined in Table 7-3.

7.2.2 PLL Power Supply

An on-die PLL filter solution is implemented on the processor.

7.3 Voltage Identification (VID)

The VID specifications for the processor V_{CC} and V_{AXG} are defined by the *VR12/IMVP7 SVID Protocol*. The processor uses three signals for the serial voltage identification interface to support automatic selection of voltages. Table 7-1 specifies the voltage level corresponding to the eight bit VID value transmitted over serial VID. A ‘1’ in this table refers to a high voltage level and a ‘0’ refers to a low voltage level. If the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself. See the *VR12/IMVP7 SVID Protocol* for further details. The VID codes will change due to temperature and/or current load changes in order to minimize the power of the part. A voltage range is provided in Table 7-1. The specifications are set so that one voltage regulator can operate with all supported frequencies.

Individual processor VID values may be set during manufacturing so that two devices at the same core frequency may have different default VID settings. This is shown in the VID range values in Table 7-5. The processor provides the ability to operate while transitioning to an adjacent VID and its associated voltage. This will represent a DC shift in the loadline.

Note: Transitions above the maximum specified VID are not permitted. Table 7-5 includes VID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained.

The VR used must be capable of regulating its output to the value defined by the new VID values issued. DC specifications for dynamic VID transitions are included in Table 7-5 and Table 7-10. See the *VR12/IMVP7 SVID Protocol* for further details.

Table 7-1. IMVP7 Voltage Identification Definition (Sheet 1 of 3)

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	HEX		V_{CC_MAX}
0	0	0	0	0	0	0	0	0	0	0.00000
0	0	0	0	0	0	0	1	0	1	0.25000
0	0	0	0	0	0	1	0	0	2	0.25500
0	0	0	0	0	0	1	1	0	3	0.26000
0	0	0	0	0	1	0	0	0	4	0.26500
0	0	0	0	0	1	0	1	0	5	0.27000
0	0	0	0	0	1	1	0	0	6	0.27500
0	0	0	0	0	1	1	1	0	7	0.28000
0	0	0	0	1	0	0	0	0	8	0.28500
0	0	0	0	1	0	0	1	0	9	0.29000
0	0	0	0	1	0	1	0	0	A	0.29500
0	0	0	0	1	0	1	1	0	B	0.30000
0	0	0	0	1	1	0	0	0	C	0.30500
0	0	0	0	1	1	0	1	0	D	0.31000
0	0	0	0	1	1	1	0	0	E	0.31500
0	0	0	0	1	1	1	1	0	F	0.32000
0	0	0	1	0	0	0	0	1	0	0.32500
0	0	0	1	0	0	0	1	1	1	0.33000
0	0	0	1	0	0	1	0	1	2	0.33500
0	0	0	1	0	0	1	1	1	3	0.34000
0	0	0	1	0	1	0	0	1	4	0.34500
0	0	0	1	0	1	0	1	1	5	0.35000
0	0	0	1	0	1	1	0	1	6	0.35500
0	0	0	1	0	1	1	1	1	7	0.36000
0	0	0	1	1	0	0	0	1	8	0.36500
0	0	0	1	1	0	0	1	1	9	0.37000
0	0	0	1	1	0	1	0	1	A	0.37500
0	0	0	1	1	0	1	1	1	B	0.38000
0	0	0	1	1	1	0	0	1	C	0.38500
0	0	0	1	1	1	0	1	1	D	0.39000
0	0	0	1	1	1	1	0	1	E	0.39500
0	0	0	1	1	1	1	1	1	F	0.40000
0	0	1	0	0	0	0	0	2	0	0.40500
0	0	1	0	0	0	0	1	2	1	0.41000
0	0	1	0	0	0	1	0	2	2	0.41500
0	0	1	0	0	0	1	1	2	3	0.42000
0	0	1	0	0	1	0	0	2	4	0.42500
0	0	1	0	0	1	0	1	2	5	0.43000
0	0	1	0	0	1	1	0	2	6	0.43500
0	0	1	0	0	1	1	1	2	7	0.44000
0	0	1	0	1	0	0	0	2	8	0.44500
0	0	1	0	1	0	0	1	2	9	0.45000
0	0	1	0	1	0	1	0	2	A	0.45500
1	0	0	0	0	0	0	0	8	0	0.88500
1	0	0	0	0	0	0	1	8	1	0.89000
1	0	0	0	0	0	1	0	8	2	0.89500
1	0	0	0	0	0	1	1	8	3	0.90000
1	0	0	0	0	1	0	0	8	4	0.90500
1	0	0	0	0	1	0	1	8	5	0.91000
1	0	0	0	0	1	1	0	8	6	0.91500
1	0	0	0	0	1	1	1	8	7	0.92000
1	0	0	0	1	0	0	0	8	8	0.92500
1	0	0	0	1	0	0	1	8	9	0.93000
1	0	0	0	1	0	1	0	8	A	0.93500
1	0	0	0	1	0	1	1	8	B	0.94000
1	0	0	0	1	1	0	0	8	C	0.94500
1	0	0	0	1	1	0	1	8	D	0.95000
1	0	0	0	1	1	1	0	8	E	0.95500
1	0	0	0	1	1	1	1	8	F	0.96000
1	0	0	1	0	0	0	0	9	0	0.96500
1	0	0	1	0	0	0	1	9	1	0.97000
1	0	0	1	0	0	1	0	9	2	0.97500
1	0	0	1	0	0	1	1	9	3	0.98000
1	0	0	1	0	1	0	0	9	4	0.98500
1	0	0	1	0	1	0	1	9	5	0.99000
1	0	0	1	0	1	1	0	9	6	0.99500
1	0	0	1	0	1	1	1	9	7	1.00000
1	0	0	1	1	0	0	0	9	8	1.00500
1	0	0	1	1	0	0	1	9	9	1.01000
1	0	0	1	1	0	1	0	9	A	1.01500
1	0	0	1	1	0	1	1	9	B	1.02000
1	0	0	1	1	1	0	0	9	C	1.02500
1	0	0	1	1	1	0	1	9	D	1.03000
1	0	0	1	1	1	1	0	9	E	1.03500
1	0	0	1	1	1	1	1	9	F	1.04000
1	0	1	0	0	0	0	0	A	0	1.04500
1	0	1	0	0	0	0	1	A	1	1.05000
1	0	1	0	0	0	1	0	A	2	1.05500
1	0	1	0	0	0	1	1	A	3	1.06000
1	0	1	0	0	1	0	0	A	4	1.06500
1	0	1	0	0	1	0	1	A	5	1.07000
1	0	1	0	0	1	1	0	A	6	1.07500
1	0	1	0	0	1	1	1	A	7	1.08000
1	0	1	0	1	0	0	0	A	8	1.08500
1	0	1	0	1	0	0	1	A	9	1.09000
1	0	1	0	1	0	1	0	A	A	1.09500

Table 7-1. IMVP7 Voltage Identification Definition (Sheet 2 of 3)

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	HEX		V_{CC_MAX}
0	0	1	0	1	0	1	1	2	B	0.46000
0	0	1	0	1	1	0	0	2	C	0.46500
0	0	1	0	1	1	0	1	2	D	0.47000
0	0	1	0	1	1	1	0	2	E	0.47500
0	0	1	0	1	1	1	1	2	F	0.48000
0	0	1	1	0	0	0	0	3	0	0.48500
0	0	1	1	0	0	0	1	3	1	0.49000
0	0	1	1	0	0	1	0	3	2	0.49500
0	0	1	1	0	0	1	1	3	3	0.50000
0	0	1	1	0	1	0	0	3	4	0.50500
0	0	1	1	0	1	0	1	3	5	0.51000
0	0	1	1	0	1	1	0	3	6	0.51500
0	0	1	1	0	1	1	1	3	7	0.52000
0	0	1	1	1	0	0	0	3	8	0.52500
0	0	1	1	1	0	0	1	3	9	0.53000
0	0	1	1	1	0	1	0	3	A	0.53500
0	0	1	1	1	0	1	1	3	B	0.54000
0	0	1	1	1	1	0	0	3	C	0.54500
0	0	1	1	1	1	0	1	3	D	0.55000
0	0	1	1	1	1	1	0	3	E	0.55500
0	0	1	1	1	1	1	1	3	F	0.56000
0	1	0	0	0	0	0	0	4	0	0.56500
0	1	0	0	0	0	0	1	4	1	0.57000
0	1	0	0	0	0	1	0	4	2	0.57500
0	1	0	0	0	0	1	1	4	3	0.58000
0	1	0	0	0	1	0	0	4	4	0.58500
0	1	0	0	0	1	0	1	4	5	0.59000
0	1	0	0	0	1	1	0	4	6	0.59500
0	1	0	0	0	1	1	1	4	7	0.60000
0	1	0	0	1	0	0	0	4	8	0.60500
0	1	0	0	1	0	0	1	4	9	0.61000
0	1	0	0	1	0	1	0	4	A	0.61500
0	1	0	0	1	0	1	1	4	B	0.62000
0	1	0	0	1	1	0	0	4	C	0.62500
0	1	0	0	1	1	0	1	4	D	0.63000
0	1	0	0	1	1	1	0	4	E	0.63500
0	1	0	0	1	1	1	1	4	F	0.64000
0	1	0	1	0	0	0	0	5	0	0.64500
0	1	0	1	0	0	0	1	5	1	0.65000
0	1	0	1	0	0	1	0	5	2	0.65500
0	1	0	1	0	0	1	1	5	3	0.66000
0	1	0	1	0	1	0	0	5	4	0.66500
0	1	0	1	0	1	0	1	5	5	0.67000

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	HEX		V_{CC_MAX}
1	0	1	0	1	0	1	1	A	B	1.10000
1	0	1	0	1	1	0	0	A	C	1.10500
1	0	1	0	1	1	0	1	A	D	1.11000
1	0	1	0	1	1	1	0	A	E	1.11500
1	0	1	0	1	1	1	1	A	F	1.12000
1	0	1	1	0	0	0	0	B	0	1.12500
1	0	1	1	0	0	0	1	B	1	1.13000
1	0	1	1	0	0	1	0	B	2	1.13500
1	0	1	1	0	0	1	1	B	3	1.14000
1	0	1	1	0	1	0	0	B	4	1.14500
1	0	1	1	0	1	0	1	B	5	1.15000
1	0	1	1	0	1	1	0	B	6	1.15500
1	0	1	1	0	1	1	1	B	7	1.16000
1	0	1	1	1	0	0	0	B	8	1.16500
1	0	1	1	1	0	0	1	B	9	1.17000
1	0	1	1	1	0	1	0	B	A	1.17500
1	0	1	1	1	0	1	1	B	B	1.18000
1	0	1	1	1	1	0	0	B	C	1.18500
1	0	1	1	1	1	0	1	B	D	1.19000
1	0	1	1	1	1	1	0	B	E	1.19500
1	0	1	1	1	1	1	1	B	F	1.20000
1	1	0	0	0	0	0	0	C	0	1.20500
1	1	0	0	0	0	0	1	C	1	1.21000
1	1	0	0	0	0	1	0	C	2	1.21500
1	1	0	0	0	0	1	1	C	3	1.22000
1	1	0	0	0	1	0	0	C	4	1.22500
1	1	0	0	0	1	0	1	C	5	1.23000
1	1	0	0	0	1	1	0	C	6	1.23500
1	1	0	0	0	1	1	1	C	7	1.24000
1	1	0	0	1	0	0	0	C	8	1.24500
1	1	0	0	1	0	0	1	C	9	1.25000
1	1	0	0	1	0	1	0	C	A	1.25500
1	1	0	0	1	0	1	1	C	B	1.26000
1	1	0	0	1	1	0	0	C	C	1.26500
1	1	0	0	1	1	0	1	C	D	1.27000
1	1	0	0	1	1	1	0	C	E	1.27500
1	1	0	0	1	1	1	1	C	F	1.28000
1	1	0	1	0	0	0	0	D	0	1.28500
1	1	0	1	0	0	0	1	D	1	1.29000
1	1	0	1	0	0	1	0	D	2	1.29500
1	1	0	1	0	0	1	1	D	3	1.30000
1	1	0	1	0	1	0	0	D	4	1.30500
1	1	0	1	0	1	0	1	D	5	1.31000

Table 7-1. IMVP7 Voltage Identification Definition (Sheet 3 of 3)

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	HEX		V_{CC_MAX}	VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	HEX		V_{CC_MAX}
0	1	0	1	0	1	1	0	5	6	0.67500	1	1	0	1	0	1	1	0	D	6	1.31500
0	1	0	1	0	1	1	1	5	7	0.68000	1	1	0	1	0	1	1	1	D	7	1.32000
0	1	0	1	1	0	0	0	5	8	0.68500	1	1	0	1	1	0	0	0	D	8	1.32500
0	1	0	1	1	0	0	1	5	9	0.69000	1	1	0	1	1	0	0	1	D	9	1.33000
0	1	0	1	1	0	1	0	5	A	0.69500	1	1	0	1	1	0	1	0	D	A	1.33500
0	1	0	1	1	0	1	1	5	B	0.70000	1	1	0	1	1	0	1	1	D	B	1.34000
0	1	0	1	1	1	0	0	5	C	0.70500	1	1	0	1	1	1	0	0	D	C	1.34500
0	1	0	1	1	1	0	1	5	D	0.71000	1	1	0	1	1	1	0	1	D	D	1.35000
0	1	0	1	1	1	1	0	5	E	0.71500	1	1	0	1	1	1	1	0	D	E	1.35500
0	1	0	1	1	1	1	1	5	F	0.72000	1	1	0	1	1	1	1	1	D	F	1.36000
0	1	1	0	0	0	0	0	6	0	0.72500	1	1	1	0	0	0	0	0	E	0	1.36500
0	1	1	0	0	0	0	1	6	1	0.73000	1	1	1	0	0	0	0	1	E	1	1.37000
0	1	1	0	0	0	1	0	6	2	0.73500	1	1	1	0	0	0	1	0	E	2	1.37500
0	1	1	0	0	0	1	1	6	3	0.74000	1	1	1	0	0	0	1	1	E	3	1.38000
0	1	1	0	0	1	0	0	6	4	0.74500	1	1	1	0	0	1	0	0	E	4	1.38500
0	1	1	0	0	1	0	1	6	5	0.75000	1	1	1	0	0	1	0	1	E	5	1.39000
0	1	1	0	0	1	1	0	6	6	0.75500	1	1	1	0	0	1	1	0	E	6	1.39500
0	1	1	0	0	1	1	1	6	7	0.76000	1	1	1	0	0	1	1	1	E	7	1.40000
0	1	1	0	1	0	0	0	6	8	0.76500	1	1	1	0	1	0	0	0	E	8	1.40500
0	1	1	0	1	0	0	1	6	9	0.77000	1	1	1	0	1	0	0	1	E	9	1.41000
0	1	1	0	1	0	1	0	6	A	0.77500	1	1	1	0	1	0	1	0	E	A	1.41500
0	1	1	0	1	0	1	1	6	B	0.78000	1	1	1	0	1	0	1	1	E	B	1.42000
0	1	1	0	1	1	0	0	6	C	0.78500	1	1	1	0	1	1	0	0	E	C	1.42500
0	1	1	0	1	1	0	1	6	D	0.79000	1	1	1	0	1	1	0	1	E	D	1.43000
0	1	1	0	1	1	1	0	6	E	0.79500	1	1	1	0	1	1	1	0	E	E	1.43500
0	1	1	0	1	1	1	1	6	F	0.80000	1	1	1	0	1	1	1	1	E	F	1.44000
0	1	1	1	0	0	0	0	7	0	0.80500	1	1	1	1	0	0	0	0	F	0	1.44500
0	1	1	1	0	0	0	1	7	1	0.81000	1	1	1	1	0	0	0	1	F	1	1.45000
0	1	1	1	0	0	1	0	7	2	0.81500	1	1	1	1	0	0	1	0	F	2	1.45500
0	1	1	1	0	0	1	1	7	3	0.82000	1	1	1	1	0	0	1	1	F	3	1.46000
0	1	1	1	0	1	0	0	7	4	0.82500	1	1	1	1	0	1	0	0	F	4	1.46500
0	1	1	1	0	1	0	1	7	5	0.83000	1	1	1	1	0	1	0	1	F	5	1.47000
0	1	1	1	0	1	1	0	7	6	0.83500	1	1	1	1	0	1	1	0	F	6	1.47500
0	1	1	1	0	1	1	1	7	7	0.84000	1	1	1	1	0	1	1	1	F	7	1.48000
0	1	1	1	1	0	0	0	7	8	0.84500	1	1	1	1	1	0	0	0	F	8	1.48500
0	1	1	1	1	0	0	1	7	9	0.85000	1	1	1	1	1	0	0	1	F	9	1.49000
0	1	1	1	1	0	1	0	7	A	0.85500	1	1	1	1	1	0	1	0	F	A	1.49500
0	1	1	1	1	0	1	1	7	B	0.86000	1	1	1	1	1	0	1	1	F	B	1.50000
0	1	1	1	1	1	0	0	7	C	0.86500	1	1	1	1	1	1	0	0	F	C	1.50500
0	1	1	1	1	1	0	1	7	D	0.87000	1	1	1	1	1	1	0	1	F	D	1.51000
0	1	1	1	1	1	1	0	7	E	0.87500	1	1	1	1	1	1	1	0	F	E	1.51500
0	1	1	1	1	1	1	1	7	F	0.88000	1	1	1	1	1	1	1	1	F	F	1.52000

7.4 System Agent (SA) V_{CC} VID

The Vcc_{SA} is configured by the processor output pins VCCSA_VID[1:0].

VCCSA_VID[0] output default logic state is low for the 2nd Generation Intel® Core™ processor family mobile and Intel® Celeron® processor family mobile. Logic high is reserved for future compatibility.

VCCSA_VID[1] output default logic state is low – will not change the SA voltage. Logic high will reduce the voltage.

Note: During boot, the processor's Vcc_{SA} is 0.9 V.

Table 7-2 specifies the different VCCSA_VID configurations.

Table 7-2. VCCSA_VID configuration

Processor family	VCCSA_VID[0]	VCCSA_VID[1]	Selected VCCSA (XE and SV segments)	Selected VCCSA (LV and ULV segments)
2nd Generation Intel® Core™ processor family mobile, Intel® Celeron® processor family mobile	0	0	0.9 V	0.9 V
	0	1	0.8 V	0.85 V
Future Intel processors	1	0	Note 1	Note 1
	1	1	Note 1	Note 1

Notes:
1. Some of V_{CCSA} configurations are reserved for future Intel processor families.

7.5 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left unconnected

Arbitrary connection of these signals to V_{CC}, V_{CCIO}, V_{DDQ}, V_{CCPLL}, V_{CCSA}, V_{AXG}, V_{SS}, or to any other signal (including each other) may result in component malfunction or incompatibility with future processors. See Chapter 8 for a pin listing of the processor and the location of all reserved signals.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability.

7.6 Signal Groups

Signals are grouped by buffer type and similar characteristics as listed in Table 7-3. The buffer type indicates which signaling technology and specifications apply to the signals. All the differential signals, and selected DDR3 and Control Sideband signals, have On-Die Termination (ODT) resistors. There are some signals that do not have ODT and need to be terminated on the board.

Table 7-3. Signal Groups[1] (Sheet 1 of 3)

Signal Group	Type	Signals
System Reference Clock		
Differential	CMOS Input	BCLK, BCLK# DPLL_REF_CLK, DPLL_REF_CLK#
DDR3 Reference Clocks[2]		
Differential	DDR3 Output	SA_CK[1:0], SA_CK#[1:0] SB_CK[1:0], SB_CK#[1:0]
DDR3 Command Signals[2]		
Single Ended	DDR3 Output	SA_BS[2:0], SB_BS[2:0] SA_WE#, SB_WE# SA_RAS#, SB_RAS# SA_CAS#, SB_CAS# SA_MA[15:0], SB_MA[15:0]
DDR3 Control Signals[2]		
Single Ended	DDR3 Output	SA_CKE[1:0], SB_CKE[1:0] SA_CS#[1:0], SB_CS#[1:0] SA_ODT[1:0], SB_ODT[1:0] SM_DRAMRST#
DDR3 Data Signals[2]		
Single ended	DDR3 Bi-directional	SA_DQ[63:0], SB_DQ[63:0]
Differential	DDR3 Bi-directional	SA_DQS[7:0], SA_DQS#[7:0] SB_DQS[7:0], SB_DQS#[7:0]
DDR3 Compensation		
	Analog Bi-directional	SM_RCOMP[2:0]
DDR3 Reference		
	Analog Input	SM_VREF
TAP (ITP/XDP)		
	Input	BCLK_ITP, BCLK_ITP#
Single Ended	CMOS Input	TCK, TDI, TMS, TRST#
Single Ended	Open-Drain Output	TDO
Single Ended	Output	DBR#
Single Ended	Asynchronous CMOS Bi-Directional	BPM#[7:0]
Single Ended	Asynchronous CMOS Input	PREQ#
Single Ended	Asynchronous CMOS Output	PRDY#

Table 7-3. Signal Groups[1] (Sheet 2 of 3)

Signal Group	Type	Signals
Control Sideband		
Single Ended	CMOS Input	CFG[17:0]
Single Ended	Asynchronous CMOS/Open Drain Bi-directional	PROCHOT#
Single Ended	Asynchronous CMOS Output	THERMTRIP#, CATERR#
Single Ended	Asynchronous CMOS Input	SM_DRAMPWROK, UNCOREPWRGOOD[4], PM_SYNC, RESET#
Single Ended	Asynchronous Bi-directional	PECI
Voltage Regulator		
Single Ended	CMOS Input	VIDALERT#
Single Ended	Open Drain Output	VIDSCLK
Single Ended	CMOS Output	VCCSA_VID[1]
Single Ended	Bi-directional CMOS Input/Open Drain Output	VIDSOUT
Single Ended	Analog Output	VCCSA_SENSE VCC_DIE_SENSE
Differential	Analog Output	VCC_SENSE, VSS_SENSE VCCIO_SENSE, VSS_SENSE_VCCIO VAXG_SENSE, VSSAXG_SENSE VCC_VAL_SENSE, VSS_VAL_SENSE VAXG_VAL_SENSE, VSSAXG_VAL_SENSE
Power / Ground / Other		
Single Ended	Power	V_{CC}, V_{CCIO}, V_{CCSA}, V_{CCPLL}, V_{DDQ}, V_{AXG}, V_{CCPQE}[3], V_{CCDQ}[3]
	Ground	V_{SS}, V_{SS_NCTF}[3], DC_TEST_xx#
	No Connect	RSVD, RSVD_NCTF
	Test Point	RSVD_TP
	Other	SKTOCC#, PROC_DETECT#[3]
PCI Express* Graphics		
Differential	PCI Express Input	PEG_RX[15:0], PEG_RX#[15:0]
Differential	PCI Express Output	PEG_TX[15:0], PEG_TX#[15:0]
Single Ended	Analog Input	PEG_ICOMPO, PEG_ICOMPI, PEG_RCOMPO
Embedded DisplayPort*		
Differential	eDP Output	eDP_TX[3:0], eDP_TX#[3:0]
Differential	eDP Bi-directional	eDP_AUX, eDP_AUX#
Single Ended	Asynchronous CMOS Input	eDP_HPD#
Single Ended	Analog Input	eDP_ICOMPO, eDP_COMPIO
Direct Media Interface (DMI)		
Differential	DMI Input	DMI_RX[3:0], DMI_RX#[3:0]
Differential	DMI Output	DMI_TX[3:0], DMI_TX#[3:0]

Table 7-3. Signal Groups[1] (Sheet 3 of 3)

Signal Group	Type	Signals
Intel® FDI		
Single Ended	CMOS Input	FDI0_FSYNC, FDI1_FSYNC, FDI0_LSYNC, FDI1_LSYNC
Single Ended	Asynchronous CMOS Input	FDI_INT
Differential	FDI Output	FDI0_TX[3:0], FDI0_TX#[3:0], FDI1_TX[3:0], FDI1_TX#[3:0]
Future Compatibility		
		PROC_SELECT#, VCCSA_VID[0], VCCIO_SEL, SA_DIMM_VREFDQ, SB_DIMM_VREFDQ

Notes:
1. Refer to Chapter 6 for signal description details.
2. SA and SB refer to DDR3 Channel A and DDR3 Channel B.
3. These signals only apply to BGA packages.
4. The maximum rise/fall time of UNCOREPWRGOOD is 20 ns.

All Control Sideband Asynchronous signals are required to be asserted/de-asserted for at least **10 BCLKs** with a maximum Trise/Tfall of 6 ns for the processor to recognize the proper signal state. See Section 7.10 for the DC specifications.

7.7 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.

The processor supports Boundary Scan (JTAG) IEEE 1149.1-2001 and IEEE 1149.6-2003 standards. Some small portion of the I/O pins may support only one of these standards.

7.8 Storage Condition Specifications

Environmental storage condition limits define the temperature and relative humidity that the device is exposed to while being stored in a moisture barrier bag. The specified storage conditions are for component level prior to board attach.

Table 7-5 specifies absolute maximum and minimum storage temperature limits that represent the maximum or minimum device condition beyond which damage, latent or otherwise, may occur. The table also specifies sustained storage temperature, relative humidity, and time-duration limits. These limits specify the maximum or minimum device storage conditions for a sustained period of time. Failure to adhere to the following specifications can affect long term reliability of the processor.

Table 7-4. Storage Condition Ratings

Symbol	Parameter	Min	Max	Notes
$T_{\text{absolute storage}}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when exceeded for any length of time.	-25 °C	125 °C	1, 2, 3, 4
$T_{\text{sustained storage}}$	The ambient storage temperature (in shipping media) for a sustained period of time	-5 °C	40 °C	5, 6
$T_{\text{short term storage}}$	The ambient storage temperature (in shipping media) for a short period of time.	-20 °C	85 °C	
$RH_{\text{sustained storage}}$	The maximum device storage relative humidity for a sustained period of time.	60% at 24 °C		6, 7
$Time_{\text{sustained storage}}$	A prolonged or extended period of time; typically associated with customer shelf life.	0 Months	30 Months	7
$Time_{\text{short term storage}}$	A short-period of time;	0 hours	72 hours	

Notes:

1. Refers to a component device that is not assembled in a board or socket and is not electrically connected to a voltage reference or I/O signal.
2. Specified temperatures are not to exceed values based on data collected. Exceptions for surface mount reflow are specified by the applicable JEDEC standard. Non-adherence may affect processor reliability.
3. $T_{\text{absolute storage}}$ applies to the unassembled component only and does not apply to the shipping media, moisture barrier bags, or desiccant.
4. Component product device storage temperature qualification methods may follow JESD22-A119 (low temp) and JESD22-A103 (high temp) standards when applicable for volatile memory.
5. Intel branded products are specified and certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40 °C to 70 °C and Humidity: 50% to 90%, non-condensing with a maximum wet bulb of 28 °C.) Post board attach storage temperature limits are not specified for non-Intel branded boards.
6. The JEDEC J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
7. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by $T_{\text{sustained storage}}$ and customer shelf life in applicable Intel boxes and bags.

7.9 DC Specifications

The processor DC specifications in this section are defined at the processor pins, unless noted otherwise. See Chapter 8 for the processor pin listings and Chapter 6 for signal definitions.

- The DC specifications for the DDR3 signals are listed in Table 7-11. Control Sideband and Test Access Port (TAP) are listed in Table 7-12.
- Table 7-5 lists the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.
- AC tolerances for all DC rails include dynamic load currents at switching frequencies up to 1 MHz.

7.9.1 Voltage and Current Specifications

Table 7-5. Processor Core (V_{CC}) Active and Idle Mode DC Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note
HFM_VID	VID Range for Highest Frequency Mode (Includes Turbo Mode Operation)	XE SV-QC SV-DC LV ULV	0.8 0.8 0.8 0.75 0.7	—	1.35 1.35 1.35 1.3 1.2	V	1, 2, 6, 8
LFM_VID	VID Range for Lowest Frequency Mode	XE SV-QC SV-DC LV ULV	0.65 0.65 0.65 0.65 0.65	—	0.95 0.95 0.95 0.9 0.9	V	1, 2, 8
V_{CC}	V_{CC} for processor core		0.3–1.52			V	2, 3
I_{CCMAX}	Maximum Processor Core I_{CC}	XE SV-QC SV-DC LV ULV	—	—	97 94 53 43 33	A	4, 6, 8
I_{CC_TDC}	Thermal Design I_{CC}	XE SV-QC SV-DC LV ULV	—	—	62 52 36 25 21.5	A	5, 6, 8
I_{CC_LFM}	I_{CC} at LFM	XE SV-QC SV-DC LV ULV	—	—	31 28 11.6 17.6 12.5	A	5
$I_{C6/C7}$	I_{CC} at C6/C7 Idle-state	XE SV-QC SV-DC LV ULV	—	—	6 5.5 2.5 3.8 2.6	A	10
TOL_{VCC}	Voltage Tolerance	PS0	—	—	±15	mV	7, 9
		PS1	—	—	±12		
		PS2, PS3	—	—	±11.5		
Ripple	Ripple Tolerance	PS0 & Icc > TDC+30%	—	—	±15	mV	7, 9
		PS0 & Icc ≤ TDC+30%	—	—	±10		
		PS1	—	—	±13		
		PS2	—	—	-7.5/ +18.5		
		PS3	—	—	-7.5/ +27.5		
VR Step	VID resolution		—	5	—	mV	

Table 7-5. Processor Core (V_{CC}) Active and Idle Mode DC Voltage and Current Specifications (Sheet 2 of 2)

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note
$SLOPE_{LL}$	Processor Loadline	XE SV-QC SV-DC LV ULV	—	-1.9 -1.9 -1.9 -2.9 -2.9	—	mΩ	

Notes:

1. Unless otherwise noted, all specifications in this table are based on post-silicon estimates and simulations or empirical data.
2. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or Low Power States).
3. The voltage specification requirements are measured across VCC_SENSE and VSS_SENSE lands at the socket with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. Processor core VR to be designed to electrically support this current.
5. Processor core VR to be designed to thermally support this current indefinitely.
6. This specification assumes that Intel Turbo Boost Technology is enabled.
7. Long term reliability cannot be assured if tolerance, ripple, and core noise parameters are violated.
8. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
9. PSx refers to the voltage regulator power state as set by the SVID protocol.
10. Idle power specification is measured under temperature condition of 35 ^{o}C.

Table 7-6. Processor Uncore (V_{CCIO}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CCIO}	Voltage for the memory controller and shared cache defined at the motherboard V_{CCIO_SENSE} and $V_{SS\_SENSE\_VCCIO}$	—	1.05	—	V	
TOL_{CCIO}	V_{CCIO} Tolerance defined across V_{CCIO_SENSE} and $V_{SS\_SENSE\_VCCIO}$	DC: ±2% including ripple AC: ±3%			%	
I_{CCMAX_VCCIO}	Max Current for V_{CCIO} Rail	—	—	8.5	A	
I_{CCTDC_VCCIO}	Thermal Design Current (TDC) for V_{CCIO} Rail	—	—	8.5	A	

Note: Long term reliability cannot be assured in conditions above or below Max/Min functional limits.

Table 7-7. Memory Controller (V_{DDQ}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{DDQ}(DC+AC)	Processor I/O supply voltage for DDR3 (DC + AC specification)	—	1.5	—	V	
TOL_{DDQ}	V_{DDQ} Tolerance	DC= ±3% AC= ±2% AC+DC= ±5%			%	
I_{CCMAX_VDDQ}	Max Current for V_{DDQ} Rail	—	—	5	A	1
I_{CCAVG_VDDQ} (Standby)	Average Current for V_{DDQ} Rail during Standby	—	66	133	mA	

Notes:
1. The current supplied to the SO-DIMM modules is not included in this specification.

Table 7-8. System Agent (V_{CCSA}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CCSA}	Voltage for the System Agent and V_{CCSA_SENSE}	0.75	—	0.90	V	
TOL_{CCSA}	V_{CCSA} Tolerance	AC+DC= ±5%			%	
I_{CCMAX_VCCSA}	Max Current for V_{CCSA} Rail	—	—	6	A	
I_{CCTDC_VCCSA}	Thermal Design Current (TDC) for V_{CCSA} Rail	—	—	6	A	
Slew Rate	Voltage Ramp rate (dV/dT)	0.5	—	10	mV/us	

Note: Long term reliability cannot be assured in conditions above or below Max/Min functional limits.

Table 7-9. Processor PLL (V_{CCPLL}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CCPLL}	PLL supply voltage (DC + AC specification)	—	1.8	v	V	
TOL_{CCPLL}	V_{CCPLL} Tolerance	AC+DC= ±5%			%	
I_{CCMAX_VCCPLL}	Max Current for V_{CCPLL} Rail	—	—	1.2	A	
I_{CCTDC_VCCPLL}	Thermal Design Current (TDC) for V_{CCPLL} Rail	—	—	1.2	A	

Note: Long term reliability cannot be assured in conditions above or below Max/Min functional limits.

Table 7-10. Processor Graphics (V_{AXG}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note[1,5]
GFX_VID	Active VID Range for V_{AXG} XE, SV-QC, SV-DC LV ULV	0.65 0.65 0.65	—	1.35 1.35 1.35	V	2, 3
VAXG	Processor Graphics core voltage	0 – 1.52			V	
I_{CCMAX_VAXG}	Max Current for Processor Graphics Rail XE, SV-QC, SV-DC (GT2) SV-DC (GT1) LV (GT2) ULV (GT2) ULV (GT1)	—	—	33 24 33 26 16	A	
I_{CCTDC_VAXG}	Thermal Design Current (TDC) for Processor Graphics Rail XE, SV-QC, SV-DC (GT2) SV-DC (GT1) LV (GT2) ULV (GT2) ULV (GT1)	—	—	21.5 20 21.5 10 8	A	
TOL_{AXG}	V_{AXG} Tolerance	PS0,PS1	—	±15	mV	4
		PS2,PS3	—	±11.5	mV	4
Ripple	Ripple Tolerance	PS0, PS1	—	±18	mV	4
		PS2	—	-7.5/+18.5	mV	4
		PS3	—	-7.5/+27.5	mV	
LL_{AXG}	V_{AXG} Loadline GT2 based units GT1 based units	-3.9 -4.6			mΩ	

Notes:

1. Unless otherwise noted, all specifications in this table are based on post-silicon estimates and simulations or empirical data.
2. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or Low Power States).
3. The voltage specification requirements are measured across VCC_SENSE and VSS_SENSE lands at the socket with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. PSx refers to the voltage regulator power state as set by the SVID protocol.
5. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or Low Power States).

Table 7-11. DDR3 Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	—	—	SM_VREF -0.1	V	2, 4, 11
V_{IH}	Input High Voltage	SM_VREF + 0.1	—	—	V	3, 11
V_{IL}	Input Low Voltage (SM_DRAMPWROK)	—	—	V_{DDQ}*0.55 -0.1	V	10
V_{IH}	Input High Voltage (SM_DRAMPWROK)	V_{DDQ}*0.55 +0.1	—	—	V	10
V_{OL}	Output Low Voltage	—	$(V_{DDQ} / 2)* (R_{ON} /(R_{ON}+R_{TERM}))$	—		6
V_{OH}	Output High Voltage	—	$V_{DDQ} - ((V_{DDQ} / 2)* (R_{ON}/(R_{ON}+R_{TERM}))$	—	V	4, 6
$R_{ON\_UP(DQ)}$	DDR3 Data Buffer pull-up Resistance	24.31	28.6	32.9	Ω	5
$R_{ON\_DN(DQ)}$	DDR3 Data Buffer pull-down Resistance	22.88	28.6	34.32	Ω	5
$R_{ODT(DQ)}$	DDR3 On-die termination equivalent resistance for data signals	83 41.5	100 50	117 65	Ω	
$V_{ODT(DC)}$	DDR3 On-die termination DC working point (driver set to receive mode)	0.43*V_{CC}	0.5*V_{CC}	0.56*V_{CC}	V	
$R_{ON\_UP(CK)}$	DDR3 Clock Buffer pull-up Resistance	20.8	26	28.6	Ω	5
$R_{ON\_DN(CK)}$	DDR3 Clock Buffer pull-down Resistance	20.8	26	31.2	Ω	5
$R_{ON\_UP(CMD)}$	DDR3 Command Buffer pull-up Resistance	16	20	22	Ω	5
$R_{ON\_DN(CMD)}$	DDR3 Command Buffer pull-down Resistance	16	20	24	Ω	5
$R_{ON\_UP(CTL)}$	DDR3 Control Buffer pull-up Resistance	16	20	22	Ω	5
$R_{ON\_DN(CTL)}$	DDR3 Control Buffer pull-down Resistance	16	20	24	Ω	5
I_{LI}	Input Leakage Current (DQ, CK) 0V 0.2*V_{DDQ} 0.8*V_{DDQ} V_{DDQ}	—	—	± 0.75 ± 0.55 ± 0.9 ± 1.4	mA	
I_{LI}	Input Leakage Current (CMD, CTL) 0V 0.2*V_{DDQ} 0.8*V_{DDQ} V_{DDQ}	—	—	± 0.85 ± 0.65 ± 1.10 ± 1.65	mA	
SM_RCOMP0	Command COMP Resistance	138.6	140	141.4	Ω	8
SM_RCOMP1	Data COMP Resistance	25.74	26	26.26	Ω	8
SM_RCOMP2	ODT COMP Resistance	198	200	202	Ω	8

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{DDQ}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull up/down driver resistance.
6. R_{TERM} is the termination on the DIMM and in not controlled by the Processor.
7. The minimum and maximum values for these signals are programmable by BIOS to one of the two sets.
8. SM_RCOMPx resistance must be provided on the system board with 1% resistors. SM_RCOMPx resistors are to V_{SS}.
9. DDR3 values are pre-silicon estimations and are subject to change.
10. SM_DRAMPWROK must have a maximum of 15 ns rise or fall time over V_{DDQ} * 0.55 ±200 mV and the edge must be monotonic.
11. SM_VREF is defined as $V_{DDQ}/2$.

Table 7-12. Control Sideband and TAP Signal Group DC Specifications

Symbol	Parameter	Min	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	—	V_{CCIO} * 0.3	V	2
V_{IH}	Input High Voltage	V_{CCIO} * 0.7	—	V	2, 4
V_{OL}	Output Low Voltage	—	V_{CCIO} * 0.1	V	2
V_{OH}	Output High Voltage	V_{CCIO} * 0.9	—	V	2, 4
R_{ON}	Buffer on Resistance	23	73	Ω	
I_{LI}	Input Leakage Current	—	±200	μA	3

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{CCIO} referred to in these specifications refers to instantaneous V_{CCIO}.
3. For V_{IN} between 0 V and V_{CCIO}. Measured when the driver is tristated.
4. V_{IH} and V_{OH} may experience excursions above V_{CCIO}. However, input signal drivers must comply with the signal quality specifications.

Table 7-13. PCI Express* DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
$V_{TX\text{-}DIFF\text{-}p\text{-}p}$	Differential Peak-to-Peak Tx Voltage Swing	0.4	0.5	0.6	V	3
$V_{TX\_CM\text{-}AC\text{-}p}$	Tx AC Peak Common Mode Output Voltage (Gen 1 Only)	0.8	1	1.2	mV	1, 2, 6
$Z_{TX\text{-}DIFF\text{-}DC}$	DC Differential Tx Impedance (Gen 1 Only)	80	—	120	Ω	1, 10
$Z_{RX\text{-}DC}$	DC Common Mode Rx Impedance	40	—	60	Ω	1, 8, 9
$Z_{RX\text{-}DIFF\text{-}DC}$	DC Differential Rx Impedance (Gen1 Only)	80	—	120	Ω	1
$V_{RX\text{-}DIFFp\text{-}p}$	Differential Rx Input Peak-to-Peak Voltage (Gen 1 only)	0.175	—	1.2	V	1, 11
$V_{RX\_CM\text{-}AC\text{-}p}$	Rx AC Peak Common Mode Input Voltage	—	—	150	mV	1, 7
PEG_ICOMPO	Comp Resistance	24.75	25	25.25	Ω	4, 5
PEG_ICOMPI	Comp Resistance	24.75	25	25.25	Ω	4, 5
PEG_RCOMPO	Comp Resistance	24.75	25	25.25	Ω	4, 5

Notes:
1. Refer to the *PCI Express Base Specification* for more details.
2. $V_{TX\text{-}AC\text{-}CM\text{-}PP}$ and $V_{TX\text{-}AC\text{-}CM\text{-}P}$ are defined in the *PCI Express Base Specification*. Measurement is made over at least 10^^{6} UI.
3. As measured with compliance test load. Defined as $2*|V_{TXD+} - V_{TXD-}|$.
4. COMP resistance must be provided on the system board with 1% resistors. COMP resistors are to V_{CCIO}.
5. PEG_ICOMPO, PEG_ICOMPI, PEG_RCOMPO are the same resistor. Intel allows using 24.9 Ω 1% resistors.
6. RMS value.
7. Measured at Rx pins into a pair of 50-Ω terminations into ground. Common mode peak voltage is defined by the expression: max{|(Vd+ - Vd-) – V-CMDC|}.
8. DC impedance limits are needed to ensure Receiver detect.
9. The Rx DC Common Mode Impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately and the 15 Rx Common Mode Impedance (constrained by RLRX-CM to 50 Ω ±20%) must be within the specified range by the time Detect is entered.
10. Low impedance defined during signaling. Parameter is captured for 5.0 GHz by RLTX-DIFF.
11. This specification is the same as $V_{RX\text{-}EYE}$

Table 7-14. Embedded DisplayPort* DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
eDP_HPD#						
V_{IL}	Input Low Voltage	-0.1	—	0.3 * V_{CCIO}	V	
V_{IH}	Input High Voltage	0.7 * V_{CCIO}	—	V_{CCIO}	V	
eDP_AUX, eDP_AUX#						
$V_{AUX\text{-}DIFFp\text{-}p}$ (Tx)	AUX Peak-to-Peak Voltage at the transmitting device	0.4	—	0.6		1
$V_{AUX\text{-}DIFFp\text{-}p}$ (Rx)	AUX Peak-to-Peak Voltage at the receiving device	0.32	—	1.36	V	1
eDP COMPs						
eDP_ICOMPI	Comp Resistance	24.75	25	25.25	Ω	2, 3
eDP_COMPIO	Comp Resistance	24.75	25	25.25	Ω	2, 3

Notes:
1. VAUX-DIFFp-p = 2*|VAUXP – VAUXM|. Refer to the VESA DisplayPort Standard specification for more details.
2. COMP resistance must be provided on the system board with 1% resistors. COMP resistors are to V_{SS}.
3. eDP_ICOMPO, eDP_ICOMPI, eDP_RCOMPO are the same resistor.

7.10 Platform Environmental Control Interface (PECI) DC Specifications

PECI is an Intel proprietary interface that provides a communication channel between Intel processors and chipset components to external Adaptive Thermal Monitor devices. The processor contains a Digital Thermal Sensor (DTS) that reports a relative die temperature as an offset from Thermal Control Circuit (TCC) activation temperature. Temperature sensors located throughout the die are implemented as analog-to-digital converters calibrated at the factory. PECI provides an interface for external devices to read the DTS temperature for thermal management and fan speed control. More detailed information may be found in the *Platform Environment Control Interface (PECI) Specification*.

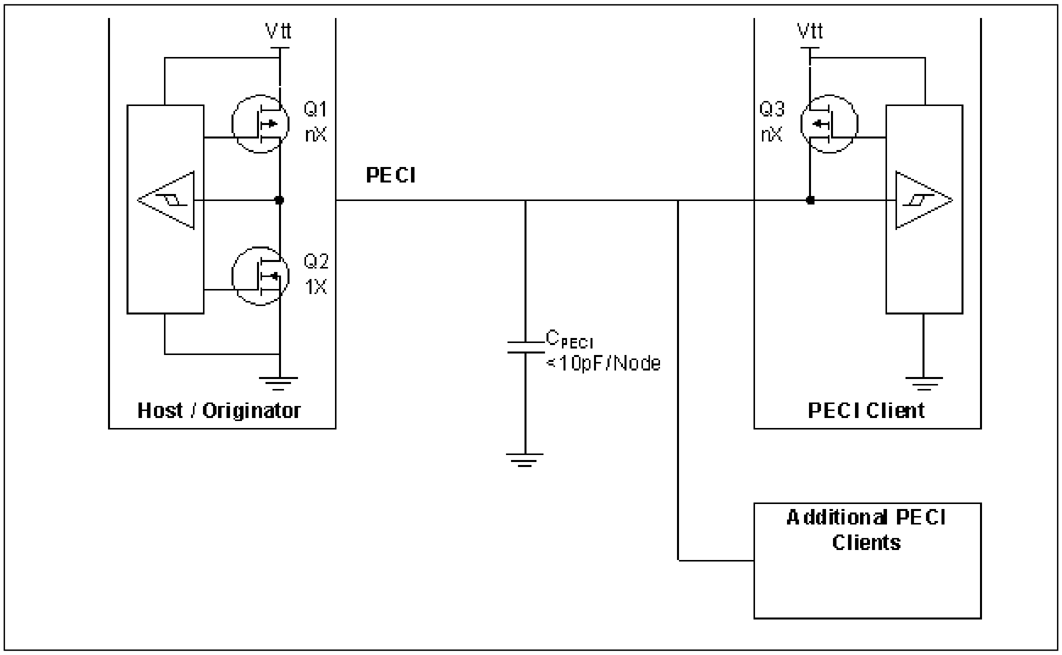
7.10.1 PECI Bus Architecture

The PECI architecture based on **wired OR bus** that the clients (such as 2nd Generation Intel® Core™ processor family mobile PECI) can pull up high (with strong drive).

The idle state on the bus is near zero.

Figure 7-1 demonstrates PECI design and connectivity, while the host/originator can be 3rd party PECI host, and one of the PECI client is a 2nd Generation Intel® Core™ processor family mobile PECI and Intel® Celeron® processor family mobile PECI device.

Figure 7-1. Example for PECI Host-clients Connection



7.10.2 PECI DC Characteristics

The PECI interface operates at a nominal voltage set by V_{CCIO} The set of DC electrical specifications shown in Table 7-15 are used with devices normally operating from a V_{CCIO} interface supply. V_{CCIO} nominal levels will vary between processor families. All PECI devices will operate at the V_{CCIO} level determined by the processor installed in the system. For specific nominal V_{CCIO} levels, refer to Table 7-6.

Table 7-15. PECI DC Electrical Limits

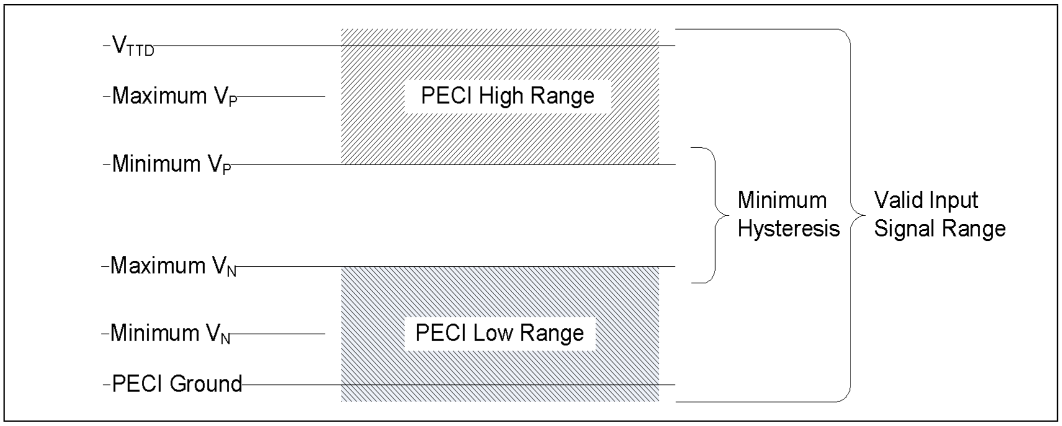
Symbol	Definition and Conditions	Min	Max	Units	Notes^1
Rup	Internal pull up resistance	15	45	Ohm	3
V_{in}	Input Voltage Range	-0.15	V_{CCIO}	V	
$V_{hysteresis}$	Hysteresis	0.1 * V_{CCIO}	N/A	V	
V_n	Negative-Edge Threshold Voltage	0.275 * V_{CCIO}	0.500 * V_{CCIO}	V	
V_p	Positive-Edge Threshold Voltage	0.550 * V_{CCIO}	0.725 * V_{CCIO}	V	
C_{bus}	Bus Capacitance per Node	N/A	10	pF	
Cpad	Pad Capacitance	0.7	1.8	pF	
Ileak000	leakage current @ 0V	—	0.6	mA	2
Ileak025	leakage current @ 0.25*V_{CCIO}	—	0.4	mA	2
Ileak050	leakage current @ 0.50*V_{CCIO}	—	0.2	mA	2
Ileak075	leakage current @ 0.75*V_{CCIO}	—	0.13	mA	2
Ileak100	leakage current @ V_{CCIO}	—	0.10	mA	2

Notes:
1. V_{CCIO} supplies the PECI interface. PECI behavior does not affect V_{CCIO} min/max specifications.
2. The leakage specification applies to powered devices on the PECI bus.
3. The PECI buffer internal pull up resistance measured at 0.75*V_{CCIO}

7.10.3 Input Device Hysteresis

The input buffers in both client and host models must use a Schmitt-triggered input design for improved noise immunity. Use Figure 7-2 as a guide for input buffer design.

Figure 7-2. Input Device Hysteresis



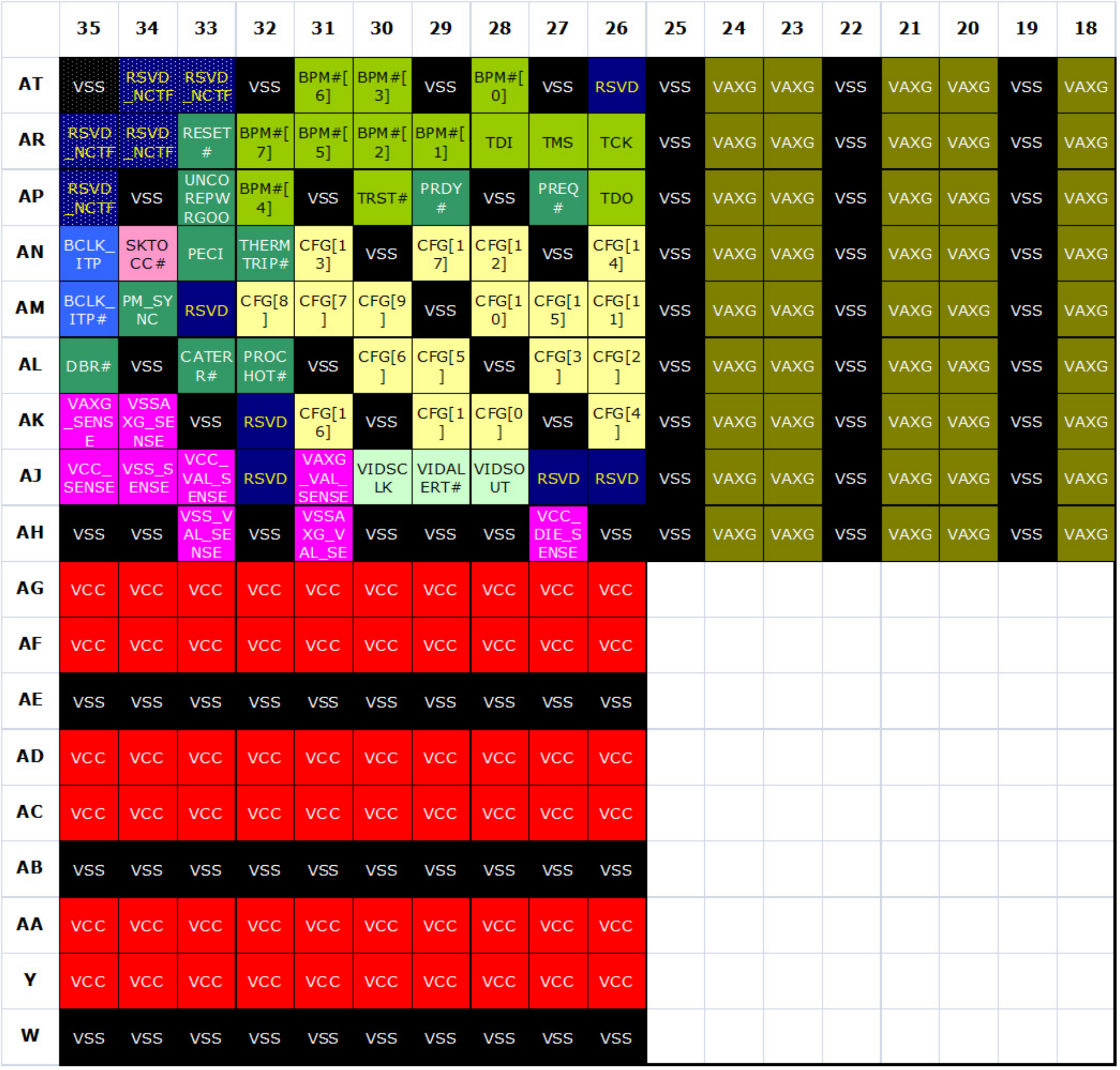
§ §

8 Processor Pin and Signal Information

8.1 Processor Pin Assignments

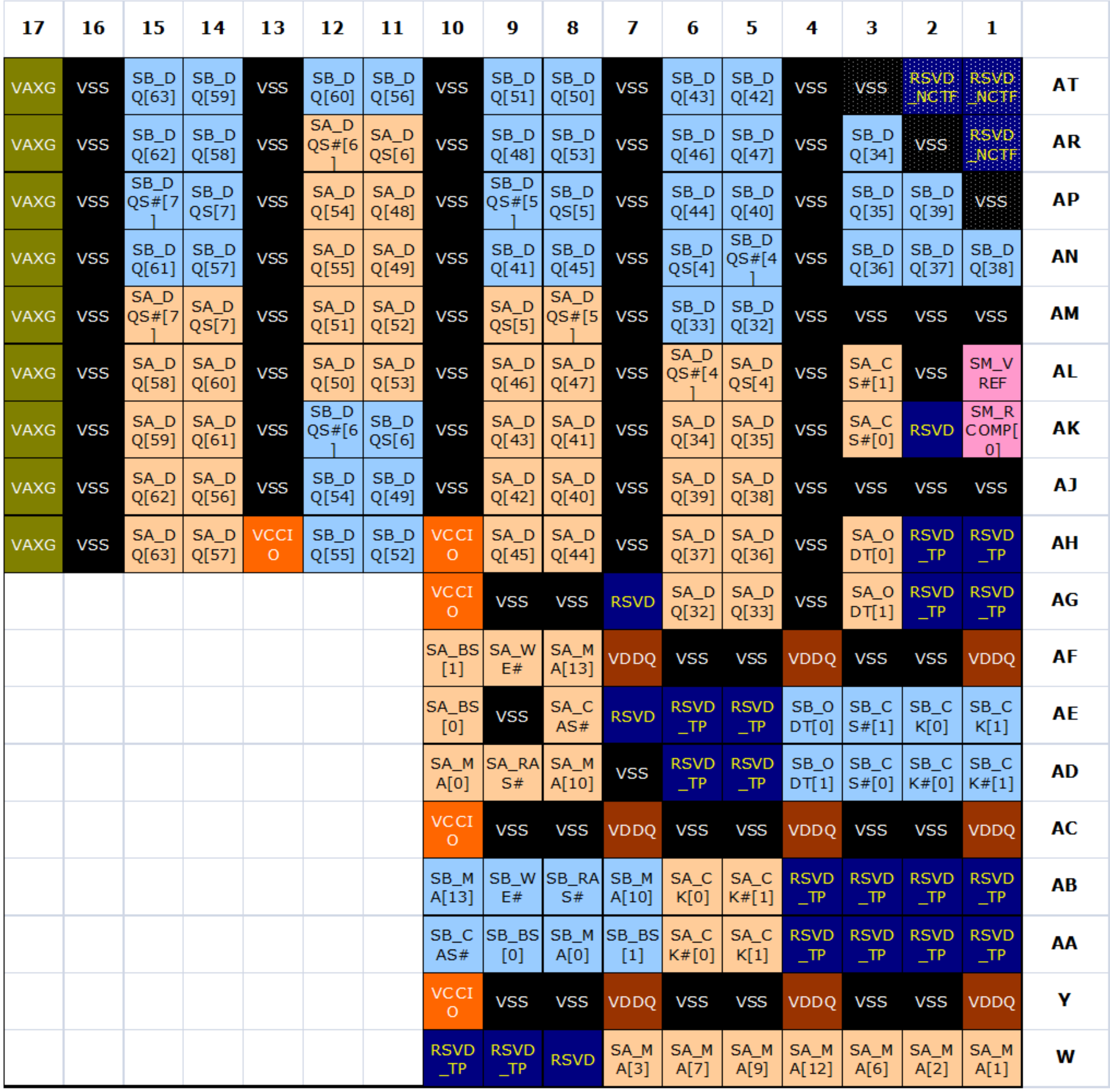
- Table 8-1, Table 8-2 and Table 8-3 all pins ordered alphabetically for the rPGA988B BGA1224 and BGA1023 package respectively.
- Figure 8-1, Figure 8-2, Figure 8-3 and Figure 8-4 show the Top-Down view of the rPGA988B pinmap.
- Figure 8-5, Figure 8-6, Figure 8-7 and Figure 8-8 show the Top-Down view of the BGA1224 ballmap.
- Figure 8-9, Figure 8-10, Figure 8-11 and Figure 8-12 show the Top-Down view of the BGA1023 ballmap.

Figure 8-1. rPGA988B (Socket-G2) Pinmap (Top View, Upper-Left Quadrant)



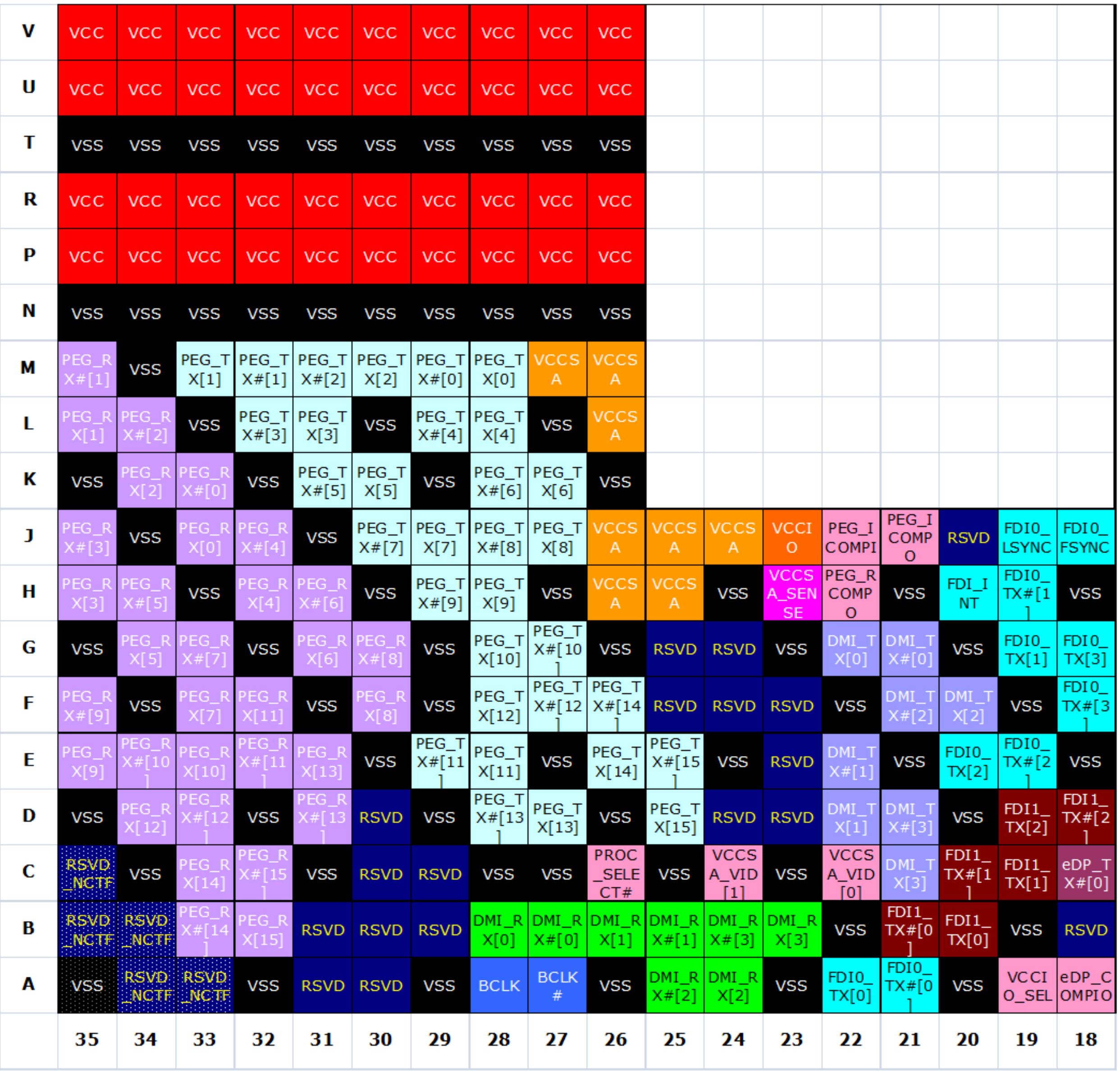
	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
AT	VSS	RSVD_NCTF	RSVD_NCTF	VSS	BPM#[6]	BPM#[3]	VSS	BPM#[0]	VSS	RSVD	VSS	VAXG	VAXG	VSS	VAXG	VAXG	VSS	VAXG
AR	RSVD_NCTF	RSVD_NCTF	RESET#	BPM#[7]	BPM#[5]	BPM#[2]	BPM#[1]	TDI	TMS	TCK	VSS	VAXG	VAXG	VSS	VAXG	VAXG	VSS	VAXG
AP	RSVD_NCTF	VSS	UNCOREPWRGOO	BPM#[4]	VSS	TRST#	PRDY#	VSS	PREQ#	TDO	VSS	VAXG	VAXG	VSS	VAXG	VAXG	VSS	VAXG
AN	BCLK_ITP	SKTOCC#	PECI	THERMTRIP#	CFG[13]	VSS	CFG[17]	CFG[12]	VSS	CFG[14]	VSS	VAXG	VAXG	VSS	VAXG	VAXG	VSS	VAXG
AM	BCLK_ITP#	PM_SYNC	RSVD	CFG[8]	CFG[7]	CFG[9]	VSS	CFG[10]	CFG[15]	CFG[11]	VSS	VAXG	VAXG	VSS	VAXG	VAXG	VSS	VAXG
AL	DBR#	VSS	CATERR#	PROCHOT#	VSS	CFG[6]	CFG[5]	VSS	CFG[3]	CFG[2]	VSS	VAXG	VAXG	VSS	VAXG	VAXG	VSS	VAXG
AK	VAXG_SENSE	VSSAXG_SENSE	VSS	RSVD	CFG[16]	VSS	CFG[1]	CFG[0]	VSS	CFG[4]	VSS	VAXG	VAXG	VSS	VAXG	VAXG	VSS	VAXG
AJ	VCC_SENSE	VSS_SENSE	VCC_VAL_SENSE	RSVD	VAXG_VAL_SENSE	VIDSCLK	VIDALERT#	VIDSOUT	RSVD	RSVD	VSS	VAXG	VAXG	VSS	VAXG	VAXG	VSS	VAXG
AH	VSS	VSS	VSS_VAL_SENSE	VSS	VSSAXG_VAL_SE	VSS	VSS	VSS	VCC_DIE_SENSE	VSS	VSS	VAXG	VAXG	VSS	VAXG	VAXG	VSS	VAXG
AG	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AF	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
AD	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AB	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
AA	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
Y	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
W	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								

Figure 8-2. rPGA988B (Socket-G2) Pinmap (Top View, Upper-Right Quadrant)



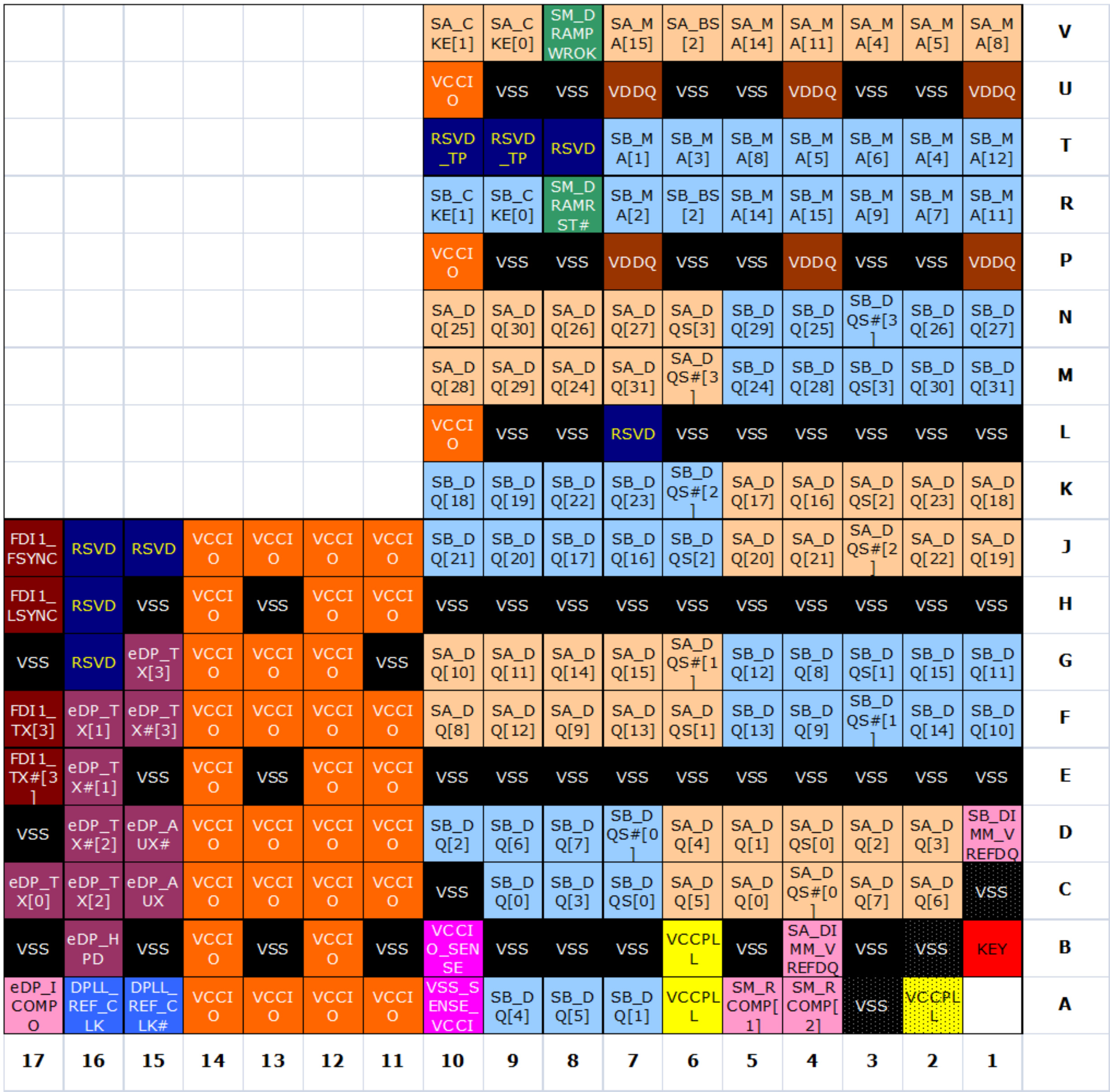
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
VAXG	VSS	SB_DQ[63]	SB_DQ[59]	VSS	SB_DQ[60]	SB_DQ[56]	VSS	SB_DQ[51]	SB_DQ[50]	VSS	SB_DQ[43]	SB_DQ[42]	VSS	VSS	RSVD_NCTF	RSVD_NCTF	**AT**
VAXG	VSS	SB_DQ[62]	SB_DQ[58]	VSS	SA_DQS#[6]	SA_DQS[6]	VSS	SB_DQ[48]	SB_DQ[53]	VSS	SB_DQ[46]	SB_DQ[47]	VSS	SB_DQ[34]	VSS	RSVD_NCTF	**AR**
VAXG	VSS	SB_DQS#[7]	SB_DQS[7]	VSS	SA_DQ[54]	SA_DQ[48]	VSS	SB_DQS#[5]	SB_DQS[5]	VSS	SB_DQ[44]	SB_DQ[40]	VSS	SB_DQ[35]	SB_DQ[39]	VSS	**AP**
VAXG	VSS	SB_DQ[61]	SB_DQ[57]	VSS	SA_DQ[55]	SA_DQ[49]	VSS	SB_DQ[41]	SB_DQ[45]	VSS	SB_DQS[4]	SB_DQS#[4]	VSS	SB_DQ[36]	SB_DQ[37]	SB_DQ[38]	**AN**
VAXG	VSS	SA_DQS#[7]	SA_DQS[7]	VSS	SA_DQ[51]	SA_DQ[52]	VSS	SA_DQS[5]	SA_DQS#[5]	VSS	SB_DQ[33]	SB_DQ[32]	VSS	VSS	VSS	VSS	**AM**
VAXG	VSS	SA_DQ[58]	SA_DQ[60]	VSS	SA_DQ[50]	SA_DQ[53]	VSS	SA_DQ[46]	SA_DQ[47]	VSS	SA_DQS#[4]	SA_DQS[4]	VSS	SA_CS#[1]	VSS	SM_VREF	**AL**
VAXG	VSS	SA_DQ[59]	SA_DQ[61]	VSS	SB_DQS#[6]	SB_DQS[6]	VSS	SA_DQ[43]	SA_DQ[41]	VSS	SA_DQ[34]	SA_DQ[35]	VSS	SA_CS#[0]	RSVD	SM_RCOMP[0]	**AK**
VAXG	VSS	SA_DQ[62]	SA_DQ[56]	VSS	SB_DQ[54]	SB_DQ[49]	VSS	SA_DQ[42]	SA_DQ[40]	VSS	SA_DQ[39]	SA_DQ[38]	VSS	VSS	VSS	VSS	**AJ**
VAXG	VSS	SA_DQ[63]	SA_DQ[57]	VCCIO	SB_DQ[55]	SB_DQ[52]	VCCIO	SA_DQ[45]	SA_DQ[44]	VSS	SA_DQ[37]	SA_DQ[36]	VSS	SA_ODT[0]	RSVD_TP	RSVD_TP	**AH**
							VCCIO	VSS	VSS	RSVD	SA_DQ[32]	SA_DQ[33]	VSS	SA_ODT[1]	RSVD_TP	RSVD_TP	**AG**
							SA_BS[1]	SA_WE#	SA_MA[13]	VDDQ	VSS	VSS	VDDQ	VSS	VSS	VDDQ	**AF**
							SA_BS[0]	VSS	SA_CAS#	RSVD	RSVD_TP	RSVD_TP	SB_ODT[0]	SB_CS#[1]	SB_CK[0]	SB_CK[1]	**AE**
							SA_MA[0]	SA_RAS#	SA_MA[10]	VSS	RSVD_TP	RSVD_TP	SB_ODT[1]	SB_CS#[0]	SB_CK#[0]	SB_CK#[1]	**AD**
							VCCIO	VSS	VSS	VDDQ	VSS	VSS	VDDQ	VSS	VSS	VDDQ	**AC**
							SB_MA[13]	SB_WE#	SB_RAS#	SB_MA[10]	SA_CK[0]	SA_CK#[1]	RSVD_TP	RSVD_TP	RSVD_TP	RSVD_TP	**AB**
							SB_CAS#	SB_BS[0]	SB_MA[0]	SB_BS[1]	SA_CK#[0]	SA_CK[1]	RSVD_TP	RSVD_TP	RSVD_TP	RSVD_TP	**AA**
							VCCIO	VSS	VSS	VDDQ	VSS	VSS	VDDQ	VSS	VSS	VDDQ	**Y**
							RSVD_TP	RSVD_TP	RSVD	SA_MA[3]	SA_MA[7]	SA_MA[9]	SA_MA[12]	SA_MA[6]	SA_MA[2]	SA_MA[1]	**W**

Figure 8-3. rPGA988B (Socket-G2) Pinmap (Top View, Lower-Left Quadrant)



V	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
U	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
T	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
R	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
P	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
N	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
M	PEG_RX#[1]	VSS	PEG_TX[1]	PEG_TX#[1]	PEG_TX#[2]	PEG_TX[2]	PEG_TX#[0]	PEG_TX[0]	VCCSA	VCCSA								
L	PEG_RX[1]	PEG_RX#[2]	VSS	PEG_TX#[3]	PEG_TX[3]	VSS	PEG_TX#[4]	PEG_TX[4]	VSS	VCCSA								
K	VSS	PEG_RX[2]	PEG_RX#[0]	VSS	PEG_TX#[5]	PEG_TX[5]	VSS	PEG_TX#[6]	PEG_TX[6]	VSS								
J	PEG_RX#[3]	VSS	PEG_RX[0]	PEG_RX#[4]	VSS	PEG_TX#[7]	PEG_TX[7]	PEG_TX#[8]	PEG_TX[8]	VCCSA	VCCSA	VCCSA	VCCIO	PEG_ICOMPI	PEG_ICOMPO	RSVD	FDI0_LSYNC	FDI0_FSYNC
H	PEG_RX[3]	PEG_RX#[5]	VSS	PEG_RX[4]	PEG_RX#[6]	VSS	PEG_TX#[9]	PEG_TX[9]	VSS	VCCSA	VCCSA	VSS	VCCSA_SENSE	PEG_RCOMPO	VSS	FDI_INT	FDI0_TX#[1]	VSS
G	VSS	PEG_RX[5]	PEG_RX#[7]	VSS	PEG_RX[6]	PEG_RX#[8]	VSS	PEG_TX[10]	PEG_TX#[10]	VSS	RSVD	RSVD	VSS	DMI_TX[0]	DMI_TX#[0]	VSS	FDI0_TX[1]	FDI0_TX[3]
F	PEG_RX#[9]	VSS	PEG_RX[7]	PEG_RX[11]	VSS	PEG_RX[8]	VSS	PEG_TX[12]	PEG_TX#[12]	PEG_TX#[14]	RSVD	RSVD	RSVD	VSS	DMI_TX#[2]	DMI_TX[2]	VSS	FDI0_TX#[3]
E	PEG_RX[9]	PEG_RX#[10]	PEG_RX[10]	PEG_RX#[11]	PEG_RX[13]	VSS	PEG_TX#[11]	PEG_TX[11]	VSS	PEG_TX[14]	PEG_TX#[15]	VSS	RSVD	DMI_TX#[1]	VSS	FDI0_TX[2]	FDI0_TX#[2]	VSS
D	VSS	PEG_RX[12]	PEG_RX#[12]	VSS	PEG_RX#[13]	RSVD	VSS	PEG_TX#[13]	PEG_TX[13]	VSS	PEG_TX[15]	RSVD	RSVD	DMI_TX[1]	DMI_TX#[3]	VSS	FDI1_TX[2]	FDI1_TX#[2]
C	RSVD_NCTF	VSS	PEG_RX[14]	PEG_RX#[15]	VSS	RSVD	RSVD	VSS	VSS	PROC_SELECT#	VSS	VCCSA_VID[1]	VSS	VCCSA_VID[0]	DMI_TX[3]	FDI1_TX#[1]	FDI1_TX[1]	eDP_TX#[0]
B	RSVD_NCTF	RSVD_NCTF	PEG_RX#[14]	PEG_RX[15]	RSVD	RSVD	RSVD	DMI_RX[0]	DMI_RX#[0]	DMI_RX[1]	DMI_RX#[1]	DMI_RX#[3]	DMI_RX[3]	VSS	FDI1_TX#[0]	FDI1_TX[0]	VSS	RSVD
A	VSS	RSVD_NCTF	RSVD_NCTF	VSS	RSVD	RSVD	VSS	BCLK	BCLK#	VSS	DMI_RX#[2]	DMI_RX[2]	VSS	FDI0_TX[0]	FDI0_TX#[0]	VSS	VCCIO_SEL	eDP_COMPIO
	35	**34**	**33**	**32**	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**

Figure 8-4. rPGA988B (Socket-G2) Pinmap (Top View, Lower-Right Quadrant)



							SA_CKE[1]	SA_CKE[0]	SM_DRAMPWROK	SA_MA[15]	SA_BS[2]	SA_MA[14]	SA_MA[11]	SA_MA[4]	SA_MA[5]	SA_MA[8]	**V**
							VCCIO	VSS	VSS	VDDQ	VSS	VSS	VDDQ	VSS	VSS	VDDQ	**U**
							RSVD_TP	RSVD_TP	RSVD	SB_MA[1]	SB_MA[3]	SB_MA[8]	SB_MA[5]	SB_MA[6]	SB_MA[4]	SB_MA[12]	**T**
							SB_CKE[1]	SB_CKE[0]	SM_DRAMRST#	SB_MA[2]	SB_BS[2]	SB_MA[14]	SB_MA[15]	SB_MA[9]	SB_MA[7]	SB_MA[11]	**R**
							VCCIO	VSS	VSS	VDDQ	VSS	VSS	VDDQ	VSS	VSS	VDDQ	**P**
							SA_DQ[25]	SA_DQ[30]	SA_DQ[26]	SA_DQ[27]	SA_DQS[3]	SB_DQ[29]	SB_DQ[25]	SB_DQS#[3]	SB_DQ[26]	SB_DQ[27]	**N**
							SA_DQ[28]	SA_DQ[29]	SA_DQ[24]	SA_DQ[31]	SA_DQS#[3]	SB_DQ[24]	SB_DQ[28]	SB_DQS[3]	SB_DQ[30]	SB_DQ[31]	**M**
							VCCIO	VSS	VSS	RSVD	VSS	VSS	VSS	VSS	VSS	VSS	**L**
							SB_DQ[18]	SB_DQ[19]	SB_DQ[22]	SB_DQ[23]	SB_DQS#[2]	SA_DQ[17]	SA_DQ[16]	SA_DQS[2]	SA_DQ[23]	SA_DQ[18]	**K**
FDI1_FSYNC	RSVD	RSVD	VCCIO	VCCIO	VCCIO	VCCIO	SB_DQ[21]	SB_DQ[20]	SB_DQ[17]	SB_DQ[16]	SB_DQS[2]	SA_DQ[20]	SA_DQ[21]	SA_DQS#[2]	SA_DQ[22]	SA_DQ[19]	**J**
FDI1_LSYNC	RSVD	VSS	VCCIO	VSS	VCCIO	VCCIO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	**H**
VSS	RSVD	eDP_TX[3]	VCCIO	VCCIO	VCCIO	VSS	SA_DQ[10]	SA_DQ[11]	SA_DQ[14]	SA_DQ[15]	SA_DQS#[1]	SB_DQ[12]	SB_DQ[8]	SB_DQS[1]	SB_DQ[15]	SB_DQ[11]	**G**
FDI1_TX[3]	eDP_TX[1]	eDP_TX#[3]	VCCIO	VCCIO	VCCIO	VCCIO	SA_DQ[8]	SA_DQ[12]	SA_DQ[9]	SA_DQ[13]	SA_DQS[1]	SB_DQ[13]	SB_DQ[9]	SB_DQS#[1]	SB_DQ[14]	SB_DQ[10]	**F**
FDI1_TX#[3]	eDP_TX#[1]	VSS	VCCIO	VSS	VCCIO	VCCIO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	**E**
VSS	eDP_TX#[2]	eDP_AUX#	VCCIO	VCCIO	VCCIO	VCCIO	SB_DQ[2]	SB_DQ[6]	SB_DQ[7]	SB_DQS#[0]	SA_DQ[4]	SA_DQ[1]	SA_DQS[0]	SA_DQ[2]	SA_DQ[3]	SB_DIMM_VREFDQ	**D**
eDP_TX[0]	eDP_TX[2]	eDP_AUX	VCCIO	VCCIO	VCCIO	VCCIO	VSS	SB_DQ[0]	SB_DQ[3]	SB_DQS[0]	SA_DQ[5]	SA_DQ[0]	SA_DQS#[0]	SA_DQ[7]	SA_DQ[6]	VSS	**C**
VSS	eDP_HPD	VSS	VCCIO	VSS	VCCIO	VSS	VCCIO_SENSE	VSS	VSS	VSS	VCCPLL	VSS	SA_DIMM_VREFDQ	VSS	VSS	KEY	**B**
eDP_ICOMPO	DPLL_REF_CLK	DPLL_REF_CLK#	VCCIO	VCCIO	VCCIO	VCCIO	VSS_SENSE_VCCIO	SB_DQ[4]	SB_DQ[5]	SB_DQ[1]	VCCPLL	SM_RCOMP[1]	SM_RCOMP[2]	VSS	VCCPLL		**A**
17	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

Table 8-1. rPGA988B Processor Pin List by Pin Name

Table 8-1. rPGA988B Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir
BCLK	A28	Diff Clk	I
BCLK#	A27	Diff Clk	I
BCLK_ITP	AN35	Diff Clk	I
BCLK_ITP#	AM35	Diff Clk	I
BPM#[0]	AT28	Asynch CMOS	I/O
BPM#[1]	AR29	Asynch CMOS	I/O
BPM#[2]	AR30	Asynch CMOS	I/O
BPM#[3]	AT30	Asynch CMOS	I/O
BPM#[4]	AP32	Asynch CMOS	I/O
BPM#[5]	AR31	Asynch CMOS	I/O
BPM#[6]	AT31	Asynch CMOS	I/O
BPM#[7]	AR32	Asynch CMOS	I/O
CATERR#	AL33	Asynch CMOS	O
CFG[0]	AK28	CMOS	I
CFG[1]	AK29	CMOS	I
CFG[2]	AL26	CMOS	I
CFG[3]	AL27	CMOS	I
CFG[4]	AK26	CMOS	I
CFG[5]	AL29	CMOS	I
CFG[6]	AL30	CMOS	I
CFG[7]	AM31	CMOS	I
CFG[8]	AM32	CMOS	I
CFG[9]	AM30	CMOS	I
CFG[10]	AM28	CMOS	I
CFG[11]	AM26	CMOS	I
CFG[12]	AN28	CMOS	I
CFG[13]	AN31	CMOS	I
CFG[14]	AN26	CMOS	I
CFG[15]	AM27	CMOS	I
CFG[16]	AK31	CMOS	I
CFG[17]	AN29	CMOS	I
DBR#	AL35	Asynch CMOS	O
DMI_RX#[0]	B27	DMI	I
DMI_RX#[1]	B25	DMI	I
DMI_RX#[2]	A25	DMI	I
DMI_RX#[3]	B24	DMI	I
DMI_RX[0]	B28	DMI	I
DMI_RX[1]	B26	DMI	I
DMI_RX[2]	A24	DMI	I
DMI_RX[3]	B23	DMI	I
DMI_TX#[0]	G21	DMI	O
DMI_TX#[1]	E22	DMI	O
DMI_TX#[2]	F21	DMI	O
DMI_TX#[3]	D21	DMI	O
DMI_TX[0]	G22	DMI	O
DMI_TX[1]	D22	DMI	O
DMI_TX[2]	F20	DMI	O
DMI_TX[3]	C21	DMI	O
DPLL_REF_CLK	A16	Diff Clk	I
DPLL_REF_CLK#	A15	Diff Clk	I
eDP_AUX	C15	eDP	I/O
eDP_AUX#	D15	eDP	I/O
eDP_COMPIO	A18	Analog	I
eDP_HPD#	B16	Asynch CMOS	I
eDP_ICOMPO	A17	Analog	I
eDP_TX#[0]	C18	eDP	O
eDP_TX#[1]	E16	eDP	O
eDP_TX#[2]	D16	eDP	O
eDP_TX#[3]	F15	eDP	O
eDP_TX[0]	C17	eDP	O
eDP_TX[1]	F16	eDP	O
eDP_TX[2]	C16	eDP	O
eDP_TX[3]	G15	eDP	O
FDI_INT	H20	Asynch CMOS	I
FDI0_FSYNC	J18	CMOS	I
FDI0_LSYNC	J19	CMOS	I
FDI0_TX#[0]	A21	FDI	O
FDI0_TX#[1]	H19	FDI	O
FDI0_TX#[2]	E19	FDI	O
FDI0_TX#[3]	F18	FDI	O
FDI0_TX[0]	A22	FDI	O
FDI0_TX[1]	G19	FDI	O
FDI0_TX[2]	E20	FDI	O
FDI0_TX[3]	G18	FDI	O
FDI1_FSYNC	J17	CMOS	I
FDI1_LSYNC	H17	CMOS	I
FDI1_TX#[0]	B21	FDI	O
FDI1_TX#[1]	C20	FDI	O
FDI1_TX#[2]	D18	FDI	O
FDI1_TX#[3]	E17	FDI	O
FDI1_TX[0]	B20	FDI	O
FDI1_TX[1]	C19	FDI	O
FDI1_TX[2]	D19	FDI	O
FDI1_TX[3]	F17	FDI	O
KEY	B1	N/A	N/A
PECI	AN33	Asynch	I/O
PEG_ICOMPI	J22	Analog	I
PEG_ICOMPO	J21	Analog	I
PEG_RCOMPO	H22	Analog	I
PEG_RX#[0]	K33	PCIe	I
PEG_RX#[1]	M35	PCIe	I
PEG_RX#[2]	L34	PCIe	I
PEG_RX#[3]	J35	PCIe	I
PEG_RX#[4]	J32	PCIe	I

Table 8-1. rPGA988B Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir
PEG_RX#[5]	H34	PCIe	I
PEG_RX#[6]	H31	PCIe	I
PEG_RX#[7]	G33	PCIe	I
PEG_RX#[8]	G30	PCIe	I
PEG_RX#[9]	F35	PCIe	I
PEG_RX#[10]	E34	PCIe	I
PEG_RX#[11]	E32	PCIe	I
PEG_RX#[12]	D33	PCIe	I
PEG_RX#[13]	D31	PCIe	I
PEG_RX#[14]	B33	PCIe	I
PEG_RX#[15]	C32	PCIe	I
PEG_RX[0]	J33	PCIe	I
PEG_RX[1]	L35	PCIe	I
PEG_RX[2]	K34	PCIe	I
PEG_RX[3]	H35	PCIe	I
PEG_RX[4]	H32	PCIe	I
PEG_RX[5]	G34	PCIe	I
PEG_RX[6]	G31	PCIe	I
PEG_RX[7]	F33	PCIe	I
PEG_RX[8]	F30	PCIe	I
PEG_RX[9]	E35	PCIe	I
PEG_RX[10]	E33	PCIe	I
PEG_RX[11]	F32	PCIe	I
PEG_RX[12]	D34	PCIe	I
PEG_RX[13]	E31	PCIe	I
PEG_RX[14]	C33	PCIe	I
PEG_RX[15]	B32	PCIe	I
PEG_TX#[0]	M29	PCIe	O
PEG_TX#[1]	M32	PCIe	O
PEG_TX#[2]	M31	PCIe	O
PEG_TX#[3]	L32	PCIe	O
PEG_TX#[4]	L29	PCIe	O
PEG_TX#[5]	K31	PCIe	O
PEG_TX#[6]	K28	PCIe	O
PEG_TX#[7]	J30	PCIe	O
PEG_TX#[8]	J28	PCIe	O
PEG_TX#[9]	H29	PCIe	O
PEG_TX#[10]	G27	PCIe	O
PEG_TX#[11]	E29	PCIe	O
PEG_TX#[12]	F27	PCIe	O
PEG_TX#[13]	D28	PCIe	O
PEG_TX#[14]	F26	PCIe	O
PEG_TX#[15]	E25	PCIe	O
PEG_TX[0]	M28	PCIe	O
PEG_TX[1]	M33	PCIe	O
PEG_TX[2]	M30	PCIe	O
PEG_TX[3]	L31	PCIe	O
PEG_TX[4]	L28	PCIe	O
PEG_TX[5]	K30	PCIe	O
PEG_TX[6]	K27	PCIe	O
PEG_TX[7]	J29	PCIe	O
PEG_TX[8]	J27	PCIe	O
PEG_TX[9]	H28	PCIe	O
PEG_TX[10]	G28	PCIe	O
PEG_TX[11]	E28	PCIe	O
PEG_TX[12]	F28	PCIe	O
PEG_TX[13]	D27	PCIe	O
PEG_TX[14]	E26	PCIe	O
PEG_TX[15]	D25	PCIe	O
PM_SYNC	AM34	Asynch CMOS	I
PRDY#	AP29	Asynch CMOS	O
PREQ#	AP27	Asynch CMOS	I
PROC_SELECT#	C26	N/A	O
PROCHOT#	AL32	Asynch CMOS	I/O
RESET#	AR33	Asynch CMOS	I
RSVD	C30		
RSVD	A31		
RSVD	B30		
RSVD	B29		
RSVD	D30		
RSVD	B31		
RSVD	A30		
RSVD	C29		
RSVD	F25		
RSVD	F24		
RSVD	F23		
RSVD	D24		
RSVD	G25		
RSVD	G24		
RSVD	E23		
RSVD	D23		
RSVD	AT26		
RSVD	AG7		
RSVD	AE7		
RSVD	W8		
RSVD	T8		
RSVD	L7		
RSVD	J20		
RSVD	J16		
RSVD	AM33		
RSVD	J15		
RSVD	H16		
RSVD	G16		
RSVD	B18		

Table 8-1. rPGA988B Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir
RSVD	AK32		
RSVD	AK2		
RSVD	AJ32		
RSVD	AJ27		
RSVD	AJ26		
RSVD_NCTF	AT34		
RSVD_NCTF	B35		
RSVD_NCTF	B34		
RSVD_NCTF	A34		
RSVD_NCTF	A33		
RSVD_NCTF	AT33		
RSVD_NCTF	AT2		
RSVD_NCTF	AT1		
RSVD_NCTF	AR35		
RSVD_NCTF	AR34		
RSVD_NCTF	AR1		
RSVD_NCTF	AP35		
RSVD_NCTF	C35		
RSVD_TP	W9		
RSVD_TP	W10		
RSVD_TP	AA4		
RSVD_TP	AA3		
RSVD_TP	AB4		
RSVD_TP	AB3		
RSVD_TP	AG1		
RSVD_TP	AH1		
RSVD_TP	AG2		
RSVD_TP	AH2		
RSVD_TP	T9		
RSVD_TP	T10		
RSVD_TP	AA2		
RSVD_TP	AB1		
RSVD_TP	AB2		
RSVD_TP	AA1		
RSVD_TP	AD6		
RSVD_TP	AE6		
RSVD_TP	AD5		
RSVD_TP	AE5		
SA_BS[0]	AE10	DDR3	O
SA_BS[1]	AF10	DDR3	O
SA_BS[2]	V6	DDR3	O
SA_CAS#	AE8	DDR3	O
SA_CK#[0]	AA6	DDR3	O
SA_CK#[1]	AB5	DDR3	O
SA_CK[0]	AB6	DDR3	O
SA_CK[1]	AA5	DDR3	O
SA_CKE[0]	V9	DDR3	O
SA_CKE[1]	V10	DDR3	O
SA_CS#[0]	AK3	DDR3	O
SA_CS#[1]	AL3	DDR3	O
SA_DIMM_VREFDQ	B4	N/A	O
SA_DQ[0]	C5	DDR3	I/O
SA_DQ[1]	D5	DDR3	I/O
SA_DQ[2]	D3	DDR3	I/O
SA_DQ[3]	D2	DDR3	I/O
SA_DQ[4]	D6	DDR3	I/O
SA_DQ[5]	C6	DDR3	I/O
SA_DQ[6]	C2	DDR3	I/O
SA_DQ[7]	C3	DDR3	I/O
SA_DQ[8]	F10	DDR3	I/O
SA_DQ[9]	F8	DDR3	I/O
SA_DQ[10]	G10	DDR3	I/O
SA_DQ[11]	G9	DDR3	I/O
SA_DQ[12]	F9	DDR3	I/O
SA_DQ[13]	F7	DDR3	I/O
SA_DQ[14]	G8	DDR3	I/O
SA_DQ[15]	G7	DDR3	I/O
SA_DQ[16]	K4	DDR3	I/O
SA_DQ[17]	K5	DDR3	I/O
SA_DQ[18]	K1	DDR3	I/O
SA_DQ[19]	J1	DDR3	I/O
SA_DQ[20]	J5	DDR3	I/O
SA_DQ[21]	J4	DDR3	I/O
SA_DQ[22]	J2	DDR3	I/O
SA_DQ[23]	K2	DDR3	I/O
SA_DQ[24]	M8	DDR3	I/O
SA_DQ[25]	N10	DDR3	I/O
SA_DQ[26]	N8	DDR3	I/O
SA_DQ[27]	N7	DDR3	I/O
SA_DQ[28]	M10	DDR3	I/O
SA_DQ[29]	M9	DDR3	I/O
SA_DQ[30]	N9	DDR3	I/O
SA_DQ[31]	M7	DDR3	I/O
SA_DQ[32]	AG6	DDR3	I/O
SA_DQ[33]	AG5	DDR3	I/O
SA_DQ[34]	AK6	DDR3	I/O
SA_DQ[35]	AK5	DDR3	I/O
SA_DQ[36]	AH5	DDR3	I/O
SA_DQ[37]	AH6	DDR3	I/O
SA_DQ[38]	AJ5	DDR3	I/O
SA_DQ[39]	AJ6	DDR3	I/O
SA_DQ[40]	AJ8	DDR3	I/O
SA_DQ[41]	AK8	DDR3	I/O
SA_DQ[42]	AJ9	DDR3	I/O

Table 8-1. rPGA988B Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir
SA_DQ[43]	AK9	DDR3	I/O
SA_DQ[44]	AH8	DDR3	I/O
SA_DQ[45]	AH9	DDR3	I/O
SA_DQ[46]	AL9	DDR3	I/O
SA_DQ[47]	AL8	DDR3	I/O
SA_DQ[48]	AP11	DDR3	I/O
SA_DQ[49]	AN11	DDR3	I/O
SA_DQ[50]	AL12	DDR3	I/O
SA_DQ[51]	AM12	DDR3	I/O
SA_DQ[52]	AM11	DDR3	I/O
SA_DQ[53]	AL11	DDR3	I/O
SA_DQ[54]	AP12	DDR3	I/O
SA_DQ[55]	AN12	DDR3	I/O
SA_DQ[56]	AJ14	DDR3	I/O
SA_DQ[57]	AH14	DDR3	I/O
SA_DQ[58]	AL15	DDR3	I/O
SA_DQ[59]	AK15	DDR3	I/O
SA_DQ[60]	AL14	DDR3	I/O
SA_DQ[61]	AK14	DDR3	I/O
SA_DQ[62]	AJ15	DDR3	I/O
SA_DQ[63]	AH15	DDR3	I/O
SA_DQS#[0]	C4	DDR3	I/O
SA_DQS#[1]	G6	DDR3	I/O
SA_DQS#[2]	J3	DDR3	I/O
SA_DQS#[3]	M6	DDR3	I/O
SA_DQS#[4]	AL6	DDR3	I/O
SA_DQS#[5]	AM8	DDR3	I/O
SA_DQS#[6]	AR12	DDR3	I/O
SA_DQS#[7]	AM15	DDR3	I/O
SA_DQS[0]	D4	DDR3	I/O
SA_DQS[1]	F6	DDR3	I/O
SA_DQS[2]	K3	DDR3	I/O
SA_DQS[3]	N6	DDR3	I/O
SA_DQS[4]	AL5	DDR3	I/O
SA_DQS[5]	AM9	DDR3	I/O
SA_DQS[6]	AR11	DDR3	I/O
SA_DQS[7]	AM14	DDR3	I/O
SA_MA[0]	AD10	DDR3	O
SA_MA[1]	W1	DDR3	O
SA_MA[2]	W2	DDR3	O
SA_MA[3]	W7	DDR3	O
SA_MA[4]	V3	DDR3	O
SA_MA[5]	V2	DDR3	O
SA_MA[6]	W3	DDR3	O
SA_MA[7]	W6	DDR3	O
SA_MA[8]	V1	DDR3	O
SA_MA[9]	W5	DDR3	O

Table 8-1. rPGA988B Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir
SA_MA[10]	AD8	DDR3	O
SA_MA[11]	V4	DDR3	O
SA_MA[12]	W4	DDR3	O
SA_MA[13]	AF8	DDR3	O
SA_MA[14]	V5	DDR3	O
SA_MA[15]	V7	DDR3	O
SA_ODT[0]	AH3	DDR3	O
SA_ODT[1]	AG3	DDR3	O
SA_RAS#	AD9	DDR3	O
SA_WE#	AF9	DDR3	O
SB_BS[0]	AA9	DDR3	O
SB_BS[1]	AA7	DDR3	O
SB_BS[2]	R6	DDR3	O
SB_CAS#	AA10	DDR3	O
SB_CK#[0]	AD2	DDR3	O
SB_CK#[1]	AD1	DDR3	O
SB_CK[0]	AE2	DDR3	O
SB_CK[1]	AE1	DDR3	O
SB_CKE[0]	R9	DDR3	O
SB_CKE[1]	R10	DDR3	O
SB_CS#[0]	AD3	DDR3	O
SB_CS#[1]	AE3	DDR3	O
SB_DIMM_VREFDQ	D1	N/A	O
SB_DQ[0]	C9	DDR3	I/O
SB_DQ[1]	A7	DDR3	I/O
SB_DQ[2]	D10	DDR3	I/O
SB_DQ[3]	C8	DDR3	I/O
SB_DQ[4]	A9	DDR3	I/O
SB_DQ[5]	A8	DDR3	I/O
SB_DQ[6]	D9	DDR3	I/O
SB_DQ[7]	D8	DDR3	I/O
SB_DQ[8]	G4	DDR3	I/O
SB_DQ[9]	F4	DDR3	I/O
SB_DQ[10]	F1	DDR3	I/O
SB_DQ[11]	G1	DDR3	I/O
SB_DQ[12]	G5	DDR3	I/O
SB_DQ[13]	F5	DDR3	I/O
SB_DQ[14]	F2	DDR3	I/O
SB_DQ[15]	G2	DDR3	I/O
SB_DQ[16]	J7	DDR3	I/O
SB_DQ[17]	J8	DDR3	I/O
SB_DQ[18]	K10	DDR3	I/O
SB_DQ[19]	K9	DDR3	I/O
SB_DQ[20]	J9	DDR3	I/O
SB_DQ[21]	J10	DDR3	I/O
SB_DQ[22]	K8	DDR3	I/O
SB_DQ[23]	K7	DDR3	I/O

Table 8-1. rPGA988B Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir
SB_DQ[24]	M5	DDR3	I/O
SB_DQ[25]	N4	DDR3	I/O
SB_DQ[26]	N2	DDR3	I/O
SB_DQ[27]	N1	DDR3	I/O
SB_DQ[28]	M4	DDR3	I/O
SB_DQ[29]	N5	DDR3	I/O
SB_DQ[30]	M2	DDR3	I/O
SB_DQ[31]	M1	DDR3	I/O
SB_DQ[32]	AM5	DDR3	I/O
SB_DQ[33]	AM6	DDR3	I/O
SB_DQ[34]	AR3	DDR3	I/O
SB_DQ[35]	AP3	DDR3	I/O
SB_DQ[36]	AN3	DDR3	I/O
SB_DQ[37]	AN2	DDR3	I/O
SB_DQ[38]	AN1	DDR3	I/O
SB_DQ[39]	AP2	DDR3	I/O
SB_DQ[40]	AP5	DDR3	I/O
SB_DQ[41]	AN9	DDR3	I/O
SB_DQ[42]	AT5	DDR3	I/O
SB_DQ[43]	AT6	DDR3	I/O
SB_DQ[44]	AP6	DDR3	I/O
SB_DQ[45]	AN8	DDR3	I/O
SB_DQ[46]	AR6	DDR3	I/O
SB_DQ[47]	AR5	DDR3	I/O
SB_DQ[48]	AR9	DDR3	I/O
SB_DQ[49]	AJ11	DDR3	I/O
SB_DQ[50]	AT8	DDR3	I/O
SB_DQ[51]	AT9	DDR3	I/O
SB_DQ[52]	AH11	DDR3	I/O
SB_DQ[53]	AR8	DDR3	I/O
SB_DQ[54]	AJ12	DDR3	I/O
SB_DQ[55]	AH12	DDR3	I/O
SB_DQ[56]	AT11	DDR3	I/O
SB_DQ[57]	AN14	DDR3	I/O
SB_DQ[58]	AR14	DDR3	I/O
SB_DQ[59]	AT14	DDR3	I/O
SB_DQ[60]	AT12	DDR3	I/O
SB_DQ[61]	AN15	DDR3	I/O
SB_DQ[62]	AR15	DDR3	I/O
SB_DQ[63]	AT15	DDR3	I/O
SB_DQS#[0]	D7	DDR3	I/O
SB_DQS#[1]	F3	DDR3	I/O
SB_DQS#[2]	K6	DDR3	I/O
SB_DQS#[3]	N3	DDR3	I/O
SB_DQS#[4]	AN5	DDR3	I/O
SB_DQS#[5]	AP9	DDR3	I/O
SB_DQS#[6]	AK12	DDR3	I/O
SB_DQS#[7]	AP15	DDR3	I/O
SB_DQS[0]	C7	DDR3	I/O
SB_DQS[1]	G3	DDR3	I/O
SB_DQS[2]	J6	DDR3	I/O
SB_DQS[3]	M3	DDR3	I/O
SB_DQS[4]	AN6	DDR3	I/O
SB_DQS[5]	AP8	DDR3	I/O
SB_DQS[6]	AK11	DDR3	I/O
SB_DQS[7]	AP14	DDR3	I/O
SB_MA[0]	AA8	DDR3	O
SB_MA[1]	T7	DDR3	O
SB_MA[2]	R7	DDR3	O
SB_MA[3]	T6	DDR3	O
SB_MA[4]	T2	DDR3	O
SB_MA[5]	T4	DDR3	O
SB_MA[6]	T3	DDR3	O
SB_MA[7]	R2	DDR3	O
SB_MA[8]	T5	DDR3	O
SB_MA[9]	R3	DDR3	O
SB_MA[10]	AB7	DDR3	O
SB_MA[11]	R1	DDR3	O
SB_MA[12]	T1	DDR3	O
SB_MA[13]	AB10	DDR3	O
SB_MA[14]	R5	DDR3	O
SB_MA[15]	R4	DDR3	O
SB_ODT[0]	AE4	DDR3	O
SB_ODT[1]	AD4	DDR3	O
SB_RAS#	AB8	DDR3	O
SB_WE#	AB9	DDR3	O
SKTOCC#	AN34	Analog	O
SM_DRAMPWROK	V8	Asynch CMOS	I
SM_DRAMRST#	R8	DDR3	O
SM_RCOMP[0]	AK1	Analog	I/O
SM_RCOMP[1]	A5	Analog	I/O
SM_RCOMP[2]	A4	Analog	I/O
SM_VREF	AL1	Analog	I
TCK	AR26	CMOS	I
TDI	AR28	CMOS	I
TDO	AP26	CMOS	O
THERMTRIP#	AN32	Asynch CMOS	O
TMS	AR27	CMOS	I
TRST#	AP30	CMOS	I
UNCOREPWRGOOD	AP33	Asynch CMOS	I
VAXG	AH17	PWR	
VAXG	AH18	PWR	
VAXG	AH20	PWR	
VAXG	AH21	PWR	

Table 8-1. rPGA988B Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir
VAXG	AH23	PWR	
VAXG	AH24	PWR	
VAXG	AJ17	PWR	
VAXG	AJ18	PWR	
VAXG	AJ20	PWR	
VAXG	AJ21	PWR	
VAXG	AJ23	PWR	
VAXG	AJ24	PWR	
VAXG	AK17	PWR	
VAXG	AK18	PWR	
VAXG	AK20	PWR	
VAXG	AK21	PWR	
VAXG	AK23	PWR	
VAXG	AK24	PWR	
VAXG	AL17	PWR	
VAXG	AL18	PWR	
VAXG	AL20	PWR	
VAXG	AL21	PWR	
VAXG	AL23	PWR	
VAXG	AL24	PWR	
VAXG	AM17	PWR	
VAXG	AM18	PWR	
VAXG	AM20	PWR	
VAXG	AM21	PWR	
VAXG	AM23	PWR	
VAXG	AM24	PWR	
VAXG	AN17	PWR	
VAXG	AN18	PWR	
VAXG	AN20	PWR	
VAXG	AN21	PWR	
VAXG	AN23	PWR	
VAXG	AN24	PWR	
VAXG	AP17	PWR	
VAXG	AP18	PWR	
VAXG	AP20	PWR	
VAXG	AP21	PWR	
VAXG	AP23	PWR	
VAXG	AP24	PWR	
VAXG	AR17	PWR	
VAXG	AR18	PWR	
VAXG	AR20	PWR	
VAXG	AR21	PWR	
VAXG	AR23	PWR	
VAXG	AR24	PWR	
VAXG	AT17	PWR	
VAXG	AT18	PWR	
VAXG	AT20	PWR	
VAXG	AT21	PWR	
VAXG	AT23	PWR	
VAXG	AT24	PWR	
VAXG_SENSE	AK35	Analog	O
VAXG_VAL_SENSE	AJ31	Analog	O
VCC	AA26	PWR	
VCC	AA27	PWR	
VCC	AA28	PWR	
VCC	AA29	PWR	
VCC	AA30	PWR	
VCC	AA31	PWR	
VCC	AA32	PWR	
VCC	AA33	PWR	
VCC	AA34	PWR	
VCC	AA35	PWR	
VCC	AC26	PWR	
VCC	AC27	PWR	
VCC	AC28	PWR	
VCC	AC29	PWR	
VCC	AC30	PWR	
VCC	AC31	PWR	
VCC	AC32	PWR	
VCC	AC33	PWR	
VCC	AC34	PWR	
VCC	AC35	PWR	
VCC	AD26	PWR	
VCC	AD27	PWR	
VCC	AD28	PWR	
VCC	AD29	PWR	
VCC	AD30	PWR	
VCC	AD31	PWR	
VCC	AD32	PWR	
VCC	AD33	PWR	
VCC	AD34	PWR	
VCC	AD35	PWR	
VCC	AF26	PWR	
VCC	AF27	PWR	
VCC	AF28	PWR	
VCC	AF29	PWR	
VCC	AF30	PWR	
VCC	AF31	PWR	
VCC	AF32	PWR	
VCC	AF33	PWR	
VCC	AF34	PWR	
VCC	AF35	PWR	
VCC	AG26	PWR	
VCC	AG27	PWR	

Table 8-1. rPGA988B Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir
VCC	AG28	PWR	
VCC	AG29	PWR	
VCC	AG30	PWR	
VCC	AG31	PWR	
VCC	AG32	PWR	
VCC	AG33	PWR	
VCC	AG34	PWR	
VCC	AG35	PWR	
VCC	P26	PWR	
VCC	P27	PWR	
VCC	P28	PWR	
VCC	P29	PWR	
VCC	P30	PWR	
VCC	P31	PWR	
VCC	P32	PWR	
VCC	P33	PWR	
VCC	P34	PWR	
VCC	P35	PWR	
VCC	R26	PWR	
VCC	R27	PWR	
VCC	R28	PWR	
VCC	R29	PWR	
VCC	R30	PWR	
VCC	R31	PWR	
VCC	R32	PWR	
VCC	R33	PWR	
VCC	R34	PWR	
VCC	R35	PWR	
VCC	U26	PWR	
VCC	U27	PWR	
VCC	U28	PWR	
VCC	U29	PWR	
VCC	U30	PWR	
VCC	U31	PWR	
VCC	U32	PWR	
VCC	U33	PWR	
VCC	U34	PWR	
VCC	U35	PWR	
VCC	V26	PWR	
VCC	V27	PWR	
VCC	V28	PWR	
VCC	V29	PWR	
VCC	V30	PWR	
VCC	V31	PWR	
VCC	V32	PWR	
VCC	V33	PWR	
VCC	V34	PWR	

Table 8-1. rPGA988B Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir
VCC	V35	PWR	
VCC	Y26	PWR	
VCC	Y27	PWR	
VCC	Y28	PWR	
VCC	Y29	PWR	
VCC	Y30	PWR	
VCC	Y31	PWR	
VCC	Y32	PWR	
VCC	Y33	PWR	
VCC	Y34	PWR	
VCC	Y35	PWR	
VCC_DIE_SENSE	AH27	Analog	O
VCC_SENSE	AJ35	Analog	O
VCC_VAL_SENSE	AJ33	Analog	O
VCCIO	J23	PWR	
VCCIO	A11	PWR	
VCCIO	A12	PWR	
VCCIO	AC10	PWR	
VCCIO	AG10	PWR	
VCCIO	AH10	PWR	
VCCIO	AH13	PWR	
VCCIO	B12	PWR	
VCCIO	C11	PWR	
VCCIO	C12	PWR	
VCCIO	D11	PWR	
VCCIO	D12	PWR	
VCCIO	E11	PWR	
VCCIO	E12	PWR	
VCCIO	F11	PWR	
VCCIO	F12	PWR	
VCCIO	G12	PWR	
VCCIO	H11	PWR	
VCCIO	H12	PWR	
VCCIO	J11	PWR	
VCCIO	J12	PWR	
VCCIO	L10	PWR	
VCCIO	P10	PWR	
VCCIO	U10	PWR	
VCCIO	Y10	PWR	
VCCIO	A13	PWR	
VCCIO	A14	PWR	
VCCIO	B14	PWR	
VCCIO	C13	PWR	
VCCIO	C14	PWR	
VCCIO	D13	PWR	
VCCIO	D14	PWR	
VCCIO	E14	PWR	

Table 8-1. rPGA988B Processor Pin List by Pin Name

Table 8-1. rPGA988B Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir
VCCIO	F13	PWR	
VCCIO	F14	PWR	
VCCIO	G13	PWR	
VCCIO	G14	PWR	
VCCIO	H14	PWR	
VCCIO	J13	PWR	
VCCIO	J14	PWR	
VCCIO_SEL	A19	N/A	O
VCCIO_SENSE	B10	Analog	O
VCCPLL	A2	PWR	
VCCPLL	A6	PWR	
VCCPLL	B6	PWR	
VCCSA	H25	PWR	
VCCSA	H26	PWR	
VCCSA	J24	PWR	
VCCSA	J25	PWR	
VCCSA	J26	PWR	
VCCSA	L26	PWR	
VCCSA	M26	PWR	
VCCSA	M27	PWR	
VCCSA_SENSE	H23	Analog	O
VCCSA_VID[0]	C22	CMOS	O
VCCSA_VID[1]	C24	CMOS	O
VDDQ	AC1	PWR	
VDDQ	AC4	PWR	
VDDQ	AC7	PWR	
VDDQ	AF1	PWR	
VDDQ	AF4	PWR	
VDDQ	AF7	PWR	
VDDQ	P1	PWR	
VDDQ	P4	PWR	
VDDQ	P7	PWR	
VDDQ	U1	PWR	
VDDQ	U4	PWR	
VDDQ	U7	PWR	
VDDQ	Y1	PWR	
VDDQ	Y4	PWR	
VDDQ	Y7	PWR	
VIDALERT#	AJ29	CMOS	I
VIDSCLK	AJ30	CMOS	O
VIDSOUT	AJ28	CMOS	I/O
VSS	A20	GND	
VSS	A23	GND	
VSS	A26	GND	
VSS	A29	GND	
VSS	A3	GND	
VSS	A32	GND	
VSS	A35	GND	
VSS	AB26	GND	
VSS	AB27	GND	
VSS	AB28	GND	
VSS	AB29	GND	
VSS	AB30	GND	
VSS	AB31	GND	
VSS	AB32	GND	
VSS	AB33	GND	
VSS	AB34	GND	
VSS	AB35	GND	
VSS	AC2	GND	
VSS	AC3	GND	
VSS	AC5	GND	
VSS	AC6	GND	
VSS	AC8	GND	
VSS	AC9	GND	
VSS	AD7	GND	
VSS	AE26	GND	
VSS	AE27	GND	
VSS	AE28	GND	
VSS	AE29	GND	
VSS	AE30	GND	
VSS	AE31	GND	
VSS	AE32	GND	
VSS	AE33	GND	
VSS	AE34	GND	
VSS	AE35	GND	
VSS	AE9	GND	
VSS	AF2	GND	
VSS	AF3	GND	
VSS	AF5	GND	
VSS	AF6	GND	
VSS	AG4	GND	
VSS	AG8	GND	
VSS	AG9	GND	
VSS	AH16	GND	
VSS	AH19	GND	
VSS	AH22	GND	
VSS	AH25	GND	
VSS	AH26	GND	
VSS	AH28	GND	
VSS	AH29	GND	
VSS	AH30	GND	
VSS	AH32	GND	
VSS	AH34	GND	
VSS	AH35	GND	

Table 8-1. rPGA988B Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir
VSS	AH4	GND	
VSS	AH7	GND	
VSS	AJ1	GND	
VSS	AJ10	GND	
VSS	AJ13	GND	
VSS	AJ16	GND	
VSS	AJ19	GND	
VSS	AJ2	GND	
VSS	AJ22	GND	
VSS	AJ25	GND	
VSS	AJ3	GND	
VSS	AJ4	GND	
VSS	AJ7	GND	
VSS	AK10	GND	
VSS	AK13	GND	
VSS	AK16	GND	
VSS	AK19	GND	
VSS	AK22	GND	
VSS	AK25	GND	
VSS	AK27	GND	
VSS	AK30	GND	
VSS	AK33	GND	
VSS	AK4	GND	
VSS	AK7	GND	
VSS	AL10	GND	
VSS	AL13	GND	
VSS	AL16	GND	
VSS	AL19	GND	
VSS	AL2	GND	
VSS	AL22	GND	
VSS	AL25	GND	
VSS	AL28	GND	
VSS	AL31	GND	
VSS	AL34	GND	
VSS	AL4	GND	
VSS	AL7	GND	
VSS	AM1	GND	
VSS	AM10	GND	
VSS	AM13	GND	
VSS	AM16	GND	
VSS	AM19	GND	
VSS	AM2	GND	
VSS	AM22	GND	
VSS	AM25	GND	
VSS	AM29	GND	
VSS	AM3	GND	
VSS	AM4	GND	
VSS	AM7	GND	
VSS	AN10	GND	
VSS	AN13	GND	
VSS	AN16	GND	
VSS	AN19	GND	
VSS	AN22	GND	
VSS	AN25	GND	
VSS	AN27	GND	
VSS	AN30	GND	
VSS	AN4	GND	
VSS	AN7	GND	
VSS	AP1	GND	
VSS	AP10	GND	
VSS	AP13	GND	
VSS	AP16	GND	
VSS	AP19	GND	
VSS	AP22	GND	
VSS	AP25	GND	
VSS	AP28	GND	
VSS	AP31	GND	
VSS	AP34	GND	
VSS	AP4	GND	
VSS	AP7	GND	
VSS	AR10	GND	
VSS	AR13	GND	
VSS	AR16	GND	
VSS	AR19	GND	
VSS	AR2	GND	
VSS	AR22	GND	
VSS	AR25	GND	
VSS	AR4	GND	
VSS	AR7	GND	
VSS	AT10	GND	
VSS	AT13	GND	
VSS	AT16	GND	
VSS	AT19	GND	
VSS	AT22	GND	
VSS	AT25	GND	
VSS	AT27	GND	
VSS	AT29	GND	
VSS	AT3	GND	
VSS	AT32	GND	
VSS	AT35	GND	
VSS	AT4	GND	
VSS	AT7	GND	
VSS	B11	GND	
VSS	B13	GND	

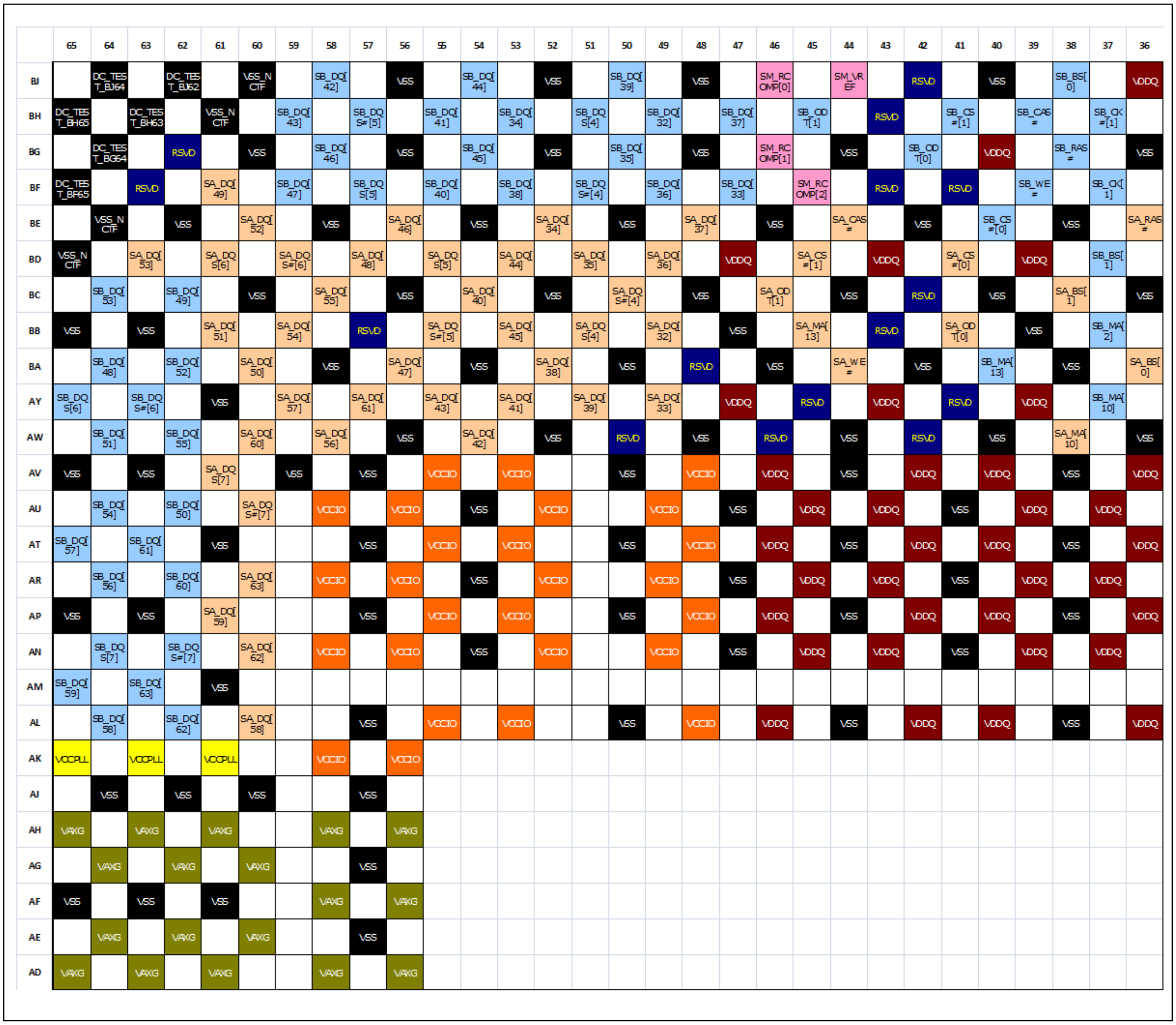
Table 8-1. rPGA988B Processor Pin List by Pin Name

Pin Name	Pin #	Buffer Type	Dir
VSS	B15	GND	
VSS	B17	GND	
VSS	B19	GND	
VSS	B2	GND	
VSS	B22	GND	
VSS	B3	GND	
VSS	B5	GND	
VSS	B7	GND	
VSS	B8	GND	
VSS	B9	GND	
VSS	C1	GND	
VSS	C10	GND	
VSS	C23	GND	
VSS	C25	GND	
VSS	C27	GND	
VSS	C28	GND	
VSS	C31	GND	
VSS	C34	GND	
VSS	D17	GND	
VSS	D20	GND	
VSS	D26	GND	
VSS	D29	GND	
VSS	D32	GND	
VSS	D35	GND	
VSS	E1	GND	
VSS	E10	GND	
VSS	E13	GND	
VSS	E15	GND	
VSS	E18	GND	
VSS	E2	GND	
VSS	E21	GND	
VSS	E24	GND	
VSS	E27	GND	
VSS	E3	GND	
VSS	E30	GND	
VSS	E4	GND	
VSS	E5	GND	
VSS	E6	GND	
VSS	E7	GND	
VSS	E8	GND	
VSS	E9	GND	
VSS	F19	GND	
VSS	F22	GND	
VSS	F29	GND	
VSS	F31	GND	
VSS	F34	GND	
VSS	G11	GND	
VSS	G17	GND	
VSS	G20	GND	
VSS	G23	GND	
VSS	G26	GND	
VSS	G29	GND	
VSS	G32	GND	
VSS	G35	GND	
VSS	H1	GND	
VSS	H10	GND	
VSS	H13	GND	
VSS	H15	GND	
VSS	H18	GND	
VSS	H2	GND	
VSS	H21	GND	
VSS	H24	GND	
VSS	H27	GND	
VSS	H3	GND	
VSS	H30	GND	
VSS	H33	GND	
VSS	H4	GND	
VSS	H5	GND	
VSS	H6	GND	
VSS	H7	GND	
VSS	H8	GND	
VSS	H9	GND	
VSS	J31	GND	
VSS	J34	GND	
VSS	K26	GND	
VSS	K29	GND	
VSS	K32	GND	
VSS	K35	GND	
VSS	L1	GND	
VSS	L2	GND	
VSS	L27	GND	
VSS	L3	GND	
VSS	L30	GND	
VSS	L33	GND	
VSS	L4	GND	
VSS	L5	GND	
VSS	L6	GND	
VSS	L8	GND	
VSS	L9	GND	
VSS	M34	GND	
VSS	N26	GND	
VSS	N27	GND	
VSS	N28	GND	
VSS	N29	GND	

Table 8-1. rPGA988B Processor Pin List by Pin Name

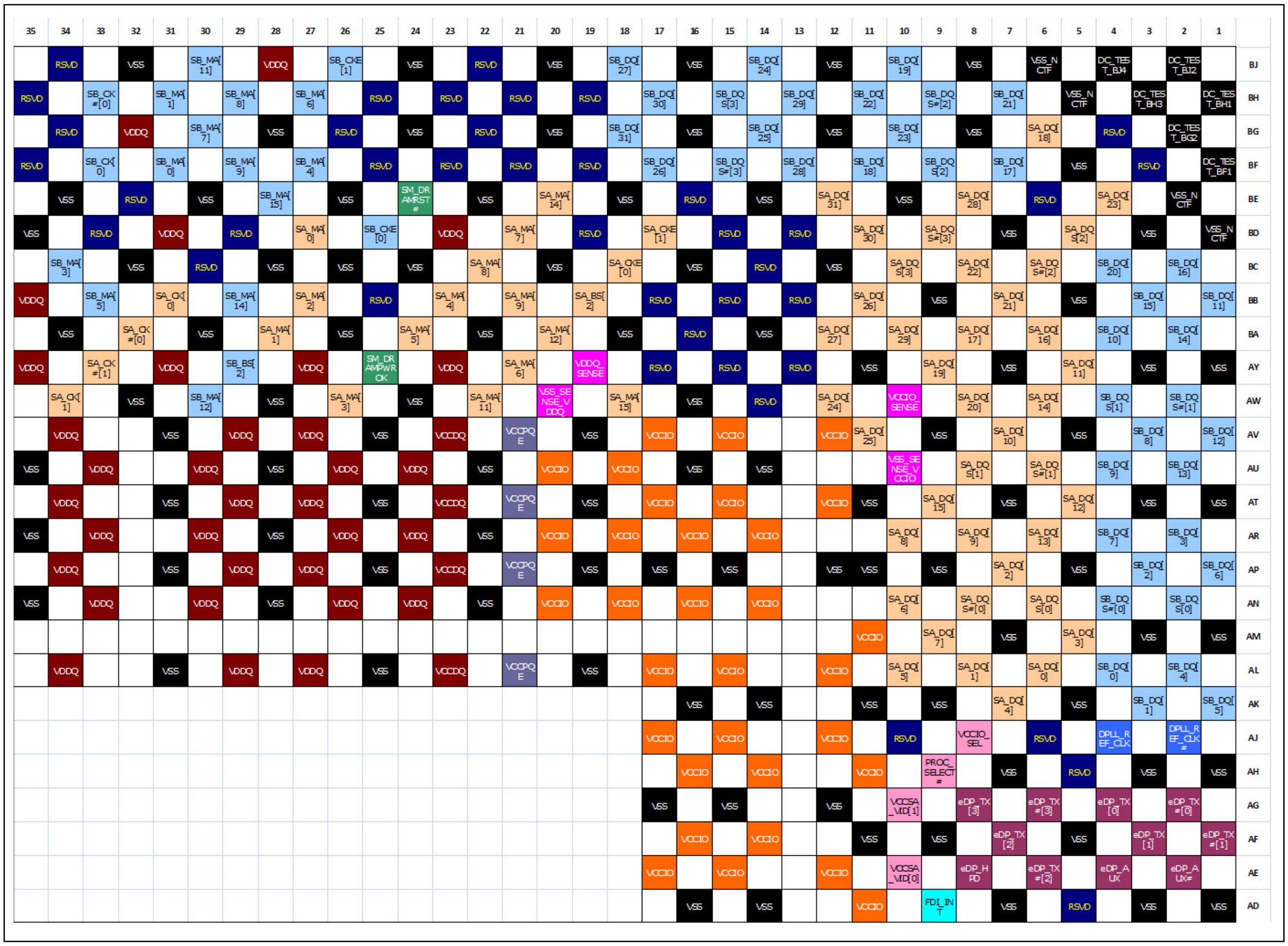
Pin Name	Pin #	Buffer Type	Dir
VSS	N30	GND	
VSS	N31	GND	
VSS	N32	GND	
VSS	N33	GND	
VSS	N34	GND	
VSS	N35	GND	
VSS	P2	GND	
VSS	P3	GND	
VSS	P5	GND	
VSS	P6	GND	
VSS	P8	GND	
VSS	P9	GND	
VSS	T26	GND	
VSS	T27	GND	
VSS	T28	GND	
VSS	T29	GND	
VSS	T30	GND	
VSS	T31	GND	
VSS	T32	GND	
VSS	T33	GND	
VSS	T34	GND	
VSS	T35	GND	
VSS	U2	GND	
VSS	U3	GND	
VSS	U5	GND	
VSS	U6	GND	
VSS	U8	GND	
VSS	U9	GND	
VSS	W26	GND	
VSS	W27	GND	
VSS	W28	GND	
VSS	W29	GND	
VSS	W30	GND	
VSS	W31	GND	
VSS	W32	GND	
VSS	W33	GND	
VSS	W34	GND	
VSS	W35	GND	
VSS	Y2	GND	
VSS	Y3	GND	
VSS	Y5	GND	
VSS	Y6	GND	
VSS	Y8	GND	
VSS	Y9	GND	
VSS_SENSE	AJ34	Analog	O
VSS_SENSE_VCCIO	A10	Analog	O
VSS_VAL_SENSE	AH33	Analog	O
VSSAXG_SENSE	AK34	Analog	O
VSSAXG_VAL_SENSE	AH31	Analog	O

Figure 8-5. BGA1224 Ballmap (Top View, Upper-Left Quadrant)



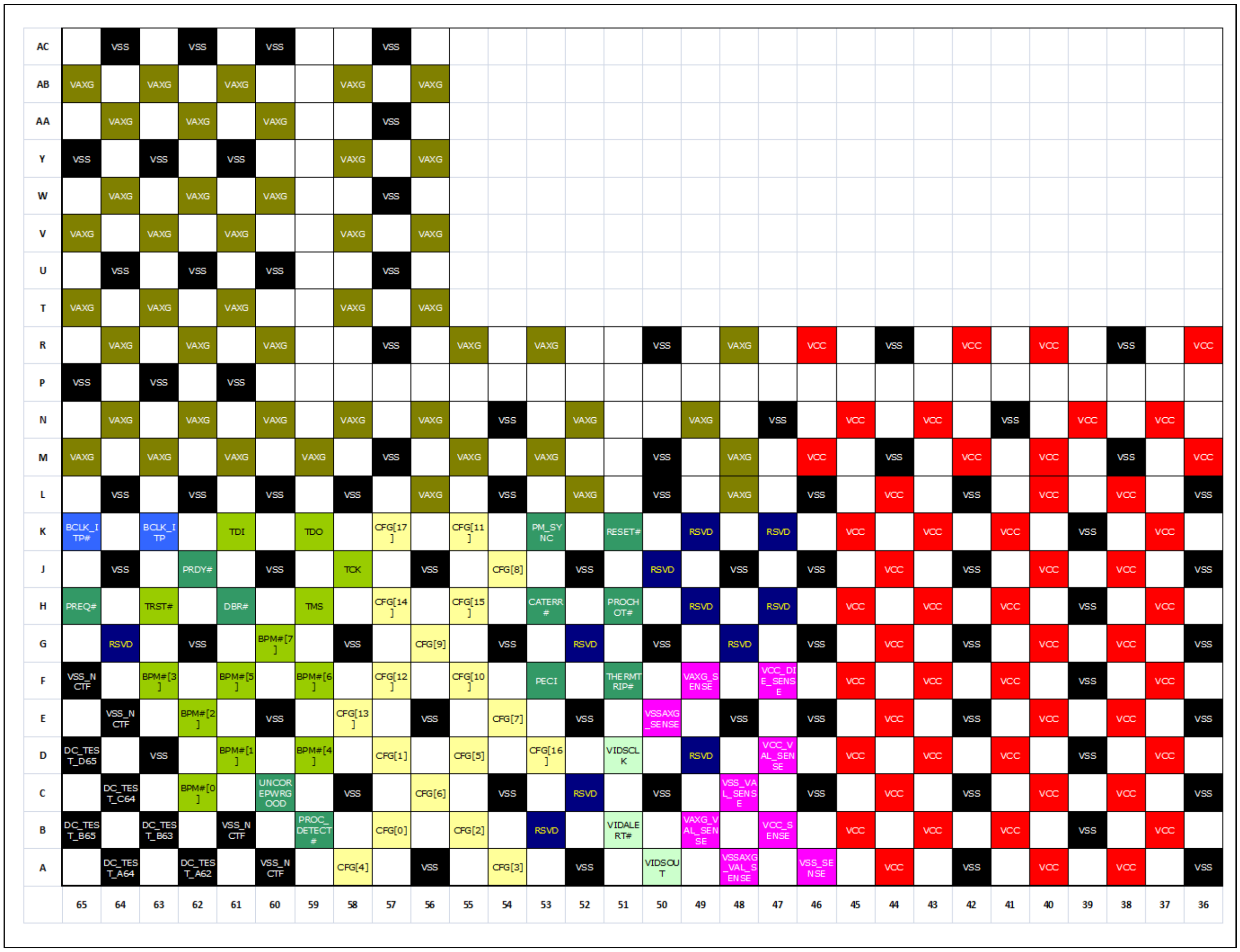
	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36
BJ		DC_TEST_BJ64		DC_TEST_BJ62		VSS_NCTF		SB_DQ[42]		VSS		SB_DQ[44]		VSS		SB_DQ[39]		VSS		SM_RCOMP[0]		SM_VREF		RSVD		VSS		SB_BS[0]		VDDQ
BH	DC_TEST_BH65		DC_TEST_BH63		VSS_NCTF		SB_DQ[43]		SB_DQS#[5]		SB_DQ[41]		SB_DQ[34]		SB_DQS[4]		SB_DQ[32]		SB_DQ[37]		SB_ODT[1]		RSVD		SB_CS#[1]		SB_CAS#		SB_CK#[1]	
BG		DC_TEST_BG64		RSVD		VSS		SB_DQ[46]		VSS		SB_DQ[45]		VSS		SB_DQ[35]		VSS		SM_RCOMP[1]		VSS		SB_ODT[0]		VDDQ		SB_RAS#		VSS
BF	DC_TEST_BF65		RSVD		SA_DQ[49]		SB_DQ[47]		SB_DQS[5]		SB_DQ[40]		SB_DQ[38]		SB_DQS#[4]		SB_DQ[36]		SB_DQ[33]		SM_RCOMP[2]		RSVD		RSVD		SB_WE#		SB_CK[1]	
BE		VSS_NCTF		VSS		SA_DQ[52]		VSS		SA_DQ[46]		VSS		SA_DQ[34]		VSS		SA_DQ[37]		VSS		SA_CAS#		VSS		SB_CS#[0]		VSS		SA_RAS#
BD	VSS_NCTF		SA_DQ[53]		SA_DQS[6]		SA_DQS#[6]		SA_DQ[48]		SA_DQS[5]		SA_DQ[44]		SA_DQ[35]		SA_DQ[36]		VDDQ		SA_CS#[1]		VDDQ		SA_CS#[0]		VDDQ		SB_BS[1]	
BC		SB_DQ[53]		SB_DQ[49]		VSS		SA_DQ[55]		VSS		SA_DQ[40]		VSS		SA_DQS#[4]		VSS		SA_ODT[1]		VSS		RSVD		VSS		SA_BS[1]		VSS
BB	VSS		VSS		SA_DQ[51]		SA_DQ[54]		RSVD		SA_DQS#[5]		SA_DQ[45]		SA_DQS[4]		SA_DQ[32]		VSS		SA_MA[13]		RSVD		SA_ODT[0]		VSS		SB_MA[2]	
BA		SB_DQ[48]		SB_DQ[52]		SA_DQ[50]		VSS		SA_DQ[47]		VSS		SA_DQ[38]		VSS		RSVD		VSS		SA_WE#		VSS		SB_MA[13]		VSS		SA_BS[0]
AY	SB_DQS[6]		SB_DQS#[6]		VSS		SA_DQ[57]		SA_DQ[61]		SA_DQ[43]		SA_DQ[41]		SA_DQ[39]		SA_DQ[33]		VDDQ		RSVD		VDDQ		RSVD		VDDQ		SB_MA[10]	
AW		SB_DQ[51]		SB_DQ[55]		SA_DQ[60]		SA_DQ[56]		VSS		SA_DQ[42]		VSS		RSVD		VSS		RSVD		VSS		RSVD		VSS		SA_MA[10]		VSS
AV	VSS		VSS		SA_DQS[7]		VSS		VSS		VCCIO		VCCIO			VSS		VCCIO		VDDQ		VSS		VDDQ		VDDQ		VSS		VDDQ
AU		SB_DQ[54]		SB_DQ[50]		SA_DQS#[7]		VCCIO		VCCIO		VSS		VCCIO			VCCIO		VSS		VDDQ		VDDQ		VSS		VDDQ		VDDQ	
AT	SB_DQ[57]		SB_DQ[61]		VSS				VSS		VCCIO		VCCIO			VSS		VCCIO		VDDQ		VSS		VDDQ		VDDQ		VSS		VDDQ
AR		SB_DQ[56]		SB_DQ[60]		SA_DQ[63]		VCCIO		VCCIO		VSS		VCCIO			VCCIO		VSS		VDDQ		VDDQ		VSS		VDDQ		VDDQ	
AP	VSS		VSS		SA_DQ[59]				VSS		VCCIO		VCCIO			VSS		VCCIO		VDDQ		VSS		VDDQ		VDDQ		VSS		VDDQ
AN		SB_DQS[7]		SB_DQS#[7]		SA_DQ[62]		VCCIO		VCCIO		VSS		VCCIO			VCCIO		VSS		VDDQ		VDDQ		VSS		VDDQ		VDDQ	
AM	SB_DQ[59]		SB_DQ[63]		VSS																									
AL		SB_DQ[58]		SB_DQ[62]		SA_DQ[58]			VSS		VCCIO		VCCIO			VSS		VCCIO		VDDQ		VSS		VDDQ		VDDQ		VSS		VDDQ
AK	VCCPLL		VCCPLL		VCCPLL			VCCIO		VCCIO																				
AJ		VSS		VSS		VSS			VSS																					
AH	VAXG		VAXG		VAXG			VAXG		VAXG																				
AG		VAXG		VAXG		VAXG			VSS																					
AF	VSS		VSS		VSS			VAXG		VAXG																				
AE		VAXG		VAXG		VAXG			VSS																					
AD	VAXG		VAXG		VAXG			VAXG		VAXG																				

Figure 8-6. BGA1224 Ballmap (Top View, Upper-Right Quadrant)



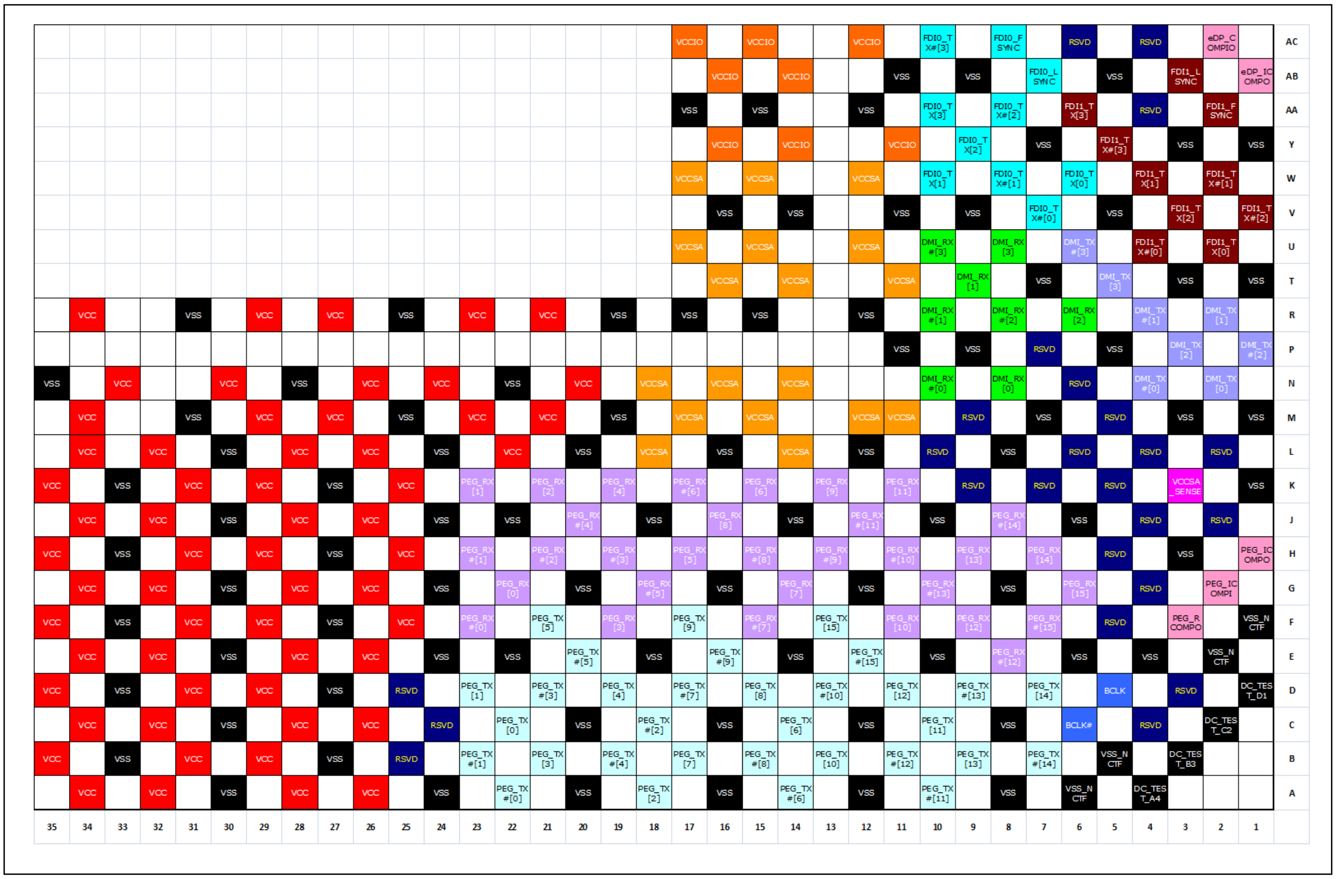
35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
	RSVD		VSS		SB_MA[11]		VDDQ		SB_CKE[1]		VSS		RSVD		VSS		SB_DQ[27]		VSS		SB_DQ[24]		VSS		SB_DQ[19]		VSS		VSS_NCTF		DC_TEST_BJ4		DC_TEST_BJ2		BJ
RSVD		SB_CK#[0]		SB_MA[1]		SB_MA[8]		SB_MA[6]		RSVD		RSVD		RSVD		RSVD		SB_DQ[30]		SB_DQS[3]		SB_DQ[29]		SB_DQ[22]		SB_DQS#[2]		SB_DQ[21]		VSS_NCTF		DC_TEST_BH3		DC_TEST_BH1	BH
	RSVD		VDDQ		SB_MA[7]		VSS		RSVD		VSS		RSVD		VSS		SB_DQ[31]		VSS		SB_DQ[25]		VSS		SB_DQ[23]		VSS		SA_DQ[18]		RSVD		DC_TEST_BG2		BG
RSVD		SB_CK[0]		SB_MA[0]		SB_MA[9]		SB_MA[4]		RSVD		RSVD		RSVD		RSVD		SB_DQ[26]		SB_DQS#[3]		SB_DQ[28]		SB_DQ[18]		SB_DQS[2]		SB_DQ[17]		VSS		RSVD		DC_TEST_BF1	BF
	VSS		RSVD		VSS		SB_MA[15]		VSS		SM_DRAMRST#		VSS		SA_MA[14]		VSS		RSVD		VSS		SA_DQ[31]		VSS		SA_DQ[28]		RSVD		SA_DQ[23]		VSS_NCTF		BE
VSS		RSVD		VDDQ		RSVD		SA_MA[0]		SB_CKE[0]		VDDQ		SA_MA[7]		RSVD		SA_CKE[1]		RSVD		RSVD		SA_DQ[30]		SA_DQS#[3]		VSS		SA_DQS[2]		VSS		VSS_NCTF	BD
	SB_MA[3]		VSS		RSVD		VSS		VSS		VSS		SA_MA[8]		VSS		SA_CKE[0]		VSS		RSVD		VSS		SA_DQS[3]		SA_DQ[22]		SA_DQS#[2]		SB_DQ[20]		SB_DQ[16]		BC
VDDQ		SB_MA[5]		SA_CK[0]		SB_MA[14]		SA_MA[2]		RSVD		SA_MA[4]		SA_MA[9]		SA_BS[2]		RSVD		RSVD		RSVD		SA_DQ[26]		VSS		SA_DQ[21]		VSS		SB_DQ[15]		SB_DQ[11]	BB
	VSS		SA_CK#[0]		VSS		SA_MA[1]		VSS		SA_MA[5]		VSS		SA_MA[12]		VSS		RSVD		VSS		SA_DQ[27]		SA_DQ[29]		SA_DQ[17]		SA_DQ[16]		SB_DQ[10]		SB_DQ[14]		BA
VDDQ		SA_CK#[1]		VDDQ		SB_BS[2]		VDDQ		SM_DRAMPWROK		VDDQ		SA_MA[6]		VDDQ_SENSE		RSVD		RSVD		RSVD		VSS		SA_DQ[19]		VSS		SA_DQ[11]		VSS		VSS	AY
	SA_CK[1]		VSS		SB_MA[12]		VSS		SA_MA[3]		VSS		SA_MA[11]		VSS_SENSE_VDDQ		SA_MA[15]		VSS		RSVD		SA_DQ[24]		VCCIO_SENSE		SA_DQ[20]		SA_DQ[14]		SB_DQS[1]		SB_DQS#[1]		AW
	VDDQ			VSS		VDDQ		VDDQ		VSS		VCCDQ		VCCPQE		VSS		VCCIO		VCCIO			VCCIO	SA_DQ[25]		VSS		SA_DQ[10]		VSS		SB_DQ[8]		SB_DQ[12]	AV
VSS		VDDQ			VDDQ		VSS		VDDQ		VDDQ		VSS		VCCIO		VCCIO		VSS		VSS				VSS_SENSE_VCCIO		SA_DQS[1]		SA_DQS#[1]		SB_DQ[9]		SB_DQ[13]		AU
	VDDQ			VSS		VDDQ		VDDQ		VSS		VCCDQ		VCCPQE		VSS		VCCIO		VCCIO			VCCIO	VSS		SA_DQ[15]		VSS		SA_DQ[12]		VSS		VSS	AT
VSS		VDDQ			VDDQ		VSS		VDDQ		VDDQ		VSS		VCCIO		VCCIO		VCCIO		VCCIO				SA_DQ[8]		SA_DQ[9]		SA_DQ[13]		SB_DQ[7]		SB_DQ[3]		AR
	VDDQ			VSS		VDDQ		VDDQ		VSS		VCCDQ		VCCPQE		VSS		VSS		VSS			VSS	VSS		VSS		SA_DQ[2]		VSS		SB_DQ[2]		SB_DQ[6]	AP
VSS		VDDQ			VDDQ		VSS		VDDQ		VDDQ		VSS		VCCIO		VCCIO		VCCIO		VCCIO				SA_DQ[6]		SA_DQS#[0]		SA_DQS[0]		SB_DQS#[0]		SB_DQS[0]		AN
																								VCCIO		SA_DQ[7]		VSS		SA_DQ[3]		VSS		VSS	AM
	VDDQ			VSS		VDDQ		VDDQ		VSS		VCCDQ		VCCPQE		VSS		VCCIO		VCCIO			VCCIO		SA_DQ[5]		SA_DQ[1]		SA_DQ[0]		SB_DQ[0]		SB_DQ[4]		AL
																			VSS		VSS			VSS		VSS		SA_DQ[4]		VSS		SB_DQ[1]		SB_DQ[5]	AK
																		VCCIO		VCCIO			VCCIO		RSVD		VCCIO_SEL		RSVD		DPLL_REF_CLK		DPLL_REF_CLK#		AJ
																			VCCIO		VCCIO			VCCIO		PROC_SELECT#		VSS		RSVD		VSS		VSS	AH
																		VSS		VSS			VSS		VCCSA_VID[1]		eDP_TX[3]		eDP_TX#[3]		eDP_TX[0]		eDP_TX#[0]		AG
																			VCCIO		VCCIO			VSS		VSS		eDP_TX[2]		VSS		eDP_TX[1]		eDP_TX#[1]	AF
																		VCCIO		VCCIO			VCCIO		VCCSA_VID[0]		eDP_HPD		eDP_TX#[2]		eDP_AUX		eDP_AUX#		AE
																			VSS		VSS			VCCIO		FDI_INT		VSS		RSVD		VSS		VSS	AD

Figure 8-7. BGA1224 Ballmap (Top View, Lower-Left Quadrant)



AC		VSS		VSS		VSS			VSS																					
AB	VAXG		VAXG		VAXG			VAXG		VAXG																				
AA		VAXG		VAXG		VAXG			VSS																					
Y	VSS		VSS		VSS			VAXG		VAXG																				
W		VAXG		VAXG		VAXG			VSS																					
V	VAXG		VAXG		VAXG			VAXG		VAXG																				
U		VSS		VSS		VSS			VSS																					
T	VAXG		VAXG		VAXG			VAXG		VAXG																				
R		VAXG		VAXG		VAXG			VSS		VAXG		VAXG			VSS		VAXG		VCC		VSS		VCC		VCC		VSS		VCC
P	VSS		VSS		VSS																									
N		VAXG		VAXG		VAXG		VAXG		VAXG		VSS		VAXG			VAXG		VSS		VCC		VCC		VSS		VCC		VCC	
M	VAXG		VAXG		VAXG		VAXG		VSS		VAXG		VAXG			VSS		VAXG		VCC		VSS		VCC		VCC		VSS		VCC
L		VSS		VSS		VSS		VSS		VAXG		VSS		VAXG		VSS		VAXG		VSS		VCC		VSS		VCC		VCC		VSS
K	BCLK_ITP#		BCLK_ITP		TDI		TDO		CFG[17]		CFG[11]		PM_SYNC		RESET#		RSVD		RSVD		VCC		VCC		VCC		VSS		VCC	
J		VSS		PRDY#		VSS		TCK		VSS		CFG[8]		VSS		RSVD		VSS		VSS		VCC		VSS		VCC		VCC		VSS
H	PREQ#		TRST#		DBR#		TMS		CFG[14]		CFG[15]		CATERR#		PROCHOT#		RSVD		RSVD		VCC		VCC		VCC		VSS		VCC	
G		RSVD		VSS		BPM#[7]		VSS		CFG[9]		VSS		RSVD		VSS		RSVD		VSS		VCC		VSS		VCC		VCC		VSS
F	VSS_NCTF		BPM#[3]		BPM#[5]		BPM#[6]		CFG[12]		CFG[10]		PECI		THERMTRIP#		VAXG_SENSE		VCC_DIE_SENSE		VCC		VCC		VCC		VSS		VCC	
E		VSS_NCTF		BPM#[2]		VSS		CFG[13]		VSS		CFG[7]		VSS		VSSAXG_SENSE		VSS		VSS		VCC		VSS		VCC		VCC		VSS
D	DC_TEST_D65		VSS		BPM#[1]		BPM#[4]		CFG[1]		CFG[5]		CFG[16]		VIDSCLK		RSVD		VCC_VAL_SENSE		VCC		VCC		VCC		VSS		VCC	
C		DC_TEST_C64		BPM#[0]		UNCOREPWRGOOD		VSS		CFG[6]		VSS		RSVD		VSS		VSS_VAL_SENSE		VSS		VCC		VSS		VCC		VCC		VSS
B	DC_TEST_B65		DC_TEST_B63		VSS_NCTF		PROC_DETECT#		CFG[0]		CFG[2]		RSVD		VIDALERT#		VAXG_VAL_SENSE		VCC_SENSE		VCC		VCC		VCC		VSS		VCC	
A		DC_TEST_A64		DC_TEST_A62		VSS_NCTF		CFG[4]		VSS		CFG[3]		VSS		VIDSOUT		VSSAXG_VAL_SENSE		VSS_SENSE		VCC		VSS		VCC		VCC		VSS
	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36

Figure 8-8. BGA1224 Ballmap (Top View, Lower-Right Quadrant)



																		VCCIO		VCCIO			VCCIO		FDI0_TX#[3]		FDI0_FSYNC		RSVD		RSVD		eDP_COMPIO		AC
																			VCCIO		VCCIO			VSS		VSS		FDI0_LSYNC		VSS		FDI1_LSYNC		eDP_ICOMPO	AB
																		VSS		VSS			VSS		FDI0_TX[3]		FDI0_TX#[2]		FDI1_TX[3]		RSVD		FDI1_FSYNC		AA
																			VCCIO		VCCIO			VCCIO		FDI0_TX[2]		VSS		FDI1_TX#[3]		VSS		VSS	Y
																		VCCSA		VCCSA			VCCSA		FDI0_TX[1]		FDI0_TX#[1]		FDI0_TX[0]		FDI1_TX[1]		FDI1_TX#[1]		W
																			VSS		VSS			VSS		VSS		FDI0_TX#[0]		VSS		FDI1_TX[2]		FDI1_TX#[2]	V
																		VCCSA		VCCSA			VCCSA		DMI_RX#[3]		DMI_RX[3]		DMI_TX#[3]		FDI1_TX#[0]		FDI1_TX[0]		U
																			VCCSA		VCCSA			VCCSA		DMI_RX[1]		VSS		DMI_TX[3]		VSS		VSS	T
	VCC			VSS		VCC		VCC		VSS		VCC		VCC		VSS		VSS		VSS			VSS		DMI_RX#[1]		DMI_RX#[2]		DMI_RX[2]		DMI_TX#[1]		DMI_TX[1]		R
																								VSS		VSS		RSVD		VSS		DMI_TX[2]		DMI_TX#[2]	P
VSS		VCC			VCC		VSS		VCC		VCC		VSS		VCC		VCCSA		VCCSA		VCCSA				DMI_RX#[0]		DMI_RX[0]		RSVD		DMI_TX#[0]		DMI_TX[0]		N
	VCC			VSS		VCC		VCC		VSS		VCC		VCC		VSS		VCCSA		VCCSA			VCCSA	VCCSA		RSVD		VSS		RSVD		VSS		VSS	M
	VCC		VCC		VSS		VCC		VCC		VSS		VCC		VSS		VCCSA		VSS		VCCSA		VSS		RSVD		VSS		RSVD		RSVD		RSVD		L
VCC		VSS		VCC		VCC		VSS		VCC		PEG_RX[1]		PEG_RX[2]		PEG_RX[4]		PEG_RX#[6]		PEG_RX[6]		PEG_RX[9]		PEG_RX[11]		RSVD		RSVD		RSVD		VCCSA_SENSE		VSS	K
	VCC		VCC		VSS		VCC		VCC		VSS		VSS		PEG_RX#[4]		VSS		PEG_RX[8]		VSS		PEG_RX#[11]		VSS		PEG_RX#[14]		VSS		RSVD		RSVD		J
VCC		VSS		VCC		VCC		VSS		VCC		PEG_RX#[1]		PEG_RX#[2]		PEG_RX#[3]		PEG_RX[5]		PEG_RX#[8]		PEG_RX#[9]		PEG_RX#[10]		PEG_RX[13]		PEG_RX[14]		RSVD		VSS		PEG_ICOMPO	H
	VCC		VCC		VSS		VCC		VCC		VSS		PEG_RX[0]		VSS		PEG_RX#[5]		VSS		PEG_RX[7]		VSS		PEG_RX#[13]		VSS		PEG_RX[15]		RSVD		PEG_ICOMPI		G
VCC		VSS		VCC		VCC		VSS		VCC		PEG_RX#[0]		PEG_TX[5]		PEG_RX[3]		PEG_TX[9]		PEG_RX#[7]		PEG_TX[15]		PEG_RX[10]		PEG_RX[12]		PEG_RX#[15]		RSVD		PEG_RCOMPO		VSS_NCTF	F
	VCC		VCC		VSS		VCC		VCC		VSS		VSS		PEG_TX#[5]		VSS		PEG_TX#[9]		VSS		PEG_TX#[15]		VSS		PEG_RX#[12]		VSS		VSS		VSS_NCTF		E
VCC		VSS		VCC		VCC		VSS		RSVD		PEG_TX[1]		PEG_TX#[3]		PEG_TX[4]		PEG_TX#[7]		PEG_TX[8]		PEG_TX#[10]		PEG_TX[12]		PEG_TX#[13]		PEG_TX[14]		BCLK		RSVD		DC_TEST_D1	D
	VCC		VCC		VSS		VCC		VCC		RSVD		PEG_TX[0]		VSS		PEG_TX#[2]		VSS		PEG_TX[6]		VSS		PEG_TX[11]		VSS		BCLK#		RSVD		DC_TEST_C2		C
VCC		VSS		VCC		VCC		VSS		RSVD		PEG_TX#[1]		PEG_TX[3]		PEG_TX#[4]		PEG_TX[7]		PEG_TX#[8]		PEG_TX[10]		PEG_TX#[12]		PEG_TX[13]		PEG_TX#[14]		VSS_NCTF		DC_TEST_B3			B
	VCC		VCC		VSS		VCC		VCC		VSS		PEG_TX#[0]		VSS		PEG_TX[2]		VSS		PEG_TX#[6]		VSS		PEG_TX#[11]		VSS		VSS_NCTF		DC_TEST_A4				A
35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
BCLK	D5	Diff Clk	I
BCLK#	C6	Diff Clk	I
BCLK_ITP	K63	Diff Clk	I
BCLK_ITP#	K65	Diff Clk	I
BPM#[0]	C62	Asynch CMOS	I/O
BPM#[1]	D61	Asynch CMOS	I/O
BPM#[2]	E62	Asynch CMOS	I/O
BPM#[3]	F63	Asynch CMOS	I/O
BPM#[4]	D59	Asynch CMOS	I/O
BPM#[5]	F61	Asynch CMOS	I/O
BPM#[6]	F59	Asynch CMOS	I/O
BPM#[7]	G60	Asynch CMOS	I/O
CATERR#	H53	Asynch CMOS	O
CFG[0]	B57	CMOS	I
CFG[1]	D57	CMOS	I
CFG[2]	B55	CMOS	I
CFG[3]	A54	CMOS	I
CFG[4]	A58	CMOS	I
CFG[5]	D55	CMOS	I
CFG[6]	C56	CMOS	I
CFG[7]	E54	CMOS	I
CFG[8]	J54	CMOS	I
CFG[9]	G56	CMOS	I
CFG[10]	F55	CMOS	I
CFG[11]	K55	CMOS	I
CFG[12]	F57	CMOS	I
CFG[13]	E58	CMOS	I
CFG[14]	H57	CMOS	I
CFG[15]	H55	CMOS	I
CFG[16]	D53	CMOS	I
CFG[17]	K57	CMOS	I
DBR#	H61	Asynch CMOS	O
DC_TEST_A4	A4	N/A	
DC_TEST_A62	A62	N/A	
DC_TEST_A64	A64	N/A	
DC_TEST_B3	B3	N/A	
DC_TEST_B63	B63	N/A	
DC_TEST_B65	B65	N/A	
DC_TEST_BF1	BF1	N/A	
DC_TEST_BF65	BF65	N/A	
DC_TEST_BG2	BG2	N/A	
DC_TEST_BG64	BG64	N/A	
DC_TEST_BH1	BH1	N/A	

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
DC_TEST_BH3	BH3	N/A	
DC_TEST_BH63	BH63	N/A	
DC_TEST_BH65	BH65	N/A	
DC_TEST_BJ2	BJ2	N/A	
DC_TEST_BJ4	BJ4	N/A	
DC_TEST_BJ62	BJ62	N/A	
DC_TEST_BJ64	BJ64	N/A	
DC_TEST_C2	C2	N/A	
DC_TEST_C64	C64	N/A	
DC_TEST_D1	D1	N/A	
DC_TEST_D65	D65	N/A	
DMI_RX#[0]	N10	DMI	I
DMI_RX#[1]	R10	DMI	I
DMI_RX#[2]	R8	DMI	I
DMI_RX#[3]	U10	DMI	I
DMI_RX[0]	N8	DMI	I
DMI_RX[1]	T9	DMI	I
DMI_RX[2]	R6	DMI	I
DMI_RX[3]	U8	DMI	I
DMI_TX#[0]	N4	DMI	O
DMI_TX#[1]	R4	DMI	O
DMI_TX#[2]	P1	DMI	O
DMI_TX#[3]	U6	DMI	O
DMI_TX[0]	N2	DMI	O
DMI_TX[1]	R2	DMI	O
DMI_TX[2]	P3	DMI	O
DMI_TX[3]	T5	DMI	O
DPLL_REF_CLK	AJ4	Diff Clk	I
DPLL_REF_CLK#	AJ2	Diff Clk	I
eDP_AUX	AE4	eDP	I/O
eDP_AUX#	AE2	eDP	I/O
eDP_COMPIO	AC2	Analog	I
eDP_HPD#	AE8	Asynch CMOS	I
eDP_ICOMPO	AB1	Analog	I
eDP_TX#[0]	AG2	eDP	O
eDP_TX#[1]	AF1	eDP	O
eDP_TX#[2]	AE6	eDP	O
eDP_TX#[3]	AG6	eDP	O
eDP_TX[0]	AG4	eDP	O
eDP_TX[1]	AF3	eDP	O
eDP_TX[2]	AF7	eDP	O
eDP_TX[3]	AG8	eDP	O
FDI_INT	AD9	Asynch CMOS	I

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
FDI0_FSYNC	AC8	CMOS	I
FDI0_LSYNC	AB7	CMOS	I
FDI0_TX#[0]	V7	FDI	O
FDI0_TX#[1]	W8	FDI	O
FDI0_TX#[2]	AA8	FDI	O
FDI0_TX#[3]	AC10	FDI	O
FDI0_TX[0]	W6	FDI	O
FDI0_TX[1]	W10	FDI	O
FDI0_TX[2]	Y9	FDI	O
FDI0_TX[3]	AA10	FDI	O
FDI1_FSYNC	AA2	CMOS	I
FDI1_LSYNC	AB3	CMOS	I
FDI1_TX#[0]	U4	FDI	O
FDI1_TX#[1]	W2	FDI	O
FDI1_TX#[2]	V1	FDI	O
FDI1_TX#[3]	Y5	FDI	O
FDI1_TX[0]	U2	FDI	O
FDI1_TX[1]	W4	FDI	O
FDI1_TX[2]	V3	FDI	O
FDI1_TX[3]	AA6	FDI	O
PECI	F53	Asynch	I/O
PEG_ICOMPI	G2	Analog	I
PEG_ICOMPO	H1	Analog	I
PEG_RCOMPO	F3	Analog	I
PEG_RX#[0]	F23	PCIe	I
PEG_RX#[1]	H23	PCIe	I
PEG_RX#[2]	H21	PCIe	I
PEG_RX#[3]	H19	PCIe	I
PEG_RX#[4]	J20	PCIe	I
PEG_RX#[5]	G18	PCIe	I
PEG_RX#[6]	K17	PCIe	I
PEG_RX#[7]	F15	PCIe	I
PEG_RX#[8]	H15	PCIe	I
PEG_RX#[9]	H13	PCIe	I
PEG_RX#[10]	H11	PCIe	I
PEG_RX#[11]	J12	PCIe	I
PEG_RX#[12]	E8	PCIe	I
PEG_RX#[13]	G10	PCIe	I
PEG_RX#[14]	J8	PCIe	I
PEG_RX#[15]	F7	PCIe	I
PEG_RX[0]	G22	PCIe	I
PEG_RX[1]	K23	PCIe	I
PEG_RX[2]	K21	PCIe	I
PEG_RX[3]	F19	PCIe	I
PEG_RX[4]	K19	PCIe	I
PEG_RX[5]	H17	PCIe	I
PEG_RX[6]	K15	PCIe	I
PEG_RX[7]	G14	PCIe	I
PEG_RX[8]	J16	PCIe	I
PEG_RX[9]	K13	PCIe	I
PEG_RX[10]	F11	PCIe	I
PEG_RX[11]	K11	PCIe	I
PEG_RX[12]	F9	PCIe	I
PEG_RX[13]	H9	PCIe	I
PEG_RX[14]	H7	PCIe	I
PEG_RX[15]	G6	PCIe	I
PEG_TX#[0]	A22	PCIe	O
PEG_TX#[1]	B23	PCIe	O
PEG_TX#[2]	C18	PCIe	O
PEG_TX#[3]	D21	PCIe	O
PEG_TX#[4]	B19	PCIe	O
PEG_TX#[5]	E20	PCIe	O
PEG_TX#[6]	A14	PCIe	O
PEG_TX#[7]	D17	PCIe	O
PEG_TX#[8]	B15	PCIe	O
PEG_TX#[9]	E16	PCIe	O
PEG_TX#[10]	D13	PCIe	O
PEG_TX#[11]	A10	PCIe	O
PEG_TX#[12]	B11	PCIe	O
PEG_TX#[13]	D9	PCIe	O
PEG_TX#[14]	B7	PCIe	O
PEG_TX#[15]	E12	PCIe	O
PEG_TX[0]	C22	PCIe	O
PEG_TX[1]	D23	PCIe	O
PEG_TX[2]	A18	PCIe	O
PEG_TX[3]	B21	PCIe	O
PEG_TX[4]	D19	PCIe	O
PEG_TX[5]	F21	PCIe	O
PEG_TX[6]	C14	PCIe	O
PEG_TX[7]	B17	PCIe	O
PEG_TX[8]	D15	PCIe	O
PEG_TX[9]	F17	PCIe	O
PEG_TX[10]	B13	PCIe	O
PEG_TX[11]	C10	PCIe	O
PEG_TX[12]	D11	PCIe	O
PEG_TX[13]	B9	PCIe	O

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
PEG_TX[14]	D7	PCIe	O
PEG_TX[15]	F13	PCIe	O
PM_SYNC	K53	Asynch CMOS	I
PRDY#	J62	Asynch CMOS	O
PREQ#	H65	Asynch CMOS	I
PROC_DETECT#	B59	Analog	O
PROC_SELECT#	AH9	N/A	O
PROCHOT#	H51	Asynch CMOS	I/O
RESET#	K51	Asynch CMOS	I
RSVD	G64		
RSVD	BJ42		
RSVD	BJ34		
RSVD	BJ22		
RSVD	BH43		
RSVD	BH35		
RSVD	BH25		
RSVD	BH23		
RSVD	BH21		
RSVD	BH19		
RSVD	BG62		
RSVD	BG34		
RSVD	BG26		
RSVD	BG22		
RSVD	BG4		
RSVD	BF63		
RSVD	BF43		
RSVD	BF41		
RSVD	BF35		
RSVD	BF25		
RSVD	BF23		
RSVD	BF21		
RSVD	BF19		
RSVD	BF3		
RSVD	BE32		
RSVD	BE16		
RSVD	BE6		
RSVD	BD33		
RSVD	BD29		
RSVD	BD19		
RSVD	BD15		
RSVD	BD13		
RSVD	BC42		
RSVD	BC30		

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
RSVD	BC14		
RSVD	BB57		
RSVD	BB43		
RSVD	BB25		
RSVD	BB17		
RSVD	BB15		
RSVD	BB13		
RSVD	BA48		
RSVD	BA16		
RSVD	AY45		
RSVD	AY41		
RSVD	AY17		
RSVD	AY15		
RSVD	AY13		
RSVD	AW50		
RSVD	AW46		
RSVD	AW42		
RSVD	AW14		
RSVD	AJ10		
RSVD	AJ6		
RSVD	AH5		
RSVD	AD5		
RSVD	AC6		
RSVD	AC4		
RSVD	AA4		
RSVD	P7		
RSVD	N6		
RSVD	M9		
RSVD	M5		
RSVD	L10		
RSVD	L6		
RSVD	L4		
RSVD	L2		
RSVD	K49		
RSVD	K47		
RSVD	K9		
RSVD	K7		
RSVD	K5		
RSVD	J50		
RSVD	J4		
RSVD	J2		
RSVD	H49		
RSVD	H47		

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
RSVD	H5		
RSVD	G52		
RSVD	G48		
RSVD	G4		
RSVD	F5		
RSVD	D49		
RSVD	D25		
RSVD	D3		
RSVD	C52		
RSVD	C24		
RSVD	C4		
RSVD	B53		
RSVD	B25		
SA_BS[0]	BA36	DDR3	O
SA_BS[1]	BC38	DDR3	O
SA_BS[2]	BB19	DDR3	O
SA_CAS#	BE44	DDR3	O
SA_CKE[0]	BC18	DDR3	O
SA_CKE[1]	BD17	DDR3	O
SA_CK#[0]	BA32	DDR3	O
SA_CK#[1]	AY33	DDR3	O
SA_CK[0]	BB31	DDR3	O
SA_CK[1]	AW34	DDR3	O
SA_CS#[0]	BD41	DDR3	O
SA_CS#[1]	BD45	DDR3	O
SA_DQ[0]	AL6	DDR3	I/O
SA_DQ[1]	AL8	DDR3	I/O
SA_DQ[2]	AP7	DDR3	I/O
SA_DQ[3]	AM5	DDR3	I/O
SA_DQ[4]	AK7	DDR3	I/O
SA_DQ[5]	AL10	DDR3	I/O
SA_DQ[6]	AN10	DDR3	I/O
SA_DQ[7]	AM9	DDR3	I/O
SA_DQ[8]	AR10	DDR3	I/O
SA_DQ[9]	AR8	DDR3	I/O
SA_DQ[10]	AV7	DDR3	I/O
SA_DQ[11]	AY5	DDR3	I/O
SA_DQ[12]	AT5	DDR3	I/O
SA_DQ[13]	AR6	DDR3	I/O
SA_DQ[14]	AW6	DDR3	I/O
SA_DQ[15]	AT9	DDR3	I/O
SA_DQ[16]	BA6	DDR3	I/O
SA_DQ[17]	BA8	DDR3	I/O
SA_DQ[18]	BG6	DDR3	I/O
SA_DQ[19]	AY9	DDR3	I/O
SA_DQ[20]	AW8	DDR3	I/O
SA_DQ[21]	BB7	DDR3	I/O
SA_DQ[22]	BC8	DDR3	I/O
SA_DQ[23]	BE4	DDR3	I/O
SA_DQ[24]	AW12	DDR3	I/O
SA_DQ[25]	AV11	DDR3	I/O
SA_DQ[26]	BB11	DDR3	I/O
SA_DQ[27]	BA12	DDR3	I/O
SA_DQ[28]	BE8	DDR3	I/O
SA_DQ[29]	BA10	DDR3	I/O
SA_DQ[30]	BD11	DDR3	I/O
SA_DQ[31]	BE12	DDR3	I/O
SA_DQ[32]	BB49	DDR3	I/O
SA_DQ[33]	AY49	DDR3	I/O
SA_DQ[34]	BE52	DDR3	I/O
SA_DQ[35]	BD51	DDR3	I/O
SA_DQ[36]	BD49	DDR3	I/O
SA_DQ[37]	BE48	DDR3	I/O
SA_DQ[38]	BA52	DDR3	I/O
SA_DQ[39]	AY51	DDR3	I/O
SA_DQ[40]	BC54	DDR3	I/O
SA_DQ[41]	AY53	DDR3	I/O
SA_DQ[42]	AW54	DDR3	I/O
SA_DQ[43]	AY55	DDR3	I/O
SA_DQ[44]	BD53	DDR3	I/O
SA_DQ[45]	BB53	DDR3	I/O
SA_DQ[46]	BE56	DDR3	I/O
SA_DQ[47]	BA56	DDR3	I/O
SA_DQ[48]	BD57	DDR3	I/O
SA_DQ[49]	BF61	DDR3	I/O
SA_DQ[50]	BA60	DDR3	I/O
SA_DQ[51]	BB61	DDR3	I/O
SA_DQ[52]	BE60	DDR3	I/O
SA_DQ[53]	BD63	DDR3	I/O
SA_DQ[54]	BB59	DDR3	I/O
SA_DQ[55]	BC58	DDR3	I/O
SA_DQ[56]	AW58	DDR3	I/O
SA_DQ[57]	AY59	DDR3	I/O
SA_DQ[58]	AL60	DDR3	I/O
SA_DQ[59]	AP61	DDR3	I/O
SA_DQ[60]	AW60	DDR3	I/O

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
SA_DQ[61]	AY57	DDR3	I/O
SA_DQ[62]	AN60	DDR3	I/O
SA_DQ[63]	AR60	DDR3	I/O
SA_DQS#[0]	AN8	DDR3	I/O
SA_DQS#[1]	AU6	DDR3	I/O
SA_DQS#[2]	BC6	DDR3	I/O
SA_DQS#[3]	BD9	DDR3	I/O
SA_DQS#[4]	BC50	DDR3	I/O
SA_DQS#[5]	BB55	DDR3	I/O
SA_DQS#[6]	BD59	DDR3	I/O
SA_DQS#[7]	AU60	DDR3	I/O
SA_DQS[0]	AN6	DDR3	I/O
SA_DQS[1]	AU8	DDR3	I/O
SA_DQS[2]	BD5	DDR3	I/O
SA_DQS[3]	BC10	DDR3	I/O
SA_DQS[4]	BB51	DDR3	I/O
SA_DQS[5]	BD55	DDR3	I/O
SA_DQS[6]	BD61	DDR3	I/O
SA_DQS[7]	AV61	DDR3	I/O
SA_MA[0]	BD27	DDR3	O
SA_MA[1]	BA28	DDR3	O
SA_MA[2]	BB27	DDR3	O
SA_MA[3]	AW26	DDR3	O
SA_MA[4]	BB23	DDR3	O
SA_MA[5]	BA24	DDR3	O
SA_MA[6]	AY21	DDR3	O
SA_MA[7]	BD21	DDR3	O
SA_MA[8]	BC22	DDR3	O
SA_MA[9]	BB21	DDR3	O
SA_MA[10]	AW38	DDR3	O
SA_MA[11]	AW22	DDR3	O
SA_MA[12]	BA20	DDR3	O
SA_MA[13]	BB45	DDR3	O
SA_MA[14]	BE20	DDR3	O
SA_MA[15]	AW18	DDR3	O
SA_ODT[0]	BB41	DDR3	O
SA_ODT[1]	BC46	DDR3	O
SA_RAS#	BE36	DDR3	O
SA_WE#	BA44	DDR3	O
SB_BS[0]	BJ38	DDR3	O
SB_BS[1]	BD37	DDR3	O
SB_BS[2]	AY29	DDR3	O
SB_CAS#	BH39	DDR3	O

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
SB_CKE[0]	BD25	DDR3	O
SB_CKE[1]	BJ26	DDR3	O
SB_CK#[0]	BH33	DDR3	O
SB_CK#[1]	BH37	DDR3	O
SB_CK[0]	BF33	DDR3	O
SB_CK[1]	BF37	DDR3	O
SB_CS#[0]	BE40	DDR3	O
SB_CS#[1]	BH41	DDR3	O
SB_DQ[0]	AL4	DDR3	I/O
SB_DQ[1]	AK3	DDR3	I/O
SB_DQ[2]	AP3	DDR3	I/O
SB_DQ[3]	AR2	DDR3	I/O
SB_DQ[4]	AL2	DDR3	I/O
SB_DQ[5]	AK1	DDR3	I/O
SB_DQ[6]	AP1	DDR3	I/O
SB_DQ[7]	AR4	DDR3	I/O
SB_DQ[8]	AV3	DDR3	I/O
SB_DQ[9]	AU4	DDR3	I/O
SB_DQ[10]	BA4	DDR3	I/O
SB_DQ[11]	BB1	DDR3	I/O
SB_DQ[12]	AV1	DDR3	I/O
SB_DQ[13]	AU2	DDR3	I/O
SB_DQ[14]	BA2	DDR3	I/O
SB_DQ[15]	BB3	DDR3	I/O
SB_DQ[16]	BC2	DDR3	I/O
SB_DQ[17]	BF7	DDR3	I/O
SB_DQ[18]	BF11	DDR3	I/O
SB_DQ[19]	BJ10	DDR3	I/O
SB_DQ[20]	BC4	DDR3	I/O
SB_DQ[21]	BH7	DDR3	I/O
SB_DQ[22]	BH11	DDR3	I/O
SB_DQ[23]	BG10	DDR3	I/O
SB_DQ[24]	BJ14	DDR3	I/O
SB_DQ[25]	BG14	DDR3	I/O
SB_DQ[26]	BF17	DDR3	I/O
SB_DQ[27]	BJ18	DDR3	I/O
SB_DQ[28]	BF13	DDR3	I/O
SB_DQ[29]	BH13	DDR3	I/O
SB_DQ[30]	BH17	DDR3	I/O
SB_DQ[31]	BG18	DDR3	I/O
SB_DQ[32]	BH49	DDR3	I/O
SB_DQ[33]	BF47	DDR3	I/O
SB_DQ[34]	BH53	DDR3	I/O

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
SB_DQ[35]	BG50	DDR3	I/O
SB_DQ[36]	BF49	DDR3	I/O
SB_DQ[37]	BH47	DDR3	I/O
SB_DQ[38]	BF53	DDR3	I/O
SB_DQ[39]	BJ50	DDR3	I/O
SB_DQ[40]	BF55	DDR3	I/O
SB_DQ[41]	BH55	DDR3	I/O
SB_DQ[42]	BJ58	DDR3	I/O
SB_DQ[43]	BH59	DDR3	I/O
SB_DQ[44]	BJ54	DDR3	I/O
SB_DQ[45]	BG54	DDR3	I/O
SB_DQ[46]	BG58	DDR3	I/O
SB_DQ[47]	BF59	DDR3	I/O
SB_DQ[48]	BA64	DDR3	I/O
SB_DQ[49]	BC62	DDR3	I/O
SB_DQ[50]	AU62	DDR3	I/O
SB_DQ[51]	AW64	DDR3	I/O
SB_DQ[52]	BA62	DDR3	I/O
SB_DQ[53]	BC64	DDR3	I/O
SB_DQ[54]	AU64	DDR3	I/O
SB_DQ[55]	AW62	DDR3	I/O
SB_DQ[56]	AR64	DDR3	I/O
SB_DQ[57]	AT65	DDR3	I/O
SB_DQ[58]	AL64	DDR3	I/O
SB_DQ[59]	AM65	DDR3	I/O
SB_DQ[60]	AR62	DDR3	I/O
SB_DQ[61]	AT63	DDR3	I/O
SB_DQ[62]	AL62	DDR3	I/O
SB_DQ[63]	AM63	DDR3	I/O
SB_DQS#[0]	AN4	DDR3	I/O
SB_DQS#[1]	AW2	DDR3	I/O
SB_DQS#[2]	BH9	DDR3	I/O
SB_DQS#[3]	BF15	DDR3	I/O
SB_DQS#[4]	BF51	DDR3	I/O
SB_DQS#[5]	BH57	DDR3	I/O
SB_DQS#[6]	AY63	DDR3	I/O
SB_DQS#[7]	AN62	DDR3	I/O
SB_DQS[0]	AN2	DDR3	I/O
SB_DQS[1]	AW4	DDR3	I/O
SB_DQS[2]	BF9	DDR3	I/O
SB_DQS[3]	BH15	DDR3	I/O
SB_DQS[4]	BH51	DDR3	I/O
SB_DQS[5]	BF57	DDR3	I/O

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
SB_DQS[6]	AY65	DDR3	I/O
SB_DQS[7]	AN64	DDR3	I/O
SB_MA[0]	BF31	DDR3	O
SB_MA[1]	BH31	DDR3	O
SB_MA[2]	BB37	DDR3	O
SB_MA[3]	BC34	DDR3	O
SB_MA[4]	BF27	DDR3	O
SB_MA[5]	BB33	DDR3	O
SB_MA[6]	BH27	DDR3	O
SB_MA[7]	BG30	DDR3	O
SB_MA[8]	BH29	DDR3	O
SB_MA[9]	BF29	DDR3	O
SB_MA[10]	AY37	DDR3	O
SB_MA[11]	BJ30	DDR3	O
SB_MA[12]	AW30	DDR3	O
SB_MA[13]	BA40	DDR3	O
SB_MA[14]	BB29	DDR3	O
SB_MA[15]	BE28	DDR3	O
SB_ODT[0]	BG42	DDR3	O
SB_ODT[1]	BH45	DDR3	O
SB_RAS#	BG38	DDR3	O
SB_WE#	BF39	DDR3	O
SM_DRAMPWROK	AY25	Asynch CMOS	I
SM_DRAMRST#	BE24	DDR3	O
SM_RCOMP[0]	BJ46	Analog	I/O
SM_RCOMP[1]	BG46	Analog	I/O
SM_RCOMP[2]	BF45	Analog	I/O
SM_VREF	BJ44	Analog	I
TCK	J58	CMOS	I
TDI	K61	CMOS	I
TDO	K59	CMOS	O
THERMTRIP#	F51	Asynch CMOS	O
TMS	H59	CMOS	I
TRST#	H63	CMOS	I
UNCOREPWRGOOD	C60	Asynch CMOS	I
VAXG	AH65	PWR	
VAXG	AH63	PWR	
VAXG	AH61	PWR	
VAXG	AH58	PWR	
VAXG	AH56	PWR	
VAXG	AG64	PWR	
VAXG	AG62	PWR	
VAXG	AG60	PWR	

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VAXG	AF58	PWR	
VAXG	AF56	PWR	
VAXG	AE64	PWR	
VAXG	AE62	PWR	
VAXG	AE60	PWR	
VAXG	AD65	PWR	
VAXG	AD63	PWR	
VAXG	AD61	PWR	
VAXG	AD58	PWR	
VAXG	AD56	PWR	
VAXG	AB65	PWR	
VAXG	AB63	PWR	
VAXG	AB61	PWR	
VAXG	AB58	PWR	
VAXG	AB56	PWR	
VAXG	AA64	PWR	
VAXG	AA62	PWR	
VAXG	AA60	PWR	
VAXG	Y58	PWR	
VAXG	Y56	PWR	
VAXG	W64	PWR	
VAXG	W62	PWR	
VAXG	W60	PWR	
VAXG	V65	PWR	
VAXG	V63	PWR	
VAXG	V61	PWR	
VAXG	V58	PWR	
VAXG	V56	PWR	
VAXG	T65	PWR	
VAXG	T63	PWR	
VAXG	T61	PWR	
VAXG	T58	PWR	
VAXG	T56	PWR	
VAXG	R64	PWR	
VAXG	R62	PWR	
VAXG	R60	PWR	
VAXG	R55	PWR	
VAXG	R53	PWR	
VAXG	R48	PWR	
VAXG	N64	PWR	
VAXG	N62	PWR	
VAXG	N60	PWR	
VAXG	N58	PWR	

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VAXG	N56	PWR	
VAXG	N52	PWR	
VAXG	N49	PWR	
VAXG	M65	PWR	
VAXG	M63	PWR	
VAXG	M61	PWR	
VAXG	M59	PWR	
VAXG	M55	PWR	
VAXG	M53	PWR	
VAXG	M48	PWR	
VAXG	L56	PWR	
VAXG	L52	PWR	
VAXG	L48	PWR	
VAXG_SENSE	F49	Analog	O
VAXG_VAL_SENSE	B49	Analog	O
VCC	R46	PWR	
VCC	R42	PWR	
VCC	R40	PWR	
VCC	R36	PWR	
VCC	R34	PWR	
VCC	R29	PWR	
VCC	R27	PWR	
VCC	R23	PWR	
VCC	R21	PWR	
VCC	N45	PWR	
VCC	N43	PWR	
VCC	N39	PWR	
VCC	N37	PWR	
VCC	N33	PWR	
VCC	N30	PWR	
VCC	N26	PWR	
VCC	N24	PWR	
VCC	N20	PWR	
VCC	M46	PWR	
VCC	M42	PWR	
VCC	M40	PWR	
VCC	M36	PWR	
VCC	M34	PWR	
VCC	M29	PWR	
VCC	M27	PWR	
VCC	M23	PWR	
VCC	M21	PWR	
VCC	L44	PWR	

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VCC	L40	PWR	
VCC	L38	PWR	
VCC	L34	PWR	
VCC	L32	PWR	
VCC	L28	PWR	
VCC	L26	PWR	
VCC	L22	PWR	
VCC	K45	PWR	
VCC	K43	PWR	
VCC	K41	PWR	
VCC	K37	PWR	
VCC	K35	PWR	
VCC	K31	PWR	
VCC	K29	PWR	
VCC	K25	PWR	
VCC	J44	PWR	
VCC	J40	PWR	
VCC	J38	PWR	
VCC	J34	PWR	
VCC	J32	PWR	
VCC	J28	PWR	
VCC	J26	PWR	
VCC	H45	PWR	
VCC	H43	PWR	
VCC	H41	PWR	
VCC	H37	PWR	
VCC	H35	PWR	
VCC	H31	PWR	
VCC	H29	PWR	
VCC	H25	PWR	
VCC	G44	PWR	
VCC	G40	PWR	
VCC	G38	PWR	
VCC	G34	PWR	
VCC	G32	PWR	
VCC	G28	PWR	
VCC	G26	PWR	
VCC	F45	PWR	
VCC	F43	PWR	
VCC	F41	PWR	
VCC	F37	PWR	
VCC	F35	PWR	
VCC	F31	PWR	
VCC	F29	PWR	
VCC	F25	PWR	
VCC	E44	PWR	
VCC	E40	PWR	
VCC	E38	PWR	
VCC	E34	PWR	
VCC	E32	PWR	
VCC	E28	PWR	
VCC	E26	PWR	
VCC	D45	PWR	
VCC	D43	PWR	
VCC	D41	PWR	
VCC	D37	PWR	
VCC	D35	PWR	
VCC	D31	PWR	
VCC	D29	PWR	
VCC	C44	PWR	
VCC	C40	PWR	
VCC	C38	PWR	
VCC	C34	PWR	
VCC	C32	PWR	
VCC	C28	PWR	
VCC	C26	PWR	
VCC	B45	PWR	
VCC	B43	PWR	
VCC	B41	PWR	
VCC	B37	PWR	
VCC	B35	PWR	
VCC	B31	PWR	
VCC	B29	PWR	
VCC	A44	PWR	
VCC	A40	PWR	
VCC	A38	PWR	
VCC	A34	PWR	
VCC	A32	PWR	
VCC	A28	PWR	
VCC	A26	PWR	
VCC_DIE_SENSE	F47	Analog	O
VCC_SENSE	B47	Analog	O
VCC_VAL_SENSE	D47	Analog	O
VCCDQ	AV23	PWR	
VCCDQ	AT23	PWR	
VCCDQ	AP23	PWR	

Table 8-2. BGA1224 Processor Ball List by Ball Name

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VCCDQ	AL23	PWR	
VCCIO	AV55	PWR	
VCCIO	AV53	PWR	
VCCIO	AV48	PWR	
VCCIO	AV17	PWR	
VCCIO	AV15	PWR	
VCCIO	AV12	PWR	
VCCIO	AU58	PWR	
VCCIO	AU56	PWR	
VCCIO	AU52	PWR	
VCCIO	AU49	PWR	
VCCIO	AU20	PWR	
VCCIO	AU18	PWR	
VCCIO	AT55	PWR	
VCCIO	AT53	PWR	
VCCIO	AT48	PWR	
VCCIO	AT17	PWR	
VCCIO	AT15	PWR	
VCCIO	AT12	PWR	
VCCIO	AR58	PWR	
VCCIO	AR56	PWR	
VCCIO	AR52	PWR	
VCCIO	AR49	PWR	
VCCIO	AR20	PWR	
VCCIO	AR18	PWR	
VCCIO	AR16	PWR	
VCCIO	AR14	PWR	
VCCIO	AP55	PWR	
VCCIO	AP53	PWR	
VCCIO	AP48	PWR	
VCCIO	AN58	PWR	
VCCIO	AN56	PWR	
VCCIO	AN52	PWR	
VCCIO	AN49	PWR	
VCCIO	AN20	PWR	
VCCIO	AN18	PWR	
VCCIO	AN16	PWR	
VCCIO	AN14	PWR	
VCCIO	AM11	PWR	
VCCIO	AL55	PWR	
VCCIO	AL53	PWR	
VCCIO	AL48	PWR	
VCCIO	AL17	PWR	
VCCIO	AL15	PWR	
VCCIO	AL12	PWR	
VCCIO	AK58	PWR	
VCCIO	AK56	PWR	
VCCIO	AJ17	PWR	
VCCIO	AJ15	PWR	
VCCIO	AJ12	PWR	
VCCIO	AH16	PWR	
VCCIO	AH14	PWR	
VCCIO	AH11	PWR	
VCCIO	AF16	PWR	
VCCIO	AF14	PWR	
VCCIO	AE17	PWR	
VCCIO	AE15	PWR	
VCCIO	AE12	PWR	
VCCIO	AD11	PWR	
VCCIO	AC17	PWR	
VCCIO	AC15	PWR	
VCCIO	AC12	PWR	
VCCIO	AB16	PWR	
VCCIO	AB14	PWR	
VCCIO	Y16	PWR	
VCCIO	Y14	PWR	
VCCIO	Y11	PWR	
VCCIO_SEL	AJ8	N/A	O
VCCIO_SENSE	AW10	Analog	O
VCCPLL	AK65	PWR	
VCCPLL	AK63	PWR	
VCCPLL	AK61	PWR	
VCCPQE	AV21	PWR	
VCCPQE	AT21	PWR	
VCCPQE	AP21	PWR	
VCCPQE	AL21	PWR	
VCCSA	W17	PWR	
VCCSA	W15	PWR	
VCCSA	W12	PWR	
VCCSA	U17	PWR	
VCCSA	U15	PWR	
VCCSA	U12	PWR	
VCCSA	T16	PWR	
VCCSA	T14	PWR	
VCCSA	T11	PWR	
VCCSA	N18	PWR	

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VCCSA	N16	PWR	
VCCSA	N14	PWR	
VCCSA	M17	PWR	
VCCSA	M15	PWR	
VCCSA	M12	PWR	
VCCSA	M11	PWR	
VCCSA	L18	PWR	
VCCSA	L14	PWR	
VCCSA_SENSE	K3	Analog	O
VCCSA_VID[0]	AE10	CMOS	O
VCCSA_VID[1]	AG10	CMOS	O
VDDQ	BJ36	PWR	
VDDQ	BJ28	PWR	
VDDQ	BG40	PWR	
VDDQ	BG32	PWR	
VDDQ	BD47	PWR	
VDDQ	BD43	PWR	
VDDQ	BD39	PWR	
VDDQ	BD31	PWR	
VDDQ	BD23	PWR	
VDDQ	BB35	PWR	
VDDQ	AY47	PWR	
VDDQ	AY43	PWR	
VDDQ	AY39	PWR	
VDDQ	AY35	PWR	
VDDQ	AY31	PWR	
VDDQ	AY27	PWR	
VDDQ	AY23	PWR	
VDDQ	AV46	PWR	
VDDQ	AV42	PWR	
VDDQ	AV40	PWR	
VDDQ	AV36	PWR	
VDDQ	AV34	PWR	
VDDQ	AV29	PWR	
VDDQ	AV27	PWR	
VDDQ	AU45	PWR	
VDDQ	AU43	PWR	
VDDQ	AU39	PWR	
VDDQ	AU37	PWR	
VDDQ	AU33	PWR	
VDDQ	AU30	PWR	
VDDQ	AU26	PWR	
VDDQ	AU24	PWR	
VDDQ	AT46	PWR	
VDDQ	AT42	PWR	
VDDQ	AT40	PWR	
VDDQ	AT36	PWR	
VDDQ	AT34	PWR	
VDDQ	AT29	PWR	
VDDQ	AT27	PWR	
VDDQ	AR45	PWR	
VDDQ	AR43	PWR	
VDDQ	AR39	PWR	
VDDQ	AR37	PWR	
VDDQ	AR33	PWR	
VDDQ	AR30	PWR	
VDDQ	AR26	PWR	
VDDQ	AR24	PWR	
VDDQ	AP46	PWR	
VDDQ	AP42	PWR	
VDDQ	AP40	PWR	
VDDQ	AP36	PWR	
VDDQ	AP34	PWR	
VDDQ	AP29	PWR	
VDDQ	AP27	PWR	
VDDQ	AN45	PWR	
VDDQ	AN43	PWR	
VDDQ	AN39	PWR	
VDDQ	AN37	PWR	
VDDQ	AN33	PWR	
VDDQ	AN30	PWR	
VDDQ	AN26	PWR	
VDDQ	AN24	PWR	
VDDQ	AL46	PWR	
VDDQ	AL42	PWR	
VDDQ	AL40	PWR	
VDDQ	AL36	PWR	
VDDQ	AL34	PWR	
VDDQ	AL29	PWR	
VDDQ	AL27	PWR	
VDDQ_SENSE	AY19	Analog	O
VIDALERT#	B51	CMOS	I
VIDSCLK	D51	CMOS	O
VIDSOUT	A50	CMOS	I/O
VSS	BJ56	GND	
VSS	BJ52	GND	

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VSS	BJ48	GND	
VSS	BJ40	GND	
VSS	BJ32	GND	
VSS	BJ24	GND	
VSS	BJ20	GND	
VSS	BJ16	GND	
VSS	BJ12	GND	
VSS	BJ8	GND	
VSS	BG60	GND	
VSS	BG56	GND	
VSS	BG52	GND	
VSS	BG48	GND	
VSS	BG44	GND	
VSS	BG36	GND	
VSS	BG28	GND	
VSS	BG24	GND	
VSS	BG20	GND	
VSS	BG16	GND	
VSS	BG12	GND	
VSS	BG8	GND	
VSS	BF5	GND	
VSS	BE62	GND	
VSS	BE58	GND	
VSS	BE54	GND	
VSS	BE50	GND	
VSS	BE46	GND	
VSS	BE42	GND	
VSS	BE38	GND	
VSS	BE34	GND	
VSS	BE30	GND	
VSS	BE26	GND	
VSS	BE22	GND	
VSS	BE18	GND	
VSS	BE14	GND	
VSS	BE10	GND	
VSS	BD35	GND	
VSS	BD7	GND	
VSS	BD3	GND	
VSS	BC60	GND	
VSS	BC56	GND	
VSS	BC52	GND	
VSS	BC48	GND	
VSS	BC44	GND	

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VSS	BC40	GND	
VSS	BC36	GND	
VSS	BC32	GND	
VSS	BC28	GND	
VSS	BC26	GND	
VSS	BC24	GND	
VSS	BC20	GND	
VSS	BC16	GND	
VSS	BC12	GND	
VSS	BB65	GND	
VSS	BB63	GND	
VSS	BB47	GND	
VSS	BB39	GND	
VSS	BB9	GND	
VSS	BB5	GND	
VSS	BA58	GND	
VSS	BA54	GND	
VSS	BA50	GND	
VSS	BA46	GND	
VSS	BA42	GND	
VSS	BA38	GND	
VSS	BA34	GND	
VSS	BA30	GND	
VSS	BA26	GND	
VSS	BA22	GND	
VSS	BA18	GND	
VSS	BA14	GND	
VSS	AY61	GND	
VSS	AY11	GND	
VSS	AY7	GND	
VSS	AY3	GND	
VSS	AY1	GND	
VSS	AW56	GND	
VSS	AW52	GND	
VSS	AW48	GND	
VSS	AW44	GND	
VSS	AW40	GND	
VSS	AW36	GND	
VSS	AW32	GND	
VSS	AW28	GND	
VSS	AW24	GND	
VSS	AW16	GND	
VSS	AV65	GND	

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VSS	AV63	GND	
VSS	AV59	GND	
VSS	AV57	GND	
VSS	AV50	GND	
VSS	AV44	GND	
VSS	AV38	GND	
VSS	AV31	GND	
VSS	AV25	GND	
VSS	AV19	GND	
VSS	AV9	GND	
VSS	AV5	GND	
VSS	AU54	GND	
VSS	AU47	GND	
VSS	AU41	GND	
VSS	AU35	GND	
VSS	AU28	GND	
VSS	AU22	GND	
VSS	AU16	GND	
VSS	AU14	GND	
VSS	AT61	GND	
VSS	AT57	GND	
VSS	AT50	GND	
VSS	AT44	GND	
VSS	AT38	GND	
VSS	AT31	GND	
VSS	AT25	GND	
VSS	AT19	GND	
VSS	AT11	GND	
VSS	AT7	GND	
VSS	AT3	GND	
VSS	AT1	GND	
VSS	AR54	GND	
VSS	AR47	GND	
VSS	AR41	GND	
VSS	AR35	GND	
VSS	AR28	GND	
VSS	AR22	GND	
VSS	AP65	GND	
VSS	AP63	GND	
VSS	AP57	GND	
VSS	AP50	GND	
VSS	AP44	GND	
VSS	AP38	GND	

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VSS	AP31	GND	
VSS	AP25	GND	
VSS	AP19	GND	
VSS	AP17	GND	
VSS	AP15	GND	
VSS	AP12	GND	
VSS	AP11	GND	
VSS	AP9	GND	
VSS	AP5	GND	
VSS	AN54	GND	
VSS	AN47	GND	
VSS	AN41	GND	
VSS	AN35	GND	
VSS	AN28	GND	
VSS	AN22	GND	
VSS	AM61	GND	
VSS	AM7	GND	
VSS	AM3	GND	
VSS	AM1	GND	
VSS	AL57	GND	
VSS	AL50	GND	
VSS	AL44	GND	
VSS	AL38	GND	
VSS	AL31	GND	
VSS	AL25	GND	
VSS	AL19	GND	
VSS	AK16	GND	
VSS	AK14	GND	
VSS	AK11	GND	
VSS	AK9	GND	
VSS	AK5	GND	
VSS	AJ64	GND	
VSS	AJ62	GND	
VSS	AJ60	GND	
VSS	AJ57	GND	
VSS	AH7	GND	
VSS	AH3	GND	
VSS	AH1	GND	
VSS	AG57	GND	
VSS	AG17	GND	
VSS	AG15	GND	
VSS	AG12	GND	
VSS	AF65	GND	

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VSS	AF63	GND	
VSS	AF61	GND	
VSS	AF11	GND	
VSS	AF9	GND	
VSS	AF5	GND	
VSS	AE57	GND	
VSS	AD16	GND	
VSS	AD14	GND	
VSS	AD7	GND	
VSS	AD3	GND	
VSS	AD1	GND	
VSS	AC64	GND	
VSS	AC62	GND	
VSS	AC60	GND	
VSS	AC57	GND	
VSS	AB11	GND	
VSS	AB9	GND	
VSS	AB5	GND	
VSS	AA57	GND	
VSS	AA17	GND	
VSS	AA15	GND	
VSS	AA12	GND	
VSS	Y65	GND	
VSS	Y63	GND	
VSS	Y61	GND	
VSS	Y7	GND	
VSS	Y3	GND	
VSS	Y1	GND	
VSS	W57	GND	
VSS	V16	GND	
VSS	V14	GND	
VSS	V11	GND	
VSS	V9	GND	
VSS	V5	GND	
VSS	U64	GND	
VSS	U62	GND	
VSS	U60	GND	
VSS	U57	GND	
VSS	T7	GND	
VSS	T3	GND	
VSS	T1	GND	
VSS	R57	GND	
VSS	R50	GND	

Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VSS	R44	GND	
VSS	R38	GND	
VSS	R31	GND	
VSS	R25	GND	
VSS	R19	GND	
VSS	R17	GND	
VSS	R15	GND	
VSS	R12	GND	
VSS	P65	GND	
VSS	P63	GND	
VSS	P61	GND	
VSS	P11	GND	
VSS	P9	GND	
VSS	P5	GND	
VSS	N54	GND	
VSS	N47	GND	
VSS	N41	GND	
VSS	N35	GND	
VSS	N28	GND	
VSS	N22	GND	
VSS	M57	GND	
VSS	M50	GND	
VSS	M44	GND	
VSS	M38	GND	
VSS	M31	GND	
VSS	M25	GND	
VSS	M19	GND	
VSS	M7	GND	
VSS	M3	GND	
VSS	M1	GND	
VSS	L64	GND	
VSS	L62	GND	
VSS	L60	GND	
VSS	L58	GND	
VSS	L54	GND	
VSS	L50	GND	
VSS	L46	GND	
VSS	L42	GND	
VSS	L36	GND	
VSS	L30	GND	
VSS	L24	GND	
VSS	L20	GND	
VSS	L16	GND	

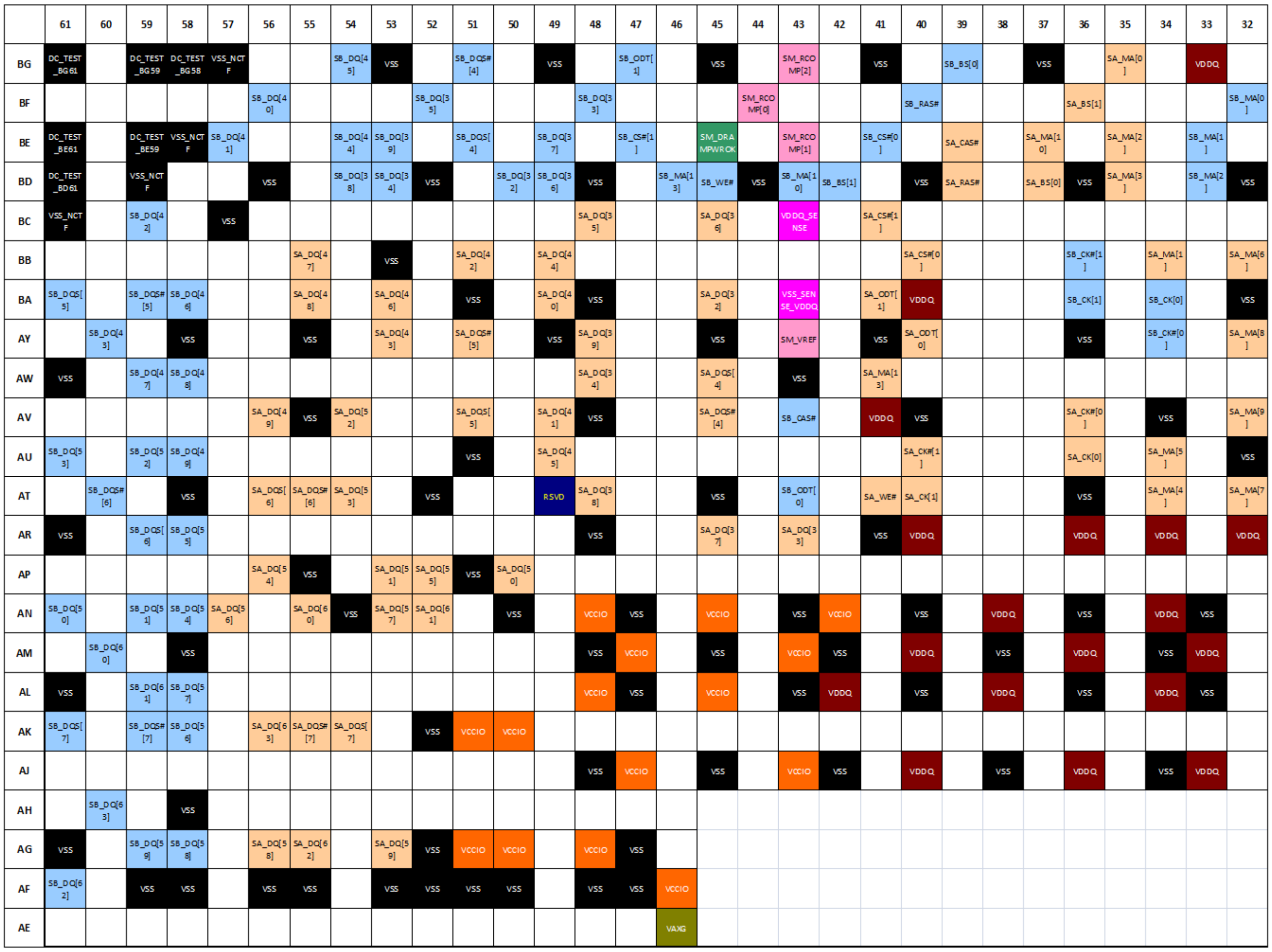
Table 8-2. BGA1224 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VSS	L12	GND	
VSS	L8	GND	
VSS	K39	GND	
VSS	K33	GND	
VSS	K27	GND	
VSS	K1	GND	
VSS	J64	GND	
VSS	J60	GND	
VSS	J56	GND	
VSS	J52	GND	
VSS	J48	GND	
VSS	J46	GND	
VSS	J42	GND	
VSS	J36	GND	
VSS	J30	GND	
VSS	J24	GND	
VSS	J22	GND	
VSS	J18	GND	
VSS	J14	GND	
VSS	J10	GND	
VSS	J6	GND	
VSS	H39	GND	
VSS	H33	GND	
VSS	H27	GND	
VSS	H3	GND	
VSS	G62	GND	
VSS	G58	GND	
VSS	G54	GND	
VSS	G50	GND	
VSS	G46	GND	
VSS	G42	GND	
VSS	G36	GND	
VSS	G30	GND	
VSS	G24	GND	
VSS	G20	GND	
VSS	G16	GND	
VSS	G12	GND	
VSS	G8	GND	
VSS	F39	GND	
VSS	F33	GND	
VSS	F27	GND	
VSS	E60	GND	
VSS	E56	GND	
VSS	E52	GND	
VSS	E48	GND	
VSS	E46	GND	
VSS	E42	GND	
VSS	E36	GND	
VSS	E30	GND	
VSS	E24	GND	
VSS	E22	GND	
VSS	E18	GND	
VSS	E14	GND	
VSS	E10	GND	
VSS	E6	GND	
VSS	E4	GND	
VSS	D63	GND	
VSS	D39	GND	
VSS	D33	GND	
VSS	D27	GND	
VSS	C58	GND	
VSS	C54	GND	
VSS	C50	GND	
VSS	C46	GND	
VSS	C42	GND	
VSS	C36	GND	
VSS	C30	GND	
VSS	C20	GND	
VSS	C16	GND	
VSS	C12	GND	
VSS	C8	GND	
VSS	B39	GND	
VSS	B33	GND	
VSS	B27	GND	
VSS	A56	GND	
VSS	A52	GND	
VSS	A42	GND	
VSS	A36	GND	
VSS	A30	GND	
VSS	A24	GND	
VSS	A20	GND	
VSS	A16	GND	
VSS	A12	GND	
VSS	A8	GND	
VSS_NCTF	BJ60		
VSS_NCTF	BJ6		

Table 8-2. BGA1224 Processor Ball List by Ball Name

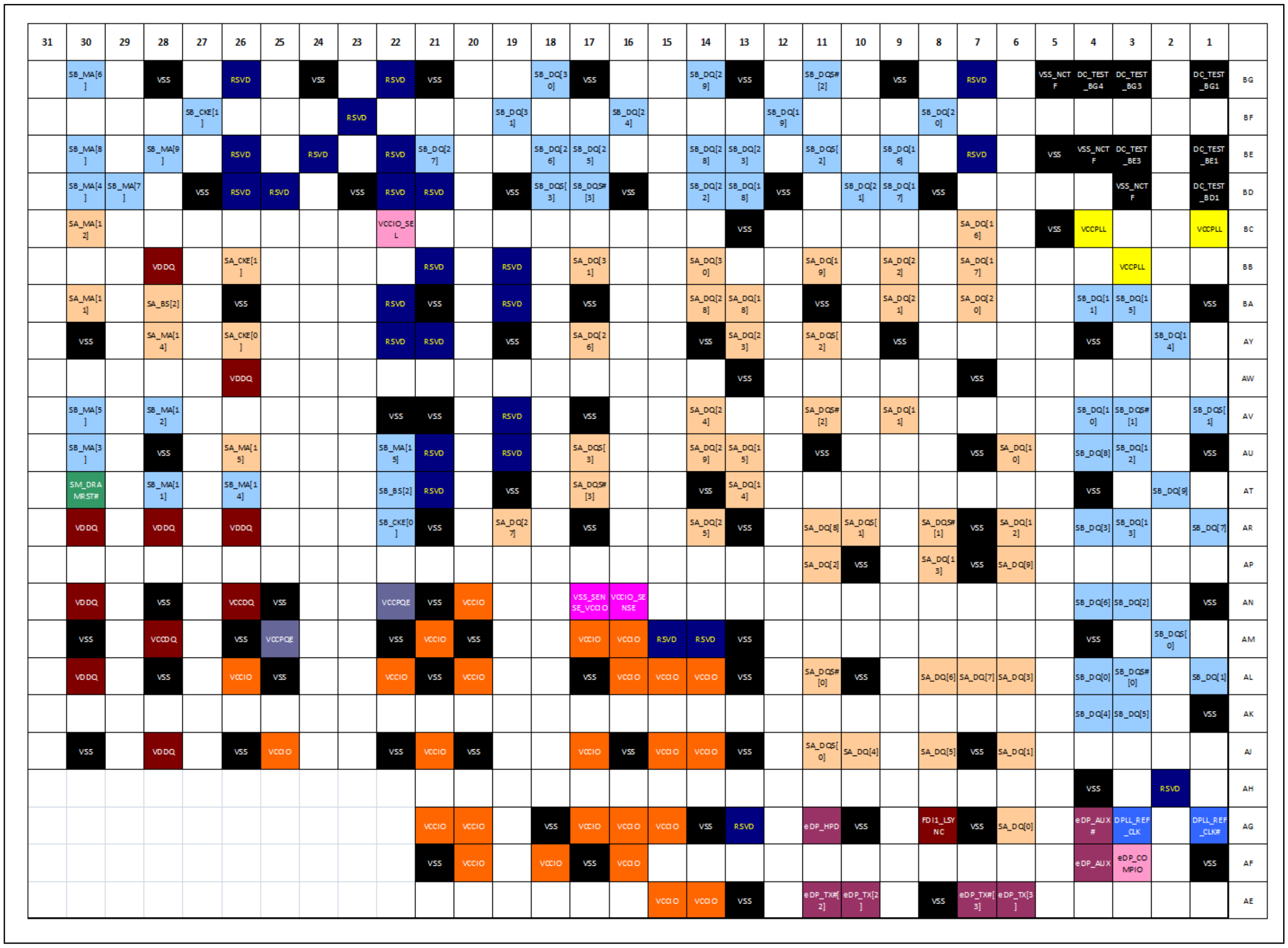
Ball Name	Ball #	Buffer Type	Dir
VSS_NCTF	BH61		
VSS_NCTF	BH5		
VSS_NCTF	BE64		
VSS_NCTF	BE2		
VSS_NCTF	BD65		
VSS_NCTF	BD1		
VSS_NCTF	F65		
VSS_NCTF	F1		
VSS_NCTF	E64		
VSS_NCTF	E2		
VSS_NCTF	B61		
VSS_NCTF	B5		
VSS_NCTF	A60		
VSS_NCTF	A6		
VSS_SENSE	A46	Analog	O
VSS_SENSE_VDDQ	AW20	Analog	O
VSS_VAL_SENSE	C48	Analog	O
VSSAXG_SENSE	E50	Analog	O
VSSAXG_VAL_SENSE	A48	Analog	O
VSS_SENSE_VCCIO	AU10	Analog	O

Figure 8-9. BGA1023 Ballmap (Top View, Upper-Left Quadrant)



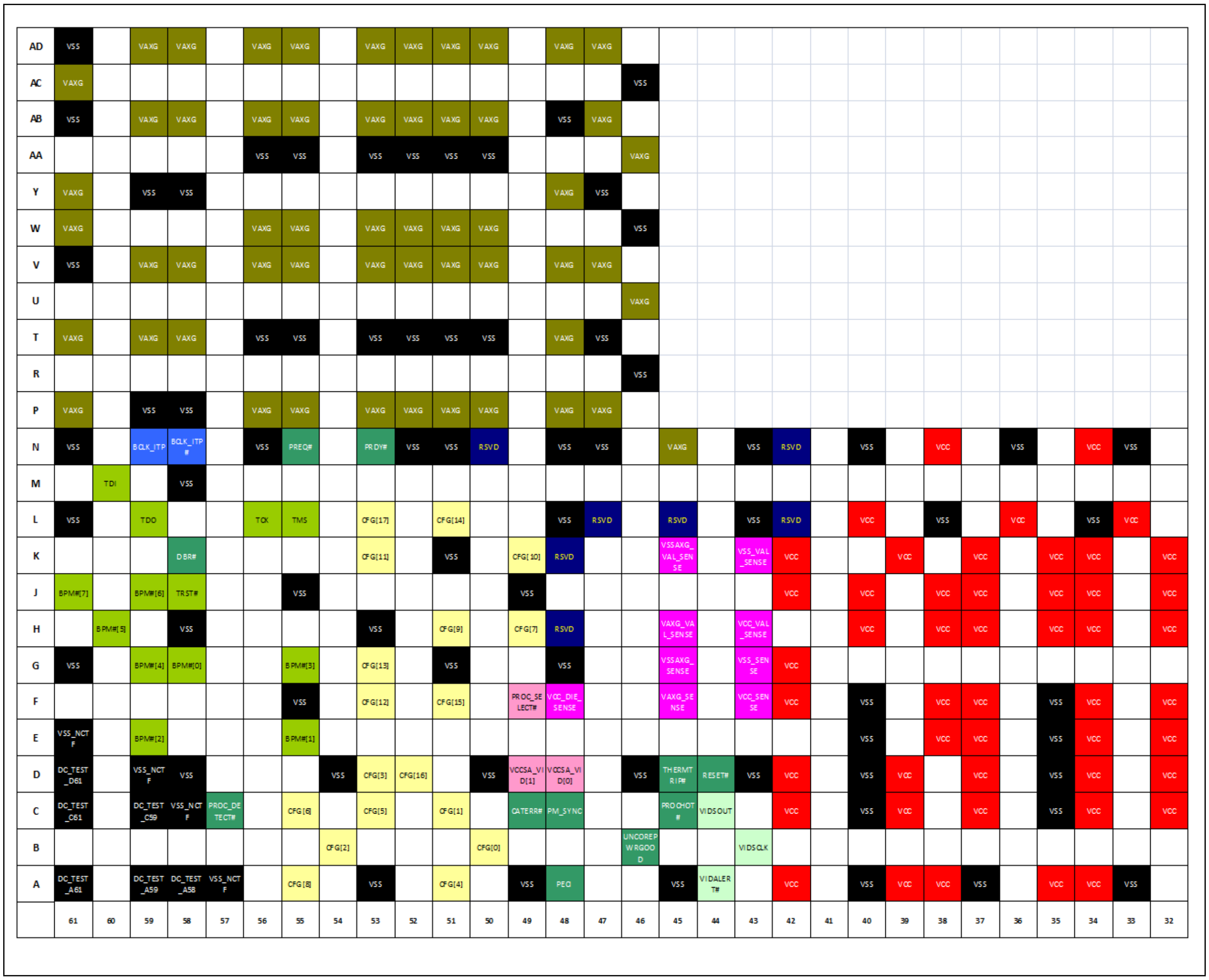
	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
BG	DC_TEST_BG61		DC_TEST_BG59	DC_TEST_BG58	VSS_NCTF			SB_DQ[45]	VSS		SB_DQS#[4]		VSS		SB_ODT[1]		VSS		SM_RCOMP[2]		VSS		SB_BS[0]		VSS		SA_MA[0]		VDDQ	
BF						SB_DQ[40]				SB_DQ[35]				SB_DQ[33]				SM_RCOMP[0]				SB_RAS#				SA_BS[1]				SB_MA[0]
BE	DC_TEST_BE61		DC_TEST_BE59	VSS_NCTF	SB_DQ[41]			SB_DQ[44]	SB_DQ[39]		SB_DQS[4]		SB_DQ[37]		SB_CS#[1]		SM_DRAMPWROK		SM_RCOMP[1]		SB_CS#[0]		SA_CAS#		SA_MA[10]		SA_MA[2]		SB_MA[1]	
BD	DC_TEST_BD61		VSS_NCTF			VSS		SB_DQ[38]	SB_DQ[34]	VSS		SB_DQ[32]	SB_DQ[36]	VSS		SB_MA[13]	SB_WE#	VSS	SB_MA[10]	SB_BS[1]		VSS	SA_RAS#		SA_BS[0]	VSS	SA_MA[3]		SB_MA[2]	VSS
BC	VSS_NCTF		SB_DQ[42]		VSS									SA_DQ[35]			SA_DQ[36]		VDDQ_SENSE		SA_CS#[1]									
BB							SA_DQ[47]		VSS		SA_DQ[42]		SA_DQ[44]									SA_CS#[0]				SB_CK#[1]		SA_MA[1]		SA_MA[6]
BA	SB_DQS[5]		SB_DQS#[5]	SB_DQ[46]			SA_DQ[48]		SA_DQ[46]		VSS		SA_DQ[40]	VSS			SA_DQ[32]		VSS_SENSE_VDDQ		SA_ODT[1]	VDDQ				SB_CK[1]		SB_CK[0]		VSS
AY		SB_DQ[43]		VSS			VSS		SA_DQ[43]		SA_DQS#[5]		VSS	SA_DQ[39]			VSS		SM_VREF		VSS	SA_ODT[0]				VSS		SB_CK#[0]		SA_MA[8]
AW	VSS		SB_DQ[47]	SB_DQ[48]										SA_DQ[34]			SA_DQS[4]		VSS		SA_MA[13]									
AV						SA_DQ[49]	VSS	SA_DQ[52]			SA_DQS[5]		SA_DQ[41]	VSS			SA_DQS#[4]		SB_CAS#		VDDQ	VSS				SA_CK#[0]		VSS		SA_MA[9]
AU	SB_DQ[53]		SB_DQ[52]	SB_DQ[49]							VSS		SA_DQ[45]									SA_CK#[1]				SA_CK[0]		SA_MA[5]		VSS
AT		SB_DQS#[6]		VSS		SA_DQS[6]	SA_DQS#[6]	SA_DQ[53]		VSS			RSVD	SA_DQ[38]			VSS		SB_ODT[0]		SA_WE#	SA_CK[1]				VSS		SA_MA[4]		SA_MA[7]
AR	VSS		SB_DQS[6]	SB_DQ[55]										VSS			SA_DQ[37]		SA_DQ[33]		VSS	VDDQ				VDDQ		VDDQ		VDDQ
AP						SA_DQ[54]	VSS		SA_DQ[51]	SA_DQ[55]	VSS	SA_DQ[50]																		
AN	SB_DQ[50]		SB_DQ[51]	SB_DQ[54]	SA_DQ[56]		SA_DQ[60]	VSS	SA_DQ[57]	SA_DQ[61]		VSS		VCCIO	VSS		VCCIO		VSS	VCCIO		VSS		VDDQ		VSS		VDDQ	VSS	
AM		SB_DQ[60]		VSS										VSS	VCCIO		VSS		VCCIO	VSS		VDDQ		VSS		VDDQ		VSS	VDDQ	
AL	VSS		SB_DQ[61]	SB_DQ[57]										VCCIO	VSS		VCCIO		VSS	VDDQ		VSS		VDDQ		VSS		VDDQ	VSS	
AK	SB_DQS[7]		SB_DQS#[7]	SB_DQ[56]		SA_DQ[63]	SA_DQS#[7]	SA_DQS[7]		VSS	VCCIO	VCCIO																		
AJ														VSS	VCCIO		VSS		VCCIO	VSS		VDDQ		VSS		VDDQ		VSS	VDDQ	
AH		SB_DQ[63]		VSS																										
AG	VSS		SB_DQ[59]	SB_DQ[58]		SA_DQ[58]	SA_DQ[62]		SA_DQ[59]	VSS	VCCIO	VCCIO		VCCIO	VSS															
AF	SB_DQ[62]		VSS	VSS		VSS	VSS		VSS	VSS	VSS	VSS		VSS	VSS	VCCIO														
AE																VAXG														

Figure 8-10. BGA1023 Ballmap (Top View, Upper-Right Quadrant)



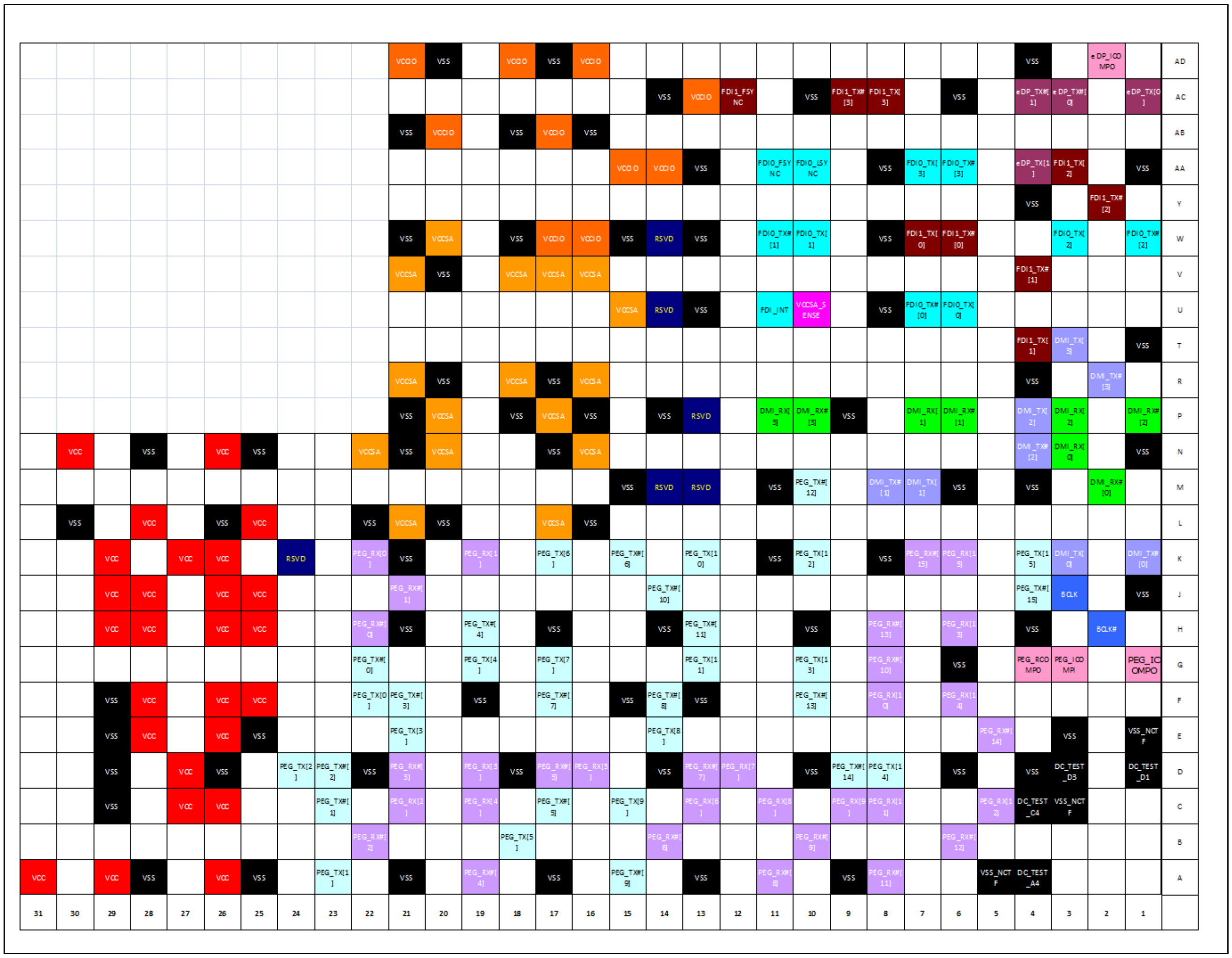
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
	SB_MA[6]		VSS		RSVD		VSS		RSVD	VSS			SB_DQ[30]	VSS			SB_DQ[29]	VSS		SB_DQS#[2]		VSS		RSVD		VSS_NCTF	DC_TEST_BG4	DC_TEST_BG3		DC_TEST_BG1	BG
				SB_CKE[1]				RSVD				SB_DQ[31]			SB_DQ[24]				SB_DQ[19]				SB_DQ[20]								BF
	SB_MA[8]		SB_MA[9]		RSVD		RSVD		RSVD	SB_DQ[27]			SB_DQ[26]	SB_DQ[25]			SB_DQ[28]	SB_DQ[23]		SB_DQS[2]		SB_DQ[16]		RSVD		VSS	VSS_NCTF	DC_TEST_BE3		DC_TEST_BE1	BE
	SB_MA[4]	SB_MA[7]		VSS	RSVD	RSVD		VSS	RSVD	RSVD		VSS	SB_DQS[3]	SB_DQS#[3]	VSS		SB_DQ[22]	SB_DQ[18]	VSS		SB_DQ[21]	SB_DQ[17]	VSS					VSS_NCTF		DC_TEST_BD1	BD
	SA_MA[12]								VCCIO_SEL									VSS						SA_DQ[16]		VSS	VCCPLL			VCCPLL	BC
			VDDQ		SA_CKE[1]					RSVD		RSVD		SA_DQ[31]			SA_DQ[30]			SA_DQ[19]		SA_DQ[22]		SA_DQ[17]				VCCPLL			BB
	SA_MA[11]		SA_BS[2]		VSS				RSVD	VSS		RSVD		VSS			SA_DQ[28]	SA_DQ[18]		VSS		SA_DQ[21]		SA_DQ[20]			SB_DQ[11]	SB_DQ[15]		VSS	BA
	VSS		SA_MA[14]		SA_CKE[0]				RSVD	RSVD		VSS		SA_DQ[26]			VSS	SA_DQ[23]		SA_DQS[2]		VSS					VSS		SB_DQ[14]		AY
					VDDQ													VSS						VSS							AW
	SB_MA[5]		SB_MA[12]						VSS	VSS		RSVD		VSS			SA_DQ[24]			SA_DQS#[2]		SA_DQ[11]					SB_DQ[10]	SB_DQS#[1]		SB_DQS[1]	AV
	SB_MA[3]		VSS		SA_MA[15]				SB_MA[15]	RSVD		RSVD		SA_DQS[3]			SA_DQ[29]	SA_DQ[15]		VSS				VSS	SA_DQ[10]		SB_DQ[8]	SB_DQ[12]		VSS	AU
	SM_DRAMRST#		SB_MA[11]		SB_MA[14]				SB_BS[2]	RSVD		VSS		SA_DQS#[3]			VSS	SA_DQ[14]									VSS		SB_DQ[9]		AT
	VDDQ		VDDQ		VDDQ				SB_CKE[0]	VSS		SA_DQ[27]		VSS			SA_DQ[25]	VSS		SA_DQ[8]	SA_DQS[1]		SA_DQS#[1]	VSS	SA_DQ[12]		SB_DQ[3]	SB_DQ[13]		SB_DQ[7]	AR
																				SA_DQ[2]	VSS		SA_DQ[13]	VSS	SA_DQ[9]						AP
	VDDQ		VSS		VCCDQ	VSS			VCCPQE	VSS	VCCIO			VSS_SENSE_VCCIO	VCCIO_SENSE												SB_DQ[6]	SB_DQ[2]		VSS	AN
	VSS		VCCDQ		VSS	VCCPQE			VSS	VCCIO	VSS			VCCIO	VCCIO	RSVD	RSVD	VSS									VSS		SB_DQS[0]		AM
	VDDQ		VSS		VCCIO	VSS			VCCIO	VSS	VCCIO			VSS	VCCIO	VCCIO	VCCIO	VSS		SA_DQS#[0]	VSS		SA_DQ[6]	SA_DQ[7]	SA_DQ[3]		SB_DQ[0]	SB_DQS#[0]		SB_DQ[1]	AL
																											SB_DQ[4]	SB_DQ[5]		VSS	AK
	VSS		VDDQ		VSS	VCCIO			VSS	VCCIO	VSS			VCCIO	VSS	VCCIO	VCCIO	VSS		SA_DQS[0]	SA_DQ[4]		SA_DQ[5]	VSS	SA_DQ[1]						AJ
																											VSS		RSVD		AH
										VCCIO	VCCIO		VSS	VCCIO	VCCIO	VCCIO	VSS	RSVD		eDP_HPD	VSS		FDI1_LSYNC	VSS	SA_DQ[0]		eDP_AUX#	DPLL_REF_CLK		DPLL_REF_CLK#	AG
										VSS	VCCIO		VCCIO	VSS	VCCIO												eDP_AUX	eDP_COMPIO		VSS	AF
																VCCIO	VCCIO	VSS		eDP_TX#[2]	eDP_TX[2]		VSS	eDP_TX#[3]	eDP_TX[3]						AE

Figure 8-11. BGA1023 Ballmap (Top View, Lower-Left Quadrant)



AD	VSS		VAXG	VAXG		VAXG	VAXG		VAXG	VAXG	VAXG	VAXG		VAXG	VAXG															
AC	VAXG															VSS														
AB	VSS		VAXG	VAXG		VAXG	VAXG		VAXG	VAXG	VAXG	VAXG		VSS	VAXG															
AA						VSS	VSS		VSS	VSS	VSS	VSS				VAXG														
Y	VAXG		VSS	VSS										VAXG	VSS															
W	VAXG					VAXG	VAXG		VAXG	VAXG	VAXG	VAXG				VSS														
V	VSS		VAXG	VAXG		VAXG	VAXG		VAXG	VAXG	VAXG	VAXG		VAXG	VAXG															
U																VAXG														
T	VAXG		VAXG	VAXG		VSS	VSS		VSS	VSS	VSS	VSS		VAXG	VSS															
R																VSS														
P	VAXG		VSS	VSS		VAXG	VAXG		VAXG	VAXG	VAXG	VAXG		VAXG	VAXG															
N	VSS		BCLK_ITP	BCLK_ITP#		VSS	PREQ#		PRDY#	VSS	VSS	RSVD		VSS	VSS		VAXG		VSS	RSVD		VSS		VCC		VSS		VCC	VSS	
M		TDI		VSS																										
L	VSS		TDO			TCK	TMS		CFG[17]		CFG[14]			VSS	RSVD		RSVD		VSS	RSVD		VCC		VSS		VCC		VSS	VCC	
K				DBR#					CFG[11]		VSS		CFG[10]	RSVD			VSSAXG_VAL_SENSE		VSS_VAL_SENSE	VCC			VCC		VCC		VCC	VCC		VCC
J	BPM#[7]		BPM#[6]	TRST#			VSS						VSS							VCC		VCC		VCC	VCC		VCC	VCC		VCC
H		BPM#[5]		VSS					VSS		CFG[9]		CFG[7]	RSVD			VAXG_VAL_SENSE		VCC_VAL_SENSE			VCC		VCC	VCC		VCC	VCC		VCC
G	VSS		BPM#[4]	BPM#[0]			BPM#[3]		CFG[13]		VSS			VSS			VSSAXG_SENSE		VSS_SENSE	VCC										
F							VSS		CFG[12]		CFG[15]		PROC_SELECT#	VCC_DIE_SENSE			VAXG_SENSE		VCC_SENSE	VCC		VSS		VCC	VCC		VSS	VCC		VCC
E	VSS_NCTF		BPM#[2]				BPM#[1]															VSS		VCC	VCC		VSS	VCC		VCC
D	DC_TEST_D61		VSS_NCTF	VSS				VSS	CFG[3]	CFG[16]		VSS	VCCSA_VID[1]	VCCSA_VID[0]		VSS	THERMTRIP#	RESET#	VSS	VCC		VSS	VCC		VCC		VSS	VCC		VCC
C	DC_TEST_C61		DC_TEST_C59	VSS_NCTF	PROC_DETECT#		CFG[6]		CFG[5]		CFG[1]		CATERR#	PM_SYNC			PROCHOT#	VIDSOUT		VCC		VSS	VCC		VCC		VSS	VCC		VCC
B								CFG[2]				CFG[0]				UNCOREPWRGOOD			VIDSCLK											
A	DC_TEST_A61		DC_TEST_A59	DC_TEST_A58	VSS_NCTF		CFG[8]		VSS		CFG[4]		VSS	PECI			VSS	VIDALERT#		VCC		VSS	VCC	VCC	VSS		VCC	VCC	VSS	
	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32

Figure 8-12. BGA1023 Ballmap (Top View, Lower-Right Quadrant)



										VCCIO	VSS		VCCIO	VSS	VCCIO												VSS		eDP_ICOMPO		AD
																	VSS	VCCIO	FDI1_FSYNC		VSS	FDI1_TX#[3]	FDI1_TX[3]		VSS		eDP_TX#[1]	eDP_TX#[0]		eDP_TX[0]	AC
										VSS	VCCIO		VSS	VCCIO	VSS																AB
																VCCIO	VCCIO	VSS		FDI0_FSYNC	FDI0_LSYNC		VSS	FDI0_TX[3]	FDI0_TX#[3]		eDP_TX[1]	FDI1_TX[2]		VSS	AA
																											VSS		FDI1_TX#[2]		Y
										VSS	VCCSA		VSS	VCCIO	VCCIO	VSS	RSVD	VSS		FDI0_TX#[1]	FDI0_TX[1]		VSS	FDI1_TX[0]	FDI1_TX#[0]			FDI0_TX[2]		FDI0_TX#[2]	W
										VCCSA	VSS		VCCSA	VCCSA	VCCSA												FDI1_TX#[1]				V
																VCCSA	RSVD	VSS		FDI_INT	VCCSA_SENSE		VSS	FDI0_TX#[0]	FDI0_TX[0]						U
																											FDI1_TX[1]	DMI_TX[3]		VSS	T
										VCCSA	VSS		VCCSA	VSS	VCCSA												VSS		DMI_TX#[3]		R
										VSS	VCCSA		VSS	VCCSA	VSS		VSS	RSVD		DMI_RX[3]	DMI_RX#[3]	VSS		DMI_RX[1]	DMI_RX#[1]		DMI_TX[2]	DMI_RX[2]		DMI_RX#[2]	P
	VCC		VSS		VCC	VSS			VCCSA	VSS	VCCSA			VSS	VCCSA												DMI_TX#[2]	DMI_RX[0]		VSS	N
																VSS	RSVD	RSVD		VSS	PEG_TX#[12]		DMI_TX#[1]	DMI_TX[1]	VSS		VSS		DMI_RX#[0]		M
	VSS		VCC		VSS	VCC			VSS	VCCSA	VSS			VCCSA	VSS																L
		VCC		VCC	VCC		RSVD		PEG_RX[0]	VSS		PEG_RX[1]		PEG_TX[6]		PEG_TX#[6]		PEG_TX[10]		VSS	PEG_TX[12]		VSS	PEG_RX#[15]	PEG_RX[15]		PEG_TX[15]	DMI_TX[0]		DMI_TX#[0]	K
		VCC	VCC		VCC	VCC				PEG_RX#[1]							PEG_TX#[10]										PEG_TX#[15]	BCLK		VSS	J
		VCC	VCC		VCC	VCC			PEG_RX#[0]	VSS		PEG_TX#[4]		VSS			VSS	PEG_TX#[11]			VSS		PEG_RX#[13]		PEG_RX[13]		VSS		BCLK#		H
									PEG_TX#[0]			PEG_TX[4]		PEG_TX[7]				PEG_TX[11]			PEG_TX[13]		PEG_RX#[10]		VSS		PEG_RCOMPO	PEG_ICOMPI		PEG_ICOMPO	G
		VSS	VCC		VCC	VCC			PEG_TX[0]	PEG_TX#[3]		VSS		PEG_TX#[7]		VSS	PEG_TX#[8]	VSS			PEG_TX#[13]		PEG_RX[10]		PEG_RX[14]						F
		VSS	VCC		VCC	VSS				PEG_TX[3]							PEG_TX[8]									PEG_RX#[14]		VSS		VSS_NCTF	E
		VSS		VCC	VSS		PEG_TX[2]	PEG_TX#[2]	VSS	PEG_RX#[3]		PEG_RX[3]	VSS	PEG_RX#[5]	PEG_RX[5]		VSS	PEG_RX#[7]	PEG_RX[7]		VSS	PEG_TX#[14]	PEG_TX[14]		VSS		VSS	DC_TEST_D3		DC_TEST_D1	D
		VSS		VCC	VCC			PEG_TX#[1]		PEG_RX[2]		PEG_RX[4]		PEG_TX#[5]		PEG_TX[9]		PEG_RX[6]		PEG_RX[8]		PEG_RX[9]	PEG_RX[11]			PEG_RX[12]	DC_TEST_C4	VSS_NCTF			C
									PEG_RX#[2]				PEG_TX[5]				PEG_RX#[6]				PEG_RX#[9]				PEG_RX#[12]						B
VCC		VCC	VSS		VCC	VSS		PEG_TX[1]		VSS		PEG_RX#[4]		VSS		PEG_TX#[9]		VSS		PEG_RX#[8]		VSS	PEG_RX#[11]			VSS_NCTF	DC_TEST_A4				A
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 8-3. BGA1023 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
BCLK	J3	Diff Clk	I
BCLK#	H2	Diff Clk	I
BCLK_ITP	N59	Diff Clk	I
BCLK_ITP#	N58	Diff Clk	I
BPM#[0]	G58	Asynch CMOS	I/O
BPM#[1]	E55	Asynch CMOS	I/O
BPM#[2]	E59	Asynch CMOS	I/O
BPM#[3]	G55	Asynch CMOS	I/O
BPM#[4]	G59	Asynch CMOS	I/O
BPM#[5]	H60	Asynch CMOS	I/O
BPM#[6]	J59	Asynch CMOS	I/O
BPM#[7]	J61	Asynch CMOS	I/O
CATERR#	C49	Asynch CMOS	O
CFG[0]	B50	CMOS	I
CFG[1]	C51	CMOS	I
CFG[2]	B54	CMOS	I
CFG[3]	D53	CMOS	I
CFG[4]	A51	CMOS	I
CFG[5]	C53	CMOS	I
CFG[6]	C55	CMOS	I
CFG[7]	H49	CMOS	I
CFG[8]	A55	CMOS	I
CFG[9]	H51	CMOS	I
CFG[10]	K49	CMOS	I
CFG[11]	K53	CMOS	I
CFG[12]	F53	CMOS	I
CFG[13]	G53	CMOS	I
CFG[14]	L51	CMOS	I
CFG[15]	F51	CMOS	I
CFG[16]	D52	CMOS	I
CFG[17]	L53	CMOS	I
DBR#	K58	Asynch CMOS	O
DC_TEST_A4	A4	N/A	
DC_TEST_A58	A58	N/A	
DC_TEST_A59	A59	N/A	
DC_TEST_A61	A61	N/A	
DC_TEST_BD1	BD1	N/A	
DC_TEST_BD61	BD61	N/A	
DC_TEST_BE1	BE1	N/A	
DC_TEST_BE3	BE3	N/A	
DC_TEST_BE59	BE59	N/A	
DC_TEST_BE61	BE61	N/A	
DC_TEST_BG1	BG1	N/A	
DC_TEST_BG3	BG3	N/A	
DC_TEST_BG4	BG4	N/A	
DC_TEST_BG58	BG58	N/A	
DC_TEST_BG59	BG59	N/A	
DC_TEST_BG61	BG61	N/A	
DC_TEST_C4	C4	N/A	
DC_TEST_C59	C59	N/A	
DC_TEST_C61	C61	N/A	
DC_TEST_D1	D1	N/A	
DC_TEST_D3	D3	N/A	
DC_TEST_D61	D61	N/A	
DMI_RX#[0]	M2	DMI	I
DMI_RX#[1]	P6	DMI	I
DMI_RX#[2]	P1	DMI	I
DMI_RX#[3]	P10	DMI	I
DMI_RX[0]	N3	DMI	I
DMI_RX[1]	P7	DMI	I
DMI_RX[2]	P3	DMI	I
DMI_RX[3]	P11	DMI	I
DMI_TX#[0]	K1	DMI	O
DMI_TX#[1]	M8	DMI	O
DMI_TX#[2]	N4	DMI	O
DMI_TX#[3]	R2	DMI	O
DMI_TX[0]	K3	DMI	O
DMI_TX[1]	M7	DMI	O
DMI_TX[2]	P4	DMI	O
DMI_TX[3]	T3	DMI	O
DPLL_REF_CLK	AG3	Diff Clk	I
DPLL_REF_CLK#	AG1	Diff Clk	I
eDP_AUX	AF4	eDP	I/O
eDP_AUX#	AG4	eDP	I/O
eDP_COMPIO	AF3	Analog	I
eDP_HPD#	AG11	Asynch CMOS	I
eDP_ICOMPO	AD2	Analog	I
eDP_TX#[0]	AC3	eDP	O
eDP_TX#[1]	AC4	eDP	O
eDP_TX#[2]	AE11	eDP	O
eDP_TX#[3]	AE7	eDP	O
eDP_TX[0]	AC1	eDP	O
eDP_TX[1]	AA4	eDP	O
eDP_TX[2]	AE10	eDP	O
eDP_TX[3]	AE6	eDP	O
FDI_INT	U11	Asynch CMOS	I
FDI0_FSYNC	AA11	CMOS	I
FDI0_LSYNC	AA10	CMOS	I
FDI0_TX#[0]	U7	FDI	O
FDI0_TX#[1]	W11	FDI	O
FDI0_TX#[2]	W1	FDI	O
FDI0_TX#[3]	AA6	FDI	O
FDI0_TX[0]	U6	FDI	O
FDI0_TX[1]	W10	FDI	O

Table 8-3. BGA1023 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
FDI0_TX[2]	W3	FDI	O
FDI0_TX[3]	AA7	FDI	O
FDI1_FSYNC	AC12	CMOS	I
FDI1_LSYNC	AG8	CMOS	I
FDI1_TX#[0]	W6	FDI	O
FDI1_TX#[1]	V4	FDI	O
FDI1_TX#[2]	Y2	FDI	O
FDI1_TX#[3]	AC9	FDI	O
FDI1_TX[0]	W7	FDI	O
FDI1_TX[1]	T4	FDI	O
FDI1_TX[2]	AA3	FDI	O
FDI1_TX[3]	AC8	FDI	O
PECI	A48	Asynch	I/O
PEG_ICOMPI	G3	Analog	I
PEG_ICOMPO	G1	Analog	I
PEG_RCOMPO	G4	Analog	I
PEG_RX#[0]	H22	PCIe	I
PEG_RX#[1]	J21	PCIe	I
PEG_RX#[2]	B22	PCIe	I
PEG_RX#[3]	D21	PCIe	I
PEG_RX#[4]	A19	PCIe	I
PEG_RX#[5]	D17	PCIe	I
PEG_RX#[6]	B14	PCIe	I
PEG_RX#[7]	D13	PCIe	I
PEG_RX#[8]	A11	PCIe	I
PEG_RX#[9]	B10	PCIe	I
PEG_RX#[10]	G8	PCIe	I
PEG_RX#[11]	A8	PCIe	I
PEG_RX#[12]	B6	PCIe	I
PEG_RX#[13]	H8	PCIe	I
PEG_RX#[14]	E5	PCIe	I
PEG_RX#[15]	K7	PCIe	I
PEG_RX[0]	K22	PCIe	I
PEG_RX[1]	K19	PCIe	I
PEG_RX[2]	C21	PCIe	I
PEG_RX[3]	D19	PCIe	I
PEG_RX[4]	C19	PCIe	I
PEG_RX[5]	D16	PCIe	I
PEG_RX[6]	C13	PCIe	I
PEG_RX[7]	D12	PCIe	I
PEG_RX[8]	C11	PCIe	I
PEG_RX[9]	C9	PCIe	I
PEG_RX[10]	F8	PCIe	I
PEG_RX[11]	C8	PCIe	I
PEG_RX[12]	C5	PCIe	I
PEG_RX[13]	H6	PCIe	I
PEG_RX[14]	F6	PCIe	I
PEG_RX[15]	K6	PCIe	I
PEG_TX#[0]	G22	PCIe	O
PEG_TX#[1]	C23	PCIe	O
PEG_TX#[2]	D23	PCIe	O
PEG_TX#[3]	F21	PCIe	O
PEG_TX#[4]	H19	PCIe	O
PEG_TX#[5]	C17	PCIe	O
PEG_TX#[6]	K15	PCIe	O
PEG_TX#[7]	F17	PCIe	O
PEG_TX#[8]	F14	PCIe	O
PEG_TX#[9]	A15	PCIe	O
PEG_TX#[10]	J14	PCIe	O
PEG_TX#[11]	H13	PCIe	O
PEG_TX#[12]	M10	PCIe	O
PEG_TX#[13]	F10	PCIe	O
PEG_TX#[14]	D9	PCIe	O
PEG_TX#[15]	J4	PCIe	O
PEG_TX[0]	F22	PCIe	O
PEG_TX[1]	A23	PCIe	O
PEG_TX[2]	D24	PCIe	O
PEG_TX[3]	E21	PCIe	O
PEG_TX[4]	G19	PCIe	O
PEG_TX[5]	B18	PCIe	O
PEG_TX[6]	K17	PCIe	O
PEG_TX[7]	G17	PCIe	O
PEG_TX[8]	E14	PCIe	O
PEG_TX[9]	C15	PCIe	O
PEG_TX[10]	K13	PCIe	O
PEG_TX[11]	G13	PCIe	O
PEG_TX[12]	K10	PCIe	O
PEG_TX[13]	G10	PCIe	O
PEG_TX[14]	D8	PCIe	O
PEG_TX[15]	K4	PCIe	O
PM_SYNC	C48	Asynch CMOS	I
PRDY#	N53	Asynch CMOS	O
PREQ#	N55	Asynch CMOS	I
PROC_DETECT#	C57	Analog	O
PROC_SELECT#	F49	N/A	O
PROCHOT#	C45	Asynch CMOS	I/O
RESET#	D44	Asynch CMOS	I
RSVD	BG26		
RSVD	BG22		
RSVD	BG7		
RSVD	BF23		
RSVD	BE26		
RSVD	BE24		
RSVD	BE22		

Table 8-3. BGA1023 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
RSVD	BE7		
RSVD	BD26		
RSVD	BD25		
RSVD	BD22		
RSVD	BD21		
RSVD	BB21		
RSVD	BB19		
RSVD	BA22		
RSVD	BA19		
RSVD	AY22		
RSVD	AY21		
RSVD	AV19		
RSVD	AU21		
RSVD	AU19		
RSVD	AT49		
RSVD	AT21		
RSVD	AM15		
RSVD	AM14		
RSVD	AH2		
RSVD	AG13		
RSVD	W14		
RSVD	U14		
RSVD	P13		
RSVD	N50		
RSVD	N42		
RSVD	M14		
RSVD	M13		
RSVD	L47		
RSVD	L45		
RSVD	L42		
RSVD	K48		
RSVD	K24		
RSVD	H48		
SA_BS[0]	BD37	DDR3	O
SA_BS[1]	BF36	DDR3	O
SA_BS[2]	BA28	DDR3	O
SA_CAS#	BE39	DDR3	O
SA_CKE[0]	AY26	DDR3	O
SA_CKE[1]	BB26	DDR3	O
SA_CK#[0]	AV36	DDR3	O
SA_CK#[1]	AU40	DDR3	O
SA_CK[0]	AU36	DDR3	O
SA_CK[1]	AT40	DDR3	O
SA_CS#[0]	BB40	DDR3	O
SA_CS#[1]	BC41	DDR3	O
SA_DQ[0]	AG6	DDR3	I/O
SA_DQ[1]	AJ6	DDR3	I/O

Table 8-3. BGA1023 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
SA_DQ[2]	AP11	DDR3	I/O
SA_DQ[3]	AL6	DDR3	I/O
SA_DQ[4]	AJ10	DDR3	I/O
SA_DQ[5]	AJ8	DDR3	I/O
SA_DQ[6]	AL8	DDR3	I/O
SA_DQ[7]	AL7	DDR3	I/O
SA_DQ[8]	AR11	DDR3	I/O
SA_DQ[9]	AP6	DDR3	I/O
SA_DQ[10]	AU6	DDR3	I/O
SA_DQ[11]	AV9	DDR3	I/O
SA_DQ[12]	AR6	DDR3	I/O
SA_DQ[13]	AP8	DDR3	I/O
SA_DQ[14]	AT13	DDR3	I/O
SA_DQ[15]	AU13	DDR3	I/O
SA_DQ[16]	BC7	DDR3	I/O
SA_DQ[17]	BB7	DDR3	I/O
SA_DQ[18]	BA13	DDR3	I/O
SA_DQ[19]	BB11	DDR3	I/O
SA_DQ[20]	BA7	DDR3	I/O
SA_DQ[21]	BA9	DDR3	I/O
SA_DQ[22]	BB9	DDR3	I/O
SA_DQ[23]	AY13	DDR3	I/O
SA_DQ[24]	AV14	DDR3	I/O
SA_DQ[25]	AR14	DDR3	I/O
SA_DQ[26]	AY17	DDR3	I/O
SA_DQ[27]	AR19	DDR3	I/O
SA_DQ[28]	BA14	DDR3	I/O
SA_DQ[29]	AU14	DDR3	I/O
SA_DQ[30]	BB14	DDR3	I/O
SA_DQ[31]	BB17	DDR3	I/O
SA_DQ[32]	BA45	DDR3	I/O
SA_DQ[33]	AR43	DDR3	I/O
SA_DQ[34]	AW48	DDR3	I/O
SA_DQ[35]	BC48	DDR3	I/O
SA_DQ[36]	BC45	DDR3	I/O
SA_DQ[37]	AR45	DDR3	I/O
SA_DQ[38]	AT48	DDR3	I/O
SA_DQ[39]	AY48	DDR3	I/O
SA_DQ[40]	BA49	DDR3	I/O
SA_DQ[41]	AV49	DDR3	I/O
SA_DQ[42]	BB51	DDR3	I/O
SA_DQ[43]	AY53	DDR3	I/O
SA_DQ[44]	BB49	DDR3	I/O
SA_DQ[45]	AU49	DDR3	I/O
SA_DQ[46]	BA53	DDR3	I/O
SA_DQ[47]	BB55	DDR3	I/O
SA_DQ[48]	BA55	DDR3	I/O

Table 8-3. BGA1023 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
SA_DQ[49]	AV56	DDR3	I/O
SA_DQ[50]	AP50	DDR3	I/O
SA_DQ[51]	AP53	DDR3	I/O
SA_DQ[52]	AV54	DDR3	I/O
SA_DQ[53]	AT54	DDR3	I/O
SA_DQ[54]	AP56	DDR3	I/O
SA_DQ[55]	AP52	DDR3	I/O
SA_DQ[56]	AN57	DDR3	I/O
SA_DQ[57]	AN53	DDR3	I/O
SA_DQ[58]	AG56	DDR3	I/O
SA_DQ[59]	AG53	DDR3	I/O
SA_DQ[60]	AN55	DDR3	I/O
SA_DQ[61]	AN52	DDR3	I/O
SA_DQ[62]	AG55	DDR3	I/O
SA_DQ[63]	AK56	DDR3	I/O
SA_DQS#[0]	AL11	DDR3	I/O
SA_DQS#[1]	AR8	DDR3	I/O
SA_DQS#[2]	AV11	DDR3	I/O
SA_DQS#[3]	AT17	DDR3	I/O
SA_DQS#[4]	AV45	DDR3	I/O
SA_DQS#[5]	AY51	DDR3	I/O
SA_DQS#[6]	AT55	DDR3	I/O
SA_DQS#[7]	AK55	DDR3	I/O
SA_DQS[0]	AJ11	DDR3	I/O
SA_DQS[1]	AR10	DDR3	I/O
SA_DQS[2]	AY11	DDR3	I/O
SA_DQS[3]	AU17	DDR3	I/O
SA_DQS[4]	AW45	DDR3	I/O
SA_DQS[5]	AV51	DDR3	I/O
SA_DQS[6]	AT56	DDR3	I/O
SA_DQS[7]	AK54	DDR3	I/O
SA_MA[0]	BG35	DDR3	O
SA_MA[1]	BB34	DDR3	O
SA_MA[2]	BE35	DDR3	O
SA_MA[3]	BD35	DDR3	O
SA_MA[4]	AT34	DDR3	O
SA_MA[5]	AU34	DDR3	O
SA_MA[6]	BB32	DDR3	O
SA_MA[7]	AT32	DDR3	O
SA_MA[8]	AY32	DDR3	O
SA_MA[9]	AV32	DDR3	O
SA_MA[10]	BE37	DDR3	O
SA_MA[11]	BA30	DDR3	O
SA_MA[12]	BC30	DDR3	O
SA_MA[13]	AW41	DDR3	O
SA_MA[14]	AY28	DDR3	O
SA_MA[15]	AU26	DDR3	O
SA_ODT[0]	AY40	DDR3	O
SA_ODT[1]	BA41	DDR3	O
SA_RAS#	BD39	DDR3	O
SA_WE#	AT41	DDR3	O
SB_BS[0]	BG39	DDR3	O
SB_BS[1]	BD42	DDR3	O
SB_BS[2]	AT22	DDR3	O
SB_CAS#	AV43	DDR3	O
SB_CKE[0]	AR22	DDR3	O
SB_CKE[1]	BF27	DDR3	O
SB_CK#[0]	AY34	DDR3	O
SB_CK#[1]	BB36	DDR3	O
SB_CK[0]	BA34	DDR3	O
SB_CK[1]	BA36	DDR3	O
SB_CS#[0]	BE41	DDR3	O
SB_CS#[1]	BE47	DDR3	O
SB_DQ[0]	AL4	DDR3	I/O
SB_DQ[1]	AL1	DDR3	I/O
SB_DQ[2]	AN3	DDR3	I/O
SB_DQ[3]	AR4	DDR3	I/O
SB_DQ[4]	AK4	DDR3	I/O
SB_DQ[5]	AK3	DDR3	I/O
SB_DQ[6]	AN4	DDR3	I/O
SB_DQ[7]	AR1	DDR3	I/O
SB_DQ[8]	AU4	DDR3	I/O
SB_DQ[9]	AT2	DDR3	I/O
SB_DQ[10]	AV4	DDR3	I/O
SB_DQ[11]	BA4	DDR3	I/O
SB_DQ[12]	AU3	DDR3	I/O
SB_DQ[13]	AR3	DDR3	I/O
SB_DQ[14]	AY2	DDR3	I/O
SB_DQ[15]	BA3	DDR3	I/O
SB_DQ[16]	BE9	DDR3	I/O
SB_DQ[17]	BD9	DDR3	I/O
SB_DQ[18]	BD13	DDR3	I/O
SB_DQ[19]	BF12	DDR3	I/O
SB_DQ[20]	BF8	DDR3	I/O
SB_DQ[21]	BD10	DDR3	I/O
SB_DQ[22]	BD14	DDR3	I/O
SB_DQ[23]	BE13	DDR3	I/O
SB_DQ[24]	BF16	DDR3	I/O
SB_DQ[25]	BE17	DDR3	I/O
SB_DQ[26]	BE18	DDR3	I/O
SB_DQ[27]	BE21	DDR3	I/O
SB_DQ[28]	BE14	DDR3	I/O
SB_DQ[29]	BG14	DDR3	I/O
SB_DQ[30]	BG18	DDR3	I/O

Table 8-3. BGA1023 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
SB_DQ[31]	BF19	DDR3	I/O
SB_DQ[32]	BD50	DDR3	I/O
SB_DQ[33]	BF48	DDR3	I/O
SB_DQ[34]	BD53	DDR3	I/O
SB_DQ[35]	BF52	DDR3	I/O
SB_DQ[36]	BD49	DDR3	I/O
SB_DQ[37]	BE49	DDR3	I/O
SB_DQ[38]	BD54	DDR3	I/O
SB_DQ[39]	BE53	DDR3	I/O
SB_DQ[40]	BF56	DDR3	I/O
SB_DQ[41]	BE57	DDR3	I/O
SB_DQ[42]	BC59	DDR3	I/O
SB_DQ[43]	AY60	DDR3	I/O
SB_DQ[44]	BE54	DDR3	I/O
SB_DQ[45]	BG54	DDR3	I/O
SB_DQ[46]	BA58	DDR3	I/O
SB_DQ[47]	AW59	DDR3	I/O
SB_DQ[48]	AW58	DDR3	I/O
SB_DQ[49]	AU58	DDR3	I/O
SB_DQ[50]	AN61	DDR3	I/O
SB_DQ[51]	AN59	DDR3	I/O
SB_DQ[52]	AU59	DDR3	I/O
SB_DQ[53]	AU61	DDR3	I/O
SB_DQ[54]	AN58	DDR3	I/O
SB_DQ[55]	AR58	DDR3	I/O
SB_DQ[56]	AK58	DDR3	I/O
SB_DQ[57]	AL58	DDR3	I/O
SB_DQ[58]	AG58	DDR3	I/O
SB_DQ[59]	AG59	DDR3	I/O
SB_DQ[60]	AM60	DDR3	I/O
SB_DQ[61]	AL59	DDR3	I/O
SB_DQ[62]	AF61	DDR3	I/O
SB_DQ[63]	AH60	DDR3	I/O
SB_DQS#[0]	AL3	DDR3	I/O
SB_DQS#[1]	AV3	DDR3	I/O
SB_DQS#[2]	BG11	DDR3	I/O
SB_DQS#[3]	BD17	DDR3	I/O
SB_DQS#[4]	BG51	DDR3	I/O
SB_DQS#[5]	BA59	DDR3	I/O
SB_DQS#[6]	AT60	DDR3	I/O
SB_DQS#[7]	AK59	DDR3	I/O
SB_DQS[0]	AM2	DDR3	I/O
SB_DQS[1]	AV1	DDR3	I/O
SB_DQS[2]	BE11	DDR3	I/O
SB_DQS[3]	BD18	DDR3	I/O
SB_DQS[4]	BE51	DDR3	I/O
SB_DQS[5]	BA61	DDR3	I/O

Table 8-3. BGA1023 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
SB_DQS[6]	AR59	DDR3	I/O
SB_DQS[7]	AK61	DDR3	I/O
SB_MA[0]	BF32	DDR3	O
SB_MA[1]	BE33	DDR3	O
SB_MA[2]	BD33	DDR3	O
SB_MA[3]	AU30	DDR3	O
SB_MA[4]	BD30	DDR3	O
SB_MA[5]	AV30	DDR3	O
SB_MA[6]	BG30	DDR3	O
SB_MA[7]	BD29	DDR3	O
SB_MA[8]	BE30	DDR3	O
SB_MA[9]	BE28	DDR3	O
SB_MA[10]	BD43	DDR3	O
SB_MA[11]	AT28	DDR3	O
SB_MA[12]	AV28	DDR3	O
SB_MA[13]	BD46	DDR3	O
SB_MA[14]	AT26	DDR3	O
SB_MA[15]	AU22	DDR3	O
SB_ODT[0]	AT43	DDR3	O
SB_ODT[1]	BG47	DDR3	O
SB_RAS#	BF40	DDR3	O
SB_WE#	BD45	DDR3	O
SM_DRAMPWROK	BE45	Asynch CMOS	I
SM_DRAMRST#	AT30	DDR3	O
SM_RCOMP[0]	BF44	Analog	I/O
SM_RCOMP[1]	BE43	Analog	I/O
SM_RCOMP[2]	BG43	Analog	I/O
SM_VREF	AY43	Analog	I
TCK	L56	CMOS	I
TDI	M60	CMOS	I
TDO	L59	CMOS	O
THERMTRIP#	D45	Asynch CMOS	O
TMS	L55	CMOS	I
TRST#	J58	CMOS	I
UNCOREPWRGOOD	B46	Asynch CMOS	I
VAXG	AE46	PWR	
VAXG	AD59	PWR	
VAXG	AD58	PWR	
VAXG	AD56	PWR	
VAXG	AD55	PWR	
VAXG	AD53	PWR	
VAXG	AD52	PWR	
VAXG	AD51	PWR	
VAXG	AD50	PWR	
VAXG	AD48	PWR	
VAXG	AD47	PWR	
VAXG	AC61	PWR	

Table 8-3. BGA1023 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VAXG	AB59	PWR	
VAXG	AB58	PWR	
VAXG	AB56	PWR	
VAXG	AB55	PWR	
VAXG	AB53	PWR	
VAXG	AB52	PWR	
VAXG	AB51	PWR	
VAXG	AB50	PWR	
VAXG	AB47	PWR	
VAXG	AA46	PWR	
VAXG	Y61	PWR	
VAXG	Y48	PWR	
VAXG	W61	PWR	
VAXG	W56	PWR	
VAXG	W55	PWR	
VAXG	W53	PWR	
VAXG	W52	PWR	
VAXG	W51	PWR	
VAXG	W50	PWR	
VAXG	V59	PWR	
VAXG	V58	PWR	
VAXG	V56	PWR	
VAXG	V55	PWR	
VAXG	V53	PWR	
VAXG	V52	PWR	
VAXG	V51	PWR	
VAXG	V50	PWR	
VAXG	V48	PWR	
VAXG	V47	PWR	
VAXG	U46	PWR	
VAXG	T61	PWR	
VAXG	T59	PWR	
VAXG	T58	PWR	
VAXG	T48	PWR	
VAXG	P61	PWR	
VAXG	P56	PWR	
VAXG	P55	PWR	
VAXG	P53	PWR	
VAXG	P52	PWR	
VAXG	P51	PWR	
VAXG	P50	PWR	
VAXG	P48	PWR	
VAXG	P47	PWR	
VAXG	N45	PWR	
VAXG_SENSE	F45	Analog	O
VAXG_VAL_SENSE	H45	Analog	O
VCC	N38	PWR	
VCC	N34	PWR	
VCC	N30	PWR	
VCC	N26	PWR	
VCC	L40	PWR	
VCC	L36	PWR	
VCC	L33	PWR	
VCC	L28	PWR	
VCC	L25	PWR	
VCC	K42	PWR	
VCC	K39	PWR	
VCC	K37	PWR	
VCC	K35	PWR	
VCC	K34	PWR	
VCC	K32	PWR	
VCC	K29	PWR	
VCC	K27	PWR	
VCC	K26	PWR	
VCC	J42	PWR	
VCC	J40	PWR	
VCC	J38	PWR	
VCC	J37	PWR	
VCC	J35	PWR	
VCC	J34	PWR	
VCC	J32	PWR	
VCC	J29	PWR	
VCC	J28	PWR	
VCC	J26	PWR	
VCC	J25	PWR	
VCC	H40	PWR	
VCC	H38	PWR	
VCC	H37	PWR	
VCC	H35	PWR	
VCC	H34	PWR	
VCC	H32	PWR	
VCC	H29	PWR	
VCC	H28	PWR	
VCC	H26	PWR	
VCC	H25	PWR	
VCC	G42	PWR	
VCC	F42	PWR	
VCC	F38	PWR	
VCC	F37	PWR	
VCC	F34	PWR	
VCC	F32	PWR	
VCC	F28	PWR	
VCC	F26	PWR	
VCC	F25	PWR	

Table 8-3. BGA1023 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VCC	E38	PWR	
VCC	E37	PWR	
VCC	E34	PWR	
VCC	E32	PWR	
VCC	E28	PWR	
VCC	E26	PWR	
VCC	D42	PWR	
VCC	D39	PWR	
VCC	D37	PWR	
VCC	D34	PWR	
VCC	D32	PWR	
VCC	D27	PWR	
VCC	C42	PWR	
VCC	C39	PWR	
VCC	C37	PWR	
VCC	C34	PWR	
VCC	C32	PWR	
VCC	C27	PWR	
VCC	C26	PWR	
VCC	A42	PWR	
VCC	A39	PWR	
VCC	A38	PWR	
VCC	A35	PWR	
VCC	A34	PWR	
VCC	A31	PWR	
VCC	A29	PWR	
VCC	A26	PWR	
VCC_DIE_SENSE	F48	Analog	O
VCC_SENSE	F43	Analog	O
VCC_VAL_SENSE	H43	Analog	O
VCCDQ	AN26	PWR	
VCCDQ	AM28	PWR	
VCCIO	AN48	PWR	
VCCIO	AN45	PWR	
VCCIO	AN42	PWR	
VCCIO	AN20	PWR	
VCCIO	AM47	PWR	
VCCIO	AM43	PWR	
VCCIO	AM21	PWR	
VCCIO	AM17	PWR	
VCCIO	AM16	PWR	
VCCIO	AL48	PWR	
VCCIO	AL45	PWR	
VCCIO	AL26	PWR	
VCCIO	AL22	PWR	
VCCIO	AL20	PWR	
VCCIO	AL16	PWR	

Table 8-3. BGA1023 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VCCIO	AL15	PWR	
VCCIO	AL14	PWR	
VCCIO	AK51	PWR	
VCCIO	AK50	PWR	
VCCIO	AJ47	PWR	
VCCIO	AJ43	PWR	
VCCIO	AJ25	PWR	
VCCIO	AJ21	PWR	
VCCIO	AJ17	PWR	
VCCIO	AJ15	PWR	
VCCIO	AJ14	PWR	
VCCIO	AG51	PWR	
VCCIO	AG50	PWR	
VCCIO	AG48	PWR	
VCCIO	AG21	PWR	
VCCIO	AG20	PWR	
VCCIO	AG17	PWR	
VCCIO	AG16	PWR	
VCCIO	AG15	PWR	
VCCIO	AF46	PWR	
VCCIO	AF20	PWR	
VCCIO	AF18	PWR	
VCCIO	AF16	PWR	
VCCIO	AE15	PWR	
VCCIO	AE14	PWR	
VCCIO	AD21	PWR	
VCCIO	AD18	PWR	
VCCIO	AD16	PWR	
VCCIO	AC13	PWR	
VCCIO	AB20	PWR	
VCCIO	AB17	PWR	
VCCIO	AA15	PWR	
VCCIO	AA14	PWR	
VCCIO	W17	PWR	
VCCIO	W16	PWR	
VCCIO_SEL	BC22	N/A	O
VCCIO_SENSE	AN16	Analog	O
VCCPLL	BC4	PWR	
VCCPLL	BC1	PWR	
VCCPLL	BB3	PWR	
VCCPQE	AN22	PWR	
VCCPQE	AM25	PWR	
VCCSA	W20	PWR	
VCCSA	V21	PWR	
VCCSA	V18	PWR	
VCCSA	V17	PWR	
VCCSA	V16	PWR	

Table 8-3. BGA1023 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VCCSA	U15	PWR	
VCCSA	R21	PWR	
VCCSA	R18	PWR	
VCCSA	R16	PWR	
VCCSA	P20	PWR	
VCCSA	P17	PWR	
VCCSA	N22	PWR	
VCCSA	N20	PWR	
VCCSA	N16	PWR	
VCCSA	L21	PWR	
VCCSA	L17	PWR	
VCCSA_SENSE	U10	Analog	O
VCCSA_VID[0]	D48	CMOS	O
VCCSA_VID[1]	D49	CMOS	O
VDDQ	BG33	PWR	
VDDQ	BB28	PWR	
VDDQ	BA40	PWR	
VDDQ	AW26	PWR	
VDDQ	AV41	PWR	
VDDQ	AR40	PWR	
VDDQ	AR36	PWR	
VDDQ	AR34	PWR	
VDDQ	AR32	PWR	
VDDQ	AR30	PWR	
VDDQ	AR28	PWR	
VDDQ	AR26	PWR	
VDDQ	AN38	PWR	
VDDQ	AN34	PWR	
VDDQ	AN30	PWR	
VDDQ	AM40	PWR	
VDDQ	AM36	PWR	
VDDQ	AM33	PWR	
VDDQ	AL42	PWR	
VDDQ	AL38	PWR	
VDDQ	AL34	PWR	
VDDQ	AL30	PWR	
VDDQ	AJ40	PWR	
VDDQ	AJ36	PWR	
VDDQ	AJ33	PWR	
VDDQ	AJ28	PWR	
VDDQ_SENSE	BC43	Analog	O
VIDALERT#	A44	CMOS	I
VIDSCLK	B43	CMOS	O
VIDSOUT	C44	CMOS	I/O
VSS	BG53	GND	
VSS	BG49	GND	
VSS	BG45	GND	
VSS	BG41	GND	
VSS	BG37	GND	
VSS	BG28	GND	
VSS	BG24	GND	
VSS	BG21	GND	
VSS	BG17	GND	
VSS	BG13	GND	
VSS	BG9	GND	
VSS	BE5	GND	
VSS	BD56	GND	
VSS	BD52	GND	
VSS	BD48	GND	
VSS	BD44	GND	
VSS	BD40	GND	
VSS	BD36	GND	
VSS	BD32	GND	
VSS	BD27	GND	
VSS	BD23	GND	
VSS	BD19	GND	
VSS	BD16	GND	
VSS	BD12	GND	
VSS	BD8	GND	
VSS	BC57	GND	
VSS	BC13	GND	
VSS	BC5	GND	
VSS	BB53	GND	
VSS	BA51	GND	
VSS	BA48	GND	
VSS	BA32	GND	
VSS	BA26	GND	
VSS	BA21	GND	
VSS	BA17	GND	
VSS	BA11	GND	
VSS	BA1	GND	
VSS	AY58	GND	
VSS	AY55	GND	
VSS	AY49	GND	
VSS	AY45	GND	
VSS	AY41	GND	
VSS	AY36	GND	
VSS	AY30	GND	
VSS	AY19	GND	
VSS	AY14	GND	
VSS	AY9	GND	
VSS	AY4	GND	
VSS	AW61	GND	
VSS	AW43	GND	

Table 8-3. BGA1023 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VSS	AW13	GND	
VSS	AW7	GND	
VSS	AV55	GND	
VSS	AV48	GND	
VSS	AV40	GND	
VSS	AV34	GND	
VSS	AV22	GND	
VSS	AV21	GND	
VSS	AV17	GND	
VSS	AU51	GND	
VSS	AU32	GND	
VSS	AU28	GND	
VSS	AU11	GND	
VSS	AU7	GND	
VSS	AU1	GND	
VSS	AT58	GND	
VSS	AT52	GND	
VSS	AT45	GND	
VSS	AT36	GND	
VSS	AT19	GND	
VSS	AT14	GND	
VSS	AT4	GND	
VSS	AR61	GND	
VSS	AR48	GND	
VSS	AR41	GND	
VSS	AR21	GND	
VSS	AR17	GND	
VSS	AR13	GND	
VSS	AR7	GND	
VSS	AP55	GND	
VSS	AP51	GND	
VSS	AP10	GND	
VSS	AP7	GND	
VSS	AN54	GND	
VSS	AN50	GND	
VSS	AN47	GND	
VSS	AN43	GND	
VSS	AN40	GND	
VSS	AN36	GND	
VSS	AN33	GND	
VSS	AN28	GND	
VSS	AN25	GND	
VSS	AN21	GND	
VSS	AN1	GND	
VSS	AM58	GND	
VSS	AM48	GND	
VSS	AM45	GND	
VSS	AM42	GND	
VSS	AM38	GND	
VSS	AM34	GND	
VSS	AM30	GND	
VSS	AM26	GND	
VSS	AM22	GND	
VSS	AM20	GND	
VSS	AM13	GND	
VSS	AM4	GND	
VSS	AL61	GND	
VSS	AL47	GND	
VSS	AL43	GND	
VSS	AL40	GND	
VSS	AL36	GND	
VSS	AL33	GND	
VSS	AL28	GND	
VSS	AL25	GND	
VSS	AL21	GND	
VSS	AL17	GND	
VSS	AL13	GND	
VSS	AL10	GND	
VSS	AK52	GND	
VSS	AK1	GND	
VSS	AJ48	GND	
VSS	AJ45	GND	
VSS	AJ42	GND	
VSS	AJ38	GND	
VSS	AJ34	GND	
VSS	AJ30	GND	
VSS	AJ26	GND	
VSS	AJ22	GND	
VSS	AJ20	GND	
VSS	AJ16	GND	
VSS	AJ13	GND	
VSS	AJ7	GND	
VSS	AH58	GND	
VSS	AH4	GND	
VSS	AG61	GND	
VSS	AG52	GND	
VSS	AG47	GND	
VSS	AG18	GND	
VSS	AG14	GND	
VSS	AG10	GND	
VSS	AG7	GND	
VSS	AF59	GND	
VSS	AF58	GND	
VSS	AF56	GND	

Table 8-3. BGA1023 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VSS	AF55	GND	
VSS	AF53	GND	
VSS	AF52	GND	
VSS	AF51	GND	
VSS	AF50	GND	
VSS	AF48	GND	
VSS	AF47	GND	
VSS	AF21	GND	
VSS	AF17	GND	
VSS	AF1	GND	
VSS	AE13	GND	
VSS	AE8	GND	
VSS	AD61	GND	
VSS	AD20	GND	
VSS	AD17	GND	
VSS	AD4	GND	
VSS	AC46	GND	
VSS	AC14	GND	
VSS	AC10	GND	
VSS	AC6	GND	
VSS	AB61	GND	
VSS	AB48	GND	
VSS	AB21	GND	
VSS	AB18	GND	
VSS	AB16	GND	
VSS	AA56	GND	
VSS	AA55	GND	
VSS	AA53	GND	
VSS	AA52	GND	
VSS	AA51	GND	
VSS	AA50	GND	
VSS	AA13	GND	
VSS	AA8	GND	
VSS	AA1	GND	
VSS	Y59	GND	
VSS	Y58	GND	
VSS	Y47	GND	
VSS	Y4	GND	
VSS	W46	GND	
VSS	W21	GND	
VSS	W18	GND	
VSS	W15	GND	
VSS	W13	GND	
VSS	W8	GND	
VSS	V61	GND	
VSS	V20	GND	
VSS	U13	GND	

Table 8-3. BGA1023 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VSS	U8	GND	
VSS	T56	GND	
VSS	T55	GND	
VSS	T53	GND	
VSS	T52	GND	
VSS	T51	GND	
VSS	T50	GND	
VSS	T47	GND	
VSS	T1	GND	
VSS	R46	GND	
VSS	R20	GND	
VSS	R17	GND	
VSS	R4	GND	
VSS	P59	GND	
VSS	P58	GND	
VSS	P21	GND	
VSS	P18	GND	
VSS	P16	GND	
VSS	P14	GND	
VSS	P9	GND	
VSS	N61	GND	
VSS	N56	GND	
VSS	N52	GND	
VSS	N51	GND	
VSS	N48	GND	
VSS	N47	GND	
VSS	N43	GND	
VSS	N40	GND	
VSS	N36	GND	
VSS	N33	GND	
VSS	N28	GND	
VSS	N25	GND	
VSS	N21	GND	
VSS	N17	GND	
VSS	N1	GND	
VSS	M58	GND	
VSS	M15	GND	
VSS	M11	GND	
VSS	M6	GND	
VSS	M4	GND	
VSS	L61	GND	
VSS	L48	GND	
VSS	L43	GND	
VSS	L38	GND	
VSS	L34	GND	
VSS	L30	GND	
VSS	L26	GND	

Table 8-3. BGA1023 Processor Ball List by Ball Name

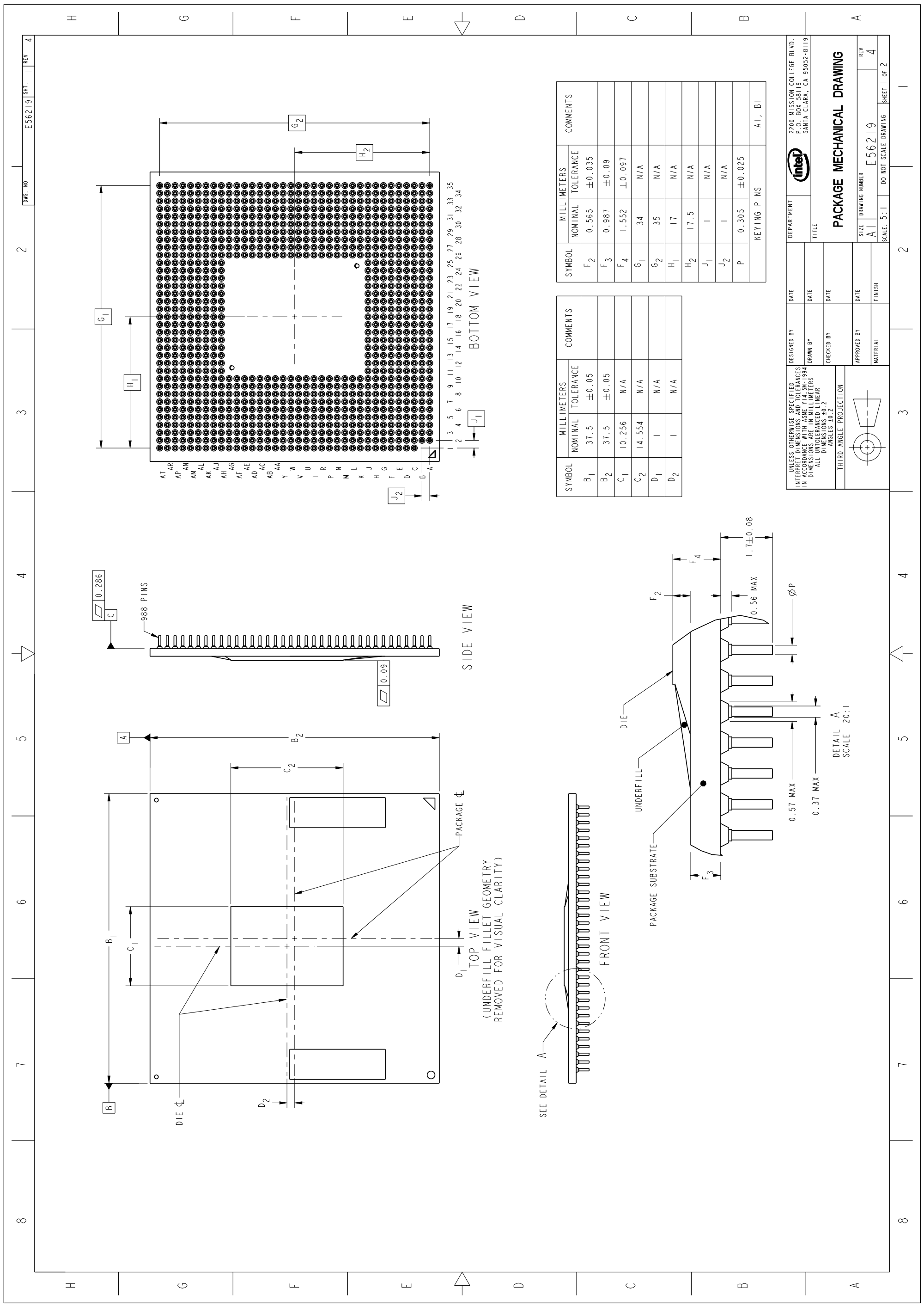
Ball Name	Ball #	Buffer Type	Dir
VSS	L22	GND	
VSS	L20	GND	
VSS	L16	GND	
VSS	K51	GND	
VSS	K21	GND	
VSS	K11	GND	
VSS	K8	GND	
VSS	J55	GND	
VSS	J49	GND	
VSS	J1	GND	
VSS	H58	GND	
VSS	H53	GND	
VSS	H21	GND	
VSS	H17	GND	
VSS	H14	GND	
VSS	H10	GND	
VSS	H4	GND	
VSS	G61	GND	
VSS	G51	GND	
VSS	G48	GND	
VSS	G6	GND	
VSS	F55	GND	
VSS	F40	GND	
VSS	F35	GND	
VSS	F29	GND	
VSS	F19	GND	
VSS	F15	GND	
VSS	F13	GND	
VSS	E40	GND	
VSS	E35	GND	
VSS	E29	GND	
VSS	E25	GND	
VSS	E3	GND	
VSS	D58	GND	
VSS	D54	GND	
VSS	D50	GND	
VSS	D46	GND	
VSS	D43	GND	
VSS	D40	GND	
VSS	D35	GND	
VSS	D29	GND	
VSS	D26	GND	
VSS	D22	GND	
VSS	D18	GND	
VSS	D14	GND	
VSS	D10	GND	
VSS	D6	GND	

Table 8-3. BGA1023 Processor Ball List by Ball Name

Ball Name	Ball #	Buffer Type	Dir
VSS	D4	GND	
VSS	C40	GND	
VSS	C35	GND	
VSS	C29	GND	
VSS	A53	GND	
VSS	A49	GND	
VSS	A45	GND	
VSS	A40	GND	
VSS	A37	GND	
VSS	A33	GND	
VSS	A28	GND	
VSS	A25	GND	
VSS	A21	GND	
VSS	A17	GND	
VSS	A13	GND	
VSS	A9	GND	
VSS_NCTF	BG57		
VSS_NCTF	BG5		
VSS_NCTF	BE58		
VSS_NCTF	BE4		
VSS_NCTF	BD59		
VSS_NCTF	BD3		
VSS_NCTF	BC61		
VSS_NCTF	E61		
VSS_NCTF	E1		
VSS_NCTF	D59		
VSS_NCTF	C58		
VSS_NCTF	C3		
VSS_NCTF	A57		
VSS_NCTF	A5		
VSS_SENSE	G43	Analog	O
VSS_SENSE_VDDQ	BA43	Analog	O
VSS_VAL_SENSE	K43	Analog	O
VSSAXG_SENSE	G45	Analog	O
VSSAXG_VAL_SENSE	K45	Analog	O
VSS_SENSE_VCCIO	AN17	Analog	O

8.2 Package Mechanical Information

Figure 8-13. Processor rPGA988B 2C (GT2) Mechanical Package (Sheet 1 of 2)



SYMBOL	MILLIMETERS		COMMENTS
	NOMINAL	TOLERANCE	
B_1	37.5	±0.05	
B_2	37.5	±0.05	
C_1	10.256	N/A	
C_2	14.554	N/A	
D_1	1	N/A	
D_2	1	N/A	

SYMBOL	MILLIMETERS		COMMENTS
	NOMINAL	TOLERANCE	
F_2	0.565	±0.035	
F_3	0.987	±0.09	
F_4	1.552	±0.097	
G_1	34	N/A	
G_2	35	N/A	
H_1	17	N/A	
H_2	17.5	N/A	
J_1	1	N/A	
J_2	1	N/A	
P	0.305	±0.025	
	KEYING PINS		A1, B1

UNLESS OTHERWISE SPECIFIED
INTERPRET DIMENSIONS AND TOLERANCES
IN ACCORDANCE WITH ASME Y14.5M-1994
DIMENSIONS ARE IN MILLIMETERS
ALL UNTOLERANCED LINEAR
DIMENSIONS ±0.2
ANGLES ±0.2

THIRD ANGLE PROJECTION

DESIGNED BY	DATE	DEPARTMENT	2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119
DRAWN BY	DATE	TITLE	PACKAGE MECHANICAL DRAWING
CHECKED BY	DATE	SIZE A1	DRAWING NUMBER E56219 · REV 4
APPROVED BY	DATE	SCALE: 5:1	DO NOT SCALE DRAWING · SHEET 1 OF 2
MATERIAL	FINISH		

Figure 8-14. Processor rPGA988B 2C (GT2) Mechanical Package (Sheet 2 of 2)

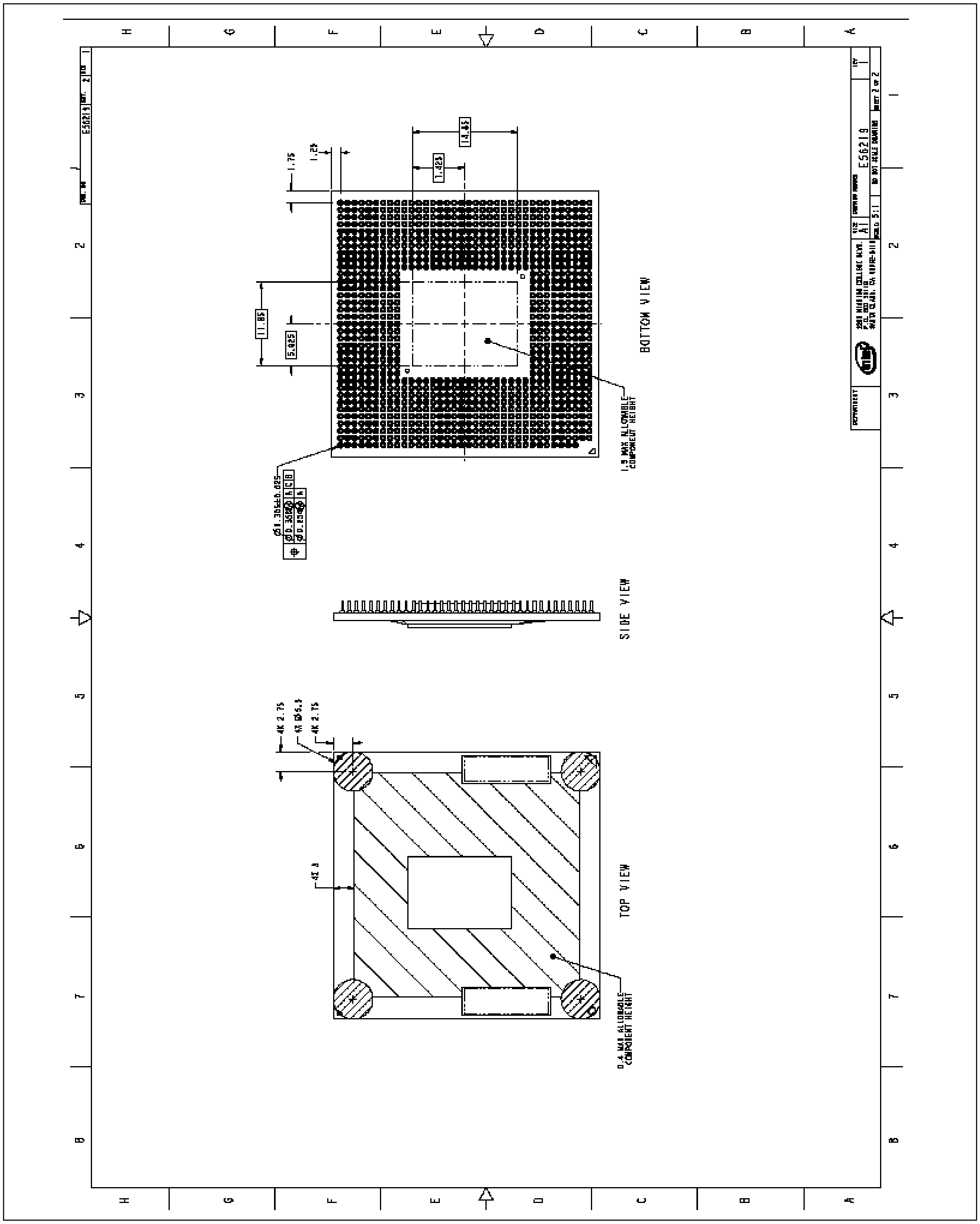
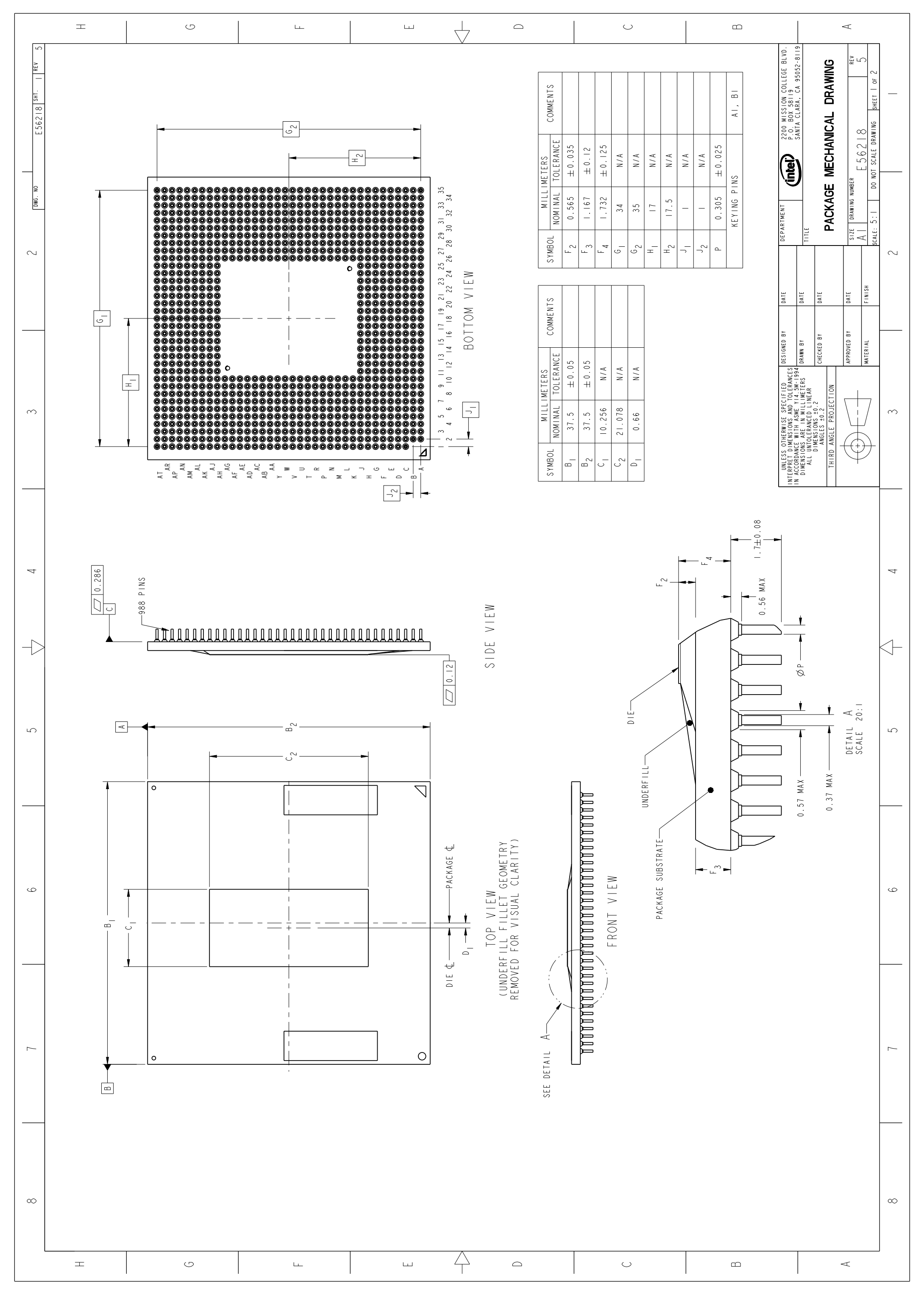


Figure 8-15. Processor rPGA988B 4C (GT2) Mechanical Package (Sheet 1 of 2)



SYMBOL	MILLIMETERS		COMMENTS
	NOMINAL	TOLERANCE	
B_1	37.5	±0.05	
B_2	37.5	±0.05	
C_1	10.256	N/A	
C_2	21.078	N/A	
D_1	0.66	N/A	

SYMBOL	MILLIMETERS		COMMENTS
	NOMINAL	TOLERANCE	
F_2	0.565	±0.035	
F_3	1.167	±0.12	
F_4	1.732	±0.125	
G_1	34	N/A	
G_2	35	N/A	
H_1	17	N/A	
H_2	17.5	N/A	
J_1	1	N/A	
J_2	1	N/A	
P	0.305	±0.025	
	KEYING PINS		A1, B1

Figure 8-16. Processor rPGA988B 4C (GT2) Mechanical Package (Sheet 2 of 2)

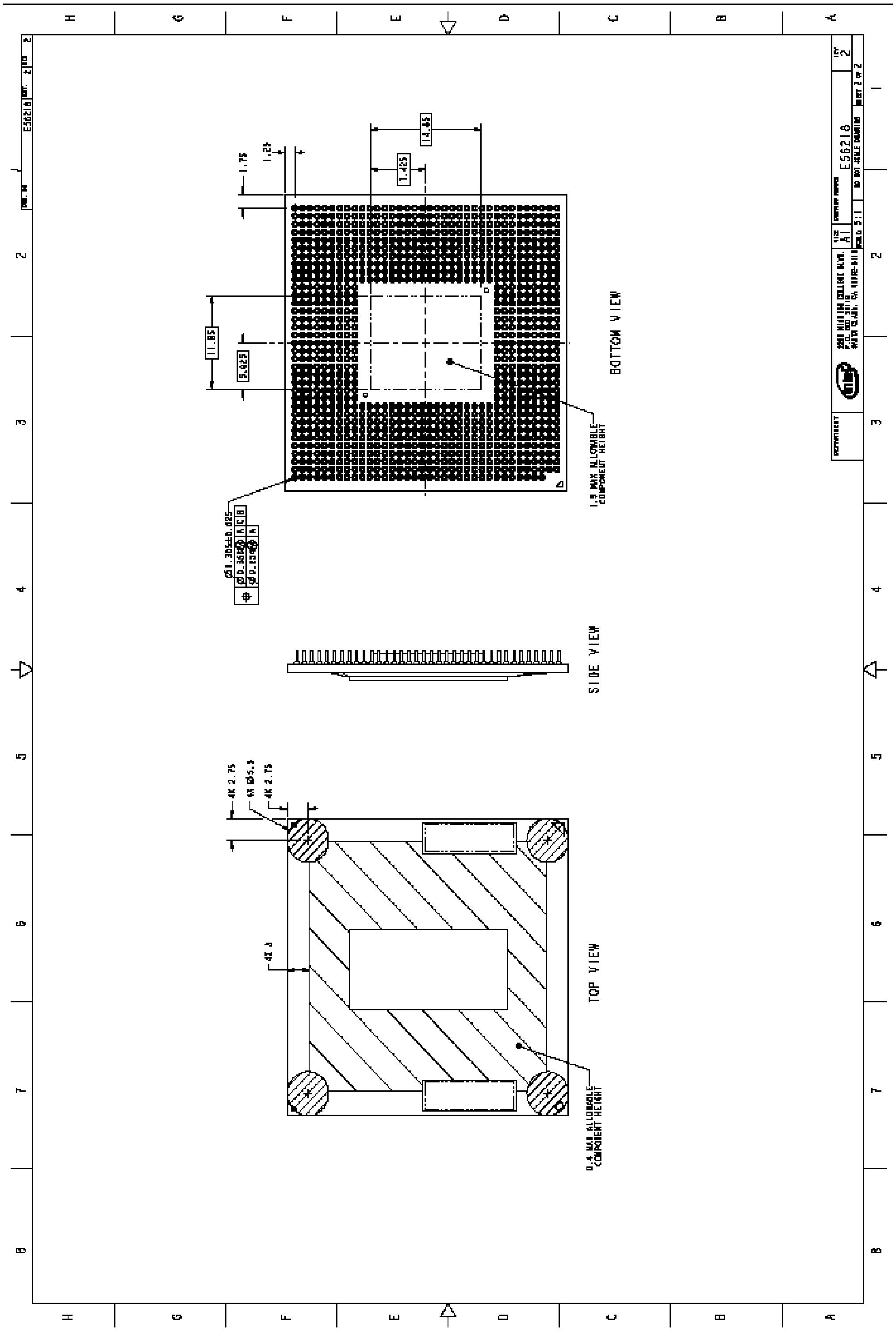
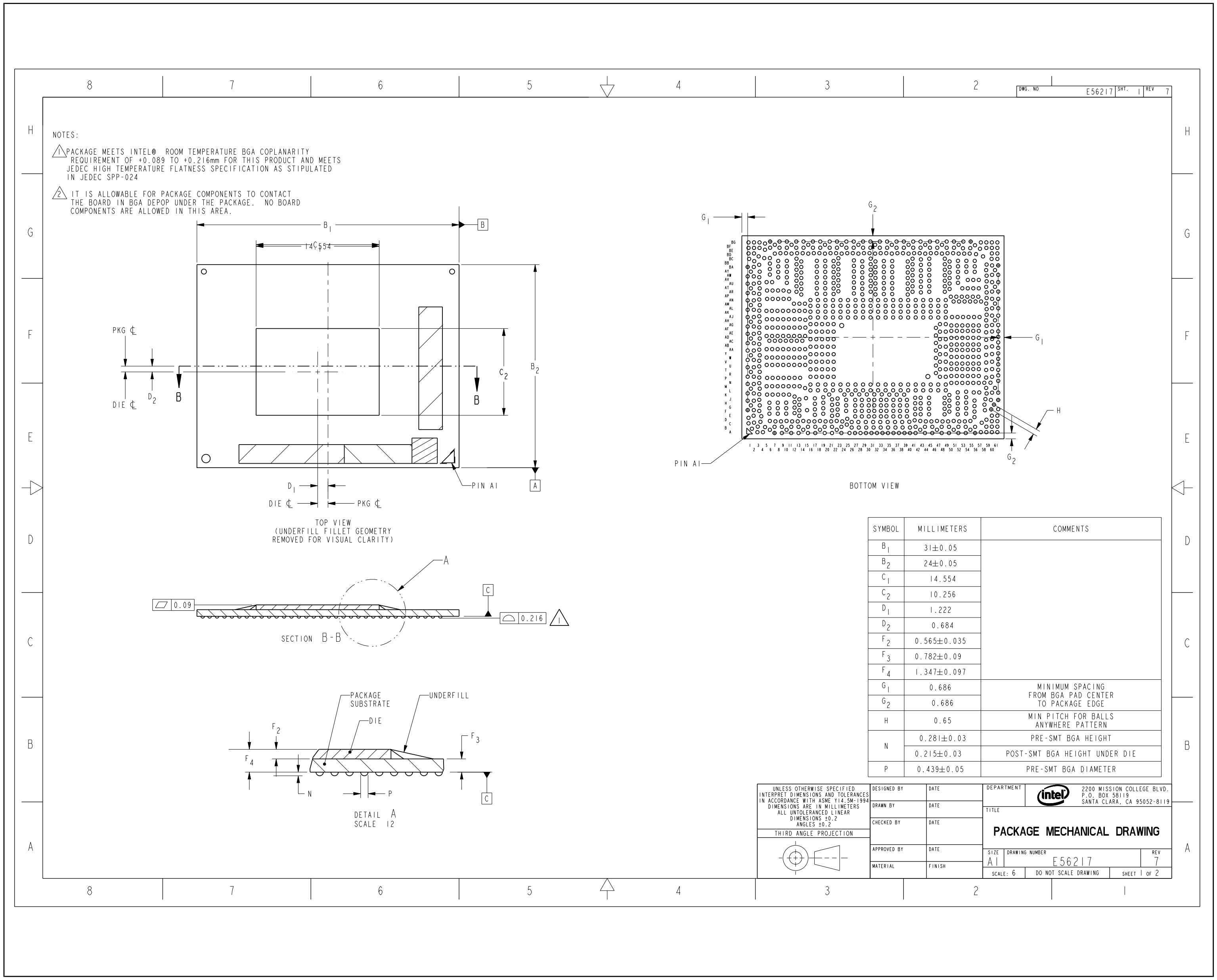


Figure 8-17. Processor BGA1023 2C (GT2) Mechanical Package (Sheet 1 of 2)



NOTES:

1. PACKAGE MEETS INTEL® ROOM TEMPERATURE BGA COPLANARITY REQUIREMENT OF +0.089 TO +0.216mm FOR THIS PRODUCT AND MEETS JEDEC HIGH TEMPERATURE FLATNESS SPECIFICATION AS STIPULATED IN JEDEC SPP-024

2. IT IS ALLOWABLE FOR PACKAGE COMPONENTS TO CONTACT THE BOARD IN BGA DEPOP UNDER THE PACKAGE. NO BOARD COMPONENTS ARE ALLOWED IN THIS AREA.

SYMBOL	MILLIMETERS	COMMENTS
B_1	31±0.05	
B_2	24±0.05	
C_1	14.554	
C_2	10.256	
D_1	1.222	
D_2	0.684	
F_2	0.565±0.035	
F_3	0.782±0.09	
F_4	1.347±0.097	
G_1	0.686	MINIMUM SPACING FROM BGA PAD CENTER TO PACKAGE EDGE
G_2	0.686	
H	0.65	MIN PITCH FOR BALLS ANYWHERE PATTERN
N	0.281±0.03	PRE-SMT BGA HEIGHT
	0.215±0.03	POST-SMT BGA HEIGHT UNDER DIE
P	0.439±0.05	PRE-SMT BGA DIAMETER

Figure 8-18. Processor BGA1023 2C (GT2) Mechanical Package (Sheet 2 of 2)

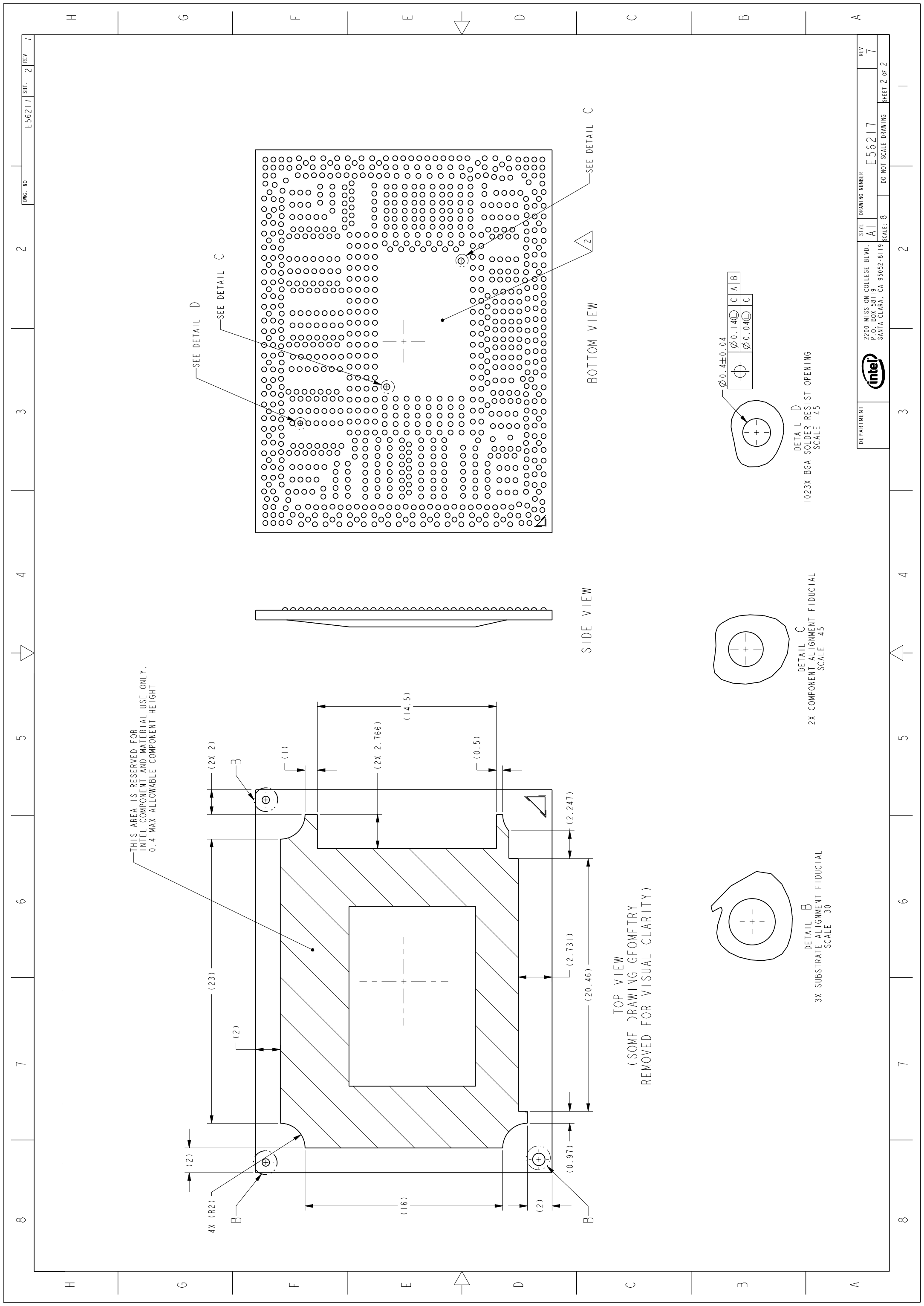
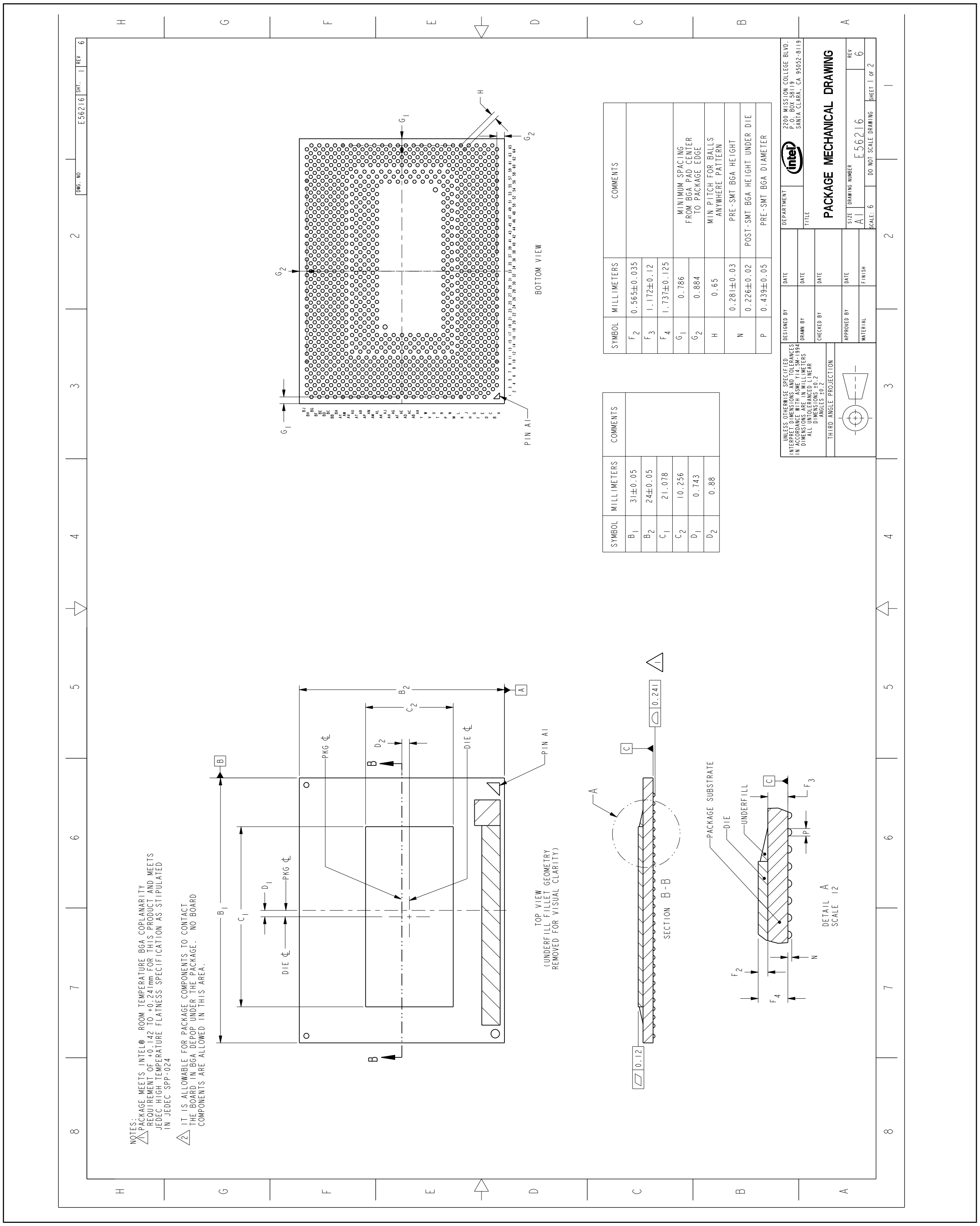


Figure 8-19. Processor BGA1224 4C (GT2) Mechanical Package (Sheet 1 of 2)



SYMBOL	MILLIMETERS	COMMENTS
B_1	31±0.05	
B_2	24±0.05	
C_1	21.078	
C_2	10.256	
D_1	0.743	
D_2	0.88	

SYMBOL	MILLIMETERS	COMMENTS
F_2	0.565±0.035	
F_3	1.172±0.12	
F_4	1.737±0.125	
G_1	0.786	MINIMUM SPACING FROM BGA PAD CENTER TO PACKAGE EDGE
G_2	0.884	
H	0.65	MIN PITCH FOR BALLS ANYWHERE PATTERN
N	0.281±0.03	PRE-SMT BGA HEIGHT
	0.226±0.02	POST-SMT BGA HEIGHT UNDER DIE
P	0.439±0.05	PRE-SMT BGA DIAMETER

Figure 8-20. Processor BGA1224 4C (GT2) Mechanical Package (Sheet 2 of 2)

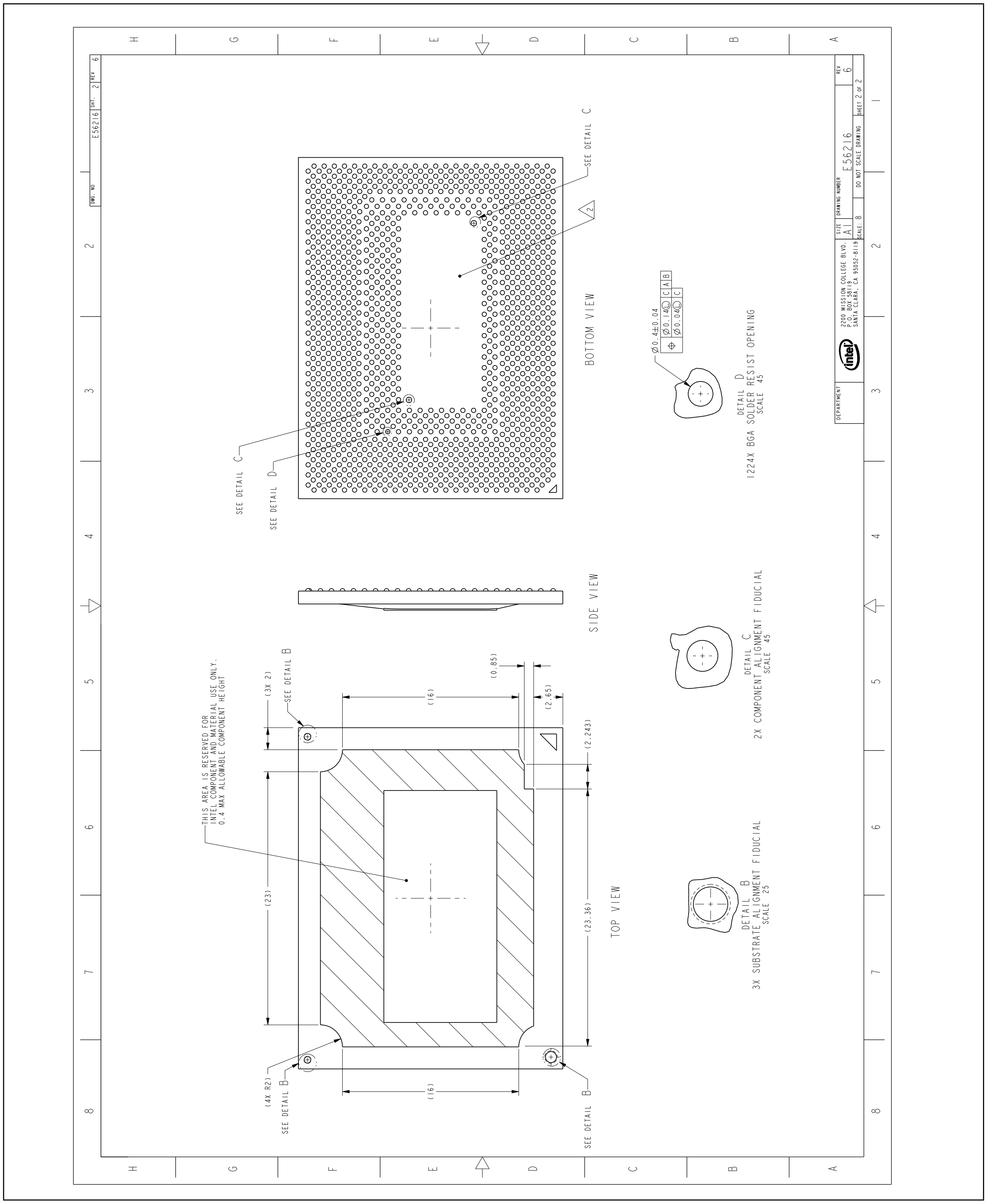
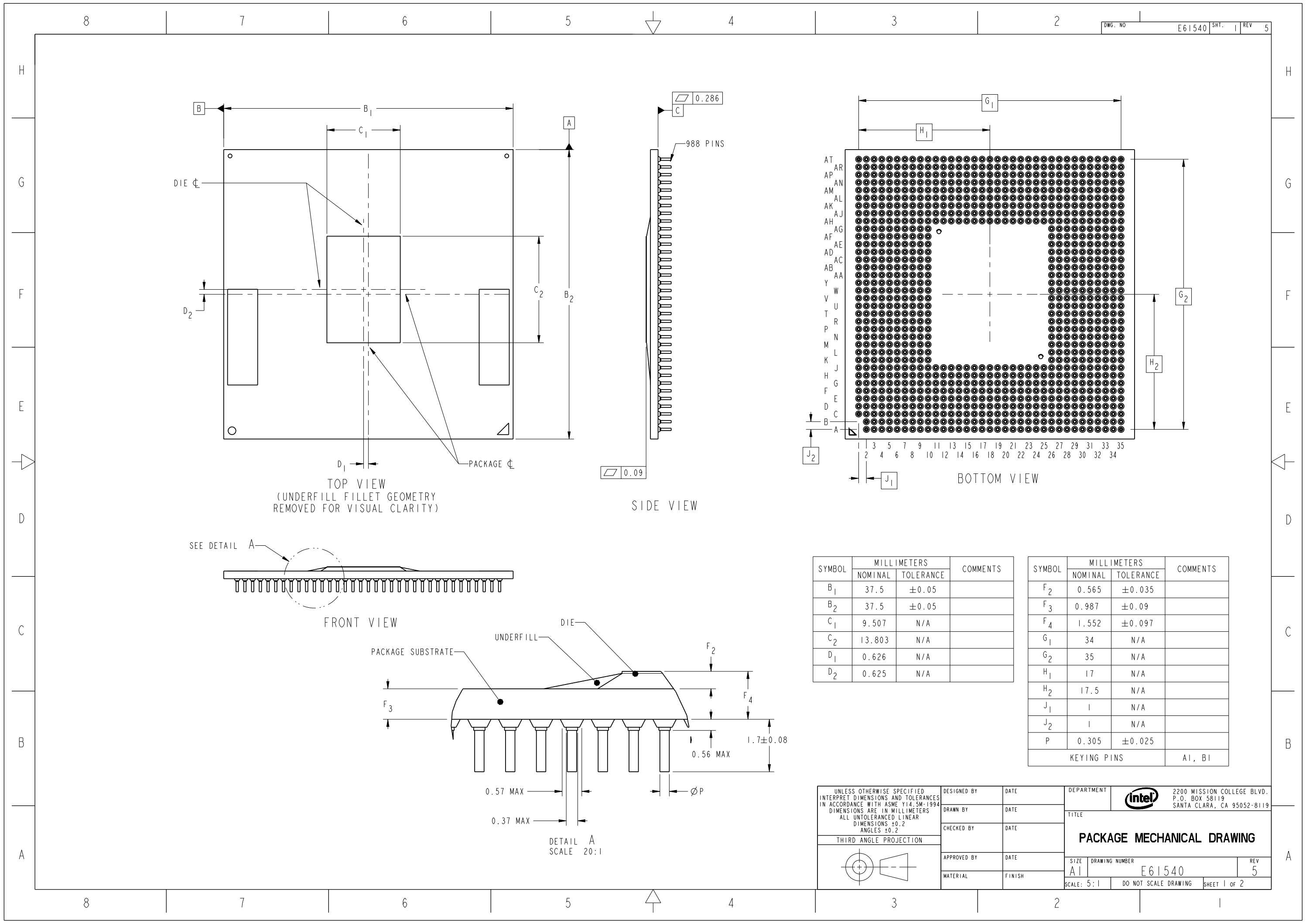


Figure 8-21. Processor rPGA988B 2C (GT1) Mechanical Package (Sheet 1 of 2)



SYMBOL	MILLIMETERS		COMMENTS
	NOMINAL	TOLERANCE	
B_1	37.5	±0.05	
B_2	37.5	±0.05	
C_1	9.507	N/A	
C_2	13.803	N/A	
D_1	0.626	N/A	
D_2	0.625	N/A	

SYMBOL	MILLIMETERS		COMMENTS
	NOMINAL	TOLERANCE	
F_2	0.565	±0.035	
F_3	0.987	±0.09	
F_4	1.552	±0.097	
G_1	34	N/A	
G_2	35	N/A	
H_1	17	N/A	
H_2	17.5	N/A	
J_1	1	N/A	
J_2	1	N/A	
P	0.305	±0.025	
KEYING PINS			A1, B1

Figure 8-22. Processor rPGA988B 2C (GT1) Mechanical Package (Sheet 2 of 2)

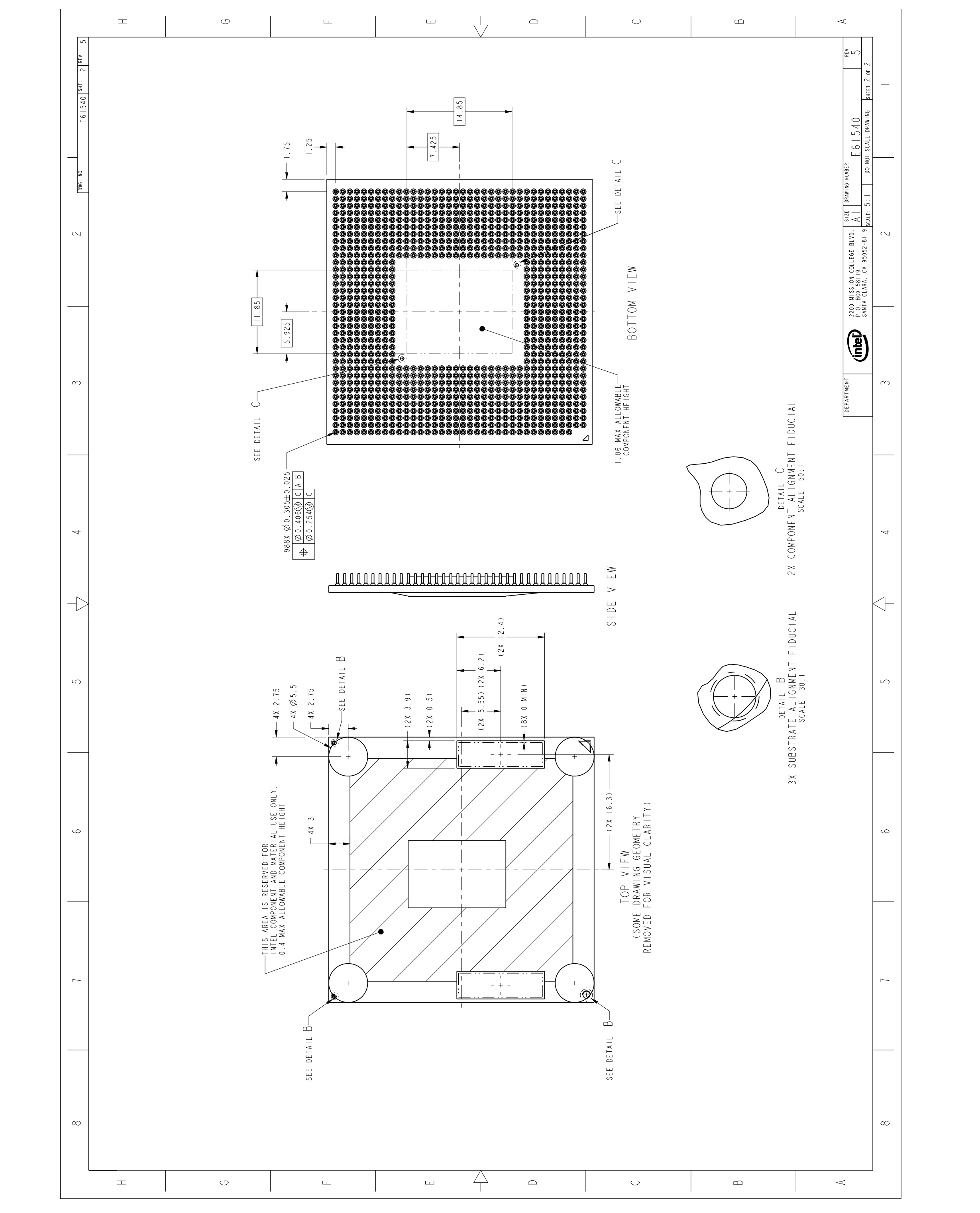
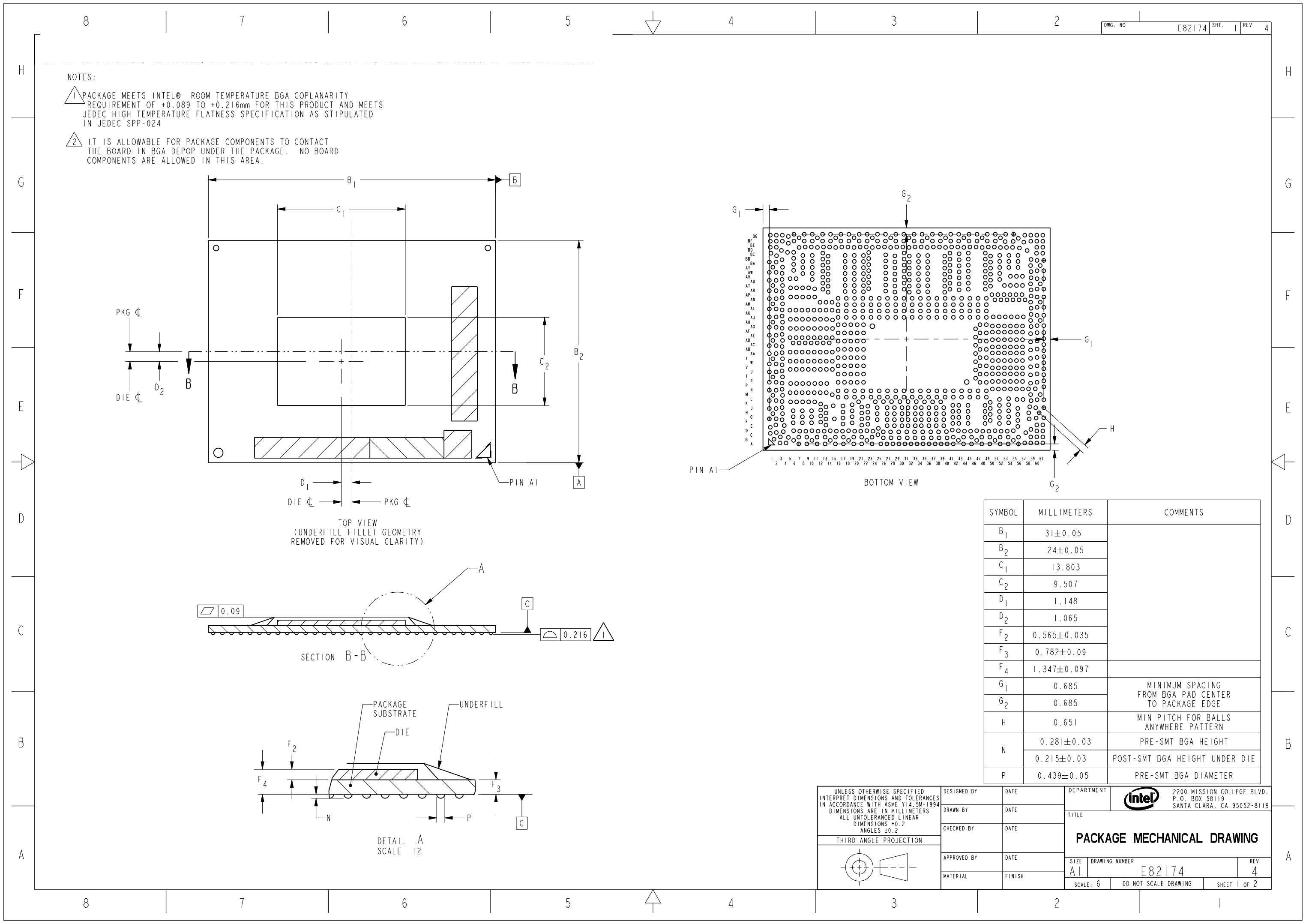


Figure 8-23. Processor BGA1023 2C (GT1) Mechanical Package (Sheet 1 of 2)



NOTES:

1. PACKAGE MEETS INTEL® ROOM TEMPERATURE BGA COPLANARITY REQUIREMENT OF +0.089 TO +0.216mm FOR THIS PRODUCT AND MEETS JEDEC HIGH TEMPERATURE FLATNESS SPECIFICATION AS STIPULATED IN JEDEC SPP-024
2. IT IS ALLOWABLE FOR PACKAGE COMPONENTS TO CONTACT THE BOARD IN BGA DEPOP UNDER THE PACKAGE. NO BOARD COMPONENTS ARE ALLOWED IN THIS AREA.

SYMBOL	MILLIMETERS	COMMENTS
B_1	31±0.05	
B_2	24±0.05	
C_1	13.803	
C_2	9.507	
D_1	1.148	
D_2	1.065	
F_2	0.565±0.035	
F_3	0.782±0.09	
F_4	1.347±0.097	
G_1	0.685	MINIMUM SPACING FROM BGA PAD CENTER TO PACKAGE EDGE
G_2	0.685	
H	0.651	MIN PITCH FOR BALLS ANYWHERE PATTERN
N	0.281±0.03	PRE-SMT BGA HEIGHT
	0.215±0.03	POST-SMT BGA HEIGHT UNDER DIE
P	0.439±0.05	PRE-SMT BGA DIAMETER

UNLESS OTHERWISE SPECIFIED
INTERPRET DIMENSIONS AND TOLERANCES
IN ACCORDANCE WITH ASME Y14.5M-1994
DIMENSIONS ARE IN MILLIMETERS
ALL UNTOLERANCED LINEAR
DIMENSIONS ±0.2
ANGLES ±0.2

THIRD ANGLE PROJECTION

DESIGNED BY / DATE
DRAWN BY / DATE
CHECKED BY / DATE
APPROVED BY / DATE
MATERIAL / FINISH

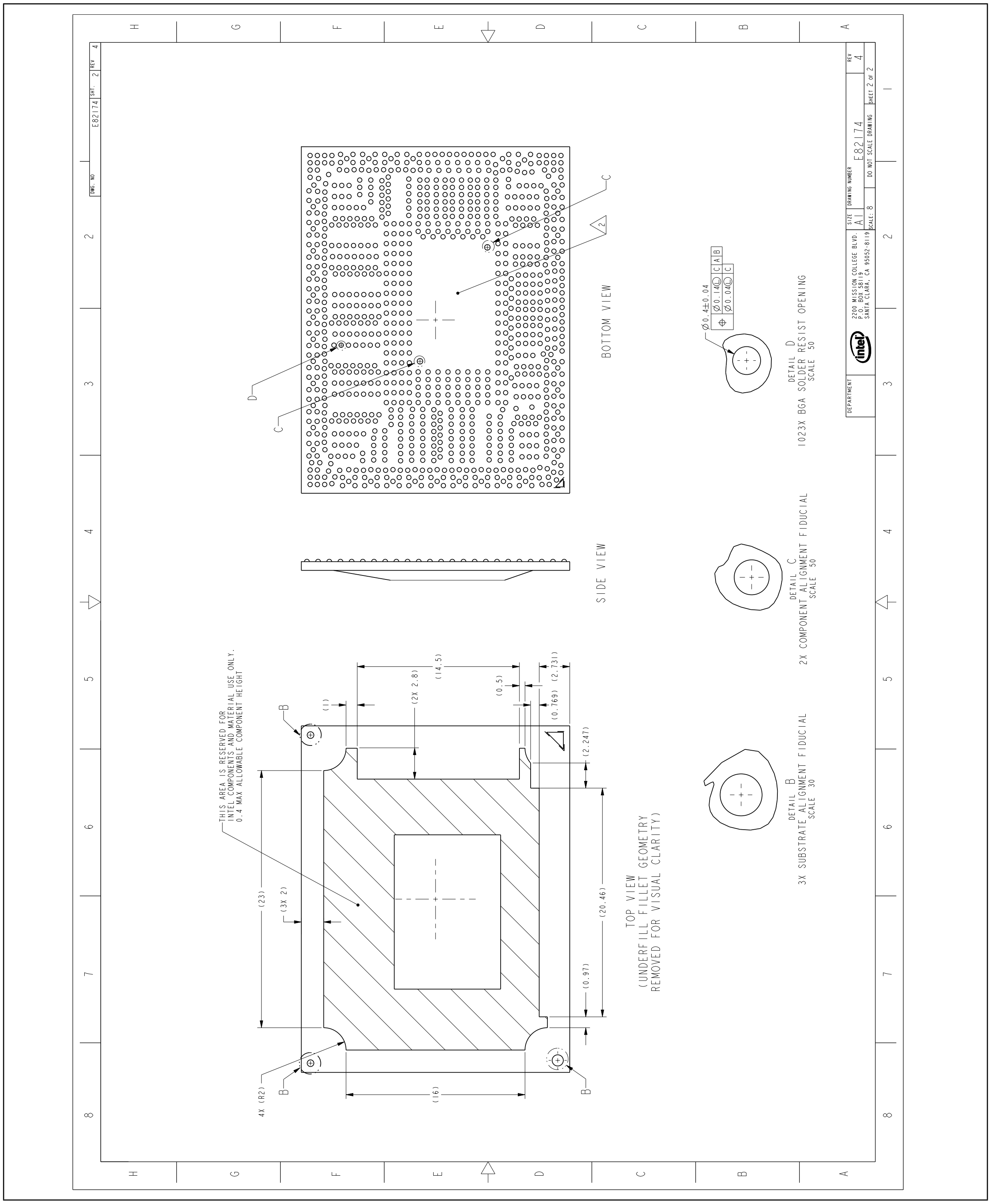
DEPARTMENT

2200 MISSION COLLEGE BLVD.
P.O. BOX 58119
SANTA CLARA, CA 95052-8119

TITLE
PACKAGE MECHANICAL DRAWING

SIZE A1
DRAWING NUMBER E82174
REV 4
SCALE: 6
DO NOT SCALE DRAWING
SHEET 1 OF 2

Figure 8-24. Processor BGA1023 2C (GT1) Mechanical Package (Sheet 2 of 2)



§ §

9 DDR Data Swizzling

To achieve better memory performance and better memory timing; Intel design performed the DDR Data pin swizzling which will allow a better use of the product across different platforms. Swizzling has no effect on functional operation and is invisible to the OS/SW.

However, during debug, swizzling needs to be taken into consideration; thus, swizzling data is presented in this chapter. When placing DIMM logic analyzer, the design engineer must pay attention to the swizzling table to perform an efficient memory debug.

Table 9-1. DDR Data Swizzling Table – Channel A

Pin Name	Pin Number rPGA	Pin Number BGA1023	Pin Number BGA1224	MC Pin Name
SA_DQ[0]	C5	AG6	AL6	DQ01
SA_DQ[1]	D5	AJ6	AL8	DQ02
SA_DQ[2]	D3	AP11	AP7	DQ07
SA_DQ[3]	D2	AL6	AM5	DQ06
SA_DQ[4]	D6	AJ10	AK7	DQ03
SA_DQ[5]	C6	AJ8	AL10	DQ00
SA_DQ[6]	C2	AL8	AN10	DQ05
SA_DQ[7]	C3	AL7	AM9	DQ04
SA_DQ[8]	F10	AR11	AR10	DQ08
SA_DQ[9]	F8	AP6	AR8	DQ10
SA_DQ[10]	G10	AU6	AV7	DQ14
SA_DQ[11]	G9	AV9	AY5	DQ15
SA_DQ[12]	F9	AR6	AT5	DQ09
SA_DQ[13]	F7	AP8	AR6	DQ11
SA_DQ[14]	G8	AT13	AW6	DQ13
SA_DQ[15]	G7	AU13	AT9	DQ12
SA_DQ[16]	K4	BC7	BA6	DQ18
SA_DQ[17]	K5	BB7	BA8	DQ20
SA_DQ[18]	K1	BA13	BG6	DQ22
SA_DQ[19]	J1	BB11	AY9	DQ21
SA_DQ[20]	J5	BA7	AW8	DQ16
SA_DQ[21]	J4	BA9	BB7	DQ17
SA_DQ[22]	J2	BB9	BC8	DQ19
SA_DQ[23]	K2	AY13	BE4	DQ23
SA_DQ[24]	M8	AV14	AW12	DQ27
SA_DQ[25]	N10	AR14	AV11	DQ25
SA_DQ[26]	N8	AY17	BB11	DQ30
SA_DQ[27]	N7	AR19	BA12	DQ31
SA_DQ[28]	M10	BA14	BE8	DQ24
SA_DQ[29]	M9	AU14	BA10	DQ26
SA_DQ[30]	N9	BB14	BD11	DQ28
SA_DQ[31]	M7	BB17	BE12	DQ29
SA_DQ[32]	AG6	BA45	BB49	DQ35
SA_DQ[33]	AG5	AR43	AY49	DQ32
SA_DQ[34]	AK6	AW48	BE52	DQ38
SA_DQ[35]	AK5	BC48	BD51	DQ39
SA_DQ[36]	AH5	BC45	BD49	DQ33
SA_DQ[37]	AH6	AR45	BE48	DQ36
SA_DQ[38]	AJ5	AT48	BA52	DQ34
SA_DQ[39]	AJ6	AY48	AY51	DQ37
SA_DQ[40]	AJ8	BA49	BC54	DQ42
SA_DQ[41]	AK8	AV49	AY53	DQ43
SA_DQ[42]	AJ9	BB51	AW54	DQ44
SA_DQ[43]	AK9	AY53	AY55	DQ47
SA_DQ[44]	AH8	BB49	BD53	DQ41
SA_DQ[45]	AH9	AU49	BB53	DQ40
SA_DQ[46]	AL9	BA53	BE56	DQ46
SA_DQ[47]	AL8	BB55	BA56	DQ45
SA_DQ[48]	AP11	BA55	BD57	DQ51
SA_DQ[49]	AN11	AV56	BF61	DQ50
SA_DQ[50]	AL12	AP50	BA60	DQ53
SA_DQ[51]	AM12	AP53	BB61	DQ52
SA_DQ[52]	AM11	AV54	BE60	DQ49
SA_DQ[53]	AL11	AT54	BD63	DQ48
SA_DQ[54]	AP12	AP56	BB59	DQ54
SA_DQ[55]	AN12	AP52	BC58	DQ55
SA_DQ[56]	AJ14	AN57	AW58	DQ58
SA_DQ[57]	AH14	AN53	AY59	DQ56
SA_DQ[58]	AL15	AG56	AL60	DQ60
SA_DQ[59]	AK15	AG53	AP61	DQ61
SA_DQ[60]	AL14	AN55	AW60	DQ57
SA_DQ[61]	AK14	AN52	AY57	DQ59
SA_DQ[62]	AJ15	AG55	AN60	DQ63
SA_DQ[63]	AH15	AK56	AR60	DQ62

Table 9-2. DDR Data Swizzling Table – Channel B

Pin Name	Pin Number rPGA	Pin Number BGA1023	Pin Number BGA1224	MC Pin Name
SB_DQ[0]	C9	AL4	AL4	DQ03
SB_DQ[1]	A7	AL1	AK3	DQ02
SB_DQ[2]	D10	AN3	AP3	DQ05
SB_DQ[3]	C8	AR4	AR2	DQ04
SB_DQ[4]	A9	AK4	AL2	DQ00
SB_DQ[5]	A8	AK3	AK1	DQ01
SB_DQ[6]	D9	AN4	AP1	DQ06
SB_DQ[7]	D8	AR1	AR4	DQ07
SB_DQ[8]	G4	AU4	AV3	DQ11
SB_DQ[9]	F4	AT2	AU4	DQ10
SB_DQ[10]	F1	AV4	BA4	DQ12
SB_DQ[11]	G1	BA4	BB1	DQ14
SB_DQ[12]	G5	AU3	AV1	DQ08
SB_DQ[13]	F5	AR3	AU2	DQ09
SB_DQ[14]	F2	AY2	BA2	DQ13
SB_DQ[15]	G2	BA3	BB3	DQ15
SB_DQ[16]	J7	BE9	BC2	DQ19
SB_DQ[17]	J8	BD9	BF7	DQ18
SB_DQ[18]	K10	BD13	BF11	DQ20
SB_DQ[19]	K9	BF12	BJ10	DQ22
SB_DQ[20]	J9	BF8	BC4	DQ17
SB_DQ[21]	J10	BD10	BH7	DQ16
SB_DQ[22]	K8	BD14	BH11	DQ21
SB_DQ[23]	K7	BE13	BG10	DQ23
SB_DQ[24]	M5	BF16	BJ14	DQ25
SB_DQ[25]	N4	BE17	BG14	DQ30
SB_DQ[26]	N2	BE18	BF17	DQ29
SB_DQ[27]	N1	BE21	BJ18	DQ28
SB_DQ[28]	M4	BE14	BF13	DQ24
SB_DQ[29]	N5	BG14	BH13	DQ31
SB_DQ[30]	M2	BG18	BH17	DQ27
SB_DQ[31]	M1	BF19	BG18	DQ26
SB_DQ[32]	AM5	BD50	BH49	DQ36
SB_DQ[33]	AM6	BF48	BF47	DQ38
SB_DQ[34]	AR3	BD53	BH53	DQ34
SB_DQ[35]	AP3	BF52	BG50	DQ35
SB_DQ[36]	AN3	BD49	BF49	DQ39
SB_DQ[37]	AN2	BE49	BH47	DQ37
SB_DQ[38]	AN1	BD54	BF53	DQ33
SB_DQ[39]	AP2	BE53	BJ50	DQ32
SB_DQ[40]	AP5	BF56	BF55	DQ44
SB_DQ[41]	AN9	BE57	BH55	DQ43
SB_DQ[42]	AT5	BC59	BJ58	DQ47
SB_DQ[43]	AT6	AY60	BH59	DQ46
SB_DQ[44]	AP6	BE54	BJ54	DQ40
SB_DQ[45]	AN8	BG54	BG54	DQ42
SB_DQ[46]	AR6	BA58	BG58	DQ45
SB_DQ[47]	AR5	AW59	BF59	DQ41
SB_DQ[48]	AR9	AW58	BA64	DQ51
SB_DQ[49]	AJ11	AU58	BC62	DQ49
SB_DQ[50]	AT8	AN61	AU62	DQ52
SB_DQ[51]	AT9	AN59	AW64	DQ48
SB_DQ[52]	AH11	AU59	BA62	DQ53
SB_DQ[53]	AR8	AU61	BC64	DQ50
SB_DQ[54]	AJ12	AN58	AU64	DQ55
SB_DQ[55]	AH12	AR58	AW62	DQ54
SB_DQ[56]	AT11	AK58	AR64	DQ56
SB_DQ[57]	AN14	AL58	AT65	DQ58
SB_DQ[58]	AR14	AG58	AL64	DQ61
SB_DQ[59]	AT14	AG59	AM65	DQ62
SB_DQ[60]	AT12	AM60	AR62	DQ57
SB_DQ[61]	AN15	AL59	AT63	DQ59
SB_DQ[62]	AR15	AF61	AL62	DQ63
SB_DQ[63]	AT15	AH60	AM63	DQ60

§ §