

Single 16 and 8, Differential 8-Channel and 4-Channel CMOS Analog MUXs with Active Overvoltage Protection

The HI-546, HI-547, HI-548 and HI-549 are analog multiplexers with active overvoltage protection and guaranteed r_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers.

Analog inputs can withstand constant $70V_{P-P}$ levels with $\pm 15V$ supplies. Digital inputs will also sustain continuous faults up to 4V greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur. Each input presents $1k\Omega$ of resistance under this condition. These features make the HI-546, HI-547, HI-548 and HI-549 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. All devices are fabricated with 44V Dielectrically Isolated CMOS technology. The HI-546 is a single 16-Channel, the HI-547 is an 8-Channel differential, the HI-548 is a single 8-Channel and the HI-549 is a 4-Channel differential device. If input overvoltage protection is not needed the HI-506/507/508/509 multiplexers are recommended. For further information see Application Notes AN520 and AN521.

For MIL-STD-883 compliant parts, request the HI-546/883, HI-547/883, HI-548/883 and HI-549/883 datasheets.

Features

- Analog Overvoltage Protection. $70V_{P-P}$
- No Channel Interaction During Overvoltage
- Guaranteed r_{ON} Matching
- Maximum Power Supply 44V
- Break-Before-Make Switching
- Analog Signal Range $\pm 15V$
- Access Time (Typical) 500ns
- Standby Power (Typical) 7.5mW
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Data Acquisition
- Industrial Controls
- Telemetry

Ordering Information

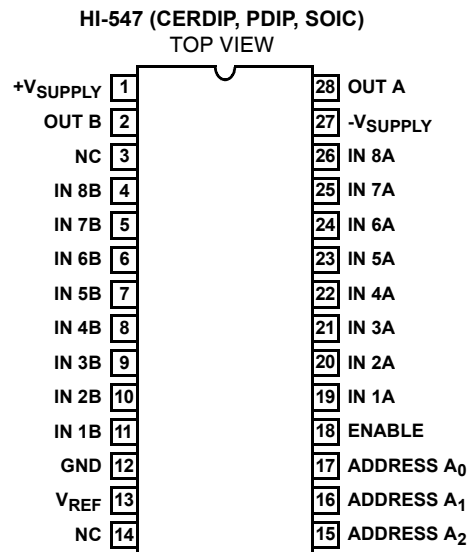
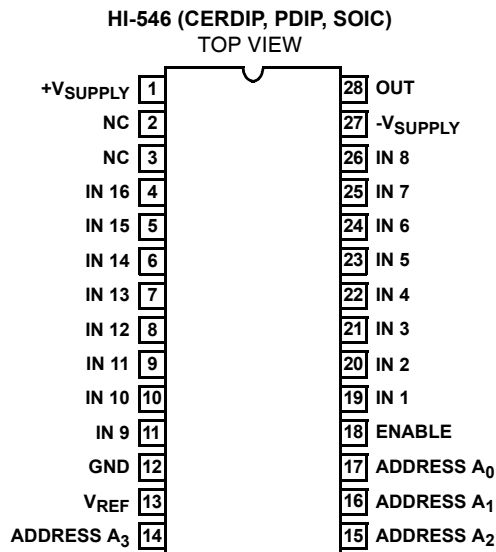
| PART NUMBER | PART MARKING | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|--|--------------|------------------|------------------------|-------------|
| HI1-0546-2 | HI1-546-2 | -55 to 125 | 28 Ld CERDIP | F28.6 |
| HI3-0546-5Z (Note) (No longer available, recommended replacement: HI9P0546-9Z, HI4P0546-5Z) | HI3-546-5Z | 0 to 75 | 28 Ld PDIP* (Pb-free) | E28.6 |
| HI4P0546-5Z (Note) | HI4P546-5Z | 0 to 75 | 28 Ld PLCC (Pb-free) | N28.45 |
| HI9P0546-9Z** (Note) | HI9P546-9Z | -40 to 85 | 28 Ld SOIC (Pb-free) | M28.3 |
| HI3-0547-5Z (Note) | HI3-0547-5Z | 0 to 75 | 28 Ld PDIP* (Pb-free) | E28.6 |
| HI4P0547-5Z (Note) (No longer available, recommended replacement: HI3-0547-5Z) | HI4P547-5Z | 0 to 75 | 28 Ld PLCC (Pb-free) | N28.45 |
| HI9P0547-9Z** (Note) | HI9P547-9Z | -40 to 85 | 28 Ld SOIC (Pb-free) | M28.3 |
| HI1-0548-2 | HI1-548-2 | -55 to 125 | 16 Ld CERDIP | F16.3 |
| HI3-0548-5Z (Note) | HI3-548-5Z | 0 to 75 | 16 LEAD PDIP (Pb-Free) | E16.3 |
| HI9P0548-5Z** (Note) | HI9P548-5Z | 0 to 75 | 16 Ld SOIC (Pb-free) | M16.15 |
| HI9P0548-9Z (Note) | HI9P548-9Z | -40 to 85 | 16 Ld SOIC (Pb-free) | M16.15 |
| HI1-0549-2 | HI1-549-2 | -55 to 125 | 16 Ld CERDIP | F16.3 |
| HI3-0549-5 (No longer available or supported) | HI3-549-5 | 0 to 75 | 16 Ld PDIP | E16.3 |
| HI3-0549-5Z (Note) | HI3-549-5Z | 0 to 75 | 16 Ld PDIP (Pb-Free) | E16.3 |
| HI4P0549-5Z (Note) (No longer available or supported) | HI4P549-5Z | 0 to 75 | 20 Ld PLCC (Pb-free) | N20.35 |
| HI9P0549-9Z (Note) | HI9P549-9Z | -40 to 85 | 16 Ld SOIC (Pb-free) | M16.15 |

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

**Add "96" suffix for tape and reel.

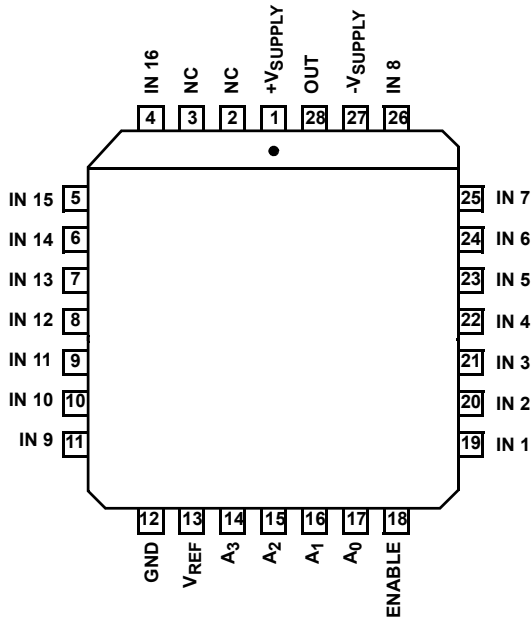
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

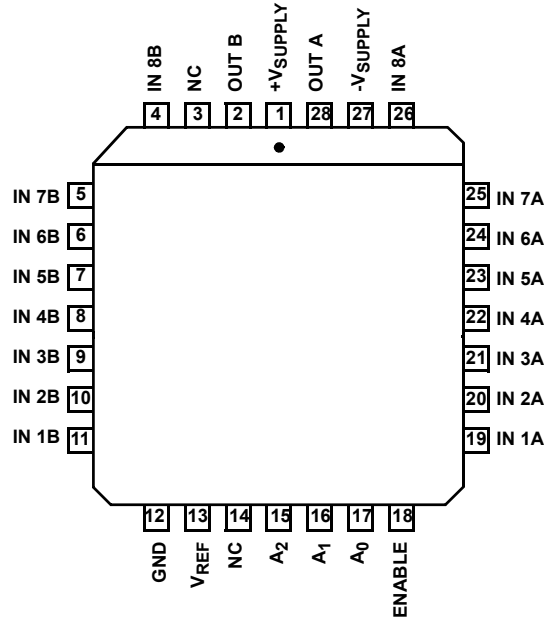


Pinouts (Continued)

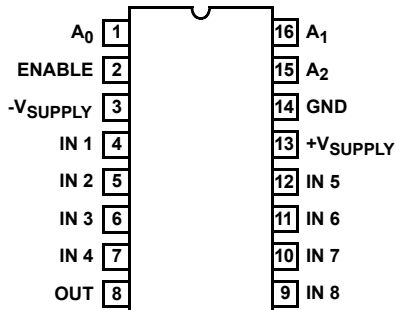
HI-546 (PLCC)
TOP VIEW



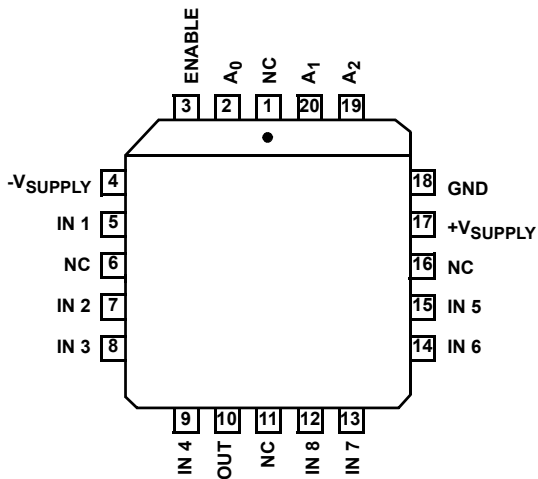
HI-547 (PLCC)
TOP VIEW



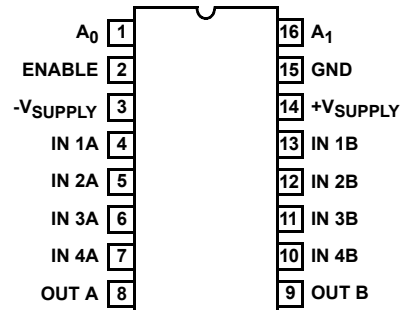
HI-548 (CERDIP, PDIP, SOIC)
TOP VIEW



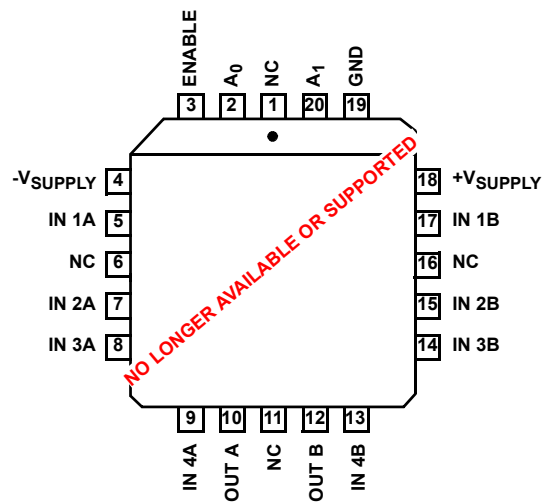
HI-548 (PLCC)
TOP VIEW



HI-549 (CERDIP, PDIP, SOIC)
TOP VIEW



HI-549 (PLCC)
TOP VIEW



HI-546, HI-547, HI-548, HI-549

TRUTH TABLE HI-546

| A ₃ | A ₂ | A ₁ | A ₀ | EN | "ON" CHANNEL |
|----------------|----------------|----------------|----------------|----|--------------|
| X | X | X | X | L | None |
| L | L | L | L | H | 1 |
| L | L | L | H | H | 2 |
| L | L | H | L | H | 3 |
| L | L | H | H | H | 4 |
| L | H | L | L | H | 5 |
| L | H | L | H | H | 6 |
| L | H | H | L | H | 7 |
| L | H | H | H | H | 8 |
| H | L | L | L | H | 9 |
| H | L | L | H | H | 10 |
| H | L | H | L | H | 11 |
| H | L | H | H | H | 12 |
| H | H | L | L | H | 13 |
| H | H | L | H | H | 14 |
| H | H | H | L | H | 15 |
| H | H | H | H | H | 16 |

TRUTH TABLE HI-547 (Continued)

| A ₂ | A ₁ | A ₀ | EN | "ON" CHANNEL PAIR |
|----------------|----------------|----------------|----|-------------------|
| H | L | L | H | 5 |
| H | L | H | H | 6 |
| H | H | L | H | 7 |
| H | H | H | H | 8 |

TRUTH TABLE HI-548

| A ₂ | A ₁ | A ₀ | EN | "ON" CHANNEL |
|----------------|----------------|----------------|----|--------------|
| X | X | X | L | None |
| L | L | L | H | 1 |
| L | L | H | H | 2 |
| L | H | L | H | 3 |
| L | H | H | H | 4 |
| H | L | L | H | 5 |
| H | L | H | H | 6 |
| H | H | L | H | 7 |
| H | H | H | H | 8 |

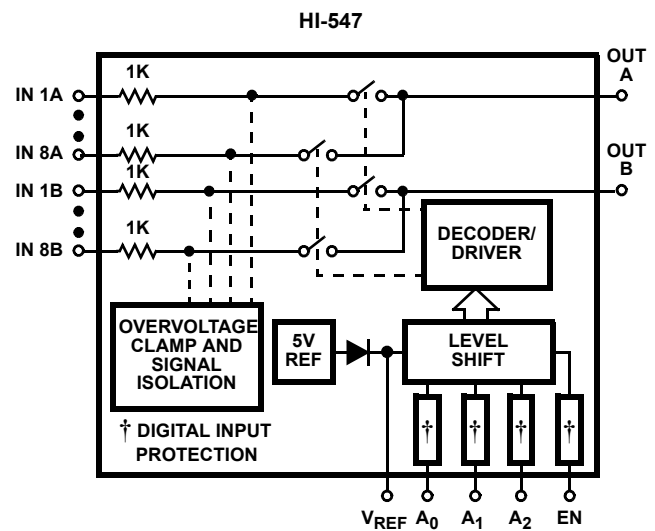
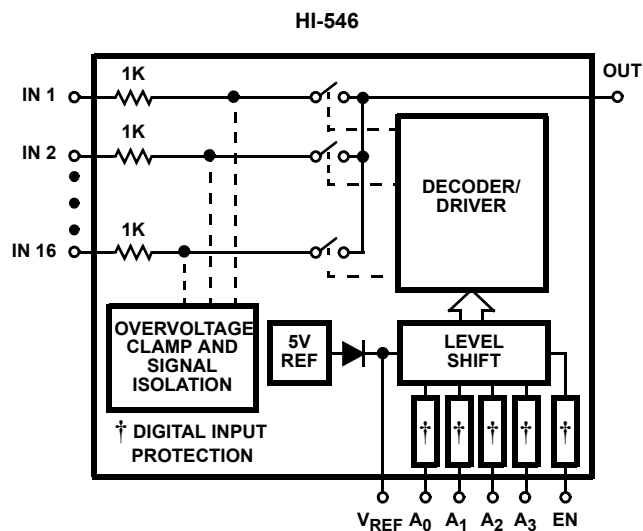
TRUTH TABLE HI-547

| A ₂ | A ₁ | A ₀ | EN | "ON" CHANNEL PAIR |
|----------------|----------------|----------------|----|-------------------|
| X | X | X | L | None |
| L | L | L | H | 1 |
| L | L | H | H | 2 |
| L | H | L | H | 3 |
| L | H | H | H | 4 |

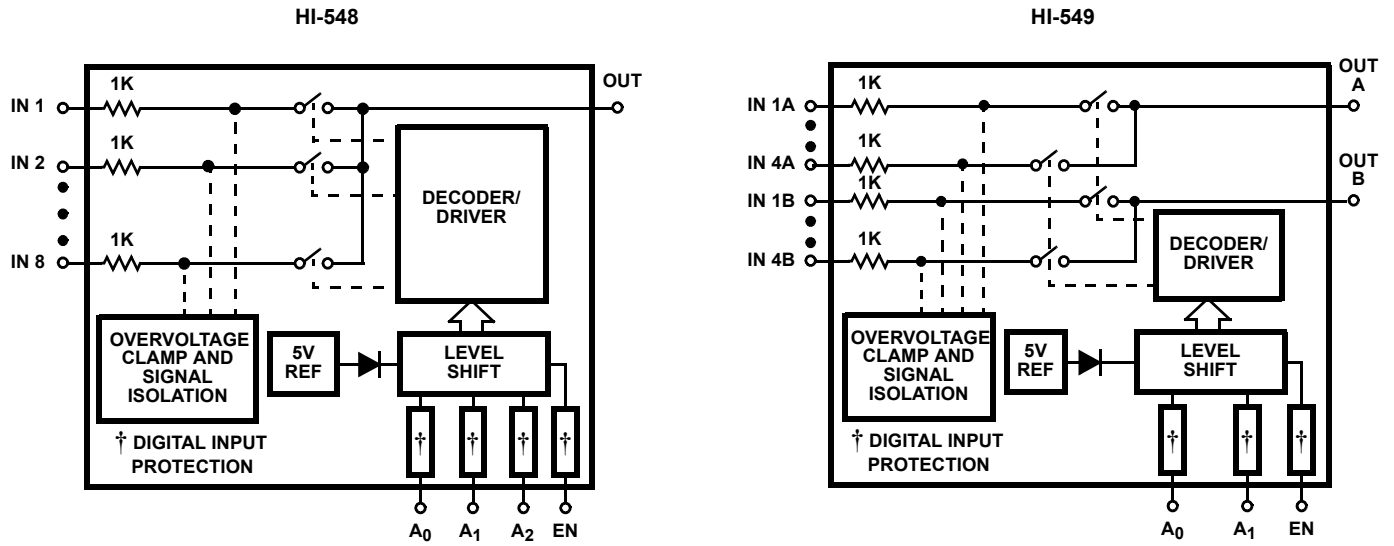
TRUTH TABLE HI-549

| A ₁ | A ₀ | EN | "ON" CHANNEL PAIR |
|----------------|----------------|----|-------------------|
| X | X | L | None |
| L | L | H | 1 |
| L | H | H | 2 |
| H | L | H | 3 |
| H | H | H | 4 |

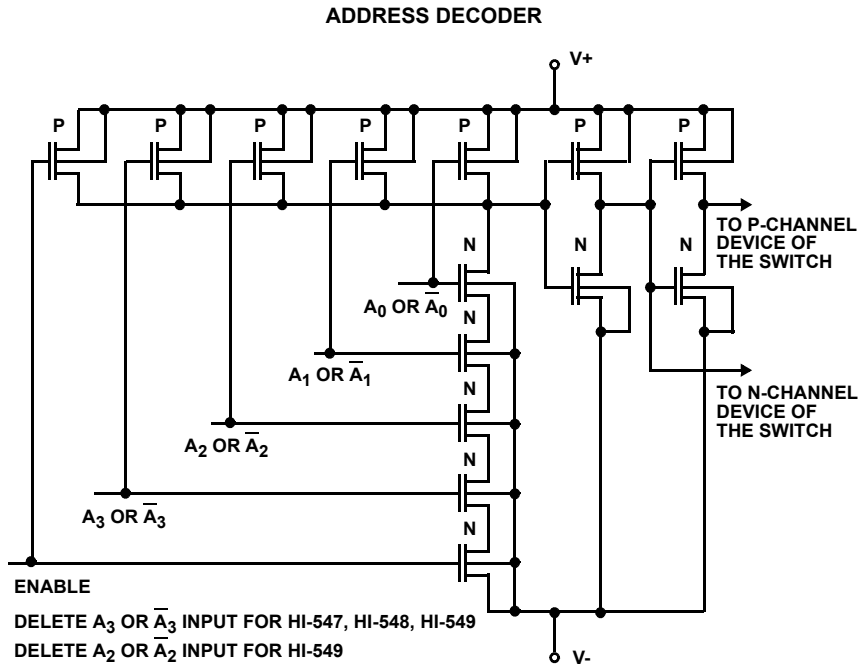
Functional Diagrams



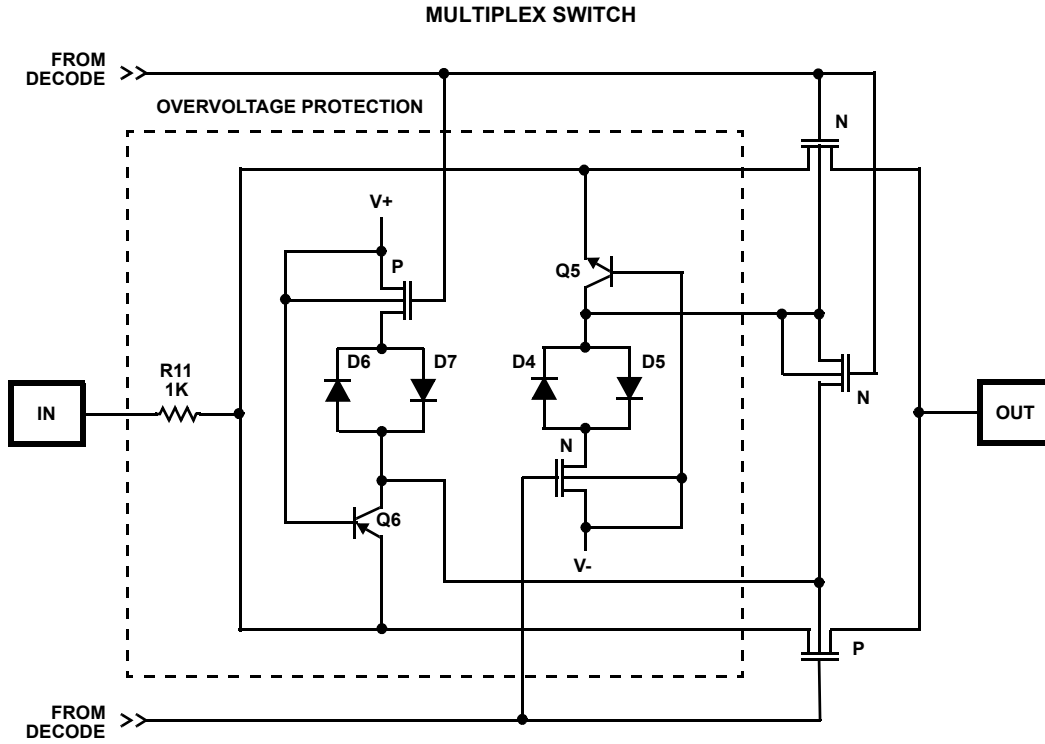
Functional Diagrams (Continued)



Schematic Diagrams

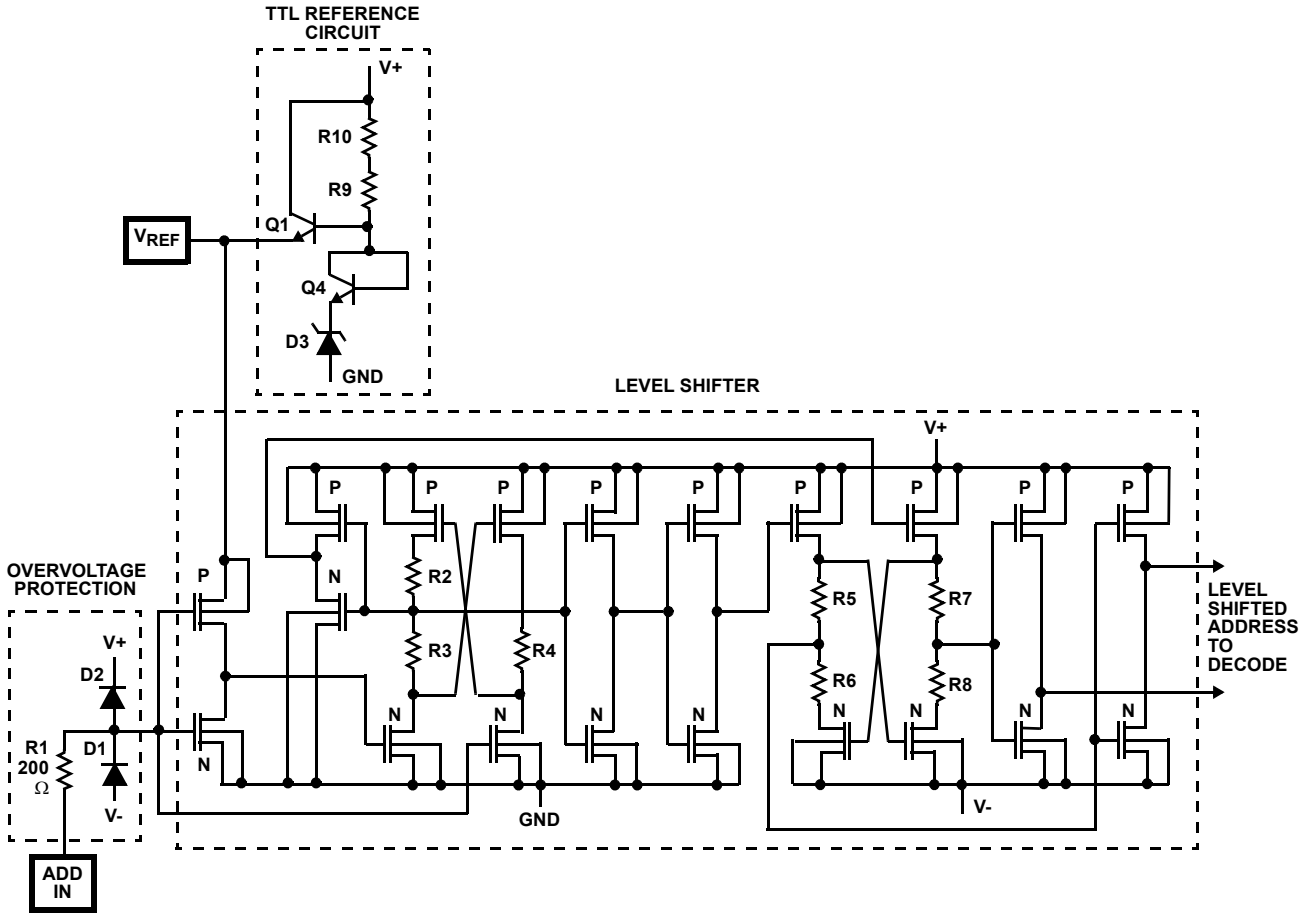


Schematic Diagrams (Continued)



Schematic Diagrams (Continued)

ADDRESS INPUT BUFFER AND LEVEL SHIFTER



HI-546, HI-547, HI-548, HI-549

Absolute Maximum Ratings

| | |
|---|---|
| V+ to V- | +44V |
| V+ to GND | +22V |
| V- to GND | -25V |
| Digital Input Voltage (V _{EN} , V _A) | (V-) -4V to (V+) +4V |
| Analog Signal (V _{IN} , V _{OUT}) | (V-) -20V to (V+) +20V or 20mA, Whichever Occurs First |
| Continuous Current, IN or OUT | 20mA |
| Peak Current, IN or OUT (Pulsed 1ms, 10% Duty Cycle Max) .. | 40mA |

Operating Conditions

| | |
|----------------------------|----------------|
| Temperature Ranges | |
| HI-546/548/549-2 | -55°C to 125°C |
| HI-546/547/548/549-5 | 0°C to 75°C |
| HI-546/547/548/549-9 | -40°C to 85°C |

Thermal Information

| | | |
|--------------------------------------|----------------------|----------------------|
| Thermal Resistance (Typical, Note 1) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
| 16 Ld CERDIP Package | 85 | 32 |
| 28 Ld CERDIP Package | 55 | 18 |
| 28 Ld PDIP Package* | 60 | N/A |
| 16 Ld PDIP Package | 90 | N/A |
| 28 Ld PLCC Package | 70 | N/A |
| 20 Ld PLCC Package | 80 | N/A |
| 28 Ld SOIC Package | 75 | N/A |
| 16 Ld SOIC Package | 105 | N/A |

| | |
|--|--|
| Maximum Junction Temperature | |
| Ceramic Packages | 175°C |
| Plastic Packages | 150°C |
| Maximum Storage Temperature Range | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) | 300°C (PLCC, SOIC - Lead Tips Only) |

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = 4V; V_{AL} (Logic Level Low) = 0.8V; Unless Otherwise Specified. For Test Conditions, Consult Test Circuits Section

| PARAMETER | TEST CONDITIONS | TEMP (°C) | -2 | | | -5, -9 | | | UNITS |
|--|------------------------|-----------|-----|-----|------|--------|-----|------|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SWITCHING CHARACTERISTICS | | | | | | | | | |
| Access Time, t _A | | 25 | - | 0.5 | - | - | 0.5 | - | μs |
| | | Full | - | - | 1.0 | - | - | 1.0 | μs |
| Break-Before Make Delay, t _{OPEN} | | 25 | 25 | 80 | - | 25 | 80 | - | ns |
| Enable Delay (ON), t _{ON(EN)} | | 25 | - | 300 | 500 | - | 300 | - | ns |
| | | Full | - | - | 1000 | - | - | 1000 | ns |
| Enable Delay (OFF), t _{OFF(EN)} | | 25 | - | 300 | 500 | - | 300 | - | ns |
| | | Full | - | - | 1000 | - | - | 1000 | ns |
| Settling Time | To 0.1% | 25 | - | 1.2 | - | - | 1.2 | - | μs |
| | To 0.01% | 25 | - | 3.5 | - | - | 3.5 | - | μs |
| Off Isolation | Note 6 | 25 | 50 | 68 | - | 50 | 68 | - | dB |
| Channel Input Capacitance, C _{S(OFF)} | | 25 | - | 10 | - | - | 10 | - | pF |
| Channel Output Capacitance C _{D(OFF)} | HI-546 | 25 | - | 52 | - | - | 52 | - | pF |
| | HI-547 | 25 | - | 30 | - | - | 30 | - | pF |
| | HI-548 | 25 | - | 25 | - | - | 25 | - | pF |
| | HI-549 | 25 | - | 12 | - | - | 12 | - | pF |
| Input to Output Capacitance, C _{D(OFF)} | | 25 | - | 0.1 | - | - | 0.1 | - | pF |
| DIGITAL INPUT CHARACTERISTICS | | | | | | | | | |
| Input Low Threshold, TTL Drive, V _{AL} | | Full | - | - | 0.8 | - | - | 0.8 | V |
| Input High Threshold, V _{AH} (Note 8) | | Full | 4.0 | - | - | 4.0 | - | - | V |
| MOS Drive, V _{AL} (HI-546/547 Only) | V _{REF} = 10V | 25 | - | - | 0.8 | - | - | 0.8 | V |

HI-546, HI-547, HI-548, HI-549

Electrical Specifications Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = 4V; V_{AL} (Logic Level Low) = 0.8V; Unless Otherwise Specified. For Test Conditions, Consult Test Circuits Section **(Continued)**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | -2 | | | -5, -9 | | | UNITS | |
|---|------------------------|-----------|------|------|-----|--------|------|-----|-------|----|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| MOS Drive, V _{AH} (HI-546/547 Only) | V _{REF} = 10V | 25 | 6.0 | - | - | 6.0 | - | - | V | |
| Input Leakage Current (High or Low), I _A | Note 5 | Full | - | - | 1.0 | - | - | 1.0 | μA | |
| ANALOG CHANNEL CHARACTERISTICS | | | | | | | | | | |
| Analog Signal Range, V _{IN} | | Full | -15 | - | +15 | -15 | - | +15 | V | |
| On Resistance, r _{ON} | Note 2 | 25 | - | 1.2 | 1.5 | - | 1.5 | 1.8 | kΩ | |
| | | Full | - | 1.5 | 1.8 | - | 1.8 | 2.0 | kΩ | |
| Δr _{ON} , (Any Two Channels) | | 25 | - | - | 7.0 | - | - | 7.0 | % | |
| Off Input Leakage Current, I _{S(OFF)} | Note 3 | 25 | - | 0.03 | - | - | 0.03 | - | nA | |
| | | Full | - | - | 50 | - | - | 50 | nA | |
| Off Output Leakage Current, I _{D(OFF)} | Note 3 | 25 | - | 0.1 | - | - | 0.1 | - | nA | |
| | | HI-546 | Full | - | - | 300 | - | - | 300 | nA |
| | | HI-547 | Full | - | - | 200 | - | - | 200 | nA |
| | | HI-548 | Full | - | - | 200 | - | - | 200 | nA |
| | | HI-549 | Full | - | - | 100 | - | - | 100 | nA |
| I _{D(OFF)} With Input Overvoltage Applied | Note 4 | 25 | - | 4.0 | - | - | 4.0 | - | nA | |
| | | Full | - | - | 2.0 | - | - | - | μA | |
| On Channel Leakage Current, I _{D(ON)} | Note 3 | 25 | - | 0.1 | - | - | 0.1 | - | nA | |
| | | HI-546 | Full | - | - | 300 | - | - | 300 | nA |
| | | HI-547 | Full | - | - | 200 | - | - | 200 | nA |
| | | HI-548 | Full | - | - | 200 | - | - | 200 | nA |
| | | HI-549 | Full | - | - | 100 | - | - | 100 | nA |
| Differential Off Output Leakage Current I _{DIFF} (HI-547, HI-549 Only) | | Full | - | - | 50 | - | - | 50 | nA | |
| POWER SUPPLY CHARACTERISTICS | | | | | | | | | | |
| Power Dissipation, P _D | | Full | - | 7.5 | - | - | 7.5 | - | mW | |
| Current, I ₊ | Note 7 | Full | - | 0.5 | 2.0 | - | 0.5 | 2.0 | mA | |
| Current, I ₋ | Note 7 | Full | - | 0.02 | 1.0 | - | 0.02 | 1.0 | mA | |

NOTES:

2. V_{OUT} = ±10V, I_{OUT} = ±100μA.
3. 10nA is the practical lower limit for high speed measurement in the production test environments.
4. Analog Overvoltage = ±33V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
6. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = 7V_{RMS}, f = 100kHz.
7. V_{EN}, V_A = 0V or 4V.
8. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5V supply are recommended.

Test Circuits and Waveforms $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = 4\text{V}$, $V_{\text{AL}} = 0.8\text{V}$, $V_{\text{REF}} = \text{Open}$, Unless Otherwise Specified

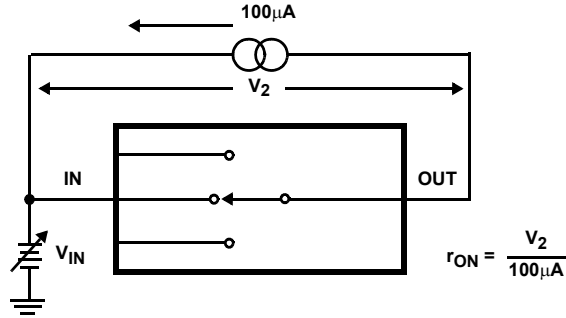


FIGURE 1A. ON RESISTANCE TEST CIRCUIT

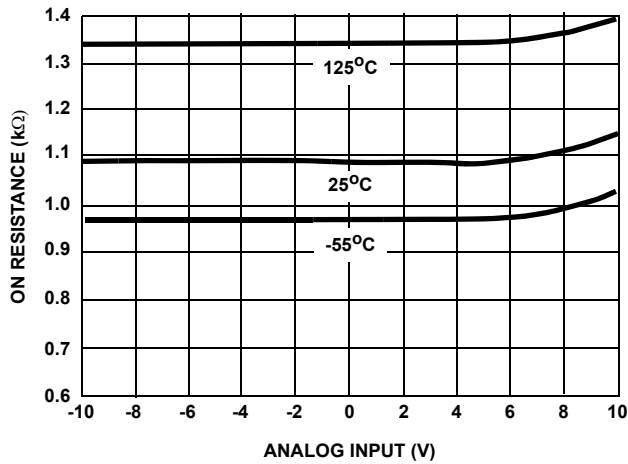


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE

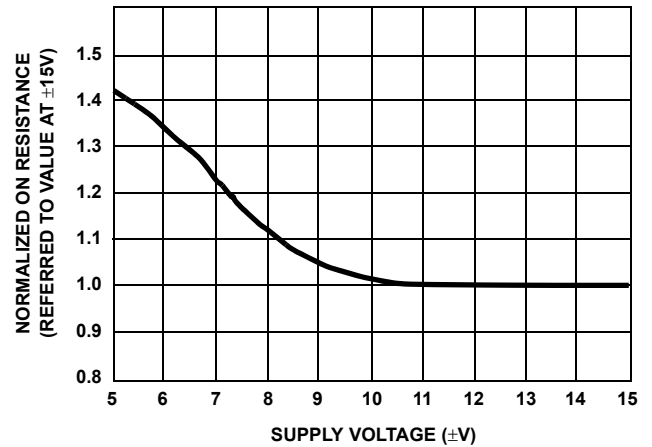


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

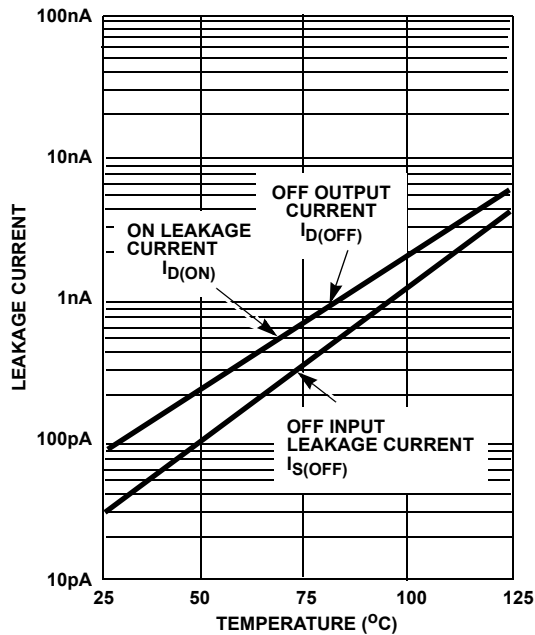


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

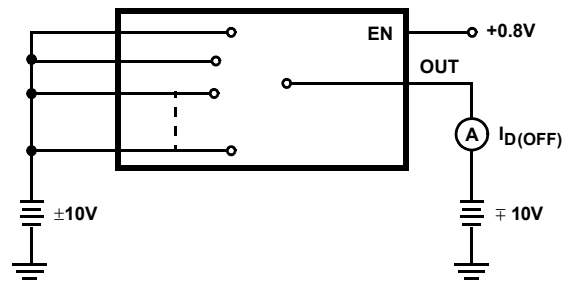


FIGURE 2B. $I_{\text{D(OFF)}}$ TEST CIRCUIT (NOTE 9)

Test Circuits and Waveforms $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = 4\text{V}$, $V_{\text{AL}} = 0.8\text{V}$, $V_{\text{REF}} = \text{Open}$, Unless Otherwise Specified

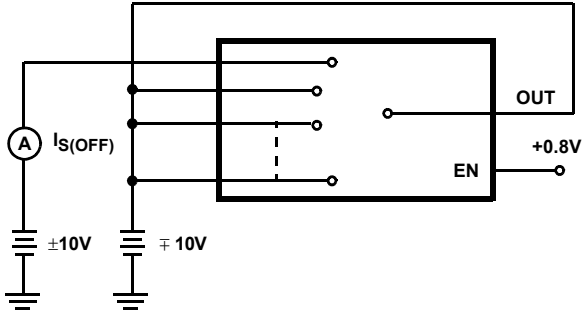


FIGURE 2C. $I_{S(\text{OFF})}$ TEST CIRCUIT (NOTE 9)

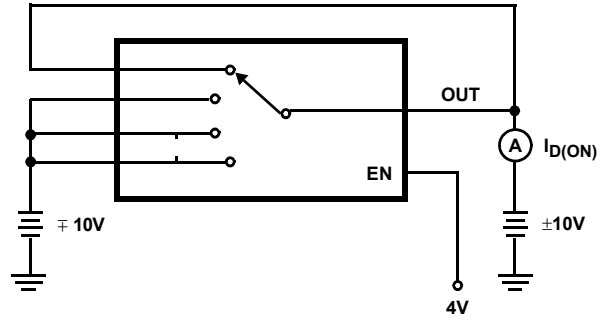


FIGURE 2D. $I_{D(\text{ON})}$ TEST CIRCUIT (NOTE 9)

NOTE:

- 9. Two measurements per channel: $\pm 10\text{V}$ and $\mp 10\text{V}$. (Two measurements per device for $I_{D(\text{OFF})}$: $\pm 10\text{V}$ and $\mp 10\text{V}$.)

FIGURE 2. LEAKAGE CURRENTS

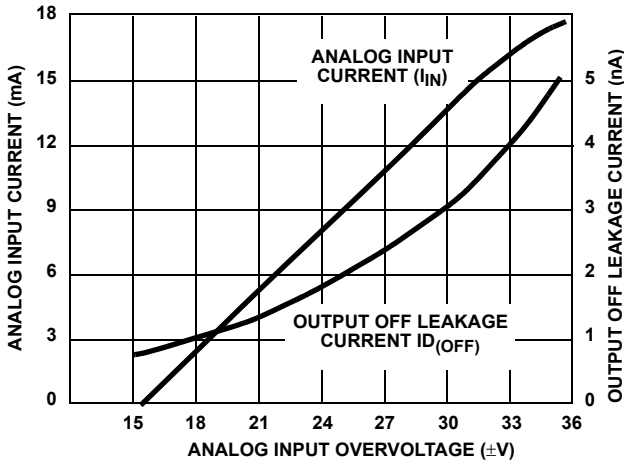


FIGURE 3A. ANALOG INPUT CURRENT AND OUTPUT OFF LEAKAGE CURRENT vs ANALOG INPUT OVER-VOLTAGE

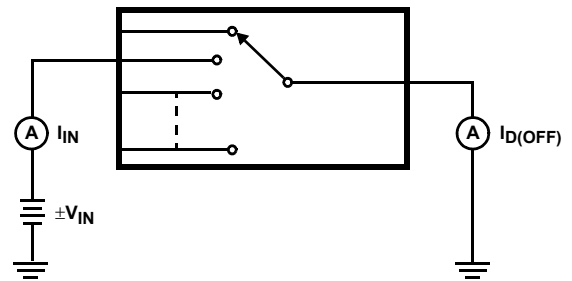


FIGURE 3B. TEST CIRCUIT

FIGURE 3. ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

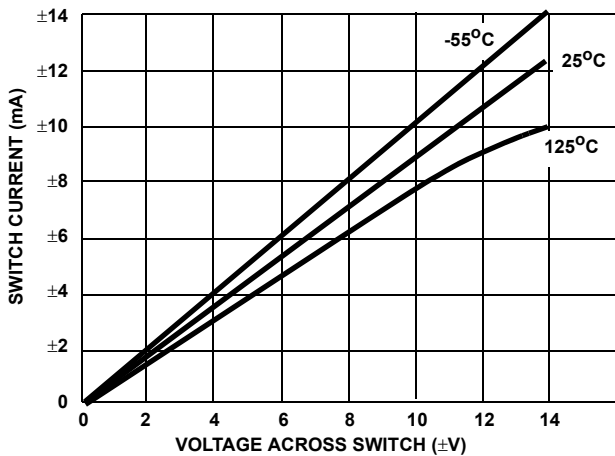


FIGURE 4A. ON CHANNEL CURRENT vs VOLTAGE

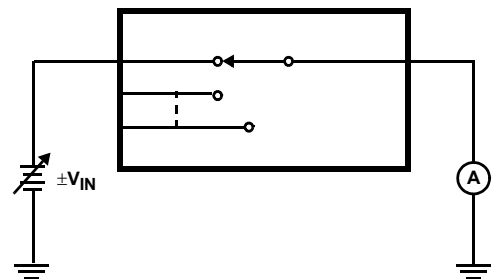


FIGURE 4B. TEST CIRCUIT

FIGURE 4. ON CHANNEL CURRENT

Test Circuits and Waveforms $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = 4\text{V}$, $V_{\text{AL}} = 0.8\text{V}$, $V_{\text{REF}} = \text{Open}$, Unless Otherwise Specified

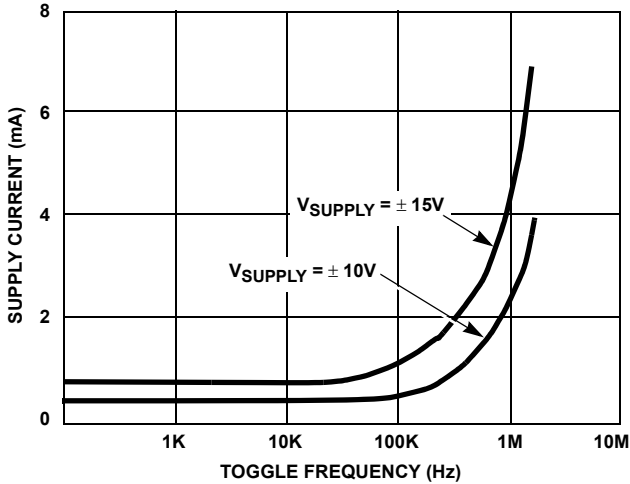
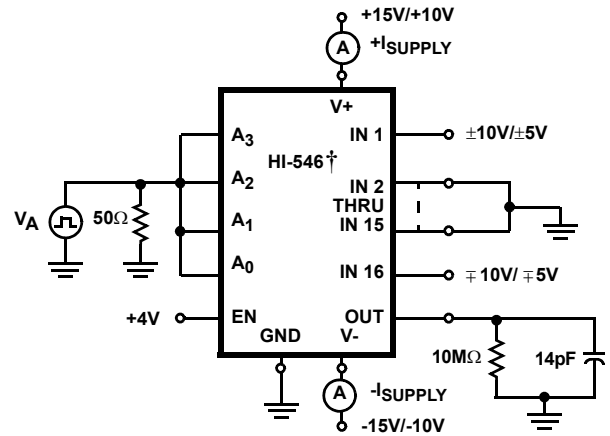


FIGURE 5A. SUPPLY CURRENT vs TOGGLE FREQUENCY

FIGURE 5. DYNAMIC SUPPLY CURRENT



† Similar connection for HI-547/HI-548/HI-549.

FIGURE 5B. TEST CIRCUIT

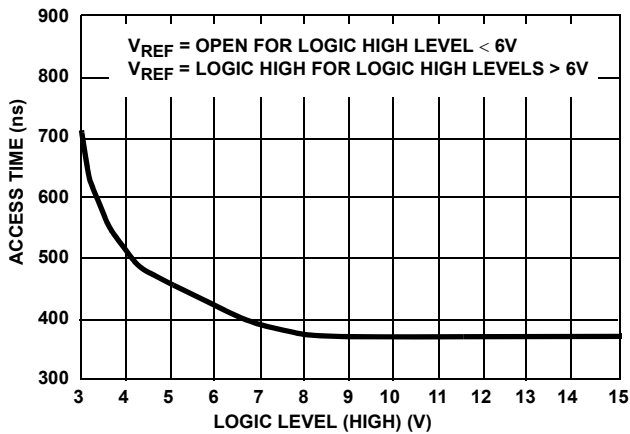
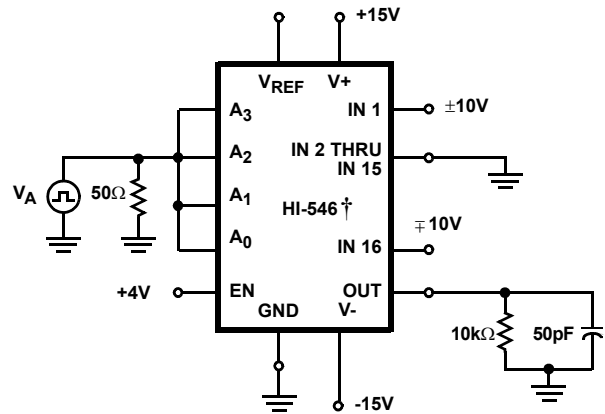


FIGURE 6A. ACCESS TIME vs LOGIC LEVEL (HIGH)



† Similar connection for HI-547/HI-548/HI-549.

FIGURE 6B. TEST CIRCUIT

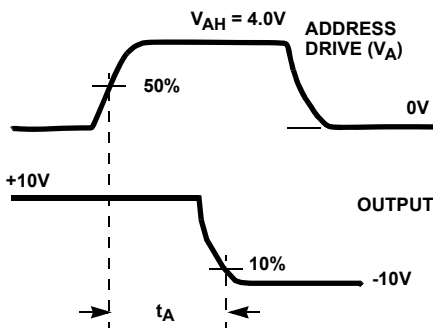


FIGURE 6C. MEASUREMENT POINTS

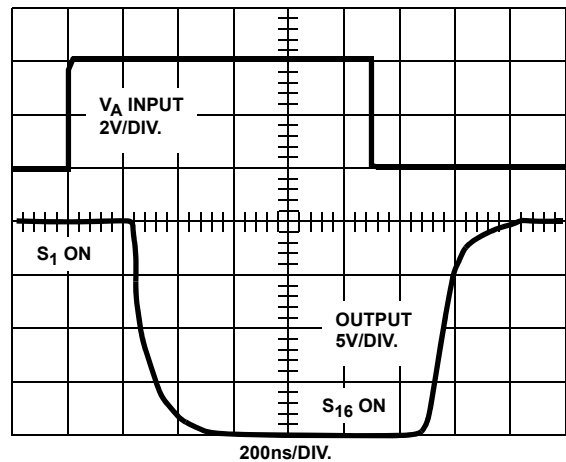
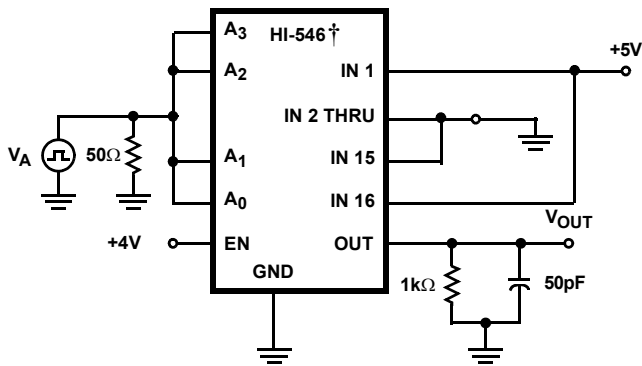


FIGURE 6D. WAVEFORMS

FIGURE 6. ACCESS TIME

Test Circuits and Waveforms $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = 4\text{V}$, $V_{\text{AL}} = 0.8\text{V}$, $V_{\text{REF}} = \text{Open}$, Unless Otherwise Specified



† Similar connection for HI-547/HI-548/HI-549

FIGURE 7A. TEST CIRCUIT

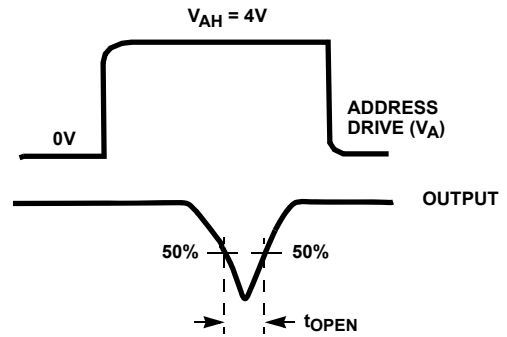


FIGURE 7B. MEASUREMENT POINTS

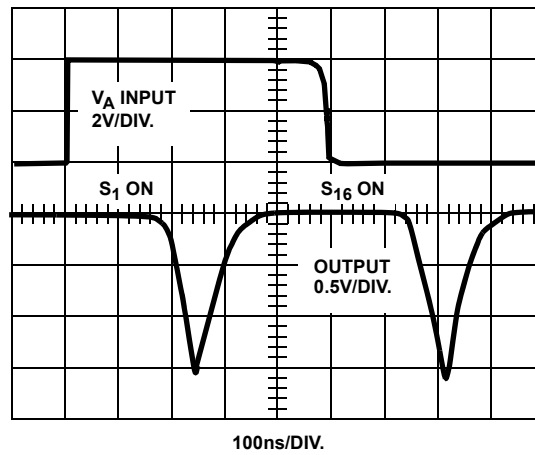
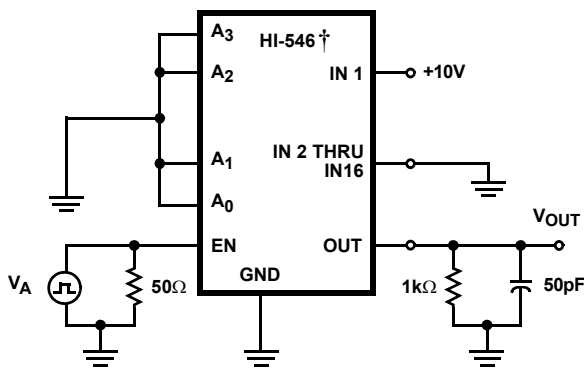


FIGURE 7C. WAVEFORMS

FIGURE 7. BREAK-BEFORE-MAKE DELAY



† Similar connection for HI-547/HI-548/HI-549

FIGURE 8A. TEST CIRCUIT

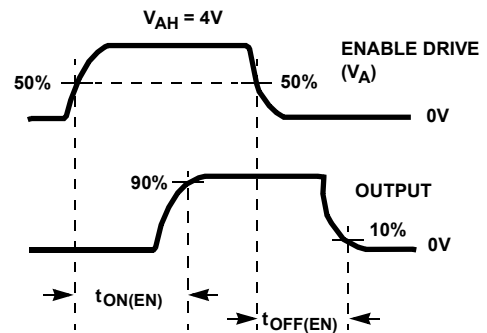


FIGURE 8B. MEASUREMENT POINTS

Test Circuits and Waveforms $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = 4\text{V}$, $V_{\text{AL}} = 0.8\text{V}$, $V_{\text{REF}} = \text{Open}$, Unless Otherwise Specified

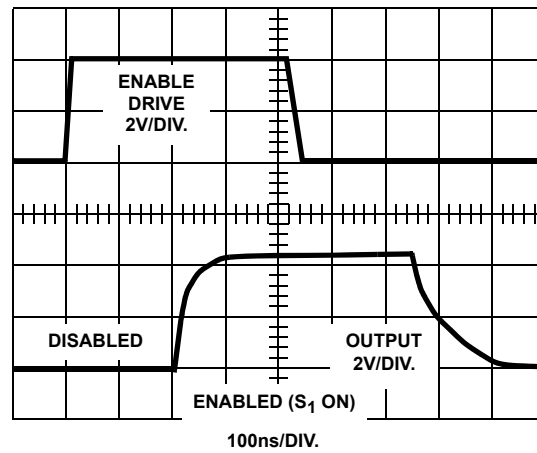


FIGURE 8C. WAVEFORMS
FIGURE 8. ENABLE DELAYS

Die Characteristics

DIE DIMENSIONS:

83.9 mils x 159 mils

METALLIZATION:

Type: CuAl

Thickness: $16k\text{\AA} \pm 2k\text{\AA}$

SUBSTRATE POTENTIAL (NOTE):

$-V_{\text{SUPPLY}}$

PASSIVATION:

Type: Nitride Over Silox

Nitride Thickness: $3.5k\text{\AA} \pm 1k\text{\AA}$

Silox Thickness: $12k\text{\AA} \pm 2k\text{\AA}$

WORST CASE CURRENT DENSITY:

$1.4 \times 10^5 \text{ A/cm}^2$

TRANSISTOR COUNT:

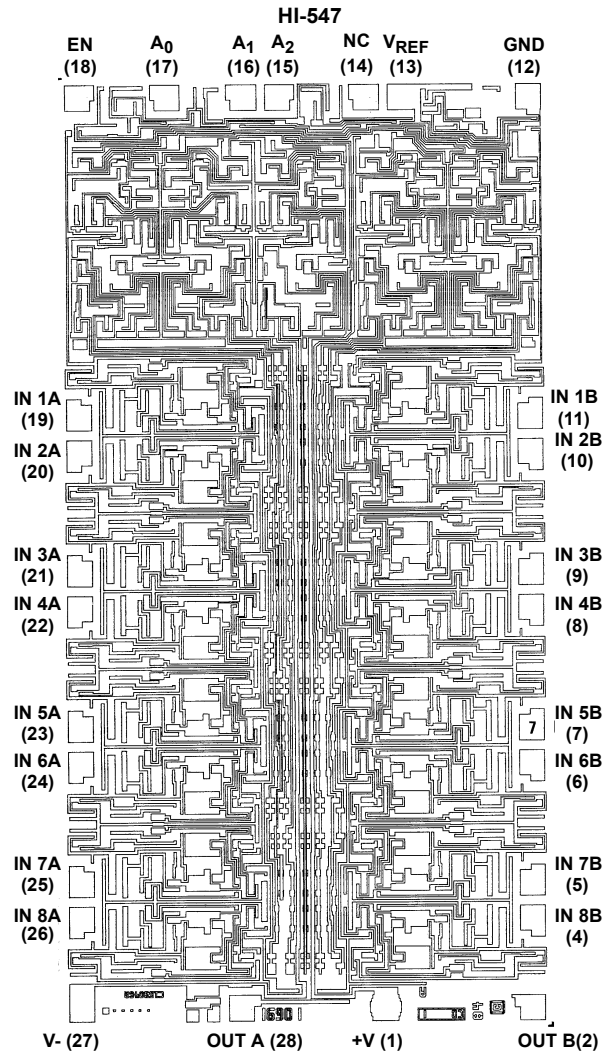
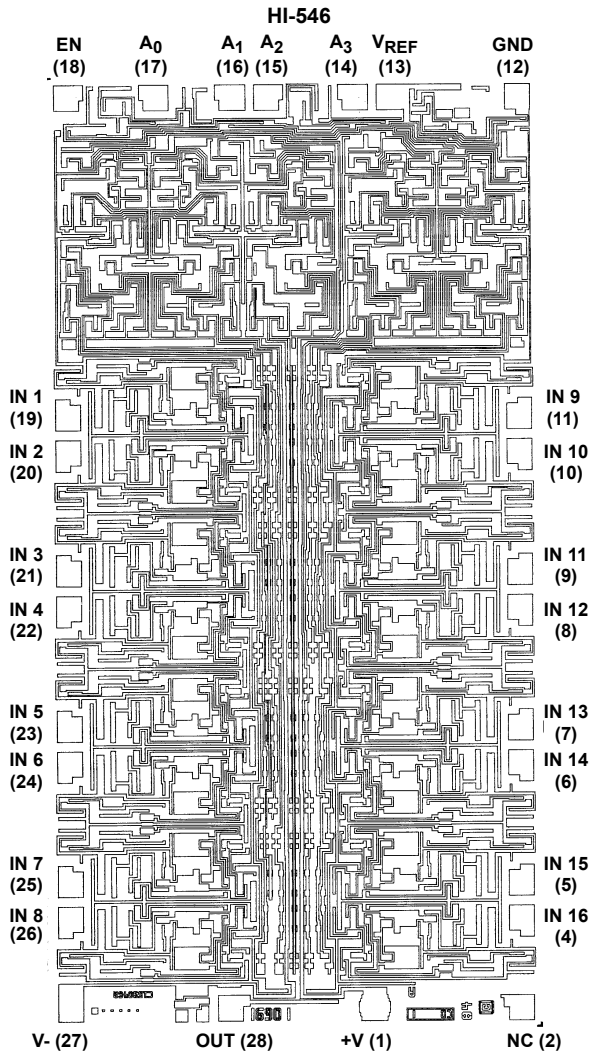
485

PROCESS:

CMOS-DI

NOTE: The substrate appears resistive to the $-V_{\text{SUPPLY}}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{\text{SUPPLY}}$ potential.

Metallization Mask Layouts



Die Characteristics

DIE DIMENSIONS:

83 mils x 108 mils

METALLIZATION:

Type: CuAl

Thickness: $16k\text{\AA} \pm 2k\text{\AA}$

SUBSTRATE POTENTIAL (NOTE):

$-V_{\text{SUPPLY}}$

PASSIVATION:

Type: Nitride Over Silox

Nitride Thickness: $3.5k\text{\AA} \pm 1k\text{\AA}$

Silox Thickness: $12k\text{\AA} \pm 2k\text{\AA}$

WORST CASE CURRENT DENSITY:

$1.4 \times 10^5 \text{ A/cm}$

TRANSISTOR COUNT:

253

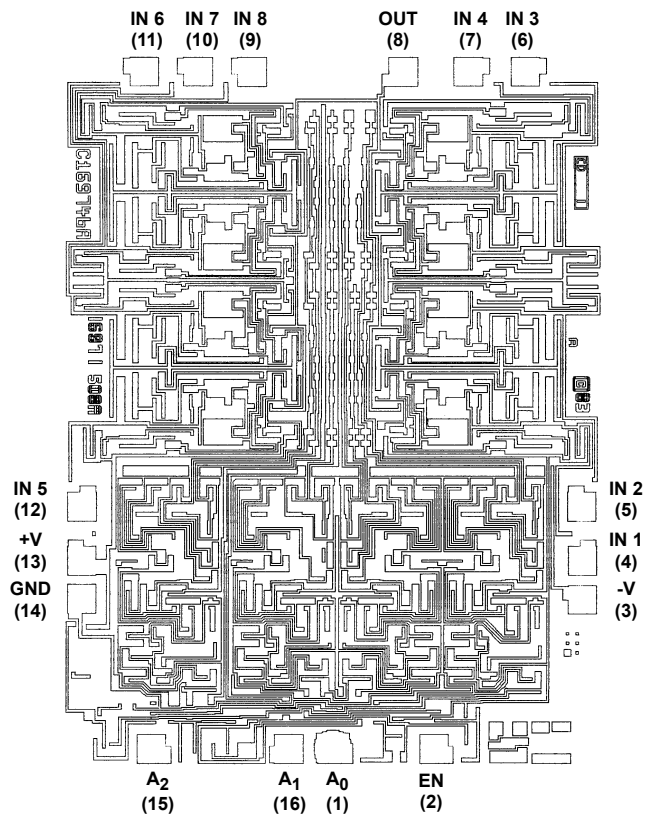
PROCESS:

CMOS-DI

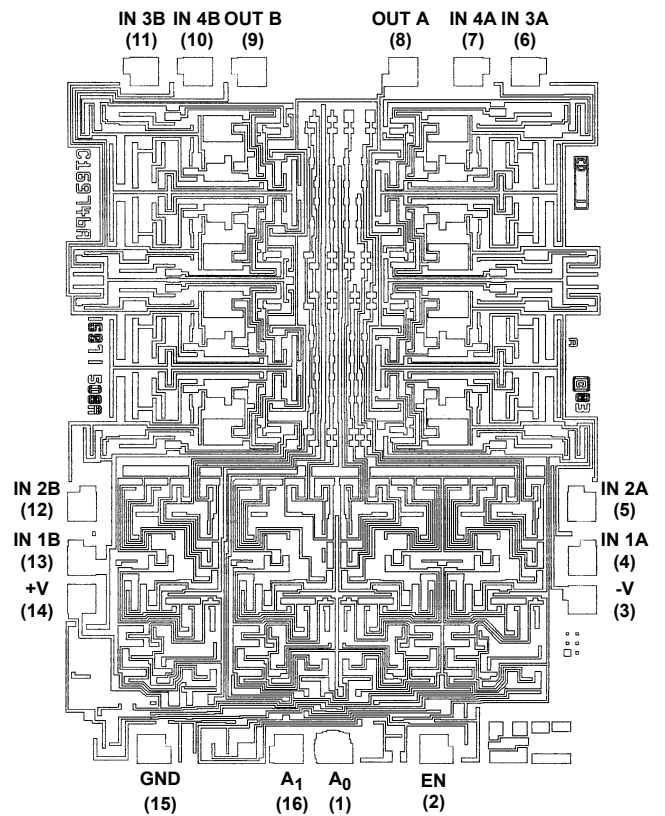
NOTE: The substrate appears resistive to the $-V_{\text{SUPPLY}}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{\text{SUPPLY}}$ potential.

Metallization Mask Layouts

HI-548



HI-549



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION | CHANGE |
|-----------------|----------|--|
| June 15, 2016 | FN3150.7 | Updated ordering information table on page 2. |
| October 1, 2015 | FN3150.6 | - Updated Ordering Information Table on page 2. - Added Revision History. - Added About Intersil Verbiage. - Updated POD M28.3 to latest revision changes are as follow: Added land pattern -Added Package Outline Drawing M16.15 to the latest revision. |

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You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

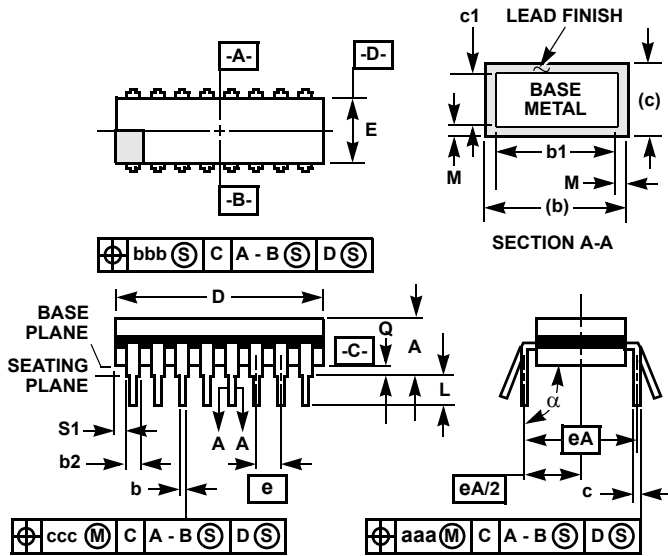
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Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



**F28.6 MIL-STD-1835 GDIP1-T28 (D-10, CONFIGURATION A)
28 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE**

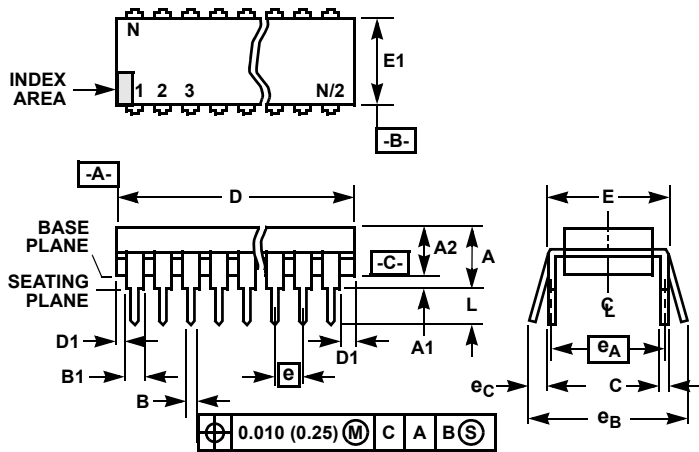
| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|--------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.232 | - | 5.92 | - |
| b | 0.014 | 0.026 | 0.36 | 0.66 | 2 |
| b1 | 0.014 | 0.023 | 0.36 | 0.58 | 3 |
| b2 | 0.045 | 0.065 | 1.14 | 1.65 | - |
| b3 | 0.023 | 0.045 | 0.58 | 1.14 | 4 |
| c | 0.008 | 0.018 | 0.20 | 0.46 | 2 |
| c1 | 0.008 | 0.015 | 0.20 | 0.38 | 3 |
| D | - | 1.490 | - | 37.85 | 5 |
| E | 0.500 | 0.610 | 12.70 | 15.49 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| eA | 0.600 BSC | | 15.24 BSC | | - |
| eA/2 | 0.300 BSC | | 7.62 BSC | | - |
| L | 0.125 | 0.200 | 3.18 | 5.08 | - |
| Q | 0.015 | 0.060 | 0.38 | 1.52 | 6 |
| S1 | 0.005 | - | 0.13 | - | 7 |
| α | 90° | 105° | 90° | 105° | - |
| aaa | - | 0.015 | - | 0.38 | - |
| bbb | - | 0.030 | - | 0.76 | - |
| ccc | - | 0.010 | - | 0.25 | - |
| M | - | 0.0015 | - | 0.038 | 2, 3 |
| N | 28 | | 28 | | 8 |

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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Dual-In-Line Plastic Packages (PDIP)



NOTES:

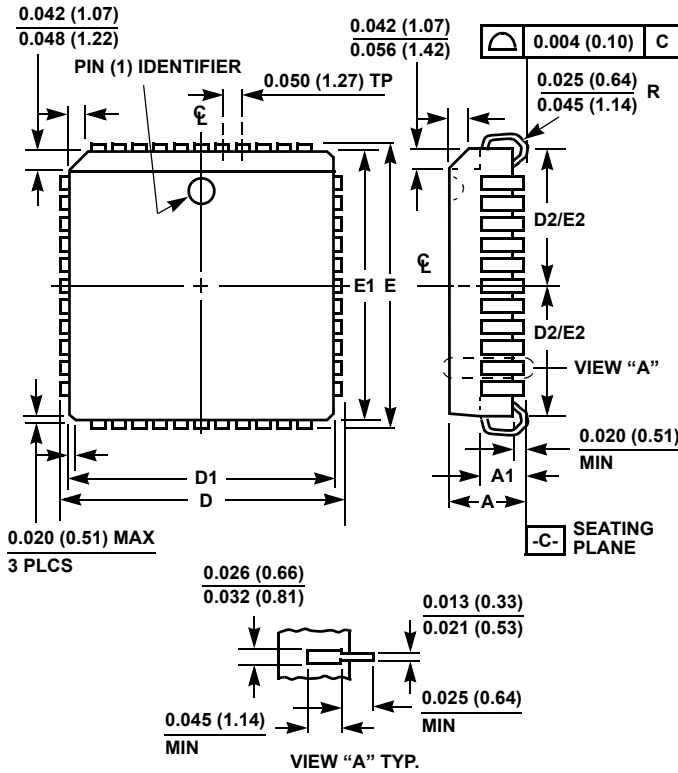
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum $-C-$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-011-AB ISSUE B)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|-------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.250 | - | 6.35 | 4 |
| A1 | 0.015 | - | 0.39 | - | 4 |
| A2 | 0.125 | 0.195 | 3.18 | 4.95 | - |
| B | 0.014 | 0.022 | 0.356 | 0.558 | - |
| B1 | 0.030 | 0.070 | 0.77 | 1.77 | 8 |
| C | 0.008 | 0.015 | 0.204 | 0.381 | - |
| D | 1.380 | 1.565 | 35.1 | 39.7 | 5 |
| D1 | 0.005 | - | 0.13 | - | 5 |
| E | 0.600 | 0.625 | 15.24 | 15.87 | 6 |
| E1 | 0.485 | 0.580 | 12.32 | 14.73 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| e_A | 0.600 BSC | | 15.24 BSC | | 6 |
| e_B | - | 0.700 | - | 17.78 | 7 |
| L | 0.115 | 0.200 | 2.93 | 5.08 | 4 |
| N | 28 | | 28 | | 9 |

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Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

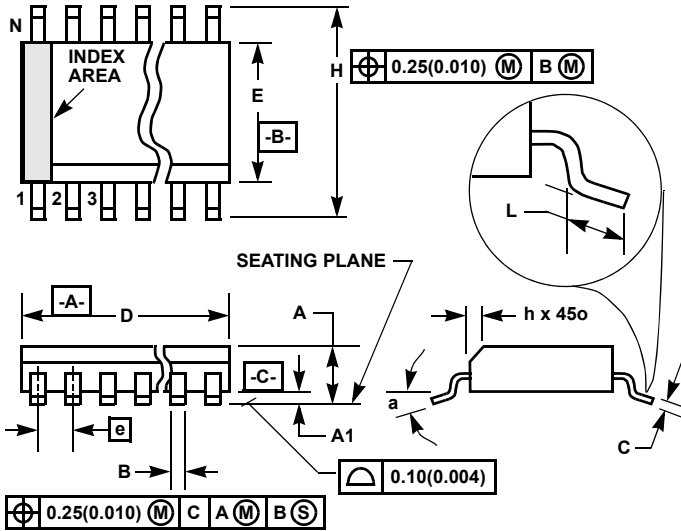
| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|--------|-------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.165 | 0.180 | 4.20 | 4.57 | - |
| A1 | 0.090 | 0.120 | 2.29 | 3.04 | - |
| D | 0.485 | 0.495 | 12.32 | 12.57 | - |
| D1 | 0.450 | 0.456 | 11.43 | 11.58 | 3 |
| D2 | 0.191 | 0.219 | 4.86 | 5.56 | 4, 5 |
| E | 0.485 | 0.495 | 12.32 | 12.57 | - |
| E1 | 0.450 | 0.456 | 11.43 | 11.58 | 3 |
| E2 | 0.191 | 0.219 | 4.86 | 5.56 | 4, 5 |
| N | 28 | | 28 | | 6 |

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NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

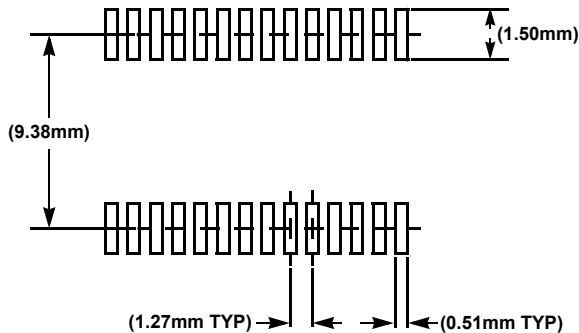
| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|----------|----------|--------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.0926 | 0.1043 | 2.35 | 2.65 | - |
| A1 | 0.0040 | 0.0118 | 0.10 | 0.30 | - |
| B | 0.013 | 0.0200 | 0.33 | 0.51 | 9 |
| C | 0.0091 | 0.0125 | 0.23 | 0.32 | - |
| D | 0.6969 | 0.7125 | 17.70 | 18.10 | 3 |
| E | 0.2914 | 0.2992 | 7.40 | 7.60 | 4 |
| e | 0.05 BSC | | 1.27 BSC | | - |
| H | 0.394 | 0.419 | 10.00 | 10.65 | - |
| h | 0.01 | 0.029 | 0.25 | 0.75 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 28 | | 28 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

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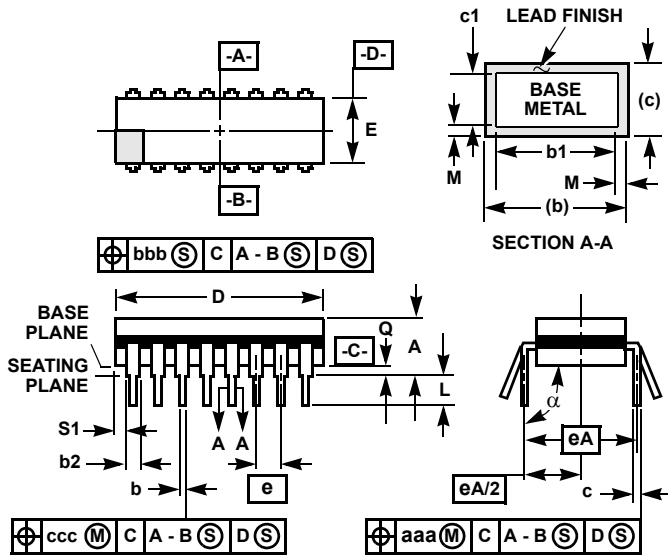
NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

TYPICAL RECOMMENDED LAND PATTERN



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

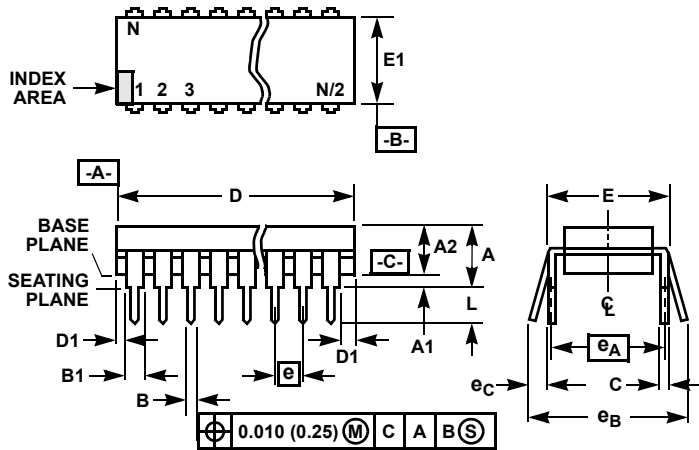
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

**F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|----------|-----------|--------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.200 | - | 5.08 | - |
| b | 0.014 | 0.026 | 0.36 | 0.66 | 2 |
| b1 | 0.014 | 0.023 | 0.36 | 0.58 | 3 |
| b2 | 0.045 | 0.065 | 1.14 | 1.65 | - |
| b3 | 0.023 | 0.045 | 0.58 | 1.14 | 4 |
| c | 0.008 | 0.018 | 0.20 | 0.46 | 2 |
| c1 | 0.008 | 0.015 | 0.20 | 0.38 | 3 |
| D | - | 0.840 | - | 21.34 | 5 |
| E | 0.220 | 0.310 | 5.59 | 7.87 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| eA | 0.300 BSC | | 7.62 BSC | | - |
| eA/2 | 0.150 BSC | | 3.81 BSC | | - |
| L | 0.125 | 0.200 | 3.18 | 5.08 | - |
| Q | 0.015 | 0.060 | 0.38 | 1.52 | 6 |
| S1 | 0.005 | - | 0.13 | - | 7 |
| α | 90° | 105° | 90° | 105° | - |
| aaa | - | 0.015 | - | 0.38 | - |
| bbb | - | 0.030 | - | 0.76 | - |
| ccc | - | 0.010 | - | 0.25 | - |
| M | - | 0.0015 | - | 0.038 | 2, 3 |
| N | 16 | | 16 | | 8 |

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Dual-In-Line Plastic Packages (PDIP)



NOTES:

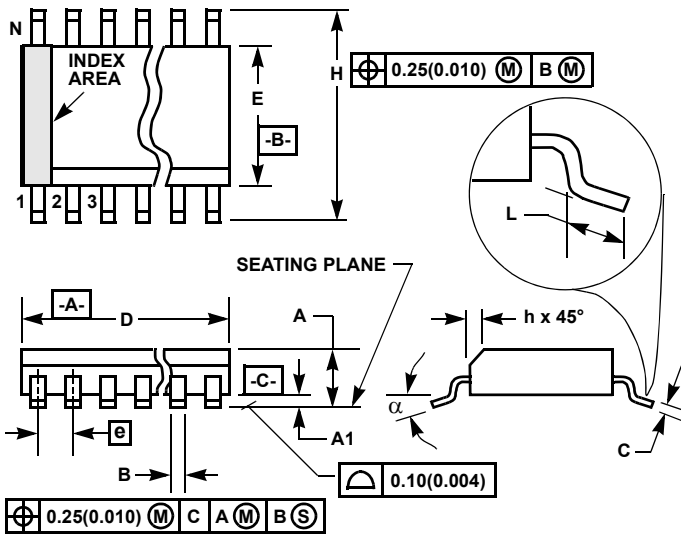
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum $-C-$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|-------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.210 | - | 5.33 | 4 |
| A1 | 0.015 | - | 0.39 | - | 4 |
| A2 | 0.115 | 0.195 | 2.93 | 4.95 | - |
| B | 0.014 | 0.022 | 0.356 | 0.558 | - |
| B1 | 0.045 | 0.070 | 1.15 | 1.77 | 8, 10 |
| C | 0.008 | 0.014 | 0.204 | 0.355 | - |
| D | 0.735 | 0.775 | 18.66 | 19.68 | 5 |
| D1 | 0.005 | - | 0.13 | - | 5 |
| E | 0.300 | 0.325 | 7.62 | 8.25 | 6 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| e_A | 0.300 BSC | | 7.62 BSC | | 6 |
| e_B | - | 0.430 | - | 10.92 | 7 |
| L | 0.115 | 0.150 | 2.93 | 3.81 | 4 |
| N | 16 | | 16 | | 9 |

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|--------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.3859 | 0.3937 | 9.80 | 10.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 16 | | 16 | | 7 |
| alpha | 0° | 8° | 0° | 8° | - |

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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