ISL43112, ISL43113

Low-Voltage, Dual Supply, SPST, High Performance Analog Switches

FN6029
Rev 3.00
Dec 11, 2015

The Intersil ISL43112 and ISL43113 are precision, high performance analog switches designed to operate from ±1.5V to ±6V supplies. These devices are fully specified for 10% tolerance ±5V and ±3.3V supplies and feature supply and leakage currents much lower than those of other single SPST switches. Turn-on and turn-off times are also improved.

Targeted applications include battery powered equipment that benefit from the devices' low power consumption (250µW), sub-nanoamp leakage currents and fast switching speeds (t_{ON} = 40ns, t_{OFF} = 25ns). The small SOT-23 packages and timing that delivers break-before-make operation, make this family ideal for custom multiplexer applications. Additionally, excellent r_{ON} flatness maintains signal fidelity over the whole input range, while micro packaging alleviates board space limitations. All these benefits combine to make Intersil's newest line of low-voltage switches ideal solutions for "Next Generation" designs.

The ISL4311x are Single-Pole/Single-Throw (SPST) switches, with the ISL43112 being Normally Open (NO) and the ISL43113 being Normally Closed (NC).

Table 1 summarizes the performance of this family. For single supply versions, see the ISL43110, ISL43111 datasheet.

TABLE 1. FEATURES AT A GLANCE

FEATURES	ISL43112	ISL43113
Number of Switches	1	1
Configuration	NO	NC
±4.5V r_{ON}	15Ω	15Ω
±4.5V t_{ON} / t_{OFF}	42ns/25ns	42ns/25ns
±3V r_{ON}	20Ω	20Ω
±3V t_{ON} / t_{OFF}	58ns/37ns	58ns/37ns
Packages	8 Ld SOIC, 5 Ld SOT-23	

Related Literature

- TB363,"Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

Features

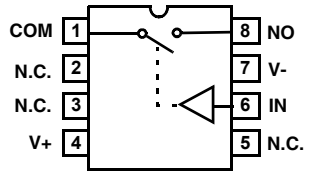
- Fully specified at V_S = ±5V and ±3.3V for 10% tolerances
- Available in SOT-23 packaging
- Dual supply operation. . . . . ±1.5V to ±6V
- ON-resistance 15Ω
- r_{ON} flatness. 5Ω
- Charge injection. 7pC
- Low leakage current (maximum at 85°C) 5nA (off leakage) . . . . . 20nA (on leakage)
- Fast switching action
  - t_{ON} 40ns
  - t_{OFF} 25ns
- Break-before-make operation at V_S = ±5V
- Minimum 2000V ESD protection per Method 3015.7
- CMOS logic compatible
- RoHS Compliant

Applications

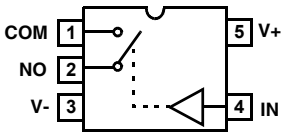
- Battery powered, handheld, and portable equipment
  - Cellular/mobile phones, pagers
  - Laptops, notebooks, palmtops, PDAs
- Communications systems
  - Radios
  - PBX, PABX
- Test equipment
  - Logic and spectrum analyzers
  - Portable meters, DVM, DMM
- Medical equipment
  - Ultrasound, MRI, CAT SCAN
  - Electrocardiograph, blood analyzer
- Audio and video switching
- General purpose circuits
  - Low voltage DACs and ADCs
  - Sample and hold circuits
  - Digital filters
  - Operational amplifier gain switching networks
  - High frequency analog switching
  - High-speed multiplexing
  - Integrator reset circuits

Pin Configurations (Note 1)

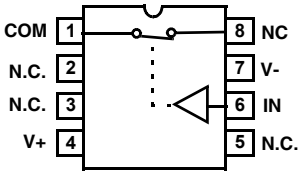
ISL43112
(8LD SOIC)
TOP VIEW



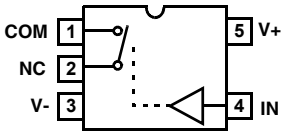
ISL43112
(5 LD SOT-23)
TOP VIEW



ISL43113
(8LD SOIC)
TOP VIEW



ISL43113
(5 LD SOT-23)
TOP VIEW



NOTE:
1. Switches Shown for Logic “0” Input.

Pin Descriptions

PIN	FUNCTION
V+	System Positive Power Supply Input (+1.5V to +6V)
V-	System Negative Power Supply Input (-1.5V to -6V)
IN	CMOS Compatible Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin
N.C.	No Internal Connection

Truth Table

LOGIC	ISL43112	ISL43113
0	OFF	ON
1	ON	OFF

NOTE: Logic “0” $\leq$ 1.5V; Logic “1” $\geq$ 3.5V at V_S = $\pm$5V

Ordering Information

PART NUMBER (Notes 3, 4)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL43112IBZ	ISL431 12IBZ	-40 to +85	8 Ld SOIC	M8.15
ISL43112IBZ-T (Note 2)	ISL431 12IBZ	-40 to +85	8 Ld SOIC	M8.15
ISL43112IHZ-T (Note 2)	112Z (Note 5)	-40 to +85	5 Ld SOT-23	P5.064
ISL43113IBZ	ISL431 13IBZ	-40 to +85	8 Ld SOIC	M8.15
ISL43113IBZ-T (Note 2)	ISL431 13IBZ	-40 to +85	8 Ld SOIC	M8.15
ISL43113IHZ-T (Note 2)	113Z (Note 5)	-40 to +85	5 Ld SOT-23	P5.064

NOTES:

2. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see product information page for ISL43112, ISL43113. For more information on MSL, please see tech brief TB363.
5. The part marking is located on the bottom of the part.

Absolute Maximum Ratings

V+ to V- . . . . . -0.3 to 15V
Input Voltages
IN (Note 6) . . . . . ((V-) - 0.3V) to ((V+) + 0.3V)
NO, NC (Note 6) . . . . . ((V-) - 0.3V) to ((V+) + 0.3V)
Output Voltages
COM (Note 6) . . . . . ((V-) - 0.3V) to ((V+) + 0.3V)
Continuous Current (Any Terminal) 20mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) 30mA
ESD Rating (Per MIL-STD-883 Method 3015) . . . . . >2kV

Thermal Information

Thermal Resistance (Typical, Note 7)	θ_{JA} (°C/W)
5 Ld SOT-23 Package	225
8 Ld SOIC Package	170

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Moisture Sensitivity (See Technical Brief TB363)
All Packages . . . . . Level 1
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Pb-Free Reflow Profile . . . . . see TB493

Operating Conditions

Temperature Range ISL4311XIX . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

6. Signals on NO, NC, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current ratings.
7. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

±5V Supply: Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, V_{INH} = 3.5V, V_{INL} = 1.5V (Note 8), unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	**V-**	-	**V+**	V
ON-Resistance, r_{ON}	V_S = ±4.5V, I_{COM} = 1.0mA, V_{COM} = 3V, see Figure 4	+25	-	15	20	Ω
		Full	-	-	**25**	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_S = ±4.5V, I_{COM} = 1.0mA, V_{COM} = -3V, 0V, 3V	+25	-	5	6	Ω
		Full	-	-	**8**	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ∓4.5V, Note 10	+25	-1	0.01	1	nA
		Full	**-5**	-	**5**	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ∓4.5V, Note 10	+25	-1	0.01	1	nA
		Full	**-5**	-	**5**	nA
COM ON Leakage Current, $I_{COM(ON)}$	V_S = ±5.5V, V_{COM} = V_{NO} or V_{NC} = ±4.5V, Note 10	+25	-2	0.01	2	nA
		Full	**-20**	-	**20**	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	**(V+) - 1.5**	-	**V+**	V
Input Voltage Low, V_{INL}		Full	**V-**	-	**(V+) - 3.5**	V
Input Current, I_{INH}, I_{INL}	V_S = ±5.5V, V_{IN} = 0V or V+	Full	**-0.5**	-	**0.5**	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to V+, see Figure 1	+25	-	42	70	ns
		Full	-	46	**85**	ns
Turn-OFF Time, t_{OFF}	V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to V+, see Figure 1	+25	-	25	45	ns
		Full	-	27	**50**	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, see Figure 2	+25	-	7	20	pC
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, see Figure 3	+25	-	>90	-	dB
Power Supply Rejection Ratio	R_L = 50Ω, C_L = 5pF, f = 1MHz	+25	-	58	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, see Figure 5	+25	-	13	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, see Figure 5	+25	-	13	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, see Figure 5	+25	-	30	-	pF

Electrical Specifications

±5V Supply: Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, V_{INH} = 3.5V, V_{INL} = 1.5V (Note 8), unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	**±1.5**	-	**±6**	V
Positive Supply Current, I+	V_S = ±5.5V, V_{IN} = 0V or V+, Switch On or Off	+25	-	15	25	µA
		Full	-	22	**50**	µA
Negative Supply Current, I-	V_S = ±5.5V, V_{IN} = 0V or V+, Switch On or Off	+25	-25	-15	-	µA
		Full	**-50**	-22	-	µA

NOTES:

8. V_{IN} = Input voltage to perform proper function.
9. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
10. Leakage parameter is 100% tested at high temperature and established by correlation at +25°C.

Electrical Specifications

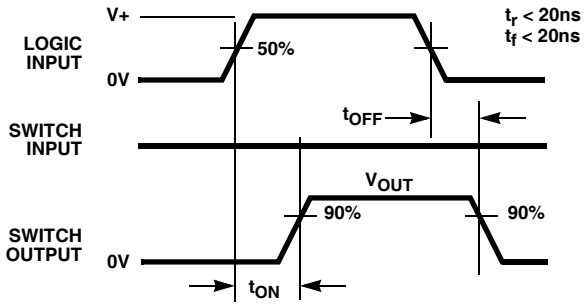
±3.3V supply test conditions: V_{SUPPLY} = ±3.0V to ±3.6V, V_{INH} = V+, V_{INL} = 0V (Note 8), unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	**V-**	-	**V+**	V
ON-Resistance, r_{ON}	V_S = ±3V, I_{COM} = 1.0mA, V_{COM} = 2V	+25	-	20	30	Ω
		Full	-	25	**40**	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_S = ±3V, I_{COM} = 1.0mA, V_{COM} = -1.5V, 0V, 1.5V	+25	-	4	8	Ω
		Full	-	5	**10**	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_S = ±3.3V, V_{COM} = ±2V, V_{NO} or V_{NC} = ∓2V, Note 10	+25	-1	-	1	nA
		Full	**-5**	-	**5**	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V_S = ±3.3V, V_{COM} = ±2V, V_{NO} or V_{NC} = ∓2V, Note 10	+25	-1	-	1	nA
		Full	**-5**	-	**5**	nA
COM ON Leakage Current, $I_{COM(ON)}$	V_S = ±3.3V, V_{COM} = V_{NO} or V_{NC} = ±2V, Note 10	+25	-2	-	2	nA
		Full	**-20**	-	**20**	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	**2.0**	1.6	-	V
Input Voltage Low, V_{INL}		Full	-	0.9	**0.6**	V
Input Current, I_{INH}, I_{INL}	V_S = ±3.6V, V_{IN} = V- or V+	Full	**-0.5**	-	**0.5**	µA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{NO} or V_{NC} = 2V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0.4V to 2.4V	+25	-	58	100	ns
		Full	-	62	**110**	ns
Turn-OFF Time, t_{OFF}	V_{NO} or V_{NC} = 2V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0.4V to 2.4V	+25	-	37	65	ns
		Full	-	40	**75**	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω	+25	-	5	12	pC
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz	+25	-	>90	-	dB
Power Supply Rejection Ratio	R_L = 50Ω, C_L = 5pF, f = 1MHz	+25	-	55	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V	+25	-	13	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V	+25	-	13	-	pF

Electrical Specifications ±3.3V supply test conditions: V_{SUPPLY} = ±3.0V to ±3.6V, V_{INH} = V+, V_{INL} = 0V (Note 8), unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

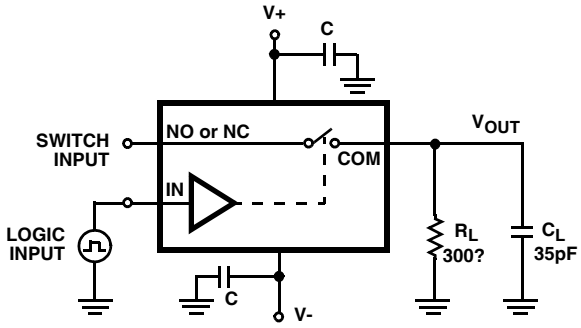
PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V	+25	-	30	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V_S = ±3.6V, V_{IN} = V- or V+, Switch On or Off	+25	-	10	25	µA
		Full	-	15	**50**	µA
Negative Supply Current, I-	V_S = ±3.6V, V_{IN} = V- or V+, Switch On or Off	+25	-25	-10	-	µA
		Full	**-50**	-15	-	µA

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS

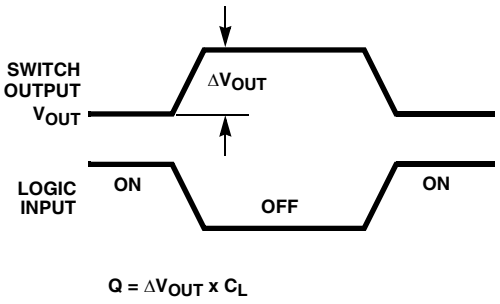


C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES



$Q = \Delta V_{OUT} \times C_L$

FIGURE 2A. MEASUREMENT POINTS

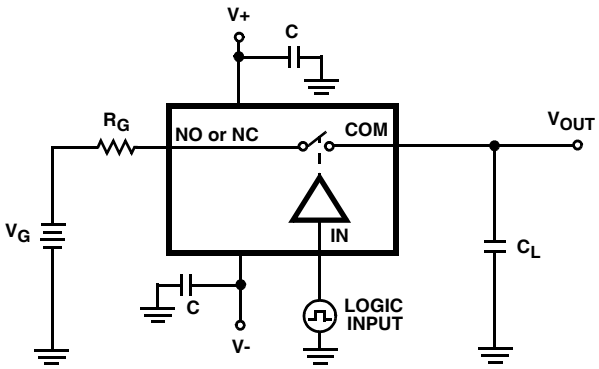


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

Test Circuits and Waveforms (Continued)

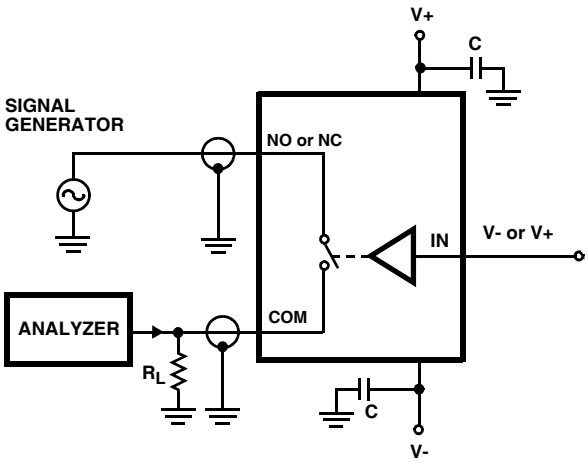


FIGURE 3. OFF-ISOLATION TEST CIRCUIT

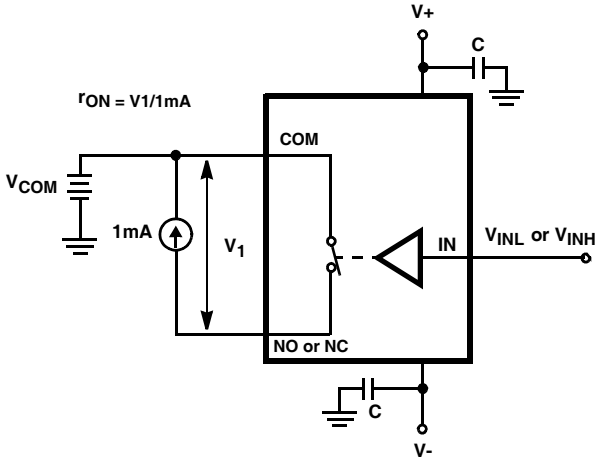


FIGURE 4. r_{ON} TEST CIRCUIT

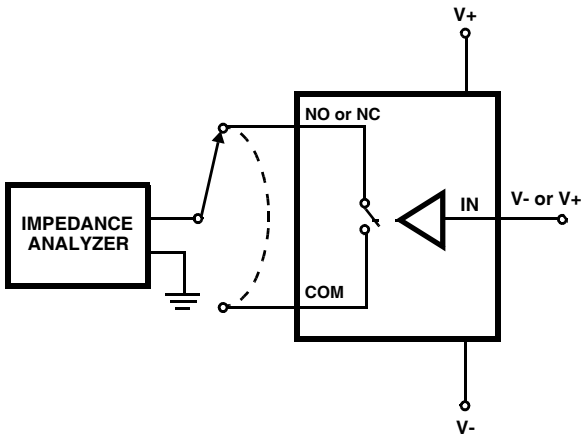


FIGURE 5. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL43112 and ISL43113 analog switches offer precise switching capability from ±1.5V to ±6V supplies with low On-resistance (15Ω) and high-speed operation (t_{ON} = 40ns, t_{OFF} = 25ns). The devices are especially well suited to portable battery powered equipment thanks to the low operating supply voltage (±1.5V), low power consumption (250µW), low leakage currents (2nA max) and the tiny SOT-23 packaging. High frequency applications also benefit from the wide bandwidth, and the very high off isolation.

Supply Sequencing And Overvoltage Protection

As with any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to V- (see Figure 6). To prevent forward biasing these diodes, V+ and V- must be applied before any input signals, and input signal voltages must remain between V+ and V-. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 6).

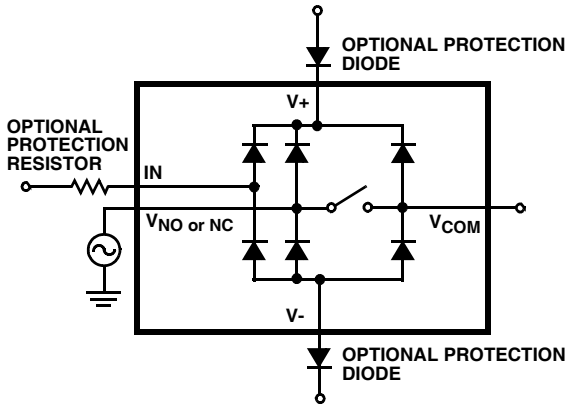


FIGURE 6. OVERVOLTAGE PROTECTION

The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 6). These additional diodes limit the analog signal from 1V below V+ to 1V above V-. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

Power-Supply Considerations

The ISL4311x construction is typical of most CMOS analog switches, except that there are only two supply pins: V+ and V-. The power supplies need not be symmetrical for useful operation. As long as the total supply voltage (V+ to V-, including supply tolerances, overshoot, and noise spikes) is less than the 15V maximum supply rating, and the digital input switching point remains reasonable (see "Logic-Level Thresholds" section), the ISL43112, ISL43113 function well. The 15V maximum supply rating provides the designer of 12V systems much greater flexibility than switches with a 13V maximum supply voltage.

The minimum recommended supply voltage is ±1.5V. It is important to note that the input signal range, switching times and On-resistance degrade at lower supply voltages, and the digital input V_{IL} becomes negative at $V_S \leq \pm 2V$. Refer to the "Typical Performance Curves" for details.

V+ and V- power the internal CMOS switches and set their analog voltage limits. These supplies also power the internal logic and level shifters. The level shifters convert the input logic levels to switched V+ and V- signals to drive the analog switch gate terminals.

This family of switches is not recommended for single supply applications. For single supply, similar performance, pin compatible, TTL compatible versions of these switches, see the ISL43110, ISL43111 datasheet.

Logic-Level Thresholds

Due to the lack of a GND pin, the switching point of the digital input is referenced predominantly to V+. The digital input is CMOS compatible at ±5V supplies, and is TTL compatible for ±3.3V supplies. For other supply combinations refer to Figures 13 and 14.

The switching point has a very low temperature sensitivity, and changes by only 100mV from +85°C to -40°C, regardless of supply voltage.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat to 30MHz, with a -3dB bandwidth of nearly 400MHz (see Figure 15). Figure 15 also illustrates that the frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to its output. OFF Isolation is the resistance to this feedthrough. Figure 16 details the high OFF Isolation provided by this family. At 10MHz, OFF Isolation is about 50dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease OFF Isolation due to the voltage divider action of the switch OFF Impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually, all the analog leakage current comes from the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog-signal path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog-signal paths and V+ or V-.

Typical Performance Curves $T_A = +25°C$, $V_{IH} = V+$, $V_{IL} = 0V$, unless otherwise specified.

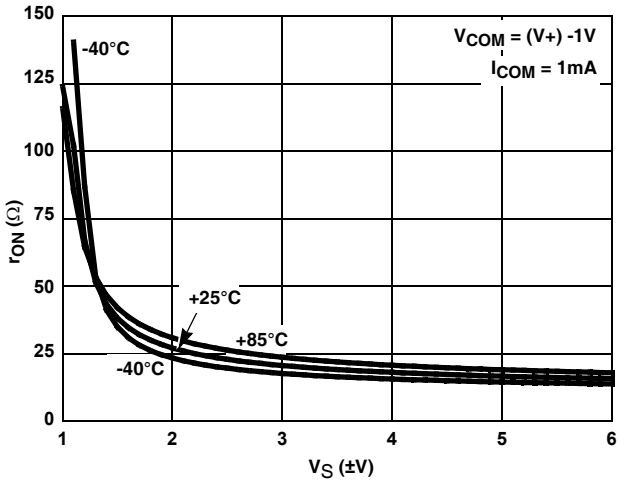


FIGURE 7. ON-RESISTANCE vs SUPPLY VOLTAGE

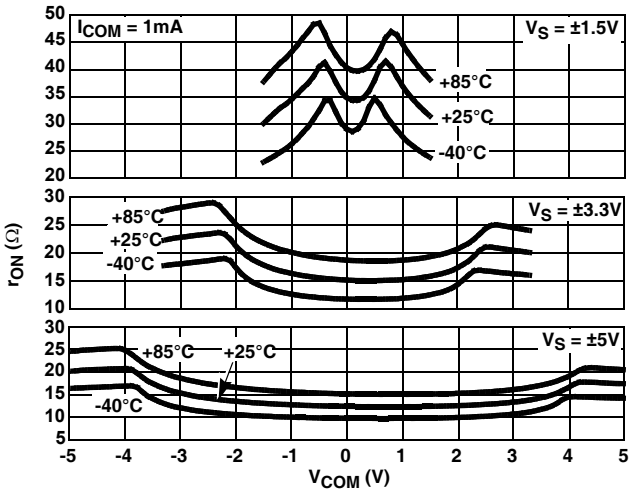


FIGURE 8. ON-RESISTANCE vs SWITCH VOLTAGE

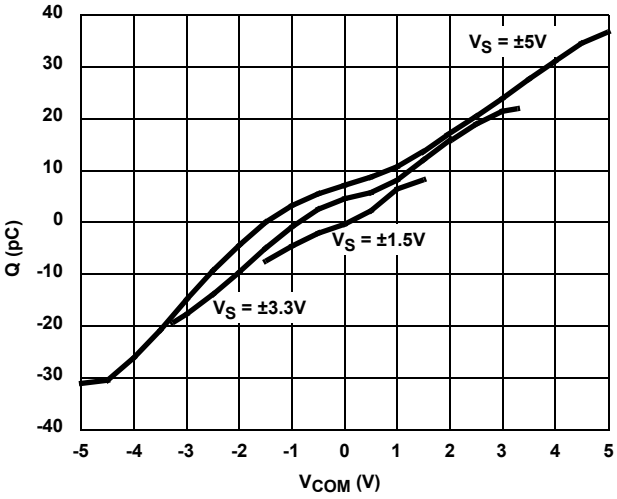


FIGURE 9. CHARGE INJECTION vs SWITCH VOLTAGE

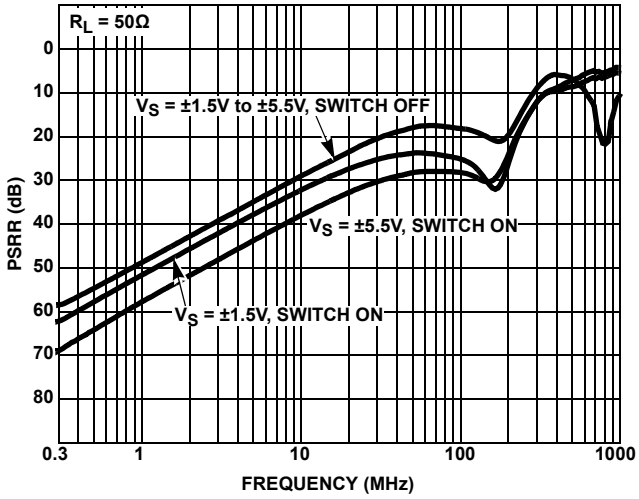


FIGURE 10. PSRR vs FREQUENCY

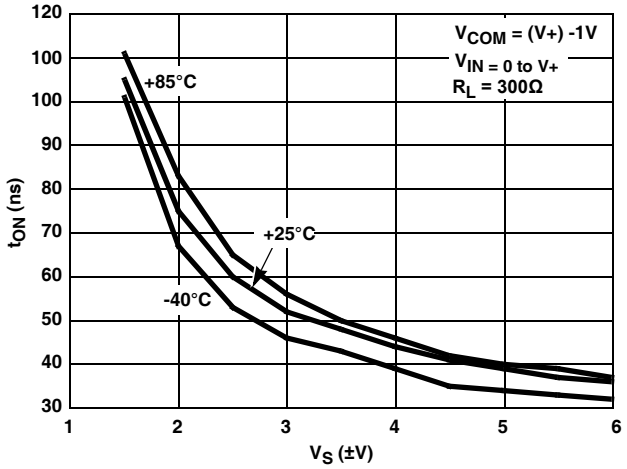


FIGURE 11. TURN-ON TIME vs SUPPLY VOLTAGE

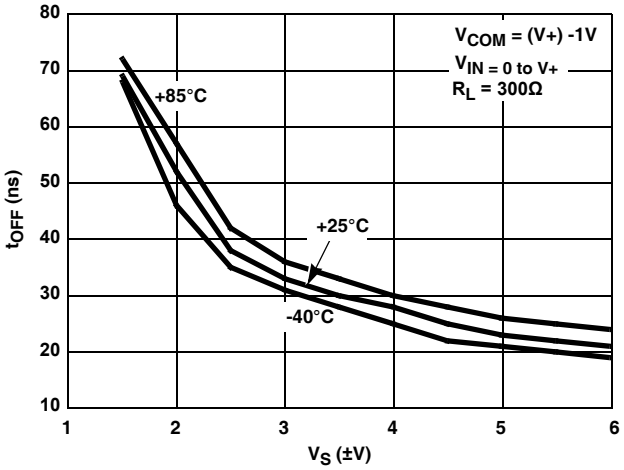


FIGURE 12. TURN-OFF TIME vs SUPPLY VOLTAGE

Typical Performance Curves T_A = +25°C, V_{IH} = V+, V_{IL} = 0V, unless otherwise specified. **(Continued)**

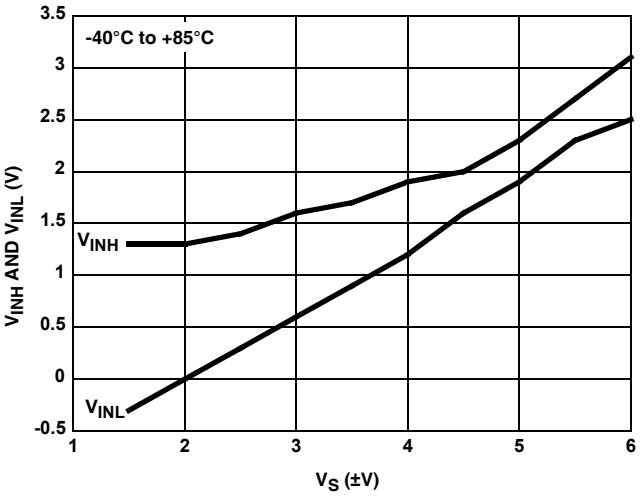


FIGURE 13. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

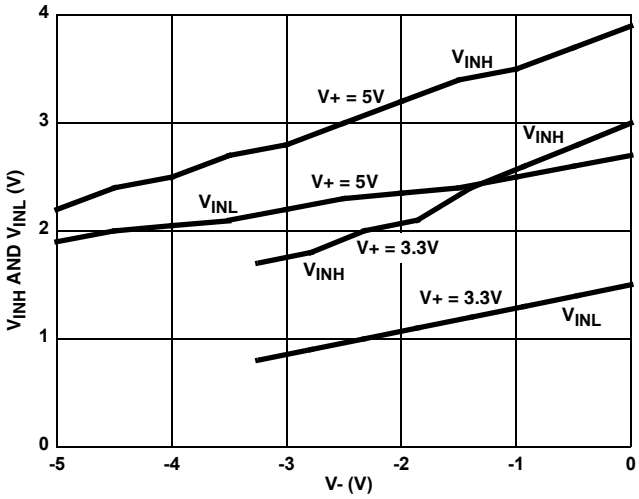


FIGURE 14. DIGITAL SWITCHING POINT vs NEGATIVE SUPPLY VOLTAGE

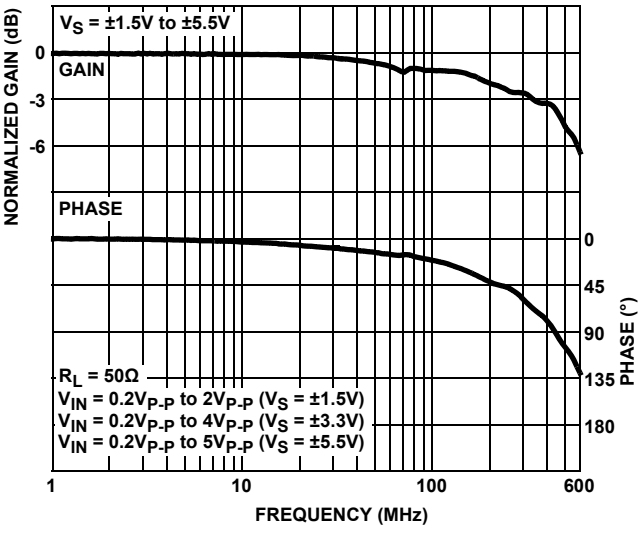


FIGURE 15. FREQUENCY RESPONSE

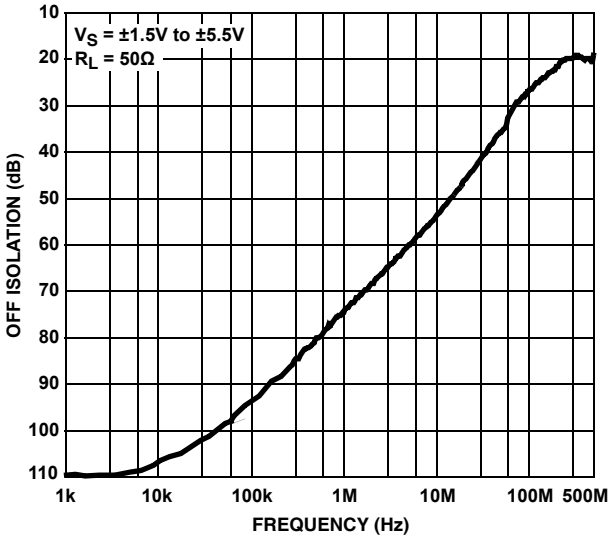


FIGURE 16. OFF ISOLATION

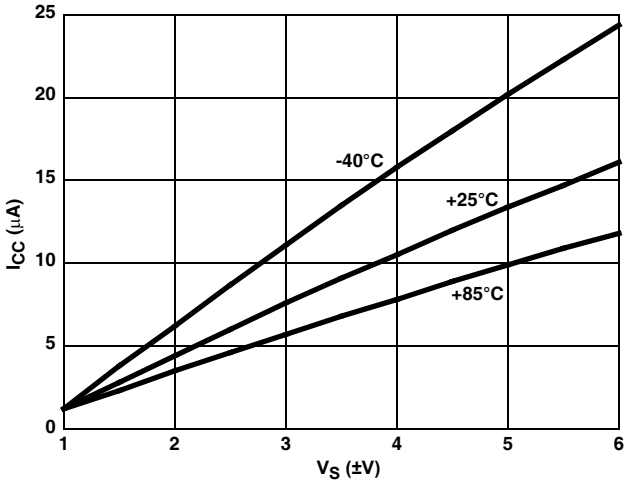


FIGURE 17. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

V-

TRANSISTOR COUNT:

ISL43112: 55
ISL43113: 55

PROCESS:

Si Gate CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
December 11, 2015	FN6029.3	Applied new Intersil standards to throughout datasheet. Updated the ordering information table by removing obsolete products, adding notes, and updating the part marking. Added the Revision History and About Intersil sections Updated POD M8.15 to the latest revision the changes are as follows: -Remove “u” symbol from drawing (overlaps the “a” on Side View). -Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern -Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -In Note 1 changed “1982” to “1994” Updated POD P5.064 to the latest revision the changes are as follows: -Converted to new format. Moved dimensions from table onto drawing and added land pattern)

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

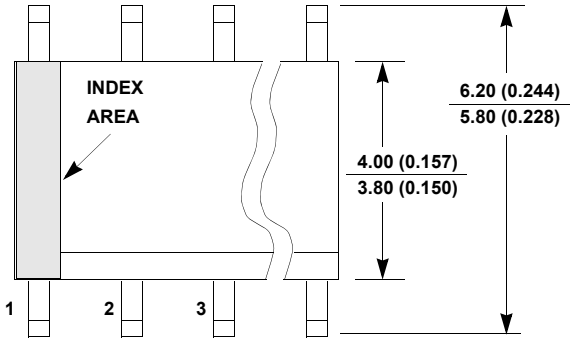
Reliability reports are also available from our website at www.intersil.com/support.

Package Outline Drawing

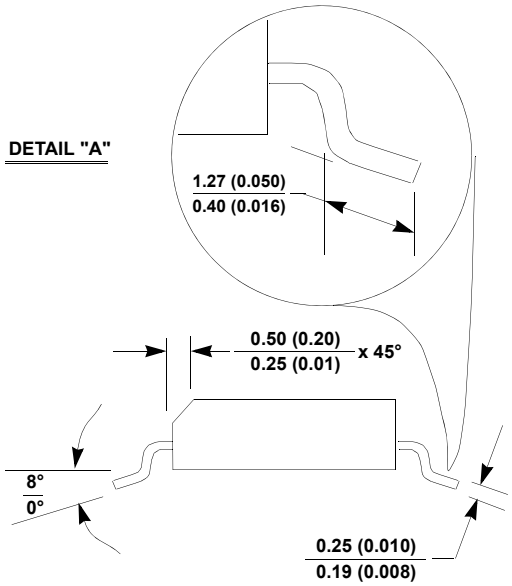
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

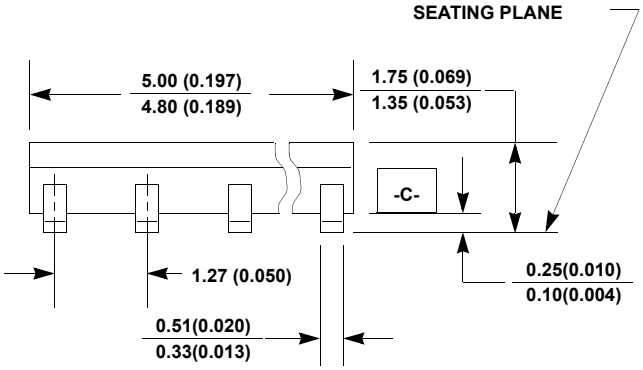
Rev 4, 1/12



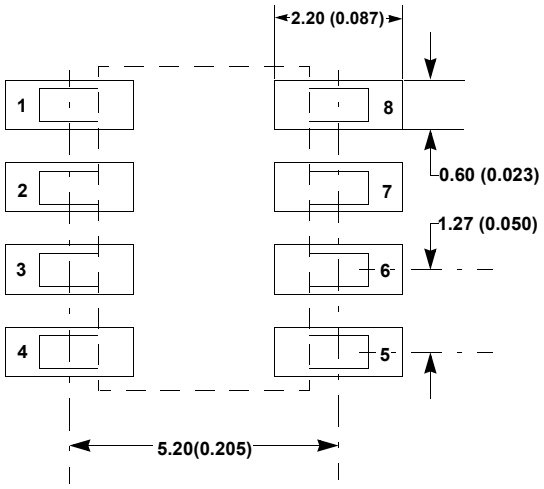
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

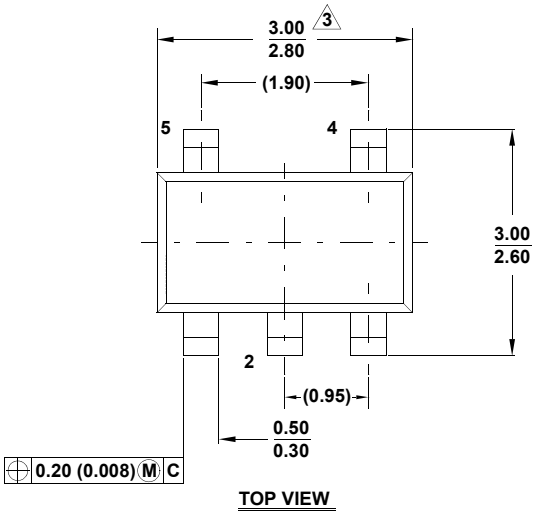
1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Package Outline Drawing

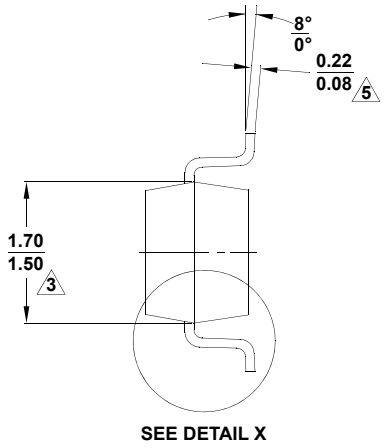
P5.064

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

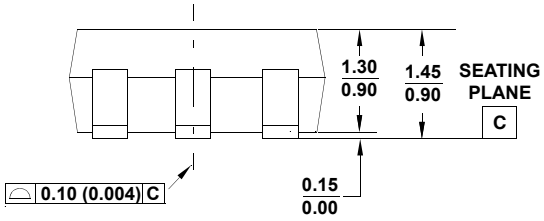
Rev 3, 4/11



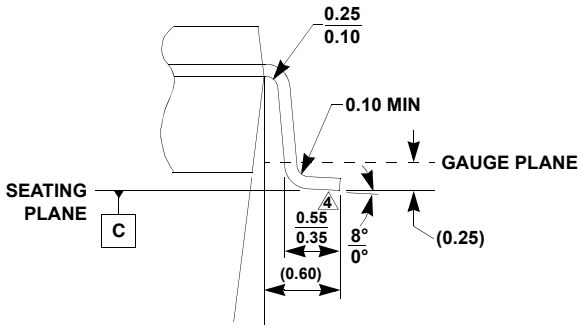
TOP VIEW



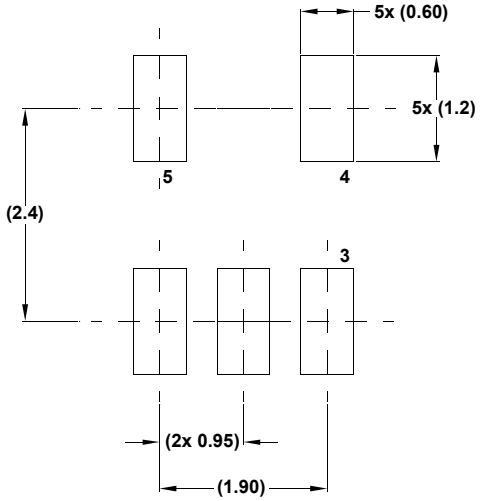
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AA.
3. Package length and width are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength measured at reference to gauge plane.
5. Lead thickness applies to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
6. Controlling dimension: MILLIMETER. Dimensions in ( ) for reference only.