

# CD22M3494

16 x 8 x 1 BiMOS-E Crosspoint Switch

FN2793 Rev 8.00 May 29, 2014

The Intersil CD22M3494 is an array of 128 analog switches capable of handling signals from DC to video. Because of the switch structure, input signals may swing through the total supply voltage range,  $V_{DD}$  to  $V_{EE}$ . Each of the 128 switches may be addressed via the ADDRESS input to the 7 to 128 line decoder. The state of the addressed switch is established by the signal to the DATA input. A low or zero input will open the switch, while a high logic level or a one will result in closure of the addressed switch when the STROBE input goes high from its normally low state. Any number or combination of connections may be active at one time. Each connection, however, must be made or broken individually in the manner previously described. All switches may be reset by taking the RESET input from a zero state to a one state and then returning it to its normal low state.

CS allows crosspoint array to be cascaded for matrix expansion.

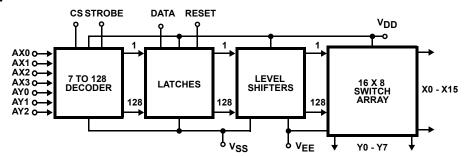
### **Features**

- · 128 Analog Switches
- Low r<sub>ON</sub>
- Guaranteed r<sub>ON</sub> Matching
- · Analog Signal Input Voltage Equal to the Supply Voltage
- Wide Operating Voltage . . . . . . . . . . . . 4V to 15V
- · Parallel Input Addressing
- High Latch-Up Current . . . . . . . . . . . . 50mA (Min)
- · Very Low Crosstalk
- Pin and Functionally Compatible with the Following Types: SGS M3494 and Mitel MT8816
- · Pb-Free (RoHS Compliant)

# **Applications**

- · PBX Systems
- · Instrumentation
- · Analog and Digital Multiplexers
- · Video Switching Networks

### **Block Diagram**



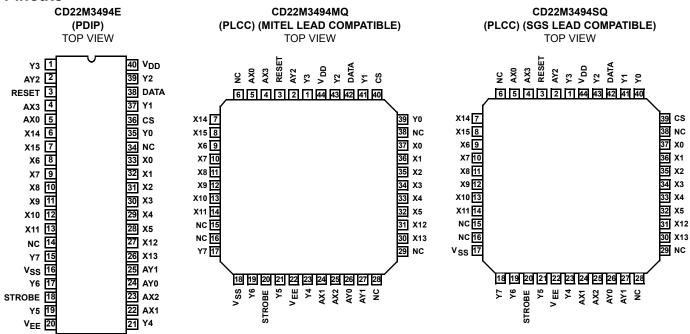
## **Ordering Information**

PART NUMBER (Note 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
CD22M3494EZ	CD22M3494EZ	-40 to 85	40 Ld PDIP (Note 2)	E40.6
CD22M3494MQZ ( <u>Note 1</u> )	CD22M3494MQZ	-40 to 85	44 Ld PLCC (Mitel Ld Compatible)	N44.65
CD22M3494MQAZ ( <u>Note 1</u> )	CD22M3494MQAZ	-40 to 85	44 Ld PLCC (Mitel Ld Compatible)	N44.65
CD22M3494SQZ ( <u>Note 1</u> )	CD22M3494SQZ	-40 to 85	44 Ld PLCC (SGS Ld Compatible)	N44.65

#### NOTES:

- 1. Add "96" suffix for tape and reel. At one time the "QZ" and "QAZ" were different products, but since 1994 these parts have been exactly the same.
- 2. Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in Reflow solder processing applications.
- 3. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

### **Pinouts**



# Pin Descriptions

	40 LD PDIP	44 LD PLCC PIN NO.		PIN NO.		
SYMBOL	1		SQ	DESCRIPTION		
POWER SUPP	LIES					
V <sub>DD</sub>	40	44	44	Positive Supply.		
V <sub>SS</sub>	16	18	17	Negative Supply (Digital).		
V <sub>EE</sub>	20	22	22	Negative Supply (Analog).		
ADDRESS						
AX0 - AX3	5, 22, 23 and 4	5, 24, 2	25 and 4	X Address Lines. These pins select one of the 16 rows of switches. See the Truth Table on page 7 for the valid addresses.		
AY0 - AY2	24, 25 and 2	26, 27	and 2	Y Address Lines. These pins select one of the 8 columns of switches. So the Truth Table on page 7 for the valid addresses.		
CONTROL						
DATA	38	4	12	DATA Input determines the state of the addressed switch. A high or one will close the switch. A low or zero will open the switch.		
STROBE	18	2	20	STROBE Input enables the action defined by the DATA and ADDRESS Inputs. A low or zero results in no action. The ADDRESS Input must be stable before the STROBE Input goes to the active high level. The DATA Input must be stable on the failing edge of the STROBE.		
RESET	3	;	3	MASTER RESET. A high or one on this line opens all switches.		
CS	36	40	39	CHIP SELECT. Device is selected when CS is at a high level, allows the crosspoint array to be cascaded for matrix expansion.		
INPUTS/OUTP	UTS	,	I.			
X0 - X5 X6 - X11 X12 - X15	33-28, 8-13, 27, 26, 6, 7	37-32, 9-14, 31, 30, 7, 8		Analog or Digital Inputs/Outputs. These pins are the rows X0 - X15.		
Y0 - Y7 I/O	35, 37, 39, 1, 21, 19, 17, 15	39, 41, 43, 1, 23, 21, 19, 17	40, 41, 43, 1, 23, 21, 19, 18	Analog or Digital Inputs/Outputs. These pins are the columns Y0 - Y7.		

### **Absolute Maximum Ratings**

DC Supply Voltage (V <sub>DD</sub> )	
Voltages Referenced to V <sub>EE</sub> 0.5	V to 16V
DC Supply Voltage (V <sub>DD</sub> )	
Voltages Referenced to V <sub>SS</sub> 0.5	V to 16V
DC Input Diode Current, I <sub>IN</sub>	
For $V_I$ , Digital $< V_{SS}$ -0.5V or $V_I$ ,	
Analog < V <sub>EE</sub> -0.5V or V <sub>I</sub> > V <sub>DD</sub> 0.5V	. ±20mA
DC Output Diode Current, I <sub>OK</sub>	
For $V_O$ , Digital < $V_{SS}$ -0.5V or $V_O$ ,	
Analog < V <sub>EE</sub> -0.5V or V <sub>O</sub> > V <sub>DD</sub> 0.5V	. ±20mA
DC Transmission Gate Current	. ±25mA
Power Dissipation Per Package (Po)	
For $T_A = -40$ °C to $+85$ °C (PDIP)	.500mW
For $T_A = -40^{\circ}C$ to $+85^{\circ}C$ (PLCC)	.600mW

### **Thermal Information**

Thermal Resistance (Typical, Note 4)	$\theta_{JA}$ (°C/W)
PDIP Package*	55
PLCC Package	43
Maximum Junction Temperature Plastic Package	
Maximum Storage Temperature Range (T <sub>STG</sub> )65°	°C to +150°C
Pb-Free Reflow Profile	. see <u>TB493</u>
*Pb-free PDIPs can be used for through hole wave solde	r processing
only. They are not intended for use in Reflow solder pro	cessing.
applications.	

### **Operating Conditions**

Operating Temperature Range (T <sub>A</sub> )
Package Type E and Q40°C to +85°C
Supply Voltage Range
For T <sub>A</sub> = Full Package Temperature Range
V <sub>SS</sub> = 0V, V <sub>EE</sub> = 0V, V <sub>DD</sub>
DC Input or Output Voltage V <sub>I</sub> or V <sub>O</sub> V <sub>EE</sub> to V <sub>DD</sub>
Digital Input VoltageV <sub>SS</sub> to V <sub>DD</sub>

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

4.  $\theta_{\mbox{\scriptsize JA}}$  is measured with the component mounted on an evaluation PC board in free air.

## **Electrical Specifications** $T_A = -40$ °C to +85°C, $V_{DD} = 5$ V, $V_{SS} = 0$ V, $V_{EE} = 0$ V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
STATIC CONTROLS						
Supply Current	I <sub>DD</sub>	V <sub>DD</sub> = 5V, Logic Inputs = V <sub>DD</sub>	-	-	2	mA
		V <sub>DD</sub> = 15V, Logic Inputs = V <sub>DD</sub>	-	-	5	mA
High-Level Input Voltage	V <sub>IH</sub>	V <sub>DD</sub> = 5V	2.4 ( <u>Note 5</u> )	-	-	V
Low-Level Input Voltage	V <sub>IL</sub>		-	-	0.8 ( <u>Note 5</u> )	V
Input Leakage Current, Digital	I <sub>IN</sub>	Reset = Low (Note 6)	-	-	±10 ( <u>Note 7</u> )	μА

# **Electrical Specifications** $T_A = -40 \,^{\circ}\text{C}$ to $+85 \,^{\circ}\text{C}$ , $V_{DD} = 12 \,^{\circ}\text{V}$ , $V_{EE} = 0 \,^{\circ}\text{V}$ , Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
STATIC CROSSPOINTS							
ON Resistance	r <sub>ON</sub>	V <sub>SS</sub> = V <sub>EE</sub> = 0V,	V <sub>DD</sub> = 10V	-	40	75	Ω
		$T_A = +25^{\circ}C$ , $V_{IN} = V_{DD}/2$ , $VX - VY = 0.2V$	V <sub>DD</sub> = 12V	-	36	65	Ω
ON Resistance	r <sub>ON</sub>	$T_A = -40$ °C to +85 °C,	V <sub>DD</sub> = 10V	-	50	75	Ω
		$V_{IN} = V_{DD}/2$ , VX -VY = 0.2V, V <sub>SS</sub> = V <sub>EE</sub> = 0V	V <sub>DD</sub> = 12V	-	45	65	Ω
Difference in ON Resistance Between Any Two Switches	Δr <sub>ON</sub>	$T_A = +25 ^{\circ}\text{C}, V_{IN} = V_{DD}/2, V_{SS}$ $V_{SS} = V_{EE} = 0V, V_{DD} = 12V$	X - VY = 0.2V,	-	6	10	Ω



# $\textbf{Electrical Specifications} \hspace{0.5cm} \textbf{T}_{A} = -40\,^{\circ}\text{C to } +85\,^{\circ}\text{C}, \\ \textbf{V}_{DD} = 12\text{V}, \\ \textbf{V}_{SS} = 0\text{V}, \\ \textbf{V}_{EE} = 0\text{V}, \\ \textbf{Unless Otherwise Specified}. \hspace{0.5cm} \textbf{(Continued)}$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Difference in ON Resistance Between Any Two Switches	Δr <sub>ON</sub>	$T_A = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C}, V_{\text{IN}} = V_{\text{DD}}/2,$ $VX - VY = 0.2V, V_{\text{DD}} = 12V$ $V_{\text{SS}} = V_{\text{EE}} = 0V, VDD = 12V$	-	-	10	Ω
OFF-State Leakage Current	ΙL	VX - VY  = 12V	-	-	±10 ( <u>Note 7</u> )	μΑ

# $\textbf{Electrical Specifications} \hspace{0.3cm} \textbf{T}_{A} = +25 ^{\circ} \text{C}, \, \textbf{V}_{SS} = \textbf{0V}, \, \textbf{V}_{EE} = \textbf{0V}, \, \textbf{V}_{DD} = \textbf{14V}, \, \textbf{C}_{L} = \textbf{50pF}, \, \textbf{Unless Otherwise Specified}.$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CROSSPOINTS				•		
Switch I/O Capacitance		$V_{IN} = V_{DD}/2$ , $f = 1MHz$	-	-	20	pF
Switch Feedthrough Capacitance		V <sub>IN</sub> = V <sub>DD</sub> /2, f = 1MHz	-	0.3	-	pF
Propagation Delay Time (Switch ON) Signal Input to Output, t <sub>PHL</sub> or t <sub>PLH</sub>			-	5	30	ns
Frequency Response Channel ON f = 20log (VX/VY) = -3dB		$C_L = 3pF, R_L = 75\Omega, V_{IN} = 2V_{P-P}$	-	50	-	MHz
Total Harmonic, THD		V <sub>IN</sub> = 2V <sub>P-P</sub> , f = 1kHz	-	0.01	-	%
Feedthrough Channel OFF Feedthrough = 20log (VX/VY) = F <sub>DT</sub>		$V_{IN} = 2V_{P-P}$ , $f = 1kHz$	-	-95	-	dB
Frequency for Signal Crosstalk, f <sub>CT</sub>	40dB	$V_{IN} = 2V_{P-P}$ , $R_L = 75\Omega$	-	10	-	MHz
Attenuation of: 110dB		$V_{IN} = 2V_{P-P}$ , $R_L = 1k\Omega \parallel 10pF$	-	5	-	kHz
Control Crosstalk DATA-Input, ADDRESS, or STROBE to Output		Control Input = $3V_{P-P}$ Square Wave, $t_R = t_F = 10$ ns $R_{IN} = 1$ K, $R_{OUT} = 10$ k $\Omega$    10pF	-	75	-	mV <sub>PEAK</sub>

# $\textbf{Electrical Specifications} \hspace{0.5cm} \textbf{T}_{A} = +25\,^{\circ}\text{C}, \textbf{V}_{SS} = 0 \\ \textbf{V}, \textbf{V}_{DD} = 14 \\ \textbf{V}, \textbf{R}_{L} = 1 \\ \textbf{k} \\ \Omega \parallel 50 \\ \textbf{pF}, \textbf{Unless Otherwise Specified}. \\ \textbf{T}_{A} = +25\,^{\circ}\text{C}, \textbf{V}_{SS} = 0 \\ \textbf{V}, \textbf{V}_{DD} = 14 \\ \textbf{V}, \textbf{R}_{L} = 1 \\ \textbf{k} \\ \Omega \parallel 50 \\ \textbf{pF}, \textbf{Unless Otherwise Specified}. \\ \textbf{T}_{A} = +25\,^{\circ}\text{C}, \textbf{V}_{SS} = 0 \\ \textbf{V}, \textbf{V}_{DD} = 14 \\ \textbf{V}, \textbf{R}_{L} = 1 \\ \textbf{K} \\ \Omega \parallel 50 \\ \textbf{PF}, \textbf{Unless Otherwise Specified}. \\ \textbf{T}_{A} = +25\,^{\circ}\text{C}, \textbf{V}_{SS} = 0 \\ \textbf{V}, \textbf{V}_{DD} = 14 \\ \textbf$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CONTROLS						
Digital Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 5V, f = 1MHz	-	5	-	pF
Propagation Delay Time STROBE to Output						
Switch Turn-ON	t <sub>PSN</sub>		-	50	100	ns
Switch Turn-OFF	t <sub>PSF</sub>		-	50	100	ns
DATA-IN to Output						
Turn-ON to High Level	t <sub>PZH</sub>		-	60	100	ns
Turn-ON to Low Level	t <sub>PZL</sub>		-	70	100	ns
ADDRESS to Output						
Turn-ON to High Level	t <sub>PAN</sub>		-	70	-	ns
Turn-OFF to Low Level	t <sub>PAF</sub>		-	70	-	ns

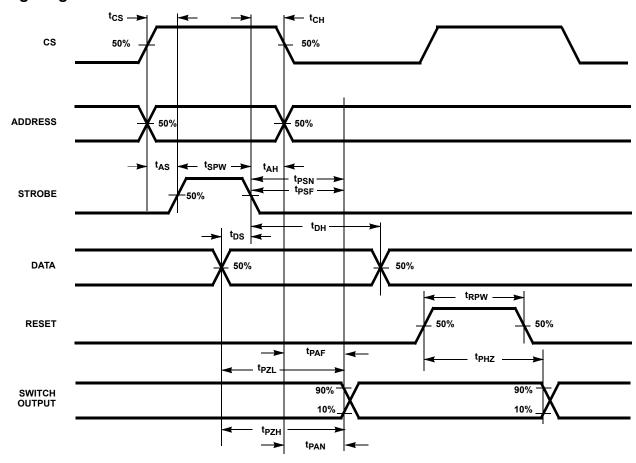
 $\textbf{Electrical Specifications} \hspace{0.5cm} \textbf{T}_{A} = +25 \,^{\circ} \, \text{C}, \ \textbf{V}_{SS} = 0 \,^{\vee} \, \textbf{V}_{EE} = 0 \,^{\vee} \, \textbf{V}_{DD} = 14 \,^{\vee} \, \textbf{V}_{L} = 1 \,^{\vee} \, \textbf{K} \, \textbf{Q} \parallel 50 \,^{\vee} \, \textbf{P}, \ \textbf{Unless Otherwise Specified}. \hspace{0.5cm} \textbf{(Continued)}$ 

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time						
CS to STROBE	t <sub>CS</sub>		10	-	-	ns
DATA-IN to STROBE	t <sub>DS</sub>		10	-	-	ns
ADDRESS to STROBE	t <sub>AS</sub>		10	-	-	ns
Hold Time						
STROBE to CS	t <sub>CH</sub>		10	-	-	ns
ADDRESS to CS			10	-	-	ns
STROBE to DATA-IN	t <sub>DH</sub>		20	-	-	ns
STROBE to ADDRESS	t <sub>AH</sub>		10	-	-	ns
DATA-IN to CS			20	-	-	ns
Pulse Width						
STROBE	t <sub>SPW</sub>		20	-	-	ns
RESET	t <sub>RPW</sub>		20	-	-	ns
RESET Turn-OFF to Output Delay	t <sub>PHZ</sub>		-	70	100	ns

### NOTES:

- 5. Operation of  $V_{IH}$  at 2.4V or  $V_{IL}$  at 0.8V will result in much higher supply current ( $I_{DD}$ ) than for logic inputs equal to  $V_{DD}$  or  $V_{SS}$  respectively.
- 6. Reset  $I_{IH}$  < 20 $\mu$ A, Reset =  $V_{IH}$ .
- 7. At  $+25^{\circ}$ C Limit is  $\pm 100$ nA.

# Timing Diagram



### **TRUTH TABLE X AXIS**

	X ADDRESS						
AX3	AX2	AX1	AX0	X SWITCH			
0	0	0	0	X0			
0	0	0	1	X1			
0	0	1	0	X2			
0	0	1	1	Х3			
0	1	0	0	X4			
0	1	0	1	X5			
0	1	1	0	X12			
0	1	1	1	X13			
1	0	0	0	X6			
1	0	0	1	X7			
1	0	1	0	X8			
1	0	1	1	X9			
1	1	0	0	X10			
1	1	0	1	X11			
1	1	1	0	X14			
1	1	1	1	X15			

### **TRUTH TABLE Y AXIS**

Y ADDRESS					
AY2	AY1 AY0		Y SWITCH		
0	0	0	Y0		
0	0	1	Y1		
0	1	0	Y2		
0	1	1	Y3		
1	0	0	Y4		
1	0	1	Y5		
1	1	0	Y6		
1	1	1	Y7		

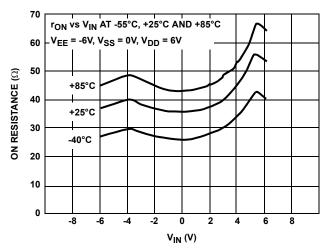
To make a connection (close switch) between any two points, specify an "X" address, a "Y" address, set "DATA" high, and switch "STROBE" from low to high. To break a connection, follow this same procedure with "DATA" low.

Example:

To connect switch X3 to switch Y4:
To connect switch X6 to switch Y7:
To break connection from X3 to Y4:

	X ADDRESS			Y ADDRESS			
DATA	AX3	AX2	AX1	AX0	AY2	AY1	AY0
1	0	0	1	1	1	0	0
1	1	0	0	0	1	1	1
0	0	0	1	1	1	0	0

# Typical Performance Curve



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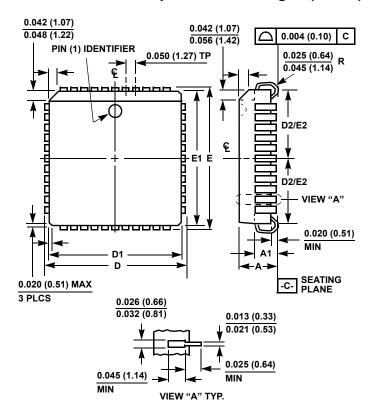
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# Plastic Leaded Chip Carrier Packages (PLCC)



### NOTES:

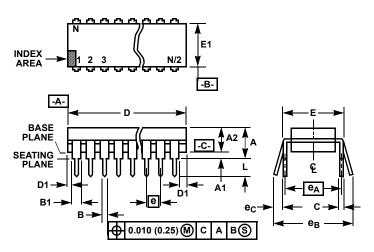
- Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
- 2. Dimensions and tolerancing per ANSI Y14.5M-1982.
- 3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
- 4. To be measured at seating plane -C- contact point.
- 5. Centerline to be determined where center leads exit plastic body.
- 6. "N" is the number of terminal positions.

N44.65 (JEDEC MS-018AC ISSUE A)
44 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.685	0.695	17.40	17.65	-
D1	0.650	0.656	16.51	16.66	3
D2	0.291	0.319	7.40	8.10	4, 5
Е	0.685	0.695	17.40	17.65	-
E1	0.650	0.656	16.51	16.66	3
E2	0.291	0.319	7.40	8.10	4, 5
N	4	4	4	14	6

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### Dual-In-Line Plastic Packages (PDIP)



#### NOTES:

- 1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- 2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- 3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- 4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions.
   Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and e<sub>A</sub> are measured with the leads constrained to be perpendicular to datum -C-.
- 7.  $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
- 8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- 9. N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

### **E40.6** (JEDEC MS-011-AC ISSUE B) 40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
В	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
С	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
Е	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
е	0.100 BSC		2.54 BSC		-
e <sub>A</sub>	0.600 BSC		15.24 BSC		6
e <sub>B</sub>	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

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