LatticeMico32/DSP Development Board for LatticeECP2

User's Guide

June 2009
Revision: EB26_02.6

Introduction

This document describes the features and functionality of the LatticeMico32™/DSP Development Board for LatticeECP2™ devices. This board is designed as a hardware platform for design and development with the LatticeMico32 microprocessor, as well as for the LatticeMico8™ microcontroller, and for various DSP functions.

Note: There are two versions of this board, named version 1 (v1) and version 2 (v2). Differences between the v1 and v2 boards are described in this document as required. The appendices of this document contain schematics of both versions. In summary, v2 boards include the following changes:

- *Copper plating indicates v2 in text (HPEminiv2)*
- *A pushbutton has been added for USB reset. This allows the FPGA to be reset independently from the USB Cable circuitry.*
- *Boards are populated with a MachXO-2280 device (v1 boards were populated with a MachXO-640).*
- *Board color is blue, and board is fully RoHS compliant.*

This document describes the numerous functional elements of the board. The schematics of the board can be found in the appendices at the end of this document.

Features

- Lattice ECP2-50 FPGA with 48 kLUTs, 387 kbit of Embedded Block RAM, 18 sysDSP™ blocks, 72 18x18 multipliers, 6 PLLs, and 500 user I/O pins
- Lattice MachXO™ with 640 LUTs and 6.1 kbit of RAM
- Serial Flash with at least 8 Mbit for non-volatile storage of FPGA configuration data.
- DDR SODIMM socket for DDR SDRAM modules (DDR1, 100-133MHz, 32-bit data bus)
- Parallel Flash 2x128 Mbit, organized as 8M 32-bit words
- SRAM 2x4 Mbit, organized as 256K 32-bit words
- USB 2.0 connector and integrated ispDOWNLOAD® cable for JTAG programming the FPGA
- Flywire connector for programming using an ispDOWNLOAD cable (available separately)
- 9-pin RS232 serial port (230 Kbps)
- 15-pin VGA (64 color encoding)
- Ethernet 10/100 M full/half duplex
- Two USB 2.0 compatible host connectors
- One USB 2.0 compatible target connector
- One USB OTG (On-the-Go) connector
- Expansion connector with 46 user I/Os
- 12x12 prototyping area for the integration of individual components (connections to the FPGA)
- Sigma Delta D/A converter
- Two SATA interfaces with four LVDS signal pairs for high-speed data transfer *(Note: Full SATA implementation is not supported)*
- AC'97 Stereo Audio Codec with line input and output
- LCD connector for character displays, with contrast potentiometer
- 25 MHz oscillator with clock distribution buffer

- Eight LEDs with test points for each LED
- Two-character 7-segment display
- Green LED to indicate the proper operation of the 3.3V and 2.5 V power supplies
- Blue LED which shows the configuration status ("DONE")
- Red LED to signal that the FPGA can be configured ("INIT")
- Yellow LED indicating the FPGA PROGRAM# I/O is asserted ("PROGRAM#")
- 3x4 key matrix
- Four DIP switches
- Single step key
- Program key to initiate the configuration sequence of the FPGA from SPI Flash memory
- Reset key
- 5V power supply
- Switching regulator for the generation of the 3.3V I/O voltage, the 2.5V DDR and LVDS voltages and the 1.2V core voltage

Getting Started

1. Unpack all components and compare them to the packaging list. All boards leave the factory fully tested. Detailed information can be found in the Troubleshooting section of this document.
2. Place the board in front of you so that the keyboard is on the left side.
3. Take the regulated DC power supply which has been supplied with the package and connect it to the power jack on the board. Two green power-on LEDs will illuminate to confirm that power is correctly applied to the board (regulating 5V to 3.3V and 2.5V).
4. To check the basic functionality, please see the Troubleshooting section of this document.

A number of example and demonstration programs are available for the LatticeMico32/DSP Development Board for LatticeECP2. Check the Lattice web site at: www.latticesemi.com/boards (and navigate to the correct board) to find additional documentation, such as the LatticeMico32 Tutorial, which describes how to use the LatticeMico32 System software to develop microprocessor solutions for this board. Additional sample programs are included with the LatticeMico32 System software. Check the software help to find these examples.

Note: Unless described otherwise, positional statements (left, right etc.) refer to the board positioned in front of you so that the key pad is in the bottom left corner.

Related Literature

- **LatticeMico32 Development Kit User's Guide**: This guide includes a tutorial for using the LatticeMico32 System software with the LatticeMico32/DSP Development Board. This document is written for the first generation board (with LatticeECP-33 FPGA), which is similar to the board described in this document. While this document may be useful, please remember there are differences in the designs of these boards.

Be sure to check the Lattice web site for updates to this document as well.

These documents can be downloaded from the Lattice web site at: www.latticesemi.com/boards. Select the **FPGA/FPSC Boards -> LatticeMico32/DSP Development board for LatticeECP2** and click on the **User Manuals** link.

Overview

The following block diagram gives you an overview of the functionality of your LatticeMico32/DSP Development Board. Subsequent pages illustrate the position of connectors, user interfaces, and modules.

Figure 1. LatticeMico32/DSP Development Board Block Diagram

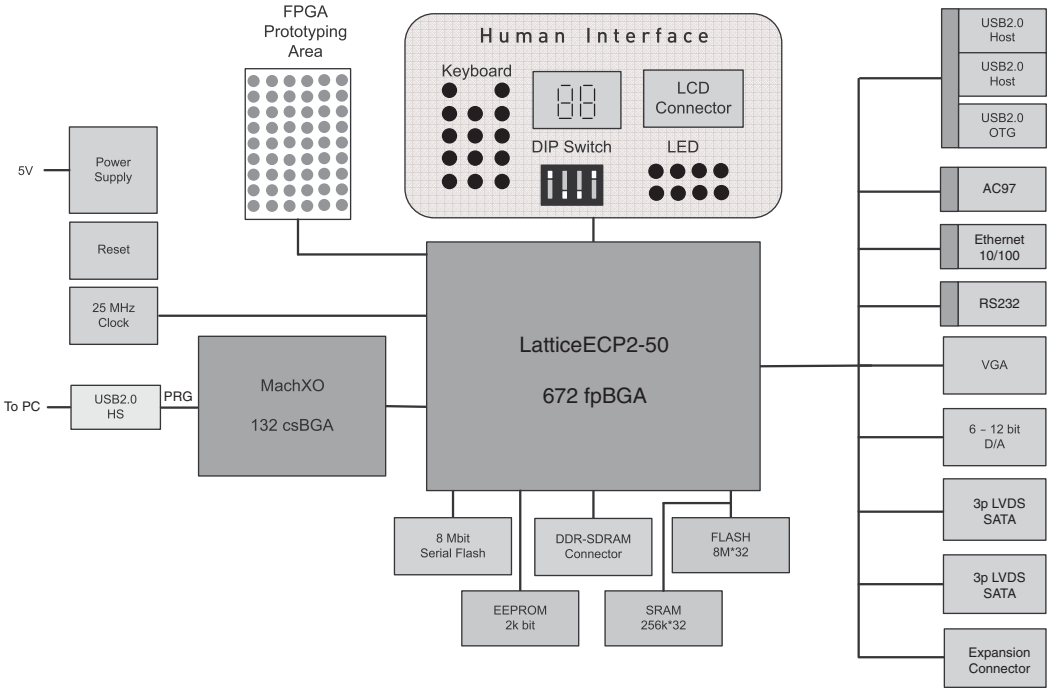


Table 1. Board Defaults

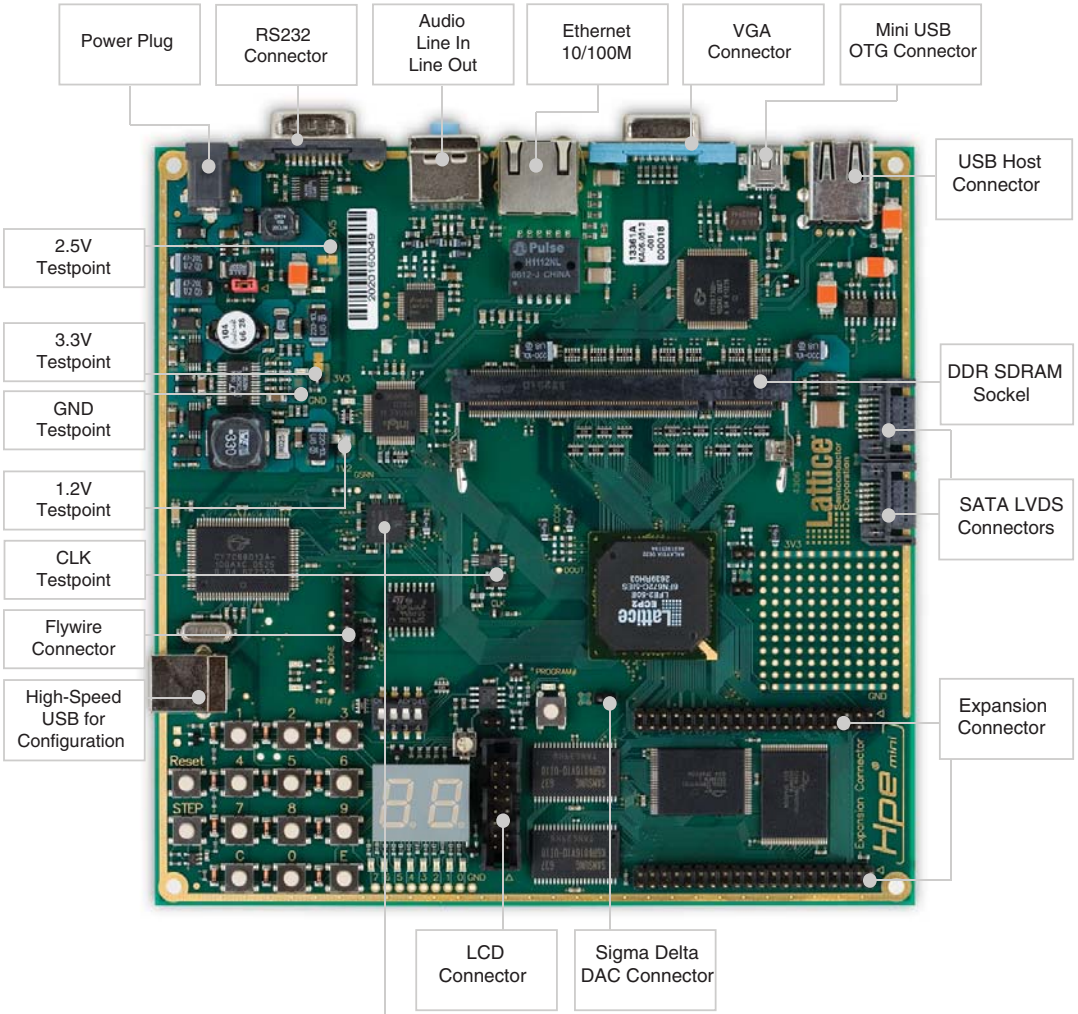
Item	Type	Default Status	Comments
LatticeECP2-50	FPGA	Programmed	The bitstream is based on Example PlatformA and the LED7SegsTest_ecp2 project. The LED7SegsTest_ecp2.mem and LED7SegsTest_ecp2.bit files are included in the LED7SegsTest_ecp2 project. Visual indications of operation are: • Left to Right and Right to Left scanning of the 8 LEDs. • Upcount and roll over of the 7 segment displays from 0 to 99 decimal at ~1 second intervals.
LCD Backlight (X5)	Jumper	Open	Backlight is off.
Configuration Switch	TMS Switch	Off (Down)	LatticeECP2-50 FPGA can be programmed.
Sigma Delta DAC Converter	Jumper	Open	
Contrast Control	Reostat	Variable	Not set to any specific level.
4-place DIP - Logic 1	Switch	Off	Logic 0 on selected pins - see Table 18.
SODIMM DDR 400 Setting (X18)	Jumper	Shorts Pins 1 and 2	Set to below DDR400 memory use.

Peripheral Interfaces

This section describes all peripheral interfaces of the LatticeMico32/DSP Development Board for LatticeECP2 in alphabetical order.

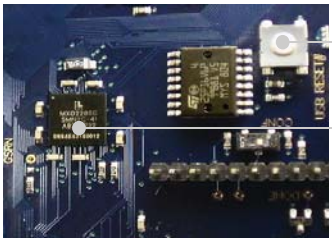
Figure 2 shows the position of peripheral interfaces available on the board.

Figure 2. Peripheral Interfaces (Version 1 Board Shown in this Figure)



In Version 2 of this board, the on-board USB cable circuit has been updated.

1. A USB RESET# pushbutton has been added. The Version 1 board includes a single Reset pushbutton that resets both the LatticeECP2 FPGA and the USB cable. The addition of the USB RESET# button allows the FPGA to be reset independent from the USB cable circuit.



2. In the Version 2 board, the MachXO device has been changed from a MachXO640 to a MachXO2280 device.

Audio Interface

The audio interface has two connectors for 3.5 mm stereo jacks. The upper one is for line-out, the lower for line-in. They are connected to the audio codec LM4549B by National Semiconductor.

Table 2. Audio Codec U1001 Pin Definitions

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
6	AC97_BITCLK	B24	47	AC97_EAPD	C23
2	AC97_EXT_CLK	D25	11	AC97_RESET#	B25
8	AC97_SDATA_IN	C26	5	AC97_SDATA_OUT	C25
10	AC97_SYNC	D24			

Detailed information on the audio codec can be found at the National Semiconductor website at www.national.com.

Clock Sources

A 25MHz oscillator supplies the FPGA (pin AD15), the CPLD (pin A8), the Ethernet controller and the Expansion Connector (pin 29 of X12). The frequency can be measured via testpoint CLK. To generate other clock frequencies use the PLLs of the FPGA. You can find detailed information on the usage of the PLLs on the Lattice website and in the LatticeECP2/M Family Data Sheet.

The USB controller requires a 24MHz quartz for configuration. Another 12MHz quartz supplies the USB host/peripheral controller.

Note: Since the Ethernet controller demands a 25MHz clock, no other basic clock can be used. Use the PLLs of the FPGA to generate custom frequencies.

DDR SODIMM Socket for DDR SDRAM Modules

The board includes a standard DDR1 SODIMM socket with 200 contacts (DDR SDRAM Module is not included). The upper four bytes of the data bus (D[63:32]) are not connected. Thus, only half of the capacity of the memory module is available.

The DDR SODIMM socket is factory configured to provide a regulated 2.5V. DDR400 modules require a power supply of 2.6V (±0.1V). Using a jumper on connector X21 (below the 5V power supply jack), the DDR power supply can be changed to suit the needs of DDR400 modules.

Note: If you want to use the DDR SDRAM interface with a 16-bit data bus, provide your HDL design with an additional input port that is assigned to pin P9 of bank 6 (connected to schematic net DDR_VREF).

Do not use this signal in your design. Deactivate the internal pull-up of the pin in the ispLEVER software. It safeguards the DDR RAM memory from getting an incorrect supply voltage which will happen when the pin is unused at a data bus width of 16 bits.

When using a 32-bit data bus, you do not have to assign this pin—ispLEVER will take care of it automatically.

Table 3. DDR SODIMM Socket (X4) - Data Bus

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
11	DDR_DQS0	AE6	47	DDR_DQS2	AB3
12	DDR_DM0	AF6	48	DDR_DM2	AB2
5	DDR_DQ0	AD9	41	DDR_DQ16	AE2
7	DDR_DQ1	AD4	43	DDR_DQ17	AD1
13	DDR_DQ2	Y5	49	DDR_DQ18	AD2
17	DDR_DQ3	AD8	53	DDR_DQ19	AD3
6	DDR_DQ4	AC8	42	DDR_DQ20	AC1
8	DDR_DQ5	AB8	44	DDR_DQ21	AC2
14	DDR_DQ6	AF7	50	DDR_DQ22	Y5
18	DDR_DQ7	AE7	54	DDR_DQ23	Y6
25	DDR_DQS1	AA6	61	DDR_DQS3	T1
26	DDR_DM1	AB6	62	DDR_DM3	T2
19	DDR_DQ8	AF5	55	DDR_DQ24	V1
23	DDR_DQ9	AE5	59	DDR_DQ25	U1
29	DDR_DQ10	AD5	65	DDR_DQ26	P4
31	DDR_DQ11	AC5	67	DDR_DQ27	P5
20	DDR_DQ12	AF4	56	DDR_DQ28	P6
24	DDR_DQ13	AE4	60	DDR_DQ29	N3
30	DDR_DQ14	AD4	66	DDR_DQ30	N4
32	DDR_DQ15	AC4	68	DDR_DQ31	N5

Table 4. DDR SODIMM Socket (X4) - Address Bus

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
112	DDR_A0	AD10	111	DDR_A1	AD14
110	DDR_A2	AB12	109	DDR_A3	AC12
108	DDR_A4	AD12	107	DDR_A5	AB13
106	DDR_A6	AC13	105	DDR_A7	AD13
102	DDR_A8	AB15	101	DDR_A9	AB14
115	DDR_A10	AC10	100	DDR_A11	AC14
99	DDR_A12	AD14	123	DDR_A13	AB10
117	DDR_BA0	AD7	116	DDR_BA1	AC7

Table 5. DDR SODIMM Socket (X4) - Other Signals

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
35	DDR_CK0+	AE12	37	DDR_CK0-	AF12
160	DDR_CK1+	Y1	158	DDR_CK1-	AA2
96	DDR_CKE0	AF11	95	DDR_CKE1	AF10
118	DDR_RAS#	AE9	119	DDR_WE#	AE10
120	DDR_CAS#	AF9	121	DDR_S0#	AF8
122	DDR_S1#	AE8			

Ethernet Interface

An Intel LXT971A is included for Ethernet PHY. This is an IEEE-compliant Fast Ethernet PHY Transceiver that directly supports both 100BASE-TX and 10BASE-T applications, full and half duplex. For more information, please refer to the data sheet of this component.

Each board has its own unique MAC address so that no conflicts with other components in the network will occur. Specify this MAC address for synthesis of Ethernet designs. It can be found on the sticker at the bottom side of your board.

Table 6. Ethernet Controller U0801 Pin Definition

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
4	HPE_RESOUT#	AE24	42	ETH_MDIO	N25
43	ETH_MDC	M26	45	ETH_RXD3	W25
46	ETH_RXD2	W26	47	ETH_RXD1	Y26
48	ETH_RXD0	AA26	49	ETH_RXDV	R25
52	ETH_RXCLK	L26	53	ETH_RXER	P26
54	ETH_TXER	U26	55	ETH_TXEN	R26
56	ETH_TXCLK	L25	57	ETH_TXD0	V26
58	ETH_TXD1	V25	59	ETH_TXD2	V24
60	ETH_TXD3	V23	62	ETH_COL	P25
63	ETH_CRS	N26	64	ETH_MDINTR#	W24

Expansion Connector

The expansion connector provides 46 user I/Os connected to the FPGA. The remaining pins serve as power and clock supplies for expansion boards. The expansion connector is configured as two 2x20 100mil centered pin headers (X12 and X13). Tables 7 and 8 describe the connections to the FPGA.

Table 7. Expansion Connector X13

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
1	GND	—	2	NC (coding)	—
3	VCC2V5	—	4	EXPCON_IO29	H4
5	EXPCON_IO30	H5	6	EXPCON_IO31	H6
7	EXPCON_IO32	H7	8	EXPCON_IO33	H8
9	EXPCON_IO34	G1	10	EXPCON_IO35	G2
11	EXPCON_IO36	G3	12	EXPCON_IO37	G4
13	EXPCON_IO38	F1	14	EXPCON_IO39	F2
15	EXPCON_IO40	F5	16	EXPCON_IO41	F6
17	EXPCON_IO42	E1	18	EXPCON_IO43	E2
19	EXPCON_IO44	E3	20	EXPCON_IO45	E4
21	VCC5V0	—	22	GND	—
23	VCC2V5	—	24	GND	—
25	VCC3V3	—	26	GND	—
27	VCC3V3	—	28	GND	—
29	EXPCON_OSC	—	30	GND	—
31	EXPCON_CLKIN	—	32	GND	—
33	EXPCON_CLKOUT	—	34	GND	—
35	VCC3V3	—	36	GND	—

Table 7. Expansion Connector X13 (Continued)

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
37	VCC3V3	—	38	GND	—
39	VCC3V3	—	40	GND	—

Table 8. Expansion Connector X14

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
1	HPE_RESET#	—	2	GND	—
3	EXPCON_IO0	R1	4	EXPCON_IO1	R2
5	EXPCON_IO2	P1	6	EXPCON_IO3	P2
7	EXPCON_IO4	N1	8	EXPCON_IO5	M6
9	EXPCON_IO6	L2	10	EXPCON_IO7	L5
11	EXPCON_IO8	L6	12	EXPCON_IO9	L7
13	EXPCON_IO10	L8	14	EXPCON_IO11	K1
15	EXPCON_IO12	K2	16	EXPCON_IO13	K3
17	EXPCON_IO14	K4	18	EXPCON_IO15	K5
19	GND	—	20	VCC3V3	—
21	EXPCON_IO16	K6	22	GND	—
23	EXPCON_IO17	K7	24	GND	—
25	EXPCON_IO18	K8	26	GND	—
27	EXPCON_IO19	J1	28	EXPCON_IO20	J2
29	EXPCON_IO21	J3	30	GND	—
31	EXPCON_IO22	J4	32	EXPCON_IO23	J5
33	EXPCON_IO24	J8	34	GND	—
35	EXPCON_IO25	J9	36	EXPCON_IO26	H1
37	EXPCON_IO27	H2	38	CARDSEL#	D1
39	EXPCON_IO28	H3	40	GND	—

ispDOWNLOAD Cable Connector

There are two ways to configure the programmable Lattice devices on the board. The USB connector requires a standard USB cable, and is described later in this document. Connector X3 is available to connect a Lattice ispDOWNLOAD cable. An ispDOWNLOAD cable is used to program IEEE 1532 compliant programmable devices. Lattice provides either a parallel port or a USB port download cable. The FPGA and CPLD are programmed using the cable and ispVM® programming software.

Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeECP2 FPGA device and render the board inoperable.*

DIP switch SW0302[1] controls the device to be configured: the FPGA or the MachXO. If it is on (in top position), the MachXO is selected; if off, the FPGA is selected.

The ispVM System software can be downloaded from the Lattice web site at: www.latticesemi.com/ispvm.

Note: Do not change the switch when the configuration of a device is in progress!

1. Caption on the board: CONF.

Note: The board as configured from the factory, has a built-in USB ispDOWNLOAD cable. The built-in cable and an external ispDOWNLOAD cable cannot be used at the same time. Doing so may damage the board.

Table 9. ispDOWNLOAD Connector X4 Pin Definition

Pin	Signal Name	Pin	Signal Name
1	VCC3V3	2	JTAG_TDO
3	JTAG_TDI	4	JTAG_PROG
5	JTAG_TRST	6	JTAG_TMS
7	GND	8	JTAG_TCK
9	JTAG_DONE	10	JTAG_INIT

LCD Connector (Optional)

The LCD connector is a 16-pin header with a standard pinning for LCD modules with back-light (e.g. Truly MTC-C202DPRN-1N). In order to use an LCD module, attach it to the connector via a 16-pin ribbon cable.

Note: The LCD module is tied to a 5V supply. The LatticeECP2-50 to LCD interface is 3.3V.

Put a jumper on connector X6 to turn on the backlight of the LCD. The contrast of the LCD module is adjustable with the potentiometer R0526, because different LCD modules need different voltages for the best contrast.

Figure 3. LCD Panel (Not Included)

Table 10. LCD Connector X6 Pin Definition

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
1	GND	—	2	VCC5V	—
3	CONTRAST	—	4	LCD_REGSEL	K24
5	LCD_RW	J24	6	LCD_ENABLE	J22
7	SEG_A#	M24	8	SEG_B#	N23
9	SEG_C#	M22	10	SEG_D#	M21
11	SEG_E#	M20	12	SEG_F#	L22
13	SEG_G#	L21	14	SEG_DP#	K22
15	BACKLIGHT	—	16	GND	—

SATA Interfaces

Find the jacks X15 and X16 for connecting SATA cables on the right side of the board. This provides a convenient method for evaluating or using LVDS signals with the FPGA. This board does not support implementation of a full SATA solution. These SATA jacks have differential nets with high-speed signals connected to them. See Table 11 for SATA pinning information. The positive signal is connected with a plus (+), the negative with a minus (-). Every differential signal pair can act as receiver or transmitter depending on the configuration of the FPGA.

Table 11. SATA Jacks X15 (Left Column) and X16 (Right Column) Pin Definition

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
2	SATA_X1D0+	M4	2	SATA_X2D0+	U3
3	SATA_X1D0-	M5	3	SATA_X2D0-	U4
5	SATA_X1D1+	P3	5	SATA_X2D1+	V2
6	SATA_X1D1-	R3	6	SATA_X2D1-	W2

Serial Interface

The board includes an RS232 serial interface port. The interface provides transmit (TX), receive (RX), and hardware handshaking. The Maxim MAX3232 data sheet provides detailed information on the interface circuit. A 9-pin female to 9-pin female null modem cable is required.

Table 12. Serial Interface X9 Pin Definition

Sub-D Pin	Signal	FPGA Pin	Direction	RS232 Function
3	RS_TXD_LVTTL	K26	Out	Transmit Data
7	RS_RTS_LVTTL	K25	Out	Request to Send
2	RS_RXD_LVTTL	J25	In	Receive Data
8	RS_CTS_LVTTL	J26	In	Clear to Send

Sigma Delta D/A Converter

The board includes a low-pass filter connected to a dedicated pin (C14) of the FPGA. With this, a sigma delta converter can be realized. Great results can be achieved by using a resolution of 8 to 10 bits. Example VHDL code is provided.

Power Supply

Four different voltages are needed: 3.3V I/O voltage, 2.5V DDR and LVDS voltages as well as 1.2V core voltage. The 3.3V supply draws up to 1A, the 2.5V and 1.2V supplies up to 2A of current.

For more information, see the power supply information in the Components section of this document.

Test Points

In order to check the various voltage levels used, several test points are provided. There is one test point for 1.2V, 2.5V, 3.3V, one for ground, and one for accessing the 25MHz oscillator. The 25MHz clock signal can be checked with another test point.

USB Host/Peripheral Interface

There are one mini USB OTG and two USB host connectors on board. These are connected to the Cypress CY7C67300 USB Host/Peripheral Controller U0702. This controller is compliant with the Universal Serial Bus Specification 2.0. You can transmit and receive serial data at both full-speed (12 Mbps) and low-speed (1.5 Mbps) data rates. For more information, please refer to the data sheet of the USB controller. U0703 and U0704 are USB power control switches, which must be enabled by the user via the USB PWEN signals. The USB OC signal pulls low to indicate voltage, current and thermal issues.

Table 13. USB GPIO Connections (U0702)

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
94	USB_GPIO0	AE20	93	USB_GPIO1	AC18
92	USB_GPIO2	AE13	91	USB_GPIO3	AB20
90	USB_GPIO4	AA20	89	USB_GPIO5	AF19
87	USB_GPIO6	AE19	86	USB_GPIO7	AD19

Table 13. USB GPIO Connections (U0702) (Continued)

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
66	USB_GPIO8	AC19	65	USB_GPIO9	AB19
61	USB_GPIO10	AA19	60	USB_GPIO11	AF18
59	USB_GPIO12	AE18	58	USB_GPIO13	AD18
57	USB_GPIO14	AC18	56	USB_GPIO15	AB18
55	USB_GPIO16	AF17	54	USB_GPIO17	AE17
53	USB_GPIO18	AD17	52	USB_GPIO19	AC17
50	USB_GPIO20	AB17	49	USB_GPIO21	AF16
48	USB_GPIO22	AE16	47	USB_GPIO23	AF15
46	USB_GPIO24	AE15	45	USB_GPIO25	AF14
44	USB_GPIO26	AE14	43	USB_GPIO27	AF13
42	USB_GPIO28	AE13	41	USB_GPIO29	-

Table 14. Additional USB GPIO Connections (U0702, U0704, and U0704)

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
U0703:1	USB_PWEN0	Y17	U0703:2	USB_OC0#	AA16
U0703:4	USB_PWEN1	Y16	U0703:3	USB_OC1#	Y20
U0704:1	USB_PWEN2	AA21	U0704:2	USB_OC2#	Y19
U0702:85	HPE_RESOUT#	AE24			

USB Configuration Connector

In addition to the ispDOWNLOAD connector, the FPGA and the MachXO can also be configured by a standard USB connection. The USB target connector is wired to the Cypress CY7C68013A device (U0301).

This programming method requires the use of the ispVM System software. This can be downloaded from the Lattice web site at: www.latticesemi.com/ispvm.

This connection will appear to the ispVM System software as if a regular USB-based ispDOWNLOAD cable is connected to the PC.

The CY7C68013A in combination with the MachXO CPLD acts as a built-in ispDOWNLOAD cable. The MachXO is connected to the ispDOWNLOAD Connector X3, and can program the LatticeECP2-50. The LatticeECP2-50 can be programmed when DIP switch SW0302 is 'off' (pushed down).

Note: Like the ispDOWNLOAD connector, the MachXO drives the JTAG signals when it is programmed for USB configuration. Only use the built-in ispDOWNLOAD cable or an external ispDOWNLOAD cable exclusively. It is not recommended to switch between cables without first power cycling the board. Failure to follow this recommendation may cause unpredictable results and may possibly damage the board.

Table 15. Connections Between the USB Controller (CY7C68013A) and the MachXO

Cypress Pin	Signal Name	MachXO Pin	Cypress Pin	Signal Name	MachXO Pin
34	GP_D0	G14	35	GP_D1	N14
36	GP_D2	H14	37	GP_D3	H13
44	GP_D4	H12	45	GP_D5	J13
46	GP_D6	J12	47	GP_D7	K14
80	GP_D8	K13	81	GP_D9	K12
82	GP_D10	L14	83	GP_D11	M13
95	GP_D12	M14	96	GP_D13	M12

Table 15. Connections Between the USB Controller (CY7C68013A) and the MachXO (Continued)

Cypress Pin	Signal Name	MachXO Pin	Cypress Pin	Signal Name	MachXO Pin
97	GP_D14	N14	98	GP_D15	N13
57	GP_ADR0	H1	58	GP_ADR1	H2
59	GP_ADR2	J1	60	GP_ADR3	J3
61	GP_ADR4	K1	62	GP_ADR5	K2
63	GP_ADR6	L1	64	GP_ADR7	L3
93	GP_ADR8	M1	69	GP_SLOE	M3
67	GP_INT0	N7	68	GP_INT1	M6
71	GP_FIFOADR0	M4	72	GP_FIFOADR1	N4
70	GP_WU2	N3	73	GP_PKTEND	P5
74	GP_SLCS#	G3	79	USBCF_WAKE	N9
3	GP_RDY0	D3	4	GP_RDY1	E2
5	GP_RDY2	F2	6	GP_RDY3	F3
7	GP_RDY4	G1	8	GP_RDY5	G2
54	GP_CTL0	D1	55	GP_CTL1	C3
56	GP_CTL2	C2	51	GP_CTL3	C1
52	GP_CTL4	B2	76	GP_CTL5	B1
23	GP_T0	M2	24	GP_T1	N1
25	GP_T2	P1	28	GP_BKPT	F12
100	USB_CLK_O	M7	26	GP_IFCLK	M8
41	GP_RXD0	E13	40	GP_TXD0	E14
43	GP_RXD1	F13	42	GP_TXD1	F14

VGA Interface

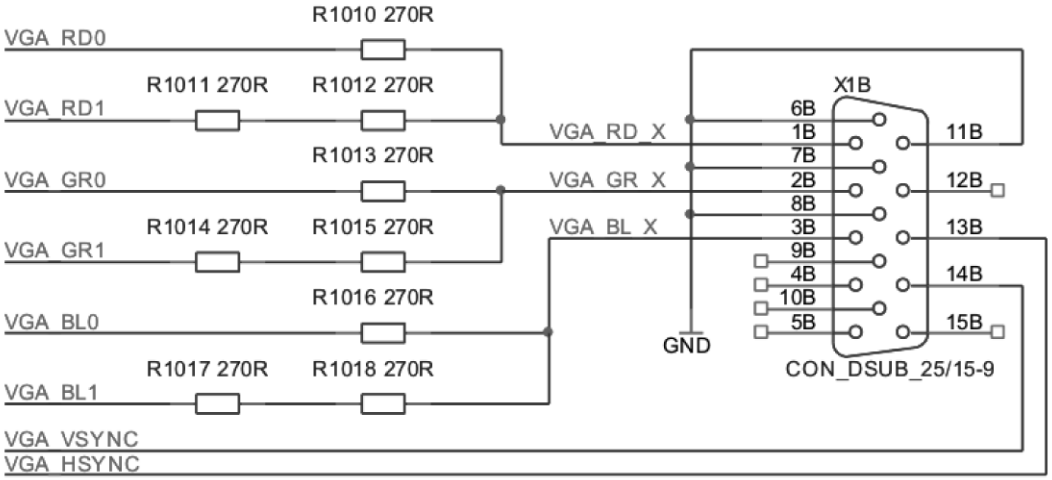
The board includes a VGA connector for driving a VGA monitor. The VGA interface is connected to a 15-pin plug socket. The pin definitions are listed in Table 16.

VGA RD0 and VGA RD1 are both connected to pin 1, but have different series resistors (see Figure 4). Thus, a 6-bit VGA interface is realized. Figure 4 shows the connection of the RGB signals. The FPGA is responsible for generating correct HSYNC and VSYNC sweep frequencies. Understand the SYNC frequencies of the VGA monitor being connected to the VGA plug and adjust the FPGA frequencies as required.

Table 16. VGA Connector X1B Pin Definition, n.c. ... Not Connected

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
1	VGA_RD0	AF24	1	VGA_RD1	AE23
2	VGA_GR0	AF23	2	VGA_GR1	AE22
3	VGA_BL0	AF22	3	VGA_BL1	AE21
4	n.c.	—	5	n.c.	—
6	GND	—	7	GND	—
8	GND	—	9	n.c.	—
10	GND	—	11	n.c.	—
12	n.c.	—	13	VGA_HSYNC	AF20
14	VGA_VSYNC	AF21	15	n.c.	—

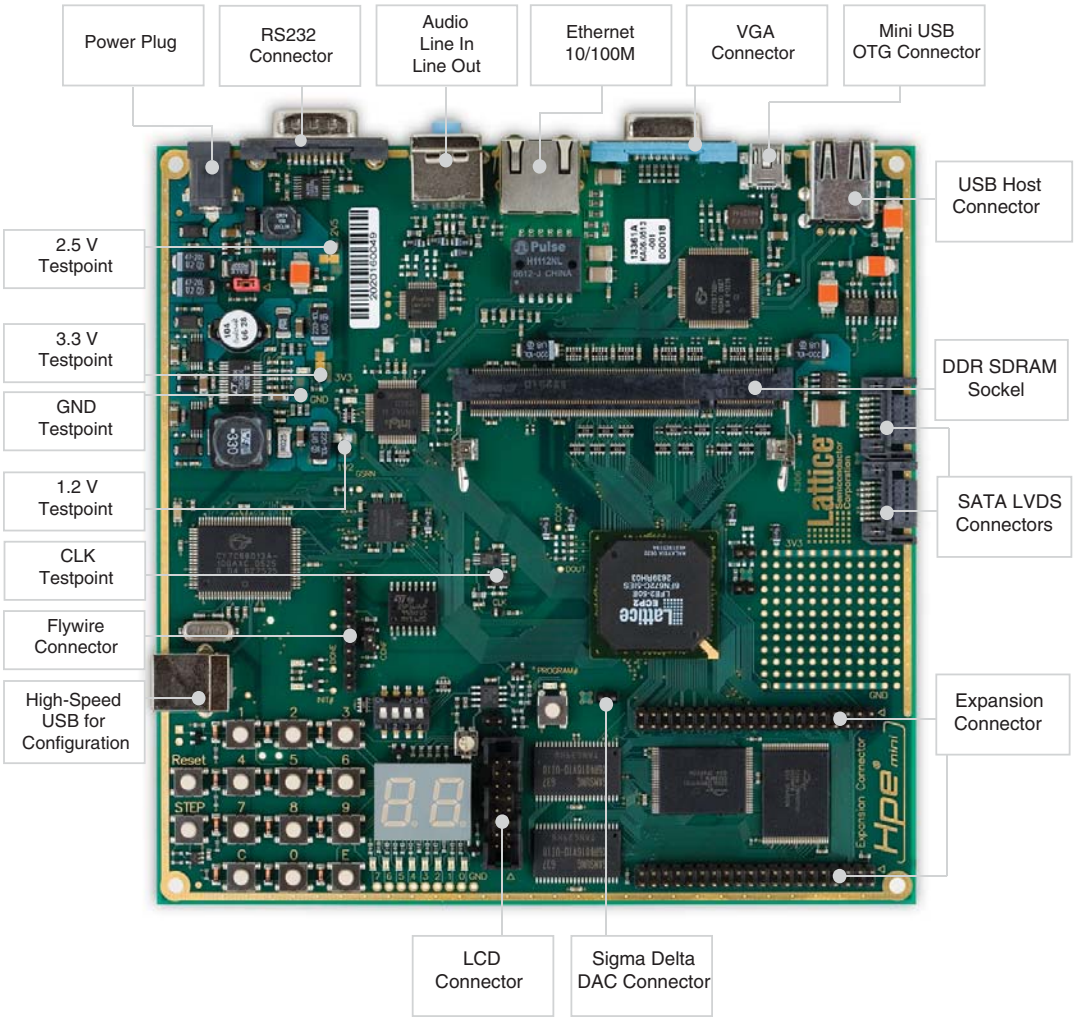
Figure 4. VGA Connector



User Interface

Figure 5 shows the position of the user interface elements.

Figure 5. User Interface Features (Version 1 Board Shown in this Figure)



7-Segment Display

The 7-segment display is wired as follows:

Table 17. 7-Segment Display U0502 Pin Definition

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
A	SEG_A#	M24	E	SEG_E#	M20
B	SEG_B#	N23	F	SEG_F#	L22
C	SEG_C#	M22	G	SEG_G#	L21
D	SEG_D#	M21	DP	SEG_DP#	K22
right	SEG_CA0#	K21	left	SEG_CA1#	K20

The signals of the 7-segment display are low-active, which means that with a logic '0', the segment is lit. SEG A# ... SEG F# and SEG DP# drive not only the two 7-segment displays, but also the LCD. To write different data to these three components, the user must drive the signals alternately to the components. This can be realized with the signals SEG CA0#, SEG CA1# and LCD ENABLE. They serve to activate the two 7-segment displays and the LCD, respectively.

DIP Switches

There is a 4-bit DIP switch on the board. When the switch is turned to the on position, a logic '1' will be seen. The connections are in Table 18.

Table 18. DIP Switches SW0514 Connection

Switch	Signal Name	FPGA Pin	Switch	Signal Name	FPGA Pin
SW315			**SW316**		
1	DSW0	F26	2	DSW1	F25
3	DSW2	E26	4	DSW3	E25

LEDs

Eight LEDs can be used for custom status signaling. They are low-active; with a logic '0' the LED is on. You can control the LEDs via the signals below.

Table 19. LED LD0501 ... LD0508 Connection

Pin	Signal Name	FPGA Pin	Pin	Signal Name	FPGA Pin
1	LED0#	R24	5	LED4#	P23
2	LED1#	R23	6	LED5#	P22
3	LED2#	R22	7	LED6#	P21
4	LED3#	R21	8	LED7#	N22

Key Matrix

The board also features a key matrix with 12 push-buttons, which are not debounced. They must be driven with three column lines and can be read with four rows. The following table shows the connections.

Table 20. Key Matrix with the Keys SW302 ... SW313 Definition

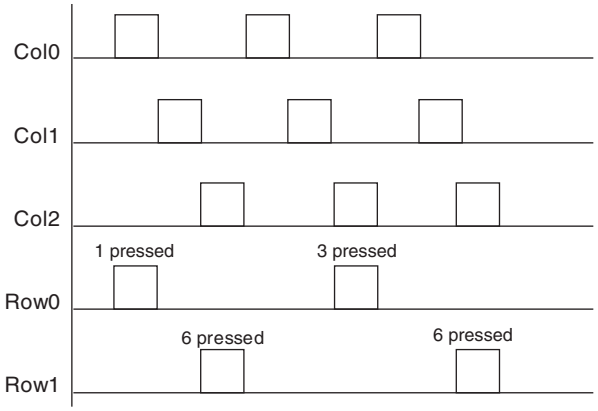
Signal Name	TST_COL0	TST_COL1	TST_COL2
TST_ROW0	1	2	3
TST_ROW1	4	5	6
TST_ROW2	7	8	9
TST_ROW3	C	0	E

Table 21. Key Matrix with the Keys SW302 ... SW313 Connection

Signal Name	FPGA Pin	Signal Name	FPGA Pin
TST_ROW0	H26	TST_COL0	G26
TST_ROW1	H25	TST_COL1	G25
TST_ROW2	H24	TST_COL2	G24
TST_ROW3	H23		

To query all keys of the matrix, you must poll the column driver signals (TST COL0, TST COL1, and TST COL2). If you press a key, a logic '1' appears in the corresponding row. The following diagram explains the functionality:

Figure 6. Polling of the Key Matrix



You do not need the polling method if only four keys are used. Connect the column driver signals of one column to VCC, the other two to GND and query the row data signals.

CPU Reset Key

The CPU reset key is a global reset. Please refer to the Reset Chip section of this document for detailed information.

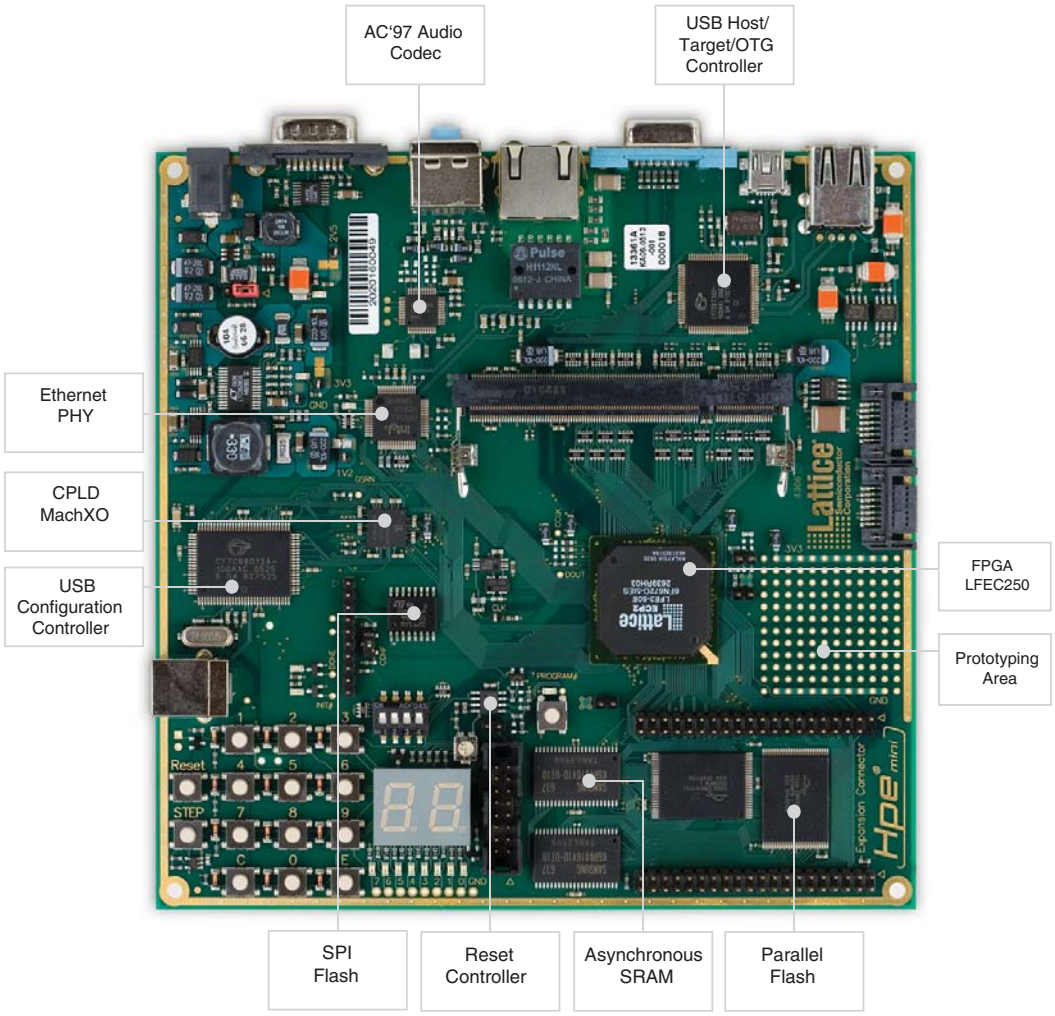
Single Step Key

The single step key is connected to a normal input of the FPGA and can be used by the application as required. This key is connected to a Schmitt trigger, meaning it is debounced. This key can be used as a single clock for testing your design.

Components

Figure 7 illustrates the position of major components.

Figure 7. Components (Version 1 board Shown in this Figure)



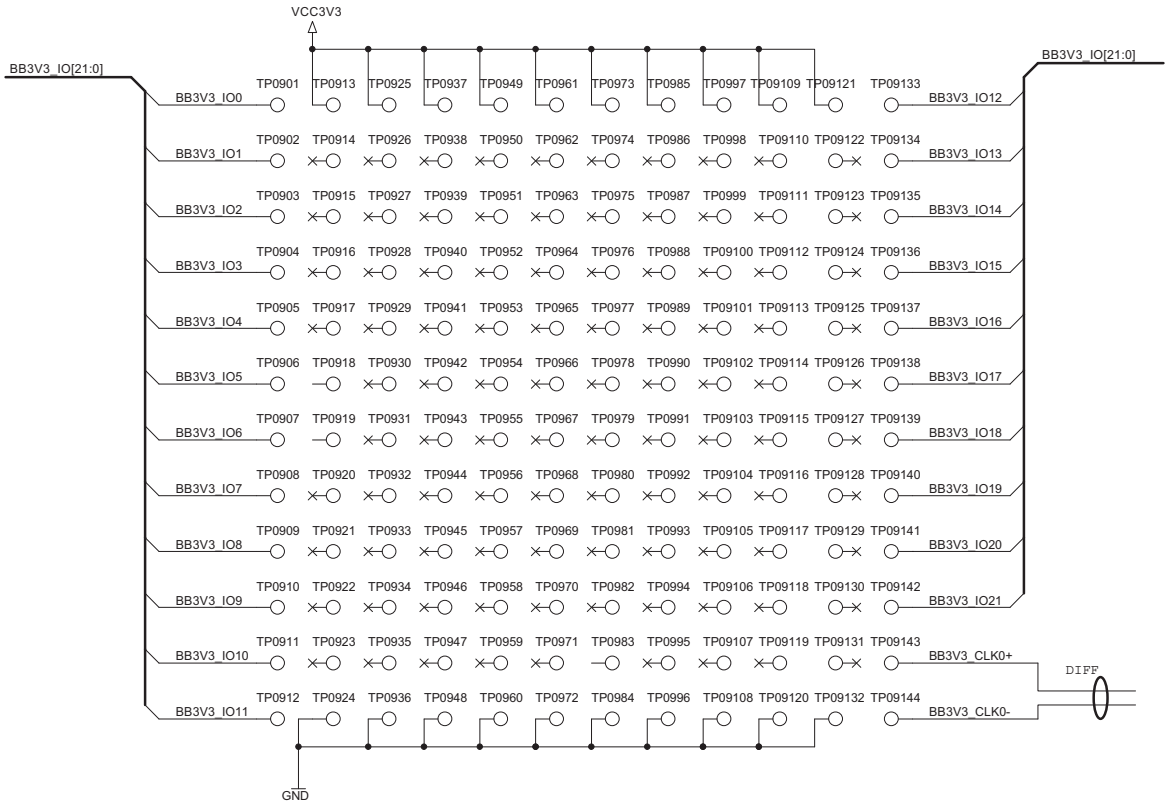
12 x 12 FPGA Prototyping Area of The FPGA

A 12x12 prototyping area is available. The lead-wire spacing of the prototyping area is 100mil (2.54 mm). Figure 8 shows the prototyping area in top view. 14 plated-through-holes on its left side are connected to the FPGA. Eight through-holes on the right side are wired to a 2.5V I/O bank. In the top row of the prototyping area there are six connections to the 3.3V power supply as well as three to 2.5V. The bottom row has ten plated-through-holes connected to GND.

Table 22. FPGA Connections for the 12x12 Prototyping Area

LRF Pin	Signal Name	FPGA Pin	LRF Pin	Signal Name	FPGA Pin
TP0901	BB3V3_IO0	A15	TP0902	BB3V3_IO1	B15
TP0903	BB3V3_IO2	C15	TP0904	BB3V3_IO3	D15
TP0905	BB3V3_IO4	A16	TP0906	BB3V3_IO5	B16
TP0907	BB3V3_IO6	E16	TP0908	BB3V3_IO7	A17
TP0909	BB3V3_IO8	B17	TP0910	BB3V3_IO9	C17
TP0911	BB3V3_IO10	D17	TP0912	BB3V3_IO11	E17
TP09133	BB3V3_IO12	A18	TP09134	BB3V3_IO13	B18
TP09135	BB3V3_IO14	C18	TP09136	BB3V3_IO15	D18
TP09137	BB3V3_IO16	E18	TP09138	BB3V3_IO17	A19
TP09139	BB3V3_IO18	B19	TP09140	BB3V3_IO19	C19
TP09141	BB3V3_IO20	D19	TP09142	BB3V3_IO21	E19
TP09143	BB3V3_CLK0+	D14	TP09144	BB3V3_CLK0-	F14
TP0913	VCC3V3	—	TP0925	VCC3V3	—
TP0937	VCC3V3	—	TP0949	VCC3V3	—
TP0961	VCC3V3	—	TP0973	VCC3V3	—
TP0985	VCC3V3	—	TP0997	VCC3V3	—
TP09109	VCC3V3	—	TP09121	VCC3V3	—
TP0924	GND	—	TP0936	GND	—
TP0948	GND	—	TP0960	GND	—
TP0972	GND	—	TP0984	GND	—
TP0996	GND	—	TP09108	GND	—
TP09120	GND	—	TP09132	GND	—

Figure 8. Schematic Illustration of the Prototyping Area



Asynchronous SRAM

The board is populated with two asynchronous K6R4016V1D SRAMs from Samsung. Each is 4 Mbit in size with a data bus width of 16 bits. They are wired as one memory with a 32-bit data bus and a depth of 256 k. The 18-bit address bus, the data bus and the control signals are connected directly to the FPGA. The 18-bit address bus, named MEMORY_A0 through MEMORY_A17, addresses word (4 bytes) locations.

Table 23. Address Signals of the Asynchronous SRAM Chips U0404 and U0405

SRAM Pin	Signal Name	FPGA Pin	SRAM Pin	Signal Name	FPGA Pin
1	MEMORY_A0	C1	2	MEMORY_A1	B2
3	MEMORY_A2	C2	4	MEMORY_A3	A3
5	MEMORY_A4	B3	18	MEMORY_A5	C3
19	MEMORY_A6	D3	20	MEMORY_A7	A4
21	MEMORY_A8	B4	22	MEMORY_A9	C4
23	MEMORY_A10	D4	24	MEMORY_A11	A5
25	MEMORY_A12	B5	26	MEMORY_A13	C5
27	MEMORY_A14	D5	42	MEMORY_A15	E5
43	MEMORY_A16	A6	44	MEMORY_A17	B6

Table 24. Data Signals of the Asynchronous SRAM Chip U0404

SRAM Pin	Signal Name	FPGA Pin	SRAM Pin	Signal Name	FPGA Pin
7	MEMORY_DQ0	E7	8	MEMORY_DQ1	F7
9	MEMORY_DQ2	G7	10	MEMORY_DQ3	A8
13	MEMORY_DQ4	B8	14	MEMORY_DQ5	C8
15	MEMORY_DQ6	D8	16	MEMORY_DQ7	E8
29	MEMORY_DQ8	F8	30	MEMORY_DQ9	G8
31	MEMORY_DQ10	A9	32	MEMORY_DQ11	B9
35	MEMORY_DQ12	C9	36	MEMORY_DQ13	D9
37	MEMORY_DQ14	E9	38	MEMORY_DQ15	A10

Table 25. Data Signals of the Asynchronous SRAM Chip U0405

SRAM Pin	Signal Name	FPGA Pin	SRAM Pin	Signal Name	FPGA Pin
7	MEMORY_DQ16	B10	8	MEMORY_DQ17	C10
9	MEMORY_DQ18	D10	10	MEMORY_DQ19	E10
13	MEMORY_DQ20	F10	14	MEMORY_DQ21	G10
15	MEMORY_DQ22	A11	16	MEMORY_DQ23	B11
29	MEMORY_DQ24	E11	30	MEMORY_DQ25	F11
31	MEMORY_DQ26	G11	32	MEMORY_DQ27	C12
35	MEMORY_DQ28	D12	36	MEMORY_DQ29	E12
37	MEMORY_DQ30	F12	38	MEMORY_DQ31	G12

Table 26. Control Signals of the Asynchronous SRAM Chips U0404 and U0405

SRAM Pin	Signal Name	FPGA Pin	SRAM Pin	Signal Name	FPGA Pin
SRAM	Pin	Signal	Name	FPGA	Pin
17	MEMORY_WE#	C13	41	MEMORY_OE#	D13
39	SRAM_BE0#	F13	40	SRAM_BE1#	G13
6	SRAM_CE#	E13			

MachXO

The LCMXO640 is a non-volatile, instant-on, reprogrammable logic device. It supports "background programming" called TransFR™ (i.e., the device can be programmed while in operation).

The MachXO comes preprogrammed from the factory. The factory program permits the CY7C68013A/MachXO combination to work as a built-in USB ispDOWNLOAD cable. Using ispVM software the built-in download cable permits the FPGA, and SPI PROM, to be programmed. It is not recommended for the MachXO to be reprogrammed. However, the MachXO does provide some connections to the LatticeECP2-50 FPGA, and to an 8x6 prototyping area.

For further information, please consult the MachXO Family Data Sheet.

Table 27. Interface Between the MachXO and the FPGA

CPLD Pin	Signal Name	FPGA Pin	CPLD Pin	Signal Name	FPGA Pin
A1	MACHXO_IO0	A20	A2	MACHXO_IO1	A23
A3	MACHXO_IO2	C20	B3	MACHXO_IO3	D20
A4	MACHXO_IO4	E20	C4	MACHXO_IO5	A21
A5	MACHXO_IO6	B21	B5	MACHXO_IO7	E21
A6	MACHXO_IO8	A22	B6	MACHXO_IO9	B22
B10	MACHXO_IO10	C22	A11	MACHXO_IO11	D22
A12	MACHXO_IO12	A23	B12	MACHXO_IO13	B23
A13	MACHXO_IO14	E23	A14	MACHXO_IO15	A24
C8	MACHXO_CLK0	H13	B8	MACHXO_CLK0	H13

FPGA

The LatticeECP2-50 FPGA represents the heart of the board. It has the following features:

- 48 k Look-Up Tables (LUTs)
- 96 kbit of distributed RAM
- 387 kbit of EBR SRAM
- 21 EBR SRAM blocks
- 18 sysDSP blocks
- 72 18 x 18 multipliers
- 6 PLLs: 2 GPLLs, 2 SPLLs, 2 GDLLs
- 500 user I/Os
- DDR memory support (DDR1-400, DDR2-400)
- Supported I/O standards: LVCMOS, LVTTL, SSTL, HSTL, LVDS, PCI, differential
- HSTL, differential SSTL, RSDS, Bus LVDS, MLVDS, LVPECL

The ispLEVER design software can be used to develop/modify programs for the FPGA using Verilog or VHDL design entry methods. For more information on the ispLEVER software, see www.latticesemi.com/software.

Sample programs for the FPGA are available on-line as well. These can be found at www.latticesemi.com/boards. Select **FPGA/FPSC Boards -> LatticeMico32/DSP Development board for LatticeECP2** and click on the **Design Files** link.

For further information please consult the LatticeECP2/M Family Data Sheet.

Parallel Flash

Two parallel MX29LV128MBTI-90Q Flash components from Macronics (or equivalents) are provided on the board for program code and data. As with the SRAM, a 32-bit data bus is realized with these two devices. Thus, Flash can be accessed as a 8Mx32 memory. The 23-bit address bus, the data bus and the control signals are connected directly to the FPGA. The 23-bit address bus, named MEMORY_A0 through MEMORY_A22, addresses word (4 bytes) locations.

Note: The LatticeMico32/DSD Development Board generates byte enable outputs at the top-level HDL module. The board does not use these outputs, which causes ispLEVER to generate some warning messages. The warnings correctly tell the user that these pins are not connected or assigned to any location. The warnings can be avoided by either commenting out these byte enable outputs, or assigning them to unused I/O.

Table 28. Address Signals of the Flash Chips U0402 and U0403

Flash Pin	Signal Name	FPGA Pin	Flash Pin	Signal Name	FPGA Pin
31	MEMORY_A0	C1	26	MEMORY_A1	B2
25	MEMORY_A2	C2	24	MEMORY_A3	A3
23	MEMORY_A4	B3	22	MEMORY_A5	C3
21	MEMORY_A6	D3	20	MEMORY_A7	A4
10	MEMORY_A8	B4	9	MEMORY_A9	C4
8	MEMORY_A10	D4	7	MEMORY_A11	A5
6	MEMORY_A12	B5	5	MEMORY_A13	C5
4	MEMORY_A14	D5	3	MEMORY_A15	E5
54	MEMORY_A16	A6	19	MEMORY_A17	B6
18	MEMORY_A18	E6	11	MEMORY_A19	A7
12	MEMORY_A20	B7	15	MEMORY_A21	C7
2	MEMORY_A22	D7			

Table 29. Data Signals of the Flash Chip U0402

Flash Pin	Signal Name	FPGA Pin	Flash Pin	Signal Name	FPGA Pin
35	MEMORY_DQ0	E7	37	MEMORY_DQ1	C9
39	MEMORY_DQ2	A11	41	MEMORY_DQ3	F12
44	MEMORY_DQ4	B8	46	MEMORY_DQ5	C8
48	MEMORY_DQ6	D8	50	MEMORY_DQ7	E8
36	MEMORY_DQ8	F8	38	MEMORY_DQ9	G8
40	MEMORY_DQ10	A9	42	MEMORY_DQ11	B9
45	MEMORY_DQ12	C9	47	MEMORY_DQ13	D9
49	MEMORY_DQ14	E9	51	MEMORY_DQ15	A10

Table 30. Data Signals of the Flash Chip U0403

Flash Pin	Signal Name	FPGA Pin	Flash Pin	Signal Name	FPGA Pin
35	MEMORY_DQ16	B10	37	MEMORY_DQ17	C10
39	MEMORY_DQ18	D10	41	MEMORY_DQ19	E10
44	MEMORY_DQ20	F10	46	MEMORY_DQ21	G10
48	MEMORY_DQ22	A11	50	MEMORY_DQ23	B11
36	MEMORY_DQ24	E11	38	MEMORY_DQ25	F11
40	MEMORY_DQ26	G11	42	MEMORY_DQ27	C12
45	MEMORY_DQ28	D12	47	MEMORY_DQ29	E12
49	MEMORY_DQ30	F12	51	MEMORY_DQ31	G12

Table 31. Control Signals of the Flash Chips U0402 and U0403

Flash Pin	Signal Name	FPGA Pin	Flash Pin	Signal Name	FPGA Pin
34	MEMORY_OE#	D13	13	MEMORY_WE#	C13
32	FLASH_CE#	A13	16	FLASH_WP#/ACC	A12
14	FLASH_RESET	B14	17	FLASH_RY/BY#_A	A14
53	FLASH_BYTE#	B12			

SPI Flash

The LatticeECP2-50 FPGA is an SRAM-based programmable device, and is therefore volatile. In order for it to be automatically configured upon power-up, a non-volatile 16 Mbit SPI Flash device is provided. The SPI Flash can be programmed with configuration bitstream data. The SPI Flash can be configured either through the ispDOWNLOAD connector or via the integrated USB configuration interface.

Table 32. FPGA to SPI Flash Connections

SPI Pin	Signal Name	FPGA Port Name	FPGA Direction	FPGA Pin
CS	CSSPIN	CEJ	Output	V22
CLK	CCLK	SCK	Output	NC/E19[1]
Q	SPIDO	SO	Input	W23
DI	SISPI	SI	Output	Y25
WPn	WP#	WPJ	Output	AA25 (FPGA NC)
HOLDn	HOLD#	HOLDJ	Output	AB26 (FPGA NC)

Note: The SPI CLK pin can be connected to FPGA E19. This allows the LatticeMico32 to access the SPI PROM for data retrieval/storage purposes. On revision B boards, CLK is E17.

To program the SPI Flash configuration device, use the FPGA Loader function of the ispVM System software. The FPGA Loader programming scheme provides an in-system JTAG programming method for configuration devices. The FPGA acts as a bridge between the JTAG interface and the SPI interface of the serial configuration device.

Configure the SPI Flash as follows:

1. In the ispVM System software, choose **Edit -> Add Device** to open the Device Information dialog box.
2. Click **Select** to open the Select Device dialog box. Select device family **LatticeECP2**, device **LFE2-50E**, and package **672 fpBGA** from the drop-down lists.
3. Change the Device Access Options to **SPI Flash Programming**.
4. Select Flash Device : **STMicro SPI-M25P16** and click **OK**.
5. Browse Data File: Select the ECP2-50 bitstream to program into the SPI PROM, click **OK**.
6. Click **OK** to close the SPI Serial Flash Device dialog.
7. Click **OK** to close the Device Information dialog
8. Click **GO**. The ispVM System software programs the SPI Flash via the FPGA.
9. Disconnect and then reconnect the power supply. The FPGA will take about three seconds to be programmed by the SPI Flash.

Power Supply

Power is supplied via a 2.1 mm DC power jack in the top left corner of the board. The board is protected against reversed power supply. The input supply is 5V DC.

A two-phase synchronous step-down switching regulator generates the 3.3V (1A max.) I/O voltage and the 1.2V (2A max.) core voltage.

Note: If you use a power supply other than the one included in the shipment, make sure it supplies regulated 5V.

Reset Chip

After power-up, a power surveillance chip (U0601) waits until the 5V supply and the 3.3V I/O voltage are stable. Then, after 200 ms, it drives the signal HPE RESET# (pin M25 of the FPGA) high. If you press the reset button, the supervisory circuit will generate a low on the HPE RESET# signal.

The surveillance chip has an I^2C serial 2 kbit CMOS EEPROM. The four most significant bits of the 8-bit slave address are programmable; the default being 1010. Detailed information on the reset circuit and the I^2C interface can be found in the data sheet of the Catalyst Semiconductor CAT1026.

Troubleshooting

If your board is not working properly, please follow these steps for diagnosis.

1. Check the 3.3V and 2.5V LEDs to ensure that the power supply is working correctly.
2. Make sure that the INIT LED is lit.
3. Load test program.
4. Make sure the FPGA has been configured properly (DONE LED must be lit).
5. Start test program 1.

Circuit diagrams for the localization of errors can be found in the appendix.

Electrical Specifications

Power requirement:	regulated 5V DC
Input current:	2000 mA

Mechanical Specifications

Dimensions:	160 mm [L] x 160 mm [W] x 31 mm [H]
Net weight:	160 g
Temperature range:	0 to 50°C

FPGA Pin Information

Table 33. Pin Table

Pin Name	Signal Name	Area
M24	SEG_A#	7-Segment Display
N23	SEG_B#	7-Segment Display
M22	SEG_B#	7-Segment Display
K21	SEG_CA0#	7-Segment Display
K20	SEG_CA0#	7-Segment Display
M21	SEG_D#	7-Segment Display
K22	SEG_DP#	7-Segment Display
M20	SEG_E#	7-Segment Display
L22	SEG_F#	7-Segment Display
L21	SEG_G#	7-Segment Display
B24	AC97_BITCLK	AC97 Audio Codec
C23	AC97_EAPD	AC97 Audio Codec
D25	AC97_EXT CLK	AC97 Audio Codec
B25	AC97_RESET#	AC97 Audio Codec
C26	AC97_SDATA_IN	AC97 Audio Codec
C25	AC97_SDATA_OUT	AC97 Audio Codec
D24	AC97_SYNC	AC97 Audio Codec
W4	ADC-	Analog Digital Converter
W3	ADC+	Analog Digital Converter
Y3	ADCS	Analog Digital Converter
AA22	CCLK	Configuration
AC24	CFG0	Configuration
W20	CFG1	Configuration
AD24	CFG2	Configuration
V22	CSSPIN	Configuration
Y24	DOUT	Configuration
AC3	EC_TCK	Configuration
AA8	EC_TDI	Configuration
AA5	EC_TDO	Configuration
AB4	EC_TMS	Configuration
AD25	JTAG_DONE	Configuration
AB24	JTAG_INIT	Configuration
V19	PROGRAM#	Configuration
Y25	SISPI	Configuration
W23	SPIDO	Configuration
AB25	SPIFASTN#	Configuration
AD10	DDR_A0	DDR SDRAM
AB11	DDR_A1	DDR SDRAM
AC10	DDR_A10	DDR SDRAM
AC14	DDR_A11	DDR SDRAM
AD14	DDR_A12	DDR SDRAM
AB10	DDR_A13	DDR SDRAM
AB12	DDR_A2	DDR SDRAM

Table 33. Pin Table (Continued)

Pin Name	Signal Name	Area
AC12	DDR_A3	DDR SDRAM
AD12	DDR_A4	DDR SDRAM
AB13	DDR_A5	DDR SDRAM
AC13	DDR_A6	DDR SDRAM
AD13	DDR_A7	DDR SDRAM
AB15	DDR_A8	DDR SDRAM
AB14	DDR_A9	DDR SDRAM
AD7	DDR_BA0	DDR SDRAM
AC7	DDR_BA1	DDR SDRAM
AF9	DDR_CAS#	DDR SDRAM
AF12	DDR_CK0-	DDR SDRAM
AE12	DDR_CK0+	DDR SDRAM
AA2	DDR_CK1-	DDR SDRAM
Y1	DDR_CK1+	DDR SDRAM
AF11	DDR_CKE0	DDR SDRAM
AF10	DDR_CKE1	DDR SDRAM
AF6	DDR_DM0	DDR SDRAM
AB6	DDR_DM1	DDR SDRAM
AB2	DDR_DM2	DDR SDRAM
T2	DDR_DM3	DDR SDRAM
AD9	DDR_DQ0	DDR SDRAM
AC9	DDR_DQ1	DDR SDRAM
AD5	DDR_DQ10	DDR SDRAM
AC5	DDR_DQ11	DDR SDRAM
AF4	DDR_DQ12	DDR SDRAM
AE4	DDR_DQ13	DDR SDRAM
AD4	DDR_DQ14	DDR SDRAM
AC4	DDR_DQ15	DDR SDRAM
AE2	DDR_DQ16	DDR SDRAM
AD1	DDR_DQ17	DDR SDRAM
AD2	DDR_DQ18	DDR SDRAM
AD3	DDR_DQ19	DDR SDRAM
AB9	DDR_DQ2	DDR SDRAM
AC1	DDR_DQ20	DDR SDRAM
AC2	DDR_DQ21	DDR SDRAM
Y5	DDR_DQ22	DDR SDRAM
Y6	DDR_DQ23	DDR SDRAM
V1	DDR_DQ24	DDR SDRAM
U1	DDR_DQ25	DDR SDRAM
P4	DDR_DQ26	DDR SDRAM
P5	DDR_DQ27	DDR SDRAM
P6	DDR_DQ28	DDR SDRAM
N3	DDR_DQ29	DDR SDRAM
AD8	DDR_DQ3	DDR SDRAM

Table 33. Pin Table (Continued)

Pin Name	Signal Name	Area
N4	DDR_DQ30	DDR SDRAM
N5	DDR_DQ31	DDR SDRAM
AC8	DDR_DQ4	DDR SDRAM
AB8	DDR_DQ5	DDR SDRAM
AF7	DDR_DQ7	DDR SDRAM
AE7	DDR_DQ7	DDR SDRAM
AF5	DDR_DQ8	DDR SDRAM
AE5	DDR_DQ9	DDR SDRAM
AE6	DDR_DQS0	DDR SDRAM
AA6	DDR_DQS1	DDR SDRAM
AB3	DDR_DQS2	DDR SDRAM
T1	DDR_DQS3	DDR SDRAM
AE9	DDR_RAS#	DDR SDRAM
AF8	DDR_S0#	DDR SDRAM
AE8	DDR_S1#	DDR SDRAM
AF3	DDR_VREF	DDR SDRAM
P9	DDR_VREF	DDR SDRAM
AE10	DDR_WE#	DDR SDRAM
C14	DAC_DIG	Digital Analog Converter
F26	DSW0	DIP Switch
F25	DSW1	DIP Switch
E26	DSW2	DIP Switch
E25	DSW3	DIP Switch
P25	ETH_COL	Ethernet
N26	ETH_CRS	Ethernet
M26	ETH_MDC	Ethernet
W24	ETH_MDINTR#	Ethernet
N25	ETH_MDIO	Ethernet
L26	ETH_RXCLK	Ethernet
AA26	ETH_RXD0	Ethernet
Y26	ETH_RXD1	Ethernet
W26	ETH_RXD2	Ethernet
W25	ETH_RXD3	Ethernet
R25	ETH_RXDV	Ethernet
P26	ETH_RXER	Ethernet
L25	ETH_TXCLK	Ethernet
V26	ETH_TXD0	Ethernet
V25	ETH_TXD1	Ethernet
V24	ETH_TXD2	Ethernet
V23	ETH_TXD3	Ethernet
R26	ETH_TXEN	Ethernet
U26	ETH_TXER	Ethernet
D1	CARDSEL#	Expansion Connector
L1	EXPCON_CLKIN	Expansion Connector

Table 33. Pin Table (Continued)

Pin Name	Signal Name	Area
M1	EXPCON_CLKOUT	Expansion Connector
R1	EXPCON_IO0	Expansion Connector
R2	EXPCON_IO1	Expansion Connector
L8	EXPCON_IO10	Expansion Connector
K1	EXPCON_IO11	Expansion Connector
K2	EXPCON_IO12	Expansion Connector
K3	EXPCON_IO13	Expansion Connector
K4	EXPCON_IO14	Expansion Connector
K5	EXPCON_IO15	Expansion Connector
K6	EXPCON_IO16	Expansion Connector
K7	EXPCON_IO17	Expansion Connector
K8	EXPCON_IO18	Expansion Connector
J1	EXPCON_IO19	Expansion Connector
P1	EXPCON_IO2	Expansion Connector
J2	EXPCON_IO20	Expansion Connector
J3	EXPCON_IO21	Expansion Connector
J4	EXPCON_IO22	Expansion Connector
J5	EXPCON_IO23	Expansion Connector
J8	EXPCON_IO24	Expansion Connector
J9	EXPCON_IO25	Expansion Connector
H1	EXPCON_IO26	Expansion Connector
H2	EXPCON_IO27	Expansion Connector
H3	EXPCON_IO28	Expansion Connector
H4	EXPCON_IO29	Expansion Connector
P2	EXPCON_IO3	Expansion Connector
H5	EXPCON_IO30	Expansion Connector
H6	EXPCON_IO31	Expansion Connector
H7	EXPCON_IO32	Expansion Connector
H8	EXPCON_IO33	Expansion Connector
G1	EXPCON_IO34	Expansion Connector
G2	EXPCON_IO35	Expansion Connector
G3	EXPCON_IO36	Expansion Connector
G4	EXPCON_IO37	Expansion Connector
F1	EXPCON_IO38	Expansion Connector
F2	EXPCON_IO39	Expansion Connector
N1	EXPCON_IO4	Expansion Connector
F5	EXPCON_IO40	Expansion Connector
F6	EXPCON_IO41	Expansion Connector
E1	EXPCON_IO42	Expansion Connector
E2	EXPCON_IO43	Expansion Connector
E3	EXPCON_IO44	Expansion Connector
E4	EXPCON_IO45	Expansion Connector
M6	EXPCON_IO5	Expansion Connector
L2	EXPCON_IO6	Expansion Connector

Table 33. Pin Table (Continued)

Pin Name	Signal Name	Area
L5	EXPCON_IO7	Expansion Connector
L6	EXPCON_IO8	Expansion Connector
L7	EXPCON_IO9	Expansion Connector
B12	FLASH_BYTE#	Flash/SRAM
A13	FLASH_CE#	Flash/SRAM
B14	FLASH_RESET#	Flash/SRAM
A14	FLASH_RY/BY# A	Flash/SRAM
B13	FLASH_RY/BY# B	Flash/SRAM
A12	FLASH_WP#/ACC	Flash/SRAM
C1	MEMORY_A0	Flash/SRAM
B2	MEMORY_A1	Flash/SRAM
D4	MEMORY_A10	Flash/SRAM
A5	MEMORY_A11	Flash/SRAM
B5	MEMORY_A12	Flash/SRAM
C5	MEMORY_A13	Flash/SRAM
D5	MEMORY_A14	Flash/SRAM
E5	MEMORY_A15	Flash/SRAM
A6	MEMORY_A16	Flash/SRAM
B6	MEMORY_A17	Flash/SRAM
E6	MEMORY_A18	Flash/SRAM
A7	MEMORY_A19	Flash/SRAM
C2	MEMORY_A2	Flash/SRAM
B7	MEMORY_A20	Flash/SRAM
C7	MEMORY_A21	Flash/SRAM
D7	MEMORY_A22	Flash/SRAM
A3	MEMORY_A3	Flash/SRAM
B3	MEMORY_A4	Flash/SRAM
C3	MEMORY_A5	Flash/SRAM
D3	MEMORY_A6	Flash/SRAM
A4	MEMORY_A7	Flash/SRAM
B4	MEMORY_A8	Flash/SRAM
C4	MEMORY_A9	Flash/SRAM
E7	MEMORY_DQ0	Flash/SRAM
F7	MEMORY_DQ1	Flash/SRAM
A9	MEMORY_DQ10	Flash/SRAM
B9	MEMORY_DQ11	Flash/SRAM
C9	MEMORY_DQ12	Flash/SRAM
D9	MEMORY_DQ13	Flash/SRAM
E9	MEMORY_DQ14	Flash/SRAM
A10	MEMORY_DQ15	Flash/SRAM
B10	MEMORY_DQ16	Flash/SRAM
C10	MEMORY_DQ17	Flash/SRAM
D10	MEMORY_DQ18	Flash/SRAM
E10	MEMORY_DQ19	Flash/SRAM

Table 33. Pin Table (Continued)

Pin Name	Signal Name	Area
G7	MEMORY_DQ2	Flash/SRAM
F10	MEMORY_DQ20	Flash/SRAM
G10	MEMORY_DQ21	Flash/SRAM
A11	MEMORY_DQ22	Flash/SRAM
B11	MEMORY_DQ23	Flash/SRAM
E11	MEMORY_DQ24	Flash/SRAM
F11	MEMORY_DQ25	Flash/SRAM
G11	MEMORY_DQ26	Flash/SRAM
C12	MEMORY_DQ27	Flash/SRAM
D12	MEMORY_DQ28	Flash/SRAM
E12	MEMORY_DQ29	Flash/SRAM
A8	MEMORY_DQ3	Flash/SRAM
F12	MEMORY_DQ30	Flash/SRAM
G12	MEMORY_DQ31	Flash/SRAM
B8	MEMORY_DQ4	Flash/SRAM
C8	MEMORY_DQ5	Flash/SRAM
D8	MEMORY_DQ6	Flash/SRAM
E8	MEMORY_DQ7	Flash/SRAM
F8	MEMORY_DQ8	Flash/SRAM
G8	MEMORY_DQ9	Flash/SRAM
D13	MEMORY_OE#	Flash/SRAM
C13	MEMORY_WE#	Flash/SRAM
F13	SRAM_BE0#	Flash/SRAM
G13	SRAM_BE1#	Flash/SRAM
E14	SRAM_BE2#	Flash/SRAM
E15	SRAM_BE3#	Flash/SRAM
E13	SRAM_CE#	Flash/SRAM
AD15	CLK_FPGA	FPGA Clock
U25	CLK_FPGA	FPGA Clock
F14	BB3V3_CLK0-	FPGA Prototyping Area
D14	BB3V3_CLK0+	FPGA Prototyping Area
A15	BB3V3_IO0	FPGA Prototyping Area
B15	BB3V3_IO1	FPGA Prototyping Area
D17	BB3V3_IO10	FPGA Prototyping Area
E17	BB3V3_IO11	FPGA Prototyping Area
A18	BB3V3_IO12	FPGA Prototyping Area
B18	BB3V3_IO13	FPGA Prototyping Area
C18	BB3V3_IO14	FPGA Prototyping Area
D18	BB3V3_IO15	FPGA Prototyping Area
E18	BB3V3_IO16	FPGA Prototyping Area
A19	BB3V3_IO17	FPGA Prototyping Area
B19	BB3V3_IO18	FPGA Prototyping Area
C19	BB3V3_IO19	FPGA Prototyping Area
C15	BB3V3_IO2	FPGA Prototyping Area

Table 33. Pin Table (Continued)

Pin Name	Signal Name	Area
D19	BB3V3_IO20	FPGA Prototyping Area
E19	BB3V3_IO21	FPGA Prototyping Area
D15	BB3V3_IO3	FPGA Prototyping Area
A16	BB3V3_IO4	FPGA Prototyping Area
B16	BB3V3_IO5	FPGA Prototyping Area
E16	BB3V3_IO6	FPGA Prototyping Area
A17	BB3V3_IO7	FPGA Prototyping Area
B17	BB3V3_IO8	FPGA Prototyping Area
C17	BB3V3_IO9	FPGA Prototyping Area
T21	I2C_SCL1	I^2C EEPROM
T22	I2C_SDA1	I^2C EEPROM
G26	TST_COL0	Key Matrix
G25	TST_COL1	Key Matrix
G24	TST_COL2	Key Matrix
H26	TST_ROW0	Key Matrix
H25	TST_ROW1	Key Matrix
H24	TST_ROW2	Key Matrix
H23	TST_ROW3	Key Matrix
J22	LCD_ENABLE	LCD
K24	LCD_REGSEL	LCD
J24	LCD_RW	LCD
R24	LED0#	LED
R23	LED1#	LED
R22	LED2#	LED
R21	LED3#	LED
P23	LED4#	LED
P22	LED5#	LED
P21	LED6#	LED
N22	LED7#	LED
H13	MACHXO_CLK0	MachXO
H14	MACHXO_CLK1	MachXO
A20	MACHXO_IO0	MachXO
B20	MACHXO_IO1	MachXO
C22	MACHXO_IO10	MachXO
D22	MACHXO_IO11	MachXO
A23	MACHXO_IO12	MachXO
B23	MACHXO_IO13	MachXO
E23	MACHXO_IO14	MachXO
A24	MACHXO_IO15	MachXO
C20	MACHXO_IO2	MachXO
D20	MACHXO_IO3	MachXO
E20	MACHXO_IO4	MachXO
A21	MACHXO_IO5	MachXO
B21	MACHXO_IO6	MachXO

Table 33. Pin Table (Continued)

Pin Name	Signal Name	Area
E21	MACHXO_IO7	MachXO
A22	MACHXO_IO8	MachXO
B22	MACHXO_IO9	MachXO
M25	HPE_RESET#	Reset
AE24	HPE_RESOUT#	Reset
J26	RS CTS_LVTTL	RS232
K25	RS RTS_LVTTL	RS232
J25	RS RXD_LVTTL	RS232
K26	RS TXD_LVTTL	RS232
M5	SATA_X1D0-	SATA
M4	SATA_X1D0+	SATA
R3	SATA_X1D1-	SATA
P3	SATA_X1D1+	SATA
U4	SATA_X2D0-	SATA
U3	SATA_X2D0+	SATA
W2	SATA_X2D1-	SATA
V2	SATA_X2D1+	SATA
E24	TST_STEP	Single Step Key
AB21	USB_CTS	USB Interface
AE20	USB_GPIO0	USB Interface
AD20	USB_GPIO1	USB Interface
AA19	USB_GPIO10	USB Interface
AF18	USB_GPIO11	USB Interface
AE18	USB_GPIO12	USB Interface
AD18	USB_GPIO13	USB Interface
AC18	USB_GPIO14	USB Interface
AB18	USB_GPIO15	USB Interface
AF17	USB_GPIO16	USB Interface
AE17	USB_GPIO17	USB Interface
AD17	USB_GPIO18	USB Interface
AC17	USB_GPIO19	USB Interface
AC20	USB_GPIO2	USB Interface
AB17	USB_GPIO20	USB Interface
AF16	USB_GPIO21	USB Interface
AE16	USB_GPIO22	USB Interface
AF15	USB_GPIO23	USB Interface
AE15	USB_GPIO24	USB Interface
AF14	USB_GPIO25	USB Interface
AE14	USB_GPIO26	USB Interface
AF13	USB_GPIO27	USB Interface
AE13	USB_GPIO28	USB Interface
AB20	USB_GPIO3	USB Interface
AA20	USB_GPIO4	USB Interface
AF19	USB_GPIO5	USB Interface

Table 33. Pin Table (Continued)

Pin Name	Signal Name	Area
AE19	USB_GPIO6	USB Interface
AD19	USB_GPIO7	USB Interface
AC19	USB_GPIO8	USB Interface
AB19	USB_GPIO9	USB Interface
AD23	USB_MISO	USB Interface
AB16	USB_MOSI	USB Interface
AA16	USB_OC0#	USB Interface
Y20	USB_OC1#	USB Interface
Y19	USB_OC2#	USB Interface
Y17	USB_PWEN0	USB Interface
Y16	USB_PWEN1	USB Interface
AA21	USB_PWEN2	USB Interface
AB22	USB_RTS	USB Interface
AC23	USB_RXD	USB Interface
AC22	USB_SCK	USB Interface
AD22	USB_SSI#	USB Interface
AA17	USB_TXD	USB Interface
AF22	VGA_BL0	VGA Interface
AE21	VGA_BL1	VGA Interface
AF23	VGA_GR0	VGA Interface
AE22	VGA_GR1	VGA Interface
AF20	VGA_HSYNC	VGA Interface
AF24	VGA_RD0	VGA Interface
AE23	VGA_RD1	VGA Interface
AF21	VGA_VSYNC	VGA Interface

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LatticeMico32/DSP Development Board for LatticeECP2	LFE2-50E-D-EV	

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
February 2007	01.0	Initial release.
March 2007	01.1	Added Ordering Information section.
April 2007	01.2	Updated SATA Interfaces information.
		Reset Chip section - updated FPGA pin number for the the HPE RESET signal.
April 2007	01.3	Ordering information (EFUP) updated.
April 2007	01.4	Added important information for proper connection of ispDOWNLOAD (Programming) Cables.
July 2007	01.5	Various minor updates to improve readability, and correct typographical errors.
August 2007	01.6	Updated information for pins 4-7 in the Expansion Connector X14 table.
		Updated information for LRF pin TP0902 in the FPGA Connections for the 12x12 Prototyping Area table.
September 2007	01.7	Updated Ascynchronous SRAM text section and corresponding table.
		Updated Parallel Flash text section.
February 2008	01.8	Updated Ordering Information.
March 2008	01.9	Corrected Schematic Illustration of the Prototyping Area diagram.
April 2008	02.0	Updated 7-Segment Display U0502 Pin Definition table.
June 2008	02.1	Updated Schematic Illustration of the Prototyping Area.
October 2008	02.2	Updated Peripheral Interfaces diagram with Board Version 2 information.
		Updated Data Signal of the Asynchronous SRAM Chip U0404 table.
		SPI Flash text section - Updated SPI Flash density to 16 bits. Added table. Updated steps for programing the SPI Flash memory.
		Added note to Parallel Flash text section.
		Added Appendix B. Board Version 2 Schematics.
October 2008	02.3	Address Signals of the Asynchronous SRAM Chips U0404 and U0405 table - updated FPGA Pin information for MEMORY_A1 and MEMORY_A2.
		Address Signals of the Flash Chips U0402 and U0403 table - updated FPGA Pin information for MEMORY_A1 and MEMORY_A2.
October 2008	02.4	Updated photo used in User Interface Features figure.
		Updated photo used in Components figure.
February 2009	02.5	Updated Audio Interface text section.
June 2009	02.6	Updated FPGA to SPI Flash Connections table.

Appendix A. Board Version 1 Schematic

Figure 9.

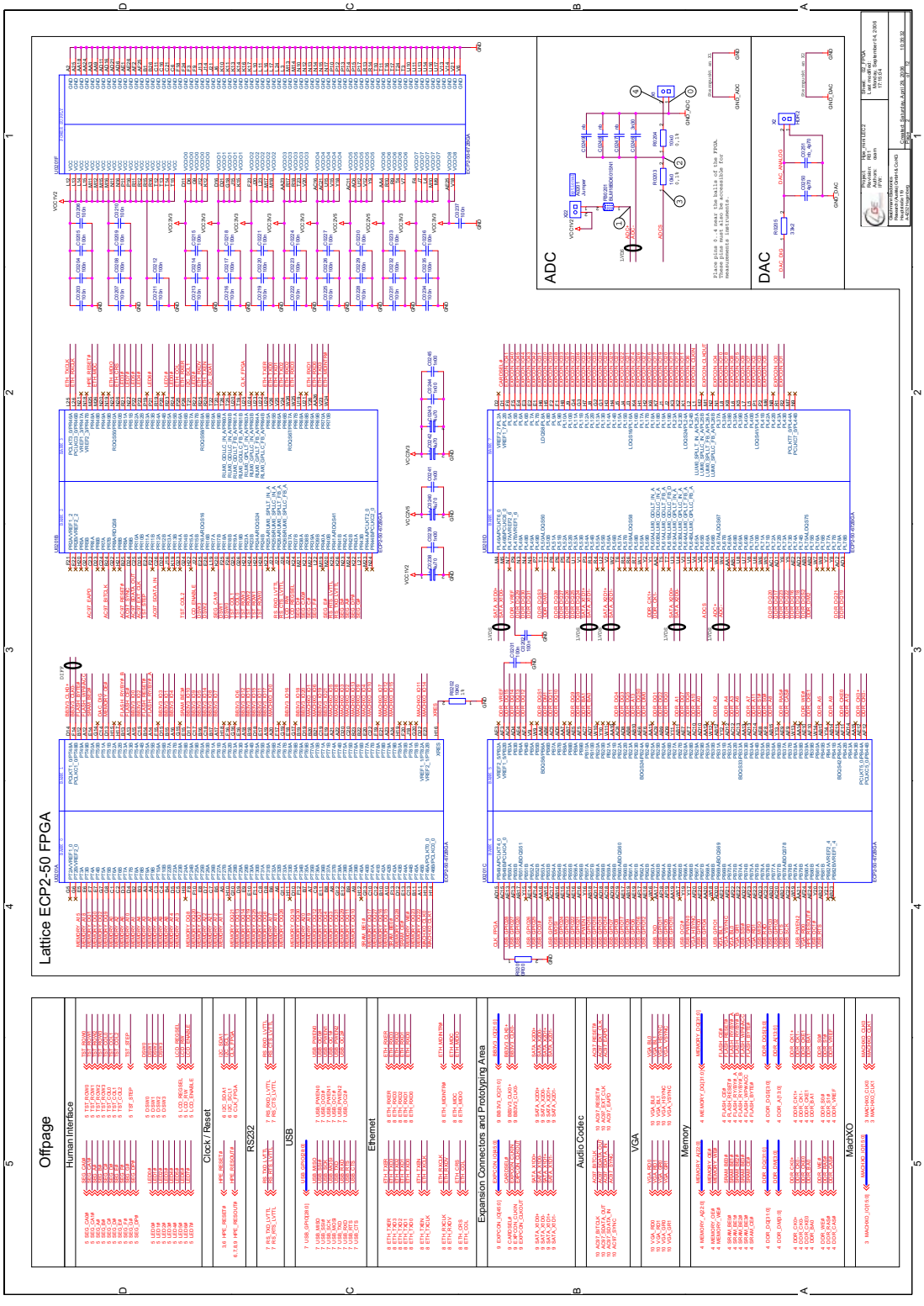


Figure 10.

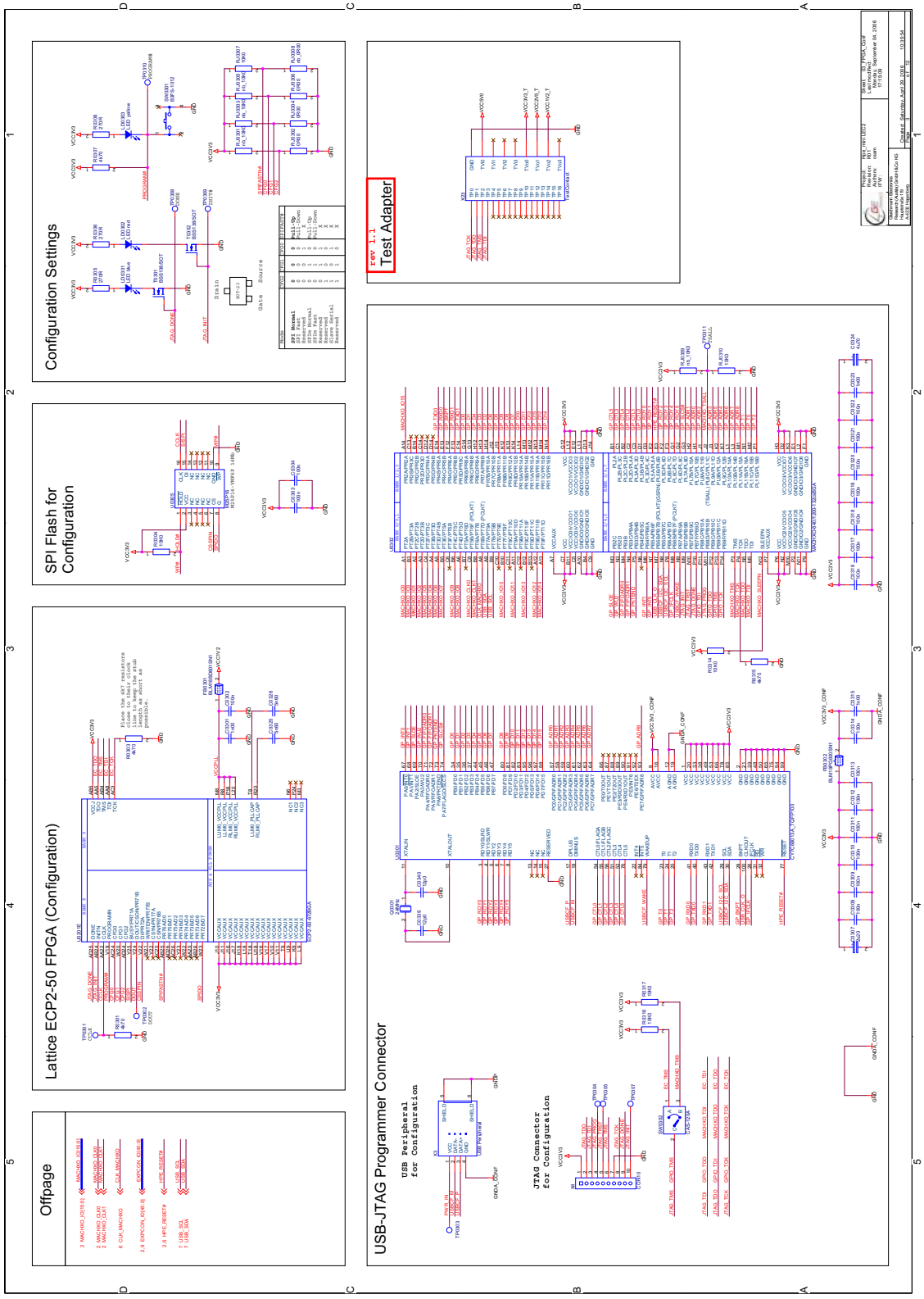

Offpage
Lattice ECP2-50 FPGA (Configuration)
SPI Flash for Configuration
Configuration Settings
Test Adapter
rev 1.1
USB-JTAG Programmer Connector
USB Peripheral for Configuration
JTAG Connector for Configuration

Figure 11.

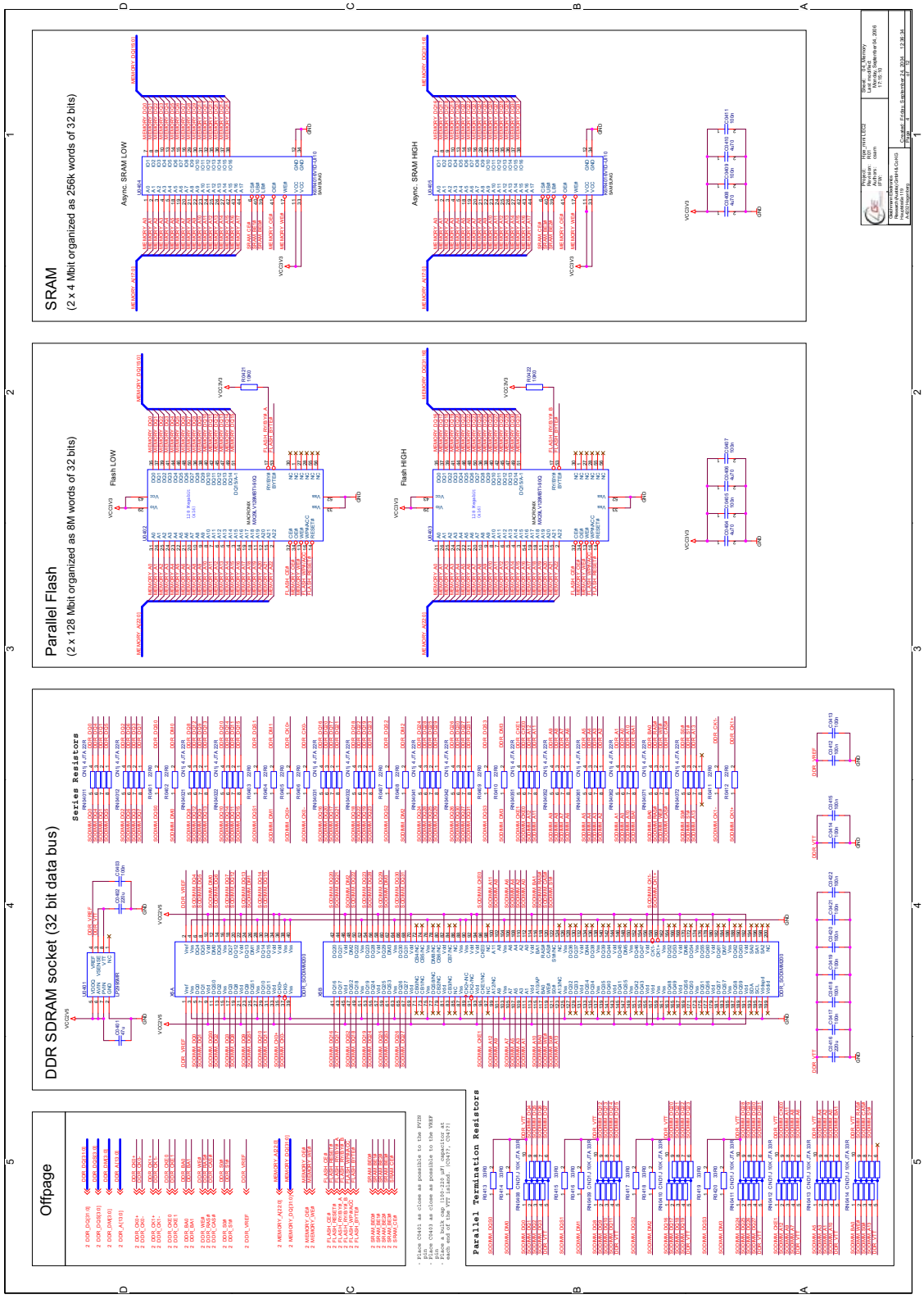

SRAM
(2 x 4 Mbit organized as 256k words of 32 bits)
Async. SRAM LOW
Async. SRAM HIGH
Parallel Flash
(2 x 128 Mbit organized as 8M words of 32 bits)
Flash LOW
Flash HIGH
DDR SDRAM socket (32 bit data bus)
Series Resistors
Parallel Termination Resistors
Offpage

Figure 12.

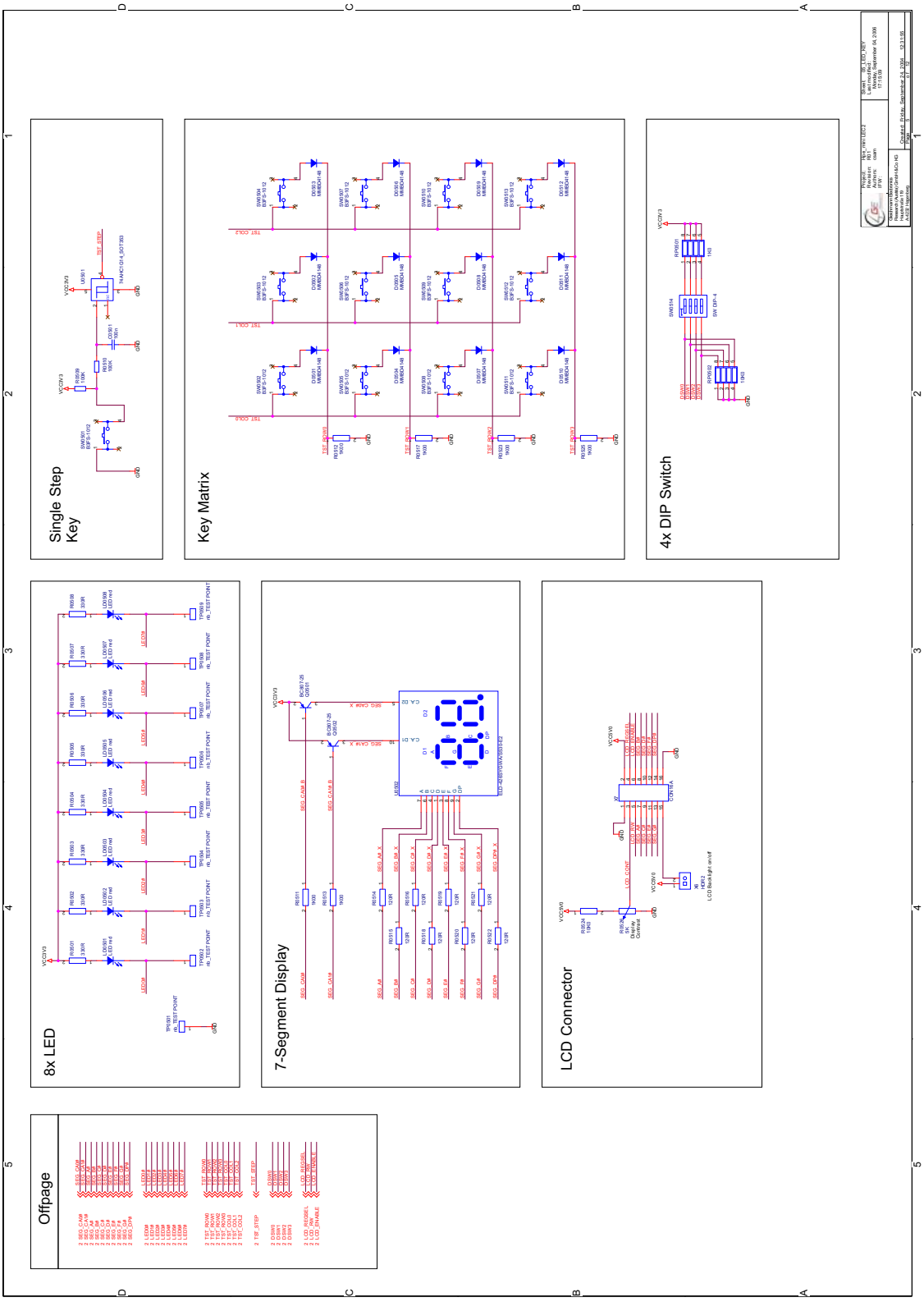

Single Step Key
Key Matrix
4x DIP Switch
8x LED
7-Segment Display
LCD Connector
Offpage

Figure 13.

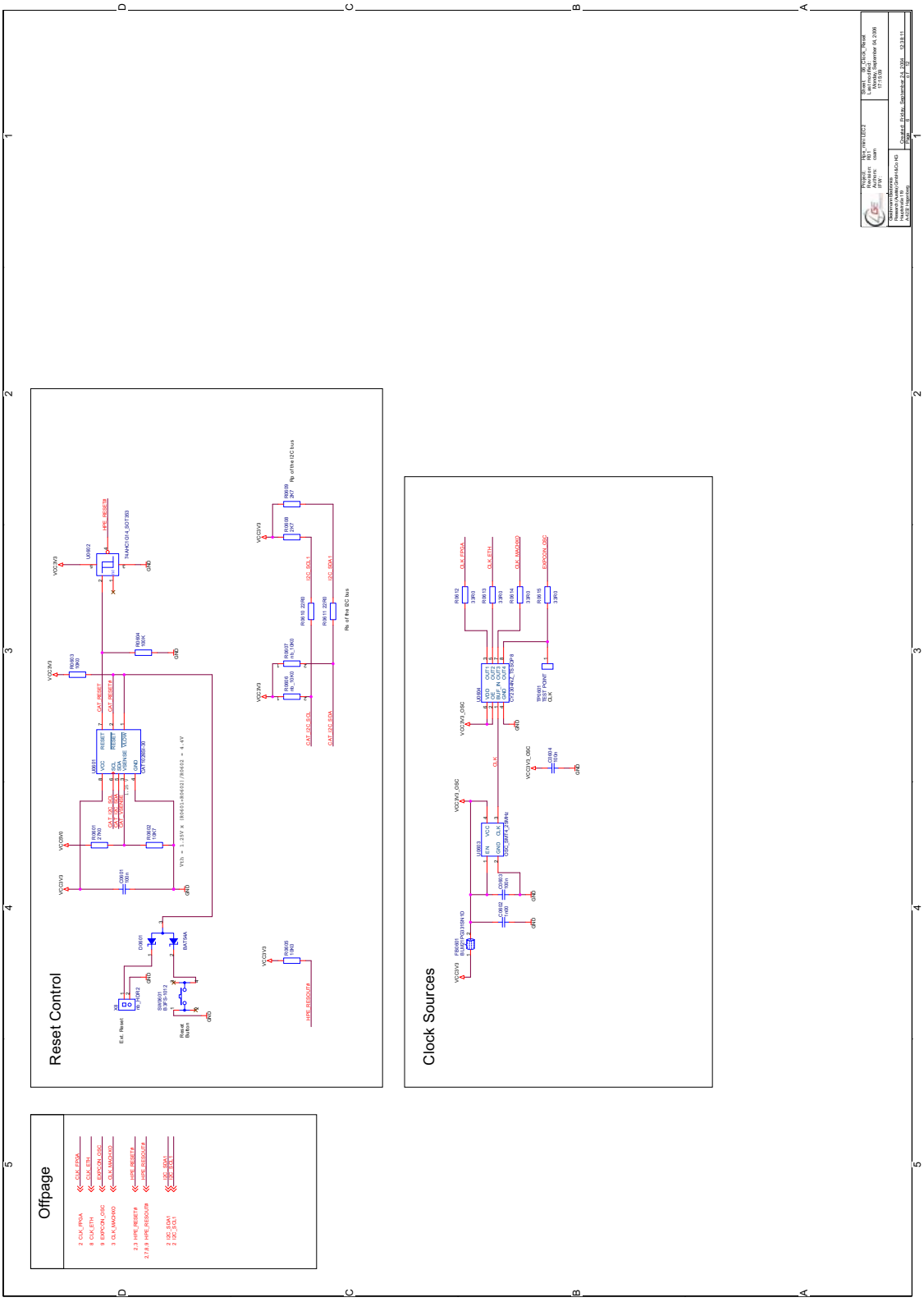


Figure 14.

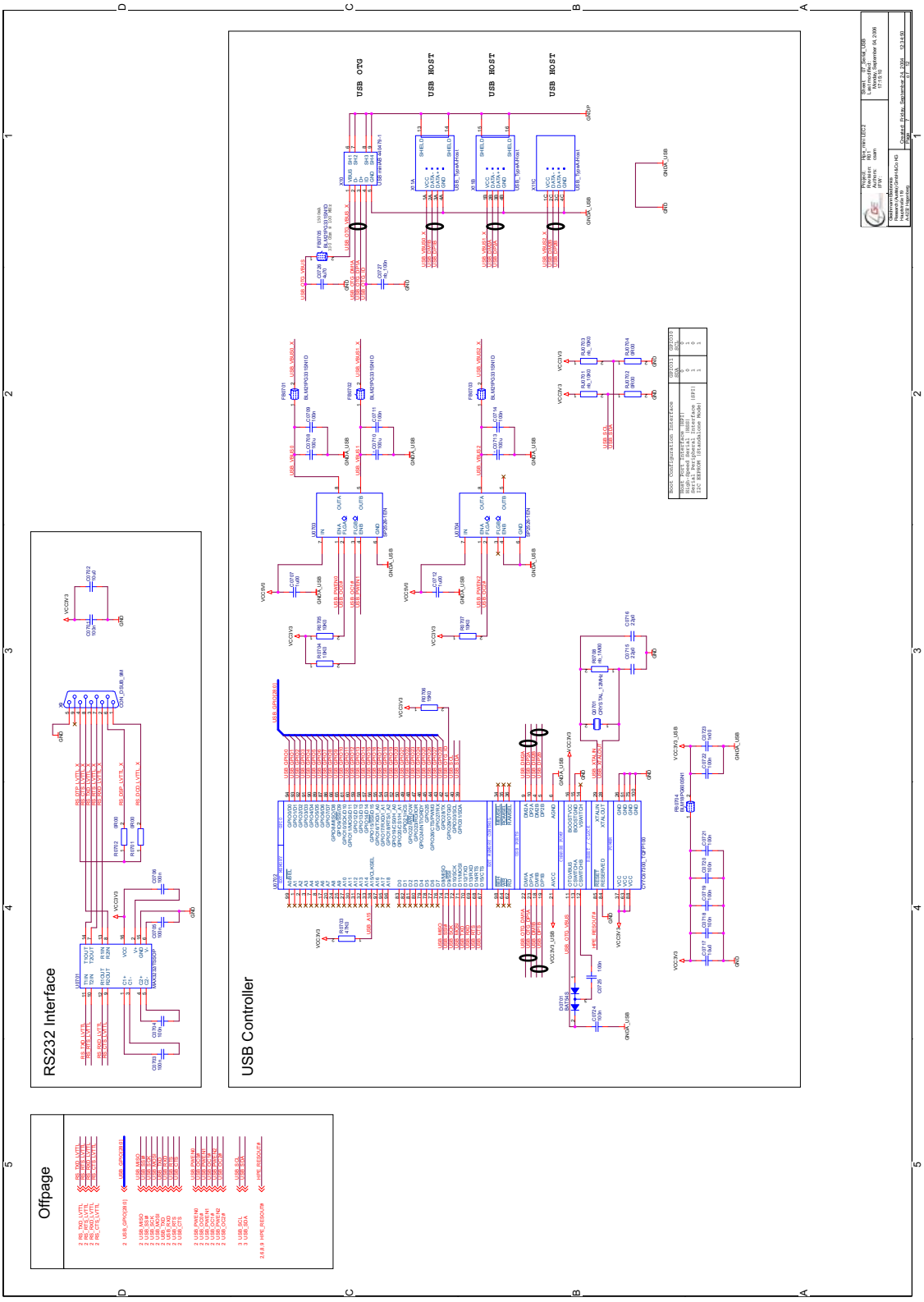

USB OTG
USB HOST
USB HOST
USB HOST
USB Controller
RS232 Interface
Offpage

Figure 15.

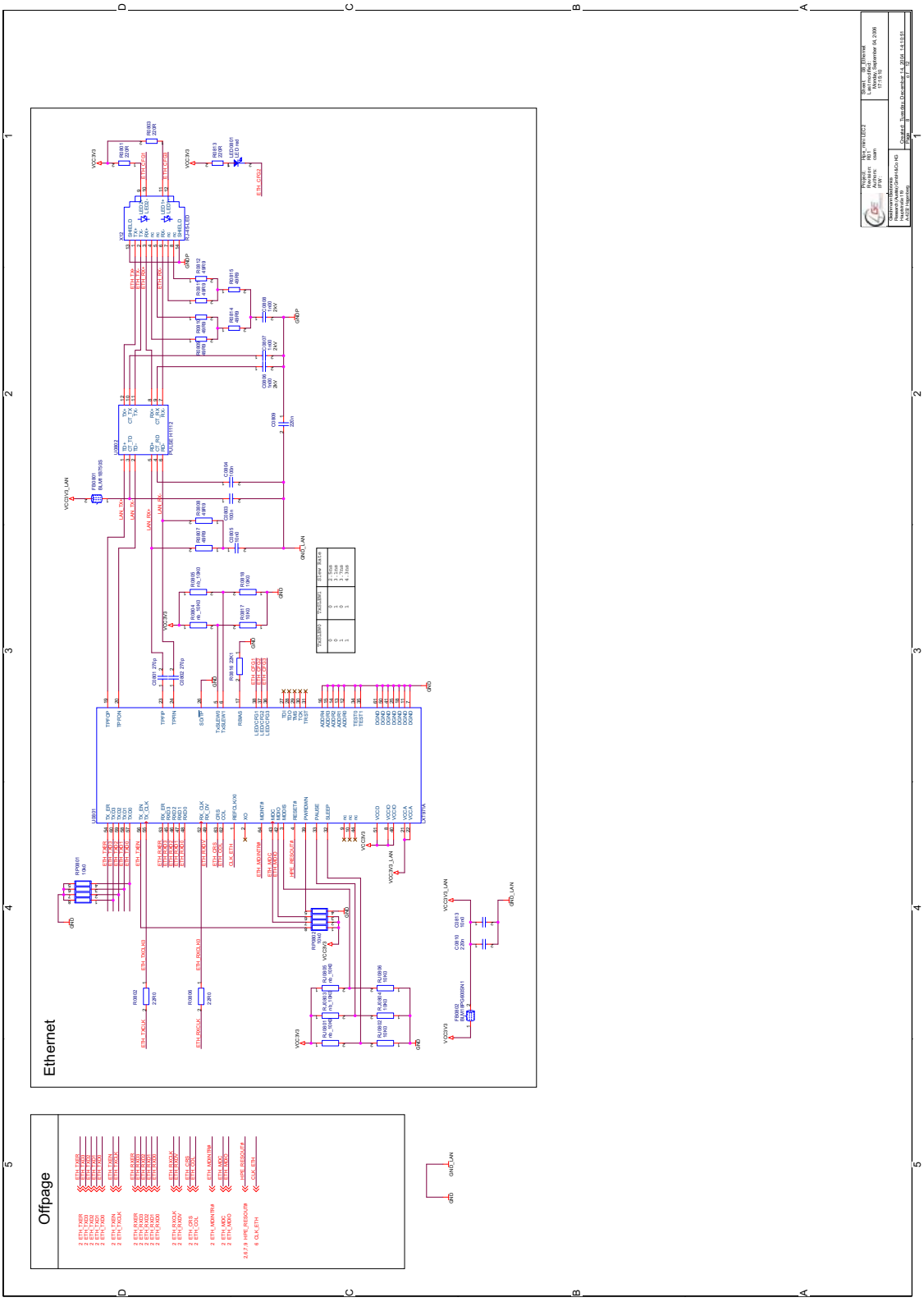


Figure 16.

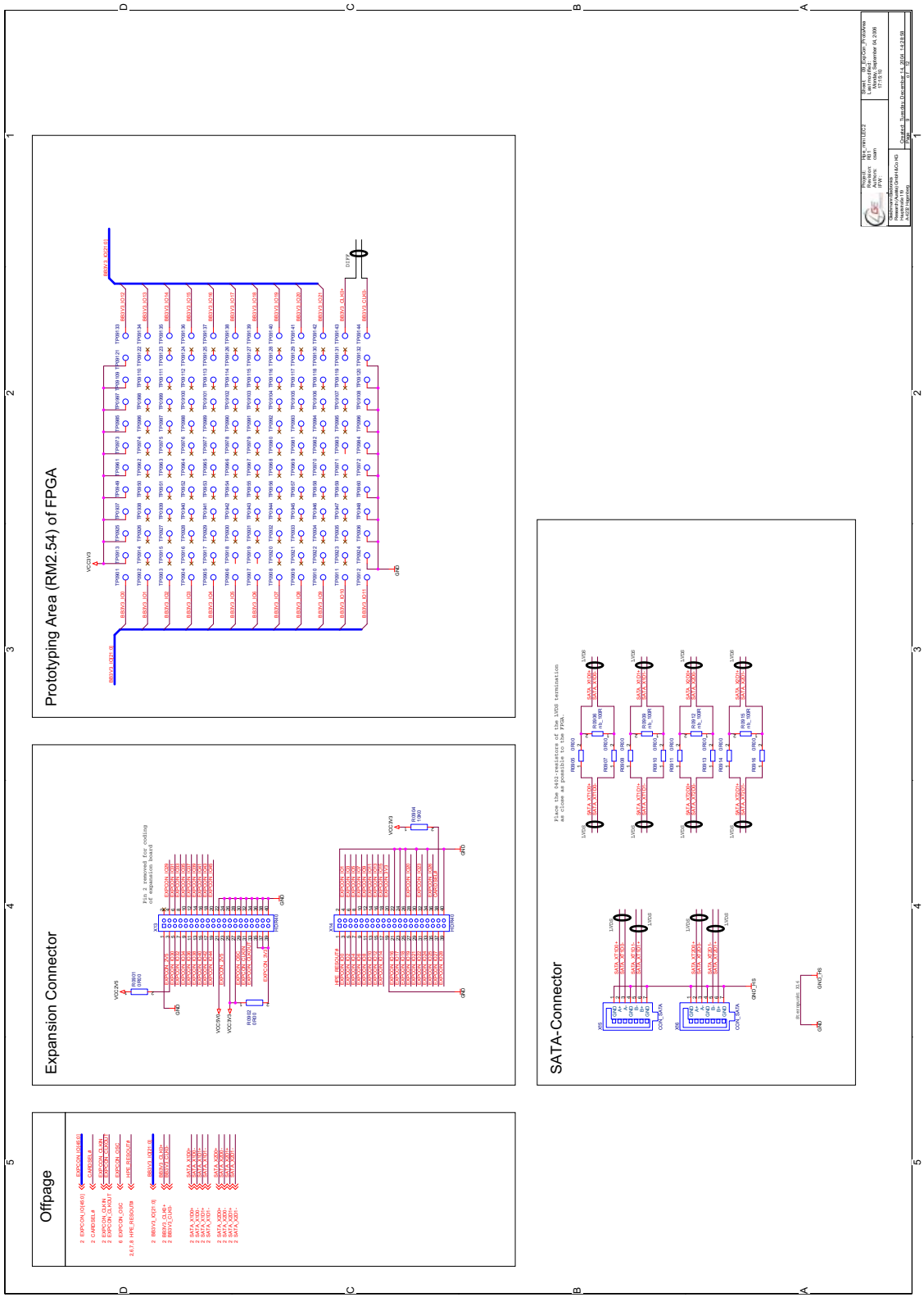

Offpage
Expansion Connector
Prototyping Area (RM2.54) of FPGA
SATA-Connector

Figure 17.

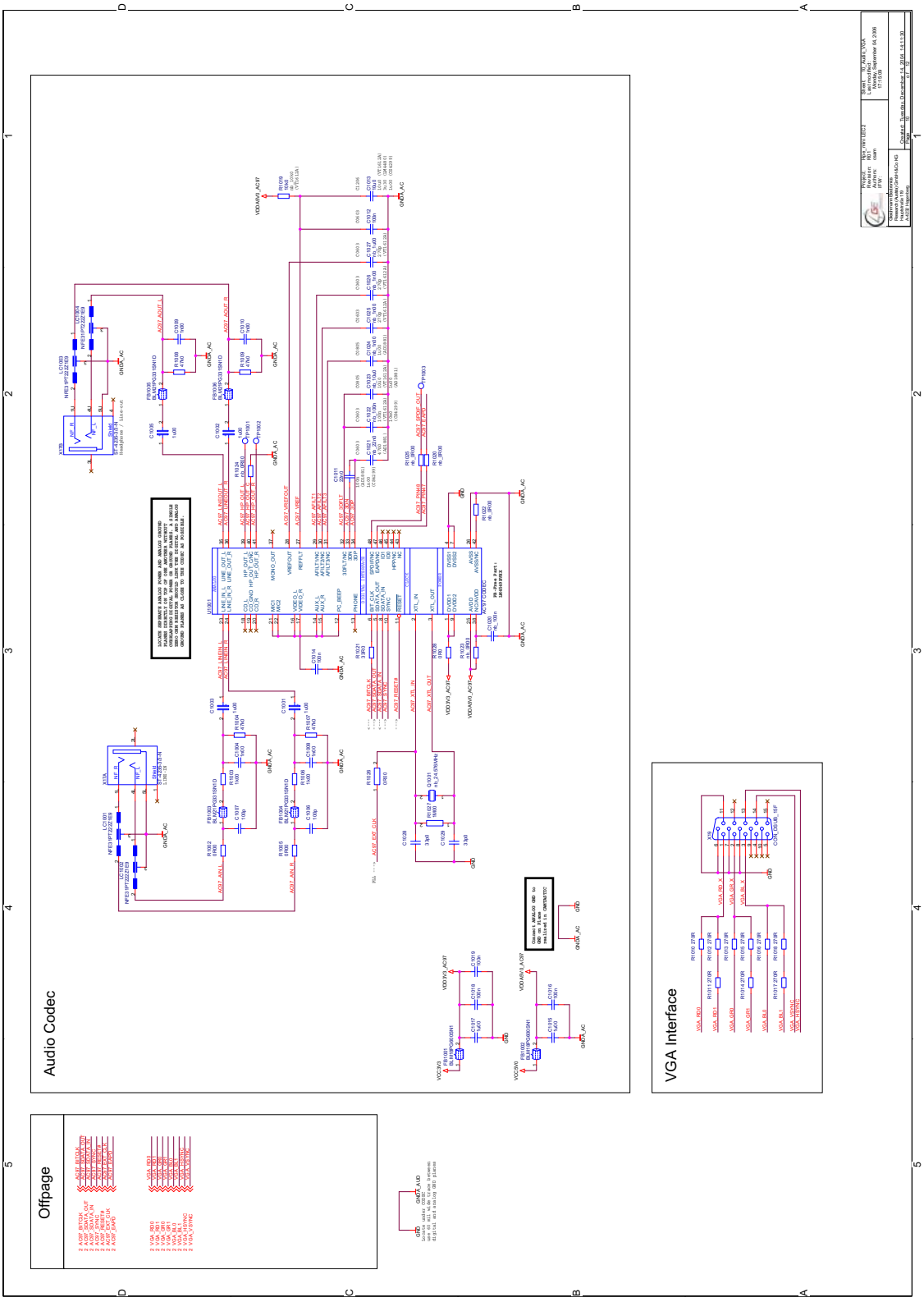
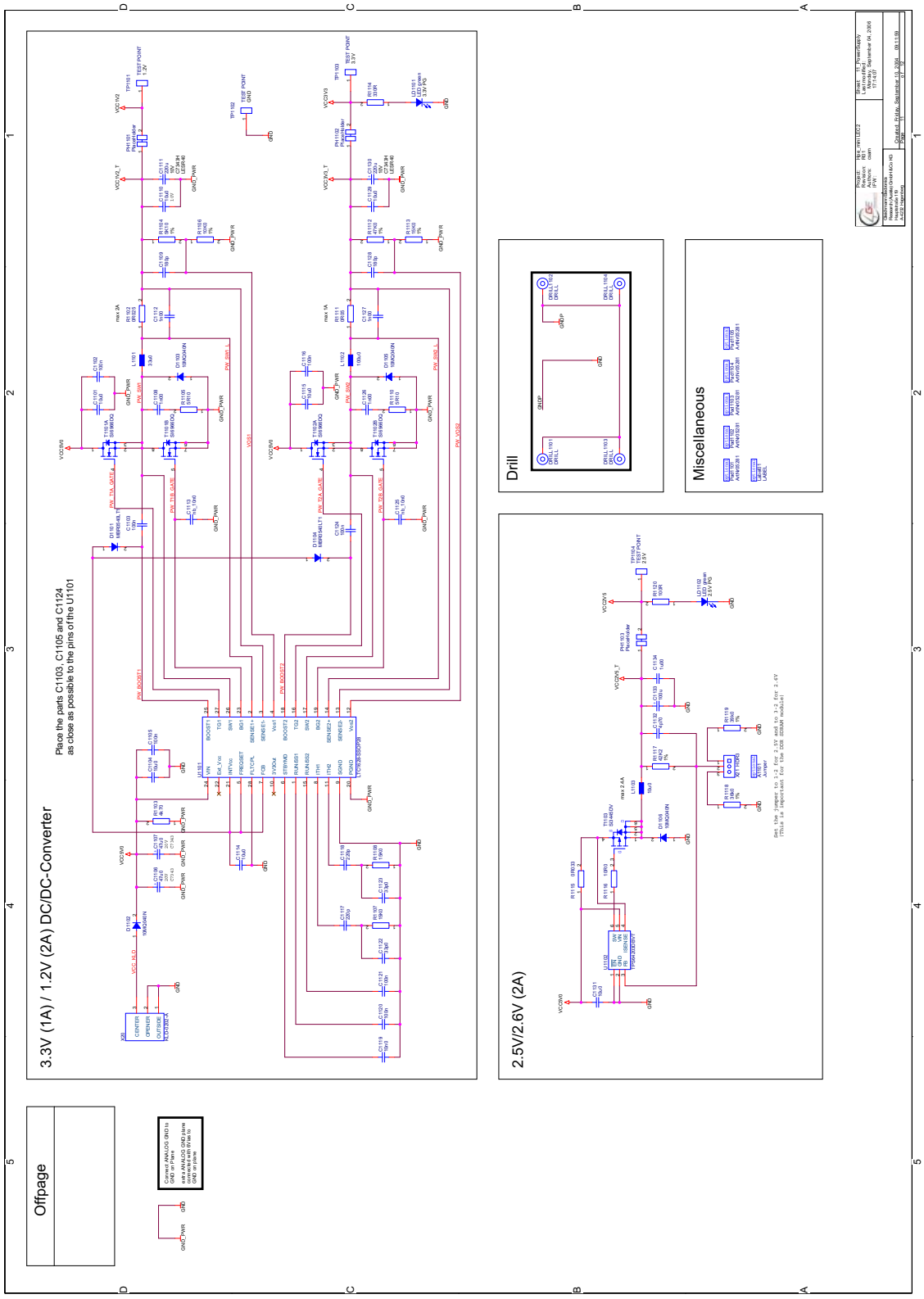


Figure 18.


3.3V (1A) / 1.2V (2A) DC/DC-Converter
Place the parts C1103, C1105 and C1124
as close as possible to the pins of the U1101
2.5V/2.6V (2A)
Drill
Miscellaneous
Offpage

Appendix B. Board Version 2 Schematic

Figure 19.

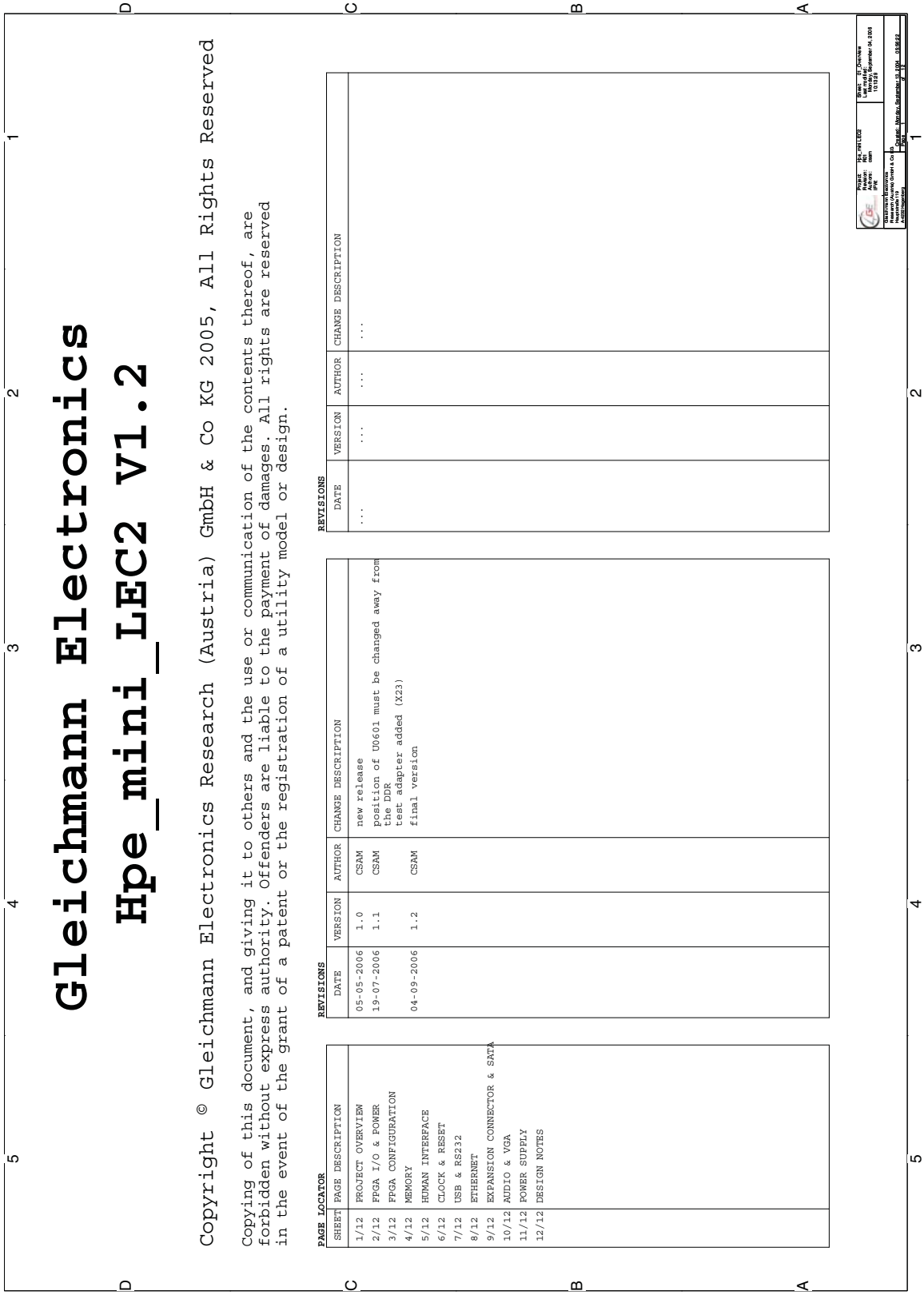


Figure 20.

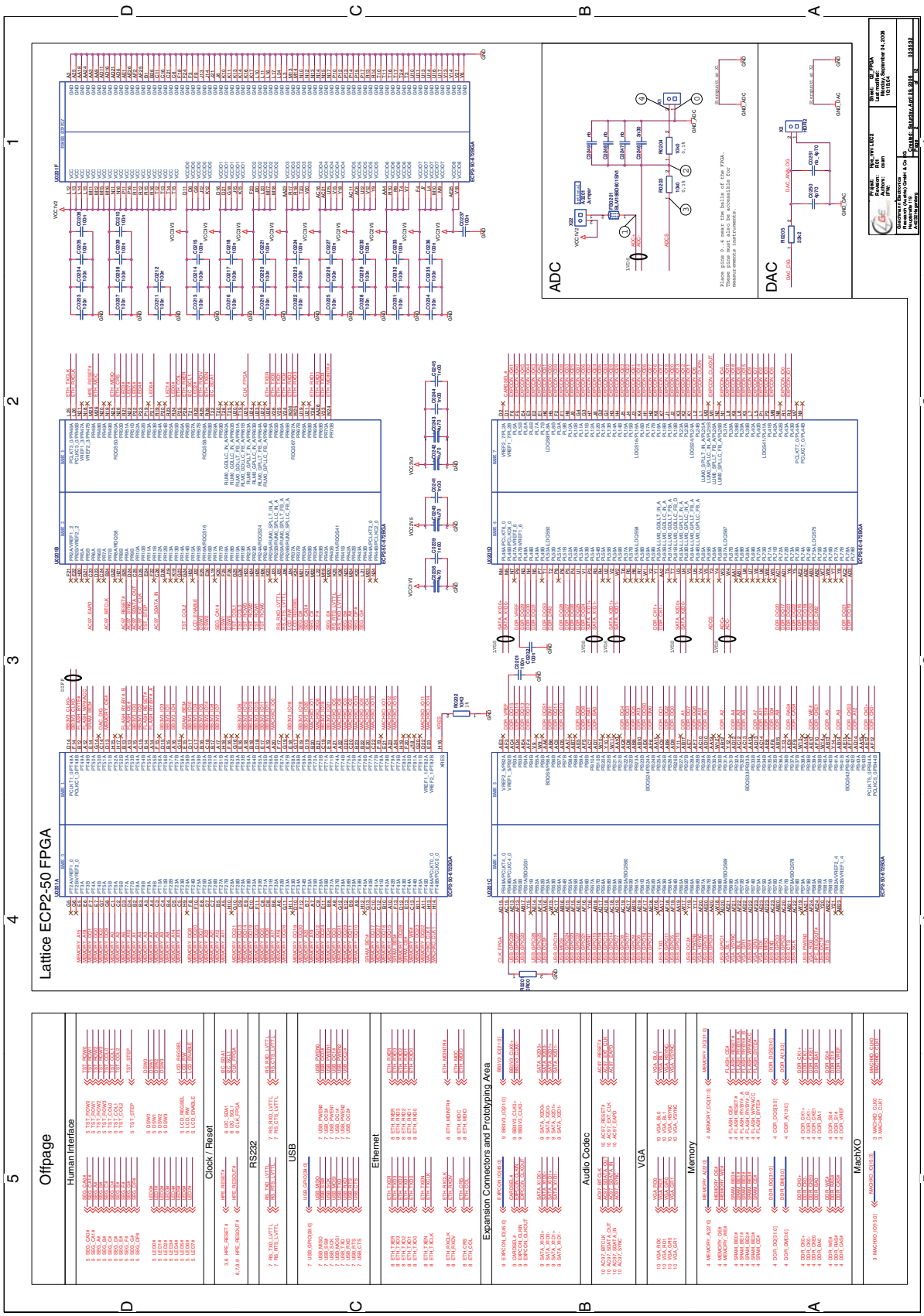

Offpage
Human Interface
Clock / Reset
RS232
USB
Ethernet
Expansion Connectors and Prototyping Area
Audio Codec
VGA
Memory
MachXO
Lattice ECP2-50 FPGA
ADC
DAC

Figure 21.

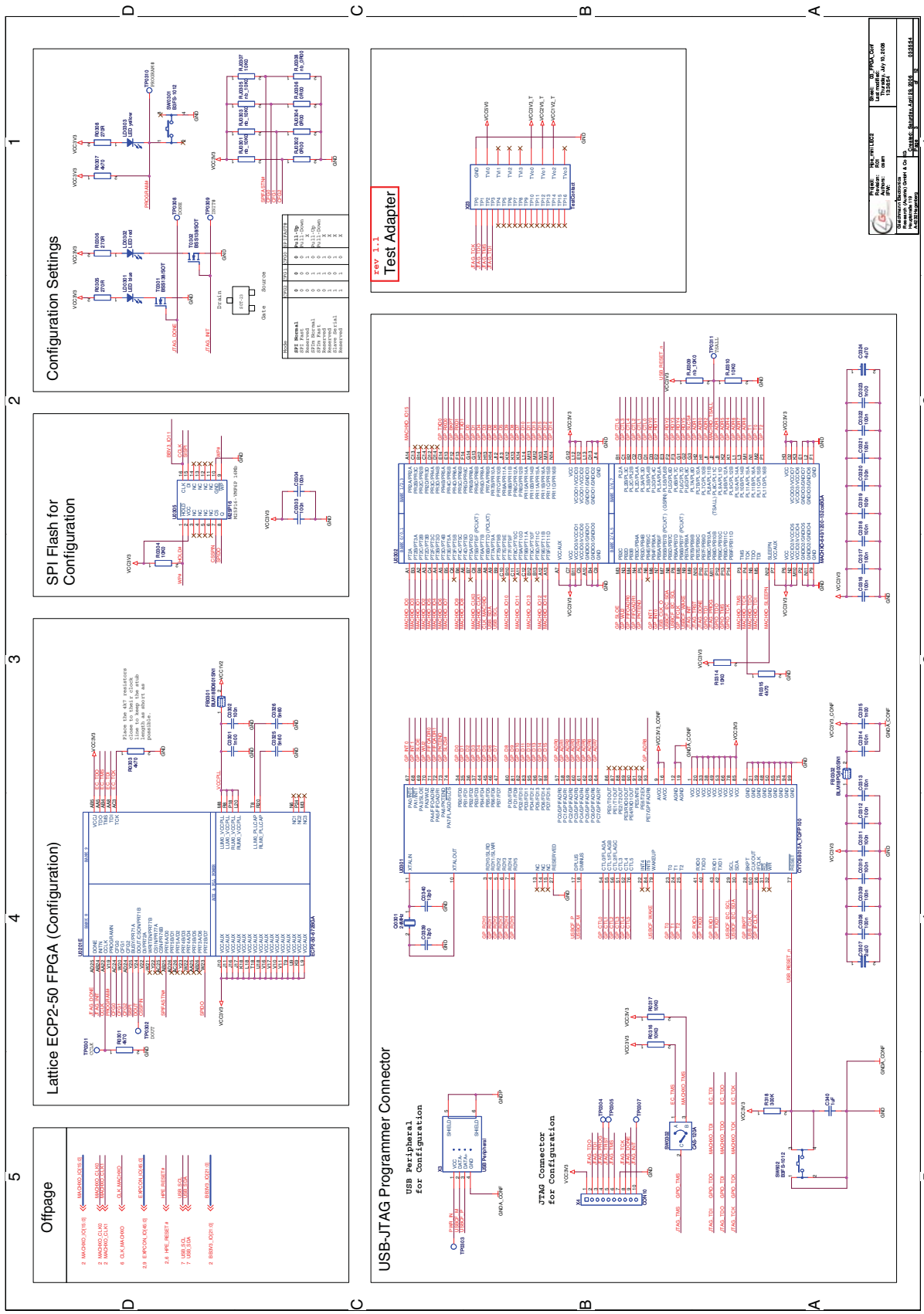

Offpage
Lattice ECP2-50 FPGA (Configuration)
SPI Flash for Configuration
Configuration Settings
Test Adapter
USB-JTAG Programmer Connector
USB Peripheral for Configuration
JTAG Connector for Configuration

Figure 22.

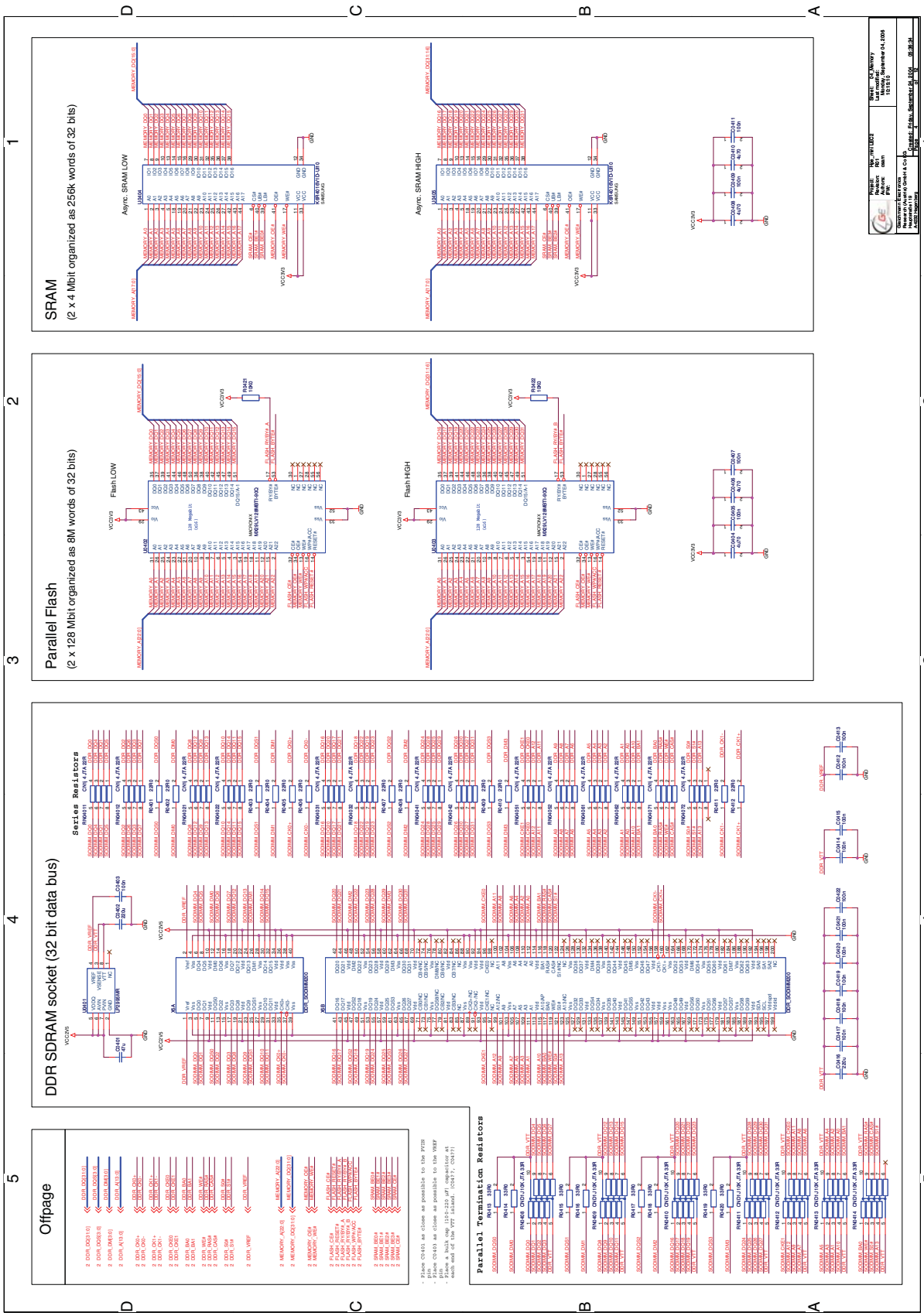

SRAM
(2 x 4 Mbit organized as 256k words of 32 bits)
Async. SRAM LOW
Async. SRAM HIGH
Parallel Flash
(2 x 128 Mbit organized as 8M words of 32 bits)
Flash LOW
Flash HIGH
DDR SDRAM socket (32 bit data bus)
Series Resistors
Offpage
Parallel Termination Resistors

Figure 23.

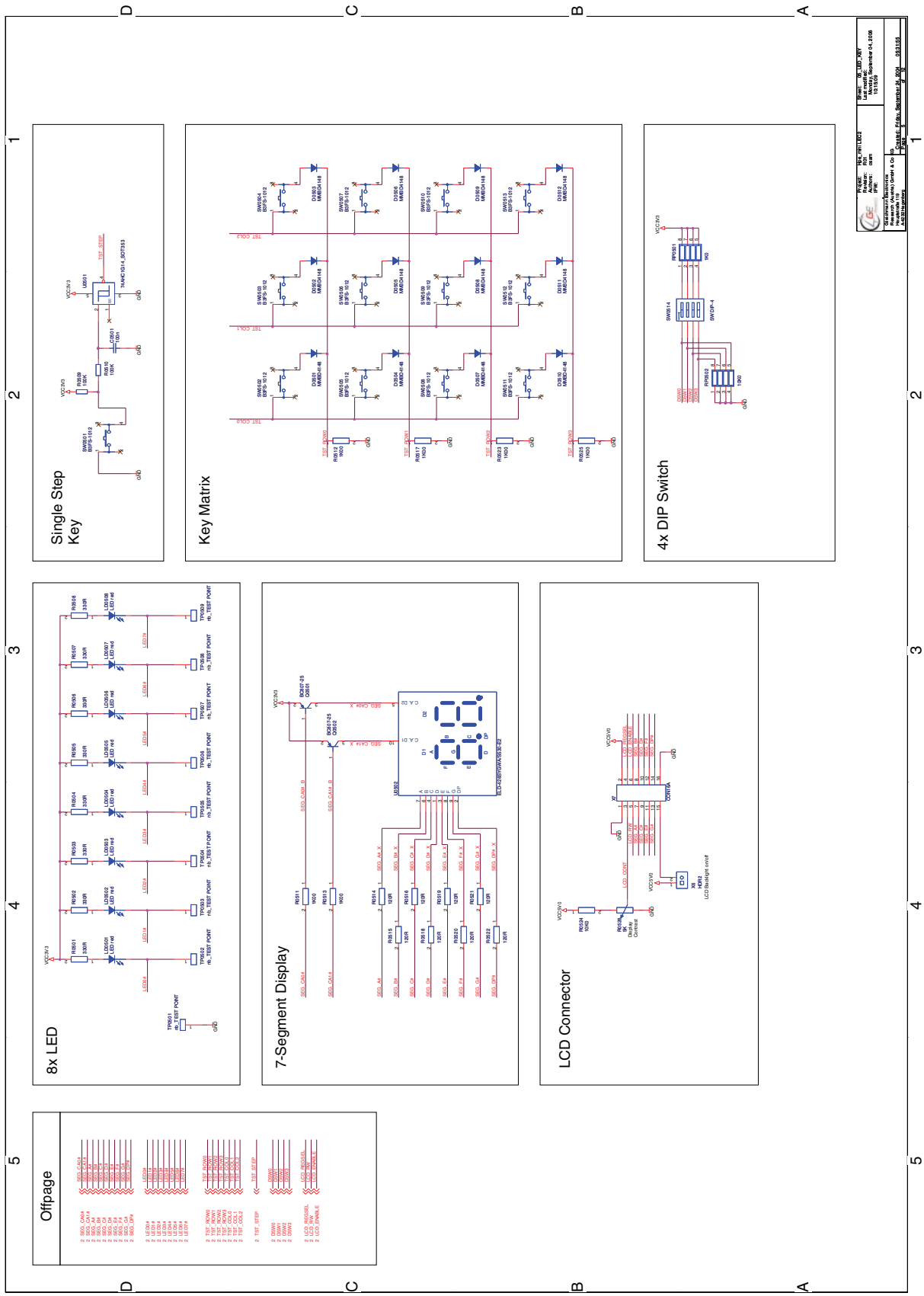

Single Step Key
Key Matrix
4x DIP Switch
8x LED
7-Segment Display
LCD Connector
Offpage

Figure 24.

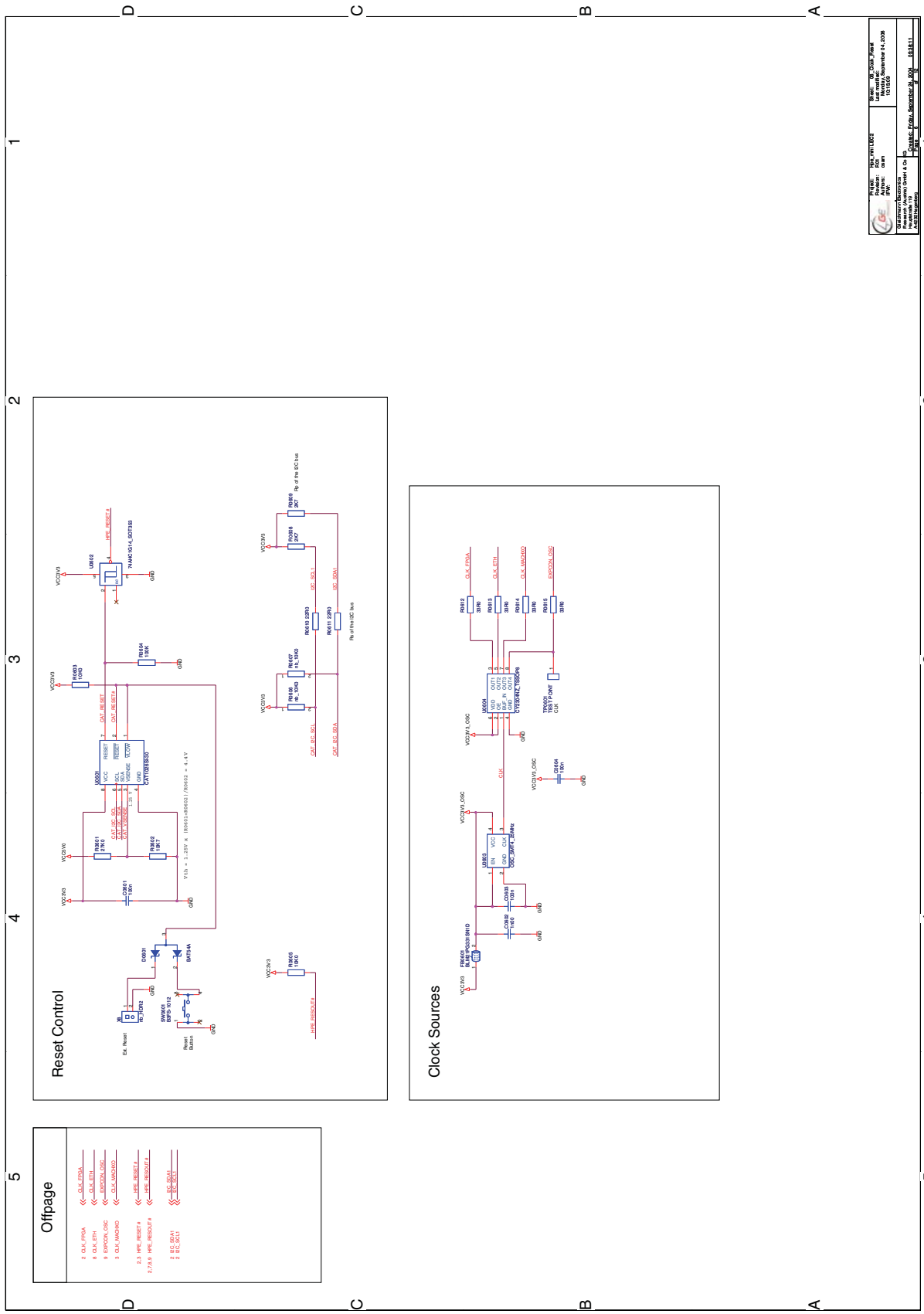


Figure 25.

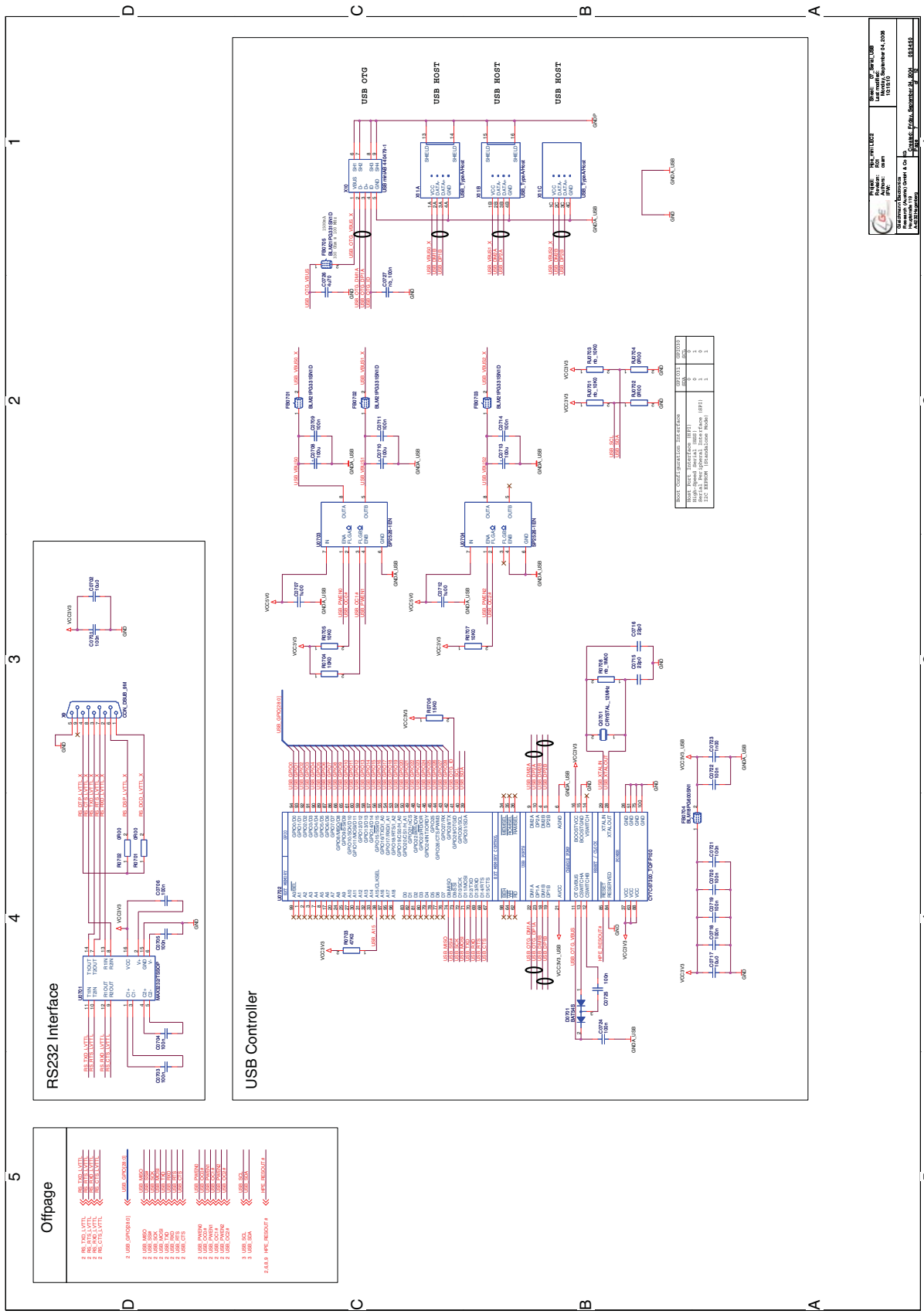

USB Controller
RS232 Interface
Offpage
USB OTG
USB HOST
USB HOST
USB HOST

Figure 26.

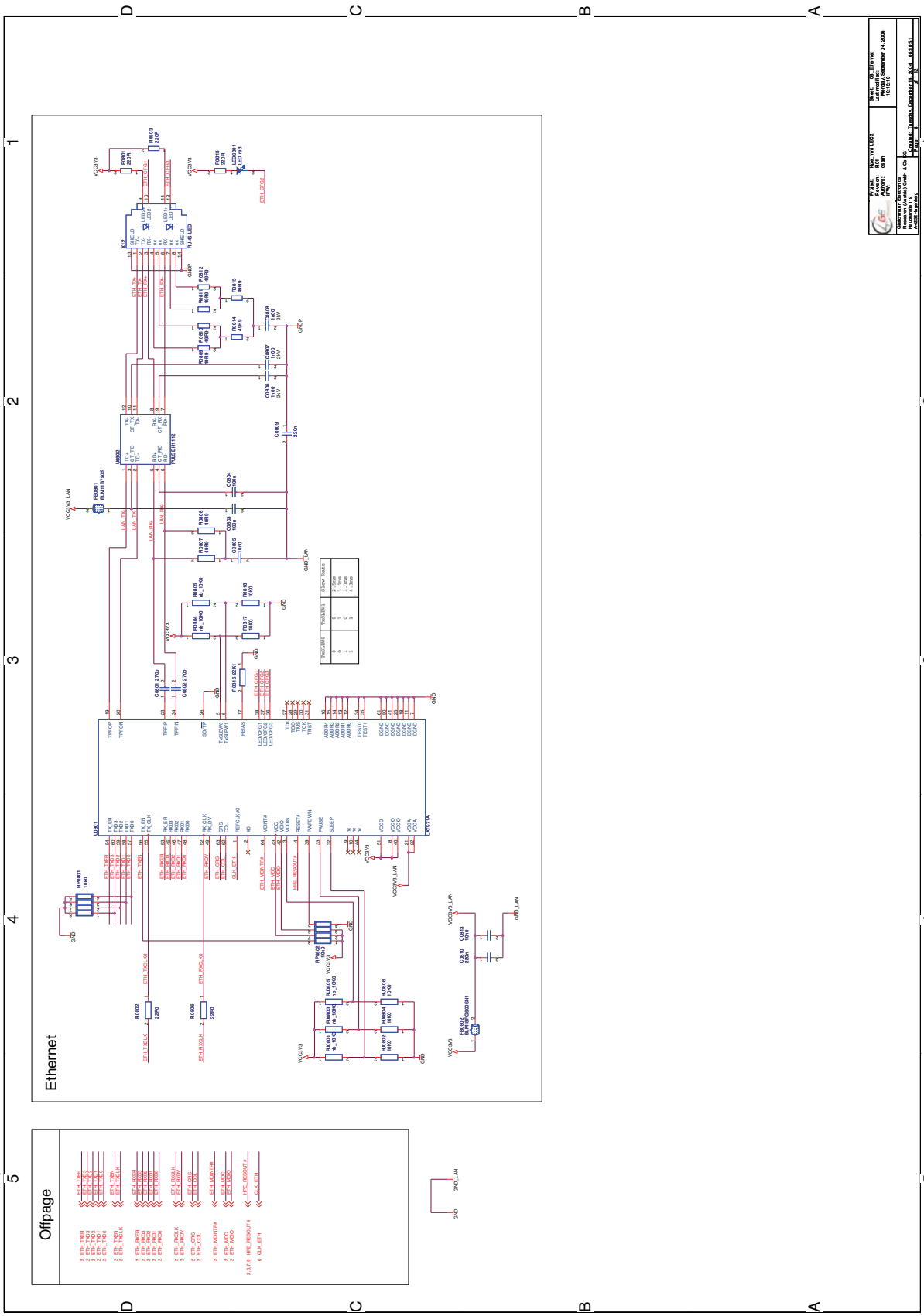


Figure 27.

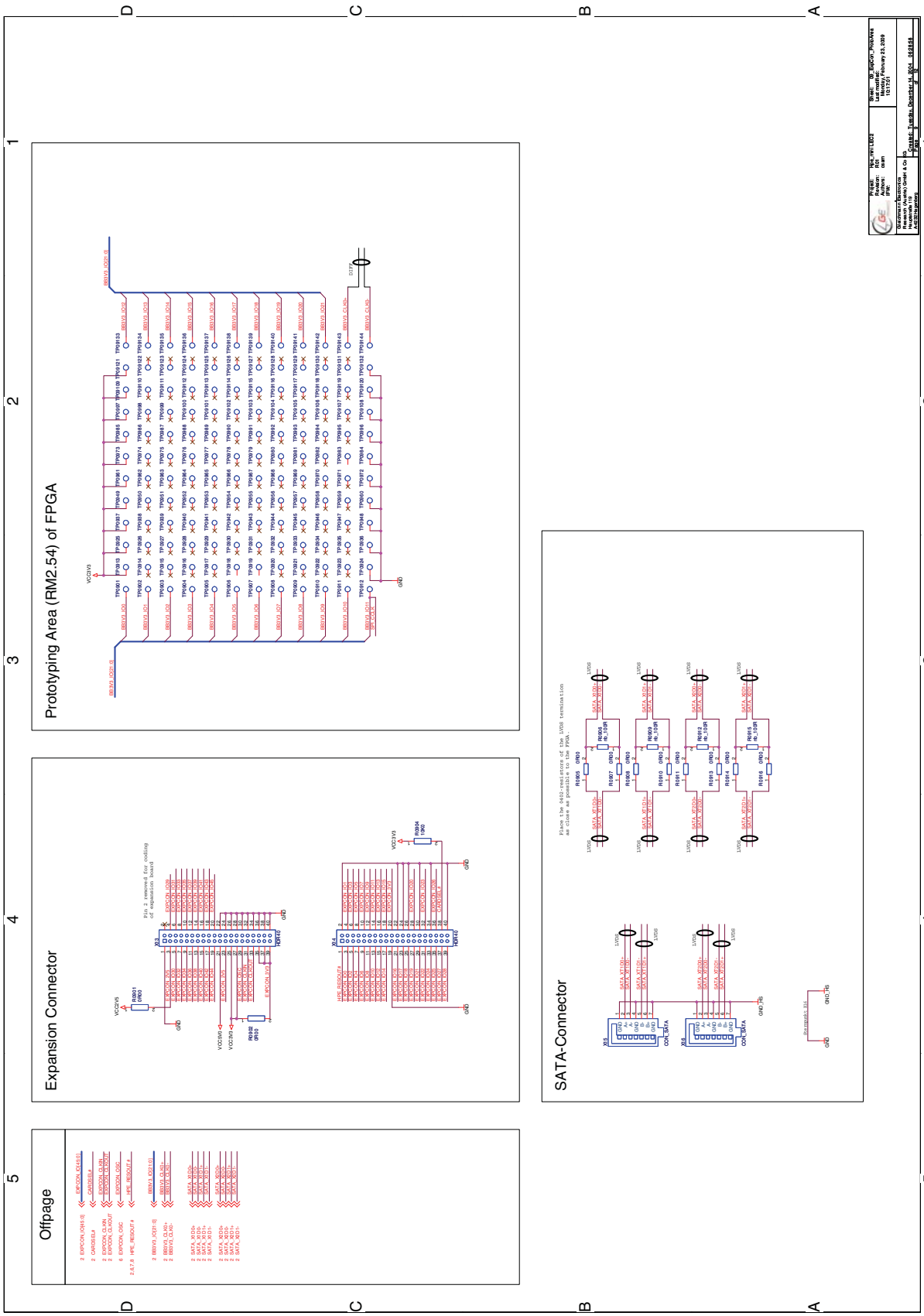

Prototyping Area (RM2.54) of FPGA
Expansion Connector
SATA-Connector
Offpage

Figure 28.

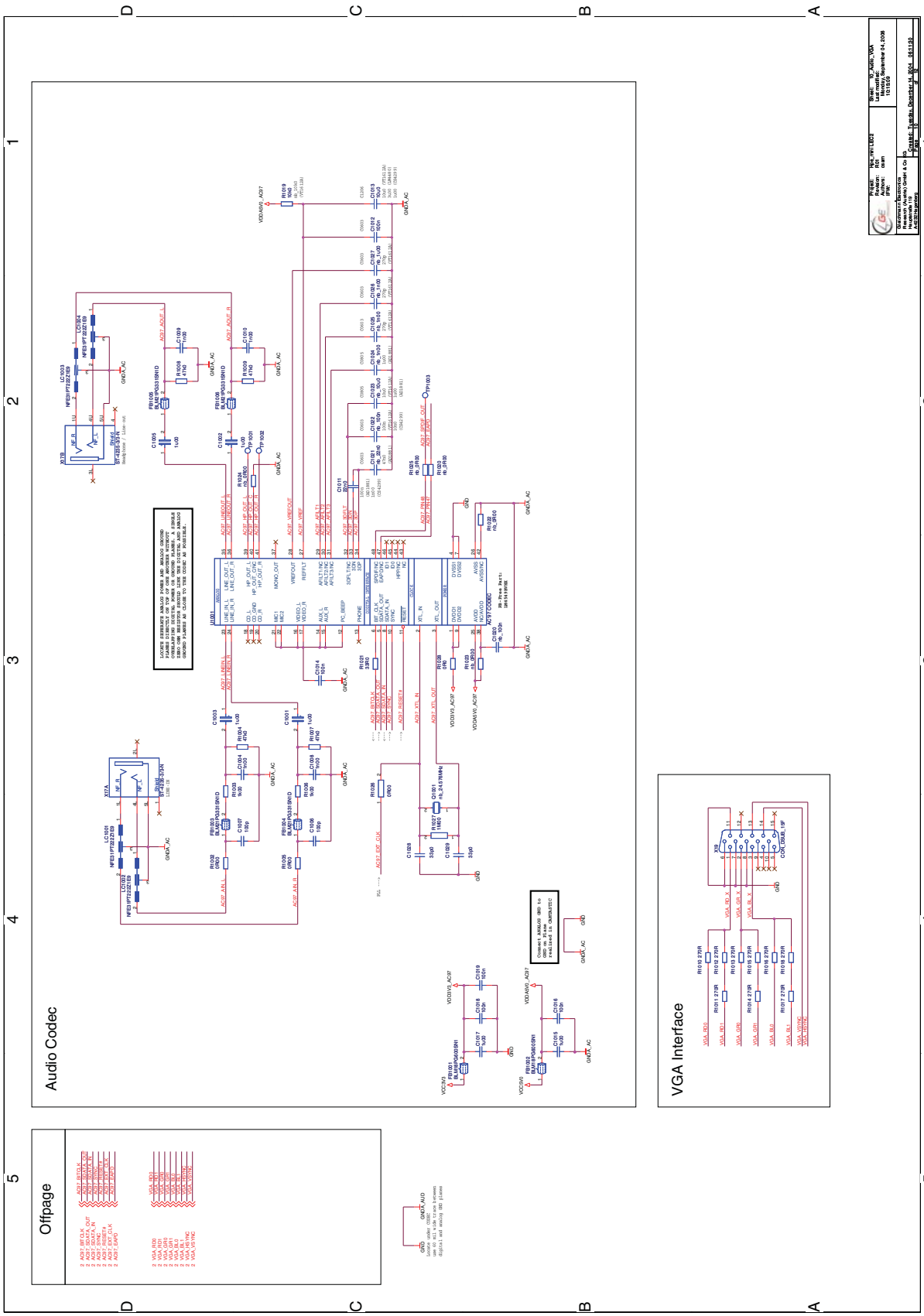


Figure 29.

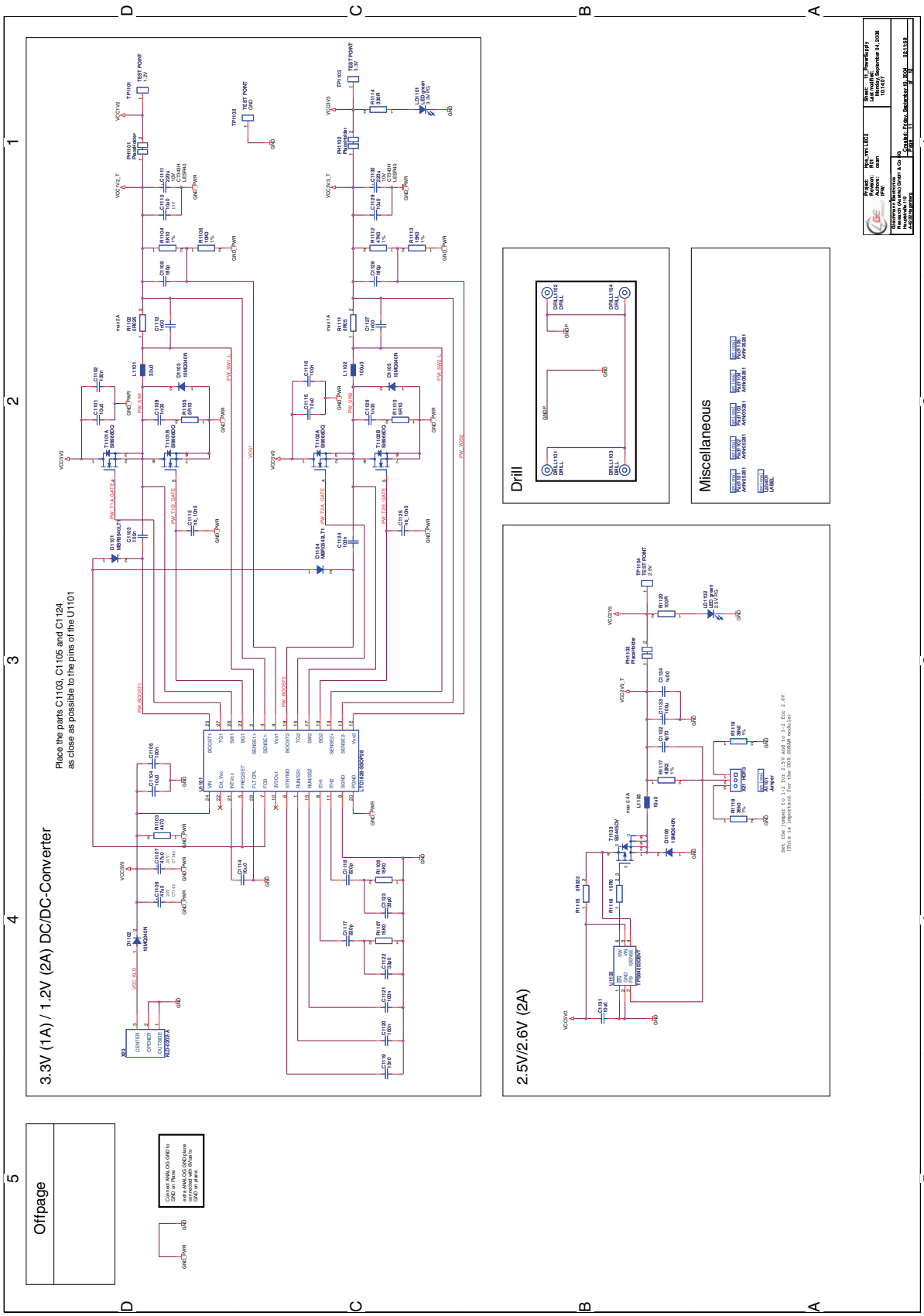
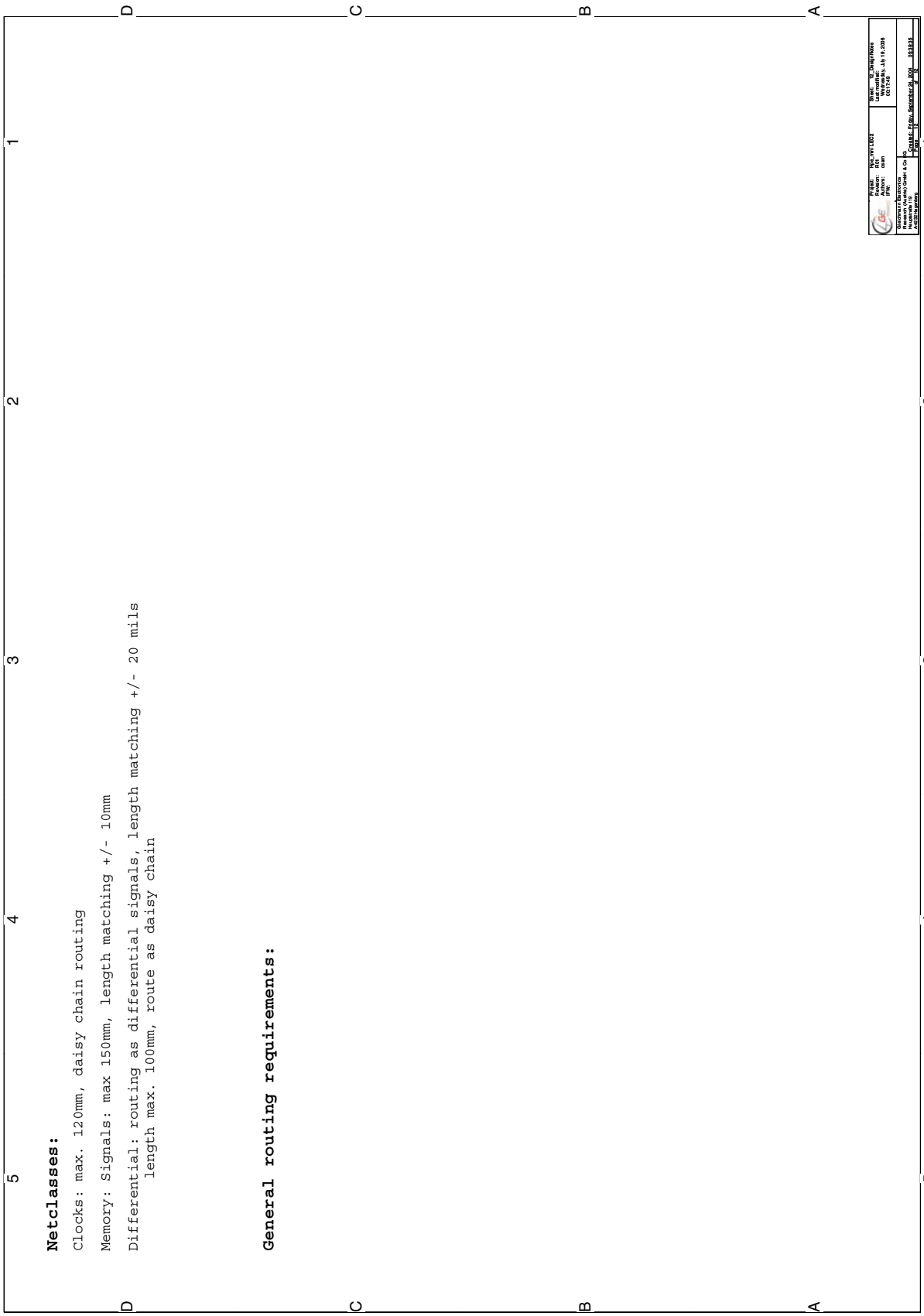

3.3V (1A) / 1.2V (2A) DC/DC-Converter
Place the parts C1103, C1105 and C1124
as close as possible to the pins of the U1101
2.5V/2.6V (2A)
Drill
Miscellaneous
Offpage

Figure 30.


Netclasses:
Clocks: max. 120mm, daisy chain routing
Memory: Signals: max 150mm, length matching +/- 10mm
Differential: routing as differential signals, length matching +/- 20 mils
length max. 100mm, route as daisy chain
General routing requirements: