HDR-60 Base Board – Revision B

User's Guide

April 2014
Revision: EB70_01.2

Introduction

The HDR-60 Base Board provides a low-cost evaluation and demonstration platform to evaluate, test and debug image signal processing user designs or IP, including High Dynamic Range (HDR) cores targeted for the LatticeECP3™-70 FPGA. The HDR-60 Base Board and NanoVesta Head Board have been designed to work together as part of the HDR-60 Video Camera Development Kit. Connections are available on the HDR-60 Base Board for the A-1000 HDRI sensor from Aptina, scalable to future sensors from Aptina, and adaptable to sensors from other manufacturers by redesigning the add-on NanoVesta Head Board. The HDR-60 Base Board features a LatticeECP3-70 FPGA in the 484-ball fpBGA package. The LatticeECP3 I/Os are connected to a rich variety of both generic and application-specific interfaces described later in this document.

Important: This document (including the schematics in Appendix A) describes the HDR-60 Base Board marked as Revision B. This marking can be seen on the silkscreen of the printed circuit board, under the Lattice Semiconductor logo. The following are the changes from Revision A to Revision B.

- *Added R136 and R137*
- *Installed R130 and R131*
- *Moved DVI_DDC_SCL signal to U2 pin D22*
- *Moved DVI_DDC_SDA signal to U2 pin G19*
- *Moved DVI_HPD signal to U2 pin C22*

The LatticeECP3 is a third-generation device utilizing reconfigurable SRAM logic technology optimized to deliver high-performance features such as an enhanced DSP architecture, high-speed SERDES and high-speed source synchronous interfaces in an economical FPGA fabric. The LatticeECP3 devices also provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), and advanced configuration support, including encryption, multi-boot capabilities and TransFR™ field upgrade features. The LatticeECP3 SERDES dedicated PCS functions, high jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII), SATA I/II, OBSAI and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

For a full description of the LatticeECP3 FPGA, including data sheet, technical notes and more, see the Lattice web site at www.latticesemi.com/products/fpga/ecp3.

Some common uses for the HDR-60 Base Board include:

- Security/surveillance and automotive camera applications
- Evaluation of the Helion NanoVesta Head Board and other camera sensors
- Applications using Aptina Head Boards
- Evaluation of Helion IONOS Imaging Pipeline IP cores
- Ethernet IP camera applications
- Evaluation of Teradek H.264 compression modules

Features

Key features of the HDR-60 Base Board include:

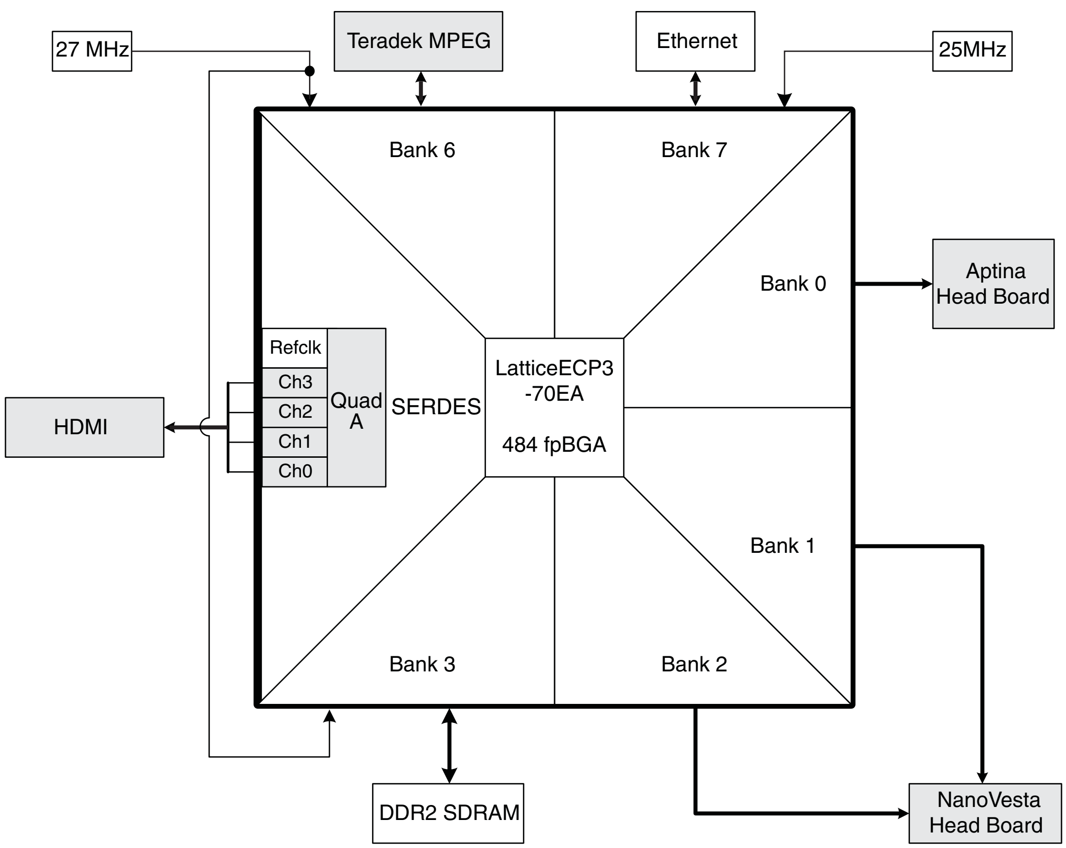
- SPI serial Flash device included for low-cost, non-volatile configuration storage
- DDR2 SDRAM: 16-bit data over a 32M address space
- Tri-speed (10/100/1000 Mbit) Ethernet PHY with RJ-45 (includes 12 core magnetics)

- Built-in USB 2.0 download to LatticeECP3
- Can be configured for a flywire ispDOWNLOAD™ cable connection
- HiSPi and parallel video data path connections with selectable VCCIO (1.8 V/2.5 V/3.3 V)
- Connectors for Aptina standard Head Board with USB 2.0 interface
- Connector for Teradek Capella H.264 codec board
- Test point connections to 19 I/O pins for prototyping
- Two MEMS and two crystal oscillators
- HDMI/DVI output using four channels (one quad) of differential SERDES
- 5.0 V, 3.3 V, 2.5 V, 1.8 V, 1.2 V voltages are generated from a single 12 V power source
- ispVM™ System programming support

General Description

The heart of the HDR-60 Base Board is the LatticeECP3 FPGA. The devices and connectors attached to the LatticeECP3 provide a means to investigate applications developed for High Dynamic Range image signal processing. The board also provides several different interconnections and support devices that permit it to be used for a variety of purposes. The HiSPi and parallel video input, DDR2 memory, Tri-speed Ethernet PHY, and HDMI output are useful for applications using Lattice IP cores. A modest number of test points were added around the board for general purpose LatticeECP3 I/O usage. The SPI memory showcases the fail-safe capabilities of the LatticeECP3. Figure 1 is the block diagram for the HDR-60 Video Camera Development Kit.

Figure 1. HDR-60 Video Camera Development Kit Block Diagram



Initial Setup and Handling

The following is recommended reading prior to removing the evaluation board from the static shielding bag and may or may not apply to your particular use of the board.

CAUTION: The devices on the board can be damaged by improper handling.

The devices on the evaluation board contain fairly robust ESD (Electro Static Discharge) protection structures within them, able to withstand typical static discharges (see the “Human Body Model” specification for an example of ESD characterization requirements). Even so, the devices are static sensitive to conditions that exceed their designed in protection. For example: higher static voltages, as well as lower voltages with lower series resistance or larger capacitance than the respective ESD specifications can potentially damage or degrade the devices on the evaluation board.

As such, it is recommended that you wear an approved and functioning grounded wrist strap at all times while handling the evaluation board when it is removed from the static shielding bag. If you will not be using the board for a while, it is best to put it back in the static shielding bag. Please save the static shielding bag and packing box for future storage of the board when it is not in use.

When reaching for the board, it is recommended that you first touch the ground plane of the board (for example, the metal shielding of the HDMI connector). This will neutralize any static voltage difference between your body and the board prior to any contact with signal I/O.

CAUTION: To minimize the possibility of ESD damage, the first and last electrical connections to the board should always be from test equipment chassis ground to the ground plane of the board.

Before connecting signals or power to the board, attach a cable from chassis ground on grounded test equipment to the ground plane of the board. Connecting the board ground to test equipment chassis ground will decrease the risk of ESD damage to the I/O on the board as the initial connections to the board are made. Likewise, when unplugging cables from the evaluation board, the last connection unplugged, should be the chassis GND connection to the evaluation board GND. If you have a signal source that is floating with respect to chassis GND, attempt to neutralize any static charge on that signal source prior to attaching it to the evaluation board.

If you are holding or carrying the board when it is not in a static shielding bag, please keep one finger on the ground plane of the board, for example the metal shielding of the HDMI connector. This will keep the board at the same voltage potential as your body until you can pick up the static shielding bag and put the board back in it.

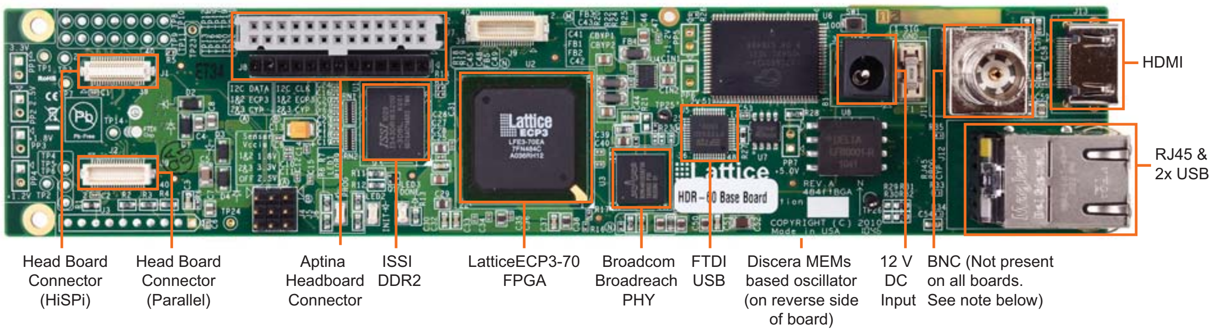
Electrical, Mechanical, and Environmental Specifications

The nominal board dimensions are 203.2 mm x 42 mm (8.000” x 1.654”). Additional mechanical board dimension information is included on the mechanical drawing shown in Appendix A, Figure 24. On the physical board itself, connectors include pin 1 indictors as either an arrow, or triangle point near pin 1 on the outer layer silk screen. The environmental specifications are as follows:

- Operating temperature: 0 °C to 55 °C
- Storage temperature: -40 °C to 75 °C
- Humidity: <95% without condensation
- 11 V to 18 V DC (20 watts max.)

Functional Description

Figure 2. HDR-60 Base Board, Top View



Note: The BNC connector (J11), and Delta Filter (U8) are designed for Ethernet-over-BNC.
This is an unsupported feature. These components are not populated on most manufacturing runs of this board.

LatticeECP3 Device

This board features a LatticeECP3-70 FPGA with a 1.2 V DC core in a 484-ball fpBGA package. The LatticeECP3-35, -70 and -95 device densities in this package can be accommodated with no change in pin connections. A complete description of this device can be found on the Lattice web site at www.latticesemi.com/products/fpga/ecp3.

Power Connector (J10)

The board is supplied by a single 12 V DC power supply at J10. On-board step-down switching regulators then provide the necessary supply voltages: 3.3 V, 2.5 V, 1.8 V, 1.2 V. For proper operation, the 12 V DC power applied at J10 should be within the range of +11 V min. to +18 V max. The requirements for the J10 power jack itself are listed in Table 1.

Table 1. Power Jack J10 Specifications

Polarity	Positive Center
Inside Diameter	0.1” (2.5mm)
Outside Diameter	0.218” (5.5mm)
Current Capacity	Up to 2.5A

The on-board switching regulator output voltages can be measured at test points located around the board as shown in Table 2.

Table 2. Test Points for On-Board Regulator Voltages

Supply	Switching Regulator	Test Point	Resistor Ratio	Comment
5.0 V	U15	PP7	R123/R122	
3.3 V	U10 (side 2)	PP1	R46/R45	
2.5 V	U10 (side 1)	PP2	R53/R5 (default) (R56 and R51 modify ratio)	1.8 V: jumper on J4 pins 1-2 2.5 V: no jumper on J4 (default) 3.3 V: jumper on J4 pins 2-3
1.8 V	U11 (side 2)	PP3	R55/R6	
1.2 V	U11 (side 1)	PP4	R54/R52	

Each of the step-down switching regulators, U10, U11, and U15, incorporate typical resistor divider voltage feedback to divide down the regulator output voltage and compare it against an internal reference voltage. The regulator then adjusts the output voltage higher or lower such that the resistor divided voltage matches the internal reference. By doing this, the regulator output voltage remains at a constant voltage value independent of the load driven. Each regulator output voltage follows this equation:

V_{out} = (1 + resistor ratio) x (regulator internal reference voltage)

See the LT3503 and LT3508 device data sheets for additional details about these devices.

The 2.5 V regulator output voltage can also be set to 1.8 V or 3.3 V by adding a shorting jumper on J4, as shown in Table 2. With no jumper on J4, the voltage divider is set by R53 and R5 and this divider sets up a nominal 2.5 V output voltage. When a shorting jumper is added to J4, the R56 and R51 resistors will be placed in parallel with either R53 or R5, which then changes the resistor divider ratio, and this changes side 1 of the U10 regulator output voltage to become 1.8 V or 3.3 V depending on the placement of the shorting jumper on J4.

The SERDES 1.2 V regulators (U4) are low dropout linear types that deliver a constant 1.2 V output voltage when powered by the 3.3 V input voltage. In contrast to the switching regulators discussed above, the U4 linear regulars do not generate switching noise, so they are a good choice for powering the LatticeECP3 SERDES to give the lowest jitter generation. Also, U4 does not use resistor divider networks to set the output voltage, instead U4 is set up to directly copy its own internal 1.215 V reference voltage to its outputs. The U4 regulator outputs are available for testing at test points PP5 and PP6. See the LT3029 device data sheets for additional details about this device.

When using the various I/O test points located around the board, be sure to not exceed the LatticeECP3 Family Data Sheet specified absolute maximum rating for Output Supply Voltage VCCIO range of -0.5 V to +3.75 V, or damage to the device may occur. Also, for I/O input capability of the various I/O standards supported by the LatticeECP3 sysIO structures, see the LatticeECP3 sysIO Usage Guide.

LatticeECP3 I/O Bank Voltages

Most of the bank voltages on the LatticeECP3 (U2) have been hard-wired to specific power supply values. Exceptions to this are banks 1 and 2 which can be set to other values used to power the sensor boards that plug into the parallel connector (J2) and HiSPi connector (J1). This is shown in Table 3.

Table 3. LatticeECP3 (U2) Bank Voltage Settings

LatticeECP3 Bank VCCIO	Voltage	Comment
0	3.3 V	Aptina Head Board
1 and 2	Adjustable	Sensor attached to J1 and J2 1.8 V: Jumper on J4 pins 1-2 2.5 V: No jumper on J4 (default) 3.3 V: Jumper on J4 pins 2-3
3	1.8 V	DDR2
Quad A	1.2 V	SERDES
6	3.3 V	Teradek MPEG Encoder
7	3.3 V	Ethernet
8	3.3 V	LatticeECP3 programming

Default Jumper Settings

Figure 3. Default Jumpers

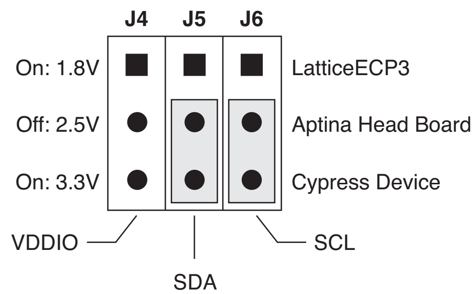


Figure 3 shows the HDR-60 Base Board default jumpers settings for VDDIO set to 2.5 V. By installing a jumper on J4 in the upper position, the VDDIO will change to 1.8 V and on the lower position, the VDDIO will change to 3.3 V.

Only when using the Aptina Head Board, do the serial clock and data signals, J5 and J6 need to be of concern. J5 and J6 select whether the Aptina Head Board will be sourced from the Cypress device (U6) directly or from the LatticeECP3. Moving the jumpers from the lower position on J5 and J6 to the upper position will change the source of the serial clock and data to be from the LatticeECP3 device (U2).

Prototype Areas

For general purpose I/O testing or monitoring, 19 unconnected test points with reference labels TP1, 2, … are provided for direct access to the LatticeECP3 device. Other I/Os on the LatticeECP3 are brought to dedicated connectors such as J1, J2, J7, J8 and J9, which could also be considered as available prototype connectors when they are not in use.

Crystal Oscillators

There are two crystal oscillators and two MEMS-based oscillators on the HDR-60 Base Board. The two crystals are used for the two USB port connections. One MEMS-based oscillator is used to set the reference frequency for the Ethernet PHY, while the other is used to drive inputs to the LatticeECP3 (U2). Table 4 shows the oscillator usage. Locations Y1 and Y4 are the MEMS-based oscillators.

Table 4. Crystal Oscillators Used on the HDR-60 Base Board

Location	Frequency	Comment	LatticeECP3 Input I/O Setting
Y1	27.000 MHz	DDR2 U2 pin R17 MPEG U2 pin T3	SSTL18 (no term) LVCMOS33
Y2	6.000 MHz	USB FTD2232D U5 pin 43 (upper USB port at J12)	—
Y3	24.000 MHz	USB Cypress U6 pin 11 (lower USB port at J12)	—
Y4	25.000 MHz	Ethernet PHY U3 pin F1	—

DVI Video Output

The LatticeECP3 (U2) SERDES Quad A outputs drive the HDMI connector (J13) through inline AC coupling capacitors C55, C56, C57, C58, C218, C219, C220, and C221. The SERDES signal paths are 50 ohms between the LatticeECP3 outputs to the HDMI connector on the HDR-60 Base Board. The DVI signal connections between the LatticeECP3 device and the HDMI connector are shown in Table 5.

Table 5. LatticeECP3 (U2) Connections to HDMI Output (J13)

J13 Pin	LatticeECP3 I/O	Polarity	sysIO Bank	Signal Name
10	AB15	P	Quad A	DVI_HDOUTP0
12	AB14	N	Quad A	DVI_HDOUTN0
7	AB12	P	Quad A	DVI_HDOUTP1
9	AB13	N	Quad A	DVI_HDOUTN1
4	AB11	P	Quad A	DVI_HDOUTP2
6	AB10	N	Quad A	DVI_HDOUTN2
1	AB8	P	Quad A	DVI_HDOUTP3
3	AB9	N	Quad A	DVI_HDOUTN3
13	—	—	—	CEC_OUT
15	E18	—	8	DVI_DDC_SCL
16	E17	—	8	DVI_DDC_SDA
19	A20	—	8	DVI_HPD

HiSPi Connector (J1)

The LatticeECP3 (U2) banks 1 and 2 can receive HiSPi sub-LVDS video signals from connector J1. When receiving HiSPi signals, you will need to set the LatticeECP3 input type to LVDS with differential 100 ohm termination. The signal connections between the LatticeECP3 device and the HiSPi connector are shown in Table 6.

Table 6. LatticeECP3 (U2) Interface to HiSPi Connector J1

J1 Pin	LatticeECP3 I/O BGA Ball	Polarity	sysIO Bank	Differential Signal	Parallel Signal
13	K21	P	2	SLVS_0P	—
11	L21	N	2	SLVS_0N	—
29	L22	P	2	SLVS_1P	—
27	M22	N	2	SLVS_1N	—
21	P21	P	2	SLVS_2P	—
19	N22	N	2	SLVS_2N	—
26	M18	P	2	SLVS_3P	—
24	N17	N	2	SLVS_3N	—
14	L18	P	2	SLVS_4P	—
12	L19	N	2	SLVS_4N	HISPI_LED
22	K20	P	2	SLVS_5P	—
20	K19	N	2	SLVS_5N	—
17	K17	P	2	SLVS_6P	—
15	K18	N	2	SLVS_6N	—
25	H21	P	2	SLVS_7P	—
23	H22	N	2	SLVS_7N	—
18	M21	P	2	SLVS_CP	—
16	M20	N	2	SLVS_CN	—
10	C13	—	1	—	HISPI_RESETN
28	K22	—	2	Note 1	RESERVED_1
30	J22	—	2	Note 1	HISPI_SDATA
32	C14	—	1	—	HISPI_SCLK
4	A13	—	1	—	VDDIO_rH

1. Routed on the HDR-60 Base Board as a differential pair.

Parallel Connector (J2)

The LatticeECP3 (U2) bank 1 receives parallel video signals from connector J2. The signal connections between the LatticeECP3 device and the HiSPi connector are shown in Table 7.

Table 7. LatticeECP3 (U2) Interface to Parallel Connector J2

J2 Pin	LatticeECP3 I/O BGA Ball	sysIO Bank	Parallel Signal	Differential Signal
16	J20	2	DOUT0	SLVS_8N
20	G22	2	DOUT1	SLVS_9N
15	F22	2	DOUT2	SLVS_11N
19	J18	2	DOUT3	SLVS_10N
14	A16	1	DOUT4	—
18	J19	2	DOUT5	SLVS_8P
13	C16	1	DOUT6	—
17	E22	2	DOUT7	SLVS_11P
22	G21	2	DOUT8	SLVS_9P
24	G14	1	DOUT9	—
21	J17	2	DOUT10	SLVS_10P
23	C17	1	DOUT11	—
10	C12	1	PIXCLK	—
9	A19	1	EXTCLK_FPGA	—
11	A18	1	LINE_VALID	—
12	B16	1	FRAME_VALID	—
25	B18	1	TRIGGER	—
27	A17	1	RESET_BAR	—
29	F16	1	OUTPUT_EN_BAR	—
31	F15	1	STANDBY	—
26	G15	1	SADDR	—
28	D15	1	SCLK	—
30	C15	1	SDATA	—
32	E15	1	OSC_ENABLE	—
4	A12	1	VDDIO_rP	—

Aptina Head Board Connector

Connectors J7 and J8 make up the Aptina Head Board connector. They are described below. Note that jumpers J5 and J6 may be required to be in the 2 and 3 positions if using Aptina DevWare software. Contact Aptina for details on running DevWare on the HDR-60 Base Board.

Dual Row Connector (J7)

The LatticeECP3 (U2) bank 0 interfaces to the Aptina dual row connector (J7) as shown in Table 8.

Table 8. LatticeECP3 (U2) Interface to Aptina Dual Row Connector (J7)

J7 Pin	LatticeECP3 I/O BGA Ball	sysIO Bank	Signal
1	C8	0	HEAD_DOUT0
2	C7	0	HEAD_DOUT1
3	F9	0	HEAD_DOUT2
4	E9	0	HEAD_DOUT3
5	C9	0	HEAD_DOUT4

Table 8. LatticeECP3 (U2) Interface to Aptina Dual Row Connector (J7) (Continued)

J7 Pin	LatticeECP3 I/O BGA Ball	sysIO Bank	Signal
6	C10	0	HEAD_DOUT5
7	B7	0	HEAD_DOUT6
8	A7	0	HEAD_DOUT7
9	B8	0	HEAD_DOUT8
10	A8	0	HEAD_DOUT9
13	A3	0	HEAD_LINE_VALID
14	B6	0	HEAD_SP5
15	G9	0	HEAD_SP7
16	F7	0	HEAD_SENSOR_RESETN
17	A4	0	HEAD_FRAME_VALID
19	E7	0	HEAD_SHIP_CLK
20	F8	0	HEAD_SP6
23	F11	0	HEAD_PIXCLK
26	D6	0	HEAD_MCLK

Aptina Single Row Connector (J8)

The LatticeECP3 (U2) bank 0 interfaces to the Aptina single row connector (J8) as shown in Table 9.

Table 9. LatticeECP3 (U2) Interface to Aptina Single Row Connector (J8)

J2 Pin	LatticeECP3 I/O BGA Ball	sysIO Bank	Signal
1	F10	0	HEAD_DOUT10
2	E10	0	HEAD_DOUT11
3	A9	0	HEAD_DOUT12
4	B10	0	HEAD_DOUT13
5	A10	0	HEAD_DOUT14
6	A11	0	HEAD_DOUT15
7	C5	0	HEAD_SP0
8	B4	0	HEAD_SP1
9	E6	0	HEAD_SP2
10	D5	0	HEAD_GSHT_CTL
11	C6	0	HEAD_TRIGGER

Teradek MPEG Encoder Connector

The LatticeECP3 (U2) bank 6 I/Os connect to the Teradek MPEG Encoder Connector (J9). The signal connections are shown in Table 10.

Table 10. LatticeECP3 (U2) Connections to Teradek MPEG Encoder (J9)

J9 Pin	LatticeECP3 I/O	sysIO Bank	Signal Name
4	N3	6	MG_VID00
6	P3	6	MG_VID01
8	N5	6	MG_VID02
10	P6	6	MG_VID03
12	P1	6	MG_VID04
14	R1	6	MG_VID05
16	R3	6	MG_VID06

Table 10. LatticeECP3 (U2) Connections to Teradek MPEG Encoder (J9) (Continued)

J9 Pin	LatticeECP3 I/O	sysIO Bank	Signal Name
18	R2	6	MG_VID07
3	W2	6	MG_VID08
5	Y1	6	MG_VID09
7	T4	6	MG_VID10
9	U4	6	MG_VID11
11	AA1	6	MG_VID12
13	Y2	6	MG_VID13
15	Y3	6	MG_VID14
17	AA2	6	MG_VID15
20	P5	6	MG_VID0_PIXCLK
19	T6	6	MG_VID1_PIXCLK
22	U1	6	VGPIO1
26	U2	6	VGPIO2
30	R7	6	VGPIO3
23	N1	6	MG_VSYNC
24	N2	6	MG_HSYNC
25	R4	6	MG_FIELD
27	V3	6	VIDEO_SCL
28	W1	6	VIDEO_SDA
31	L4	6	MG_MCLK_IN
32	W3	6	MG_LRCLK_IN
33	M5	6	MG_BCLK_IN
35	T5	6	MG_SPDIF
34	P7	6	MG_IDAT0
36	V1	6	MG_IDAT1

SPI Serial Flash

The U9 SPI Flash device used on this board is a 16-pin, 64-Mbit device, sufficient to store two bitstreams simultaneously in order to support SPIm mode. The HDR-60 Base Board is configured to download bitstreams stored in the SPI Flash (U9) into the LatticeECP3 when the +12 V power is applied at connector J10. The SPI Flash device is a Numonyx SPI-M25P64 in a 16-pin SOIC package.

Downloading Bitstreams into the LatticeECP3 (U2)

In order to download bitstreams into the LatticeECP3 (U2) device, the HDR-60 Video Camera Development Kit includes two USB-A to USB-A cables that can connect a PC with ispVM System software installed, to the HDR-60 Base Board. Each USB-A to USB-A cable is 6’ (1.83 m) in length. As both ends of the USB cables are the same, either end can plug into a PC’s USB port, while the other end connects to the HDR-60 Base Board J12 upper USB port. The J12 upper USB port connects to a FTD2232D USB transceiver (U5) that can produce JTAG signals able to drive the LatticeECP3 device (U2). Given this, the ispVM System software can detect the LatticeECP3 device, download bitstreams directly into the LatticeECP3 SRAM, or bitstreams can be downloaded into the on board SPI Flash (U9).

Note that the J12 lower USB port has no USB-to-JTAG signal path connections to any Lattice device, so the ispVM System software will not detect any devices at the J12 lower USB port.

See the “Configuring/Programming the Board” section of this document for details on how to download bitstreams into the LatticeECP3 device. See www.latticesemi.com/hdr60 for additional downloadable project files and bitstreams designed for use with this board.

LEDs

There are three LEDs on the HDR-60 Base Board that are used to show the programming state of the LatticeECP3. See Table 11 for information on the programming state LEDs.

Table 11. Programming LEDs

LED	Pin	Color	Function
LED1	PROGRAMN	Red	On when signal is low
LED2	INITN	Red	On when initializing
LED3	DONE	Green	On when configuration is complete

DDR2 Memory

The HDR-60 Base Board is equipped with an 84-ball BGA DDR2 SDRAM such as the IS43DR16320B, which provides memory resources with16 bits of data width that span a 32M address space. The DDR2 memory is powered by an on-board 1.8 V regulator with a 0.9 V midpoint bias termination regulator (U12). The evaluation board includes terminations for address, command and data signals. The suggested configuration is to set the DDR2 SDRAM (U1) for internal 150 ohms ODT, and the LatticeECP3 (U2) address, control and data signals to slow slew, 8 ma, with no ODT. This gives a low-noise, low-power DDR2 memory configuration usable to over 400 MT/s. Table 12 shows the pin connections for both the LatticeECP3 (U2) and DDR2 SDRAM (U1).

Table 12. LatticeECP3 Interface to DDR2 SDRAM

Signal Name	LatticeECP3 I/O Pin (U2)	sysIO Bank	DDR2 SDRAM Pin (U1)
DDR2_DQ0	R22	3	G8
DDR2_DQ1	R20	3	G2
DDR2_DQ2	T20	3	H7
DDR2_DQ3	T22	3	H3
DDR2_DQ4	R21	3	H1
DDR2_DQ5	N19	3	H9
DDR2_DQ6	P22	3	F1
DDR2_DQ7	M19	3	F9
DDR2_DM0	N20	3	F3
DDR2_DQS0_P	N18	3	F7
DDR2_DQS0_N	P19	3	E8
DDR2_DQ8	Y21	3	C8
DDR2_DQ9	V22	3	C2
DDR2_DQ10	W22	3	D7
DDR2_DQ11	W21	3	D3
DDR2_DQ12	U22	3	D1
DDR2_DQ13	Y22	3	D9
DDR2_DQ14	R16	3	B1
DDR2_DQ15	P17	3	B9
DDR2_DM1	R18	3	B3
DDR2_DQS1_P	T21	3	B7
DDR2_DQS1_N	U20	3	A8
DDR2_VREF	P20	3	J2

Table 12. LatticeECP3 Interface to DDR2 SDRAM (Continued)

Signal Name	LatticeECP3 I/O Pin (U2)	sysIO Bank	DDR2 SDRAM Pin (U1)
DDR2_A0	AB19	3	M8
DDR2_A1	R14	3	M3
DDR2_A2	AA21	3	M7
DDR2_A3	V17	3	N2
DDR2_A4	AB17	3	N8
DDR2_A5	W17	3	N3
DDR2_A6	Y17	3	N7
DDR2_A7	W18	3	P2
DDR2_A8	AB18	3	P8
DDR2_A9	U18	3	P3
DDR2_A10	T19	3	M2
DDR2_A11	AA17	3	P7
DDR2_A12	Y19	3	R2
DDR2_BA0	Y18	3	L2
DDR2_BA1	U15	3	L3
DDR2_CK_P	AA22	3	J8
DDR2_CK_N	AB21	3	K8
DDR2_CKE	T18	3	K2
DDR2_RASN	T14	3	K7
DDR2_CASN	V18	3	L7
DDR2_WEN	U16	3	K3
DDR2_ODT	R19	3	K9
DDR2_CSN	U19	3	L8

Ethernet PHY

To the right of the LatticeECP3 FPGA is U3, a Broadcom BCM54810 triple-speed 10/100/1000BASE-T Gigabit Ethernet (GbE) transceiver. The LatticeECP3 FPGA interacts with the PHY over a 3.3 V Gigabit Media Independent Interface (GMII). The PHY is connected to an RJ45 connector J12 at the Media Dependent Interface (MDI). The RJ45 connector J12 has built-in magnetics and link activity indicator LEDs driven by the PHY. The J12 PHY link LEDs are set to indicate the link status, as shown in Table 13.

Table 13. J12 Link Status LEDs

J12 LED Color	Link Status
Orange and Green	1000Base-T
Orange	100Base-T
Green	10Base-T
Yellow	Activity
(off)	No link

The PHY is available on the board in order to demonstrate the Lattice Ethernet Media Access (MAC) IP core. However, it is also possible to use the PHY to evaluate a custom MAC solution.

During power-up, the resistors R21, R22, R23, R24, R25, R103, R105, and R107 set the initialized PHY configuration to: auto-negotiate, full duplex, 10/100/1000Base-T. The PHY can also be programmed after power-up to use a new configuration. The PHY signal path is factory-configured to send and receive 10/100/1000Base-T Ethernet signals at the RJ45 connector (J12). It is possible to change the configuration of the PHY signal path to instead provide a legacy Ethernet coaxial link using the BNC connector (J11) by removing three resistors off the HDR-60 Base Board and then add back on three resistors as shown in Table 14. However, Ethernet-over-BNC is an unsupported feature on this board. The BNC connector and Delta filter (U8) are unpopulated on most production runs of this board. This information is provided as a reference only.

Table 14. Ethernet Connection at J11 or J12 [1]

Connector	Cable	LAN Speed	PCB Configuration
J12 (RJ45)	Cat5	10/100/1000Base-T	R31, R32 = 0 ohms R23 = 4.7K ohms R29, R30, R21 = open
J11 (BNC)	Coaxial	10/100Base-T	R29, R30 = 0 ohms R21 = 4.7K ohms R31, R32, R23 = open

1. J11 (BNC) and U8 (Delta filter) are unpopulated on most manufacturing runs of this board. Ethernet-over-BNC is an unsupported feature of this board. The information in this table is for reference only.

Refer to the HDR-60 Base Board schematic in Appendix A and the Broadcom BCM54810 Data Sheet for detailed information about the operation of the Ethernet PHY interface on this device. Refer to Table 15 for a description of the Ethernet PHY GMII connections to the LatticeECP3.

Table 15. LatticeECP3 Interface to Ethernet PHY

Signal Name	LatticeECP3 I/O Pin (U2)	sysIO Bank	BCM54810 Pin (U3)
PHY_A0	E3	7	H10
PHY_A1	D4	7	J10
PHY_A2	E5	7	J9
PHY_A3	E4	7	K10
PHY_A4	B2	7	K9
GTXCLK	F5	7	A7
ECP3_GSRN	F4	7	--
PHY_LOWPWR	G4	7	F5
MDC	G5	7	E3
TXD0	B1	7	C7
TXD1	G3	7	C8
TXD2	H6	7	B6
TXD3	C1	7	B7
TXD4	H4	7	B8
TXD5	E2	7	B9
TXD6	F3	7	B10
TXD7	H5	7	A10
TX_EN	J4	7	A8
TX_ER	G2	7	A9
CRS	F1	7	E5
COL	H2	7	D5
RESETN	G1	7	E4
RXD0	J1	7	D4
RXD1	K6	7	D3
RXD2	J7	7	C3
RXD3	J3	7	C4
RXD4	J6	7	C5

Table 15. LatticeECP3 Interface to Ethernet PHY (Continued)

Signal Name	LatticeECP3 I/O Pin (U2)	sysIO Bank	BCM54810 Pin (U3)
RXD5	E1	7	B5
RXD6	H3	7	B4
RXD7	H1	7	B3
RX_ER	K3	7	A1
TXC	K4	7	C6
MDIO	K5	7	F4
125MHz	K1	7	B1
RX_DV	L1	7	B2
RXC	L5	7	A2

Configuring/Programming the Board

Requirements

- PC with Lattice ispVM System software version 17.9 (or later) installed with USB driver.
  Note: An option to install this driver is included as part of the ispVM System setup.

For a complete discussion of the LatticeECP3 configuration and programming options, refer to the LatticeECP3 sysCONFIG Usage Guide.

Download Procedures for the Lattice HDR-60 Base Board

The download instructions described below show how to download bitstreams into the LatticeECP3 SRAM using the ispVM System software. Downloads can be either direct through a cable connection to a PC, or indirect by first programming the on-board SPI Flash and then downloading the bitstream to the LatticeECP3 SRAM from SPI Flash. You can download bitstreams through a download cable to the LatticeECP3 SRAM at any time. After a bitstream has been downloaded to SPI Flash, you can download the bitstream from SPI Flash to the LatticeECP3 SRAM by cycling the power to the evaluation board.

The Lattice HDR-60 Base Board provides support for two types of download cable connections: a standard USB-A to USB-A cable at J12, or a Lattice ispDOWNLOAD cable (USB type or parallel port type with flywire connections) at J3 as described in Appendix C. Given that you might want to download to either the LatticeECP3 SRAM or the SPI Flash, separate LatticeECP3 download procedures will follow that cover each type of download.

Note that the first download procedure shows the menus as viewed on a Windows XP operating system. Follow-on download procedures are very similar and do not show the menus.

LatticeECP3 SRAM Configuration Using a Standard USB Cable at J12

The LatticeECP3 SRAM can be configured easily using the ispVM System software to download a bitstream via a standard USB-A to USB-A cable. The LatticeECP3 device is SRAM based, so it must remain powered on to retain its configuration when programming the SRAM.

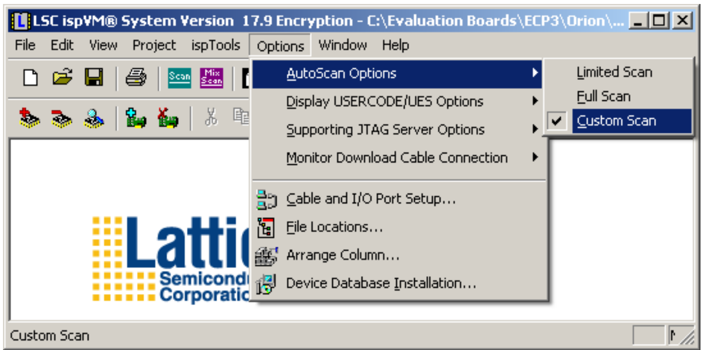
1. Attach a ground connection from test equipment chassis ground to the ground plane of the board, for example, on the metal HDMI connector.

2. Connect the USB-A to USB-A cable from your PC's USB connector to the upper USB port on J12 on the HDR-60 Base Board.

3. Connect the 12 V wall power adaptor cable to J10 and check to see that the wall power adapter is plugged in to a 120 VAC source.

4. Start the ispVM System software. Select the menu items **Options > Autoscan Options > Custom Scan** as shown in Figure 4.

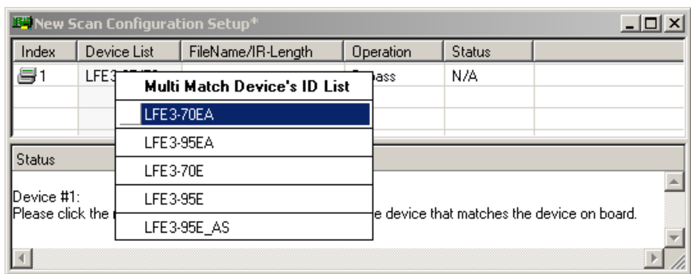
Figure 4. Setting the ispVM Custom Scan Option



5. Select **Options > Cable and I/O Port Setup**. For the Cable Type, select **USB2**, then click **OK**.

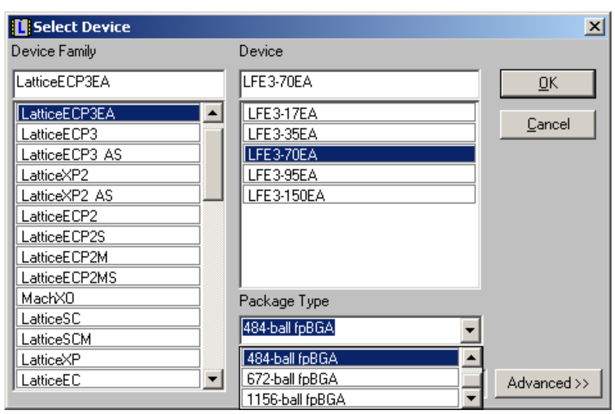
6. Push the **Scan** button. You should now see the LFE3-95/70 device listed in the New Scan Configuration Setup window. In the device list, left-click on the **LatticeECP3** device to select it. If offered other selections, select **LFE3-70EA**. See Figure 5.

Figure 5. ispVM New Scan Configuration Setup



7. Click **Edit > Edit Device** to edit the device. A Device Information window will be opened. Click the **Select** button and select the package type **484-ball fpBGA** as shown in Figure 6, then click **OK.**

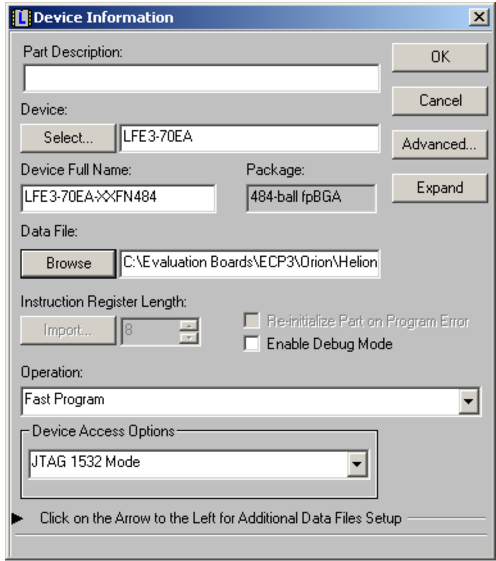
Figure 6. LatticeECP3 Package Size Selection



8. Check that the Device Access Options drop-down menu control selects the **JTAG 1532 Mode**. Check that the Operation drop-down menu selects **Fast Program**.

9. Click the data file **Browse** button and select the path to the LatticeECP3 ".BIT" bitstream file as shown in Figure 7, then click **OK**.

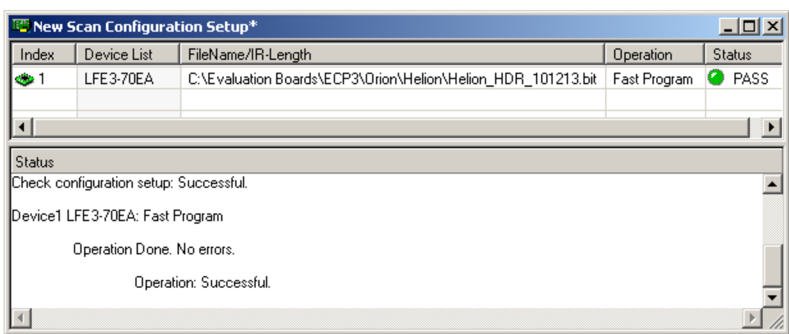
Figure 7. Bitstream Ready to Download into LatticeECP3 SRAM



10. Click **Project >Download** or the green **Go** button to download the bitstream into the LatticeECP3 device (U2). A small window will appear as shown in Figure 8. It will take about 12 seconds to download the bitstream for a PC with USB 2.0 ports. When the LatticeECP3 has loaded in correctly, the ispVM status window will report "Operation Successful" as shown in Figure 9.

Figure 8. Bitstream Downloading into LatticeECP3

Figure 9. Bitstream Download Operation Successful



LatticeECP3 SRAM Configuration Using SPI Flash and USB Cable at J12

The LatticeECP3 SRAM can be configured easily using the ispVM System software to program the on-board SPI Flash via a standard USB cable connected to the upper USB port at J12. The LatticeECP3 device is SRAM-based, so it must remain powered on to retain its configuration when programming the SRAM. The on-board SPI Flash retains its programmed bitstreams when power is off, and can quickly load programmed bitstreams into the LatticeECP3 device when power is applied.

1. Attach a ground connection from test equipment chassis ground to the ground plane of the board, for example on the metal HDMI connector.

2. Connect the USB-A to USB-A cable from your PC's USB connector to the upper USB port on J12 on the HDR-60 Base Board.

3. Connect the 12 V wall power adaptor cable to J10 and check to see that the wall power adapter is plugged in to a 120 VAC source.

4. Start the ispVM System software. Select the menu items **Options** > **Autoscan Options** > **Custom Scan**.

5. Select **Options** > **Cable** and **I/O Port Setup**. For the Cable Type, select **USB2**, then click **OK**.

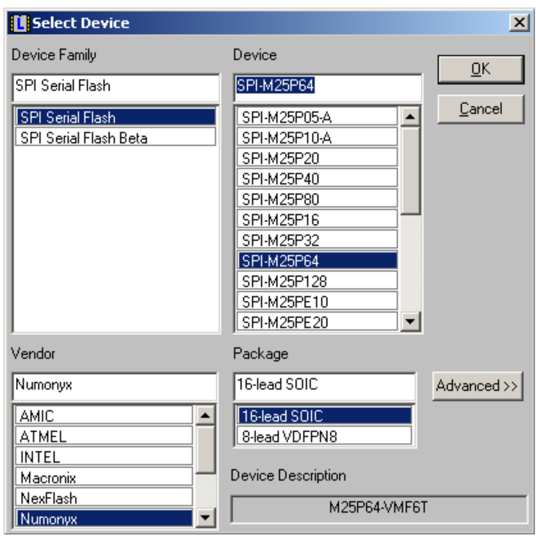
6. Push the **Scan** button. You should now see the LFE3-95/70 device listed in the New Scan Configuration Setup window. In the device list, left-click on the **LatticeECP3** device to select it. If offered other selections, select **LFE3-70EA**.

7. Click **Edit** > **Edit Device** to edit the device. A Device Information window will be opened. Click the **Select** button and select the package type **484-ball fpBGA**, then click **OK**.

8. Click the **Device Access Options** drop-down menu control and select **SPI Flash Background Programming**. A SPI Serial Flash Device window will open.

9. Push the **Select** button and select the Vendor as **Numonyx**, the device as **SPI-M25P64** and the package **16-lead SOIC** as shown in Figure 10. Push the **OK** button.

Figure 10. SPI Flash Device Selection



10. Click the data file **Browse** button and select the path to the LatticeECP3 ".BIT" bitstream file. Push the **Load From File** button and then click **OK** to complete the SPI Flash device selection as shown in Figure 11. Again click **OK** to exit the Device Information menu. The bitstream is now set up for downloading into the SPI Flash as shown in Figure 12.

Figure 11. SPI Flash Device Setup Complete

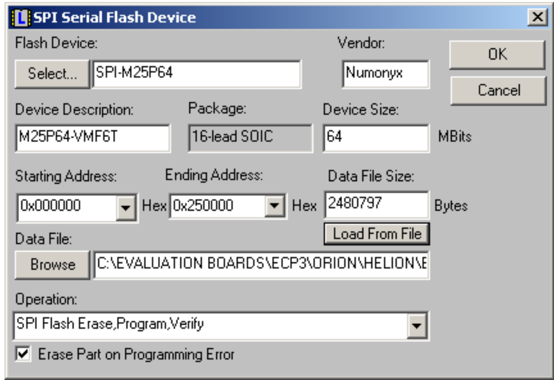
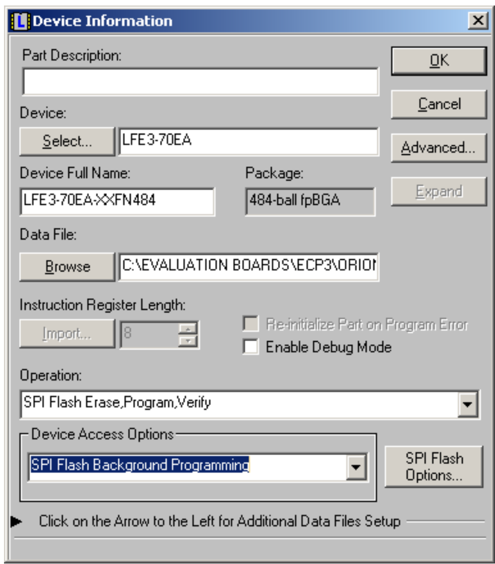


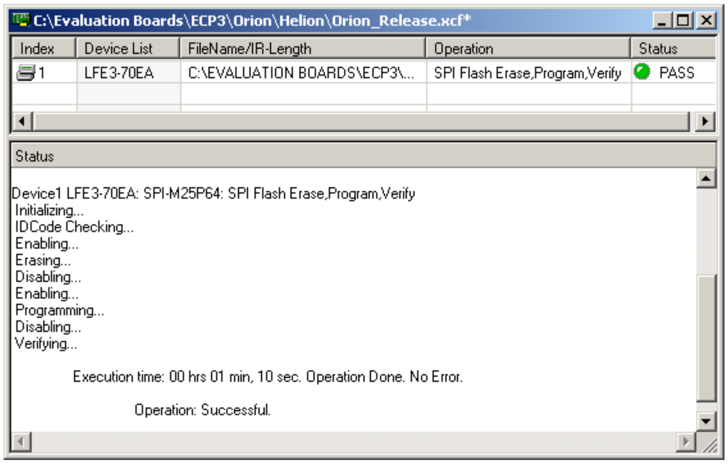
Figure 12. Bitstream Ready to Download into SPI Flash



11. Click **Project** > **Download** or the green **Go** button to download the bitstream into the SPI Flash device (U9), the bitstream download progress indictor will pop up as shown in Figure 13. When using the built-in USB download cable, it will take about two minutes to erase, program and verify the bitstream loaded properly into the SPI Flash for a PC with USB 2.0 ports. After the SPI Flash contents have been verified, the ispVM status window will report "Operation Successful" as shown in Figure 14.

Figure 13. Bitstream Download Progress Indicator

Figure 14. SPI Flash Download Operation Successful



12. Unpower the HDR-60 Base Board for a few seconds then power it back up. The design will load into the LatticeECP3 (U2) from the external SPI Flash (U9) in two seconds, and the “DONE” LED (LED3) will light up.

References

- HDR-60 Video Camera Development Kit web page
- DS1021, LatticeECP3 Family Data Sheet
- HB1009, LatticeECP3 Family Handbook
- QS010, HDR-60 Video Camera Development Kit QuickSTART Guide
- EB63, NanoVesta Head Board User’s Guide
- TN1177, LatticeECP3 sysIO Usage Guide
- TN1169, LatticeECP3 sysCONFIG Usage Guide

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
HDR-60 Video Camera Development Kit *(Contains: HDR-60 Base Board with LatticeECP3 FPGA pre-loaded with Image Signal Processing (ISP) Demo, NanoVesta Head Board with Aptina A-1000 720p HDR Sensor and Sunex lens, two USB cables, HDMI cable with HDMI-to-DVI adapter, 12 V AC adapter power supply, QuickSTART Guide)*	LFE3-70EAHDR60-DKN	
HDR-60 Video Camera Base Board *(Contains: HDR-60 Base Board with LatticeECP3 FPGA pre-loaded with Image Signal Processing (ISP) Demo, two USB cables, HDMI cable with HDMI-to-DVI adapter, 12 V AC adapter power supply, QuickSTART Guide)* Note: Does not include NanoVesta Head Board.	LFE3-70EAHDR60-EVN	

Technical Support Assistance

e-mail: techsupport@latticesemi.com

Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
August 2012	01.0	Initial release.
March 2013	01.1	Added HDR-60 Video Camera Base Board in Ordering Information.
April 2014	01.2	Updated references to BNC connector (J11) and Delta filter (U8) to indicate these are unpopulated on most boards. Ethernet-over-BNC is an unsupported feature of this board.
		Updated Technical Support Assistance information.

Appendix A. Schematic

Figure 15. Block Diagram

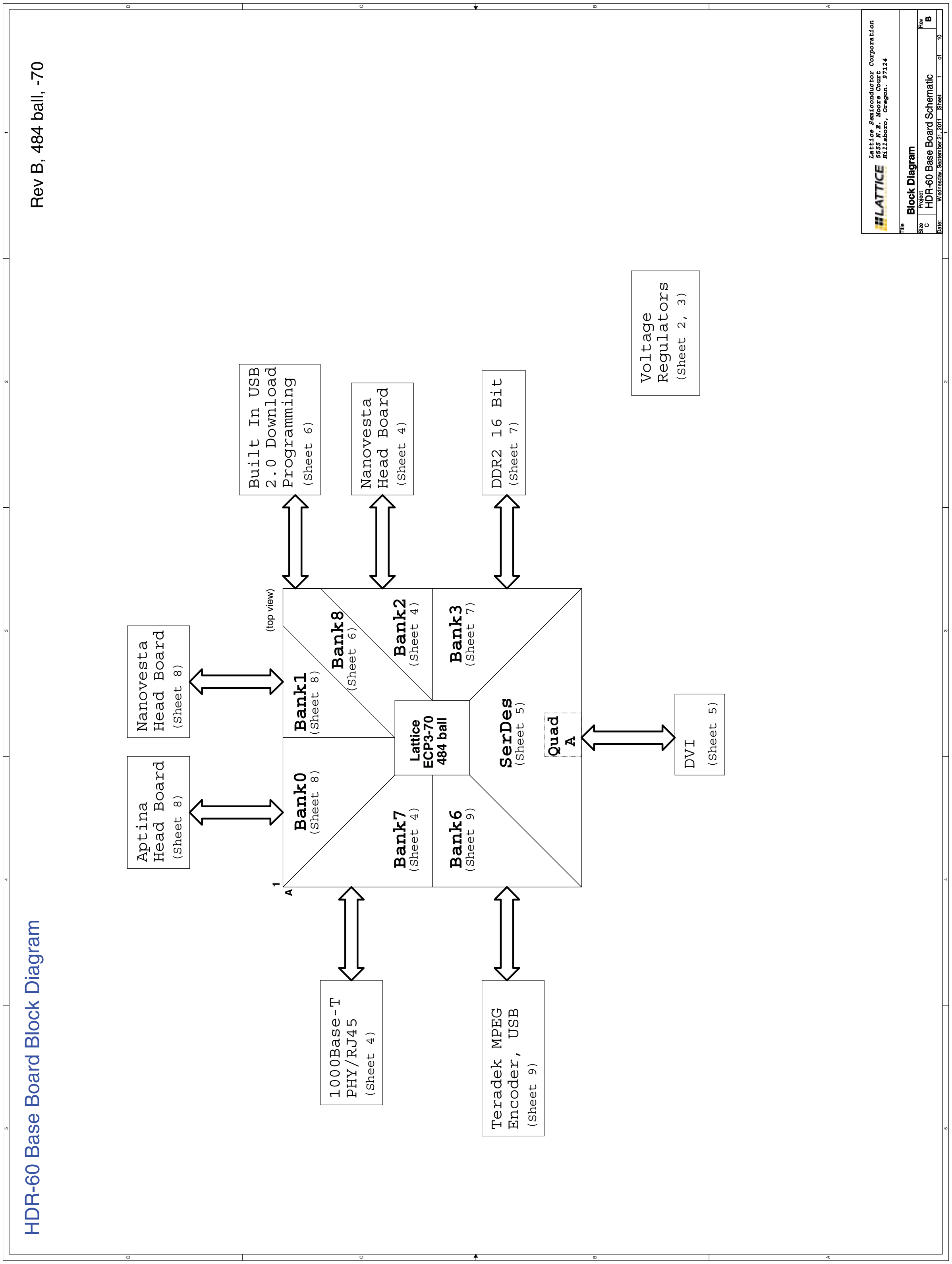


Figure 16. Voltage Regulators

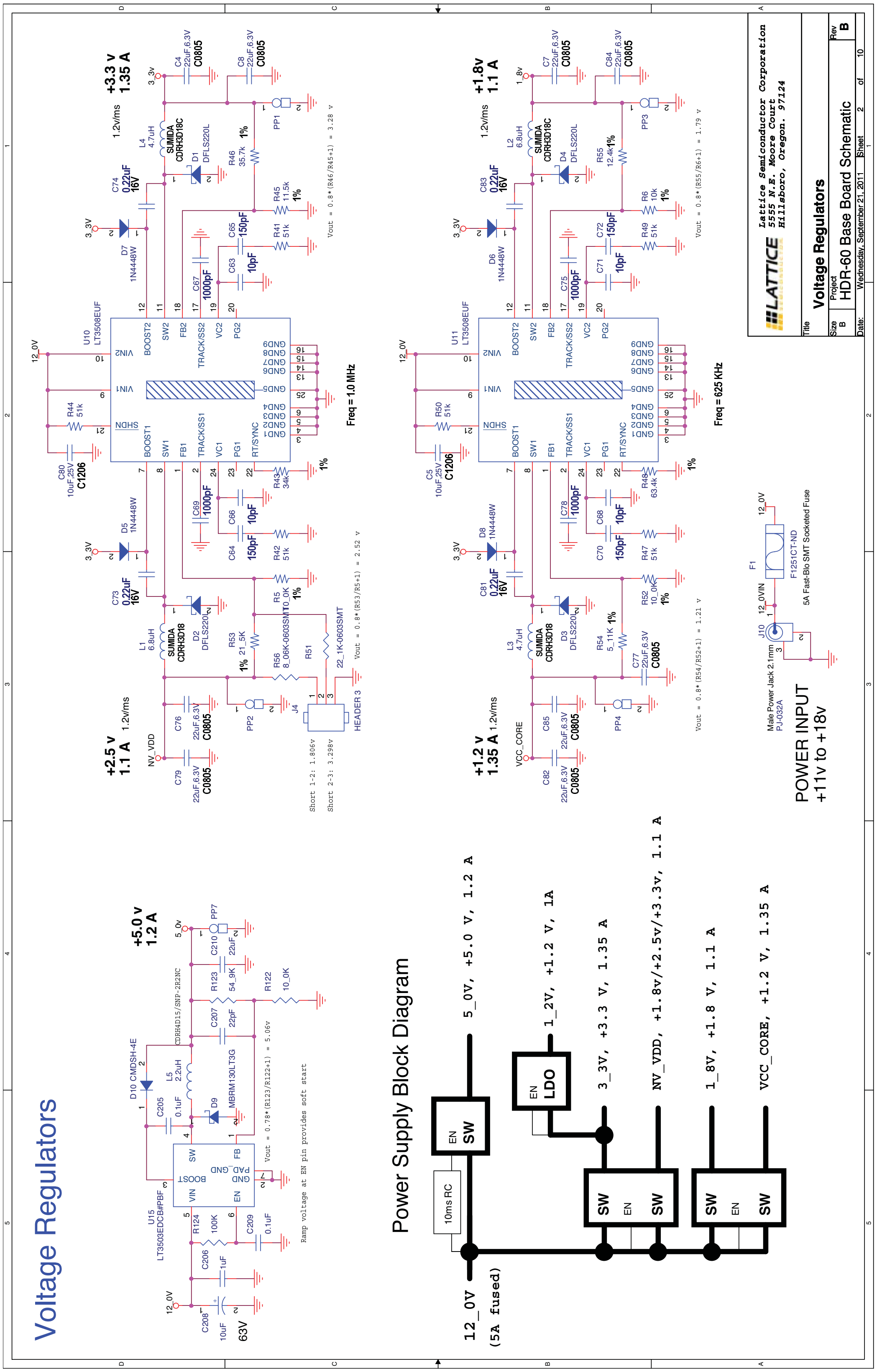


Figure 17. Core Power

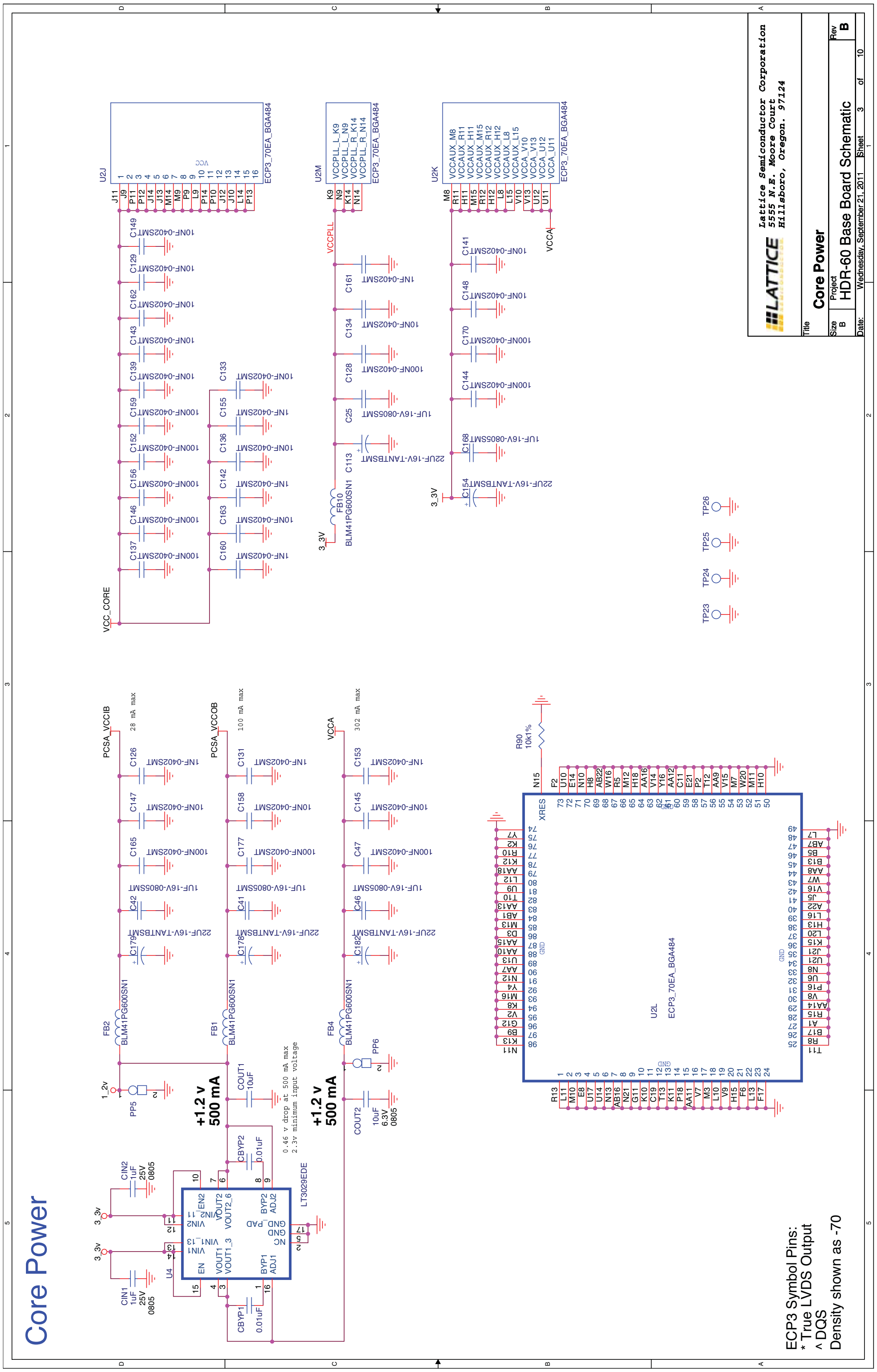


Figure 18. 100Base-T PHY/RJ45

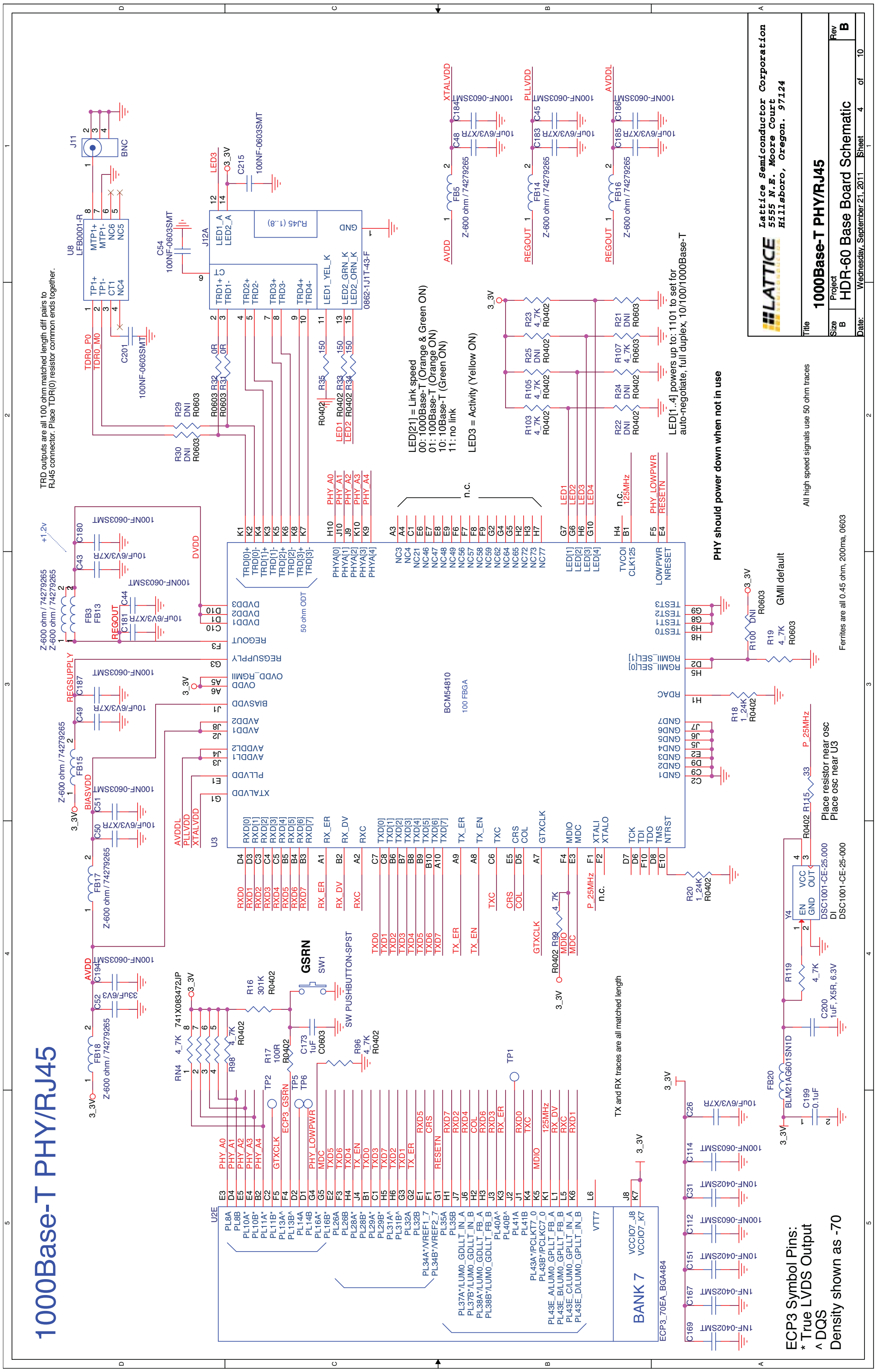


Figure 19. DVI

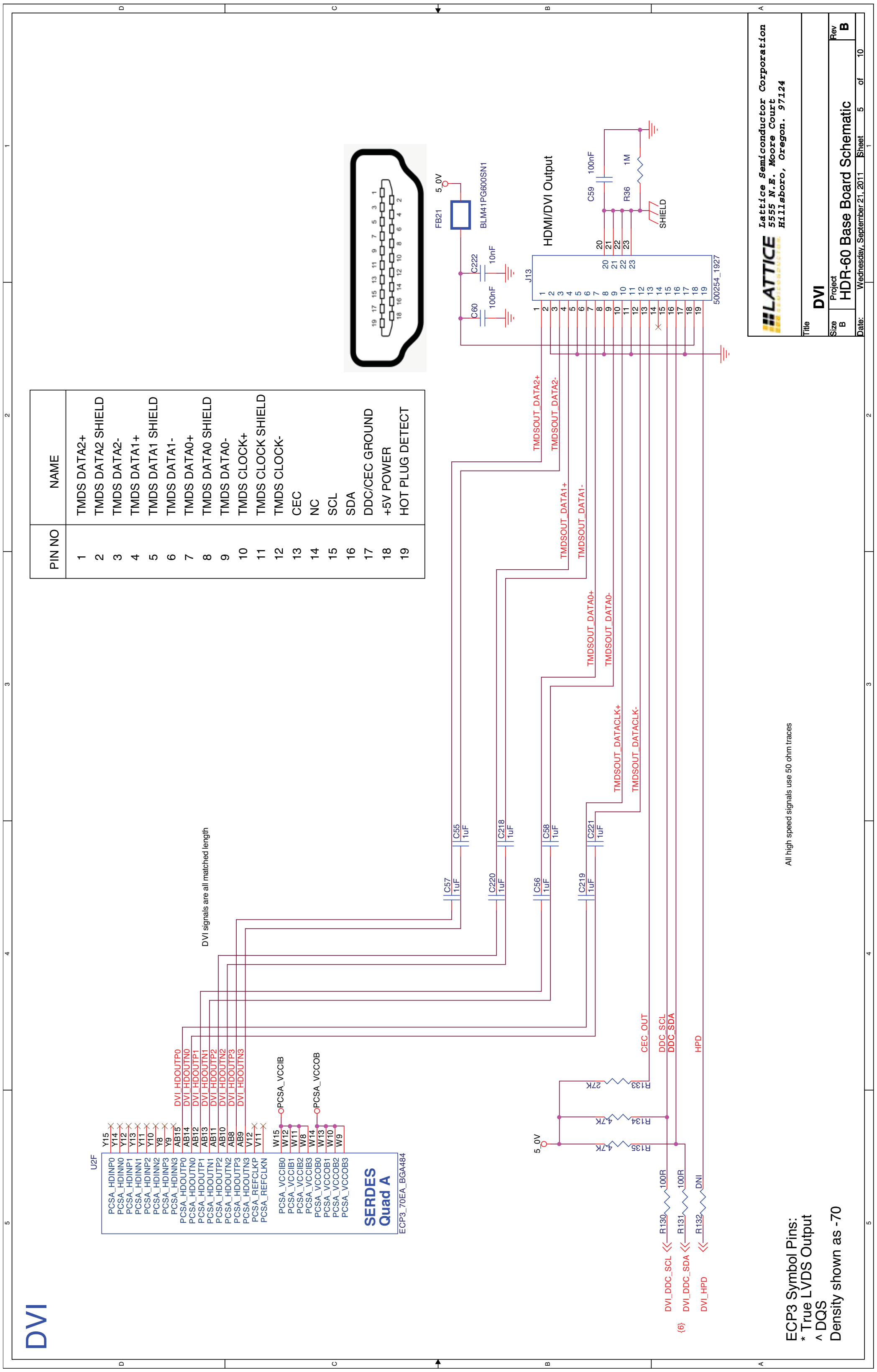


Figure 20. USB Download

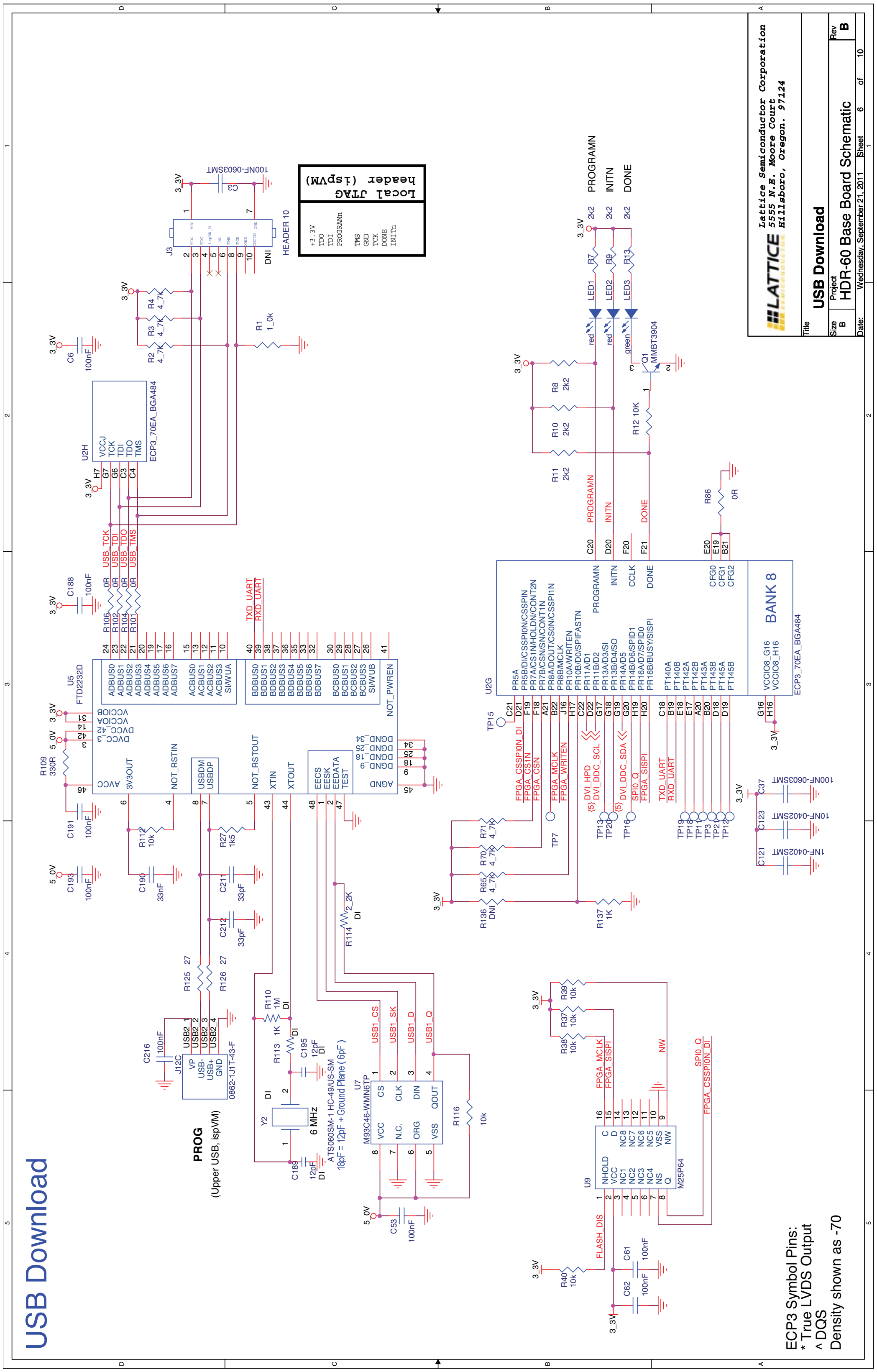


Figure 21. DDR2 Memory

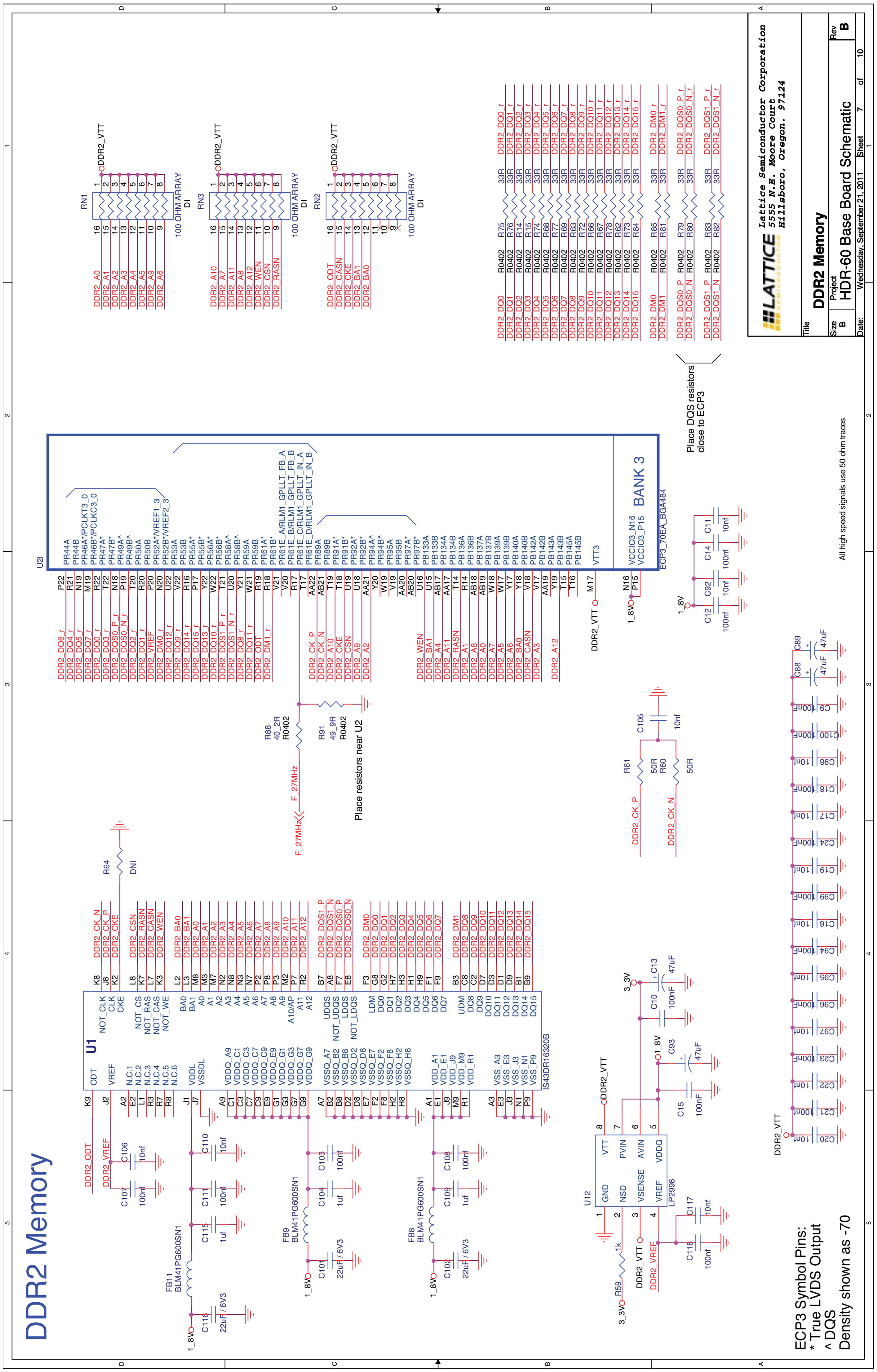


Figure 22. Head Board

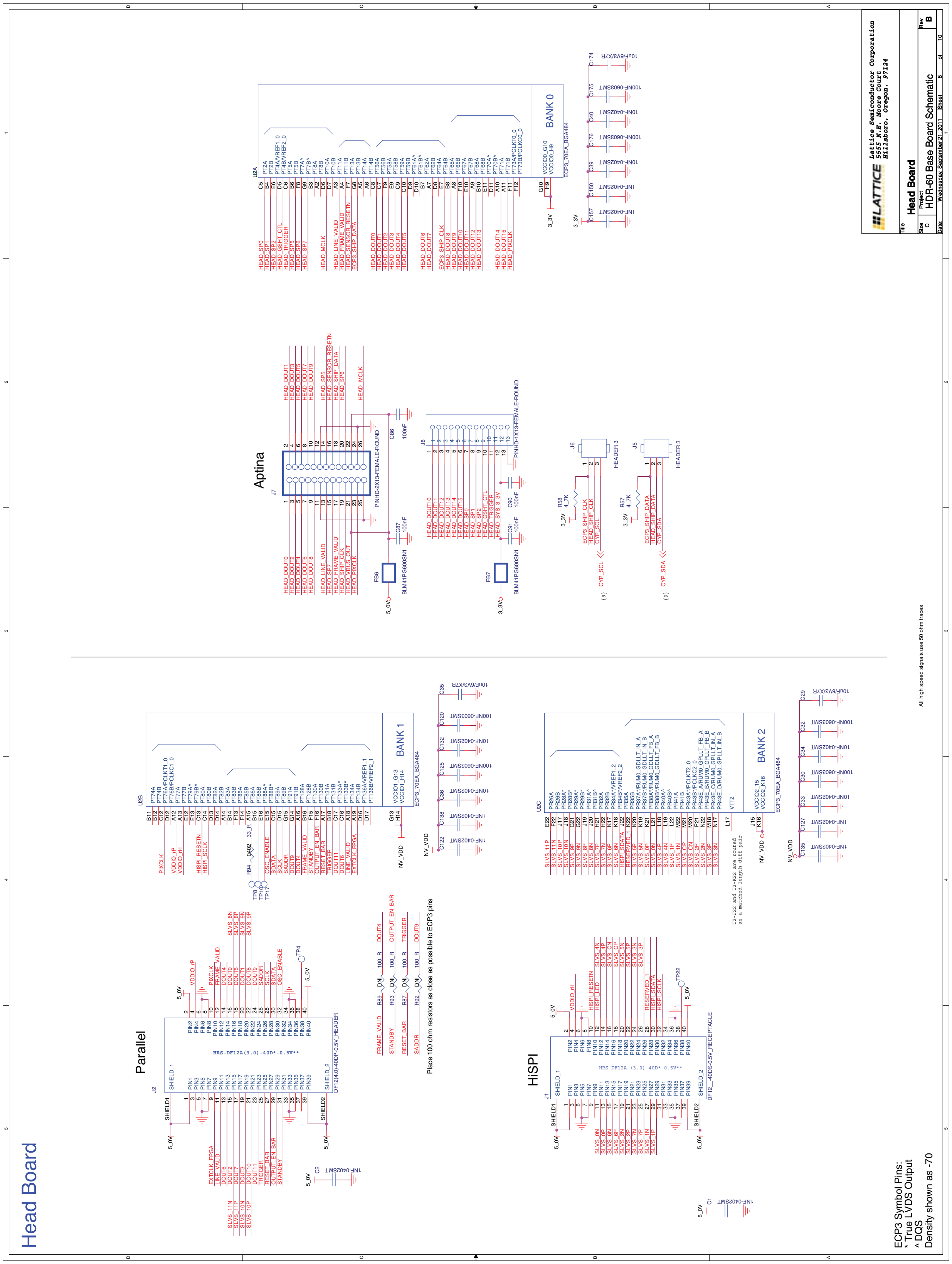


Figure 23. Teradek MPEG Encoder

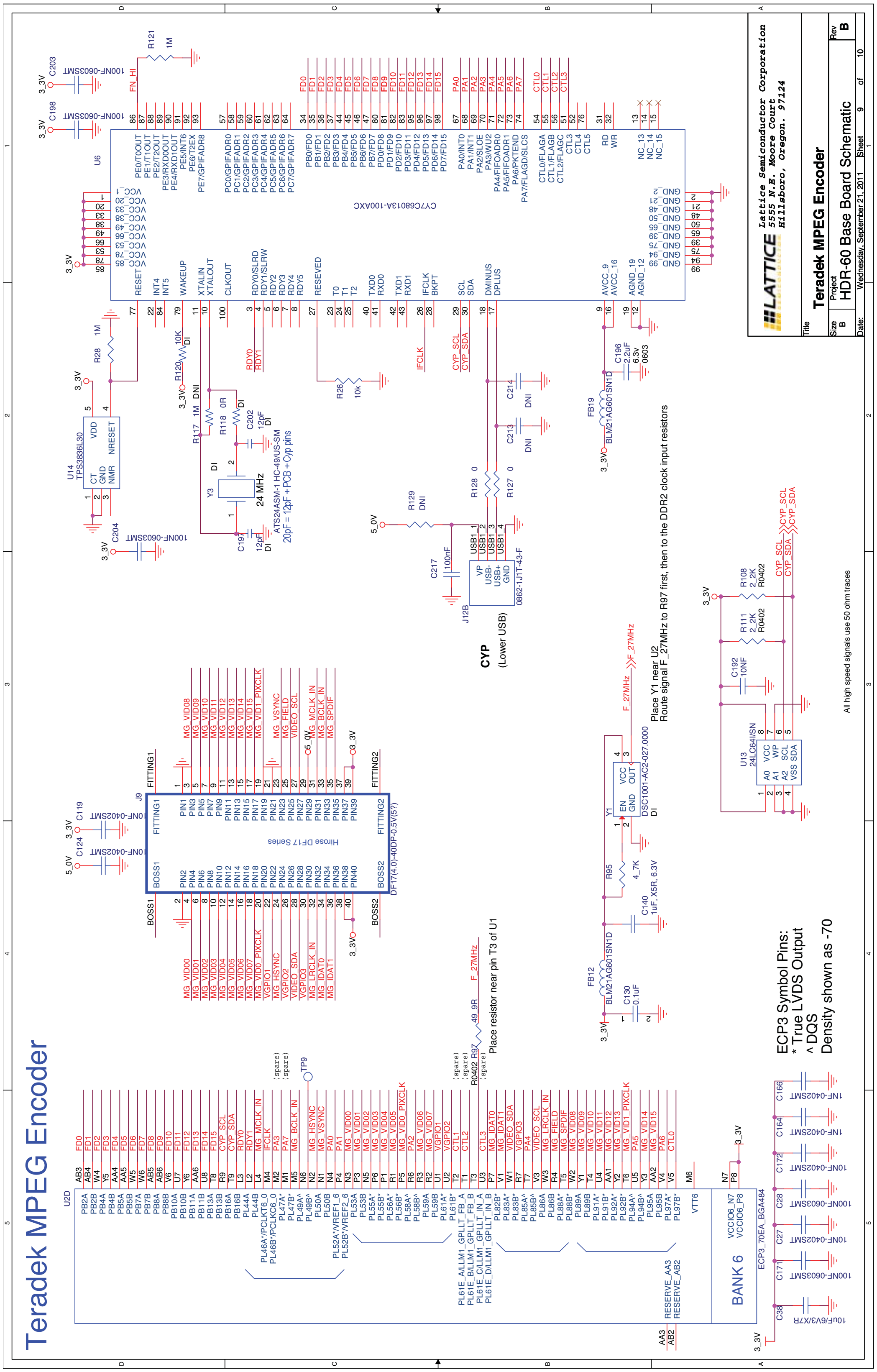
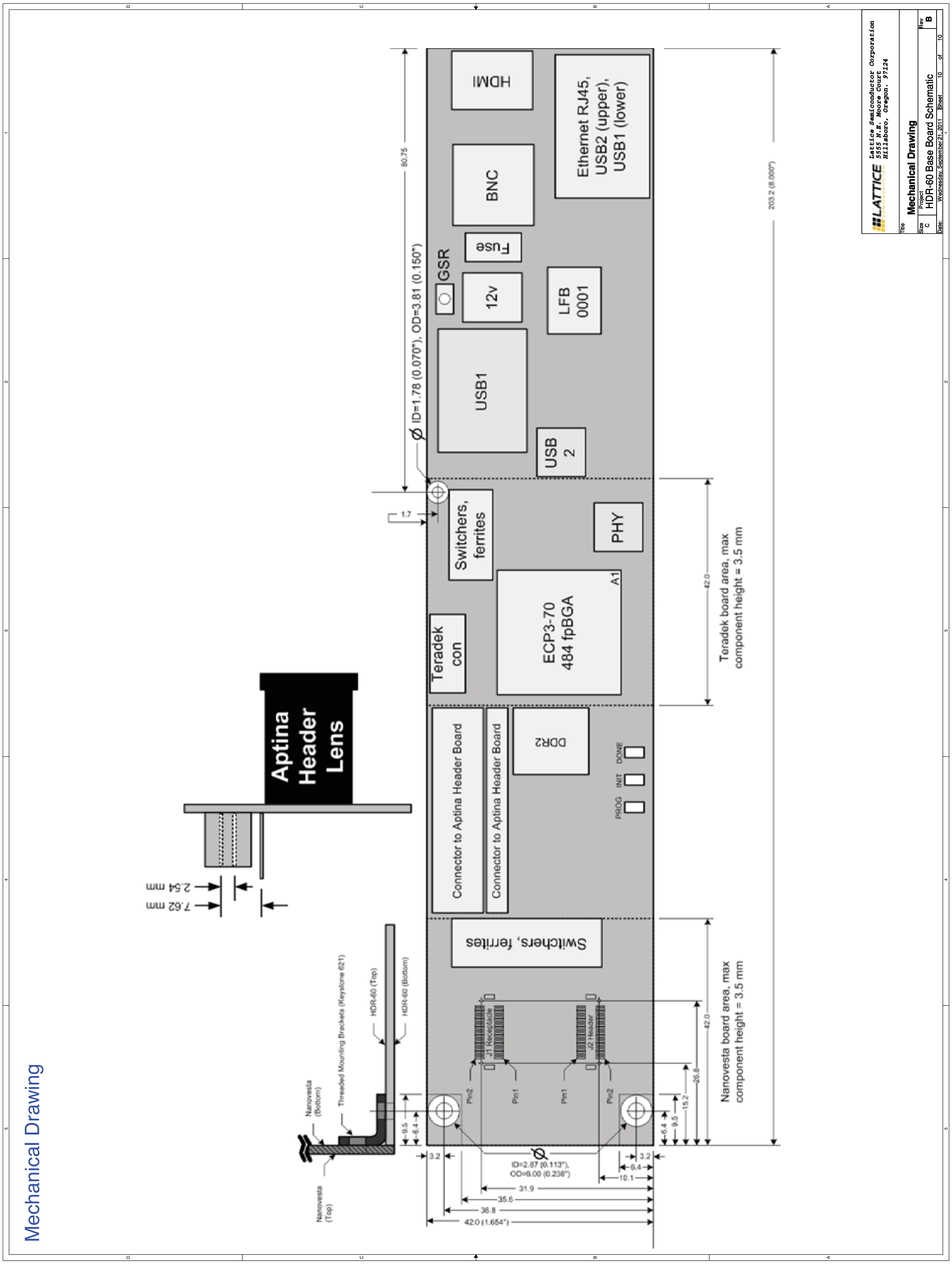
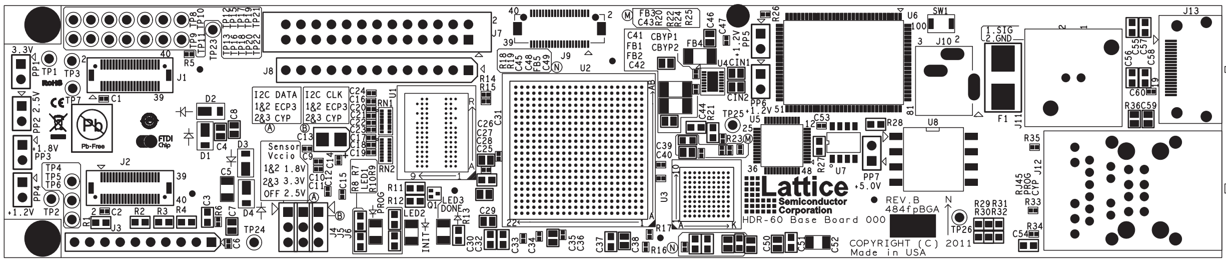
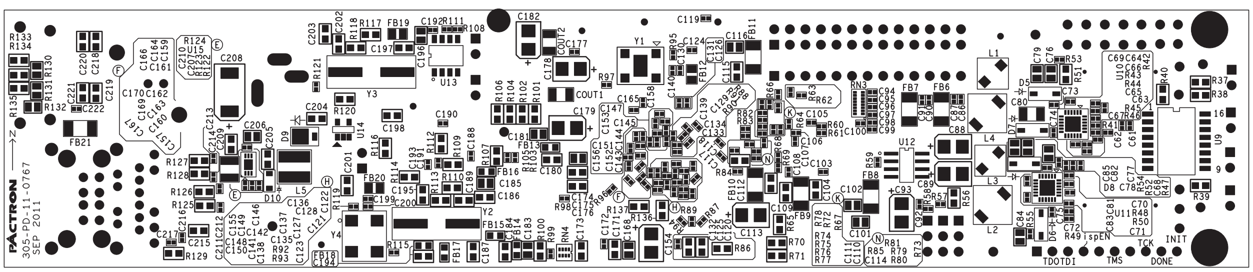


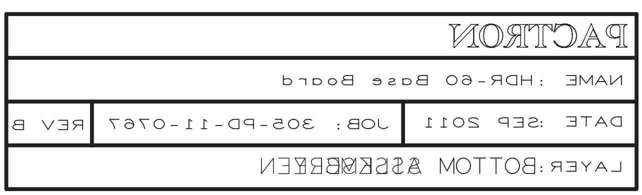
Figure 24. Mechanical Drawing



Appendix B. Silkscreen







Appendix C. Programming Using JTAG Flywire Connections

LatticeECP3 Configuration Using JTAG Flywire Connections

The HDR-60 Base Board includes a provision for the flywire connected programming header J3. The pins for the J3 header are not installed, as typical use of the board will be through the USB download. In the instance where a user of the board would like to use a flywire JTAG connection rather than the built-in USB download at J12, the user will need to first acquire and install the header pins for J3. The pinout for J3 is provided in Table 16.

Important Note: The board must be un-powered when connecting, disconnecting, or reconnecting an ispDOWNLOAD cable or USB cable. Always connect an ispDOWNLOAD cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeECP3 FPGA and render the board inoperable.

Table 16. JTAG Flywire Programming Header J3

J3 Pin	JTAG Signal
1	3_3V
2	TDO
3	TDI
4	NC
5	NC
6	TMS
7	GND
8	TCK
9	NC
10	NC

Requirements

- PC with Lattice ispVM System programming software version 17.9 (or later), installed with appropriate drivers (USB driver for USB cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD cable). *Note: An option to install these drivers is included as part of the ispVM System setup.*
- Any ispDOWNLOAD or Lattice USB cable (pDS4102-DL2x, HW7265-DL3x, HW-USB-2x, etc.).

For a complete discussion of the LatticeECP3's configuration and programming options, refer to the LatticeECP3 sysCONFIG Usage Guide.

The remainder of this JTAG flywire download procedure is identical to the download procedures described previously in the sections of this document: "LatticeECP3 SRAM Configuration Using a Standard USB Cable at J12" and "LatticeECP3 SRAM Configuration Using SPI Flash and USB Cable at J12". However, instead of the programming signals arriving at J12, they arrive at J3, and in step 5 of those procedures, where it says to select USB2, instead select the Lattice ispDOWNLOAD flywire connected cable type you are attaching to the J3 header pins.

Appendix D. Known Issues

The following resistors should not be populated by default: R87, R89, R92 and R93. The location of these resistors is on the bottom side of the HDR-60 Base Board Revision B (reverse side of the LatticeECP3-70). These resistors may have been installed on some boards and may cause issues for custom designs that use the signals connected to these resistors.