MT9M024 NanoVesta Head Board

User's Guide

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Revision: EB63_01.1

Introduction

The NanoVesta Head Board comprises a compact, low cost, high dynamic range (HDR) image sensor, lens and lens housing with adjustable focus, that can bolt directly onto the Lattice HDR-60 Base Board. Both the NanoVesta and HDR-60 boards have been designed to work together as part of the Lattice HDR-60 Video Camera Development Kit. The NanoVesta Head Board is designed to use the Aptina MT9M024 1/3-inch CMOS Digital Image Sensors which feature:

- Superior low-light performance
- HD video (720p60)
- Selectable linear or high dynamic range capture
- Selectable video or single frame modes
- On-chip auto exposure and statistics engine
- Parallel and serial output
- Auto black level calibration
- Context switching

Read more about the image sensor specifications in the Aptina MT9M024 data sheet.

Important: This document (including the schematics in Appendix A) describes the Lattice NanoVesta Head Board marked as Revision 2. This marking can be seen on the top layer silkscreen of the printed circuit board, below the outside perimeter of the lens holder.

Features

Key features of the NanoVesta Head Board include:

- Aptina MT9M024 1/3-inch CMOS Digital Image Sensor
- Lens: F/1.59, <7% distortion, with minimized flare, halo, and ghosting
- Lens holder with adjustable focus
- HiSPi and parallel signal connections to the HDR-60 Base Board
- Selectable 1.8V or 2.8V sensor VDDIO
- Selectable on-board 27.000 MHz MEMs oscillator, or HDR-60 Base Board oscillator
- 2.8V, VDDIO, 1.8V, 0.4V voltages are generated from the HDR-60 Base Board 5V
- Power status LEDs with one user-defined LED

General Description

The NanoVesta Head Board has been designed for use on the HDR-60 Base Board as part of the HDR-60 Video Camera Development Kit. The NanoVesta Head Board contains the camera sensor portion of the kit, while the HDR-60 Base Board contains the follow-on video camera image processing system. See the HDR-60 Base Board User's Guide for more information concerning that board.

Initial Setup and Handling

The following is recommended reading prior to removing the evaluation board from the static shielding bag and may or may not apply to your particular use of the board.

CAUTION: The devices on the boards can be damaged by improper handling.

The devices on the evaluation boards contain fairly robust ESD (Electro Static Discharge) protection structures within them, able to withstand typical static discharges (see the "Human Body Model" specification for an example of ESD characterization requirements). Even so, the devices are static-sensitive to conditions that exceed their designed-in protection. For example: higher static voltages, as well as lower voltages with lower series resistance or larger capacitance than the respective ESD specifications require can potentially damage or degrade the devices on the evaluation board.

As such, it is recommended that you wear an approved and functioning grounded wrist strap at all times while handling the evaluation boards when they are removed from the static shielding bag. If you will not be using the boards for a while, it is best to put them back in the static shielding bag. Please save the static shielding bag and packing box for future storage of the boards when they are not in use.

When reaching for the boards, it is recommended that you first touch the outside shield portion of the J11 BNC connector on the HDR-60 Base Board. If the NanoVesta Head Board is not installed on the HDR-60 Base Board, then when reaching for the NanoVesta board, it is recommended that you first touch the outside edge of the mounting holes on the NanoVesta board. This will neutralize any static voltage difference between your body and the board prior to any contact with signal I/O.

CAUTION: To minimize the possibility of ESD damage, the first and last electrical connection to the board, should be from test equipment chassis ground to the J11 BNC shield GND on the HDR-60 Base Board.

Before connecting signals or power to the board, attach a cable from chassis ground on grounded test equipment to the J11 BNC shield GND on the HDR-60 Base Board. Connecting the board ground to test equipment chassis ground will decrease the risk of ESD damage to the I/O on the board as the initial connections to the board are made. Likewise, when unplugging cables from the evaluation board, the last connection unplugged should be the chassis GND connection to the evaluation board GND. If you have a signal source that is floating with respect to chassis GND, attempt to neutralize any static charge on that signal source prior to attaching it to the evaluation board.

If you are holding or carrying the board while it is not in a static shielding bag, please keep one finger on the J11 BNC shield GND on the HDR-60 Base Board. If carrying the NanoVesta board alone, keep one finger one of the mounting holes. This will keep the board at the same voltage potential as your body until you can pick up the static shielding bag and put the board back in it.

Electrical, Mechanical, and Environmental Specifications

The nominal board dimensions are 42mm x 42mm (1.654" x 1.654"). Additional mechanical board dimension information is included on the mechanical drawing shown in Appendix A, Figure 6. On the physical board itself, connectors include pin 1 indictors as either an arrow, or triangle point near pin 1 on the outer layer silk screen. The environmental specifications are as follows:

- Operating temperature: 0°C to 55°C
- Storage temperature: -40°C to 75°C
- Humidity: <95% without condensation

Functional Description

Figure 1. NanoVesta Head Board Revision 2

Voltage Regulators

The NanoVesta Head Board power is supplied by the 5V DC power applied at connectors J4 and J5, pins 1, 2, 39 and 40. The on-board linear voltage regulators then provide the necessary supply voltages to power the sensor: 2.8V, VDDIO, 1.8V, and 0.4V. LEDs D1, D2, and D3 will light up if their respective powers are active. The regulator output voltages are set as shown in Table 1.

Table 1. NanoVesta Head Board Regulator Voltages

Supply	Voltage Regulator	Resistor Ratio	LED	Comment
5.0V	On HDR-60 Base Board	—	D3	5V arrives at J4 and J5
2.8V	U4	R43/R45	D2	
VDDIO	U3	R16/(R19+R20)	—	2.8V: Jumper on J3 (default) 1.8V: No jumper on J3
1.8V	U5	R44/R46	D1	
0.4V	U2	R17/R18	—	

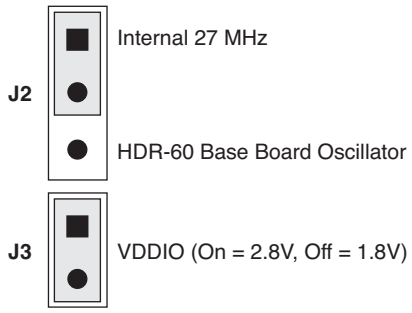
Each of the LT3025 regulators U2, U3, U4, and U5, are the linear low dropout voltage type that incorporate an external resistor divider voltage feedback to divide down the regulator output voltage and compare it against an internal reference voltage. The regulator then adjusts the output voltage higher or lower such that the resistor divided voltage matches the internal reference. By doing this, each regulator output voltage remains at a constant voltage value independent of the load it drives. Each regulator output voltage follows this equation:

V_{OUT} = (1 + resistor ratio) x (regulator internal reference voltage)

See the LT3025 device data sheet for additional details about this device.

The VDDIO regulator output voltage can be set to 1.8V or 2.8V by removing or adding a shorting jumper on J3, as shown in Table 1. With a jumper on J3, the voltage divider is set by R16 and R20 and this divider sets up a nominal 2.8V output voltage. When the shorting jumper on J3 is removed, the R19 resistor is placed in series with R20, which then changes the resistor divider ratio, and this changes the VDDIO regulator output voltage to become 1.8V. The default configuration is with the NanoVesta Head Board VDDIO set to 2.8V as shown in Figure 2.

Figure 2. NanoVesta Head Board Default Jumpers Diagram



MEMS Oscillator (Y1)

As shown in Figure 2, J2 is set such that the NanoVesta sensor will receive a clock input signal from the internal 27.000 MHz MEMS oscillator (Y1). The alternate position of J2 down will select the HDR-60 Base Board oscillator for the NanoVesta sensor clock input.

HiSPi Connector (J5)

The Aptina MT9M024 (U1) can produce HiSPi sub-LVDS video signals available at connector J5 after the proper set-up commands have been sent to it using the serial MT9M02_SCLK and MT9M02_SDATA signals, as discussed in the Aptina MT9M024 data sheet. The HiSPi clock and data signals have the "SLVS" text in the signal name, they are differential output signal pairs with "P" and "N" polarities, and they are biased at the +0.2V common mode level. The receiving LatticeECP3™ device should be set to LVDS, 100 ohm differential termination. The other signals on J5 are single-ended LVCMOS type and switch between the VDDIO level and GND. The J5 signal connections at the Aptina MT9M024 devices, HiSPi connector J5, and LatticeECP3 on the Lattice HDR-60 Base Board are shown in Table 2.

Table 2. Sensor (U1) Interface to HiSPi Connector J5

NanoVesta Head Board				HDR-60 Base Board	
J5 Pin	MT9M024 I/O Pin	Signal	Polarity	LatticeECP3 I/O Pin	sysIO™ Bank
13	A3	MT9M02_SLVS0P[1]	P	K21	2
11	A2	MT9M02_SLVS0N[1]	N	L21	2
29	A5	MT9M02_SLVS1P[1]	P	L22	2
27	A4	MT9M02_SLVS1N[1]	N	M22	2
21	B5	MT9M02_SLVS2P[1]	P	P21	2
19	B4	MT9M02_SLVS2N[1]	N	N22	2
26	C4	MT9M02_SLVS3P[1]	P	M18	2
24	C3	MT9M02_SLVS3N[1]	N	N17	2
18	B3	MT9M02_SLVSCP[1]	P	M21	2
16	B2	MT9M02_SLVSCN[1]	N	M20	2
4	—	VDDIO_rH	—	A13	1
10	H8	MT9M02_RESET_BAR[1]	—	C13	1
12	—	MT9M02_LED[1]	—	L19	2
30	D3	MT9M02_SDATA[1]	—	J22	2
32	D2	MT9M02_SCLK[1]	—	C14	1

1. Signals labeled MT9M02* can be used for the MT9M024 image sensor.

Parallel Connector (J4)

The Aptina MT9M024 (U1) can produce parallel LVCMOS video signals available at connector J4 after the proper set-up commands have been sent to it using the serial MT9M02_SCLK and MT9M02_SDATA signals, as discussed in the Aptina MT9M024 data sheet. The J4 signal connections at the Aptina MT9M024 device, parallel connector J4, and LatticeECP3 on the HDR-60 Base Board are shown in Table 3.

Table 3. Sensor (U1) Interface to Parallel Connector J4

NanoVesta Head Board			HDR-60 Base Board	
J4 Pin	**MT9M024 I/O Pin**	**Signal**	**LatticeECP3 I/O Pin**	**sysIO Bank**
16	H1	MT9M02_DOUT0[1]	J20	2
20	H2	MT9M02_DOUT1[1]	G22	2
15	H3	MT9M02_DOUT2[1]	F22	2
19	H4	MT9M02_DOUT3[1]	J18	2
14	G1	MT9M02_DOUT4[1]	A16	1
18	G2	MT9M02_DOUT5[1]	J19	2
13	G3	MT9M02_DOUT6[1]	C16	1
17	G4	MT9M02_DOUT7[1]	E22	2
22	F1	MT9M02_DOUT8[1]	G21	2
24	F2	MT9M02_DOUT9[1]	G14	1
21	F3	MT9M02_DOUT10[1]	J17	2
23	F4	MT9M02_DOUT11[1]	C17	1
10	E3	MT9M02_PIXCLK[1]	C12	1
9	C1	MT9M02_EXTCLK_FPGA[1]	A19	1
11	E1	MT9M02_LINE_VALID[1]	A18	1
12	E2	MT9M02_FRAME_VALID[1]	B16	1
25	G7	MT9M02_TRIGGER[1]	B18	1
27	H8	MT9M02_RESET_BAR[1]	A17	1
29	G8	MT9M02_OUTPUT_EN_BAR[1]	F16	1
31	A8	MT9M02_STANDBY[1]	F15	1
26	D1	MT9M02_SADDR[1]	G15	1
28	D2	MT9M02_SCLK[1]	D15	1
30	D3	MT9M02_SDATA[1]	C15	1
32	—	MT9M02_OSZ_ENABLE[1]	E15	1
4	—	VDDIO_rP	A12	1

1. Signals labeled MT9M02* can be used for MT9M024 image sensors.

Test and I²C Expansion Connector (J1)

The Test and I²C Expansion Connector provides access to serial I²C signals that can be used to control the Aptina MT9M024 (U1) by an external controller. There is also a MT9M02_FLASH output that is active when the sensor is acquiring the video image, which can be useful to trigger a Flash lamp. The Test and I²C Expansion Connector signals are shown in Table 4.

Table 4. Sensor (U1) Interface to Test and I²C Expansion Connector (J1)

NanoVesta Head Board			HDR-60 Base Board	
J1 Pin	MT9M024 I/O Pin	Signal	LatticeECP3 I/O Pin	sysIO Bank
1	—	+5V	—	—
2	—	+5V	—	—
3	—	VDDIO	A12, A13	1
4	D1	MT9M02_SADDR[1]	G15	1
5	—	GND	—	—
6	D2	MT9M02_SCLK[1]	D15	1
7	D3	MT9M02_SDATA[1]	C15	1
8	E4	MT9M02_FLASH[1]	—	—

1. Signals labeled MT9M02* can be used for MT9M024 image sensors.

Changes Made to Board in Revision 2

Revision 2 of the NanoVesta board was built to dissipate more heat from image sensor IC. The ground and power planes were modified to 1-ounce copper and the mounting holes were connected to the ground plane. Many components were moved to different locations on the PCB, but maintain the same functionality as the Revision A board.

References

- HDR-60 Video Camera Development Kit web page
- DS1021, LatticeECP3 Family Data Sheet
- HB1009, LatticeECP3 Family Handbook
- EB59, HDR-60 Base Board User's Guide
- QS010, LatticeECP3 Video Camera Development Kit QuickSTART Guide

Ordering Information

The 9MT024 Sensor NanoVesta Head Board is designed solely for use with the HDR-60 Video Camera Development Kit. One 9MT024 Sensor NanoVesta Head Board is included with the HDR-60 Video Camera Development Kit, or it is available separately as a stand-alone item.

Description	Ordering Part Number	China RoHS Environment Friendly
9MT024 Sensor NanoVesta Head Board	LF-9MT024NV-EVN	
HDR-60 Video Camera Development Kit *(Contains: HDR-60 Base Board with LatticeECP3 FPGA pre-loaded with Image Signal Processing (ISP) Demo, NanoVesta Head Board with Aptina A-1000 720p HDR Sensor and Sunex lens, two USB cables, HDMI cable with HDMI-to-DVI adapter, 12V AC adapter power supply, QuickSTART Guide)*	LFE3-70EAHDR60-DKN	

Technical Support Assistance

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+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
February 2011	01.0	Initial release.
May 2012	01.1	Updated document with new corporate logo.
		Document title changed from "NanoVesta Head Board User's Guide" to "MT9024 NanoVesta Head Board User's Guide".
		Updated document to support NanoVesta Head Board Revision 2.

Appendix A. Schematic

Figure 3. HiSPi Interface

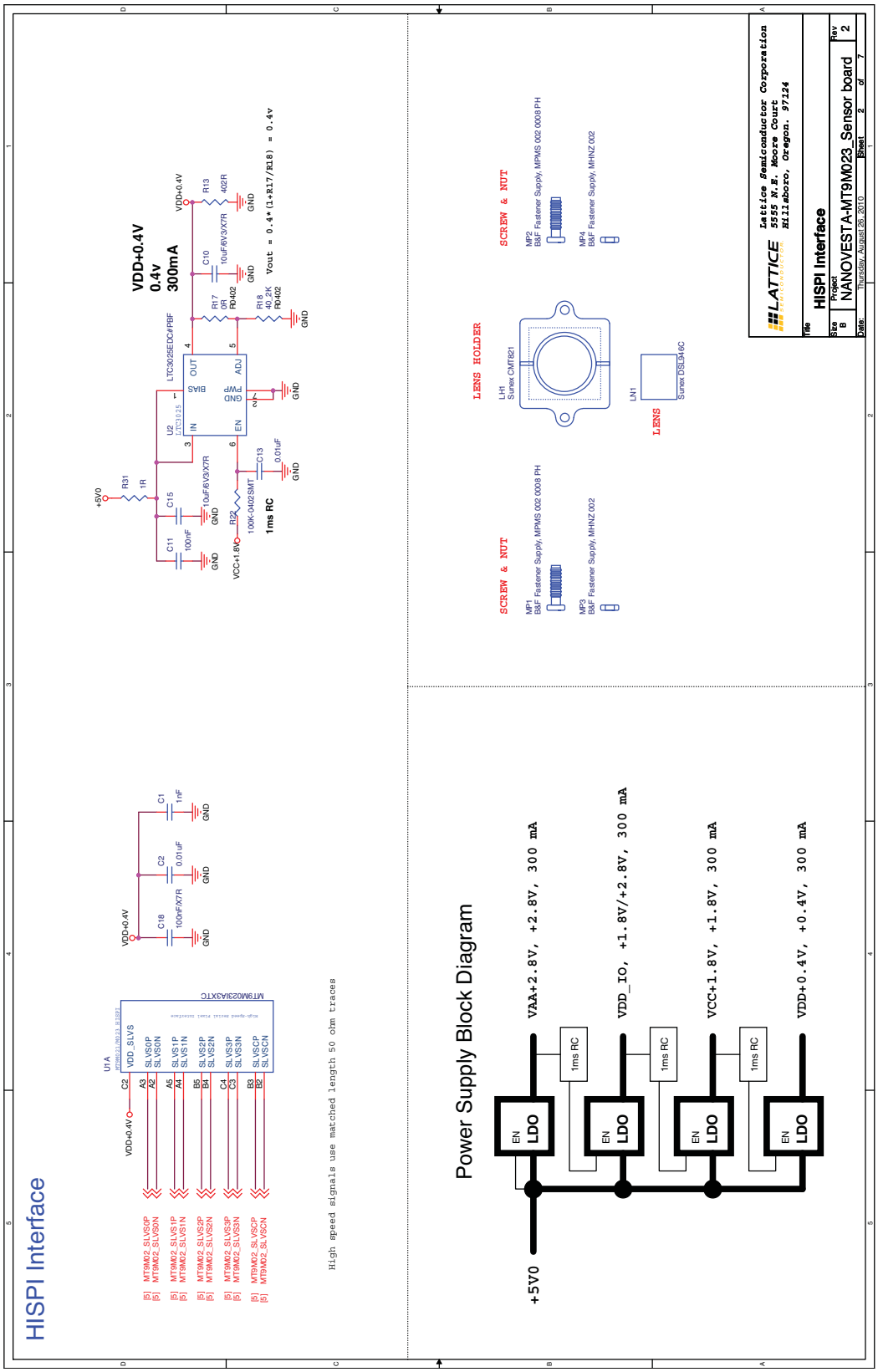

Figure 4. Power and Regulators

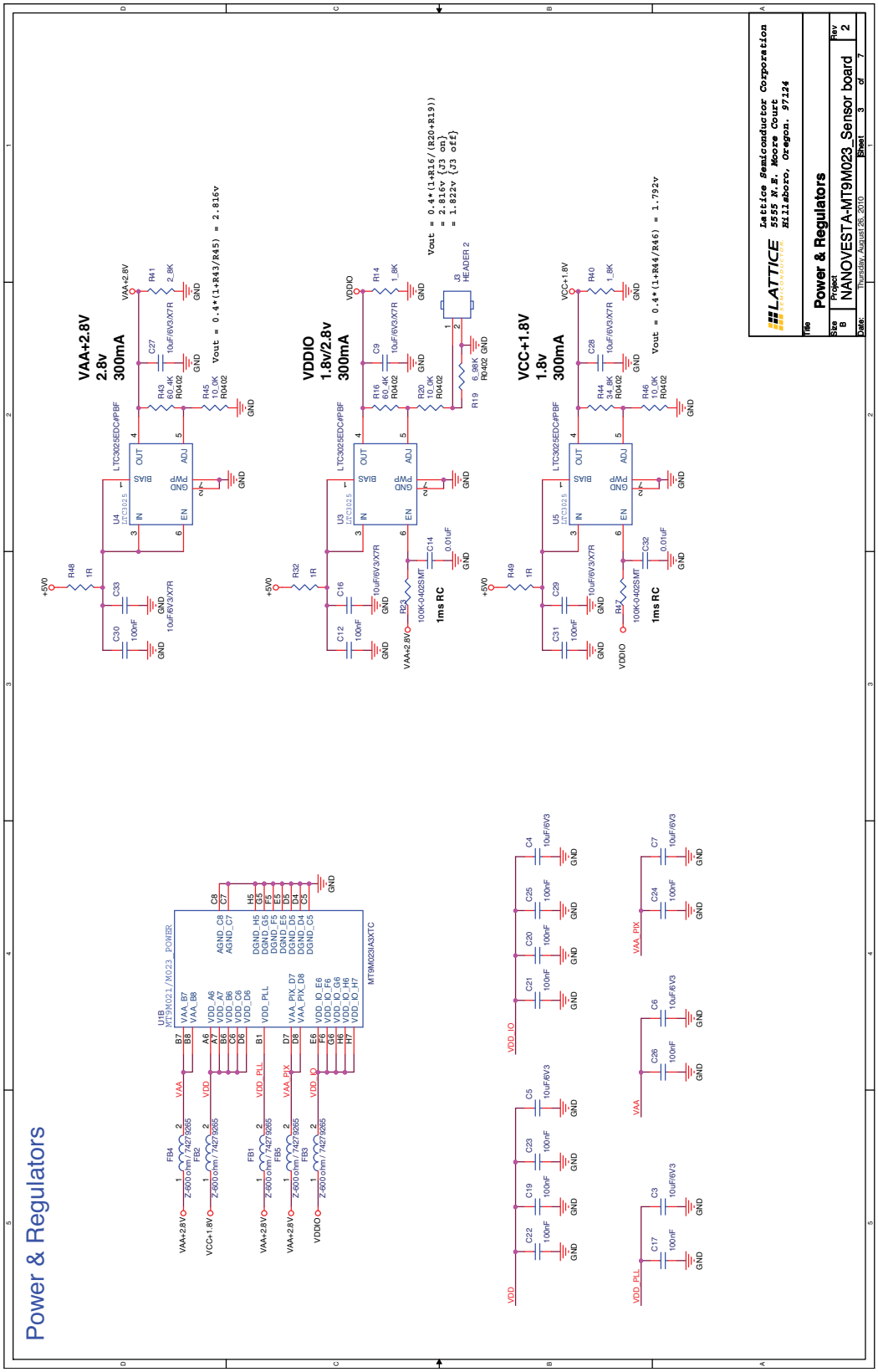

Figure 5. Image Sensor

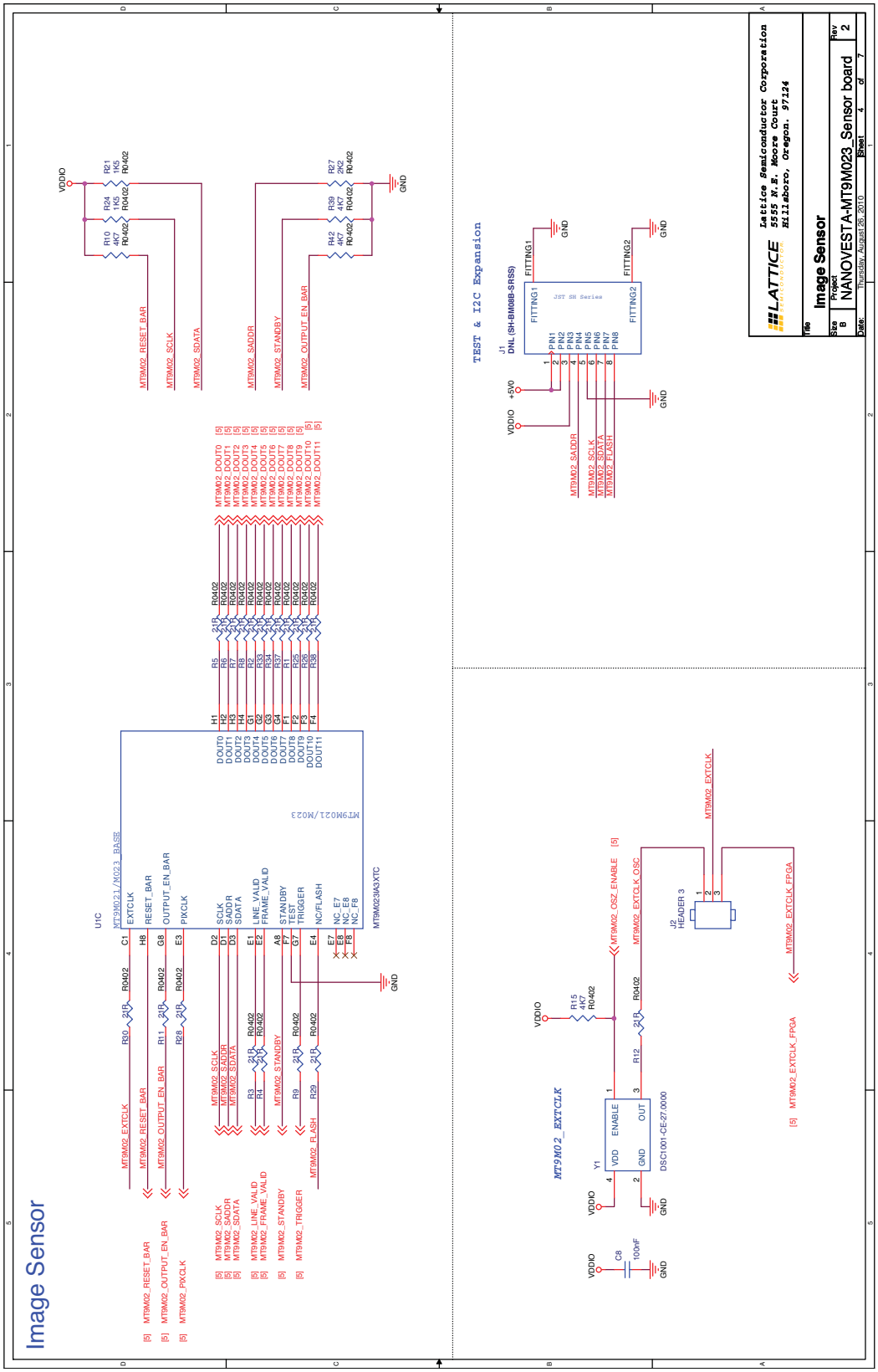

Figure 6. Interface Connectors