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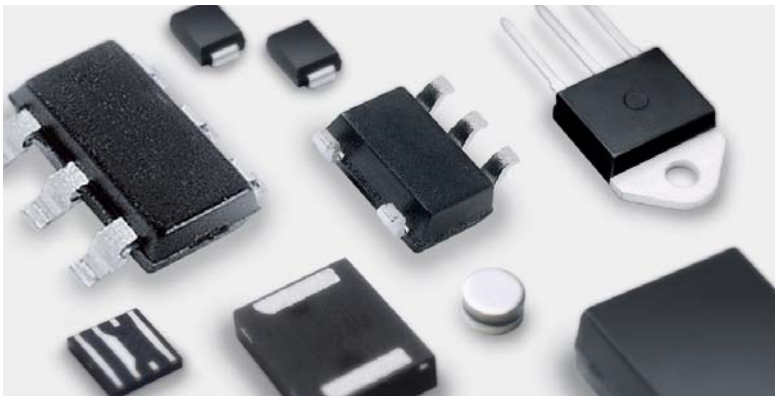
PRODUCT
CATALOG



SIDACTOR®

Protection Thyristor Semiconductor Products

TABLE OF CONTENTS

Series Name		Package Type	Type	Standoff (working) Voltage (V_{DRM})	Switching Voltage (V_S)	Peak Pulse Rating:			RoHS Compliant	UL Compliant
						2x10µs	10x1000µs	8X20µs		
Broadband Optimized Protection:										
SDP Biased Series		5x6 QFN	C	6-320	25-400	500A	100A	400A	•	•
		SOT23-6	G	19	29			20A	•	•
SDP Series		SOT23-5	G	8-24	15-35			50A	•	•
SDP TwinChip™ Series		3x3 QFN	F	16	43	100	30A	80A	•	•
P0080T023G5		SOT23-5	G	8	15	45A	18A	50A	•	•
TwinChip™ Series		DO-214AA	A	58-550	77-700	150A	45A	150A	•	•
			B			250A	80A	250A		
			C			500A	100A	400A		
		DO-15	B	220-320	300-400		80A			
SEP Biased Series		5x6 QFN	C	6-75	25-98	500A	100A	400A	•	•
Q2L Series		3x3 QFN	A	6-320	25-400	150A	45A	150A	•	•
			B			250A	80A	250A		
		3.3x3.3 QFN	C	6-400	25-530	500A	100A	400A		
MC Multiport Series		MS-013	C	6-320	25-400	500A	100A	400A	•	•
MC Series		DO-214AA	A	6-25	25-40	150A	45A	150A	•	•
			C	6-320	25-400	500A	100A	400A		
		TO-92	C	6-320	25-400	500A	100A	400A		
Balanced MC Series		Modified TO-220	C	Pin 1-2, 3-2, 1-3: 130-420	Pin 1-2, 3-2, 1-3: 180-600	500A	100A	400A	•	•
Subscriber Line Interface Circuit (SLIC) Protection:										
Fixed Voltage Series		DO-214AA	A	58 - 120	77 - 160	150A	45A	150A	•	•
			C			500A	100A	400A		
			D			1000A	200A	800A		

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SIDACtor® Protection Thyristors

Series Name		Package Type	Type	Standoff (working) Voltage (V_{DRM})	Switching Voltage (V_S)	Peak Pulse Rating: 2x10µs	10x1000µs	8X20µs	RoHS Compliant	UL Compliant
Subscriber Line Interface Circuit (SLIC) Protection:										
Fixed Voltage Twin SLIC Series		Modified DO-214AA	A	58 - 160	77 - 200	G150A	45A	150A	•	•
Fixed Voltage Q2L Series		QFN 3.3x3.3	C	58 - 160	77 - 200	500A	100A	400A	•	•
Fixed Voltage Enhanced Single Series		MS-012	F	58 - 160	77 - 200	120A	30A	100A	•	•
Fixed Voltage Multiport Series		MS-013	A	58 - 160	77 - 200	150A	45A	150A	•	•
			C			500A	100A	400A		
Battrax® Series Positive/Negative		Mod DO-214AA	A	These devices track their reference voltages. Please refer to data sheets in SIDACtor products catalog or www.littelfuse.com for detailed information.		150A	45A	150A	•	•
			C			500A	100A	400A		
Battrax® Series Single Port Negative		MS-013	C			500A	100A	400A	•	•
Battrax® Series Single Port Positive/Negative		MS-013	C			500A	100A	400A	•	•
Battrax® Series Dual Port Negative		MS-013	C			500A	100A	400A	•	•
Line Circuit Access Switch (LCAS) Protection:										
Asymmetrical Multiport Series		MS-013	A	These products have asymmetric trigger voltages. See data sheet.		150A	45A	150A	•	•
			C			500A	100A	400A		
Baseband Protection (Voice-DS1):										
SIDACtor® Series		DO-214AA	A	6-320	25-400	150A	45A	150A	•	•
			B			250A	80A	250A		
			C	6-400	25-530	500A	100A	400A		
		DO-214AC (SMA)	A	6-320	25-400	150A	50A	150A	•	•
		TO-92	A	6-320	25-400	150A	45A	150A	•	•
			B			250A	80A	250A		
			C			500A	100A	400A		
		DO-15	A	90-320	130-400		45A		•	•
			B				80A			
		Modified TO-220	A	Pins 1-2,3-2: 25-275 Pins 1-3: 50-550	Pins 1-2,3-2: 40-350 Pins 1-3: 80-700	150A	45A	150A	•	•
			B			250A	80A	250A		
			C			500A	100A	400A		
SIDACtor® Multiport Series		MS-013	A	Pins 1-2,3-2,4-5,6-5: 6-320 Pins 1-3,4-6: 12-640	Pins 1-2,3-2,4-5,6-5: 25-400 Pins 1-3,4-6: 50-800	150A	45A	150A	•	•
			C			500A	100A	400A		
SIDACtor® Balanced Series		MS-013	A	130-420	180-600	150A	45A	150A	•	•
			B			250A	80A	250A		
			C			500A	100A	400A		
		Modified TO-220	A	Pins 1-2, 3-2: 130-420 Pins 1-3: 130-420	Pins 1-2, 3-2: 180-600 Pins 1-3: 180-600	150A	45A	150A	•	•
			B			250A	80A	250A		
			C			500A	100A	400A		
SIDACtor® Balanced Multiport Series		MS-013	A	130-420	180-600	150A	45A	150A	•	•
			B			250A	80A	250A		
			C			500A	100A	400A		
			Asym. A6	Pins 1-2,2-3,4-5,5-6: 170-420 Pins 4-6,1-3: 50-420	Pins 1-2,2-3,4-5,5-6: 250-600 Pins 4-6,1-3: 80-600	150A	45A	150A		
			Asym. B6			250A	80A	250A		
			Asym. C6			500A	100A	400A		

SIDACtor® Protection Thyristors

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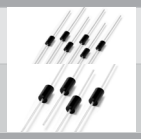
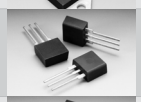
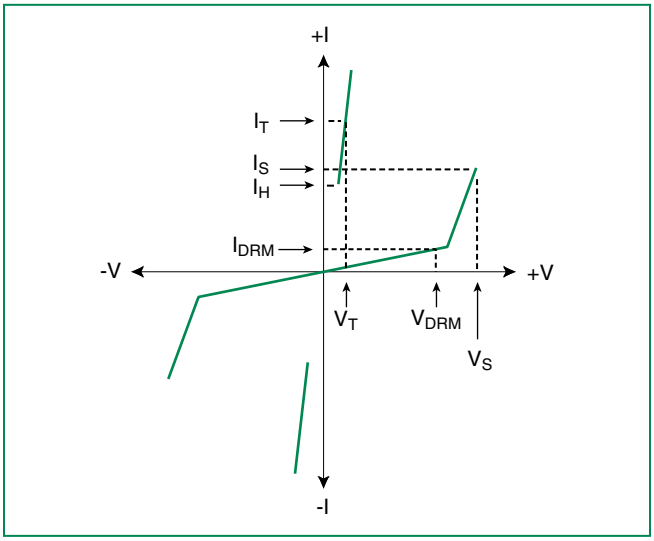
Series Name		Package Type	Type	Standoff (working) Voltage (V_{DRM})	Switching Voltage (V_S)	Peak Pulse Rating:			RoHS Compliant	UL Compliant
						2x10µs	10x1000µs	8X20µs		
Baseband Protection (Voice-DS1):										
T10A Series		DO-15	A	50-245	84-370		50A	100A	•	•
T10B Series		DO-201	B	70-240	125-370		100A	250A	•	•
High Exposure Surge Protection:										
High Surge Current Series		DO-214AA	D	6-320	25-400	1000A	200A	800A	•	•
5kA Series		TO-218	E	140-180	180-260			5000A	•	•
Primary Protection Series		Modified TO-220	C	Pins 1-2,3-2: 25-275 Pins 1-3: 50-550	Pins 1-2,3-2: 40-350 Pins 1-3: 80-700	500A	100A	400A	•	•
Primary Protection Balanced Series		Modified TO-220	C	Pins 1-2, 3-2: 130-420 Pins 1-3: 130-420	Pins 1-2, 3-2: 180-600 Pins 1-3: 180-600	500A	100A	400A	•	•

SIDACtor Product Description

SIDACtor components are solid state crowbar devices designed to protect telecom equipment during hazardous transient conditions. Capitalizing on the latest in thyristor advancements, Littelfuse makes *SIDACtor* devices with a patented ion implant technology. This technology ensures effective protection within nanoseconds, up to 5000 A surge current ratings, and simple solutions for regulatory requirements such as GR 1089, TIA-968-A (formerly known as FCC Part 68), ITU-T K.20, ITU-T K.21, and UL 60950-1.

Figure 1.1 V-I Characteristics



Operation

In the standby mode, *SIDACtor* devices exhibit a high off-state impedance, eliminating excessive leakage currents and appearing transparent to the circuits they protect. Upon application of a voltage exceeding the switching voltage (V_S), *SIDACtor* devices crowbar and simulate a short circuit condition until the current flowing through the device is either interrupted or drops below the *SIDACtor* device's holding current (I_H). Once this occurs, *SIDACtor* devices reset and return to their high off-state impedance.

Advantages

SIDACtor devices:

- Cannot be damaged by voltage
- Eliminate hysteresis and heat dissipation typically found with clamping devices
- Eliminate voltage overshoot caused by fast-rising transients
- Are non-degenerative
- Will not fatigue
- Have Low capacitance, making them ideal for high-speed transmission equipment

Applications*

When protecting telecommunication circuits, *SIDACtor* devices are connected between tip-to-ring for metallic protection and between tip-to-ground and ring-to-ground for longitudinal protection. They typically are placed behind some type of current-limiting device, such as the Littelfuse *TeleLink*® lightning tolerant fuse or the Littlefuse POLYFUSE® lightning tolerant resettable PTC devices. Common applications include:

- T1/E1/J1 and HDSL2/4
- *Subscriber Line Interface Card* (SLIC) in Fiber to the Curb (FTTC) and Fiber to the Premises (FTTP)
- Non-Fiber SLIC for Central Office (CO) locations and Remote Terminals (RT)
- xDSL applications such as ADSL, ADSL2+, VDSL, and VDSL2+
- Ethernet 10/100/1000BaseT, PoE (Power over Ethernet) systems
- Customer Premises Equipment (CPE) such as VoIP, modems, answering machines, multi-function printers, telephones, fax machines, and security systems
- ISDN "U" and "S/T" interfaces
- Baystation T1/E1/J1, T3 (DS3) trunk cards
- PBXs, IP PBXs, KSUs, and other switches
- Main Distribution Frames (MDFs), five-pin modules, Network Interface Devices (NIDs)

For more information regarding specific applications, design requirements, or surge suppression, please contact Littelfuse directly at +1 800-999-9445 or through your local area representative. To find the Littelfuse representative near you visit http://www.littelfuse.com/contact.

*** See also SIDACtor Family Application Selector Table (page7)**

Revised: 02/23/17

SIDACtor Product Description (continued)

Broadband Optimized™ Protection

The Broadband Optimized™ family of products is focused on addressing the performance and regulatory requirements of broadband equipment. The **Broadband Optimized** family, with its wide range of solutions provides applications with the options needed to address the unique protection needs of DSL equipment (up to VDSL) as well as Ethernet (up to 1000baseT). Optimization is accomplished using proprietary and patented approaches that minimize the negative effects of device capacitance on broadband signals. The **Broadband Optimized** family provides an overvoltage protection solution that helps applications comply with Telcordia GR-1089 Issue 4, and ITU-T recommendations K.20, K.21, K.44, and K.45.

SLIC Protection

The **SLIC** family of products is focused on addressing the unique protection needs of SLIC (Subscriber Line Interface Circuit) chip sets. The family offers **Fixed Voltage** and **Battrax®** battery tracking protection solutions capable of protecting SLIC devices from transients caused by lightning and AC power cross. The **SLIC** family provides an overvoltage protection solution that helps applications comply with Telcordia GR-1089 Issue 4, and ITU-T recommendations K.20, K.21, K.44, and K.45.

LCAS Protection

The **LCAS** family of products is focused on the specialized protection needs of Line Circuit Access Switches (LCAS). This family utilizes a specialized asymmetric design specially formulated for LCAS devices. The **LCAS** family provides an overvoltage protection solution that helps applications comply with Telcordia GR-1089 Issue 4, and ITU-T recommendations K.20, K.21, K.44 and K.45.

Baseband Protection

The **Baseband** family of products is focused on addressing the performance and regulatory requirements of baseband telecommunications equipment such as voice, modems, and DS1. They offer an overvoltage protection solution that helps applications comply with Telcordia GR-1089 Issue 4, ITU-T recommendations K.20, K.21, K.44, and K.45, and TIA-968-A.

High Surge Current Protection

The **High Surge Current** products are a unique family of very robust solid state protection devices intended for use in high exposure environments. This family includes products specifically designed for primary protection such as cell and TO-220 devices. The **High Surge Current** family also has devices capable of meeting 5kA 8/20µs for use in extreme conditions. For enhanced secondary protection requirements, a D-rated device capable of 1000A 2/10µs is available in a DO-214 package. The **High Surge Current** Protection family provides an overvoltage protection solution that help applications comply with Telcordia GR-1089 Issue 4, and ITU-T recommendations K.20, K.21, K.44, and K.45.

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SIDACtor Family Application Selector Table

Telecom Application	Broadband Optimized ™ Protection	SLIC Protection	Baseband Protection (Voice-DS1)	LCAS Protection	High Surge Current Protection
ADSL	●		●		
ADSL2/2+	●				
VDSL	●				
VDSL2	●				
HDSL2/4	●		●		
ISDN	●		●		
Ethernet 10/100/1000BaseT	●				
PoE	●				
VoIP FXO	●				
VoIP FXS		●			
Negative Ringing SLIC		●			
Positive & Negative Ringing SLIC		●			
LCAS Relay				●	
POTS-Telephone-corded & cordless			●		
MDC Modem			●		
PCI Modem			●		
Multifunction Printer-Fax			●		
T1/E1/J1 (DS1)	●		●		
Security System			●		
Primary Protection Modules					●
Secondary Protection Modules-Strip Protectors			●		●
Low Pair Count Installations					●
CATV Power Amplifiers					●
Base Stations					●

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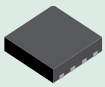
Product Packages

	Package (illustrations not to scale)	Family				
		Broadband Optimized™ Protection	SLIC Protection	LCAS Protection	Baseband Protection (Voice - DS1)	High Surge Current Protection
Surface Mount	 SOT23-5	•				
	 SOT23-6	•				
	 3x3x1 QFN	•				
	 3.3x3.3x1 QFN	•	•			
	 5x6x1.5 QFN	•				
	 DO-214AA	•	•	•	•	•
	 Modified DO-214AA		•			
	 MS-012		•			
	 MS-013	•	•	•	•	
Through-Hole	 TO-92	•			•	
	 Modified TO-220	•			•	•
	 TO-218					•
	 DO-201AD				•	
	 DO-15	•			•	

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Construction and Operation

SIDACtor devices are thyristor devices used to protect sensitive circuits from electrical disturbances caused by lightning-induced surges, inductive-coupled spikes, and AC power fault conditions. The unique structure and characteristics of the thyristor are used to create an overvoltage protection device with precise and repeatable turn-on characteristics with low voltage overshoot and high surge current capabilities.

Key Parameters

Key parameters for *SIDACtor* devices are $\mathbf{V_{DRM}}$, $\mathbf{I_{DRM}}$, $\mathbf{V_S}$, $\mathbf{I_H}$, and $\mathbf{V_T}$ (please refer to Figure 1.3 on page 11).

$\mathbf{V_{DRM}}$ is the repetitive peak off-state voltage rating of the device (also known as stand-off voltage) and is the continuous peak combination of AC and DC voltage that may be applied to the *SIDACtor* device in its off-state condition.

$\mathbf{I_{DRM}}$ is the maximum value of leakage current that results from the application of V_{DRM}.

Switching voltage (V_S) is the maximum voltage that subsequent components may be subjected to during a fast-rising (100 V/µs) overvoltage condition.

Holding current (I_H) is the minimum current required to maintain the device in the on state.

On-state voltage (V_T) is the maximum voltage across the device during full conduction.

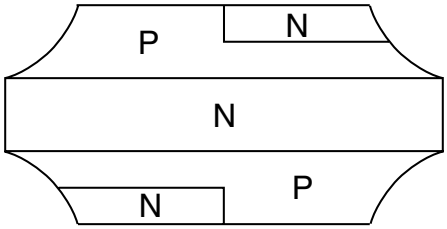
Operation

The device operates much like a switch. In the off state, the device exhibits leakage currents (I_{DRM}) less than 5 µA, making it invisible to the circuit it is protecting. As a transient voltage exceeds the device's V_{DRM}, the device begins to enter its protective mode with characteristics similar to an avalanche diode. When supplied with enough current (I_S), the device switches to an on state, shunting the surge from the circuit it is protecting. While in the on state, the device is able to sink large amounts of current because of the low voltage drop (V_T) across the device. Once the current flowing through the device is either interrupted or falls below a minimum holding current (I_H), the device resets, returning to its off state. If the I_{PP} rating is exceeded, the device typically becomes a permanent short circuit.

Physics

The device is a semiconductor device characterized as having four layers of alternating conductivity: PNPN (Figure 1.2 below). The four layers include an emitter layer, an upper base layer, a mid-region layer, and a lower base layer. The emitter is sometimes referred to as a cathode region, with the lower base layer being referred to as an anode region.

Figure 1.2 Geometric Structure of Bidirectional SIDACtor devices



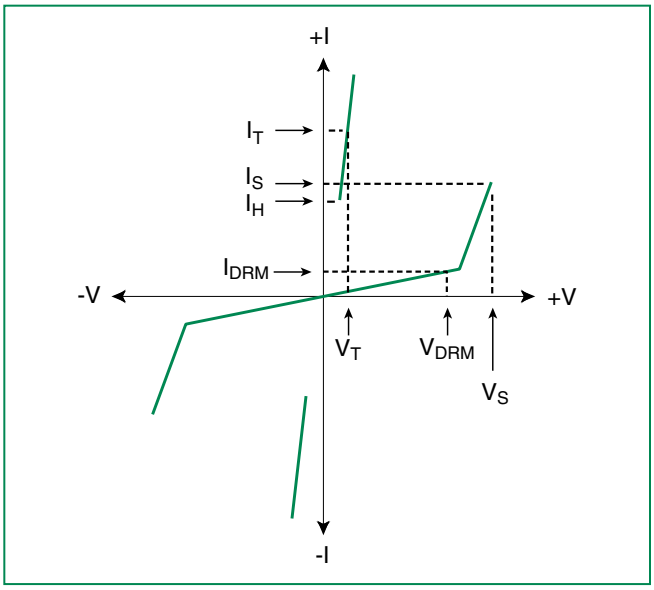
As the voltage across the device increases and exceeds the device's V_{DRM}, the electric field across the center junction reaches a value sufficient to cause avalanche multiplication. As avalanche multiplication occurs, the impedance of the device begins to decrease, and current flow begins to increase until the device's current gain exceeds unity. Once unity is exceeded, the device switches from a high impedance (measured at V_S) to a low impedance (measured at V_T) until the current flowing through the device is reduced below its holding current (I_H).

Electrical Parameters

SIDACtor electrical parameters are based on the following definition of conditions:

- **On state** (also referred to as the **crowbar condition**) is the low impedance condition reached during full conduction and simulates a short circuit.
- **Off state** (also referred to as the **blocking condition**) is the high impedance condition prior to beginning conduction and simulates an open circuit.

Figure 1.3 V-I Characteristics



Please refer to Figure 1.3 above related to many of the following terms:

C_O	**Off-state Capacitance**—capacitance measured in off state @ 2 V bias and 1 MHz
di/dt	**Rate of Rise of Current**—maximum rated value of the acceptable rate of rise in current over time
dv/dt	**Rate of Rise of Voltage**—rate of applied voltage over time
I_S	**Switching Current**—maximum current required to switch to on state
I_{DRM}	**Leakage Current**—maximum peak off-state current measured at V_{DRM}
I_H	**Holding Current**—minimum current required to maintain on state
I_{PP}	**Peak Pulse Current**—maximum rated peak impulse current
I_T	**On-state Current**—maximum rated continuous on-state current
I_{TSM}	**Peak One-cycle Surge Current**—maximum rated one-cycle AC current
V_S	**Switching Voltage**—maximum voltage prior to switching to on state during 100 V/µs surge
V_{DRM}	**Peak Off-state Voltage**—maximum voltage that can be applied while maintaining off state
V_F	**On-state Forward Voltage**—maximum forward voltage measured at rated on-state current
V_T	**On-state Voltage**—maximum voltage measured at rated on-state current

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Selection Criteria

When selecting a *SIDACtor*® device, use the following criteria:

Off-state Voltage (V_{DRM})

The V_{DRM} of the *SIDACtor*® device must be greater than the maximum operating voltage of the circuit that the *SIDACtor*® device is protecting.

Example 1: For a POTS (Plain Old Telephone Service) application, convert the maximum operating Ring voltage (150 V_{RMS}) to a peak voltage, and add the maximum DC bias of the central office battery:

$$150\ V_{RMS}\ \sqrt{2} + 56.6\ V_{PK} = 268.8\ V_{PK}$$

$$\therefore V_{DRM} > 268.8\ V$$

Example 2: For an ISDN application, add the maximum voltage of the DC power supply to the maximum voltage of the transmission signal (for U.S. applications, the U-interface will not have a DC voltage, but European and Japanese ISDN applications may):

$$150\ V_{PK} + 3\ V_{PK} = 153\ V_{PK}$$

$$\phi V_{DRM} > 153\ V$$

Switching Voltage (V_S)

The V_S of the *SIDACtor*® device should be equal to or less than the instantaneous peak voltage rating of the component it is protecting.

Example 1: $V_S \le V_{Relay\ Breakdown}$

Example 2: $V_S \le SLIC\ V_{PK}$

Peak Pulse Current (I_{PP})

For circuits that do not require additional series resistance, the surge current rating (I_{PP}) of the *SIDACtor*® device should be greater than or equal to the surge currents associated with the lightning immunity tests of the applicable regulatory requirement (I_{PK}):

$$I_{PP} \ge I_{PK}$$

For circuits that use additional series resistance, the surge current rating (I_{PP}) of the *SIDACtor*® device should be greater than or equal to the available surge currents associated with the lightning immunity tests of the applicable regulatory requirement ($I_{PK(available)}$):

$$I_{PP} \ge I_{PK(available)}$$

The maximum available surge current is calculated by dividing the peak surge voltage (V_{PK}) by the total circuit resistance (R_{TOTAL}):

$$I_{PK(available)} = V_{PK}/R_{TOTAL}$$

For longitudinal surges (Tip-Ground, Ring-Ground), R_{TOTAL} is calculated for both Tip and Ring:

$$R_{SOURCE} = V_{PK}/I_{PK}$$

$$R_{TOTAL} = R_{TIP} + R_{SOURCE}$$

$$R_{TOTAL} = R_{RING} + R_{SOURCE}$$

For metallic surges (Tip-Ring):

$$R_{SOURCE} = V_{PK}/I_{PK}$$

$$R_{TOTAL} = R_{TIP} + R_{RING} + R_{SOURCE}$$

Example 1: A modem manufacturer must pass the Type A surge requirement of TIA-968-A without any series resistance.

$$I_{PK} = 100\ A,\ 10x560\ \mu s$$

$$I_{PP} \ge 100\ A,\ 10x560\ \mu s$$

Therefore, either a "B" rated or "C" rated *SIDACtor*® device would be selected.

Example 2: A line card manufacturer must pass the surge requirements of GR 1089 with 30 Ω on Tip and 30 Ω on Ring.

$$I_{PK} = 100\ A,\ 10x1000\ \mu s$$

$$V_{PK} = 1000\ V$$

$$R_{SOURCE} = V_{PK}/I_{PK} = 10\ \Omega$$

$$R_{TOTAL} = R_{SOURCE} + R_{TIP} = 40\ \Omega$$

$$I_{PK\ (available)} = V_{PK}/R_{TOTAL} = 1000\ V/40\ \Omega$$

$$\therefore I_{PP} \ge 25\ A$$

Holding Current (I_H)

Because TIA-968-A 4.4.1.7.3 specifies that registered terminal equipment not exceed 140 mA dc per conductor under short-circuit conditions, the holding current of the *SIDACtor*® device is set at 150 mA.

For specific design criteria, the holding current (I_H) of the *SIDACtor*® device must be greater than the DC current that can be supplied during an operational and short circuit condition.

Off-State Capacitance (C_O)

Assuming that the critical point of insertion loss is 70 percent of the original signal value, the *SIDACtor*® device can be used in most applications with transmission speeds up to 30 MHz. For transmission speeds greater than 30 MHz, the new MC series is highly recommended.

Revised: 02/23/17

Overvoltage Protection Comparison

The four most commonly used technologies for overvoltage protection are as follows:

- *SIDACtor*® devices
- Gas Discharge Tubes (GDTs)
- Metal Oxide Varistors (MOVs)
- TVS diodes

All four technologies are connected in parallel with the circuit being protected, and all exhibit a high off-state impedance when biased with a voltage less than their respective blocking voltages.

SIDACtor® devices

A *SIDACtor*® device is a PNPN device that can be thought of as a thyristor device without a gate. Upon exceeding its peak off-state voltage (V_{DRM}), a *SIDACtor*® device will clamp a transient voltage to within the device's switching voltage (V_S) rating. Then, once the current flowing through the *SIDACtor*® device exceeds its switching current, the device will crowbar and simulate a short-circuit condition. When the current flowing through the *SIDACtor*® device is less than the device's holding current (I_H), the *SIDACtor*® device will reset and return to its high off-state impedance.

Advantages

Advantages of the *SIDACtor*® device include its fast response time (Figure 1.1), stable electrical characteristics, long term reliability, and Low capacitance. Also, because the *SIDACtor*® device is a crowbar device, it cannot be damaged by voltage.

Restrictions

Because the *SIDACtor*® device is a crowbar device, it cannot be used directly across the AC line; it must be placed behind a load. Failing to do so will result in exceeding the *SIDACtor*® device's maximum on-state current rating, which may cause the device to enter a permanent short-circuit condition.

Applications

Although found in other applications, *SIDACtor*® devices are primarily used as the principle overvoltage protector in telecommunications and data communications circuits. For applications outside this realm, follow the design criteria in "*SIDACtor*® Device Selection Criteria".

Gas Discharge Tubes

Gas discharge tubes (GDTs) are either glass or ceramic packages filled with an inert gas and capped on each end with an electrode. When a transient voltage exceeds the DC breakdown rating of the device, the voltage differential causes the electrodes of the gas tube to fire, resulting in an arc, which in turn ionizes the gas within the tube and provides a low impedance path for the transient to follow. Once the transient drops below the DC holdover voltage and current, the gas tube returns to its off state.

Advantages

Gas discharge tubes have high surge current and Low capacitance ratings. Current ratings can be as high as 20 kA, and capacitance ratings can be as low as 1 pF with a zero-volt bias.

Applications

Gas discharge tubes are typically used for primary protection due to their high surge rating. However, their low interference for high frequency components make them a candidate for high speed data links.

Metal Oxide Varistors

Metal Oxide Varistors (MOVs) are two-leaded, through-hole components typically shaped in the form of discs. Manufactured from sintered oxides and schematically equivalent to two back-to-back PN junctions, MOVs shunt transients by decreasing their resistance as voltage is applied.

Advantages

Since MOVs surge capabilities are determined by their physical dimensions, high surge current ratings are available. Also, because MOVs are clamping devices, they can be used as transient protectors in secondary AC power line applications.

Applications

Although MOVs are restricted from use in many telecom applications (other than disposable equipment), they are useful in AC applications where a clamping device is required and tight voltage tolerances are not.

Revised: 02/23/17

Overvoltage Protection Comparison (continued)

TVS Diodes

Transient Voltage Suppressor (TVS) diodes are clamping voltage suppressors that are constructed with back-to-back PN junctions. During conduction, TVS diodes create a low impedance path by varying their resistance as voltage is applied across their terminals. Once the voltage is removed, the diode will turn off and return to its high off-state impedance.

Advantages

Because TVS diodes are solid state devices, they do not fatigue nor do their electrical parameters change as long as they are operated within their specified limits. TVS diodes effectively clamp fast-rising transients and are well suited for low-voltage applications that do not require large amounts of energy to be shunted.

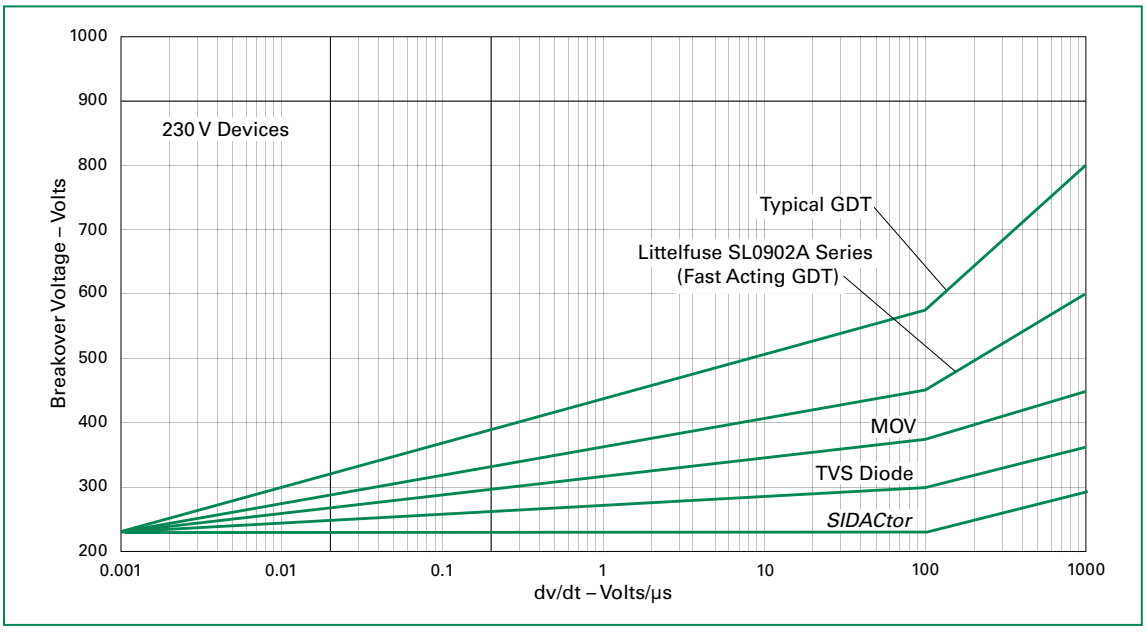
Applications

Due to their low power ratings, TVS diodes are not used as primary interface protectors across Tip and Ring, but they can be used as secondary protectors that are embedded within a circuit.

Overshoot Levels versus dv/dt

Firgure 1.4 below shows a peak voltage comparison between *SIDACtor*® devices, Gas Discharge Tubes (GDT), Metal-Oxide Varistors (MOVs), and TVS diodes, all with a nominal stand-off voltage rating of 230 V. The X axis represents the dv/dt (rise in voltage with respect to time) applied to each protector, and the Y axis represents the maximum voltage drop across each protector.

Figure 1.4 Overshoot Levels versus dv/dt



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Custom Part Number Capabilities

Littelfuse will provide customer specific part numbers based on the screening of key electrical parameters as well as custom lead forms.

Electrical parameters such as V_{DRM}, V_S, and I_H can be screened to different levels depending on the part number, package and the requested screening level. Please contact your local Littelfuse sales representative to request a specially screened product. Upon request, Littelfuse product management and engineering will evaluate the request for feasibility and cost impacts. A special part number will be assigned to the screened part upon acceptance by Littelfuse and the customer.

For custom lead forms, the process is similar to electrical screening. Each requested lead form will be evaluated for manufacturability and costs to implement. Upon mutual approval by Littelfuse and the customer, a special part number will be assigned to the standard part number utilizing the special lead form.

Agency Approvals

Littelfuse products are recognized under the Components program of Underwriters Laboratories. The following table shows agency file numbers for Littelfuse products.

Product	UL File Number
SIDACtor® Devices / **Battrax®** [1]	E133083
T10A / T10B	E128662

Note : 1. Recognized component under 'Conditions of Acceptability'

Trademarks and Patents

Littelfuse, Inc., manufacturer of Teccor® brand circuit protection devices, is the proprietor of the SIDACtor®, Battrax®, TeleLink®, TwinCHIP™, TwinSLIC™ and Broadband Optimized™ trademarks. All other brand names may be trademarks of their respective companies. Teccor® brand products are covered by these and other U.S. Patents:

4,685,120
4,827,497
4,905,119
5,479,031
5,516,705
7,429,785

Revised: 02/23/17

Quality and Reliability Assurance

Littelfuse Quality Policy

Littelfuse is committed to being sensitive to customer expectations and providing quality products and services at a competitive price. In support of this commitment, Littelfuse will:

- **Encourage** quality awareness and quality performance in all associates at all levels of the company through management leadership;
- **Promote** the participation of all associates in making individual contributions to the quality improvement process;
- **Support** continuous quality improvements by providing our associates with necessary training, tools and information feedback to enable enhancement of the quality of our products and services;
- **Develop** relationships with suppliers who consistently demonstrate their ability to fulfill quality, price and delivery objectives that are mutually beneficial; and;
- **Build** quality into our products and services, striving for zero defects in everything we do, thereby reducing cost and increasing **Total Customer Satisfaction**.

Quality Management Principles

In support of and in addition to the above policies, Littelfuse is committed to the following eight quality management principles:

- **Customer Focus:** Littelfuse depends on its customers and makes every effort to understand their current and future needs. Littelfuse strives to meet customer requirements and to exceed customer expectations.
- **Leadership:** Leaders at Littelfuse establish unity of purpose and direction for the organization. Our leaders should create and maintain the internal environment in which our associates can become fully involved in achieving company objectives.
- **Involvement of People:** Associates at all levels are the essence of Littelfuse. Their full involvement enables their abilities to be used for the benefit of the company.
- **Process Approach:** The results desired by Littelfuse are achieved more efficiently when activities and related resources are managed as a process.
- **System Approach to Management:** Identifying, understanding and managing interrelated processes as a system contributes to effectiveness and efficiency in achieving Littelfuse objectives.
- **Continual Improvement:** Continual improvement of the overall performance should be a permanent objective of Littelfuse.
- **Factual Approach to Decision Making:** Effective decisions are based on the analysis of data and information at Littelfuse.
- **Mutually Beneficial Supplier Relationships:** Littelfuse and its suppliers are interdependent and a mutually beneficial relationship enhances the ability of both to create value.

Quality Assurance

Littelfuse continually engages in processes designed to assure quality through all stages of production, including:

- **Incoming Material Quality:** Littelfuse vendor analysis programs provide stringent requirements before components are delivered to Littelfuse. In addition, purchased materials are tested rigidly at incoming inspection for specification compliance prior to acceptance for use.
- **Process Controls:** From silicon slice input through final testing, we use statistical methods to control all critical processes. Process audits and lot inspections are performed routinely at all stages of the manufacturing cycle.
- **Parametric Testing:** All devices are 100% computer tested for specific electrical characteristics at critical processing points.
- **Final Inspection:** Each completed manufacturing lot is sampled and tested for compliance with electrical and mechanical requirements.
- **Reliability Testing:** Random samples are taken from various product families for ongoing reliability testing.
- **Finished Goods Inspection:** Product assurance inspection is performed immediately prior to shipping.

Design Assurance

The design and production of Littelfuse devices is a demanding and challenging task. Disciplined skills coupled with advanced computer-aided design, production techniques, and test equipment are essential elements in Littelfuse's ability to meet your demands for the very highest levels of quality.

All products must first undergo rigid quality design reviews and pass extensive environmental life testing. Littelfuse uses Statistical Process Control (SPC) with associated control charts throughout to monitor the manufacturing processes.

Section continues on next page.

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Quality and Reliability Assurance (continued)

Only those products which pass tests designed to assure Littelfuse high quality and reliability standards, while economically satisfying customer requirements, are approved for shipment. All new products and materials must receive approval of QRA prior to being released to production.

The combination of reliability testing, process controls, and lot tracking assures the quality and reliability of Littelfuse's devices. Since even the best control systems cannot overcome measurement limitations, Littelfuse designs and manufactures its own computerized test equipment.

The Littelfuse Reliability Engineering Group conducts ongoing product reliability testing to further confirm the design and manufacturing parameters.

Reliability Stress Tests

The following table contains brief descriptions of the reliability tests commonly used in evaluating Littelfuse product reliability on a periodic basis. These tests are applied across product lines depending on product availability and test equipment capacities. Other tests may be performed when appropriate.

Test Type	Typical Conditions	Test Description	Standards
High Temperature AC Blocking	80% of Rated V_{DRM} (VAC-peak), 125°C or 150°C, 504 or 1008 hours	Evaluation of the reliability of product under bias conditions and elevated temperature	MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
High Temperature Storage Life	150°C, 1008 hours	Evaluation of the effects on devices after long periods of storage at high temperature	MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Biased Temperature & Humidity	52V_{DC}, 85°C, 85%RH, 504 up to 1008 hours	Evaluation of the reliability of non-hermetic packaged devices in humid environments	EIA/JEDEC, JESD22-A101
Temperature Cycle [Air to Air]	-65°C to 150°C, 15-minute dwell, 10 up to 100 cycles	Evaluation of the device's ability to withstand the exposure to extreme temperatures and the forces of TCE during transitions between temperatures	MIL-STD-750 (Method 1051), EIA/JEDEC, JESD22-A104
Thermal Shock [Liquid to Liquid]	0°C to 100°C, 5-minute dwell, 10-second transfer, 10 cycles	Evaluation of the device's ability to withstand the sudden changes in temperature and exposure to extreme temperatures	MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (PCT)	121°C, 100%RH, 2atm, 24 up to 168 hours	Accelerated environmental test to evaluate the moisture resistance of plastic packages	EIA/JEDEC, JESD22-A102
Resistance to Solder Heat	260°C, 30 seconds	Evaluation of the device's ability to withstand the temperatures as seen in wave soldering operations	MIL-STD-750 (Method 2031)
Solderability	Steam Aging (1 to 8 hrs) 245°C Solder Temperature	Evaluation of the solderability of device terminals after simulated aging	ANSI J-STD-002 JEDEC, JESD-B-102
Lead Bend	225g weight, three 90° bends	Evaluation of resistance of device leads to metal fatigue	MIL-STD-750 (Method 2036)
Moisture Sensitivity Level	85%RH, 85°C, 168hrs 3 reflow cycles (260°C peak)	Evaluation to determine device immunity to moisture	JEDEC J-STD-020 Level 1
ESD	HBM, 8kV CDM, 15kV	Evaluation to determine device immunity to electro-static discharge	JESD22-A114, MIL-STD-883D 3015.7, JESD22-C101

Flammability Test

For the UL 94V0 flammability test, all epoxies used in Littelfuse encapsulated devices are recognized by Underwriters Laboratories.

Revised: 02/23/17

Global Commitment to Green and Environmental Compliance

A Global Commitment to Green

Littelfuse has taken an industry-leading role with our global commitment to green. This commitment includes the establishment of focused and rigorous programs to develop high-performance eco-friendly products along with a comprehensive set of processing/reliability data and technical process expertise.

These processes are designed to detect, document and eliminate hazardous substances such as Lead, Cadmium, Hexavalent Chromium, Mercury and Brominated flame-retardants (PBB and PBDE) to ensure we deliver products that are RoHS compliant.

Environmental Compliance

As members of the global community, we at Littelfuse have always strived to understand the impact of what we do, and of what we create, on the world around us. Because of this, our concern for the environment has always been an integral and fundamental part of our business. We continually work to balance our business objectives with the need to protect and improve the local and global environment.

Primary Areas of Concern

Littelfuse is focused on a variety of environmental issues. A key area of concern is the reduction or elimination of specific toxic materials in the manufacturing of our products. This includes raw materials and processed materials purchased from our suppliers. Currently, we are focusing on the reduction and elimination of:

- Lead
- Cadmium
- Specific forms of Chromium (Hexavalent Cr)
- Mercury
- Specific Brominated Flame retardants

All of these substances are included in a class of substances immediately or gradually being banned by regional or country laws and ordinances. Littelfuse is committed to ensuring that the use of these substances ultimately be eliminated from our products so that we can comply with related laws and regulations and reduce the negative impact of these substances on the ecosystem and thereby contribute to the preservation of the global environment. This includes the use of these substances in all products that are designed, manufactured, sold or distributed by Littelfuse.

Environmental Management Practices

In effort to reduce and eliminate negative environmental impact of our operations, Littelfuse has devised comprehensive environmental management practices.

Through regular communication of objectives, action plans and achievements, Littelfuse associates are kept informed of these practices. Employees are fully committed to understanding and implementing the relevant aspects of our system as part of their day to day work.

Littelfuse is committed to minimizing the environmental impacts of its operations through various continual improvement programs. It is the practice of Littelfuse to:

- Comply with all applicable laws and regulations worldwide
- Reduce and eliminate the use of hazardous materials in our products
- Reduce the amount of raw materials used in operations and reuse, rather than dispose, whenever possible and promote recycling and use of recycled materials
- Prevent pollution by reducing and eliminating emissions to the environment
- Work closely with our customers and suppliers to minimize their overall impact on the environment
- Communicate environmental issues with all Littelfuse associates through training programs and meetings
- Monitor our environmental performance on a regular basis and communicate our progress to all interested parties

RoHS and Halogen-Free Definitions

RoHS **RoHS** (Restriction of Hazardous Substances): Product complies with the requirement of RoHS or EU directive 2002/95/EC and all of its amendments.

HF **Halogen-Free**: Product contains minimal halogens and their compounds in any form (exceeds IEC 61249-2-21):

- Chlorine: Less than 800 ppm of product weight
- Bromine: Less than 800 ppm of product weight
- All halogens combined (Fluorine, Chlorine, Bromine, Iodine) less than 1000 ppm of product weight

Revised: 02/23/17

Telecommunications Protection

Because early telecommunications equipment was constructed with components such as mechanical relays, coils, and vacuum tubes, it was somewhat immune to lightning and power fault conditions. But as step-by-step switches and digital loop carriers have given way to more modern equipment such as multiplexers, routers, gateways and IP switches, there is an increased need for protecting this equipment against system transients caused by lightning and power fault conditions.

Lightning

During an electrical storm, transient voltages are induced onto the telecommunications system by lightning currents which enter the conductive shield of suspended cable or through buried cables via ground currents.

As this occurs, the current traveling through the conductive shield of the cable produces an equal voltage on both the Tip and Ring conductors at the terminating ends. Known as a longitudinal voltage surge, the peak value and waveform associated with this condition is dependent upon the distance the transient travels down the cable and the materials with which the cable is constructed.

Although lightning-induced surges are always longitudinal in nature, imbalances resulting from terminating equipment and asymmetric operation of primary protectors can result in metallic transients as well. A Tip-to-Ring surge is normally seen in terminating equipment and is the primary reason most regulatory agencies require telecom equipment to have both longitudinal and metallic surge protection.

Power Fault

Another system transient that is a common occurrence for telecommunications cables is exposure to the AC power system. The common use of poles, trenches, and ground wires results in varying levels of exposure which can be categorized as direct power fault, power induction, and ground potential rise.

Direct power fault occurs when a power line makes direct contact to telecommunications cables. Direct contact is commonly caused by falling trees, winter icing, severe thunderstorms, and vehicle accidents. Direct power fault can result in large currents being present on the line.

Power induction is common where power cables and telecommunications cables are run in close proximity to one another. Electromagnetic coupling between the cables results in system transients being induced onto the telecommunications cables, which in turn can cause excessive heating and fires in terminal equipment located at the cable ends.

Ground potential rise is a result of large fault currents flowing to Ground. Due to the varying soil resistivity and multiple grounding points, system potential differences may result.

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Telecommunications Protection (continued)

Lightning is one of nature's most common and dangerous phenomena. At any one time, approximately 2,000 thunderstorms are in progress around the globe, with lightning striking the earth over 100 times per second. According to IEEE C.62, during a single year in the United States lightning strikes an average of 52 times per square mile, resulting in 100 deaths, 250 injuries, and over 100 million dollars in damage to equipment property.

The Lightning Phenomenon

Lightning is caused by the complex interaction of rain, ice, up drafts, and down drafts that occur during a typical thunderstorm. The movement of rain droplets and ice within the cloud results in a large build up of electrical charges at the top and bottom of the thunder cloud. Normally, positive charges are concentrated at the top of the thunderhead while negative charges accumulate near the bottom. Lightning itself does not occur until the potential difference between two charges is great enough to overcome the insulating resistance of air between them.

Formation of Lightning

Cloud-to-ground lightning begins forming as the level of negative charge contained in the lower cloud levels begins to increase and attract the positive charge located at Ground. When the formation of negative charge reaches its peak level, a surge of electrons called a stepped leader begins to head towards the earth. Moving in 50-meter increments, the stepped leader initiates the electrical path (channel) for the lightning strike. As the stepped leader moves closer to the ground, the mutual attraction between positive and negative charges results in a positive stream of electrons being pulled up from the ground to the stepped leader. The positively charged stream is known as a streamer. When the streamer and stepped leader make contact, it completes the electrical circuit between the cloud and ground. At that instant, an explosive flow of electrons travels to ground at half the speed of light and completes the formation of the lightning bolt.

Lightning Bolt

The initial flash of a lightning bolt results when the stepped leader and the streamer make connection resulting in the conduction of current to Ground. Subsequent strokes (3-4) occur as large amounts of negative charge move farther up the stepped leader. Known as return strokes, these subsequent bolts heat the air to temperatures in excess of 50,000°F and cause the flickering flash that is associated with lightning. The total duration of most lightning bolts lasts between 500 millisecond and one second.

During a lightning strike, the associated voltages range from 20,000 V to 1,000,000 V while currents average around 35,000 A. However, maximum currents associated with lightning have been measured as high as 300,000 A.

10 Key Facts about Lightning

1. Lightning strikes the earth on an average of 100 times per second.
2. Lightning strikes can affect computers and other electronic equipment as far as a kilometer away.
3. Lightning causes transient overvoltages (very fast electrical surges) on power, data communication, and signal and telephone lines. These surges then carry to and affect vulnerable equipment.
4. At-risk electronic equipment includes computer and peripheral equipment, building management systems, IP-PBX systems, CATV equipment, fire and security systems, PoE systems, and lightning arrays.
5. Transient overvoltages can cause instant damage to equipment and its circuitry, leading to costly and lengthy stoppages to operation and latent damage, and can result in breakdowns weeks or months later.
6. Even equipment in a building with structural lightning protection is still at great risk, as structural protection is designed to prevent damage to the building and to prevent loss of life.
7. While most businesses are at risk, campus or multi-building sites tend to be especially vulnerable.
8. Lightning can and does strike in the same place and can strike the same place multiple times. Sites that have suffered once are proven vulnerable and often suffer again within a matter of months.
9. Protecting electronic systems from transient overvoltage damage costs only a fraction of the cost of damage.
10. Littelfuse designs and manufactures quality lightning protection equipment.

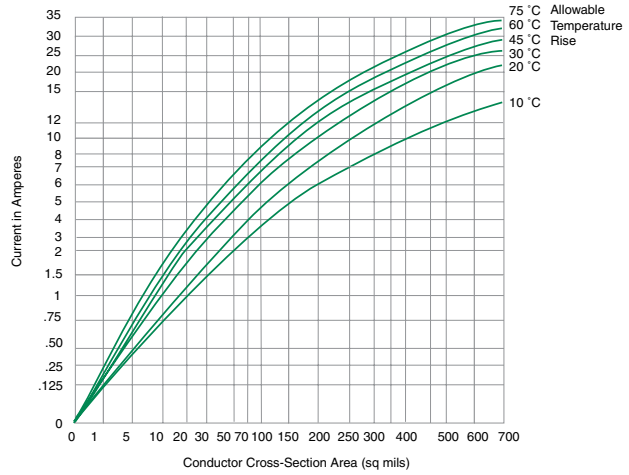
Telecommunications Protection (continued)

Because the interface portion of a Printed Circuit Board (PCB) is subjected to high voltages and surge currents, consideration should be given to the trace widths, trace separation, and grounding.

Trace Widths

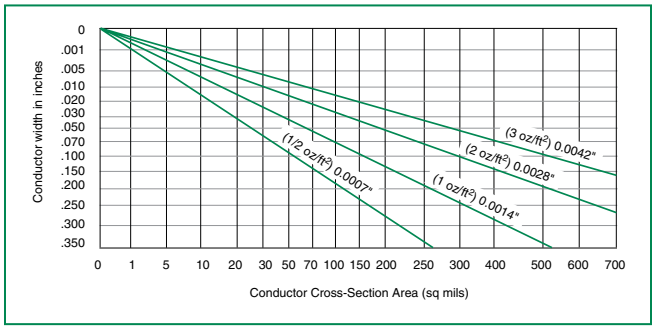
Based on the Institute for Interconnecting and Packaging Electronic Currents, IPC D 275 specifies the trace widths required for various current-carrying capacities. This is very important for grounding conditions to ensure the integrity of the trace during a surge event. The required width is dependent on the amount of copper used for the trace and the acceptable temperature rise which can be tolerated. Littelfuse recommends a 0.025-inch trace width with one ounce copper. (For example, a 38-AWG wire is equal to approximately 8 mils to 10 mils. Therefore, the minimum trace width should be greater than 10 mils.)

Figure 1.5 Current versus Area



The minimum width and thickness of conductors on a PCB is determined primarily by the current-carrying capacity required. This current-carrying capacity is limited by the allowable temperature rise of the etched copper conductor. An adjacent ground or power layer can significantly reduce this temperature rise. A single ground plane can generally raise the allowed current by 50 percent. An easy approximation can be generated by starting with the information in Figure 1.5 to calculate the conductor cross-sectional area required. Once this has been done, refer to Figure 1.6 for the conversion of the cross-sectional area to the required conductor width, dependent on the copper foil thickness of the trace.

Figure 1.6 Conductor Width versus Area



Trace Separation

Tip and Ring traces are subjected to various transient and overvoltage conditions. To prevent arcing between traces, minimum trace separation should be maintained. UL 60950 provides additional information regarding creepage and clearance requirements, which are dependent on the Comparative Tracking Index (CTI) rating of the PCB, working voltage, and the expected operating environment. For additional information refer to the UL 60950-1 summary in the Regulatory section of this catalog.

A good rule of thumb for outside layers is to maintain a minimum of 18 mils for 1 kV isolation. Route the Tip and Ring traces towards the edge of the PCB, away from areas containing static sensitive devices.

Section continues on next page.

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Telecommunications Protection (continued)

Grounding

Although often overlooked, grounding is a very important design consideration when laying out a protection interface circuit. To optimize its effectiveness, several things should be considered in sequence:

1. Provide a large copper plane with a grid pattern for the Ground reference point.
2. Decide whether to use a single-point or a multi-point grounding scheme. A single-point (also called centralized) grounding scheme is used for circuit dimensions smaller than one-tenth of a wavelength (λ = 300,000/frequency) and a multi-point (distributed) grounding scheme is used for circuit trace lengths greater than one-fourth of a wavelength.
3. Because traces exhibit a certain level of inductance, keep the length of the ground trace on the PCB as short as possible in order to minimize its voltage contribution during a transient condition. In order to determine the actual voltage contributed to trace inductance, use the following equations:

$V = L\ (di/dt)$

$L = 0.0051\ \rho\ [\log_e 2\ \rho/(t+w) + ½ - \log_e G]$ in µH
where ρ = length of trace

G = function of thickness and width (as provided in Table 1.2)

t = trace thickness

w = trace width

For example, assume circuit A is protected by a P3100SCL with a V_S equal to 300 V and a ground trace one inch in length and a self-inductance equal to 2.4 µH/inch. Assume circuit B has the identical characteristics as Circuit A, except the ground trace is five inches in length instead of one inch in length. If both circuits are surged with a 100 A, 10x1000 µs wave-form, the results would be as shown in Table 1.1:

Table 1.1 Overshoot Caused by Trace Inductance

	$V_L = L\ (di/dt)$	SIDACtor® device V_S	Protection Level ($V_L + V_S$)
Circuit A	V_L = 2.4 µH (100 A/10 µs) = 24 V	300 V	324 V
Circuit B	V_L = 12 µH (100 A/10 µs) = 120 V	300 V	420 V

Other practices to ensure sound grounding techniques are:

1. Cross signal grounds and earth grounds perpendicularly in order to minimize the field effects of "noisy" power supplies.
2. Make sure that the ground fingers on any edge connector extend farther out than any power or signal leads in order to guarantee that the ground connection invariably is connected first.

Table 1.2 Values of Constants for the Geometric Mean Distance of a Rectangle

t/w or w/t	K	$\log_e G$
0.000	0.22313	0.0
0.025	0.22333	0.00089
0.050	0.22346	0.00146
0.100	0.22360	0.00210
0.150	0.22366	0.00239
0.200	0.22369	0.00249
0.250	0.22369	0.00249
0.300	0.22368	0.00244
0.350	0.22366	0.00236
0.400	0.22364	0.00228
0.450	0.22362	0.00219
0.500	0.22360	0.00211
0.550	0.22358	0.00203
0.600	0.22357	0.00197
0.650	0.22356	0.00192
0.700	0.22355	0.00187
0.750	0.22354	0.00184
0.800	0.22353	0.00181
0.850	0.22353	0.00179
0.900	0.22353	0.00178
0.950	0.223525	0.00177
1.000	0.223525	0.00177

Note: Sides of the rectangle are t and w. The geometric mean distance R is given by: $\log_e R = \log_e(t+w) - 1.5 + \log_e G$. $R = K(t+w)$, $\log_e K = -1.5 + \log_e G$.

PCB Layout Considerations for an Ethernet Application or Other High Speed Circuits

1. Use at least a 4-layer PCB (this stack-up allows routing of critical signal traces without vias).
2. 2nd layer is a solid and contiguous ground plane.
3. 3rd layer is a solid power plane.
4. 4th layer is for bottom signal traces.
5. Use a single ground plane connection to chassis ground (reduces EMI and improves ESD resistibility characteristics).
6. Use void areas on both ground and power plane under any magnetic.
7. No PCB traces with 90° turns and proper width as indicated in SIDACtor catalogue.
8. Avoid vias and pads for any critical signals.
9. Use controlled impedances on all high speed traces with correct terminations (all differential signal traces should be equal length).
   a) 5-mil trace width and 5-mil trace separation of identical length and short as possible for TX/RX signal lines with 100 ohm controlled trace impedance pair (i.e. 50 ohm single-ended).
   b) If possible, separate adjacent TX/RX pairs > 20 mils apart from each other to reduce crosstalk issues.
10. Recognize propagation delays for traces on an outer layer is approximately 145 pS/inch while embedded trace between planes is approximately 180 pS/inch.
    a) Circuit board traces are generally considered as transmission lines if the unloaded signal transition (rise/fall) time is ≤ round-trip propagation delay on the trace.
    b) When this condition exists (PCB traces = transmission line) then line impedance control (exact and constant) is utmost importance.
    c) Use an in-line TVS Diode Array or SEP SIDACtor overvoltage protection device that allows traces to go directly underneath the device rather than using stub connections is best (minimizes signal ringing and signal reflections).
11. FR-4 PCB material is good for frequencies up to 500 MHz (but GE-Tek materials could be considered for performance enhancement over FR-4).
12. Place all IC coupling capacitors as close as practicable to IC with minimized lead lengths or SMT (same guidance for all crystal components).
13. Implement at least 0.30 inches separation between all PCB layers and PCB chassis ground.
14. Use a 1nF 2 kV capacitor between power supply ground and chassis ground.
15. Place high speed devices in close proximity to power supply so that shortest trace lengths can be used (reduces ground bounce).
16. Place overvoltage and overcurrent protection and transformer as close as possible to RJ45 connector.
17. For CAT5e systems, consider using 52 Ω in Bob Smith termination circuit instead of 75 Ω.
18. For CAT6 systems, consider using 66 Ω resistor in Bob Smith termination circuit instead of 75 Ω.

Revised: 02/23/17

PCB Placement Guidelines for QFN - Quad Flatpak No-Lead Package

Introduction

This document is written to serve as a guideline to help the user in developing the proper PCB design and surface mount process. Development effort and actual studies may still be needed to optimize the process in order to meet individual specific requirements.

Littelfuse's Q2L Quad Flatpak - No Lead Package (QFN) is a near Chip Scale Package (CSP) that uses conventional copper leadframe technology. Mechanical, thermal, and electrical connections are made through the exposed lands on the bottom of the package. This construction enables the use of a stable thermal path and electrical ground through a robust mechanical solder connection to the PCB. Its miniature dimension and low profile (1.0 mm height on PCB) requires less board area which increases board density compared to traditional leaded surface mount packages.

The QFN packaged product allows for a decreased package size without sacrificing performance. This package platform is ideal for high density circuits and for handheld electronic products.

Package Design

The QFN packages are designed in MAP (Matrix Array Package) leadframe format and individually singulated by using a saw process (see Fig. 1.7 below). It can provide customized body size and customized land format design for specific design needs and applications.

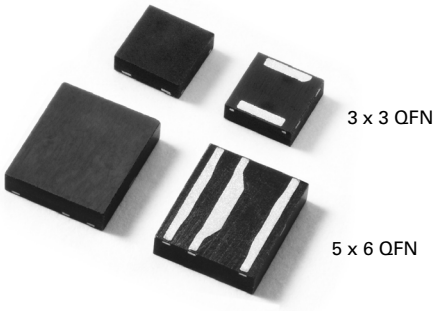


Figure 1.7: QFN package images

PCB Design Guidelines

There are two different types of PCB pad configurations commonly used for surface mount leadless QFN packages:

1) Non Solder Mask Defined Style (NSMD)

2) Solder Mask Defined Style (SMD)

The NSMD contact pads have the solder mask pulled away from the solderable metallization, while the SMD pads have the solder mask over the edge of the metallization.

With the SMD pads, the solder mask restricts the flow of solder paste on the top of metallization that prevents the solder from flowing along the side of the metal pad (see Fig. 1.8 below).

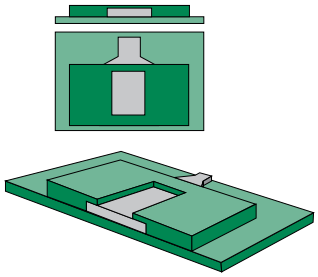


Figure 1.8: SMD pad

This is different from the NSMD where the solder will flow around both the top and sides of the metallization (see Fig. 1.9 below).

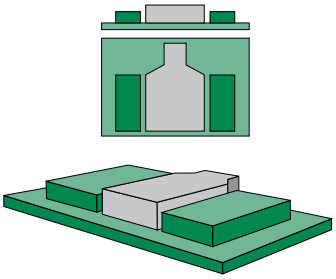


Figure 1.9: NSMD pad

NSMD pads are recommended over SMD pads since the copper etching process is capable of a tighter tolerance than the solder masking process. Additionally, NSMD pads with solder mask opening larger than the metal pad size also improves the reliability of the solder joint as solder is allowed to wrap around the sides of the metal pads.

NSMD Pad Design Considerations

The solder mask should be located at least +/-3 mils (0.076mm) away from the edge of the solderable pad when dimensionally possible. This allows for solder mask registration tolerances and ensures the solder is not inhibited by the mask as it reflows along the side of the metal pads.

Revised: 02/23/17

PCB Placement Guidelines for QFN - Quad Flatpak No-Lead Package (continued)

PCB Pad Pattern

The dimensions of the PCBs solderable pads should match those of the pads on the package (see Fig. 1.10 A-D below).

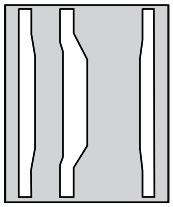


Figure 1.10 A:
5x6 OFN Footprint

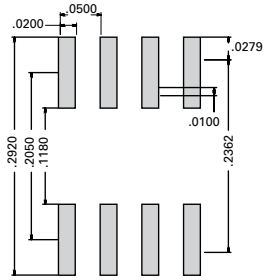


Figure 1.10 B:.
5x6 QFN PCB Layout

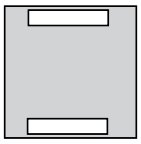


Figure 1.10 C:
3x3 OFN Footprint

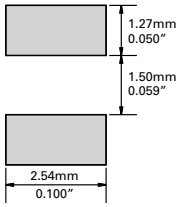


Figure 1.10 D:.
3x3 QFN PCB Layout

PCB Surface Finishes

The key factor in selecting an acceptable surface finish is to ensure that the land pads have a uniform coating. Irregular surface plating, uneven solder paste thickness, and crowning of the solder plating can reduce the overall surface mount yields.

There are two common surface finishes which are used for PCB surface mount devices. The first consists of an organic solderability preservative (OSP) coating over a copper plated pad. The organic coating assists in reducing oxidation in order to preserve the copper metallization for soldering.

The second recommended surface finish consists of plated electroless nickel over the copper pad followed by immersion gold.

Of all the coating and plating options available, Ni/Au is the most versatile, providing the gold thickness is controlled. Typically, 5um nickel, and between 0.05um and 0.1um gold are needed to prevent gold embrittlement which may affect the reliability of the solder joint.

Board Mounting Considerations

Solder Paste

The quality of the paste print is an important factor in producing high-yield assemblies. The paste is the vehicle that provides the flux and solder alloy necessary for a reliable and repeatable assembly process.

A low-residue, "no-clean" type 3 solder paste should be used in mounting QFNs. Typically, the choice of solder paste determines the profile and reflow parameters. Most paste manufacturers provide a suggested thermal profile for their productsand must be referenced prior to manufacturing.

Solder Stencil

The stencil thickness, as well as etched pattern geometry, determines the precise volume of solder paste deposited onto the device land pattern. Stencil alignment accuracy and consistent solder volume transfer are critical for uniform reflow-solder processing.

Stencils are usually made of brass or stainless steel, with stainless steel being more durable. Apertures must be trapezoidal to ensure uniform release of the solder paste and to reduce smearing (see Fig. 1.11).

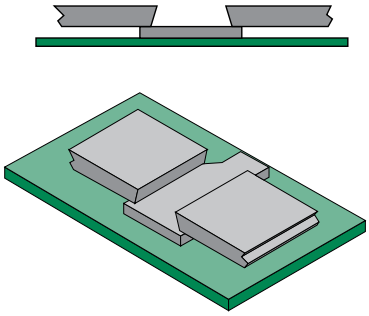


Figure 1.11: Solder Stencil Profile

The solder joint thickness of QFN lead fingers must be 0.050mm to 0.075mm. Thickness of the stencils is usually in the 0.100mm to 0.150mm.

The blade angle and speed must be fine-tuned to ensure even paste transfer. An inspection of stenciled board is recommended before placing the parts, because proper stencil application is the most important factor with regards to reflow yields further on in the process. As a guide, stencil thickness of 0.125mm for QFN components is recommended.

Revised: 02/23/17

PCB Placement Guidelines for QFN - Quad Flatpak No-Lead Package (continued)

Lead Finger Stencil Design

The optimum and reliable solder joints on the perimeter pads should have 50 to 75 microns (2 to 3 mils) standoff height.

The first step in achieving good standoff is the solder paste stencil design for perimeter pads. The stencil aperture opening should be designed so that the maximum paste release is achieved. This is typically achieved by considering the following two ratios:

1) Area Ratio = Area of Aperture Opening / Area of Aperture Wall
2) Aspect Ratio = Aperture Width / Stencil Thickness

For rectangular aperture openings, as required for this package, these ratios are:

Area Ratio = LW/2T(L+W)

Aspect ratio = W/T

where L & W are aperture length and width, T is stencil thickness.

For optimum paste release the area and aspect ratios should be greater than 0.66 and 1.5 respectively.

It is recommended that stencil aperture should be 1:1 to PCB pad sizes as both area and aspect ratio targets are easily achieved by this aperture.

The stencil should be laser cut and electropolished. The polishing helps in smoothing the stencil walls resulting in better paste release.

It is also recommended that the stencil aperture tolerances should be tightly controlled, especially for 0.4 and 0.5mm pitch devices, as these tolerances can effectively reduce the aperture size.

Package Placement and Alignment

The pick and place accuracy governs the package placement and rotational (theta) alignment. This is equipment/ process dependent. Slightly misaligned pads (less than 50% off the pad center) automatically self-align during reflow due to surface tension of the solder (see Fig. 1.12).

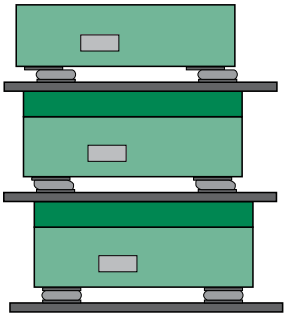


Figure 1.12: Self-Assignment at Reflow

Grossly misaligned packages (greater than 50% off the pad center) must be removed prior to reflow, as they may develop electrical shorts resulting from solder bridges, if they are subjected to reflow.

Solder Reflow

There are no special requirements when reflowing QFN components. As with all SMT components, it is important that profiles be checked on all new board designs.

In addition, if there are multiple packages on the board, the profile must be checked at different locations on the PCB. Component temperatures may vary because of surrounding components, location of the device on the board, and package densities.

Figure 1.13 is an example of a standard reflow profile for a lead-free solder paste. The paste manufacturer will determine the exact profile, since the chemistry and viscosity of the flux may vary.

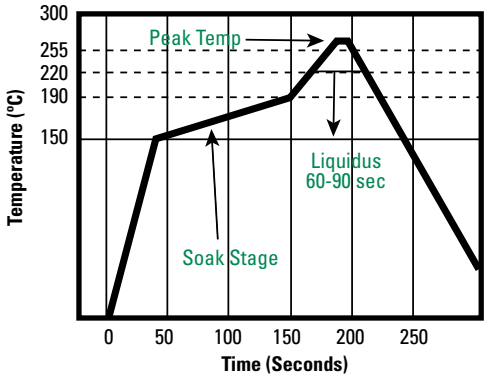


Figure 1.13: Typical Profiles for Lead-Free Solder

In general, the temperature of the part should not be raised more than 2° C/sec during the initial stages of the reflow profile. The soak zone then occurs when the part is approximately 150° C up to 190° C and should last for 90 to 120 seconds. Extending the time in the soak zone will typically reduce the risk of voiding within the solder. The temperature is then raised and will be above the liquidus of the solder for 60 to 90 seconds depending on the mass of the board. The peak temperature of the profile should be 30° C to 40° C above the melting point of the solder. However, the temperature during reflow should not exceed the maximum temperature the package is qualified for according to Moisture Sensitivity Level Testing. Finally, Ramp Down Rate from peak temperature to room temperature should not exceed 4° C/sec.

PCB Cleaning

If a low-residue, "No Clean" solder paste is used, PCB cleaning is not required, and has little effect on QFNs. "No Clean" solder paste simply means that there are no harmful residues left on the board that could cause corrosion or damage to the components if left on the board.

However, some types of "No Clean" solder paste may not be satisfyingly free from contamination on the final board, so it is recommended that an experiment should be conducted to examine whether eventually the flux residues are required to be removed.

PCB Placement Guidelines for QFN - Quad Flatpak No-Lead Package (continued)

Solder Joint Inspection

Inspection of QFNs on a PCB is commonly accomplished with the use of an X-ray inspection system.

In most cases, 100% inspection is not performed. Typically, X -ray inspection is used to establish process parameters and then to monitor the production equipment and process. The X-ray inspection system can detect bridging, shorts, opens, and solder voids.

In addition to searching for defects, the mounted device should be rotated on its side to inspect the sides of the solder joints. These joints should have enough solder volume with the proper stand-of height so than an "hour glass" shaped connection is not formed (see Fig. 1.14 below).

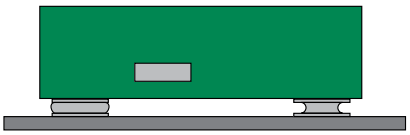


Figure 1.14: Desirable vs. Hour Glass Solder Joint

Rework Methodology

Due to the fact that the QFN is a leadless device, the entire package must be removed from the PCB if there is an issue with the solder joints. It is important to minimize the chance of overheating neighboring devices during the removal of the package since the devices are typically in close proximity with each other.

Standard SMT rework systems are recommended for this procedure since the airflow and temperature gradients can be carefully controlled. It is also recommended that the PCB be placed in an oven at 125° C for 4 to 8 hours prior to heating the parts to remove excess moisture from the packages.

Component Removal

The gas nozzle used during this process surrounds the device and seals against the board. The QFN is heated from the topside with hot gas while residual heat is exhausted up and away from adjacent components.
The anti-crushing feature in the nozzle prevents excessive topside force from being applied to the QFN.

The entire assembly is also heated from the bottom side with an under-board heater to help prevent warpage.

Preheating the board to a fixed temperature before the component is heated also helps to ensure process repeatability.

Once the reflow process is complete, the nozzle vacuum cup is automatically activated and the component is slowly lifted off the pads. The vacuum cup in the nozzle is designed to disengage if the component has not fully reflowed for any reason. This prevents the potential for lifting pads.

Site Redress

Once the QFN has been removed, the residual solder that remains on the pads must be removed. The QFN PCB site is very fragile because of its small pad sizes. To avoid damaging the pads or solder mask, the site redress process must be performed very carefully. "No Clean" flux is applied to the site after component removal. Using a temperature-controlled soldering iron fitted with a small flat blade, gently apply solder braid that has been presoaked in flux over the PCB pads.

Residual flux is removed from the site with alcohol and a lint-free swab. This site is then inspected prior to the replacement process.

Component Replacement and Reflow

Due to the small pad configurations of the QFN, and since the pads are on the underside of the package, a manual pick and place procedure without the aid of magnification is not recommended. A dual image optical system where the underside of the package can be aligned to the PC board should be used instead.

Reflowing the component onto the board can be accomplished by either passing the board through the original reflow profile, or by selectively heating the QFN with the same process that was used to remove it. The benefit of subjecting the entire board to a second reflow is that the QFNs will be mounted consistently and by a profile that was already defined. The disadvantage is that all of the other devices mounted with the same solder type will be reflowed for a second time.

If subjecting all of the parts to a second reflow is either a concern or unacceptable for a specific application, then the localized reflow option would be the recommended procedure.

Revised: 02/23/17

Lead-Free Soldering Recommendations

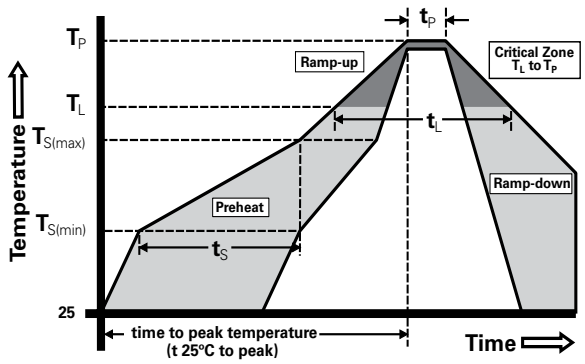
Littelfuse now offers only RoHS-compliant SIDACtor® devices. This conversion requires a change from former Sn-Pb board-mounting process parameters for two reasons:

- The wettability (how well the molten solder flows on solderable surfaces) is degraded for Sn-Ag-Cu alloys (industry-preferred lead-free solder) as compared to Sn-Pb eutectics.
- The melting point for Sn-Ag-Cu alloys is typically around 220°C (varying slightly among different alloys), much higher than the 183°C melting point of conventional Sn-Pb eutectic solder.

Increasing profile temperatures and/or dwell times typically overcomes these issues.

This board-mounting standard serves as a design guideline for the electronics business unit relative to lead-free or RoHS-compliant product development across all Littelfuse facilities worldwide. This design guideline is applicable to all new product development programs as well as modifications of existing products.

Recommended Soldering Reflow Profile



Convection Reflow - Surface Mount Devices (SMD)

Table 1.3 defines the reflow parameter and lead-free requirements for convection reflow SMD soldering.

Table 1.3 Convection Reflow (SMD) Parameters and Lead-Free Requirement

Reflow Condition		Pb-Free assembly (see figure above)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Wave Solder - Through-Hole Devices (THD)

Table 1.4 defines the wave parameter and lead-free requirements for THD wave soldering.

Table 1.4 Wave Solder (THD) Parameters and Lead-Free Requirement

Reflow Parameter	Lead-Free Requirement
Preheat (depending on flux only) Temperature Min Temperature Max Time (Min to Max)	 150°C 200°C 60–180 seconds
Solder Pot Temperature	245–265°C (Max)
Solder Dwell Time	2–3.5 seconds
Cooling	-6°C/second (Max)

Revised: 02/23/17

Sn-Pb Soldering Recommendations

When placing surface mount components, a good solder bond is critical because:

- The solder provides a thermal path in which heat is dissipated from the packaged silicon to the rest of board
- A good bond is less subject to thermal fatiguing and results in improved component reliability.

Reflow Soldering

The preferred technique for mounting the DO-214AA package is to reflow-solder the device onto a PCB-printed circuit board, as shown in Figure 1.15.

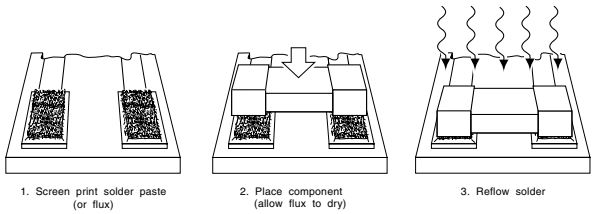


Figure 1.15: Reflow Soldering Procedure

For reliable connections, the PCB should first be screen printed with a solder paste or fluxed with an easily removable, reliable solution, such as Alpha 5003 diluted with benzyl alcohol. If using a flux, the PCB should be allowed to dry to touch at room temperature (or in a 70°C oven) prior to placing the components on the solder pads.

Relying on the adhesive nature of the solder paste or flux to prevent the devices from moving prior to reflow, components should be placed with either a vacuum pencil or automated pick and place machine.

With the components in place, the PCB should be heated to a point where the solder on the pads begins to flow. This is typically done on a conveyor belt which first transports the PCB through a pre-heating zone. The pre-heating zone is necessary in order to reduce thermal shock and prevent damage to the devices being soldered, and should be limited to a maximum temperature of 165°C for 10 seconds.

After pre-heating, the PCB goes to a vapor zone. The vapor zone is obtained by heating an inactive fluid to its boiling point while using a vapor lock to regulate the chamber temperature. This temperature is typically 215°C, but for temperatures in excess of 215°C, care should be taken so that the maximum temperature of the leads does not exceed 275°C and the maximum temperature of the plastic body does not exceed 260°C. (Figure 1.16)

During reflow, the surface tension of the liquid solder draws the leads of the device towards the center of the soldering area, correcting any misalignment that may have occurred during placement and allowing the device to set flush on the pad. If the footprints of the pad are not concentrically aligned, the same effect can result in undesirable shifts as well. Therefore, it is important to use a standard contact pattern which leaves sufficient room for self-positioning.

After the solder cools, connections should be visually inspected and remnants of the flux removed using a vapor degreaser with an azeotrope solvent or equivalent.

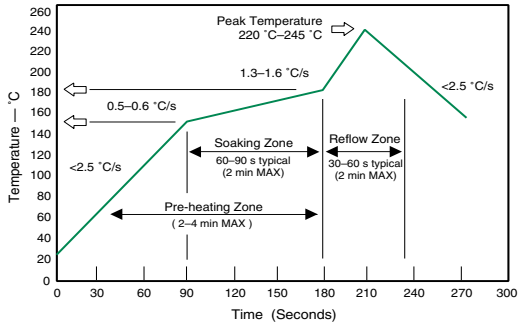


Figure 1.16: Reflow Soldering Profile for SN-Pb Soldering

Wave Soldering

Another method for soldering components to a PCB is wave soldering. After fluxing the PCB, an adhesive is applied to the respective footprints so that components can be glued in place. Once the adhesive cures, the board is pre-heated and then placed in contact with a molten wave of solder with a temperature between 240°C and 260°C and permanently affixes the component to the PCB (Figures 1.17 & 1.18)

Although a popular method, wave soldering has drawbacks:

- A double pass is often required to remove excess solder
- Solder bridging and shadows begin to occur as board density increases
- Wave soldering uses the sharpest thermal gradient

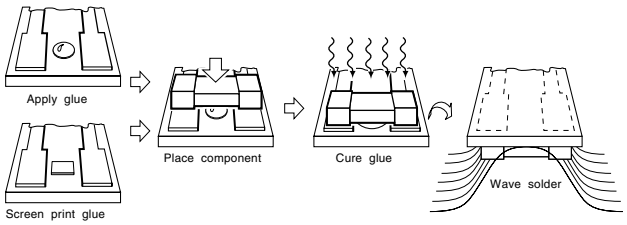


Figure 1.17: Wave Soldering of Surface Mount Components

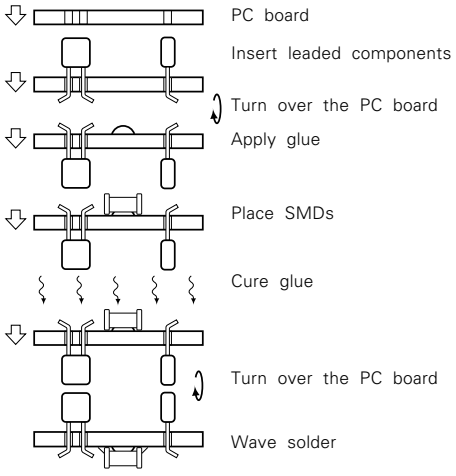


Figure 1.18: Wave Soldering of Surface Mount and Leaded Components

Revised: 02/23/17

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Revised: 02/23/17

Regulatory Requirements

Surge Waveforms for Various Standards

TIA-968-A Telecommunications - Telephone Terminal Equipment - Technical Requirements for Connection of Terminal Equipment to the Telephone Network, is valid for approvals until March 22, 2011 when it will be superseded by TIA-968-B. Until March 22, 2011, users may cite either TIA-968-A, along with its addenda, or TIA-968-B.

TIA-968-A replaced FCC Part 68 with the exception of hearing aid compatibility (HAC), volume control, and indoor cabling. TIA-968-B now in turn replaces TIA-968-A and its A1,A2, A3, and A4 addenda. This new version is closely harmonized with the Canadian CS03 requirements. Continued efforts between TIA TR41 and Industry Canada will continue these harmonization efforts. Various countries around the world also recognize this USA standard and use it either wholly or in part for their telephone terminal equipment programs.

GR 1089 is a standard generally supported by the US Regional Bell Operating Companies (RBOCs). It is updated by Telcordia Technology (formerly Bellcore). The RBOCs typically require compliance with GR 1089 for any of their telecom purchases. GR-1089 Issue 6 is the most recent update as is expected to be published March 2011.

The ITU is a specialized agency of the UN devoted to international harmonization. Most European countries recognize the ITU standards.

CNET is the Centre National d'etudes de Telecommunications, a French organization.

VDE is the Verband Deutsher Elektrotechniker, a Federation of German electrical engineers. VDE is very similar to the IEEE (Institute of Electrical and Electronics Engineers) but is national in scope rather than global.

ANSI is the American National Standards Institute, which is a non-government organization. The British equivalent to this is BSI.

IEC is the International Electrotechnical Commission, a result of Europe's move toward a single market structure and its drive to formalize and harmonize member countries' requirements.

FTZ R12 is a German specification.

Mainland China publishes various technical requirements and test methods for protection of telecommunication equipment, terminal equipment, and access network equipment. Some of these standards are based on ITU-T Recommendations. Type testing, factory inspection and follow-up factory inspection procedures similar to those imposed by UL within the USA, are also required in China.

The following page contains Table 3.1, which shows in its far right most column the recommended SIDACtor ® device surge rating (A, B, or C) that is required to comply with each specific waveshape definition without the need of additional limiting resistors.

Revised: 02/23/17

Regulatory Requirements (continued)

Table 3.1 Surge Waveforms for Various Standards

Standard			Peak Voltage	Rise/Decay time	Peak current	Rise/Decay time	SIDACtor® Device
			Volts	µs	Amps	µs	w/o series R
TIA-968-B	Surge A Metallic		800 - 880	6-10/560-860	100 - 115	5-10/560-760	C
	Surge A Longitudinal		1500 - 1650	6-10 /160-260	200 - 230	5-10/160-210	C
	Surge B Metallic		1000 - 1100	9±2.7/720±144	25 - 27.5	5±1.5/320±64	A, B or C
	Surge B Longitudinal		1500 - 1650	9±2.7/720±144	37.5 – 41.3	5±1.5/320±64	A, B or C
GR 1089	Test 1		600	10x1000	100	10x1000	C
	Test 2		1000	10x360	100	10x360	B or C
	Test 3		1000	10x1000	100	10x1000	C
	Test 4		2500	2x10	500	2x10	C
	Test 5		1000	10x360	25	10x360	A, B or C
CNET 131-24			1000	0.5x700	25	0.8x310	A, B or C
VDE 0433			2000	10x700	50	5x310	A, B or C
VDE 0878			2000	1.2x50	50	1x20	A, B or C
IEC 61000-4-5	Metallic	Class 2	500	1.2x50	12	8x20	A, B or C
		Class 3	1000	1.2x50	24	8x20	A, B or C
		Class 4 & 5	2000	10x700	48	5x310	B or C
	Longitudinal	Class 2*	1000	1.2x50	24	8x20	A, B or C
		Class 3*	2000	1.2x50	48	8x20	A, B or C
		Class 4* & 5*	4000	1.2x50	96	8x20	A, B or C
		Class 5* long-distance circuits	4000	10x700	100	5x310	A, B or C
FTZ R12			2000	10x700	50	5x310	A, B or C
YD/T 993-1998	Without Primary Protection Metallic, Single Tip and Ring Pair		1500	10x700	37.5	5x310	A, B or C
			1500	10x700	37.5	5x310	A, B or C
	Without Primary Protection Longitudinal, Single Tip and Ring Pair		1500	10x700	37.5	5x310	A, B or C
			1500	10x700	37.5	5x310	A, B or C
	Without Primary Protection Longitudinal, All Tip and Ring Pair		1000	10x700	25	5x310	A, B or C
			1000	10x700	25	5x310	A, B or C
	With Primary Protection Metallic, Single Tip and Ring Pair		4000	10x700	100	5x310	C
			4000	10x700	100	5x310	C
	With Primary Protection Longitudinal, Single Tip and Ring Pair		4000	10x700	100	5x310	C
			4000	10x700	100	5x310	C
	With Primary Protection Longitudinal, All Tip and Ring Pair		4000	10x700	100	5x310	C
			4000	10x700	100	5x310	C
			Without Primary Protector / With Primary Protector				
ITU K.20	Basic single port		1000 / 4000	10x700	25 / 100	5x310	A, B, C / B, C
	Enhanced single		1500 / 4000	10x700	37.5 / 100	5x310	A, B, C / B, C
	Basic multiple ports		1500 / 4000	10x700	37.5 / 100	5x310	A, B, C / B, C
	Enhanced multiple		1500 / 6000	10x700	37.5 / 150	5x310	A, B, C / C
	Basic power fault		600	50 Hz, 60 Hz	1	0.2 s	04611.25
	Enhanced power fault		600 / 1500	50 Hz, 60 Hz	1 / 7.5	0.2 s / 2 s	04611.25
ITU K.21	Basic single port		1500 / 4000	10x700	37.5 / 100	5x310	A, B, C / B, C
	Enhanced single		6000 / 6000	10x700	37.5 / 150	5x310	A, B, C / C
	Basic multiple ports		1500 / 4000	10x700	37.5 / 100	5x310	A, B, C / B, C
	Enhanced multiple		1500 / 6000	10x700	37.5 / 150	5x310	A, B, C / C
	Basic power fault		600	50 Hz, 60Hz	1	0.2 s	04611.25
	Enhanced power fault		600 / 1500	50 Hz, 60Hz	1 / 7.5	0.2 s / 2 s	04611.25

* Tested with Primary Protection

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Regulatory Requirements (continued)

GR-1089-CORE

In the United States, the telecommunication network is primarily operated by the Regional Bell Operating Companies (RBOC) who follow the standards set by the Generic Requirements (GR) document referred to as GR-1089-CORE, "*Electromagnetic Compatibility and Electrical Safety - Generic Criteria for Network Telecommunications Equipment*". This GR document provides criteria for both EMC and electrical safety for equipment that is used in Central Offices (COs), Remote Terminals (RTs), Controlled Environmental Vaults (CEVs), Electronic Equipment Enclosures (EEEs), network equipment located at the customer premises, and other such locations. This document reflects the opinion of Telcordia and participating industry representatives. The criteria in this document are intended to insure safe and reliable operation of equipment during and after nearby lightning strikes, 60 Hz power fault conditions, Electrostatic Discharge events (ESD), Electrical Fast Transient events (EFTs), and Electromagnetic Interference events (EMI). These criteria apply to wireless systems installed in telecommunication network equipment locations. The following sections apply to specific interface ports of the equipment.

Section 2 of GR-1089 addresses EFT.

Section 3 addresses conducted emission & immunity criteria

Section 4 addresses lightning and AC power fault

Section 5 addresses steady-state power induction

Section 6 addresses DC potential difference

Section 8 addresses corrosion

Section 10 addresses DC power port load equipment

These interface ports could be coaxial cable, signal, telecommunication, antenna, and power. In this document, a telecommunication port includes paired conductor interfaces such as the tip and ring leads, sleeve leads, E & M leads, and 10/100/1000 BaseT ports (including PoE).

Section 7, *Electrical Safety Criteria*, addresses the safety of personnel who have access to the equipment

Section 9, *Bonding and Grounding*, describes the requirements for grounding systems

The criteria for these standards are based on the assumption that a primary protector will limit transient voltages to 1000 V peak for surge conditions and 600 V rms for power fault conditions. All network equipment shall be listed by a Nationally Recognized Testing Laboratory (NRTL) if the equipment is directly powered by Commercial AC. Network equipment located on customer premises shall be listed by a NRTL. Equipment required to meet GR 1089 must be designed to pass:

- Both First and Second Level Lightning Surge and AC Power Fault Tests
- Current Limiter Test
- Short Circuit Test

GR-1089 compliant products shall be manufactured in accordance with the applicable requirements contained in:

Federal Communications Commission (FCC) {specifically FCC Part 68, Part 15, and TIA-968-A}

National Electric Code (NEC)

National Electrical Safety Code (NESC)

Department of Labor – Occupational Safety and Health Administration (OSHA)

And other applicable local requirements, including country (parish), state and federal law, regulations, and ordinances.

In conjunction with primary voltage protectors, operating companies also may incorporate fuse links if there is the possibility of exposing the twisted pair to outside power lines. These fuse links are equivalent to 24- or 26-gauge copper wire and are coordinated with the current-carrying capacity of the voltage protector.

The last element of protection that may be provided by the operating company are current limiters which, if provided, are found on the line side of the network equipment after the primary voltage protection device. These current limiters typically come in the form of heat coils and have a continuous rating of 350 mA.

Changes to GR-1089

Changes to Section 4 of the GR 1089 in October 2002 now require conformance with additional definitions and tests:

- Ethernet (including 10BaseT, 100BaseT, and 1000BaseT) are considered telecommunications lines and GR 1089 requirements apply.
- The 2x10 surge is not used for systems having primary protectors mounted on the side of the enclosure or within the enclosure. It also is not used if the length of the conductors between the primary protector and the circuit pack is less than one meter if a metallic enclosure is used and all terminals are bonded to the enclosure and the longest dimension of the enclosure is less than three meters.
- The 600 V and 1000 V 100 A 10x1000 surge events voltage level may be reduced for CO equipment using solid state protectors.
- The secondary protector must coordinate with the primary protector OR have a 100 A 10x1000 rating. This requirement became effective January 2006; before that date it was only an objective.
- First level power fault adds a 440 V 2.2 A two-second test and a 600 V 3 A 1.1-second test.
- Second level testing allows the wiring simulator fuse to be either the MDL 2.0 A or the MDQ 1.6 A. The second level requirement is the same for either the CPE or non-CPE.

Additional 15-minute test conditions of 3 A, 3.75 A, 5 A, 10 A, 12.5 A, 20 A, and 30 A conditions have been added. However, compliance with UL 60950 Annex NAC conditions 3, 4, and 5 are still accepted. The 2 A and 2.6 A tests are conducted without the simulator fuse in the circuit. However, it must meet applicable time-current curve.

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Regulatory Requirements (continued)

Reasons for GR-1089-CORE, Issue 3

- Section 2, *System-Level Electrostatic Discharge (ESD)*
  Harmonize with the recent revisions to IEC 61000-4-2 (ESD), and IEC 61000-4-4. (EFT)
- Section 3, *Electromagnetic Interference*
  Add conducted emissions and immunity criteria at broadband frequencies
- Section 4, *Lightning and AC Power Fault Resistibility*
  Add a conditional requirement and objective regarding external current limiters in high-speed digital networks, add an objective to address coordination, change 1st level power fault tests 6, 7, 8, and 9 from objectives to requirements, clarify the number of samples to be tested, clarify the number of ports to be tested, revise the criteria for customer premises 2nd level power fault tests, clarify the test procedure for 1st level tests and relocate all listing requirements to Section 7.
- Section 5, *Steady-State Power Induction*
  Add criteria for coaxial port immunity to steady-state power induction.
- Section 7, *Electrical Safety Criteria*
  Harmonize electrical safety terminology with international and North American telecommunications safety standards.
- Section 9, *Bonding and Grounding*
  Provide guidance on the application of the criteria to various types of network equipment add criteria for bonding, modify the short-circuit tests clarify the number of samples required to be tested, provide test procedures related to non-switching systems, clarify test procedures where necessary.

Reasons for GR-1089-CORE, Issue 4

- Include wireless systems criteria.
- Add a new definition appendix.
- Clarify criteria and test procedures.
- Section 1, *Introduction*
  Included guidelines for evaluation and added generic criteria.
- Section 2, *System-Level Electrostatic Discharge (ESD)*
  Extended date for objective to become a requirement, revised the ESD Warning Labels and established date for EFT objectives to become requirements.
- Section 3, *Electromagnetic Interference*
  Adopted the new FCC Part 15 requirements for ac power lines, revised the conducted emissions and immunity criteria for dc power ports and revised the conducted emissions and immunity criteria for broadband leads.
- Section 4, *Lightning and AC Power Fault Resistibility*
  Clarified procedures for calibration of generators, revised test conditions for equipment with 4-wire and multi-wire interfaces, changed the number of samples to be tested for second-level tests , added intra-building criteria for equipment with multi-wire interfaces, added intra-building criteria for equipment connected to shielded cables, communications and coaxial , revised second-level tests as applied to equipment with secondary protection , added surge testing methods for equipment that delivers power over communications wiring, revised the protection coordination tests, established new equipment port type for equipment located at remote sites, added a new subsection that provides appropriate criteria for equipment with agreed primary protection, added a new subsection that provides appropriate criteria for equipment with integrated primary protection, revised lightning criteria for equipment with ac power ports and added surge criteria for dc power ports for equipment located at OSP facilities.
- Section 7, *Electrical Safety Criteria*
  revised test procedure for classifying the source limits and revised the powering limitation criteria
- Section 9, *Bonding and Grounding*
  revised the grounding requirements of embedded power sources than 150 VA for specific applications.
- Section 10, *DC Power Port of Telecom. Equipment*
  revised the grounding requirements of embedded power sources than 150 VA for specific applications. that provides criteria on dc power ports of telecommunications equipment, which are powered from a shared dc power plant.

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Regulatory Requirements (continued)

Section 2 System-Level Electrostatic Discharge (ESD) and Electrical Fast Transient (EFT)

Circuit packs are tested for ESD immunity at the system level only (see Table 3.2). Therefore, ESD events are applied to faceplates, ejector tabs, etc. points and surfaces that are accessible during normal operation of the equipment and under installation and maintenance conditions. GR-78-CORE *Generic Requirements for the Physical Design and Manufacture of Telecommunications Products and Equipment* contains ESD immunity criteria for stand-alone circuit cards.

The EUT shall be tested using the methods of IEC 61000-4-2 (ESD), clauses 7 and 8, with the preferred method being the contact discharge method as specified in clause 7. The EUT shall not be damaged and shall continue to operate without negatively affecting service nor requiring the need for manual intervention.

Table 3.2: ESD Immunity Requirements for Normal Operation Mode and Installation & Maintenance Mode

Test Level	Air discharge	Contact discharge	Repetitions
2	4 kV		±10*
4	15 kV		±10*
4		8kV	±10*

* For a total of 40 times for air discharge or a total of 20 times for contact discharges

The EUT shall be tested using the methods of IEC 61000-4-4 (EFT), clauses 6, 7, & 8 (see Table 3.3). The capacitively coupling clamp specified in clause 6.3 of IEC 61000-4-4 is the preferred EFT test method. IF Bit Error Rate (BER) measuring equipment is used to verify the EUT performance, then this BER measuring equipment must be able to withstand the EFT burst application.

Table 3.3: EFT Immunity Requirements by port type

Port Types	Voltage	Total Number of 5 kHz repetition frequency events
1 & 2	0.25 kV	±5*
3& 4	0.5 kV	±5*
AC & DC ports	0.5 kV	±5*
AC & DC ports on customer premises	1 kV	±5*

* For a duration of 1 minute.

Section 4 Lightning and AC Power Fault

The lightning surge and ac power fault test conditions shall be applied to telecommunications ports, antenna ports, ac power ports, dc power ports, and coaxial cable ports.

Table 3.4 below provides the description of Test conditions "A" and "B" for both 2-wire and 4-wire interfaces. Intra-building tests apply to ports that are not directly connected to OSP (outside plant). These are designated as Type 2 and Type 4 ports. Type 1, 3, and 5 ports are directly connected to the OSP, therefore the inter-building tests apply. These three port types are subjected to short-circuit tests with 1st level criteria for compliance. These short-circuit tests are applied for 30 minutes between:

1. tip to ring
2. tip to ground with ring open
3. ring to ground with tip open
4. tip and ring to ground simultaneously

GR-1089 defines a 1st level and 2nd level criteria for the EUT (equipment under test).

1st Level Criteria:

The EUT shall not be damaged and shall continue to function properly without human intervention or power cycling after the tests

2nd Criteria:

The EUT may sustain damage but it shall not become a fire or fragmentation hazard nor an electrical safety hazard

Table 3.4: Tests Conditions

Test	Generator connections	
	2-wire interfaces	4-wire interfaces
A	1. tip to generator, ring to ground	1. tip to generator, ring, tip1, ring1 to ground
	2. ring to generator, tip to ground	2. ring to generator, tip, tip1, ring1 to ground
	3. Not applicable	3. tip1 to generator, tip, ring, ring1 to ground
	4. Not applicable	4. ring1 to generator, tip, ring, tip1 to ground
	5. tip and ring to generator simultaneously	5. tip and ring to generator simultaneously, tip1 and ring1 to ground
	6. Not applicable	6. tip1 and ring1 to generator simultaneously, tip and ring to ground
B	Tip and ring to generator simultaneously	Tip, ring, tip1, and ring1 to generator simultaneously

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Regulatory Requirements (continued)

Figure 3.1: Application of Lightning and AC Power Fault Test Voltages

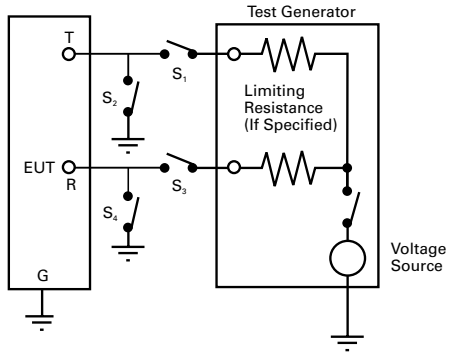


Table 3.5: Connections to Test Generator

	S1	S2	S3	S4
A1	CLOSED	OPEN	OPEN	CLOSED
A2	OPEN	CLOSED	CLOSED	OPEN
A5	CLOSED	OPEN	CLOSED	OPEN

For equipment that provides or receives remote power (i.e. span powering, PoE, etc.) over the copper conductors, GR-1089 contains an objective (NOT a requirement) that a coupling element should be used to isolate auxiliary or load equipment from the surge source for ±10 repetitions of surge test #3 (Table 3.6 below), then the remaining ±15 repetitions should be performed by applying the surge directly to the port. This coupling element is used to reduce the surge energy that would otherwise enter the power source (please see Figure 4-3, 4-4, 4-5, 4-6, 4-7, and 4-8 of GR-1089-CORE Issue 4 for more details).

First Level Lightning Surge Test

For all First Level lightning and power fault events, a total of three ports of the EUT shall be tested.

Table 3.6: First Level Lightning Surge Tests

Test (notes 1&2)	Surge Voltage (V_{PK})	Waveform (µs)	Surge Current (per Conductor) (A)	Repetitions Each Polarity	Test Connections (Table 3.4)
1	±600	10x1000	100	25	A
2 (note 3)	±1000	10x360	100	25	A
3 (note 3)	±1000	10x1000	100	25	A
4	±2500	2x10	500	10	B
5	±1000	10x360	25	5	(note 4)

Notes:
1. Primary protectors are removed for all tests.
2. For EUT containing secondary voltage limiting and current limiting protectors, tests are to be performed at the indicated voltage(s) and repeated at a reduced voltage and current just below the operating threshold of the secondary protectors.
3. Test 1 and 2 can be replaced with Test 3 or vice versa.
4. This test is to be performed on up to 24 conductors simultaneously with respect to ground.

If during test 3 (or alternatively Test 1), the EUT conducted current exceeds 95A OR the voltage measured across the EUT port exceeds 95% of the voltage-limiting value of the primary protector, then no further coordination tests are required for Type 1, 3, and 5 ports. By using the Littelfuse TeleLink fuse and SIDACtor® technology (C, D, or E rated) or Greentube™ gas plasma arresters in combination, this 95A threshold should easily be reached and thus GR-1089 testing is greatly simplified. Otherwise, a coordination test sequence is required.

Table 3.7: Protection Coordination Lightning Surge Test

Peack Voltage V	Peack Current A	Waveform µs	Repetitions
400–2000	100 A at 1 kV	10x1000	10

Refer to the equipment supplier documentation for specifications on the primary protection with which the equipment is designed to coordinate. The maximum switching voltage threshold value for this primary protector must comply with GR 974 (1 kV for a 1 kV/µs event). This coordination test procedure requires that the peak voltage of this test start at the primary protector's specified voltage-limiting value. This value must be a minimum of 400 V and a maximum of 1000 V. The primary protector must effectively turn on during each of these conditions

Second Level Lightning Surge Test

The Second Level Lightning Surge Test presented in table 3.8 does not require the EUT to pass operationally, but GR 1089 does require that the EUT not become a fire, fragmentation or electrical safety hazard. This is referred to as passing "non-operationally."

Table 3.8: Second Level Lightning Surge Test

Test	Surge Voltage (V_{PK})	Waveform (µs)	Surge Current (A)	Repetitions Each Polarity	Test Connections
1	±5000	2x10	500	1	B

Notes:
1. Primary protectors are removed for all tests.
2. For EUT containing secondary voltage limiting and current limiting protectors, tests are to be performed at the indicated voltage(s) and repeated at a reduced voltage and current just below the operating threshold of the secondary protectors.

Regulatory Requirements (continued)

First Level Intra-building surges

Intra-building tests are not required for:

1. Intra-building wiring connecting equipment separated by a distance of 6 m or less within the same frame or cabinet
2. Intra-building wiring that is not grounded and has no power ports
3. Intra-building wiring used exclusively for maintenance purpose

There are two separate intra-building surge setups, one for ports having 2 ports or less (Table 3.9), and another one for ports having more than 2 ports (four conductors, Table 3.10).

Table 3.9: Intra-building lightning surge test for 2-wire interfaces

Test	Surge Voltage (V_{PK})	Waveform (µs)	Surge Current (per Conductor) (A)	Repetitions Each Polarity	Test Connections
1	±800	2x10	100	1	A1, A2
2	±1500	2x10	100	1	B

Notes:
1. For EUT containing secondary voltage limiting and current limiting protectors, tests are to be performed at the indicated voltage(s) and repeated at a reduced voltage and current just below the operating threshold of the secondary protectors.
2. Surge test 1 is not applicable to Ethernet ports IF the port does not contain secondary protection referenced to ground and all unused pins of the port are not grounded.

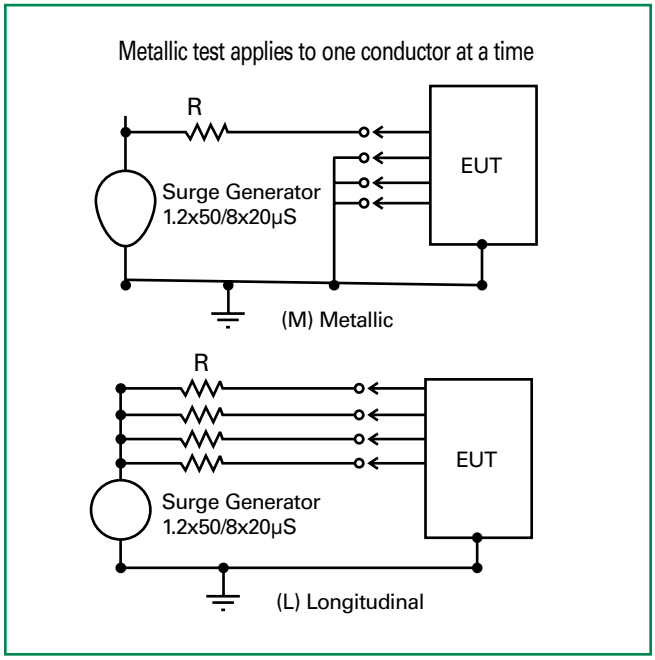
Intra-building lightning surge tests for ports with more than two pairs (four conductors) take into account the dividing factor of multiple wires in parallel. See Table 3.10 and Figure 3.2.

Table 3.10: First Level Intra-building Lightning Surge Test for EUT with greater than 2 pairs (four conductors)

Test	Surge Voltage (V_{PK})	Number of Pairs	Value of external R (ohm)	Repetitions Each Polarity	Test Connections
1	±800	3 or 4	6	1	See Figure 3.2 (M)
2	±1500	3 or 4	20	1	See Figure 3.2 (L)
1	±800	> than 4	6	1	See Figure 3.2 (M)
2	±1500	> than 4	20	1	See Figure 3.2 (L)

Notes:
1. For EUT containing secondary voltage limiting and current limiting protectors, tests are to be performed at the indicated voltage(s) and repeated at a reduced voltage and current just below the operating threshold of the secondary protectors.
2. The combination wave 1.2x50/8x20 waveshape with a 2-ohm internal impedance generator as defined in IEEE C62.41.2 shall be used.

Figure 3.2: Surge Generator Setup



Regulatory Requirements (continued)

AC Power Fault Tests

Power companies and telephone operating companies often share telephone poles and trenches; therefore, network equipment is often subjected to the voltages seen on power lines. If direct contact between the telephone line and the primary power line occurs, the operating company's network equipment may see as much as 600 V rms for five seconds, by which time the power company's power system should clear itself. If direct contact occurs with the secondary power line, voltages will be limited to 277 V rms; however, these voltages may be seen indefinitely because the resultant current may be within the operating range of the power system and the power system will not reset itself.

Another risk involved with power lines is indirect contact. Because of the large magnetic fields created by the currents in the power lines, large voltages may be induced upon phone lines via electro-magnetic coupling. In this instance voltages should be limited to 1000 V peak and 600 V rms using primary protectors, while the current will be limited by the current-carrying capacity of the 24-gauge wire.

First Level AC Power Fault Criteria

Table 3.11 presents test conditions for the First Level AC Power Fault Test. The EUT is required to pass operationally.

Table 3.11: First Level Power Fault

Test	Applied Voltage, 60 Hz (V_{RMS})	Short Circuit Current per Conductor (A)	Duration	Primary Protectors	Test Connections
1 (Note 1)	50	0.33	15 min	Removed	A
2 (Note 1)	100	0.17	15 min	Removed	A
3 (Note 1)	200, 400, 600	1A at 600V	60 applications, 1s each	Removed	A
4 (Note 4)	1000	1	60 applications, 1s each	In place	B
5 (Note 2)	N/A	N/A	60 applications, 5s each	Removed	N/A
6 (Note 3)	600	0.5	30 s	Removed	A
7 (Note 3)	440	2.2	2 s	Removed	A
8 (Note 3)	600	3	1.1 s	Removed	A
9 (Note 3)	1000	5	0.4 s	In place	B

Notes:
1. For EUT containing secondary voltage limiting and current limiting protectors, tests are to be performed at the indicated voltage(s) and repeated at a reduced voltage and current just below the operating threshold of the secondary protectors.
2. Test 5 simulates a high impedance induction fault. For specific information, contact Littelfuse, Inc.
3. Sufficient time may be allowed between applications to preclude thermal accumulation.
4. This test is intended to establish compatibility of the EUT with the primary protector. The maximum current is limited to 1 A rms as in Test 3, but the voltage is increased to 1,000 V to permit operation of the protector. Sufficient time may be allowed between applications to preclude thermal accumulation.

Second Level AC Power Fault Criteria

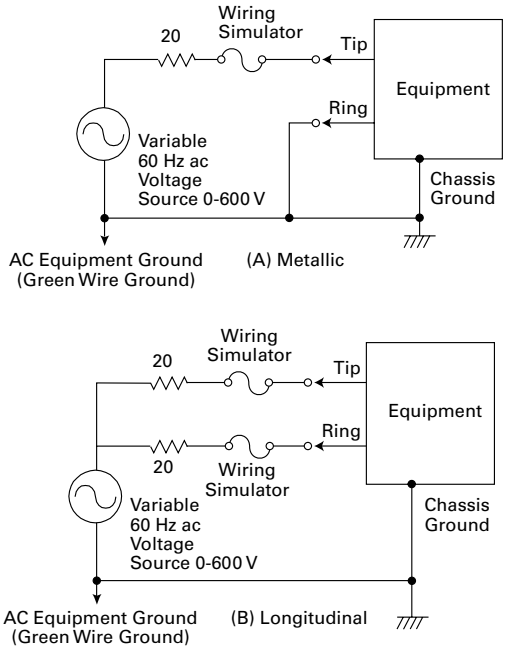
Table 3.12 below presents test conditions for both customer premises and non-customer premises equipment. (Note that test conditions 1, 3, and 4 may be omitted if the EUT has previously met UL 60950-1.)

Table 3.12: Second Level AC Power Fault Test (and Intra-building 2nd level)

Test (Notes 1, 2)	Applied Voltage, 60 Hz (V_{RMS})	Short Circuit Current per Conductor (A) (Note 4)	Duration	Test Connections
1 (Note 5)	120, 277	25	15 min	A
2	600	60	5 s	A
3	600	7	5 s	A
4	600	2.2A at 600 V	15 min	A
5 (Note 3)	N/A	N/A	15 min	N/A

Notes:
1. Primary protectors are removed for all tests.
2. For EUT containing secondary voltage limiting and current limiting protectors, tests are to be performed at the indicated voltage(s) and repeated at a reduced voltage and current just below the operating threshold of the secondary protectors.
3. Test 5 simulates a high impedance induction fault. Specific information regarding this test is available upon request.
4. These tests are repeated using a short-circuit value just below the operating threshold of the current limiting device, or, if the EUT uses a fuse as current limiting protection, the fuse may be bypassed and the short circuit current available adjusted to 135 percent of the fuse rating.
5. Intra-building, second level power fault test uses test condition 1 only. The applied voltage is at 120 V rms only.

Figure 3.3: Second Level AC Power Fault and Current Limiter Connection



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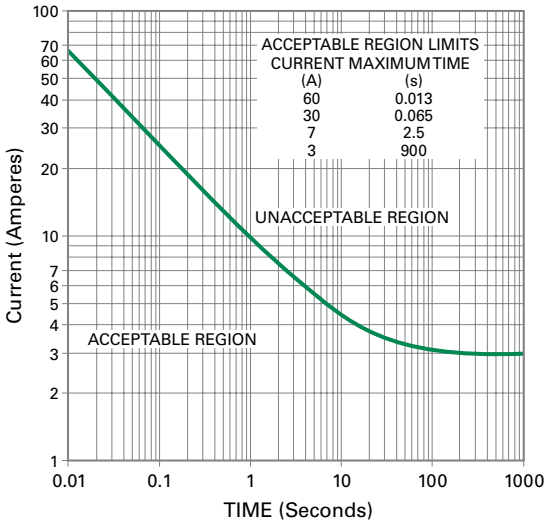
Regulatory Requirements (continued)

Current Limiting Protector Test

The purpose of the Current Limiting Protector Test is to determine if the EUT allows an excessive amount of current flow under power fault conditions. During this test, the EUT is connected to a circuit equivalent to that shown in Figure 3.3 above with a 1.6 A Type MDQ fuse or MDL 2.0A fuse as the wiring simulator. If the EUT draws enough current to open the fuse, then the acceptable time/current criteria have not been met, and external current limiting protectors must be specified for use with that quipment in the manufacturer's documentation. This test is conducted at 2.2 A, 2.6 A ,3 A, 3.75 A, 5 A, 7 A, 10 A, 12.5 A, 20 A, 25 A, and 30 A for 15 minutes at each subsequent value until the equipment interrupts the current or reduces it to less than 50 mA. IF the wiring simulator opens, the EUT does not meet the criteria.

Figure 3.4: Time-current characteristics of the external current-limiter indicator.



Short-circuit Test

In addition to the AC Power Fault and Current Limiter Tests, equipment must also pass a Short-circuit Test to comply with GR 1089. During this test, a short-circuit condition is applied to the following Tip and Ring appearances for 30 minutes while the EUT is powered and under operating conditions:

- Tip-to-Ring, Tip-to-Ground with Ring open circuit
- Ring-to-Ground with Tip open circuit
- Tip- and Ring-to-Ground simultaneously for 30 minutes

At no time will the short circuit impedance exceed 1-ohm. For equipment with more than one twisted pair, the short circuit is applied to all twisted pair simultaneously. To comply with the short circuit test, the EUT must function normally after the short-circuit condition is removed, and a fire or electrical safety hazard may not be present. The equipment shall not require manual intervention to restore service.

Lightning Protection tests for Equipment located in high exposure locations (Port Type 3 & 5)

The surge generator for high exposure risk environments shall be capable of delivering 4kV into an open circuit and capable of delivering 500A into a short circuit, with a 10x250 µS waveshape. The switching voltage of the primary protector must first be determined before applying this 10x250 surge to the EUT OR the EUT must have a surge withstand capability adequate to survive these severe events. For a EUT that is preceded by a 3 mil carbon block, which is typically a worse case scenario, the maximum let-through voltage this carbon block allows would be 1 kV. Under these conditions, the EUT would see a 1 kV open circuit voltage and 125A short circuit surge event. Some primary protectors contain series elements that would further reduce the current delivered into the EUT. Therefore, the primary protector characteristics must be determined before this high exposure test is conducted. Once it surge characteristics are determined, then this 10x250 surge event is applied ±10 at the allowed let-through voltage and current levels.

Criteria for Equipment containing agreed primary protectors

This generic requirements document contains a section for customer premises and non-CO type facilities equipment that are protected by a known defined primary protector other than 3-mil blocks. This section contains four different categories for agreed primary protection. The categorization will then reduce the open circuit voltage used for lightning and power fault testing as previously defined in first and second level lightning and ac power fault tables. Please see Littelfuse for more details on this section.

Criteria for Equipment with Integrated Primary Protectors (EIPP)

This GR also contains a section for equipment that has integrated primary protection on the ports with direct connections to the OSP. Please contact Littelfuse, Inc. for more details on this section.

Lightning surge Tests for Severe Climatic Conditions

For Type 3 and 4 ports that interface with 8 or fewer OSP conductors, a more severe lightning surge event is applied. See Table 3.13 below.

Table 3.13: Severe Climatic Surge Test

Surge Level	Surge Voltage (V_{PK})	Current Waveshape (µs)	Surge Current per Conductor (A)	Repetitions Each Polarity	Test Connections
1st	±3000	10x250	2000	1	T to R; single pair only
2nd	±5000	8x20	20000	1	T to R; single pair only

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Regulatory Requirements (continued)

Criteria for Equipment Interfacing with coaxial cable ports

Table 3.14: First Level Lightning Surge Test for Broadband Equipment over coaxial cable

Test	Surge Voltage (V_{PK})	Waveshape (µs)	Surge Current per Conductor (A)	Repetitions Each Polarity
1	±1000	10x1000	100	25
2	±2000	10x250	1000	5

Note:
1. For EUT containing secondary voltage limiting and current limiting protectors, tests are to be performed at the indicated voltages and 2 is to be repeated at a reduced voltage and current just below the operating threshold of the secondary protectors.

Table 3.15: Second Level Lightning Surge Test for Broadband Equipment over coaxial cable

Test	Surge Voltage (V_{PK})	Waveshape (µs)	Surge Current per Conductor (A)	Repetitions Each Polarity
1	±4000	10x250	2000	1

Note:
1. For EUT containing secondary voltage limiting and current limiting protectors, tests are to be performed at the indicated voltages and then repeated at a reduced voltage and current just below the operating threshold of the secondary protectors.

Table 3.16: First Level AC Power Fault Test for Broadband Equipment over coaxial cable

Test	Voltage (50 or 60 Hz)	Current (A_{RMS})	Duration (S)	Repetitions
1	600 V_{RMS}	40	1	1
2	600 V_{RMS}	10	1	5
3	600 V_{RMS}	1	1	60
4	600 V_{RMS}	0.5	30	1

Notes:
1. For EUT containing secondary voltage limiting and current limiting protectors, tests are to be performed at the indicated voltages and then repeated at a reduced voltage and current just below the operating threshold of the secondary protectors.
2. For EUT containing an external protector, only Text 3 & 4 are conducted. The voltage is lowered to 400V and the repetitions for test 3 is reduced to one.

Table 3.17: Second Level AC Power Fault Test for Broadband Equipment over coaxial cable

Test	Voltage (50 or 60 Hz)	Current (A_{RMS})	Duration (minutes)	Repetitions
1	1000 V_{RMS}	5	15	1
2	1000 V_{RMS}	15	15	1
3	1000 V_{RMS}	30	15	1
4	1000 V_{RMS}	60	15	1
5	1000 V_{RMS}	120	15	1
6	1000 V_{RMS}	350	3	1

Notes:
1. For EUT containing secondary voltage limiting and current limiting protectors, tests are to be performed at the indicated voltages and then repeated at a reduced voltage and current just below the operating threshold of the secondary protectors.
2. For EUT containing an external protector, the voltage is lowered to 400V_{RMS}.

First Level Intra-building surge tests for coaxial ports

This test applies to both grounded and ungrounded coaxial ports. The 1.2x50/8x20 surge generator with a 2-ohm internal impedance (as defined in IEEE C62.41.2) will be connected through an external non-inductive 3-ohm resistor to the EUT. The open circuit voltage shall be 1500 V. This surge shall be applied one time in each polarity.

Table 3.18: Lightning criteria for equipment interfacing with antennas [1st Level Lightning Surge Test (Antenna Ports)]

Test	Surge Voltage (V_{PK})	Voltage Waveshape (µs)	Surge Current (A)	Current Waveshape	Repetitions Each Polarity
1	±600	1.2x50	300	8x20	5

Note:
1. For EUT containing secondary voltage limiting and current limiting protectors, tests are to be performed at the indicated voltage and repeated at a reduced voltage and current just below the operating threshold of the secondary protectors.

Table 3.19: Lightning criteria for AC power ports [First Level Lightning Surge (Power ports)]

Test	Surge Voltage (V_{PK})	Voltage Waveshape (µs)	Surge Current (A)	Current Waveshape	Repetitions Each Polarity
1	±2000	1.2x50	1000	8x20	4

Note:
1. For EUT without an external SPD, the surge voltage is increased to 6000V and the surge current to 3000A.

Table 3.20: Second Level Lightning Surge (Power ports)

Test	Surge Voltage (V_{PK})	Voltage Waveshape (µs)	Surge Current (A)	Current Waveshape	Repetitions Each Polarity
1	±6000	1.2x50	3000	8x20	1

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Regulatory Requirements (continued)

First Level Lightning surges for DC power ports

Five repetitions of each polarity of the 0.5 µS 100 kHz ring wave surge with a peak voltage of 0.5 kV and a current level of 41.7A per conductor shall be applied. The IEEE C62.41.2 combination wave 1.2x50/8x20 at a peak of 500V applied through an external non-inductive resistance of 10-ohms may be substituted for this ring wave. These surges are to be applied simultaneously between

1) the supply lead and ground
2) the return lead and ground

Criteria for DC Power Port

This section applies to the equipment that is powered from a shared dc power plant. It is based on T1.315-2001 Voltage Levels for DC-Powered Equipment Used in Telecommunications Environments. This section contains criteria for:

- minimum operating voltages,
- under voltage transients,
- over voltage transients,
- impulse transients,
- single transient, and
- noise related issues

Table 3.21: Undervoltage Transient test conditions

Waveform	Nominal-value	Tolerance
Undervoltage transient Level	-5 V	-4 to -5 V
Fall-time	10µS	0 to 12 µS
Transient duration	10 mS	10 to 12 mS
Rise-time	< 5 µS	0 to 5 µS

Table 3.22: Overvoltage Transient test conditions

Waveform	Nominal-value	Tolerance
Overvoltage transient Level	-75 V	-75 to -95 V
Slope	10 V/mS	9 to 11 V/mS
Transient duration	10 mS	10 to 12 mS
Rise-time	< 2 µS	0 to 2 µS

Table 3.23: Impulse Transient test conditions

Waveform	Nominal-value	Tolerance
Overvoltage transient Level	-100 V	-100 to -120 V
Rise-time	< 2 µS	0 to 2 µS
Fall-time to half value	50 µS	28 to 60 µS

Table 3.24: Equipment Port Types

Type 1	Network equipment connected to the outside plant (OSP)
Type 2	Network equipment not connected to the OSP.
Type 3	Customer premises equipment connected to the OSP.
Type 4	Customer premises equipment not connected to the OSP.
Type 5	Network equipment deployed in OSP & connected to the outside plant (OSP)
Type 6	Equipment directly connected to external antennas
Type 7	Equipment directly connected to ac power systems
Type 8	Equipment directly connected to dc power systems

Regulatory Requirements (continued)

Although the International Telecommunication Union (ITU) does not have the authority to legislate that organizations follow their recommendations, their standards are recognized throughout Europe and the Far East.

ITU-T, the Telecommunication Standardization Sector of the ITU, developed fundamental testing methods that cover various environmental conditions to help predict the survivability of network and customer-based switching equipment. The testing methods cover the following conditions:

- Surges due to lightning strikes on or near twisted pair and plant equipment (excluding a direct strike)
- Short-term induction of AC voltage from adjacent power lines or railway systems
- Direct contact between telecommunication lines and power lines (often referred to as AC power fault)

Two ITU-T standards apply for most telecommunications equipment connected to the network:

- ITU-T K.20
- ITU-T K.21

ITU-T K.20 is primarily for switching equipment powered by the central office; however, for complex subscriber equipment, test administrators may choose either K.20 or K.21, depending on which is deemed most appropriate.

Note : Both specifications are intended to address equipment reliability versus equipment safety. For specific concerns regarding equipment safety, research and follow national standards for each country in which the equipment is intended for use.

K.21 covers telecommunication equipment installed at customer premises. Equipment submitted under these requirements must meet one of two levels: basic or enhanced. Guidelines for determining under which level the equipment under test (EUT) falls can be found in ITU-T K.11, but note that the final authority rests with the test administrator. ITU-T K.44 describes the test conditions used in K.20 and K.21.

ITU-T defines the following acceptance criteria:

- **Criterion A** states that equipment shall withstand the test without damage and shall operate properly after the test. It is not required to operate correctly during the test.
- **Criterion B** states that a fire hazard shall not occur as a result of the tests. Any damage shall be confined to a small part of the equipment.

Table 3.25 shows the lightning surge test conditions for ITU K.20. Figure 3.5 shows the connection schematic for the lightning surge tests. Table 3.26 shows the power fault test conditions for ITU K.20. Figure 3.6 shows the connection schematic for the power fault tests. Table 3.27 and Table 3.28 show the same test conditions respectively for ITU K.21.

Table 3.25 K.20 Lightning Test Conditions for Telecom Equipment in Central Office/Remote Terminal

Voltage (10x700 µs)		Current (5x310 µs) Basic/Enhanced (A)	Repetitions *	Primary Protection	Acceptance Criteria
Single Port Metallic and Longitudinal Basic/Enhanced	Multiple Ports Longitudinal Only Basic/Enhanced				
1 kV/1.5 kV		25/37.5	±5	None **	A
4 kV/4 kV		100/100	±5	Installed if used	A
	1.5 kV/1.5 kV	37.5/37.5	±5	None	A
	4 kV/6 kV	100/150	±5	Installed if used	A

* One-minute rest between repetitions ** Test not conducted if primary protection is used

Table 3.26 K.20 Power Fault Test Conditions for Telecom Type Ports, Metallic, and Longitudinal

Voltage Basic/Enhanced	Current Basic/Enhanced (A)	Duration Basic/Enhanced	Repetitions *	Primary Protection	Acceptance Criteria Basic/Enhanced
600 V/600 V 50 Hz or 60 Hz	1/1	0.2 s	5	None	A/A
600/1.5 kV 50 Hz or 60 Hz	1/7.5	1 s/2 s	5	None	A/A
230/230 V -- 50 Hz or 60 Hz	23/23	15 min	1	None	B/B
	11.5/11.5				B/B
	5.75/5.75				B/B
	2.875/2.875				B/B
	1.44/1.44				B/A
	0.77/0.77				B/A
	0.38/0.38				B/A
	0.23/0.23				B/B

* One-minute rest between repetitions

Regulatory Requirements (continued)

Table 3.27 K.21 Lightning Test Conditions for Telecom Equipment on Customer Premises

Voltage (10x700 µs)			Current (5x310 µs) Basic/Enhanced (A)	Repetitions *	Primary Protection	Acceptance Criteria
Single Port		Multiple Ports Longitudinal Only (kV) Basic/Enhanced				
Longitudinal (kV) Basic/Enhanced	Metallic (kV) Basic/Enhanced					
1.5/6 **			37.5/150	±5	None	A ***
4/6			100/150	±5	Installed if used	A
	1.5/1.5	1.5/1.5	37.5/37.5	±5	None	A ***
	4/6	4/6	100/150	±5	Installed if used	A

* One-minute rest between repetitions ** Reduce to 1.5 kV if SPD connects to Ground *** Does not apply if primary protectors are used

Table 3.28 K.21 Power Fault Test Conditions for Telecom Type Ports, Metallic, and Longitudinal

Voltage Basic/Enhanced	Current Basic/Enhanced (A)	Duration Basic/Enhanced	Repetitions *	Primary Protection	Acceptance Criteria Basic/Enhanced
600 V / 600 V 50 Hz or 60 Hz	1/1	0.2 s	5	None	A/A
600/1.5 kV 50 Hz or 60 Hz	1/7.5	1 s/2 s	5	Installed if used	A/A
230 V / 230 V 50 Hz or 60 Hz	23/23	15 min	1	None	B/B
	11.5/11.5				B/B
	5.75/5.75				B/B
	2.875/2.875				B/B
	1.44/1.44				B/A
	0.77/0.77				B/A
	0.38/0.38				B/A
	0.23/0.23				B/B

* One-minute rest between repetitions

Figure 3.5 Connection Appearances

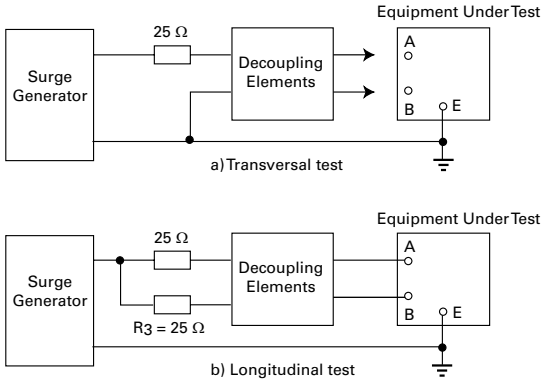
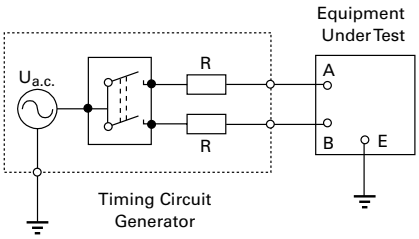
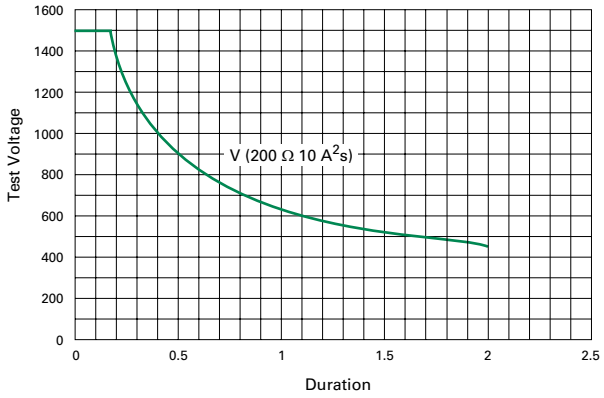


Figure 3.6 Connection Appearances (R = 10 Ω, 20 Ω, 40 Ω, 80 Ω, 160 Ω, 300 Ω, 600 Ω, and 1000 Ω for the various power fault tests)



Enhanced power fault test condition of 1.5 kV 200 W 2 second test must meet the time current curve shown in Figure 3.7.

Figure 3.7 Test Voltage Versus Duration for Specific Energy / Source Resistance



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Regulatory Requirements (continued)

TIA-968-A (formerly known as FCC Part 68)

TIA-968-A applies to all terminal equipment connected to the Public Switched Telephone Network (PSTN) in the USA, and holds the "rule of law" by congressional order.

The purpose of TIA-968-A is to provide a set of uniform standards to protect the telephone network from any damage or interference caused by the connection of terminal equipment. This standard includes environmental simulations such as vibration tests, temperature and humidity cycling, drop tests and tests for hazardous voltages and currents, as well as tests for signal power levels, line balance, on-hook impedance, and billing protection. All these standards must be met before and after the environmental tests are applied.

Overvoltage Test

TIA-968-A compliant equipment must undergo an overvoltage test that includes a Type A and Type B Metallic Voltage Surge and a Type A and Type B Longitudinal Voltage Surge. These surges are part of the environmental simulation, and although a provision does allow the EUT to reach an open circuit failure mode during the Type A tests, failures must:

1. Arise from an intentional design that will cause the phone to be either disconnected from the public network or repaired rapidly
2. Be designed so that it is substantially apparent to the end user that the terminal equipment is not operable [A common example of an acceptable failure would be an open circuit due to an open connection on either Tip or Ring.]

For Type B surges, equipment protection circuitry is not allowed to fail. The EUT must be designed to withstand Type B surges and continue to function in all operational states.

Metallic Voltage Surge

The Type A and Type B Metallic Voltage Surges are applied in both the positive and negative polarity across Tip and Ring during all operational states (on-hook, off-hook, ringing, and so on). The Type A surge is an 800 V, 100 A peak surge while the Type B surge is a 1000 V, 25 A peak surge, as presented in Table 3.29.

Table 3.29 TIA-968-A Voltage Surge

Surge Type	Peak Voltage (V_{PK})	Rise & Decay Time (Voltage Waveform)	Peak Current (A)	Rise & Decay Time (Current Waveform)	Repetitions Each Polarity
Metallic A	±800	10x560 µs	100	10x560 µs	1
Longitudinal A	±1500	10x160 µs	200	10x160 µs	1
Metallic B	±1000	9x720 µs	25	5x320 µs	1
Longitudinal B	±1500	9x720 µs	37.5	5x320 µs	1

Notes:
- For Type A surges, the EUT may pass either "operationally" or "non-operationally."
- For Type B surges, the EUT must pass "operationally."
- The peak current for the Type A longitudinal surge is the total available current from the surge generator.
- The peak current for the Type B longitudinal surge is the current supplied to each conductor.

Longitudinal Voltage Surge

The Type A and Type B Longitudinal Voltage Surges are applied in both positive and negative polarity during all operational states. The Type A surge is a 1500 V, 200 A peak surge applied to the EUT with Tip and Ring tied together with respect to Ground. The Type B Longitudinal Voltage Surge is a simultaneous surge in which 1500 V and 37.5 A are applied concurrently to Tip with respect to Ground and Ring with respect to Ground, as presented in Table 3.29.

Note : Type B surge requirements guarantee only a minimum level of surge protection. For long term reliability of terminal equipment, consideration should be given to complying with Type A surges operationally.

On-hook Impedance Limitations

Another important aspect of TIA-968-A is on-hook impedance, which is affected by transient protection. On-hook impedance is analogous to the leakage current between Tip and Ring, and Tip, Ring, and Ground conductors during various on-hook conditions. "On-hook Impedance Measurements" (next paragraph) outlines criteria for on-hook impedance and is listed as part of the Ringer Equivalent Number (REN). The REN is the largest of the unitless quotients not greater than five; the rating is specified as the actual quotient followed by the letter of the ringer classification (for example, 2B).

On-hook Impedance Measurements

On-hook impedance measurements are made between Tip and Ring and between Tip and Ground and Ring and Ground. For all DC voltages up to and including 100 V, the DC resistance measured must be greater than 5 MΩ. For all DC voltages between 100 V and 200 V, the DC resistance must be greater than 30 kΩ. The REN values are then determined by dividing 25 MΩ by the minimum measured resistance up to 100 V and by dividing 150 kΩ by the minimum measured resistance between 100V and 200V.

On-hook impedance is also measured during the application of a simulated ringing signal. This consists of a 40 V rms through 150 V rms ringer signal at frequencies ranging from 15.3 Hz to 68 Hz superimposed on a 56.5 V dc for a class "B" ringer. During this test, the total DC current may not exceed 3 mA. In addition, the minimum DC resistance measured between Tip and Ring must be greater than 1600Ω, while the DC resistance measured between the Tip and Ring conductors and Ground must be greater than 100 kΩ. The REN values for the simulated ringing test are determined by dividing the maximum DC current flowing between Tip and Ring by 0.6 mA, and by dividing 8000 Ω by the minimum impedance value measured.

Regulatory Requirements (continued)

TIA-968-A applies to all terminal equipment connected to the Public Switched Telephone Network (PSTN) in the USA, and holds the "rule of law" by congressional order.

The purpose of TIA-968-B is to provide a set of uniform standards to protect the telephone network from any damage or interference caused by the connection of terminal equipment. This standard includes environmental simulations such as vibration tests, temperature and humidity cycling, drop tests and tests for hazardous voltages and currents, as well as tests for signal power levels, line balance, on-hook impedance, and billing protection. All these standards must be met before and after the environmental tests are applied.

Overvoltage Test

TIA-968-B compliant equipment must undergo an overvoltage test that includes a Type A and Type B Metallic Voltage Surge and a Type A and Type B Longitudinal Voltage Surge. These surges are part of the environmental simulation, and although a provision does allow the EUT to reach an open circuit failure mode during the Type A tests, failures must:

1. Arise from an intentional design that will cause the phone to be either disconnected from the public network or repaired rapidly
2. Be designed so that it is substantially apparent to the end user that the terminal equipment is not operable [A common example of an acceptable failure would be an open circuit due to an open connection on either Tip or Ring.]

For Type B surges, equipment protection circuitry is not allowed to fail. The EUT must be designed to withstand Type B surges and continue to function in all operational states.

Metallic Voltage Surge

The Type A and Type B Metallic Voltage Surges are applied in both the positive and negative polarity across Tip and Ring during all operational states (on-hook, off-hook, ringing, and so on). The Type A metallic surge can be as high as 880 V, 115A peak surge while the Type B metallic surge can be as high as 1100 V, 27.5 A peak surge, as presented in Table 3.29.

The repetition rate contained in TIA-968-B is ± 1 for each surge event. However, the companion test document TSB-31-D (Rationale and Measurement Guidelines for U.S. Network Protection)cites TIA-571-B (Electrical, Thermal, Mechanical Environmental Performance Requirements), which requires ± 4 surges for each Type A surge event and ± 8 surges for each Type B surge event. It also requires incremental testing from 100 V to the maximum output level in 100 V increments for Type A surges. Therefore, engineering consideration should be made for surge repetition rates greater than those specifically stated in TIA-968-B.

Table 3.29 TIA-968-B Voltage Surge

Surge Type	Peak Voltage volts	Rise/Decay time µs	Peak current amps	Rise/Decay time µs	Reps
Metallic A	800 - 880	6-10/560-860	100 - 115	5-10/560-760	±1
Longitudinal A	1500 - 1650	6-10 /160-260	200 - 230	5-10/160-210	±1
Metallic B	1000 - 1100	9±2.7/720±144	25 - 27.5	5±1.5/320±64	±1
Longitudinal B	1500 - 1650	9±2.7/720±144	37.5 – 41.3	5±1.5/320±64	±1

Notes:
- For Type A surges, the EUT may pass either "operationally" or "non-operationally."
- For Type B surges, the EUT must pass "operationally."
- The peak current for the Type A longitudinal surge is the total available current from the surge generator.
- The peak current for the Type B longitudinal surge is the current supplied to each conductor.

Longitudinal Voltage Surge

The Type A and Type B Longitudinal Voltage Surges are applied in both positive and negative polarity during all operational states. "The Type A longitudinal surge can be as high as 1650 V, 230A peak surge while the Type B longitudinal surge can be as high as 1650 V, 41.3 A peak surge, as presented in Table 3.29. This longitudinal surge is applied to the EUT with tip and ring connected together and surged with respect to ground.

The repetition rate contained in TIA-968-B is ± 1 for each surge event. However, the companion test document TSB-31-D (Rationale and Measurement Guidelines for U.S. Network Protection)cites TIA-571-B (Electrical, Thermal, Mechanical Environmental Performance Requirements), which requires ± 4 surges for each Type A surge event and ± 8 surges for each Type B surge event. It also requires incremental testing from 100 V to the maximum output level in 100 V increments for Type A surges. Therefore, engineering consideration should be made for surge repetition rates greater than those specifically stated in TIA-968-B.

Note : Type B surge requirements guarantee only a minimum level of surge protection. For long term reliability of terminal equipment, consideration should be given to complying with Type A surges operationally.

Regulatory Requirements (continued)

On-hook Impedance Limitations

Another important aspect of TIA-968-B is on-hook impedance, which is affected by transient protection. On-hook impedance is analogous to the leakage current between tip to ring, tip to ground, and ring to ground during various on-hook conditions. "On-hook Impedance Measurements" (next paragraph) outlines criteria for on-hook impedance and is listed as part of the Ringer Equivalent Number (REN). The REN is the largest of the unitless quotients not greater than five; the rating is specified as the actual quotient followed by the letter of the ringer classification (for example, 2B).

On-hook Impedance Measurements

On-hook impedance measurements are made between tip to ring, tip to ground, and ring to ground. For all DC voltages up to and including 100 V, the DC resistance measured must be greater than 5 MΩ. For all DC voltages between 100 V and 200 V, the DC resistance must be greater than 30 kΩ. The REN values are then determined by dividing 25 MΩ by the minimum measured resistance up to 100 V and by dividing 150 kΩ by the minimum measured resistance between 100V and 200V.

On-hook impedance is also measured during the application of a simulated ringing signal. This consists of a 40 V rms through 150 V rms ringer signal at frequencies ranging from 15.3 Hz to 68 Hz superimposed on a 56.5 V dc for a class "B" ringer. During this test, the total DC current may not exceed 3 mA. In addition, the minimum DC resistance measured between tip to ring must be greater than 1600Ω, while the DC resistance measured between the Tip and Ring conductors and Ground must be greater than 100 kΩ. The REN values for the simulated ringing test are determined by dividing the maximum DC current flowing between tip to ring by 0.6 mA, and by dividing 8000 Ω by the minimum impedance value measured.

IEC 61000-4-2, 4-4 and 4-5 Summary

Part 1: Introduction, definitions, & terminology

Part 2: Description & classification of the environment

Part 3: Emission & immunity limits

Part 4: Testing & measurement techniques

Part 5: Installation & mitigation guidelines

A summary of Part 4 from IEC 61000-4-2, 61000-4-4, & 61000-4-5 follows.

IEC 61000-4-2 Testing and measurement techniques – Electrostatic Discharge (ESD) Immunity test

This standard defines test procedures to evaluate equipment ESD resistibility performance.

Figure 3.8 ESD generator schematic

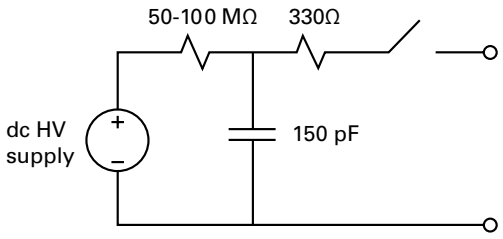


Table 3.30 Test Levels

Level	Contact discharge	Air discharge
	Voltage	
1	2 kV	2 kV
2	4 kV	4 kV
3	6 kV	8 kV
4	8 kV	15 kV
X	Special	Special

"x" is an open level, to be specified in dedicated equipment specification

Table 3.31 Test waveform values

Level	Voltage	Initial current peak value	Rise time	Current at 30 nS	Current at 60 nS
1	2 kV	7.5A	0.7 to 1	4 A	2A
2	4 kV	15 A		8A	4A
3	6 kV	22.5A		12A	6A
4	8 kV	30A		16A	8A

Table 3.32 Guidelines for test level selection

Class	Relative Humidity as low as	Anti-static material	Synthetic material	Maximum voltage
1	35%	*		2 kV
2	10%	*		4 kV
3	50%		*	8 kV
4	10%		*	15 kV

The test level chosen for a particular application should consider its installation and environmental conditions.

Regulatory Requirements (continued)

IEC 61000-4-4 Testing and measurement techniques – Electrical fast transient (EFT) Immunity test

This standard defines test procedures to evaluate equipment EFT resistibility performance.

Table 3.33 Test Levels

Level	Repetition rate kHz	Power Ports kV	I/O ports kV
1	5 or 100	0.5	0.25
2		1	0.5
3		2	1
4		4	2
X		Special	Special

Table 3.34 Test waveform values

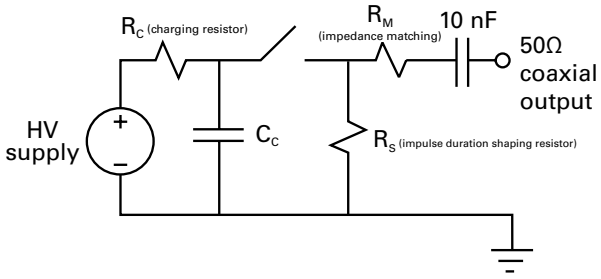
Set voltage	V_P (open circuit)	V_P (1 kΩ)	V_P (50Ω)	Repetition rate
250 V	250 V	240 V	125 V	5 kHz or 100 kHz
500 V	500 V	480 V	250 V	
1 kV	1 kV	950 V	500 V	
2 kV	2 kV	1.9 kV	1 kV	
4 kV	4 kV	3.8 kV	2 kV	

Burst duration 15 mS ± 20% at 5 kHz, 0.75 mS ± 20% at 100 kHz, burst period 300 mS ± 20%; 5 nS ± 30% rise time, 50 nS ± 30% decay to half value time

Table 3.35 Guidelines for test level selection

Level	Environment	Description
1	Well-protected	Shielded power cables, suppression of all EFT in power supply & control circuits, proper separation of application from other environments
2	Adequately-protected	Physical separation of unshielded power cables, partial suppression of EFT in power supply & control circuits
3	Industrial	Poor separation between power supply, control, signal & communication cables, no suppression of EFT in power supply & control circuits
4	Severe industrial	No separation between power supply, control, signal & communication cables, no suppression of EFT in power supply & control circuits
5	Special	Special situation that remain to be analyzed

Figure 3.9 EFT generator schematic



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Regulatory Requirements (continued)

IEC 61000-4-5 Testing and measurement techniques – Surge immunity (lightning surge effects) test

This standard defines test procedures to evaluate equipment resistibility to uni-directional surges resulting from electrical switching and nearby lightning strikes. The switching transients are associated with power system switching disturbances, and various system faults. The lightning transients are associated with direct lightning strokes into the common ground of applications, indirect lightning strokes such as cloud to cloud, and nearby lightning strikes.

Two different coupling methods are discussed in this document:

1) capacitive coupling
2) arrestor coupling

Capacitive coupling is the preferred method for unbalanced I/O circuits while arrestor coupling is the preferred coupling method for unshielded balanced circuits (such as telecommunication).

Table 3.36 – Test levels

Level	Description
Class 0	Well-protected environment
Class 1	Partially protected environment
Class 2	Well separated cables
Class 3	Cables run in parallel
Class 4	Multi-wire cables for both electronic & electrical circuits
Class 5	Connection to telecommunications cables and overhead power lines (low density populated areas)
Class x	Special testing as defined in product specification

Figure 3.10 – 1.2/50-8/20 CWG simplified schematic

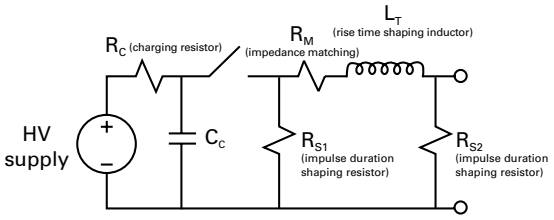

Figure 3.11 – 10/700-5/320 CCITT simplified schematic

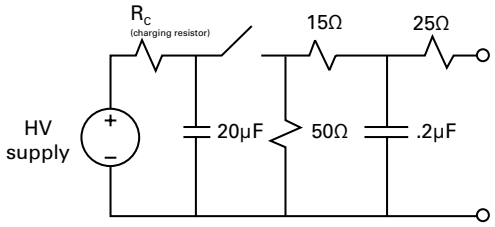

Table 3.37 – Test requirements

Class	Surge definition	Test Levels									
		DC Power supply		Unsymmetrical interface (long distance bus)		Symmetrical interface	Data Bus (short distance)	AC Power Supply connected to Mains		AC Power Supply NOT connected to Mains	
		Differential	Common mode	Differential	Common mode	Common mode	Common mode	Differential	Common mode	Differential	Common mode
		Zs = 2 Ω	Zs = 12 Ω	Zs = 42 Ω	Zs = 42 Ω	Zs = 40 Ω*	Zs = 42 Ω	Zs = 2 Ω	Zs = 12 Ω	Zs = 2 Ω	Zs = 12 Ω
0	Voltage/current	N/A									
	Waveforms µs										
1	Voltage/current	N/A			500 V/ 11.90A	500V/ 12.5A	N/A		500 V/ 11.90A	N/A	
	Waveforms µs	N/A			1.2/50-8/20	10/700-5/320	N/A		1.2/50 - 8/20	N/A	
2	Voltage/current	N/A		500 V/ 11.90A	1kV/ 23.80A	1kV/ 25A	500V/ 11.90A	500A/ 250A	1kV/ 83.33A	N/A	
	Waveforms µs	N/A		1.2/50-8/20		10/700-5/320	1.2/50-8/20			N/A	
3	Voltage/current	1kV/ 500A	2kV/ 166.67A	1kV/ 23.8A	2kV/ 47.6A	2kV/ 50A	2kV/ 47.6A	1kV/ 500A	2kV/ 166.67A	1kV/ 500A	2kV/ 166.67A
	Waveforms µs	1.2/50-8/20				10/700-5/320	1.2/50-8/20				
4/5	Voltage/current	2kV/ 1kA	4kV/ 333.33V	2kV/ 47.6A	4kV/ 95.24A	2kV/ 50A	4kV/ 95.24A	2kV/ 1kA	4kV/ 333.33V	2kV/ 1kA	4kV/ 333.33V
	Waveforms µs	1.2/50-8/20				10/700-5/320	1.2/50-8/20				
x	Voltage/current	Per special conditions in the product specification									
	Waveforms µs										

*Simultaneous surge is applied, so effective Zs = 40 Ω

Regulatory Requirements (continued)

Mainland China Standard - YD/T 950-1998

YD/T 950-1998 establishes the technical requirements and test methods for protection against overvoltages and overcurrents on telecommunication switching equipment for Mainland China.

This Standard is based on the ITU-T Recommendation K.20 "Resistibility of Telecommunication Equipment Installed in a Telecommunications Center for Overvoltages and Overcurrents" (1996 version).

It was approved by the Ministry of Information Industry of the People's Republic of China on August 7, 1998 and has been in effect since September 1, 1998.

Technical Requirements

The following major transmission parameters and interface feature parameters of the equipment should comply with requirements contained in GF 002-9002 or YD 344:

- Transmission loss
- Loss frequency distortion
- Gains changing with input level
- Cross talk
- Scratching noise
- Return loss
- Unbalanced earth impedance

After the following tests are conducted, the equipment should provide normal communications functions and comply with these requirements.

Without primary protection:

1. When the lightning waveform is 10/700 µs and the peak voltage is 1 kV
2. When the induction voltage of the power line is 600 V rms and the duration is 0.2 s

With primary protection:

1. When the lightning waveform is 10/700 µs and the peak voltage is 4 kV
2. When the induction voltage of the power line is 600 V rms and the duration is 1 s

Without primary protection, the equipment should be fireproof when it is in contact with power lines with a voltage of 220 V rms for a duration of 15 minutes and should provide normal communications functions after the test.

After the equipment is tested for contact discharge at an electrostatic voltage of 6 kV or for air discharge at 8 kV, it should provide normal communications functions.

Test Methods

All tests should be conducted in the following standard atmospheric conditions:

- Temperature: 15 °C ~ 35 °C
- Relative humidity: 45% ~ 75%
- Air pressure: 86 ~ 106 kP

Test procedure sequence is as follows:

1. Normal equipment operation
2. Characteristics and parameters
3. Simulation of lightning strike
4. Check of functions
5. Power line induction
6. Check of functions
7. Check of functions
8. ESD
9. Check of functions
10. Power line contact
11. Characteristics and parameters

Power Line Induction

Without primary protection:

600 V, 1 A, 0.2 s applied between Tip and Ring to Ground five times

With primary protection:

600 V, 1 A, 1 s applied between Tip and Ring to Ground five times

Time between successive events shall be one minute. Characteristics and parameters shall be tested within 30 minutes after the completion of these events.

Power Line Contact

Without primary protection:

220 V rms @ 0.367 A, 1.1 A, 22 A for 15 minutes applied between Tip and Ring to Ground one time each

With primary protection:

220 V rms 0.367 A for 15 minutes applied between Tip and Ring to Ground five times

ESD (electrostatic discharge)

±5 repetitions direct contact with one-second duration between successive discharges

±5 repetitions indirect contact (0.1 m distance) with one-second duration between successive discharges

For additional information, please refer to Table 3.40 and 3.41 on the following page.

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Regulatory Requirements (continued)

Table 3.40 – Simulation of Lightning Strike

Testing Terminals	V/I Waveform	Peak Voltage	Peak Current	Number of Tests	Primary Protection
Tip to Ring Grounded	10x700 / 5x310	1 kV	25 A	±5	No
Ring to Tip Grounded	10x700 / 5x310	1 kV	25 A	±5	No
Tip and Ring to Ground	10x700 / 5x310	1 kV	25 A	±5	No
Tip to Ring Grounded	10x700 / 5x310	4 kV	100 A	±5	Yes
Ring to Tip Grounded	10x700 / 5x310	4 kV	100 A	±5	Yes
Tip and Ring to Ground	10x700 / 5x310	4 kV	100 A	±5	Yes
Tip and Ring to Ground *	10x700 / 5x310	1 kV	25 A	±5	No

* Simultaneous surge for 50% of the ports

Table 3.41 – Waveform Parameters

Indicated Voltage	Peak of Initiation of the Discharge Currents I_p	Time of Rising During Discharge Switch On / Off t_r	Current at 20 ms I_1	Current at 60 ns I_2
6 kV	22.5 A ± 10%	0.7–1 ns	12 A ± 30%	6 A ± 30%

Regulatory Requirements (continued)

Mainland China Standard - YD/T 993-1998

YD/T 993-1998 establishes the technical requirements and test methods for lightning protection of telecommunication terminal equipment for Mainland China.

This Chinese Standard parallels the ITU-T K.21 "Resistibility of Subscriber's Terminal to Overvoltages and Overcurrents" (1996) document very closely. This standard is the technical basis for simulated lightning induced event testing requirements for Telecommunication Terminal Equipment such as modems, fax machines, telephone sets, and so on.

Normal operation of EUT is not required during the lightning surge simulation test. However, all functions of the EUT should meet the requirements of relevant standards after the completion of these tests. All lightning surge simulation tests should be conducted at:

- Temperature: 15 °C – 35 °C
- Relative humidity: ±5% – ±75%
- Air pressure: 86 – ±56 kPa

Once the lightning surge simulation testing is completed, an electric isolation test is conducted. The power is removed from the unit for this test.

Measure the insulation with 500 V dc voltage after the completion of the insulation test. The resistance should be no less than 2 MΩ.

Table 3.42 Surge Simulations - Tip & Ring Connections

Lightning Surge Test Conditions			Voltage and Current Waveform µs	Test Voltage / Current * (kV/A)
Without Primary Protection	Metallic Test	Single Tip and Ring Pair	10x700 / 5x310	1.5/37.5
			10x700 / 5x310	1.5/37.5
	Longitudinal Test	Single Tip and Ring Pair	10x700 / 5x310	1/25
			10x700 / 5x310	1/25
		All Tip and Ring Pair	10x700 / 5x310	1/25
			10x700 / 5x310	1/25
With Primary Protection	Metallic Test	Single Tip and Ring Pair	10x700 / 5x310	4/100
			10x700 / 5x310	4/100
	Longitudinal Test	Single Tip and Ring Pair	10x700 / 5x310	4/100
			10x700 / 5x310	4/100
		All Tip and Ring Pair	10x700 / 5x310	4/100
			10x700 / 5x310	4/100

Table 3.43 Surge Simulations - Power Line Connections

Lightning Surge Test Conditions			Voltage and Current Waveform µs	Test Voltage / Current * (kV/A)
Without Primary Protection	Metallic Test	Power Line	1.2x50 / 8x20	1.5/750
			1.2x50 / 8x20	1.5/750
	Longitudinal Test	Power Line	1.2x50 / 8x20	1/83.3
			1.2x50 / 8x20	1/83.3
With Primary Protection	Metallic Test	Power Line	1.2x50 / 8x20	4/2000
			1.2x50 / 8x20	4/2000
	Longitudinal Test	Power Line	1.2x50 / 8x20	4/333.3
			1.2x50 / 8x20	4/333.3

* All tests are conducted ±5 times with at least one minute between events.

Table 3.44 Electrical Insulation Test

Equipment Type	Voltage / Current	V&I Waveform µs	Repetition
Handheld	2.5 kV / 62.5 A	10x700 / 5x310	±5
Non-handheld	1.5 kV / 37.5 A	10x700 / 5x310	±5

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Regulatory Requirements (continued)

Mainland China Standard - YD/T 1082-2000

YD/T 1082-2000 establishes the technical specifications on overvoltage and overcurrent protection of access network equipment for Mainland China.

This Chinese Standard parallels the ITU-T K series. This Standard specifies the technical requirements and test methods for overvoltage and overcurrent protection and the basic environmental adaptability of access network equipment. This Standard does not deal with protection against radiated electromagnetic fields.

The specifications as presented here are a succinct summary of the lightning surge, power fault, and ESD testing required by this document.

The ports of the Network equipment are classified into five categories:

I. Ports used to connect the twisted pairs introduced from outside of the building, namely analog user interface, ISDN-BRA interface, ADSL interface, and so on

II. Twisted pair ports used to interconnect the different equipment inside the building, namely V.24 interface, V.35 interface, 2048 kbits/s interface connected to twisted pairs, 10/100 Base-T Ethernet interface, and so on

III. Coaxial cable port: 2048 kbits/s interface connected to coaxial cables, ISDN-PRA interface, and so on

IV. AC Power interface

V. DC power interface

The sequence of testing shall follow this order:

ESD --> EFT --> simulation of lightning strike --> power line induction --> power line contact

ESD Testing

The environmental conditions for ESD testing shall be:

- Temperature—15 °C ~ 35 °C
- Relative humidity—30% ~ 60%
- Air pressure —86 ~ 106 kPa

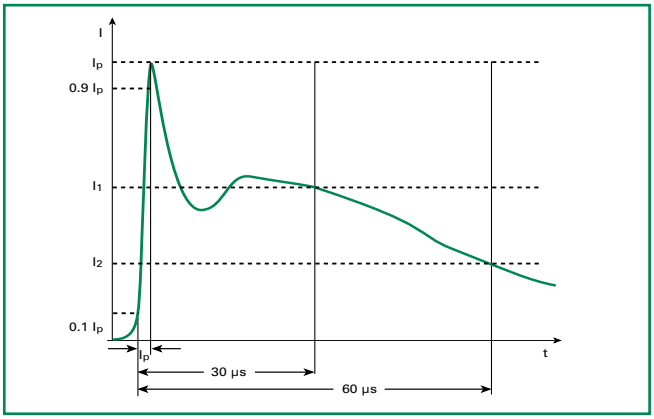
The waveform of the generator should meet the requirements of YD/T 950 as shown in table 3.45.

Establish a communications link via any port of the EUT before the test. The communications link should be capable of normal use without being attended to manually after the test.

Table 3.45 Waveform Parameters

Indicated Voltage	Peak of Initiation of the Discharge Currents I_p	Time of Rising During Discharge Switch On / Off t_r	Current at 20 ms I_1	Current at 60 ns I_2
6 kV	22.5 A ± 30%	0.7–1 ns	12 A ± 30%	6 A ± 30%

Figure 3.12 ESD Waveform



EFT (Electrically Fast Transient)

Waveform of the generator should meet the requirements of ITU-T K.34.

Table 3.46 EFT

Tested Port	Number of Ports		Test Conditions
	Remote	Central Office	
I	1	—	1 kV, 5 kHz, ≥ 1 min
II	1	1	1 kV, 5 kHz, ≥ 1 min
III	1	1	1 kV, 5 kHz, ≥ 1 min
IV	1	—	2 kV, 2.5 kHz, ≥ 1 min
V	—	1	2 kV, 2.5 kHz, ≥ 1 min
VI	—	1	2 kV, 2.5 kHz, ≥ 1 min

Table 3.47 Lightning Surge Test Conditions

Class of Port	Number of Ports		Voltage and Current Waveforms µs	Amplitude *
	Central Office	Remote		
I	—	3	10/700 – 5/310	4 kV
		8	1.2/50 – 8/20	6 kV
II	1	1	1.2/50 – 8/20	500 V
III	1	1	1.2/50 – 8/20	500 V
IV	—	1	1.2/50 – 8/20	10 kV, 5 kA
V	1	1	1.2/50 – 8/20	500 V

* All tests are conducted ±5 times with at least one minute between events.

Table 3.48 Power Line Induction and Contact Testing

Tested Port	Number of Ports		Test Conditions
	Remote	Central Office	
I	3	—	600 V, 600Ω, 50 Hz, 1 s
I	1	—	220 V, 50 Hz, 1 h, 600/200/10Ω

Regulatory Requirements (continued)

Certification and Accreditation Administration of the People's Republic of China

Type testing and initial inspection of the factory and follow-up inspection similar to UL standards shall be required in China. The formal application shall be submitted with the following documents:

1. Circuit diagram and/or system block
2. List of critical components and/or materials
3. Description of the difference between the different model/type of products in the same application unit.
4. Service manual and user's manual in Chinese
5. Nameplate and warnings in Chinese
6. Other necessary documents

Testing standards are as follows:

1. GB4943-1995 *Safety of Information Technology Equipment Including Electrical Business Equipment*
2. YD/T993 T*echnical Requirements and Test Methods of Lightning Resistibility for Telecommunication Terminal Equipment*
3. GB9254-1998 *Information Technology Equipment—Radio Disturbance Characteristics –Limits and Methods of Measurement*
4. YD1103 *Requirements and Measurement Methods of Electromagnetic Compatibility for Cordless Telephone*
5. YD1032 *Limits and Measurement Methods of Electromagnetic Compatibility for 900/1800 MHz Digital Cellular Telecommunications System Part 1: Mobile Station and Ancillary Equipment*
6. YD1169.1 *Requirement and Measurement Method of Electromagnetic Compatibility for 800 MHz CDMA Digital Cellular Telecommunications System Part 1: Mobile Station and Ancillary Equipment*

These documents require:

1. Test items for safety
2. Testing items for lightning, lightning test of telecommunication interface, and lightning test of power line
3. Testing items for EMC

Note: The test items for safety shall include all appropriate items specified in standards of GB4943-1995.

The following parameters outline testing procedures for lightning-induced surges and power fault events:

- Surge requirements:
  100 A 10x1000 waveform
  10 A, 50 Hz, 1 s
  5 A, 50 Hz, 30 s
  260 V on 100 kV/s
  400 V on 1 kV/µs
- Temperature limits: -40 to 65 °C
- Insulation leakage requirements: 0.1 µA @ 100 V dc
- Maximum load capacitance: 200 pF

The following is actual text of the circular from the Certification and Accreditation Administration of the People's Republic of China (CNCA).

Standard	Testing Item
GB9254	Radiated emissions Conducted emissions
YD1103	Radiated emissions Conducted emissions Electrostatic discharge (ESD) immunity Radiated radio-frequency electromagnetic field immunity Electric fast transient / burst immunity Immunity to conducted disturbance, induced by radio-frequency fields
YD1032	Conducted spurious emissions Radiated spurious emissions Radiated emissions Conducted emissions Electrostatic discharge (ESD) immunity Electric fast transient / burst immunity Surge immunity
YD1169.1	Conducted spurious emissions Radiated spurious emissions Radiated emissions Conducted emissions Electrostatic discharge (ESD) immunity Radiated radio-frequency electromagnetic field immunity Electric fast transient / burst immunity Surge immunity

YD1103 only applies to cordless telephone and YD1032 applies to GSM mobile terminal while YD1169.1 only applies to CDMA mobile terminal.

Circular Relevant to the Implementation of the Compulsory Product Certification System

by the Certification and Accreditation Administration of the People's Republic of China (CNCA) December 3, 2001

The Compulsory Product Certification System (CPCS) is jointly announced for statutory implementation by the State General Administration for Quality Supervision and Inspection and Quarantine of the People's Republic of China (AQSIQ) and the Certification and Accreditation Administration of the People's Republic of China (CNCA). This new system consists of Regulations for Compulsory Product Certification, Regulations for Compulsory Product Certification Mark, and the First Catalogue of Products Subject to Compulsory Certification (hereinafter referred to as the Catalogue), and so on. The Old System, namely, the Safety License System for Import Commodities administered by the former State Administration for Entry-Exit Inspection and Quarantine of the People's Republic of China (CIQ), and the Compulsory Supervision System for Product Safety Certification administered by the former China State Bureau of Quality and Technical Supervision (CSBTS), will be replaced. The following circular is announced concerning the transition from the Old System to the New System.

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Regulatory Requirements (continued)

1. *The time when the New System is implemented and the Old System is annulled Regulations for Compulsory Product Certification stipulates that the New System be implemented on May 1, 2002 and the Old System be annulled on May 1, 2003 so as to ensure a smooth transition and an effective safeguard of the legitimate rights and interests of all the parties concerned.*

2. *Supervision of products applicable to either the New System or the Old System*

   1) *Starting from May 1, 2003, the Catalogue products either marketed by domestic manufacturers or imported must obtain the certificate for compulsory product certification (hereinafter referred to as the New Certificate) and be applied China Compulsory Certification mark (hereinafter referred to as the New Mark) before they are imported or marketed.*

   2) *Starting from May 1, 2003, the sales outlets or importers are not permitted to purchase, import or sell the Catalogue products that do not bear the New Certificate and the New Mark. Whereby the Catalogue products that are purchased or imported before April 30, 2003 and bear either the Import Safety License and CCIB Mark or the Safety Certificate and the Great Wall Mark (hereinafter referred to as the Old Certificate and the Old Mark) may still be sold under the supervision of the AQSIQ local branches with which such products are filed.*

   3) *Starting from May 1, 2003, if the Catalogue products that have obtained the New Certificate and the New Mark need continue to use the outer packing applied with the Old Mark, they can be marketed or imported only when the New Mark is applied along with the Old Mark.*

   4) *Prior to April 30, 2003, the Catalogue products for which the Old Certificate and the Old Mark is compulsory can be marketed or imported by either the Old Certificate and the Old Mark or the New Certificate and the New Mark.*

   5) *Starting from May 1, 2002, with regard to products for which the Old Certificate and the Old Mark was compulsory but being no longer covered by the Catalogue this time, the Old Certificate and the Old Mark will not be required when they are marketed or imported.*

3. *The acceptance of the certification application*

   1) *Starting from May 1, 2002, the certification bodies designated by CNCA (hereinafter referred to as DCBs) begin to accept applications for the New Certificate and the New Mark relevant to the Catalogue products and will no longer accept applications for the Old Certificate and the Old Mark.*

   2) *Prior to April 30, 2002, the Catalogue products for which the Old Certificate and the Old Mark is compulsory may continue to apply for the Old Certificate and the Old Mark.*

4. *Supplements*

   1) *With regard to the Catalogue products for which the application has already been filed but the Old Certificate is yet to be granted, or for which the Old Certificate has been granted, the New Certificate and the New Mark can be granted upon further application by the applicant and the confirmation of the product's qualification by the DCB.*

   2) *The cost incurred for the New Certificate an the New Mark referred to in 4.1 will be borne by the applicant based on the actual items required according to the fee chart of the New System.*

Regulations for Compulsory Product Certification Chapter I General Provisions

Article 1

Based on relevant laws and regulations covering product safety licensing and product quality certification so as to improve and enhance regulatory functions in the field of compulsory product certification as well as to effectively safeguard national and public interests in a feasible manner, the following regulations are announced for statutory implementation in accordance with the functions of the State General Administration for Quality Supervision and Inspection and Quarantine of the People's Republic of China (AQSIQ) and the Certification and Accreditation Administration of the People's Republic of China (CNCA) authorized by the State Council.

Article 2

The Compulsory Product Certification System (hereinafter referred to as CPCS) is applied to products related to human life and health, animals, plants, environmental protection and national security.

Article 3

Authorized by the State Council, CNCA is in charge of nation-wide certification and accreditation activities.

Article 4

With regard to CPCS, one Catalogue of Products Subject to Compulsory Product Certification (hereinafter referred to as the Catalogue), one set of applicable technical regulations, national standards and conformity assessment procedures, one obligatory mark and one structural fee chart will be announced for statutory implementation.

Article 5

Any product covered by the Catalogue must first be certified by a certification body designated by relevant competent authorities (hereinafter referred to as DCB). The subject product must obtain the certificate and be applied the certification mark before it can be marketed, imported or used for any commercial purposes.

Regulatory Requirements (continued)

UL 497 Series of Safety Standards

The UL 497 series is a family of three safety standards that provides requirements for protection devices used in low-voltage circuits.

- UL 497 addresses requirements for primary protectors used in paired communications circuits.
- UL 497A covers secondary protectors for use in single or multiple pair-type communications circuits.
- UL 497B addresses protectors used in data communication and fire alarm circuits.
- UL 497C addresses protectors for coaxial circuits.
- UL 497D addresses protectors located on the equipment side of a primary protector, also known as the protected side of the circuit (typically current activated devices such as TBUs.)

The focus of UL 497 is to ensure that paired communication circuit protectors do not become a fire or safety hazard. The requirements in UL 497 cover any protector that is designed for paired communications circuits and is employed in accordance with Article 800 of the National Electric Code. The protectors covered in UL 497 include solid state primary and station protectors. These circuit protectors are intended to protect equipment, wiring, and service personnel against the effects of excessive voltage potential and currents in the telephone lines caused by lightning, power fault, power induction, and rises in Ground potential.

UL 497 Construction and Performance Requirements

The "Construction" section covers the following requirements:

- General
- Components
- Protection Against Corrosion
- Field-wiring Connections
- Enclosures
- Spacing

The "Performance" section covers the following requirements:

- General
- Instrument Fuse Test
- Polymeric Material Test
- Jarring Test
- Drop Test
- Strain Relief Test
- Line Fuse Test
- Arrester Test
- Rubber Materials Test
- Water Spray Test
- Cover Replacement Test
- Marking
- Corrosion Test, Outdoor Use Protector
- Replacement Arresters Installation Test
- Appliqué Assemblies Installation Test
- Dielectric Voltage-withstand Test
- Manufacturing and Production Tests

Performance Tests

Key performance tests which concern overvoltage protectors are detailed in the arrester test section. Requirements are:

- **Breakdown Voltage Measurement**—Arresters are to be tested in the protector blocks or panels in which they are intended to be employed. Arresters are required to break down within ±25% of the manufacturer's specified breakdown rating. In no case shall the breakdown voltage exceed 750 V peak when subjected to the strike voltage test. (Figure 3.13) At no time during this test will the supply voltage be increased at a rate greater than 2000 V/µs.
- **Impulse Spark-over Voltage Measurement**—The arrester must break down at less than 1000 V peak when subjected to a single impulse potential. Arresters are to be tested in each polarity with a rate of voltage rise of 100 V/µs, ±10%.
- **Abnormal Operation**—Single pair fuseless arresters must be able to simultaneously carry 30 A rms at 480 V rms for 15 minutes without becoming a fire hazard. A fire hazard is determined by mounting the arrester on a vertical soft wood surface and covering the unit with cheesecloth. Any charring or burning of the cheesecloth results in test failure. During this test, although the arresters may short, they must not have an impulse spark-overvoltage or DC breakdown voltage greater than 1500 V peak.
- **Discharge Test**—Protectors must comply with the strike voltage requirements after being subjected to five successive discharges from a 2 µF capacitor charged to 1000 V dc. (Figure 3.14).
- **Repeated Discharge Test**—The arrester must continue to break down at or below its maximum rated breakdown voltage after being subjected to 500 discharges from a 0.001 µF capacitor charged to a potential of 10,000 V dc. The interval between pulses is five seconds. Arresters are to be tested in each polarity, and it is acceptable for the protector to short circuit following the discharge testing. (Figure 3.14)

Figure 3.13 UL 497 Breakdown Voltage Measurement

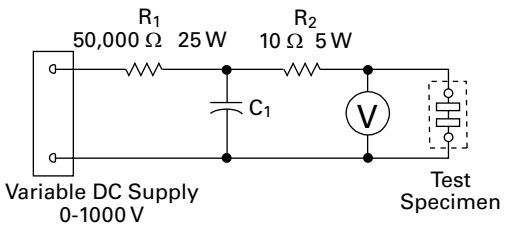
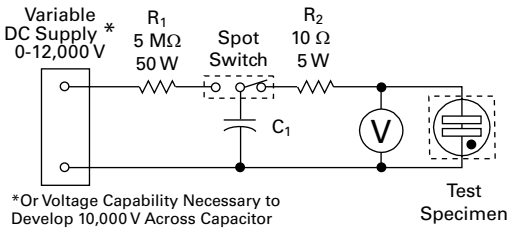


Figure 3.14 UL 497 Discharge Test



Revised: 02/23/17

Regulatory Requirements (continued)

UL 497A addresses secondary protectors for use in single or multiple pair-type communication circuits intended to be installed in accordance with Article 800 of the National Electric Code (NEC) and to have an operating voltage of less than 150 V rms with respect to Ground. The purpose of UL 497A is to help reduce the risk of fire, electric shock, or injury resulting from the deployment and use of these protectors. UL 497A requirements do not cover telephone equipment or key systems.

UL 497A Construction, Risk of Injury, and Performance Requirements

The "Construction" section covers the following requirements:

- General
- Product Assembly
- Enclosures
- Internal Material
- Accessibility and Electric Shock
- Protection Against Corrosion
- Cords
- Current-carrying Parts
- Internal Wiring
- Interconnecting Cords and Cables
- Insulating Material
- Printed Wiring
- Spacing

The "Risk of Injury" section covers the following requirements:

- Modular Jacks
- Sharp Edges
- Stability
- Protection of Service Personnel

The "Performance" section covers the following requirements:

- General
- Impulse Voltage Measurement
- Overvoltage Test
- Endurance Conditioning
- Component Temperature Test
- Drop Test
- Crush Test
- Leakage Current Test
- Dielectric Voltage-withstand Test
- Rain Test
- Maximum Moment Measurement Test
- Weather-o-meter and Micro Tensile Strength Test
- Thermal Aging and Flame Test
- Electric Shock Current Test
- Manufacturing and Production Line Test
- Marking, Installation, and Instructions

Performance Tests

The following key performance tests relate to overvoltage protection of the secondary protectors:

1. **Impulse Voltage Measurement Test**—Secondary protectors must break down within ±25% of the manufacturer's breakdown rating when tested in each polarity with a rate of voltage rise of 100 V/µs, ±10%. Note that the manufacturer may assign separate breakdown voltage ratings for the Breakdown Voltage Measurement Test. This requirement only applies to secondary protectors that connect between Tip and Ring of the telephone loop.
2. **Breakdown Voltage Measurement Test**—Secondary protectors must break down within ±25% of the manufacturer's breakdown rating when tested in each polarity with a rate of voltage rise no greater than 2000 V/s. The secondary protector is to be mounted in accordance with the manufacturer's installation instructions and then subjected to the test circuit shown in Figure 3.15. This requirement applies only to secondary protectors connected between Tip and Ring or Tip/Ring and Ground of the telephone loop.
3. **Overvoltage Test**—Secondary protectors must limit current and extinguish or open the telephone loop without loss of its overvoltage protector, indication of fire risk, or electric shock. Upon completion of this test, samples must comply with the Dielectric Voltage-withstand Test.

The overvoltage test is used to determine the effects on secondary protectors and is shown in Table 3.48. Test connections are shown in Figure 3.16.

Regulatory Requirements (continued)

Test Compliance

Compliance with the overvoltage test is determined by meeting the following criteria:

- Cheesecloth indicator may not be either charred or ignited
- Wiring simulator (1.6 A Type MDQ fuse or 26 AWG line cord) may not be interrupted
- Protector meets the applicable dielectric voltage withstand requirements after the completion of the overvoltage tests

Table 3.48 UL 497A Overvoltage Test

Test	Voltage (V_{RMS})	Current (A)	Time	Comments
L1	600	40	1.5 s	(Note 1, Figure 4.11)
L2	600	7	5 s	(Note 1, Figure 4.11)
L3	600	2.2, 1, 0.5, 0.25	30 min at each current level	(Note 2, Figure 4.11)
L4	200 V rms or just below the breakdown voltage of the overvoltage protection device	2.2 A or just below the interrupt value of the current interrupting device	30 min	(Note 2, Figure 4.11)
L5	240	24	30 min	(Note 1, Figure 4.11)

Notes:
1. Apply Tests L1, L2, and L5 between Tip and Ground or Ring and Ground.
2. Apply Tests L3 and L4 simultaneously from both Tip and Ring to Ground.

Figure 3.15 UL 497A Breakdown Voltage Measurement Test

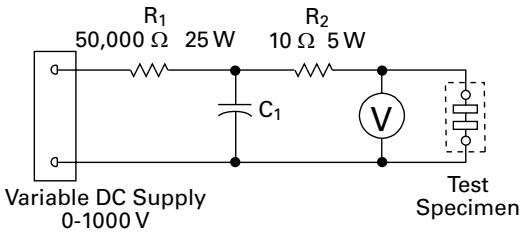
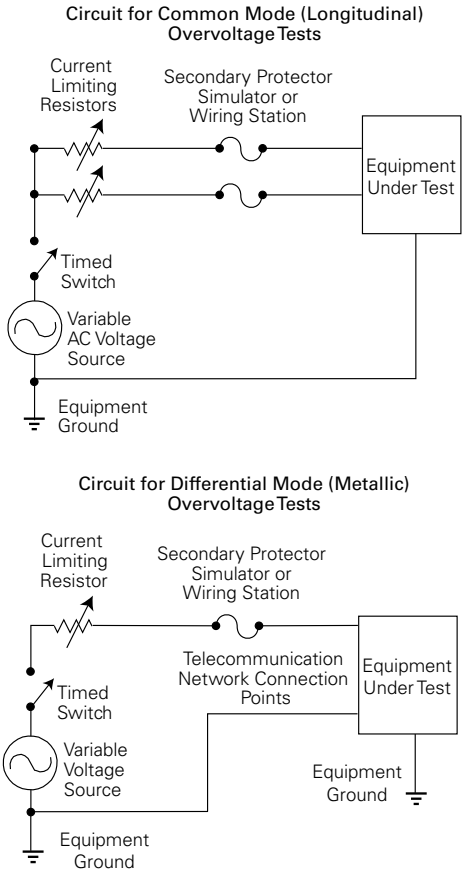


Figure 3.16 UL 497A Overvoltage Test



Regulatory Requirements (continued)

UL 497B provides requirements for protectors used in communication and fire alarm circuits. This standard does not cover devices for primary protection or protection devices used on telephone lines. *SIDACtor®* devices are components recognized in accordance with UL 497B under UL file number E133083.

Construction and Performance Requirements

The "Construction" section covers the following requirements:

- General
- Corrosion Protection
- Field-wiring Connections
- Components
- Spacing
- Fuses

The "Performance" section covers the following requirements:

- General
- Strike Voltage Breakdown
- Endurance Conditioning
- Temperature Test
- Dielectric Voltage-withstand Test
- Vibration Conditioning
- Jarring Test
- Discharge Test
- Repeated Discharge Test
- Polymeric Materials Test
- High Temperature Test
- Marking

Performance Requirements Specific to SIDACtor® Devices

1. **Strike Voltage Breakdown Test**—Protectors are required to break down within the manufacturer's specified breakdown range or within 10% of a nominal single breakdown voltage rating. (Figure 3.17)
2. **Endurance Conditioning**—Protectors are subjected to 50 impulse cycles. Each cycle is a 1000 V peak, 10 A, 10x1000 µs pulse. Pulses are applied in one polarity at 10-second intervals and then repeated in the opposite polarity.
3. **Variable Ambient Conditioning**—Protectors must comply with the strike voltage requirements after being subjected to an ambient temperature of 0 °C for four hours and again after being subjected to an ambient temperature of 49 °C for an additional four hours.
4. **Discharge Test**—Protectors must comply with strike voltage requirements after being subjected to five successive discharges from a 2 µF capacitor charged to 1000 V dc. (Figure 3.18)
5. **Repeated Discharge Test**—Protectors must not break down at a voltage higher than the manufacturer's maximum rated breakdown voltage nor lower than rated stand-off voltage after being subjected to 500 discharges from a 0.001 µF capacitor charged to 10,000 V dc. The discharges are applied in five-second intervals between one side of the protector and Ground. Upon completion of the discharge tests, protectors are once again required to meet the strike voltage requirement. (Figure 3.18)

Note : The epoxy used to construct a *SIDACtor®* device body meets UL 94V-0 requirements for flammability.

Figure 3.17 UL 497B Strike Voltage Breakdown Test

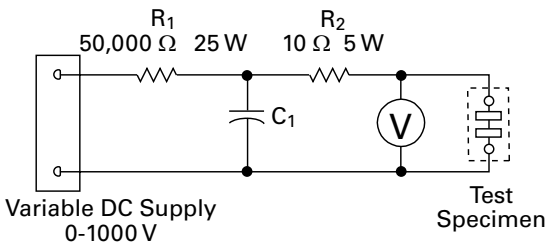
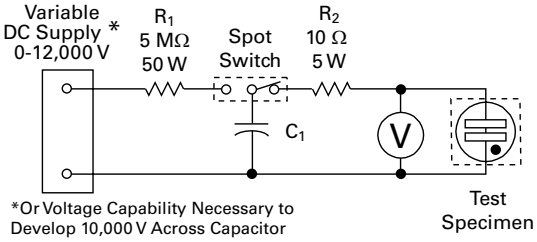


Figure 3.18 UL 497B Discharge Test



Revised: 02/23/17

Regulatory Requirements (continued)

UL 497C requirements cover protectors for use on coaxial cable circuits. This standard covers construction and performance requirements.

UL 497C Construction and Performance Requirements

The "Construction" section covers the following requirements:

- General
- Corrosion Protection
- Field-wiring Connections
- Components
- Spacing
- Enclosures

The "Performance" section covers the following requirements:

- General
- I^2t Limiting
- Abnormal Sustained Current
- Component Temperature Test
- Breakdown Voltage Measurement
- Impulse Spark-over Voltage Measurement
- Limited Short-circuit Test
- High Current Ground Path Test
- Cable Shield Fuse Test
- Endurance Conditioning Test
- Induced Low Current Test
- Distortion Test
- Flame Test
- Impact Test (Polymeric Enclosures)
- Jarring Test
- Water Spray Test
- Leakage Current Test
- Dielectric Voltage-withstand Test
- Ultraviolet Light and Water Exposure
- Tensile Strength and Elongation Tests
- Air Oven Aging
- Ozone Exposure

Performance Requirements Specific to SIDACtor® Devices

1. **Strike Voltage Breakdown Test**—Protectors are required to break down within ±25% of the manufacturer's specified breakdown range but no higher than 750 V at ≤ 2 kV/s rise time.
2. **Endurance Conditioning**—Protectors are subjected to 500 impulse cycles. Each cycle is a 1000 V peak, 10 A, 10x1000 µs pulse. Pulses are applied in one polarity at 10-second intervals and then repeated in the opposite polarity. Then, 100 cycles of 1000 V peak, 100 A, 10x1000 µs pulse are applied to three new protectors. Finally, two cycles of 1000 V peak, 5000 A, 8x20 µs pulse are applied to three new protectors, with a rest period of one minute between surges.
3. **Variable Ambient Conditioning**—Protectors must comply with the strike voltage requirements after being subjected to an ambient temperature of 25 °C for four hours and again after being subjected to an ambient temperature of 90 °C for an additional four hours.
4. **Discharge Test**—Protectors must comply with strike voltage requirements after being subjected to a discharge of 1000 V, 100 ± 10 V/µs, 10 A impulse.

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Regulatory Requirements (continued)

UL 497D

UL 497D covers secondary protector components for communications circuits located on the equipment side of a primary protector, also known as the protected side of the circuit. With a few exceptions, these devices shall also comply with all the requirements of UL 497A.

These components provide voltage and/or current surge protection after the primary protector but "these components do not normally provide protection for the voltage suppression device needed in the circuit to limit the voltage to less than the component ratings." It will limit current to the capacity of the protected wiring, however; they do not provide protection against excessive currents that may flow during the operation of the primary protection device. Thus, additional overcurrent protection prior to the voltage suppression device may be required.

The overvoltage test of UL 497A, Section 27, are to be performed using a reduced test voltage based on the voltage ratings of the component being tested. These tests are:

a) **Test L1** – @ Voltage rating of device, 40A, 1.5 S.

b) **Test L2** – @ Voltage rating of device, 7A, 5 S.

c) **Test L3** – @ Voltage rating of device, 2.2A, 30 M (and 1.0A, 0.5A, & 0.25A)

d) **Test L4** – 200V, 2.2A, 30 M or, when the equipment contains voltage-limiting devices operating between 200 and 600 volts AC, and the secondary protector employs other components that can be affected by the fault; at a voltage value just below the breakdown point of the overvoltage device is to be used. When the secondary protector contains current interrupting devices operating below 2.2 amperes, a current value just below the interrupting point of such device is to be used. This test is conducted for a minimum of thirty minutes. The test may be ended when during the trial it can be verified that the sample has mechanically disconnected the test current as described for Test L3.

Compliance with this test is based on the following conditions being met:

a) There shall be no ignition or charring of the cheesecloth indicator.

b) Based on the wiring simulator that is used:

   1) The fuse or device used as the wiring simulator (MDQ 1-6/10) shall not interrupt the current during the test or

   2) When a No. 26 AWG (0.13 mm2) solid copper wire is used as the wiring simulator, it shall not fuse open and shall not cause ignition or charring of the cheesecloth indicator.

c) The secondary protector shall comply with the Dielectric Voltage-Withstand Test:

   1) one minute, without breakdown, the application of 40-70 Hz AC, between live parts and the enclosure; live parts and exposed dead-metal parts; and live parts of circuits operating at different potentials or frequencies. The test potential shall be:

      a) For a unit rated 30 volts AC rms (42.2 volts AC peak) or less – 500 volts

      b) For a unit rated between 31 and 150 volts AC rms – 1000 volts

Regulatory Requirements (continued)

UL 60950-1 2nd Edition

UL 60950-1 1st edition replaced UL 60950 effective July 1, 2006. UL 60950-1 2nd edition will effectively replace UL 60950-1 1st edition December 1, 2010. This 2nd Edition version made several changes but the most important ones to consider for telcom related applications are:

1) the reduced minimum clearances and creepage distances
2) pollution degree 2 and 3 clearance dimensions were modified so they now agree with the IEC 60664-1 Table G.2 values and
3) ringing signals test procedure for FCC Part 68 were corrected

The UL 60950-1 1st edition has an effective date of July 1, 2006, meaning that new products submitted after that date will be evaluated using the 1st edition version. However, products submitted after December 1, 2010 will be evaluated using the 2nd edition version. Therefore, between July 2006 and December 2010, the equipment may be tested to either 1st or 2nd edition. Products certified by UL to requirements prior to these effective dates may continue to be certified without further reinvestigation unless otherwise indicated specifically by UL.

The Technical Harmonization Committee (THC) 62368 is considering the development of a new U.S./Canadian bi-national standard based on a new IEC Standard (February 2010 expected completion date). The IEC is developing a new hazard-based standard for Audio/Video, Information Technology and Communication Technology Equipment, which will eventually replace the existing Telcom Standard (IEC 60950-1) and the Audio/Video Standard (IEC 60065).

This safety standard is intended to prevent injury or harm due to electrical shock, energy hazards, fire, heat hazards, mechanical hazards, radiation hazards, and chemical hazards.

After the divestiture of the AT&T/Bell system, the National Electric Code (NEC) implemented Article 800-4, which mandates that "all equipment intended for connection to the public telephone network be listed for that purpose" in order to ensure electrical safety. A manufacturer can meet this requirement by listing their product with Underwriters Laboratories under UL 60950-1 (based on IEC 60950-1,). The NEC requires all telecommunication wiring that enters a building to pass through a primary protector, which is designed to limit AC transients in excess of 600 V rms. These transients are due to the fact that telephone lines run in close proximity to AC power lines. Most telecommunication equipment uses a secondary overvoltage protector such as the *SIDACtor*® device. The secondary devices typically limit transients in excess of 350 V rms. Therefore, a potentially dangerous condition exists because of the voltage threshold difference of the primary protector and the secondary protector. To minimize this danger, compliance with UL 60950-1 is required. UL 60950-1 covers equipment with a rated voltage (primary power voltage) not exceeding 600 V and equipment designed to be installed in accordance with the NEC NFPA 70. This standard does not apply to air-conditioning equipment, fire detection equipment, power supply systems, or transformers.

It defines three classes of equipment:

- **Class 1**—protection achieved by basic insulation
- **Class 2**—protection achieved by double or reinforced insulation
- **Class 3**—protection relying upon supply from SELV circuits (voltages up to 40 V peak or 60 V dc)

UL 60950-1 also defines five categories of insulation:

- Functional
- Basic
- Supplementary
- Reinforced
- Double

UL 60950-1 Terminology

The following definitions assist in understanding UL 60950-1:

Creepage distance is the shortest distance between two conductors, measured along the surface of the insulation. DC voltages are included in determining the working voltage for creepage distances. (The peak value of any superimposed ripple or short disturbances, such as cadenced ringing signals, shall be ignored.) Clearance distance is the shortest distance between two conductive parts or between a conductive part and the outer surface of the enclosure measured through air. DC voltages and the peak value of any superimposed ripple are included in determining the working voltage for clearance distances. Creepage and clearance distances are subject to the pollution degree of the equipment:

- Pollution degree 1—components and assemblies sealed to prevent ingress of dust and moisture
- Pollution degree 2—generally applicable to equipment covered by UL 60950-1
- Pollution degree 3—equipment subject to conductive pollution or to dry non-conductive pollution, which could become conductive due to expected condensation

UL 60950-1 defines a secondary circuit as a circuit with no direct connection to a primary circuit and defines a primary circuit as a circuit directly connected to the ac mains supply.

SELV (Secondary Electrical Low Voltage) Secondary circuit whose voltage values do not exceed a safe value (voltage less than hazardous levels of 42.4 V peak or 60 V dc); regarded as not hazardous under dry conditions for an area of contact equivalent to the size of a human hand

TNV Telecommunication Network Voltage (a secondary circuit) (please refer to Table 3.49 on next page)

TNV-1 This is a TNV circuit with normal operating voltages that do not exceed SELV limits and has exposure to overvoltages

TNV-2 This is a TNV circuit with normal operating voltages that do not exceed SELV limits and has no exposure to overvoltages

TNV-3 This is a TNV circuit with normal operating voltages that exceed SELV limits and has exposure to overvoltages

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Regulatory Requirements (continued)

UL 60950-1 Terminology (continued)

When determining the working voltage for TNV-2 & 3, it is assumed to be 120V dc unless it is specifically known for the application. For a TNV, it is assumed to be 60V dc, unless it is specifically known for the application. Telephone ringing signals are NOT taken into account for this determination.

Table 3.49 TNV Levels

Overvoltages from TELECOMMUNICATION NETWORKS possible?	Normal operating voltages	
	Within SELV CIRCUIT limits	Exceeding SELV CIRCUIT limits but within TNV CIRCUIT limits
Yes	TNV-1 CIRCUIT	TNV-3 CIRCUIT
No	SELV CIRCUIT	TNV-2 CIRCUIT

To ensure safe operating conditions of equipment, UL 60950-1 focuses on the insulation rating of the circuit(s) under consideration. Tables 3.50 and 3.51 (next page) indicate the required creepage and clearance distances depending on material group, pollution degree, working voltage and maximum transient voltage in the secondary circuit. For a typical telecommunication application with a working voltage of 200 V, pollution degree 2, material group IIIb, the creepage distance is 2 mm. In this example, the clearance distance would be 1.8 mm if the transients are limited to values less than 800 V but allowed to go higher than 71 V (and no special quality control program is in place). This clearance distance is intended to prevent arcing during overvoltage events. IF the minimum creepage distance derived from these tables is less than the applicable minimum clearance distance, then that clearance distance would be used.

The highest transient voltage in a TNV-1 or TNV-3 circuit is determined by applying a 10x700 µS voltage waveshape surge event with an open circuit value of 1.5 kV and a 5x310 current waveshape with a short circuit value of 37.5A. For a TNV-2 circuit, this highest transient voltage is determined by applying a 10x700 µS voltage waveshape surge event with an open circuit value of 800 V and a 5x310 current waveshape with a short circuit value of 20A. These surges are applied 3 to 6 times in each polarity with a minimum of one second between impulses across:

1) the positive and negative supply points
2) between all supply points joined together and protective earth
3) between tip and ring and
4) then between tip and ring joined together and earth.

A coated PCB may use the smaller separation distances as provided in the table below IF its manufacturing process is subjected to a quality control program that assures double insulation and reinforced insulation compliance.

Table 3.52

PEAK WORKING VOLTAGE ≤ X V peak	FUNCTIONAL, BASIC or SUPPLEMENTARY INSTALATION mm	REINFORCED INSULATION mm
90	0.1	0.2
180	0.2	0.4
230	0.3	0.6
285	0.4	0.8
355	0.6	1.2
455	0.8	1.6
570	1.0	2.0
710	1.3	2.6
895	1.8	3.6

Regulatory Requirements (continued)

Table 3.50 Minimum clearances in secondary circuits (mm)

PEAK WORKING VOLTAGE X ≤	CLEARANCES in mm																	
	Highest transient overvoltage in the SECONDARY CIRCUIT (V peak)																	
	X ≤ 71V			71V < X ≤ 800V			X ≤ 800V			800V < X ≤ 1500V						1500V < X ≤ 2500V		
	Pollution Degree																	
	1 and 2						3			1 and 2			3			1, 2 and 3		
V	F	B/S	R	F	B/S	R	F	B/S	R	F	B/S	R	F	B/S	R	F	B/S	R
71	0.2	0.4 -0.2	0.8 (0.4)	0.2	0.7 (0.2)	1.4 (0.4)	0.8	1.3 (0.8)	2.6 (1.6)	0.5	1.0 (0.5)	2.0 (1.0)	0.8	1.3 (0.8)	2.6 (1.6)	1.5	2.0 (1.5)	4.0 (3.0)
140	0.2	0.7 (0.2)	1.4 (0.4)	0.2	0.7 (0.2)	1.4 (0.4)	0.8	1.3 (0.8)	2.6 (1.6)	0.5	1.0 (0.5)	2.0 (1.0)	0.8	1.3 (0.8)	2.6 (1.6)	1.5	2.0 (1.5)	4.0 (3.0)
210	0.2	0.7 (0.2)	1.4 (0.4)	0.2	0.9 (0.2)	1.8 (0.4)	0.8	1.3 (0.8)	2.6 (1.6)	0.5	1.0 (0.5)	2.0 (1.0)	0.8	1.3 (0.8)	2.6 (1.6)	1.5	2.0 (1.5)	4.0 (3.0)
280	0.2	1.1 (0.2)	2.2 (0.4)	F 0.8B/S 1.4 (0.8) R 2.8(1.6)												1.5	2.0 (1.5)	4.0 (3.0)
420	0.2	1.4 (0.2)	2.8 (0.4)	F 1.0 B/S 1.9 (1.0) R 3.8(2.0)												1.5	2.0 (1.5)	4.0 (3.0)

Note: The values in parentheses apply to BASIC INSULATION, SUPPLEMENTARY INSULATION or REINFORCED INSULATION if manufacturing is subjected to a quality control program.
Note: F = Functional B = Basic S = Supplementary R = Reinforced D = Double

Table 3.51 Minimum creepage distances (mm)

RMS WORKING VOLTAGE ≤ X	CREEPAGE DISTANCES in mm								
	Pollution degree								
	1	2	1	2			3		
	Material group								
	Printed boards		Other materials						
	I, II, IIIa, IIIb	I, II, IIIa	I, II, IIIa, IIIb	I	II	IIIa, IIIb	I	II	IIIa, IIIb
10	0.025	0.04	0.08	0.4	0.4	0.4	1.0	1.0	1.0
12.5	0.025	0.04	0.09	0.42	0.42	0.42	1.05	1.05	1.05
16	0.025	0.04	0.1	0.45	0.45	0.45	1.1	1.1	1.1
20	0.025	0.04	0.11	0.48	0.48	0.48	1.2	1.2	1.2
25	0.025	0.04	0.125	0.5	0.5	0.5	1.25	1.25	1.25
32	0.025	0.04	0.14	0.53	0.53	0.53	1.3	1.3	1.3
40	0.025	0.04	0.16	0.56	0.8	1.1	1.4	1.6	1.8
50	0.025	0.04	0.18	0.6	0.85	1.2	1.5	1.7	1.9
63	0.04	0.06	0.2	0.63	0.9	1.25	1.6	1.8	2.0
80	0.063	0.10	0.22	0.67	0.9	1.3	1.7	1.9	2.1
100	0.1	0.16	0.25	0.71	1.0	1.4	1.8	2.0	2.2
125	0.16	0.25	0.28	0.75	1.05	1.5	1.9	2.1	2.4
160	0.25	0.40	0.32	0.8	1.1	1.6	2.0	2.2	2.5
200	0.4	0.63	0.42	1.0	1.4	2.0	2.5	2.8	3.2
250	0.56	1.0	0.56	1.25	1.8	2.5	3.2	3.6	4.0
320	0.7	1.6	0.75	1.6	2.2	3.2	4.0	4.5	5.0
400	1.0	2.0	1.0	2.0	2.8	4.0	5.0	5.6	6.3
500	1.3	2.5	1.3	2.5	3.6	5.0	6.3	7.1	8.0
630	1.8	3.2	1.8	3.2	4.5	6.3	8.0	9.0	10
800	2.4	4.0	2.4	4.0	5.6	8.0	10	11	12.5

The Material Groups are defined as:

Material Group I CTI ≥ 600
Material Group II 600 > CTI ≥ 400
Material Group IIIa 400 > CTI ≥ 175
Material Group IIIb 175 > CTI ≥ 100

If the Material Group is not known, then Material Group IIIb shall be assumed.

Regulatory Requirements (continued)

Clause 6.1.2 *Separation of the telecommunication network from earth* contains the following test requirements:

1) For applications where the nominal ac mains supply > 130 V, a 1.5 kV insulation test is conducted with surge suppressors bridging the insulation barrier removed (applied between tip/ring and earth)
2) For applications where the nominal ac mains supply < 130 V, a 1 kV insulation test is conducted with surge suppressors bridging the insulation barrier removed (applied between tip/ring and earth)
3) IF the surge suppressors were removed then the tip and ring leads are connected together with surge suppressors connected and:
   a) for case #1 above a 230 V 50 /60 Hz signal is applied through a 5 k ohm resistor between them and protective earth with surge suppressors connected. The current must be < 10 mA.
   b) for case #2 above a 120 V 50 /60 Hz signal is applied through a 5 k ohm resistor between them and protective earth with surge suppressors connected. The current must be < 10 mA.

The voltage applied to the insulation under test for test condition 1 and 2 above is gradually raised from zero to the prescribed voltage and held at that value for 60 S.

Surge suppressors that connect to protective ground shall have a minimum operating voltage that is equal to:

1) (180 V + 20% of its rated operating voltage) for ac mains < 130 V and
2) (360 V + 20% of the rated operating voltage) for ac mains > 130V

These separation requirements do NOT apply to any of the following:

1) permanently connected equipment or pluggable equipment type B
2) equipment that is intended to be installed by a service person and has instructions requiring the equipment be connected to a socket-outlet with a protective earthing connection OR
3) equipment that has provision for a permanently connected earthing conductor and is provided with instructions for installation of that conductor

The electric strength test for telecommunication networks contains two test condition categories. Compliance is checked by testing to one of these two categories. This is intended to protect users from overvoltages on the telcom network.

1) Impulse Test

- ±10 10x700 µS voltage waveshape surge event with an open circuit value of 2.5 kV and a 5x310 current waveshape with a short circuit value of 62.5A between all tip and rings connected together and any hand-held part of the EUT (with a minimum of 60 S between surge events)
- ±10 10x700 µS voltage waveshape surge event with an open circuit value of 1.5 kV and a 5x310 current waveshape with a short circuit value of 37.5A between all tip and rings connected together and earth ground connection of the EUT (with a minimum of 60 S between surge events); surge suppressors are allowed to operate
- ±10 10x700 µS voltage waveshape surge event with an open circuit value of 1.5 kV and a 5x310 current waveshape with a short circuit value of 37.5A between all tip and rings connected together and any other conductors that are intended to be connected to other equipment all tied together (with a minimum of 60 S between surge events); surge suppressors are allowed to operate

2) Steady State

- ac test of 1.5 kV is applied between all tip and rings connected together and any hand-held part of the EUT (surge suppressor across the insulation barrier are not removed)
- the ac test of 1 kV is applied between all tip and rings connected together and earth ground connection of the EUT (surge suppressor across the insulation barrier are removed but then must pass impulse test listed above)
- the ac test of 1 kV is applied between all tip and rings connected together and any other conductors that are intended to be connected to other equipment all tied together (surge suppressor across the insulation barrier are removed but then must pass impulse test listed above)

There can be no breakdown of the insulation barrier. Any surge suppressors across the insulation barrier that was removed for the 1 kV steady-state tests but then must comply with the impulse tests.

ANNEX C of UL 60950-1 covers transformers

The secondary side is loaded for maximum heating effect. The maximum working voltage is applied to the primary. The DC peak value of any superimposed ripple shall be included. The permitted temperature limits for the windings depend on the classifications listed at right:

- Class A limit is 150 °C.
- Class B limit is 175 °C.
- Class E limit is 165 °C.
- Class F limit is 190 °C.
- Class H limit is 210 °C.

Regulatory Requirements (continued)

Overvoltage Flowchart

The overvoltage flowchart in Figure 3.19 shows specific guidelines for determining overvoltage requirements applicable to telcom applications that use outside cable exposed to power line fault conditions. These overvoltage events can be the result of

a) contact with a multi-earthed neutral distribution power line (4 kV to approximately 50 kV),

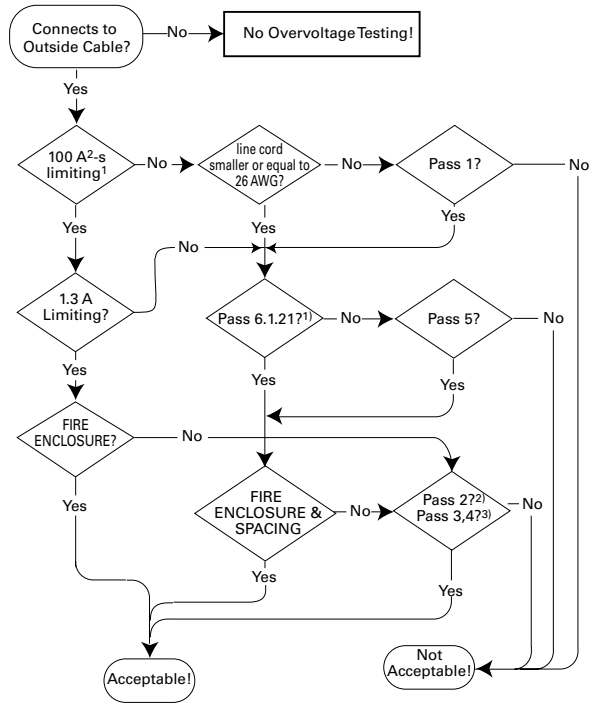
b) induction from a distribution power line fault to earth,

c) EPR (earth potential rise) due to power line fault current flowing to earth, and

d) contact with 120 V power line.

The worse case protection for inside wiring with 3-mil carbon blocks can result in a maximum longitudinal voltage of 600 V. Asymmetrical operation of these carbon blocks result in transverse (differential or metallic) voltages up to this 600 V. Furthermore, a high impedance power line fault to earth can result in a maximum induced current of 2.2A. Induction or EPR events can cause a maximum current event of 7A enduring for up to 5 S. A power line contact with a shielded telephone cable can result in an I^2t of 2,400 A^2-S. A 40 A, 1.5 S event is considered the worst case. A 120 V power line cross with a telephone line can deliver up to 25 A to the telephone wiring, limited by the wiring impedance.

Figure 3.19 Overvoltage Flowchart



Notes:
1) The telephone line is adequately isolated from earth for the operating mode being considered at a voltage of 120 V.
2) Test Condition 2 is not required for equipment containing a method for limiting current to 1.3 A max steady state (e.g., a fuse rated 1.0 A maximum).
3) Test Conditions 3 and 4 are not required for equipment whose application (because of system function, design limitations, etc.) is limited to connections to outside cable not exceeding 1,000 m (for example, equipment that connects to ISDN S/T reference points and certain proprietary telephone sets).

The questions "Passes 1, 2, 3, 4, and 5" shown in Figure 3.19 refer respectively to Tests L1 and M1, L2 and M2, L3 and M3, L4 and M4, and L5 shown in Table 3.53.

These tests are designed to simulate the following:

- Contact with primary power
- Short-term induction as a result of a primary power fault to a multi-earth neutral
- Long duration power fault to Ground
- Direct contact between the power mains and a telecommunications cable

Table 3.53 UL 60950 Overvoltage Test

Test	Voltage (V_{RMS})	Current (A)	Time	Comments
L1	600V	40	1.5 s	
L2	600V	7	5 s	
L3	600V	2.2	See Note 2	Reduce to 135% fuse rating
L4	See Note 1	2.2	See Note 2	Reduce to 135% fuse rating
L5	120V	25	See Note 2	
M1	600V	40	1.5 s	
M2	600V	7	5 s	
M3	600V	2.2	See Note 2	Reduce to 135% fuse rating
M4	See Note 1	2.2	See Note 2	Reduce to 135% fuse rating

Notes:
1 Voltage < conduction voltage of protection
2 Test for 30 minutes or until an open circuit occurs unless it appears possible that risk of fire or safety hazard may result; then continue test until ultimate results are obtained (maximum 7 hours).
General Notes:
- ISDN S/T interface only L1, L2, L5, M1, and M2.
- If Test 3 resulted in open condition, bypass the fuse, reduce current to 135% of the fuse rating and continue the test.
- L4 and M4 are conducted at a voltage level just below Vs only if *SIDACtor*® VS ≥285 V_S.
- For test conditions M1, L1, M5, and L5 a wiring simulator (MDL 2 A fuse) is used.
- Compliance means no ignition or charring of the cheesecloth, and/or wiring simulator does not open.
- Tests 2, 3, and 4 are required only if the unit is not a fire enclosure.
- EUT shall continue to comply with the requirements of Clause 6.2 (Separation requirements and Electric strength requirements) at the conclusion of these overvoltage tests.

Figure 3.20 Metallic Connection Appearances

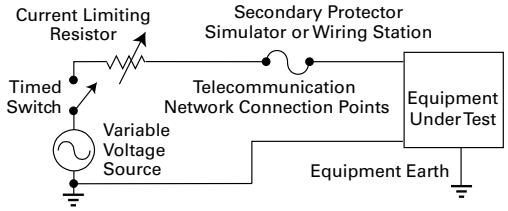
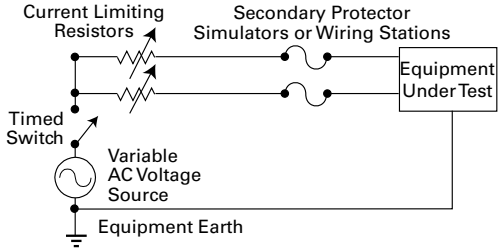


Figure 3.21 Longitudinal Connection Appearances



Revised: 02/23/17

Regulatory Requirements (continued)

Overvoltage Test Procedures

Use the following criteria when applying the overvoltage tests presented in Table 3.53.

1. Test Set-up—Equipment is to be mounted as it is intended to be used. Tests may be conducted on either the equipment as an assembly, individual subassemblies, or a partial assembly containing those components which may be exposed to an overvoltage condition.
2. Indicators—Before testing, two single pieces of cheesecloth are to be wrapped tightly around the assembly, subassembly, or partial assembly. The cheesecloth acts as an indicator for conditions that may result in fire.
3. Line Cords—Equipment with a removable telecommunications line cord is to be connected to the test circuit with a line cord having 0.4 mm (26 AWG) or larger copper wire conductors and not more than 1Ω total resistance.
4. Functional Circuitry—UL mandates that functional circuitry must be used for each overvoltage test conducted. This allows repair or replacement of damaged circuitry before subsequent testing. Alternatively, separate samples may be used for each test.
5. Wiring Simulators—A wiring simulator is used to indicate whether the maximum I2t imposed upon telecommunications wiring has been exceeded. For Tests 1 and 5, a wiring simulator is to be used unless the equipment is specified for use with a suitable secondary protector or a secondary protector simulator. The wiring simulator can consist of one of the following:
   a. 50 mm length of 0.2 mm (32 AWG) bare or enameled solid copper wire (for test condition 1 and 5)
   b. Type MDL-2A fuse (for test condition 1 and 5) or equivalent
   c. Current probe used with a 300 mm length of 0.5 mm (24 AWG) copper wire (for test condition 1 only)

Note: Test conditions 2, 3, and 4 do not require the use of a wiring simulator or a secondary protector simulator. Any secondary protection simulators used in Tests 1 and 5 should be similar to the test fuse used in UL 497A, "*Standard for Secondary Protectors for Communications Circuits*."

Overvoltage Test Compliance

Equipment is deemed compliant if each of the following conditions is met during test:

- Absence of ignition or charring of the cheesecloth indicator (Charring is deemed to have occurred when the threads are reduced to char by a glowing or flaming condition.)
- Wiring simulator does not open during test condition 1 or 5
- For test condition 1, presented in Table 3.53, the integral I^2t measured with a current probe is less than 100 A2s.

After completion of the overvoltage tests, equipment must comply with either the Dielectric Voltage-withstand Test requirements with all components in place or the Leakage Current Test requirements.

Special Considerations Regarding the SIDACtor® Device and UL 60950-1

The epoxy used for *SIDACtor®* devices is UL recognized and the encapsulated body passes UL 94V-0 requirements for flammability. The only specific requirements of UL 60950-1that pertain to the *SIDACtor®* device itself are the impulse test and the mandate that components be UL recognized. All other UL 60950-1 requirements pertain to the equipment being evaluated.

Coax cable distribution Systems

The insulation between the primary circuit and the terminal or lead provided for the connection of a cable distribution system shall pass either:

1) the voltage surge test of UL 60950-1 Clause 7.4.2 for equipment intended to be connected to outdoor antennas; or
2) the impulse test of UL 60950-1 Clause 7.4.3 for equipment intended to be connected to other cable distribution system

If the EUT is intended for connection to both an outdoor antenna and another cable distribution system, it shall pass the tests of both UL 60950-1 Clause 7.4.2 and UL 60950-1 clause 7.4.3.

The following conditioning pulses are applied between:

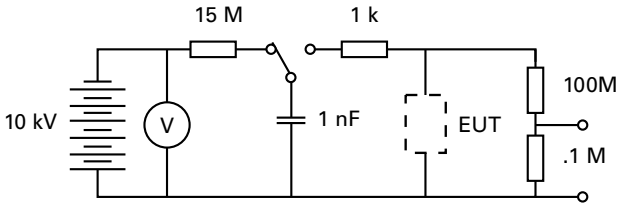
1) the connection points for the cable distribution system all joined together AND
2) the supply circuit terminals joined together with the main protective earthing terminal

At the conclusion of these surges, the electric strength tests are conducted. All components between the connection points for the cable distribution system and the protective earthing terminal are disconnected before these tests are applied.

UL 60950-1 Clause 7.4.2

The 10 kV surge generator as defined in IEC 60065 (example shown in figure 3.22) is used to apply 50 surges to the EUT. These surges are applied at a maximum rate of 12 pulses per minute.

FIgure 3.22 IEC 60065 Surge Generator



UL 60950-1 Clause 7.4.3

1) ±10 10x700 µS voltage waveshape surge event with an open circuit value of 5 kV and a 5x310 current waveshape with a short circuit value of 125A for power-fed repeaters

2) ±10 10x700 µS voltage waveshape surge event with an open circuit value of 4 kV and a 5x310 current waveshape with a short cir 100A for all other equipment

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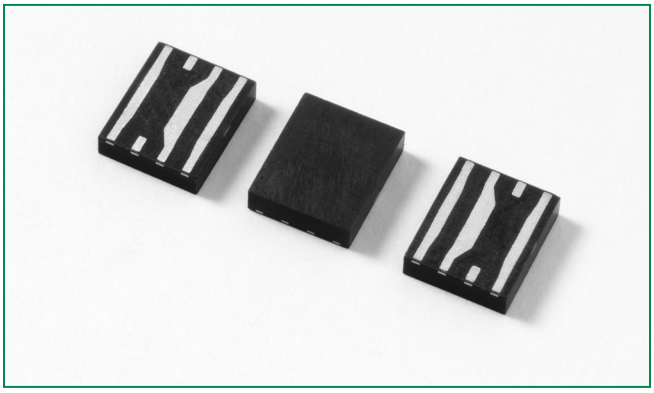
SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Littelfuse
Expertise Applied | Answers Delivered

SDP Biased Series - 5x6 QFN

HF RoHS Pb e3



Description

This new SDP Biased series provides overvoltage protection for applications such as VDSL2, ADSL2, and ADSL2+ with minimal effect on data signals. This latest silicon design innovation results in a capacitive loading characteristic that is compatible with these high bandwidth applications. This surface mount QFN package provides a surge capability that exceeds most worldwide standards and recommendations for lightning surge withstand capability of secondary protectors.

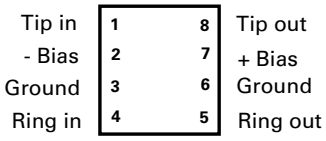
Agency Approvals

Agency	Agency File Number
UL	E133083

Features & Benefits

- Compatible with VDSL2 (30MHz)
- Balanced overvoltage protection
- Low distortion
- Low insertion loss
- Low profile
- SO-8 footprint compatible
- Fails short circuit when surged in excess of ratings
- 2nd level interconnect is Pb-free per IPC/JEDEC J-STD-609A.01

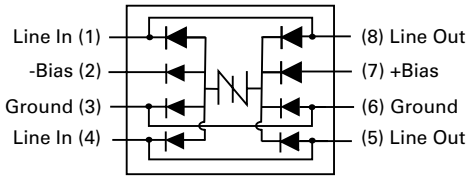
Pinout Designation



Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- IEC 61000-4-5
- GR 1089 Inter-building
- GR 1089 Intra-building
- YD/T 1082
- YD/T 993
- YD/T 950

Schematic Symbol



Electrical Characteristics

Part Number	Marking	V_{DRM}@I_{DRM}=5µA	V_S@100V/µs	I_H	I_S	I_T	V_T@I_T=2.2 Amps	Capacitance
		V min	V max	mA min	mA max	A max	V max	
SDP0080Q38CB	SDP-8C	6	25	50	800	2.2	8	See Capacitance vs Voltage Chart
SDP0220Q38CB	SDP02C	16	30	50	800	2.2	8	
SDP0640Q38CB	SDP06C	58	77	150	800	2.2	8	
SDP0720Q38CB	SDP07C	65	88	150	800	2.2	8	
SDP0900Q38CB	SDP09C	75	98	150	800	2.2	8	
SDP1100Q38CB	SDP11C	90	130	150	800	2.2	8	
SDP1300Q38CB	SDP13C	120	160	150	800	2.2	8	
SDP1800Q38CB	SDP18C	170	220	150	800	2.2	8	
SDP2600Q38CB	SDP26C	220	300	150	800	2.2	8	
SDP3100Q38CB	SDP31C	275	350	150	800	2.2	8	
SDP3500Q38CB	SDP35C	320	400	150	800	2.2	8	

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Devices are bi-directional (unless otherwise noted).
- Part with * is under development.

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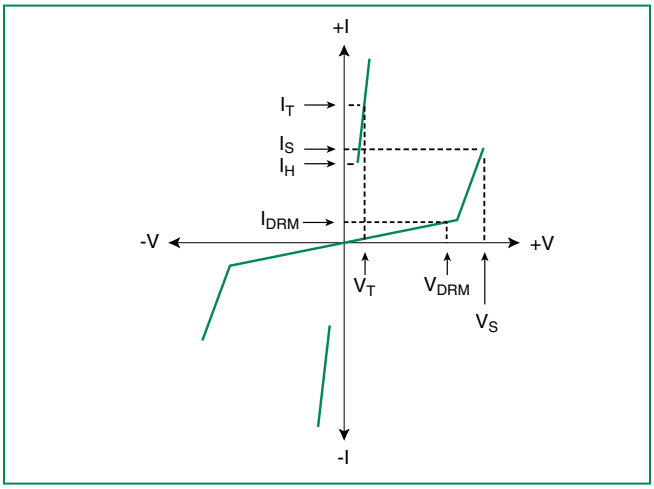
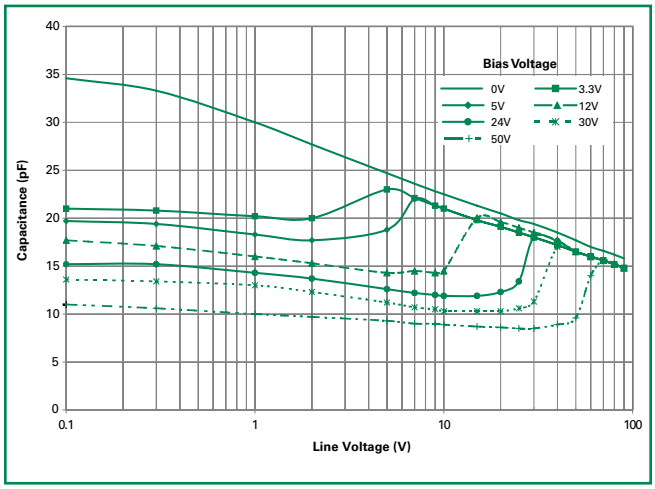
SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

V-I: Characteristics



Capacitance vs. Voltage*



* Bias voltage must be lower than V_{DRM}

50/60Hz Ratings

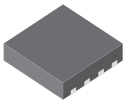
Parameter Name	Test Conditions	Value	Units
I_{TSM} Maximum non-reptitive on-state current, 50/60Hz	0.5s	6.5	A
	1s	4.6	
	2s	3.4	
	5s	2.3	
	30s	1.3	
	900s	0.73	

Surge Ratings

Series	I_{PP}				I_{TSM}
	2x10µs	1.2x50µs/8x20µs	10x700/5x310µs	10x1000µs	$600V_{RMS}$ 1 cycle
	A min	A min	A min	A min	A_{RMS}
C	500	400	200	100	30

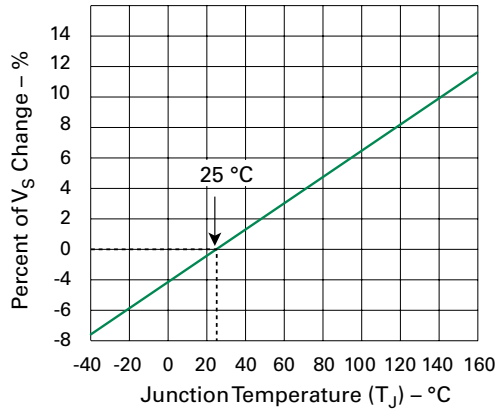
Notes:
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The device must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

Thermal Considerations

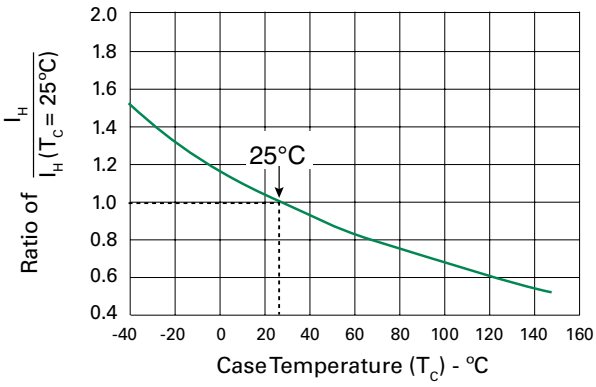
Package	Symbol	Parameter	Value	Unit
 5x6 QFN	T_J	Junction Temperature	-40 to +150	°C
	T_{STG}	Storage Temperature Range	-40 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	100	°C/W

Revised: 02/23/17

Normalized V_S Change vs. Junction Temperature



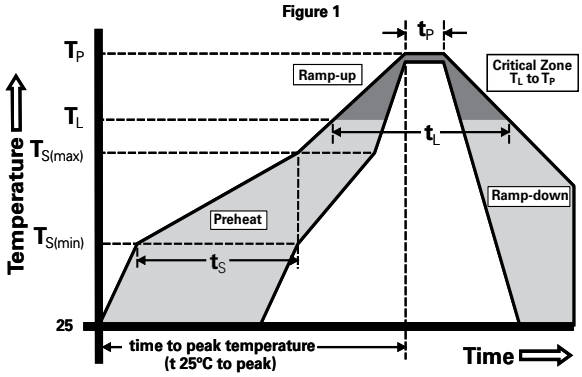
Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification 94V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

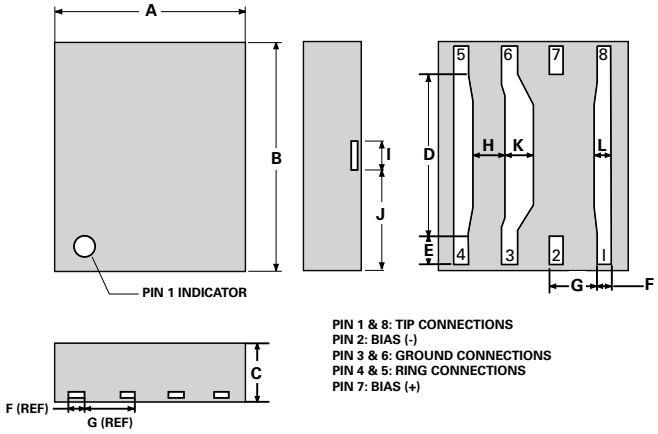
Additional Information

Datasheet | **Resources** | **Samples**

Revised: 02/23/17

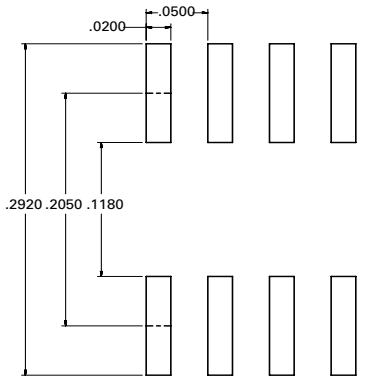
SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Dimensions — 5x6 QFN



Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	0.187	0.207	4.745	5.253
B	0.226	0.246	5.745	6.253
C	0.054	0.064	1.374	1.628
D	0.165	0.171	4.199	4.351
E	0.027	0.033	0.686	0.838
F	0.011	0.017	0.279	0.432
G	0.047	0.053	1.194	1.346
H	0.032	0.038	0.800	0.953
I	0.027	0.033	0.686	0.838
J	0.100	0.106	2.540	2.692
K	0.027	0.033	0.686	0.838
L	0.015	0.021	0.381	0.533

5x6 QFN Solder Pad Layout

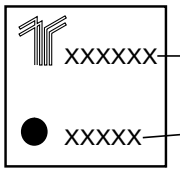


Part Numbering

SDP xxx 0 Q38 C B

- **TYPE** — SIDACtor DSL Protector
- **MEDIAN VOLTAGE**
- **CONSTRUCTION VARIABLE**
- **PACKAGE TYPE**
- **I_{PP} RATING**
- **BIASED**

Part Marking



- XXXXXX — Part Marking Code (Refer to Electrical Characteristics Table)
- XXXXX — Date Code

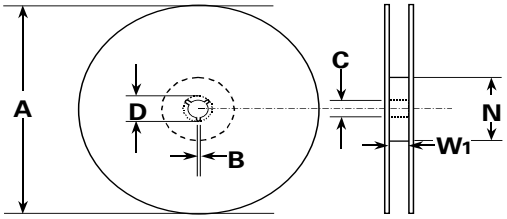
Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
Q38	5x6x1.5 QFN Tape and Reel Pack	4000	N/A	EIA-481-D

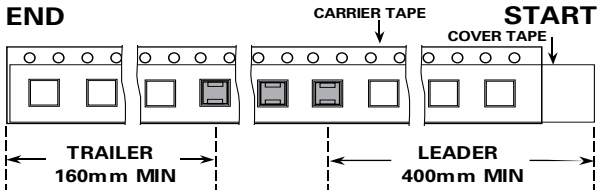
Revised: 02/23/17

Tape and Reel Specifications — 5x6 QFN

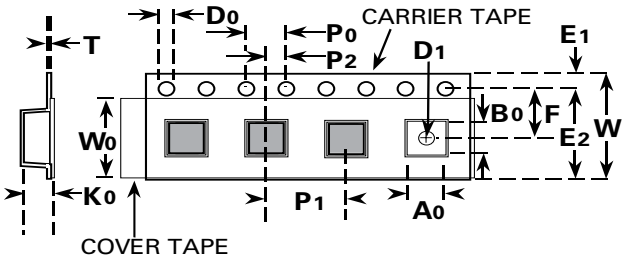
Reel Dimension



Tape Leader and Trailer Dimensions



Tape Dimension Items

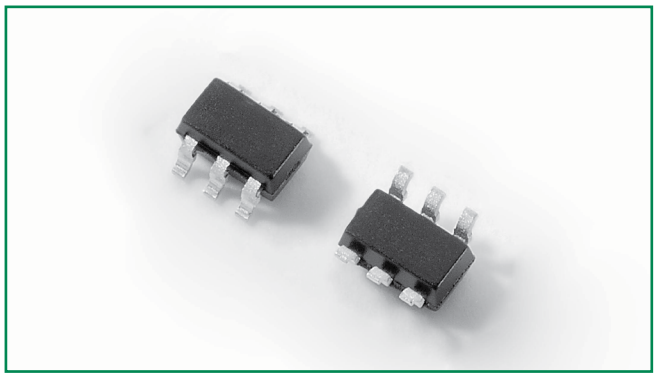


Symbols	Description	Inches		Millimeters	
		Min	Max	Min	Max
A	Reel Diameter	N/A	12.992	N/A	330.0
B	Drive Spoke Width	0.059	N/A	1.50	N/A
C	Arbor Hole Diameter	0.504	0.531	12.80	13.50
D	Drive Spoke Diameter	0.795	N/A	20.20	N/A
N	Hub Diameter	1.969	N/A	50.00	N/A
W_1	Reel Inner Width at Hub	0.488	0.567	12.40	14.40
A_0	Pocket Width at Bottom	0.204	0.212	5.20	5.40
B_0	Pocket Length at Bottom	0.244	0.252	6.20	6.40
D_0	Feed Hole Diameter	0.059	0.063	1.50	1.60
D_1	Pocket Hole Diameter	0.059	N/A	1.50	N/A
E_1	Feed Hole Position 1	0.065	0.073	1.65	1.85
E_2	Feed Hole Position 2	0.400	0.408	10.15	10.35
F	Feed Hole Center - Pocket Hole Center 2	0.212	0.220	5.40	5.60
K_0	Pocket Depth	0.067	0.075	1.70	1.90
P_0	Feed Hole Pitch	0.153	0.161	3.90	4.10
P_1	Component Spacing	0.311	0.319	7.90	8.10
P_2	Feed Hole Center - Pocket Hole Center 1	0.077	0.081	1.90	2.10
T	Carrier Tape Thickness	0.010	0.014	0.25	0.35
W	Embossed Carrier Tape Width	0.460	0.484	11.70	12.30
W_0	Cover Tape Width	0.358	0.366	9.10	9.30

Littelfuse
Expertise Applied | Answers Delivered

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

SDP Biased Series - SOT23-6



Description

This new SDP Biased series provides overvoltage protection for applications such as VDSL2, ADSL2, and ADSL2+ with minimal effect on data signals. This silicon design innovation results in a capacitive loading characteristic that is compatible with these high bandwidth applications. This surface mount SOT23-6 package provides a surge capability that exceeds most worldwide standards and recommendations for lightning surge withstand capability of tertiary protectors.

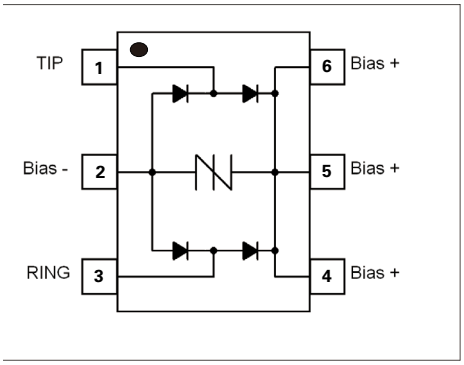
Features & Benefits

- Compatible with VDSL2 (30MHz) and with G.fast (106MHz)
- Balanced overvoltage protection
- Low distortion
- Low insertion loss
- Low profile
- Response time under 500ns
- RoHS Compliant
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Agency Approvals

Agency	Agency File Number
UL	E133083

Pinout Designation & Schematic Symbol



Applicable Global Standards

- ANSI C62.41
- IEC 61000-4-12
- IEC 61000-4-5, 30A (t_P=8/20µs) 2nd edition
- IEC 61000-4-2 level 4
  -- 15kV (air discharge)
  -- 8kV (contact discharge)

Additional Information

Datasheet | Resources | Samples

Absolute Maximum Ratings between pin1 and pin 3, Ta= 25°C (Unless otherwise noted)

Part Number	Marking	Maximum Junction Temperature	Storage Temperature Range	I_{pp} 8/20µs
		°C	°C	A Max
SDP0240T023G6RP	P24	150	-65 to 150	30 [1]

Notes:

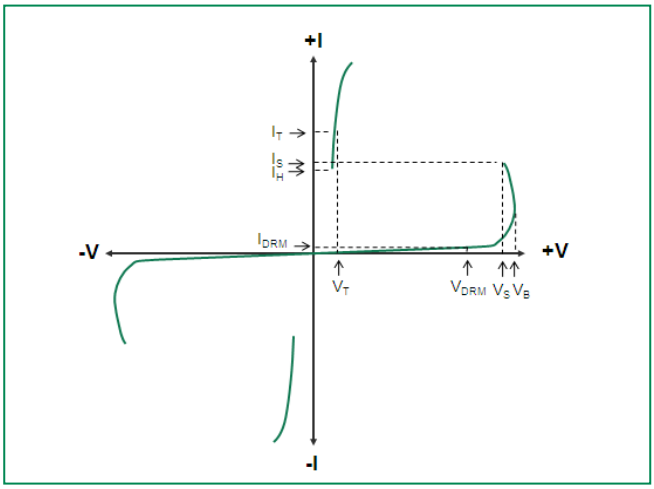
1. The device must be in thermal equilibrium at 25°C

Electrical Characteristics between pin 1 and pin 3, Ta = 25°C

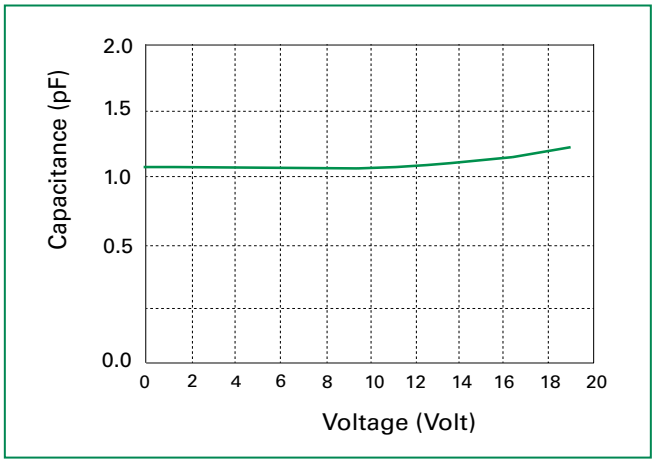
Part Number	Marking	V_{DRM} @I_{DRM}=100nA	I_{DRM} @V_{DRM}=19V	V_S@1V/µs	I_H	I_S	Co@f=1MHz,2V	Delta Co@ Line Bias = 1 V to 19 V
		V min	pA typ	V max	mA typ	mA min	pF max	pF max
SDP0240T023G6RP	P24	19	300	29	40	10	3.0	0.5

Revised: 02/23/17

V-I: Characteristics



Typical capacitance against line voltage (without external bias)



Surge Ratings

Series	I_{PP}
	1.2/50µs [1] / 8/20µs [2]
	A min
G	30

Notes:

1 Voltage waveform in µs
2 Current waveform in µs

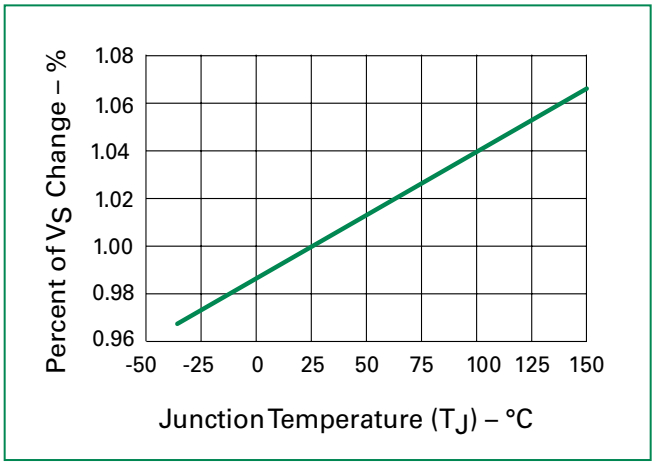
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- The component must be in thermal equilibrium at 25°C.

Thermal Information

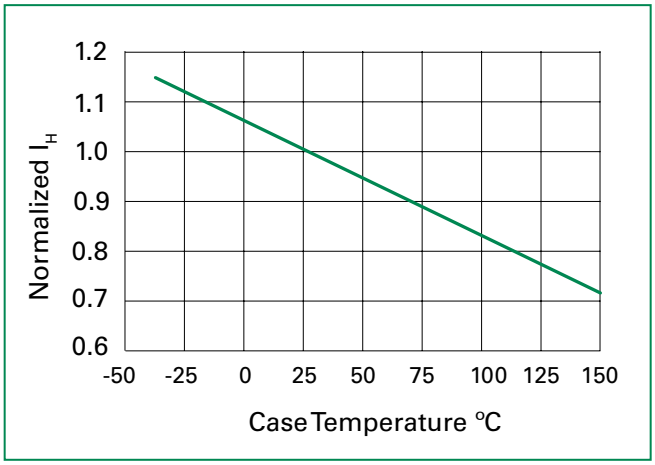
Parameter	Rating	Units
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 10s)	260	°C

Revised: 02/23/17

Normalized V_S Change vs. Junction Temperature

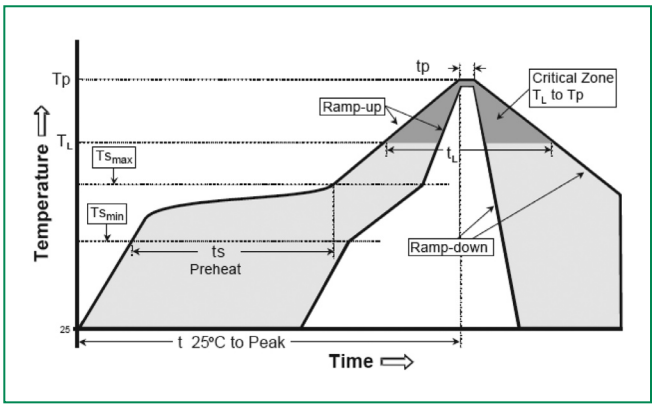


Normalized Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		250(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		20-40 secs.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		260°C



Revised: 02/23/17

Physical Specifications

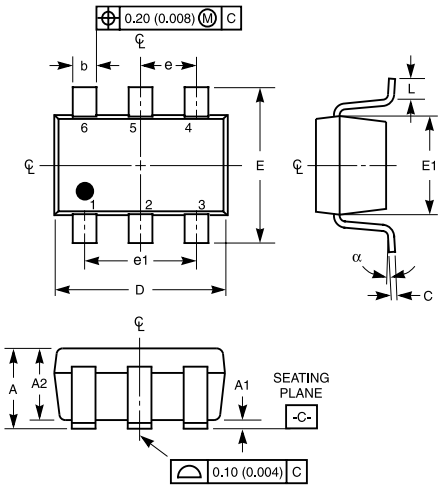
Lead Plating	SOT23: Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	V-0

Notes:
1. All dimensions are in millimeters.
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC MO-178
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte tine

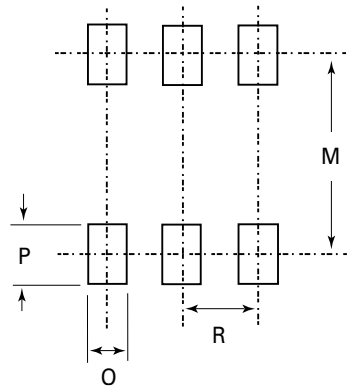
Environmental Specifications

Temp Cycling	Mil-STD-883, Method 1010.8 Condition C, -65°C to +150°C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Bias Humidity	JESD 22-A101 85°C , 85°CRH. 50V 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Pressure Cooker	JEDEC 22-A102 No Bias, 121°C, 100%RH 96Hrs/192Hrs. 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
High Temp Storage	JESD 22-A103 Con B. 150°C, no bias 1000Hrs
HTRB	JESD 22-108 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Thermal Shock	Mil-STD-883, Method 1011.9 Condition A, 0°C to 100°C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
C-SAM	As per flow, JSTD-020 pre&post preconditioning test.
Wet Humidity (Tin only)	JESD 201 standard: 55°C/85%RH

Dimensions - SOT23-6



Recommended Solder Pad Layout



Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.041	0.057	1.050	1.450
A1	0.000	0.006	0.000	0.150
A2	0.041	0.051	1.050	1.300
b	0.014	0.020	0.350	0.508
C	0.004	0.008	0.090	0.200
D	0.110	0.118	2.800	3.000
E	0.102	0.118	2.600	3.000
E1	0.057	0.069	1.450	1.750
e	0.037 (BSC)		0.950 (BSC)	
e1	0.071	0.075	1.800	1.900
L (note 4.5)	0.004	0.023	0.100	0.600
N (note 6)	6		6	
α	0°C	10°C	0°C	10°C
M	-	0.102	-	2.590
O	-	0.027	-	0.690
P	-	0.039	-	0.990
R	-	0.038	-	0.950

Notes:
1. Dimensioning and tolearances per ANSI 14.5M-1982.
2. Package conforms to EIAJ SC-74 (1992)
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Foot lenth L measured at reference to seatng plane.
5. "L" is the length of flat foot surface for soldering to substrate.
6. "N" is the number of terminal positions.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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SIDACtor® Protection Thyristors
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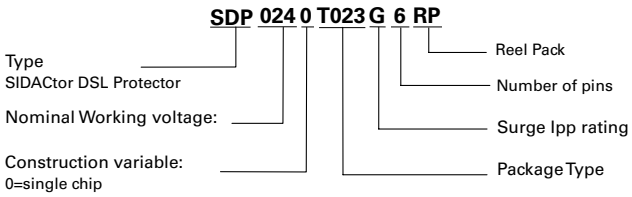
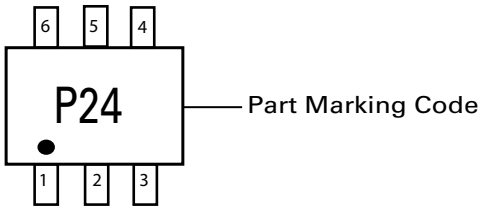
Part Numbering



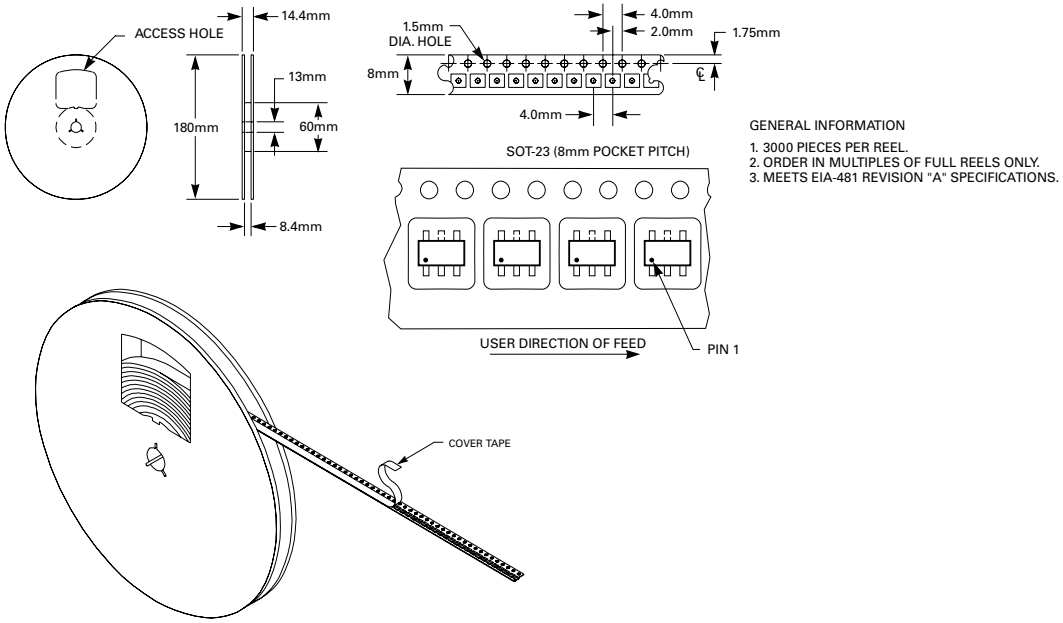
Part Marking



Packing Options

Package Type	Description	Quantity
SOT23-6	Tape and Reel	3000

Embossed Carrier Tape & Reel Specification - SOT23-6

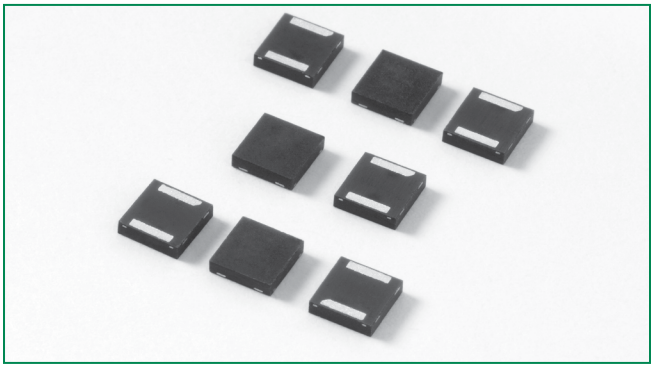


SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Littelfuse
Expertise Applied | Answers Delivered

SDP TwinChip™ Series - 3x3 QFN

HF RoHS



Description

The SDP TwinChip™ Series provides overvoltage protection on the secondary side of the coupling transformer used in xDSL driver circuits. This SDP0242Q12F provides a fast switching, robust, solution that is referenced to neither ground nor power. This prevents the surge events from the being dumped into these rails. The integrated TwinChip™ design reduces any negative solid-state effects on the broadband signals.

Agency Approvals

Agency	Agency File Number
	E133083

Features & Benefits

- Differential protection
- Low insertion loss
- Low
- Low profile
- Small 3x3mm footprint
- Designed for 16-24 V line drivers
- 80A 8/20µs surge rating
- 2nd level interconnect is Pb-free per IPC/JEDEC J-STD-609A.01

Pinout Designation

Not Applicable

Schematic Symbol

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-5
- YD/T 1082
- YD/T 993
- YD/T 950

Electrical Characteristics

Part Number	Marking	V_{DRM} @Idrm=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @IT=2.2 amps	@1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
SDP0242Q12FLRP	DP24F	16	43	30	800	2.2	8	10	15

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Devices are bi-directional (unless otherwise noted).

Additional Information

Datasheet | **Resources** | **Samples**

Revised: 02/23/17

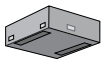
SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Surge Ratings

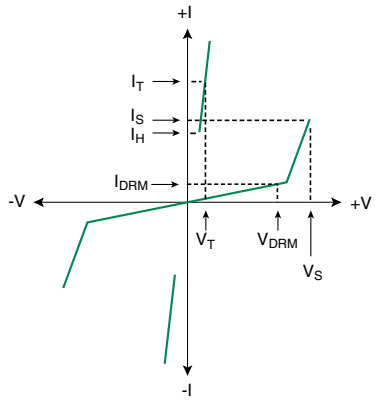
Series	I_{PP}				I_{TSM}
	2x10µs	1.2x50µs/8x20µs	10x700/5x310µs	10x1000µs	50 / 60 Hz
	A min	A min	A min	A min	A min
F	100	80	37.5	30	15

Notes:
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The device must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

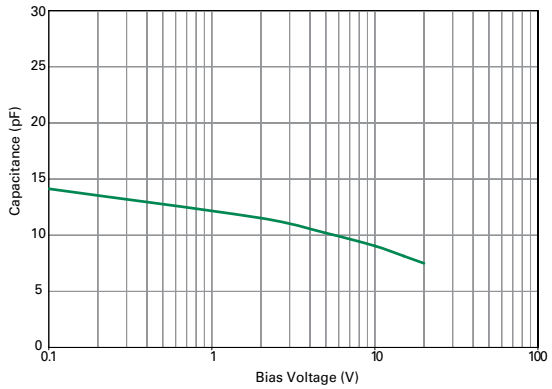
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
3x3 QFN 	T_J	Junction Temperature	-40 to +150	°C
	T_{STG}	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	100	°C/W

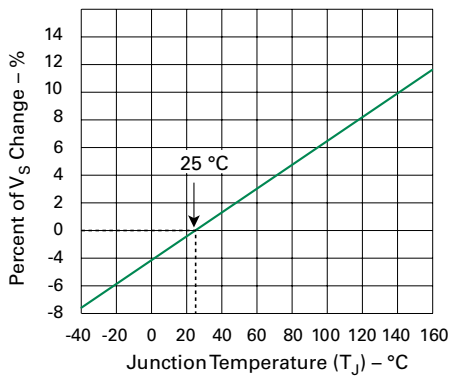
V-I Characteristics



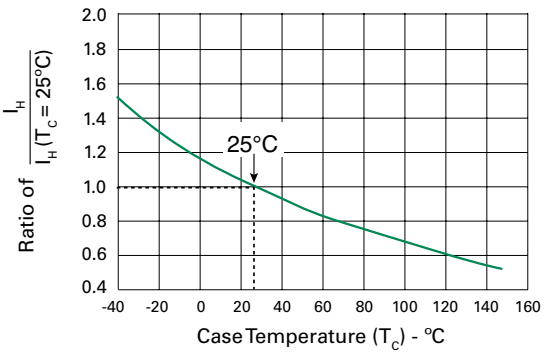
Capacitance and Bias Voltage



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

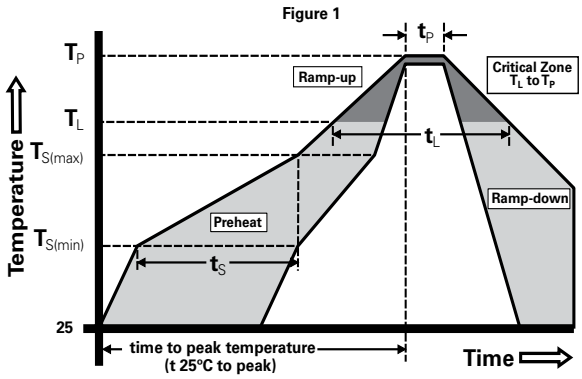


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



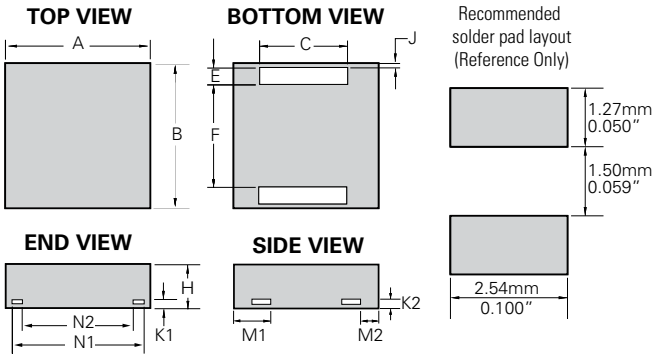
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification 94V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Dimensions — 3x3 QFN

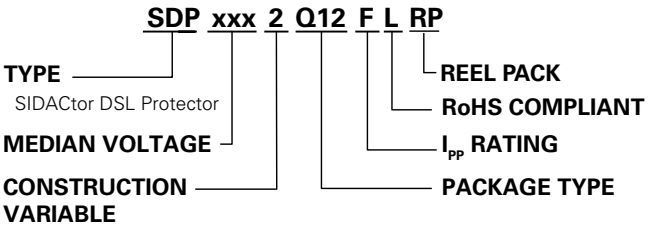


Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.114	0.122	2.900	3.100
B	0.114	0.122	2.900	3.100
C	0.077	0.081	1.950	2.050
E	0.013	0.017	0.335	0.435
F	0.078	0.082	1.980	2.080
H	0.037	0.041	0.950	1.050
J	0.002	0.006	0.050	0.150
K1	0.006	0.001	0.150	0.250
K2	0.006	0.001	0.150	0.250
M1	0.028	0.031	0.700	0.800
M2	0.013	0.017	0.330	0.430
N1	0.097	0.101	2.470	2.570
N2	0.084	0.088	2.130	2.230

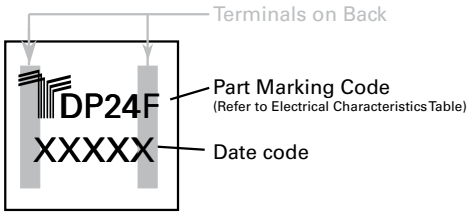
Revised: 02/23/17

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Part Numbering



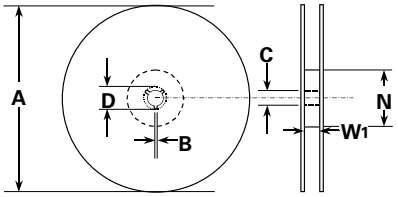
Part Marking



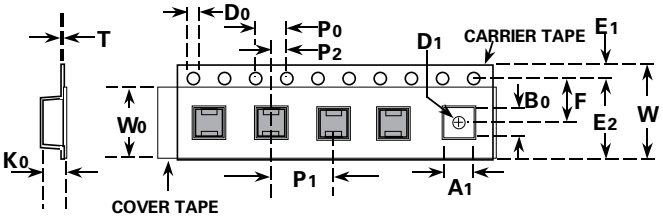
Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
Q12	3x3 QFN Tape and Reel	5000	RP	EIA-481-D

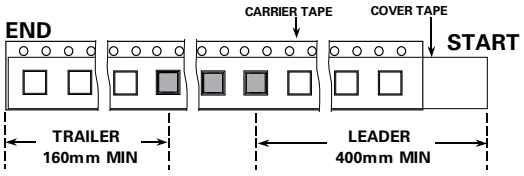
Tape and Reel Specifications — 3x3 QFN



Reel Dimension



Tape Dimension Items



Leader and Trailer dimension of the tape

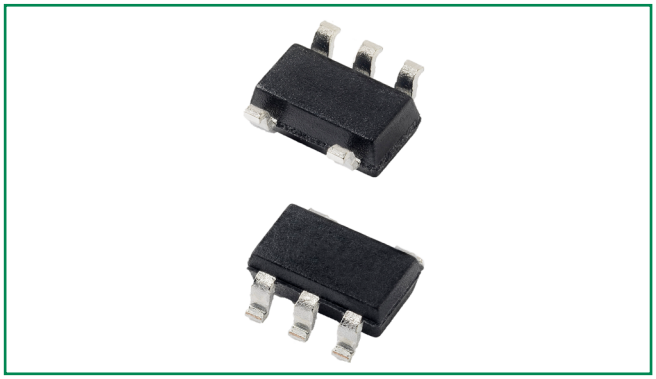
Symbols	Description	Inches		Millimeters	
		Min	Max	Min	Max
A	Reel Diameter	N/A	12.992	N/A	330.0
B	Drive Spoke Width	0.059	N/A	1.50	N/A
C	Arbor Hole Diameter	0.504	0.531	12.80	13.50
D	Drive Spoke Diameter	0.795	N/A	20.20	N/A
N	Hub Diameter	1.969	N/A	50.00	N/A
W_1	Reel Inner Width at Hub	0.488	0.567	12.40	14.40
A_0	Pocket Width at Bottom	0.126	0.134	3.20	3.40
B_0	Pocket Length at Bottom	0.126	0.134	3.20	3.40
D_0	Feed Hole Diameter	0.059	0.063	1.50	1.60
D_1	Pocket Hole Diameter	0.059	N/A	1.50	N/A
E_1	Feed Hole Position 1	0.065	0.073	1.65	1.85
E_2	Feed Hole Position 2	0.400	0.408	10.15	10.35
F	Feed Hole Center - Pocket Hole Center 2	0.215	0.219	5.45	5.55
K_0	Pocket Depth	0.039	0.051	1.00	1.30
P_0	Feed Hole Pitch	0.153	0.161	3.90	4.10
P_1	Component Spacing	0.311	0.319	7.90	8.10
P_2	Feed Hole Center - Pocket Hole Center 1	0.077	0.081	1.90	2.06
T	Carrier Tape Thickness	0.010	0.014	0.25	0.35
W	Embossed Carrier Tape Width	0.453	0.484	11.50	12.30
W_0	Cover Tape Width	0.358	0.366	9.10	9.30

SIDACtor® Protection Thyristors
Teccor® brand SIDACtor® DSL Protection Devices

Littelfuse
Expertise Applied | Answers Delivered

SDP Series - SOT23-5

HF RoHS



Description

This new SIDACtor series thyristors are targeted for the tertiary or line driver side protection position for VDSL2+, ADSL2 applications and general I/O protection functions. This new low capacitance over voltage protection does not require a bias voltage and is sufficiently robust for the chip-side position behind the coupling transformer.

This SOT23-5 solution, with its flow-through design, minimizes PCB trace layout routing, while its four different stand-off voltage values offer compatibility with a variety of line drivers. Its low capacitance makes it compatible with ADSL2 and VDSL2, and the 30MHz bandplan of VDSL2+.

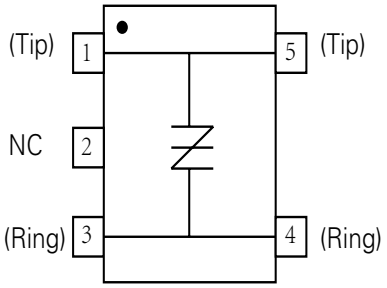
Agency Approvals

Agency	Agency File Number
	E133083

Features & Benefits

- Lower overshooting protection than clamping
- SOT23-5 surface mount package
- Low insertion loss
- Low capacitance
- Bidirectional transient voltage protection
- Robust surge rating
- Starts to switch in nanoseconds
- RoHS compliant and Halogen-Free
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Schematic Symbol



Applicable Global Standards

- YD/T 950
- YD/T 993
- YD/T 1082
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-2
- IEC 61000-4-5 2nd edition
- ITU K.20/21/45 Basic Level
- ITU K.20/21/45 Enhanced Level
- TIA-968-A
- TIA-968-B

Additional Information

Datasheet | **Resources** | **Samples**

Electrical Characteristics

Part Number	Marking	V_{DRM}@I_{DRM}=5µA	V_S@250V/µs	I_H	I_S	V_T@I_T=1.0 Amps	Co@f=1MHz,2V	
		V min	V max	mA typ	mA max	V max	pF typ	pF max
SDP0080T023G5RP	P8G	8	15	30	500	4.0	8.0	9.0
SDP0120T023G5RP	P12G	12	20	30	500	4.0	7.8	9.0
SDP0180T023G5RP	P18G	18	25	30	500	4.0	7.3	8.3
SDP0240T023G5RP	P24G	24	35	30	500	4.0	5.7	6.5

Notes:

- All measurement are made at an ambient temperature of 25°C.
- Ipp applies to -40°C through +85°C temperature range.
- Ipp is repetitive surge rating and is guaranteed for the life of the product.
- SIDACtor components are bidirectional. All electrical parameters and surge rating apply to forward and reverse polarities.

Revised: 02/23/17

SIDACtor® Protection Thyristors
Teccor® brand SIDACtor® DSL Protection Devices

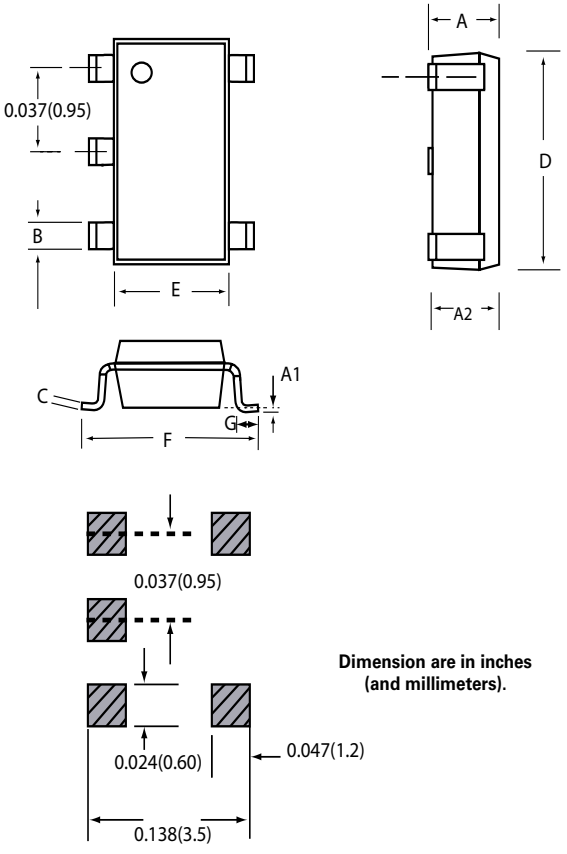
Maximum Ratings

Parameter Name	Symbol	Test Conditions		Value		Units
Lightning surge waveforms	I_{pp}	8/20[1] 1.2/50[2]	min	SDP0080T023G5RP	50	A
				SDP0120T023G5RP	70	
				SDP0180T023G5RP	70	
				SDP0240T023G5RP	70	
		5/310[1] 10/700[2]	min		20	
				min	max	
Operating Free Temperature Range	T_A			-40	+85	°C
Junction temperature	T_J			-40	+150	°C
Storage temperature	T_{STG}			-40	+150	°C

Notes:
1. Voltage waveform in µs
2. Current waveform in µs
- The device also complies with IEC 61000-4-2 ESD ±15kV (air discharge), ±8 kV(contact discharge) and IEC 61000-4-4 EFT 40A(5/50nS) in equipment level ESD test when used behind the xDSL transformer.
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C
- The lightning surge may be repeated after the device returns to its initial conditions.

Mechanical dimensions, recommended layout dimensions

The epoxy meets UL 94V-0 ratings.

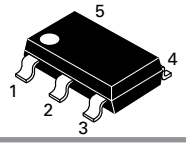


Dimension are in inches (and millimeters).

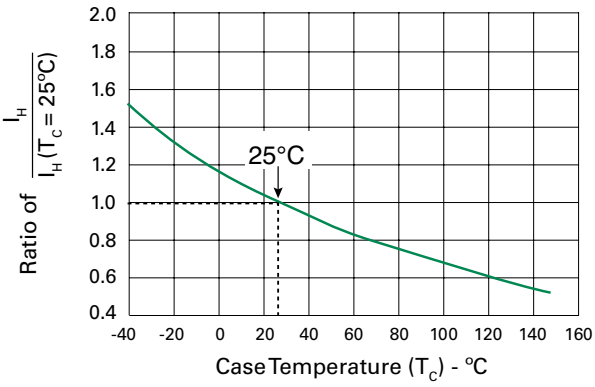
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	0.035	0.057	0.90	1.45
A1	0	0.004	0	0.10
A2	0.035	0.051	0.90	1.30
B	0.014	0.020	0.35	0.50
C	0.004	0.008	0.09	0.20
D	0.11	0.118	2.80	3.00
E	0.059	0.069	1.50	1.75
F	0.102	0.118	2.6	3.00
G	0.004	0.024	0.10	0.60

Revised: 02/23/17

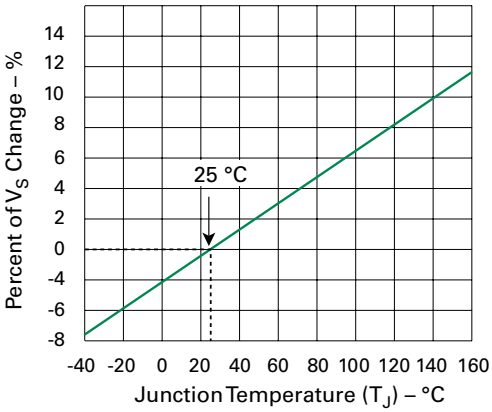
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_{STG}	Storage Temperature Range	-40 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	120	°C/W

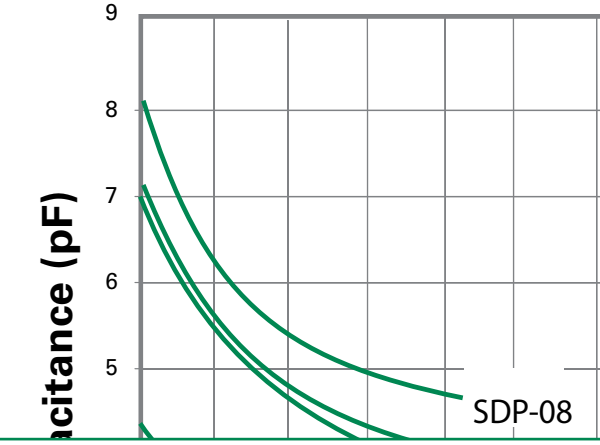
Holding Current vs. Case Temperature



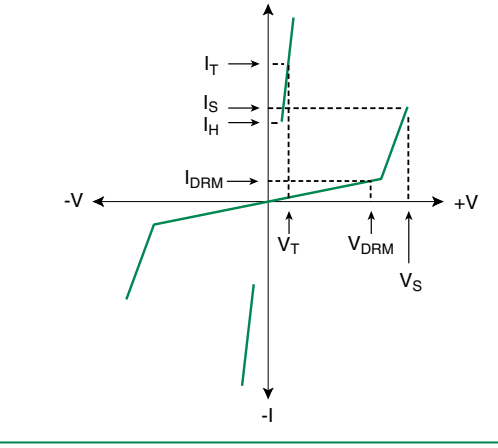
V_S vs. Junction Temperature



Capacitance vs. Bias Voltage



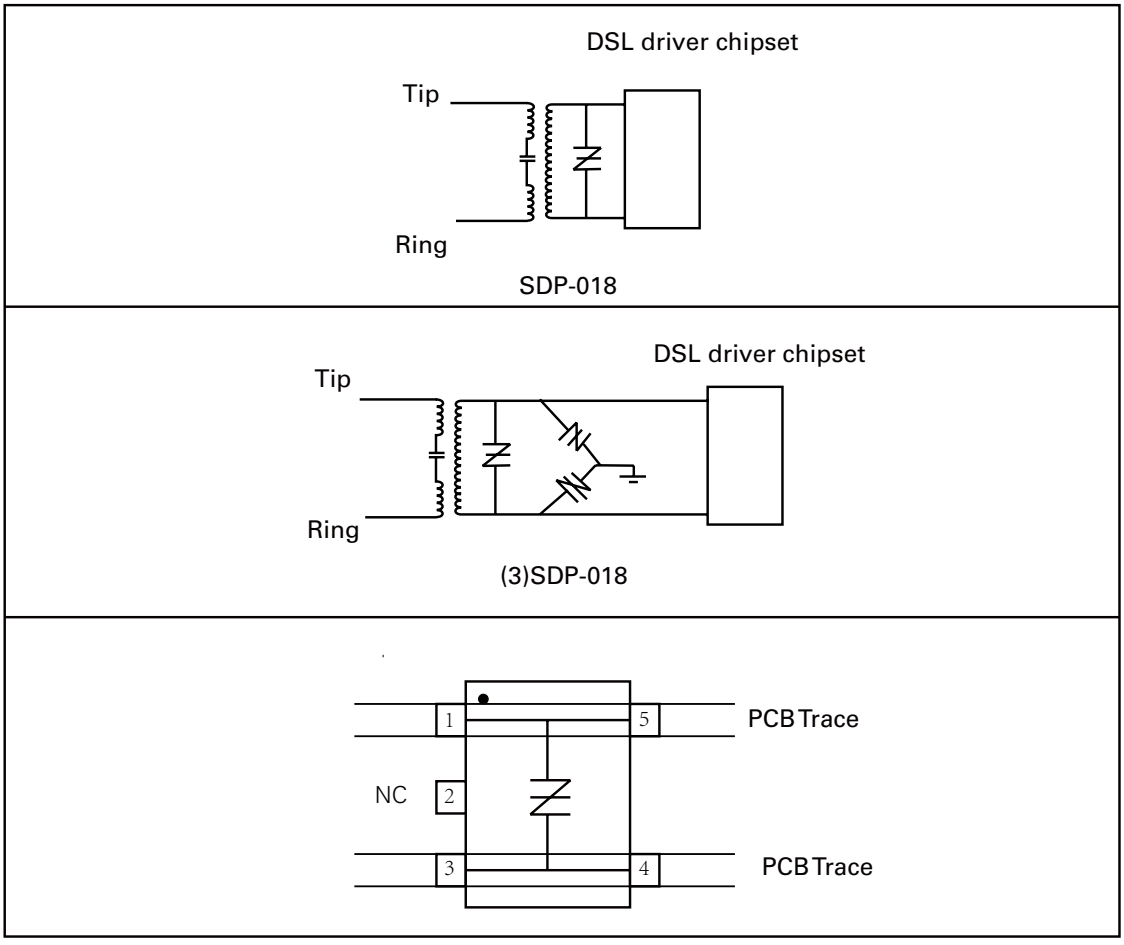
V-I Characteristics



Revised: 02/23/17

SDP-xxx Application example

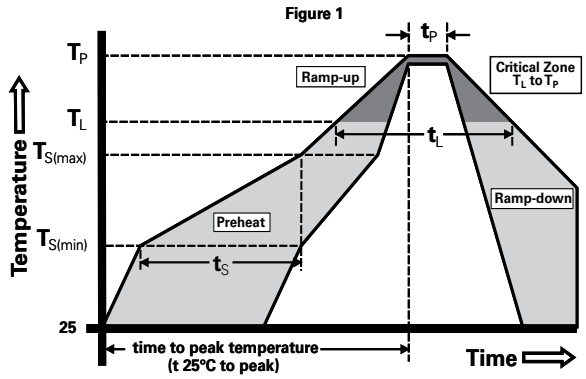
The following schematics show alternate protection solutions for a typical DSL interface that connects to outside wiring. This surface mount SOT23-5 chip-side solution provides a minimum footprint solution appropriate for high density card designs. The SDP-xxx0T023 will protect the interface from lightning induced surges on the chip-side of the coupling transformer. This tertiary protector may be preceded by line-side protection such as the TeleLink over-current protector and the SDP3500Q38CB overvoltage protector. GDTs may also be used on the line side of the coupling transformer. The flow-through design of the SOT23-5 package is illustrated below. If the inter winding capacitance of the transformer is allowing some common mode events to get coupled across, then the SDP-xxx0T023 can be placed in a three chip mode, as shown below for additional chip-side protection.



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Terminal Material	100% Matte-Tin Plated
Solderability	EIA J-STD-002, TEST A.

Environmental Specifications

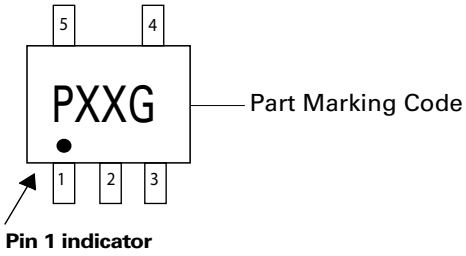
Temp Cycling	Mil-STD-883, Method 1010.8 Condition C, -65°C to +150°C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Bias Humidity	JESD 22-A101 85°C , 85°CRH. 50V 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Pressure Cooker	JEDEC 22-A102 No Bias, 121°C, 100%RH 96Hrs/192Hrs. 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
High Temp Storage	JESD 22-A103 Con B. 150°C, no bias 1000Hrs
HTRB	JESD 22-108 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Thermal Shock	Mil-STD-883, Method 1011.9 Condition A, 0°C to 100°C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
C-SAM	As per flow, JSTD-020 pre&post preconditioning test.
Wet Humidity (Tin only)	NEMI standard: 60°C/93%RH

Part Numbering

SDP xxx 0 T023 G 5 RP

- Type: SIDACtor DSL Protector
- Nominal Working voltage: 008=8V, 012=12V, 018=18V, 024=24V
- Construction variable: 0=single chip
- Package: T023=SOT23-5
- Surge Ipp rating
- Number of pins
- Packing Option: RP: Reel Pack

Part Marking



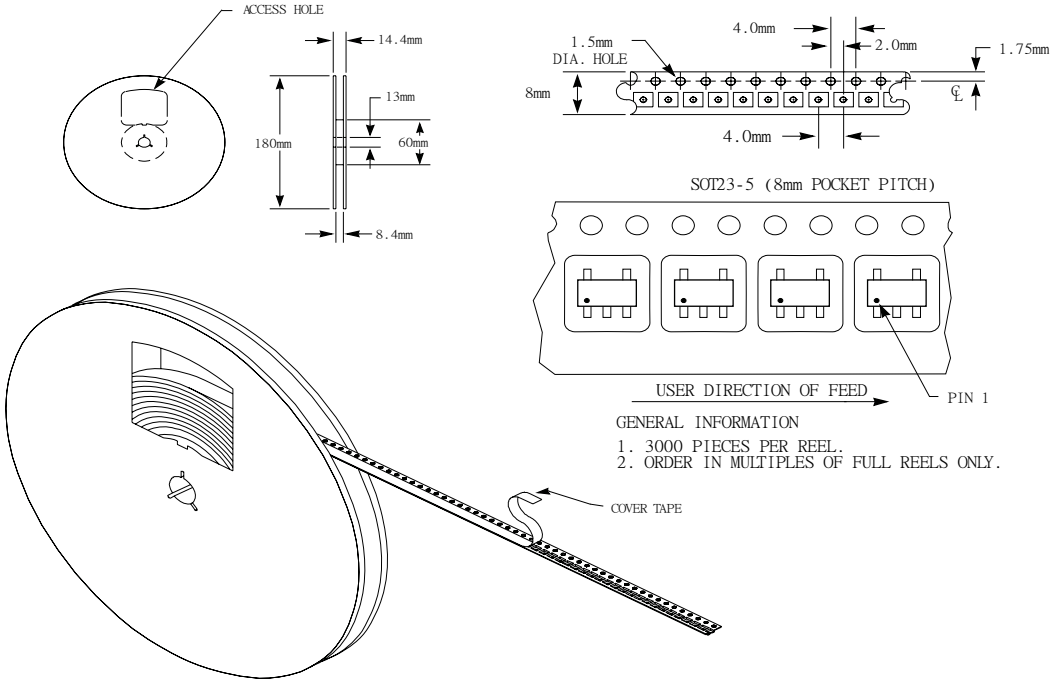
Revised: 02/23/17

Packing Options

Package Type	Description	Quantity	Added Suffix	Min. Order Qty.	Industry Standard
T023	SOT23-5 Tape & Reel Pack	3000	RP	3000	EIA-481-A

Tape and Reel Specification — SOT23-5

8mm TAPE AND REEL

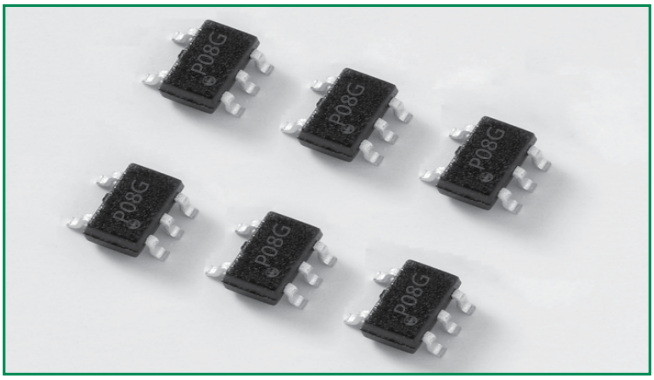


SIDACtor® Protection Thyristors
Teccor® brand SIDACtor® DSL Protection Devices

Littelfuse
Expertise Applied | Answers Delivered

P0080T023G5

HF RoHS



Description

This new P0080T023G5 is targeted for the tertiary or line driver side protection position for VDSL2+ and ADSL2+ applications. This new low capacitance over voltage protection does not require a bias voltage and is sufficiently robust for the chip-side position behind the coupling transformer. This SOT23-5 solution, with its flow-through design, minimizes PCB trace layout routing makes it compatible with a variety of line drivers. Its low capacitance makes it compatible with ADSL2 and VDSL2, and the 30MHz bandplan of VDSL2+.

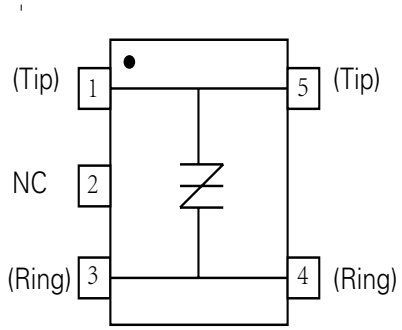
Agency Approvals

Agency	Agency File Number
	E133083

Features & Benefits

- Lower overshoot protection than clamping
- SOT23-5 surface mount package
- Low insertion loss
- Low capacitance
- Bidirectional transient voltage protection
- Robust surge rating
- RoHS compliant
- 2nd level interconnect is Pb-free per IPC/JEDEC J-STD-609A.01

Schematic Symbol



Protection solution to meet

- YD/T 950
- YD/T 993
- YD/T 1082
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-2
- IEC 61000-4-5
- ITU K.20/21 Basic Level
- ITU K.20/21 Enhanced Level
- TIA-968-A
- TIA-968-B

Additional Information

Datasheet | **Resources** | **Samples**

Surge Ratings

Series	I_{PP}	
	10x1000µs	8x20µs
	Amps min	Amps min
G	18	50

Electrical Characteristics

Part Number	Marking	V_{DRM}@I_{DRM}=5µA	V_S@250V/µs	I_H	I_S	I_T	V_T@I_T=2.2 Amps	Co@f=1MHz,2V	
		V min	V max	mA typ	mA max	A max	V max	pF typ	pF Max
P0080T023G5RP	P08G	8	15	30	500	2.2	4	9.0	10

Notes:

- All measurement are made at an ambient temperature of 25°C Ipp applies to -40°C throught +85°C temperature range.
- Ipp is repetitive surge rating and is guaranteed for the life of the product.
- SIDACtor devices are bidirectional. All electrical parameters and surge rating apply to forward and reverse polarities.
- Specifications are subject to change without notice.

Revised: 02/23/17

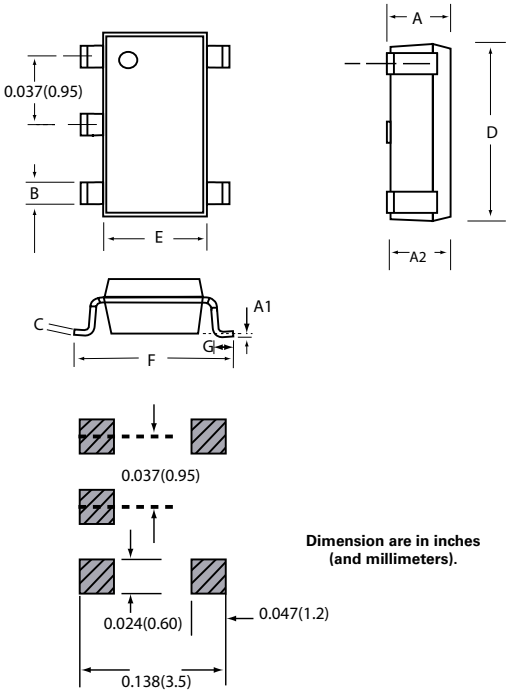
Maximum Ratings

Parameter Name	Symbol	Test Conditions	Value		Units
Lightning surge waveforms	I_{pp}	10x1000µs	18		A
		10x700µs/5x310µs	25		A
		1.2x50µs/8x20µs	50		A
		2x10µs	45		A
			min	max	
Operating Free Temperature Range	T_A		-40	+85	°C
Junction temperature	T_J		-40	+150	°C
Storage temperature	T_{STG}		-40	+150	°C

Notes:
- The device also complies with IEC 61000-4-2 ESD ±15kV (air discharge), ±8 kV(contact discharge) and IEC 61000-4-4 EFT 40A(5/50nS)
- The device must initially be in thermal equilibrium with -40°C $\leq T_J \leq$ +150°C
- The lightning surge may be repeated after the device returns to its initial conditions.

Mechanical dimensions, recommended layout dimensions

The epoxy meets UL 94V0 ratings.

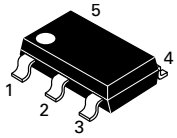


Dimension are in inches (and millimeters).

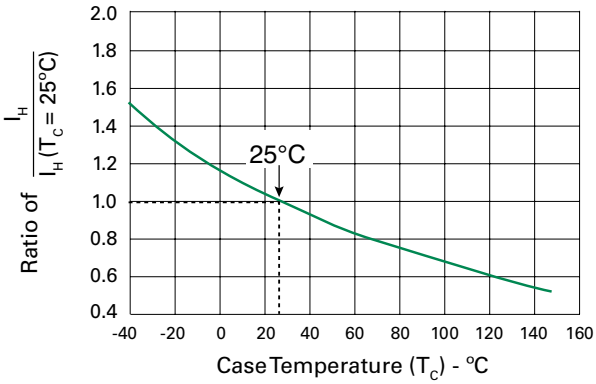
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	0.035	0.057	0.90	1.45
A1	0.000	0.004	0.00	0.10
A2	0.035	0.051	0.90	1.30
B	0.014	0.020	0.35	0.50
C	0.004	0.008	0.09	0.20
D	0.110	0.118	2.80	3.00
E	0.059	0.069	1.50	1.75
F	0.102	0.118	2.60	3.00
G	0.004	0.024	0.10	0.60

Revised: 02/23/17

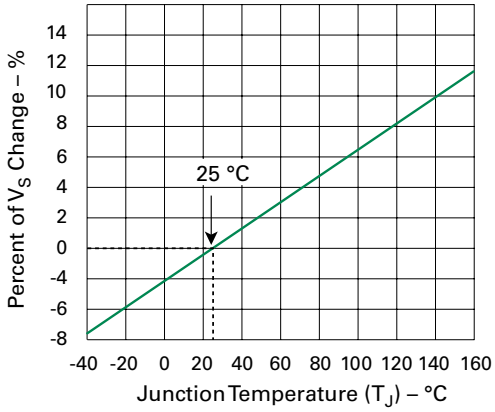
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_{STG}	Storage Temperature Range	-40 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	120	°C/W

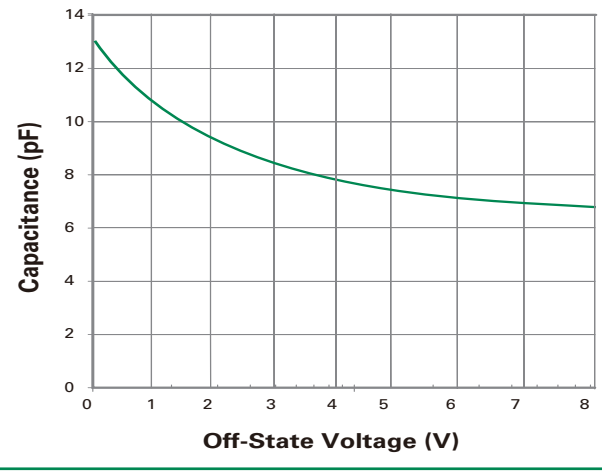
Holding Current vs. Case Temperature



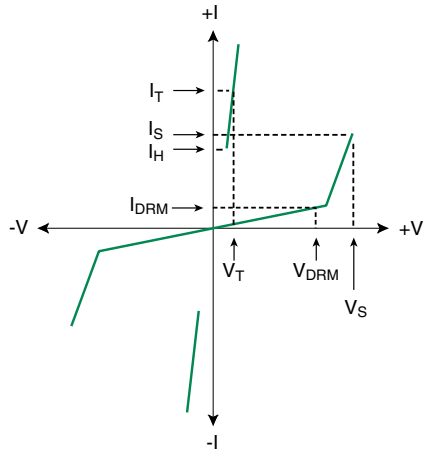
V_S vs. Junction Temperature



Capacitance vs. Bias Voltage*



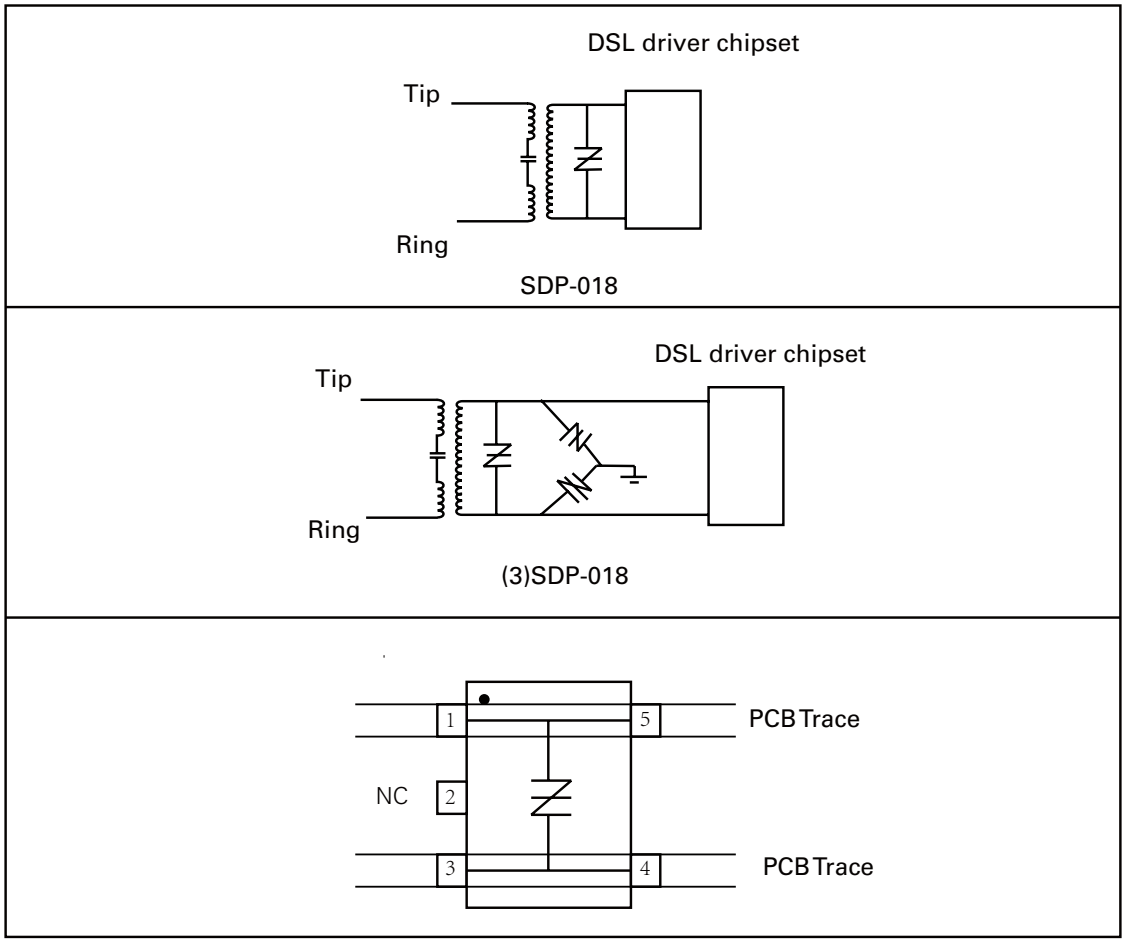
V-I Characteristics



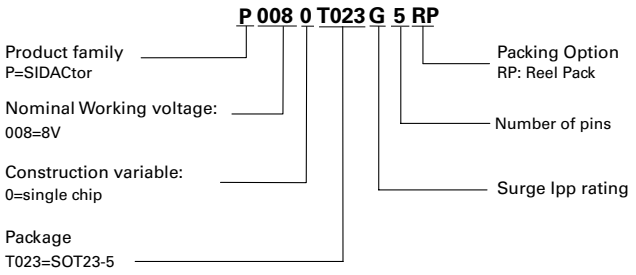
Revised: 02/23/17

P0080T023G5 Application example

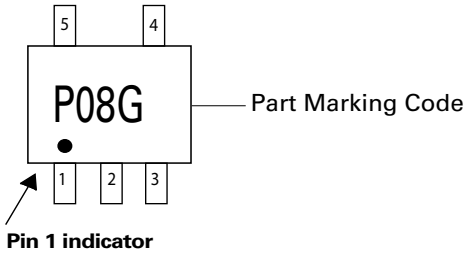
The following schematics show alternate protection solutions for a typical DSL interface that connects to outside wiring. This surface mount SOT23-5 chip-side solution provides a minimum footprint solution appropriate for high density card designs. The P0080T023G5 will protect the interface from lightning induced surges on the chip-side of the coupling transformer. This tertiary protector may be preceded by line-side protection such as the TeleLink over-current protector and the P0080T023G5 overvoltage protector. GDTs may also be used on the line side of the coupling transformer. The flow-through design of the SOT23-5 package is illustrated below. If the inter winding capacitance of the transformer is allowing some common mode events to get coupled across, then the P0080T023G5 can be placed in a three chip mode, as shown below for additional chip-side protection.



Part Numbering



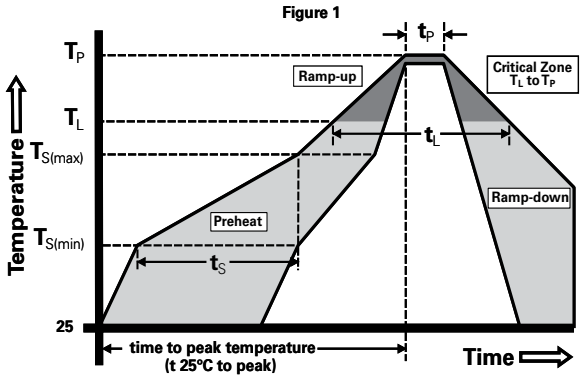
Part Marking



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Terminal Material	100% Matte-Tin Plated
Solderability	EIA J-STD-002, TEST A.

Environmental Specifications

Temp Cycling	Mil-STD-883F, Method 1010.8 Condition C, -65°C to +150°C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Bias Humidity	JESD 22-A101-B 85°C , 85°CRH. 50V 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Pressure Cooker	JEDEC 22-A102C No Bias, 121°C, 100%RH 96Hrs/192Hrs. 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
High Temp Storage	JESD 22-A103C Con B. 150°C, no bias 1000Hrs
HTRB	JESD 22-108C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Thermal Shock	Mil-STD-883F, Method 1011.9 Condition A, 0°C to 100°C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
C-SAM	As per flow, JSTD-020C pre&post preconditioning test.
Wet Humidity (Tin only)	NEMI standard: 60°C/93%RH

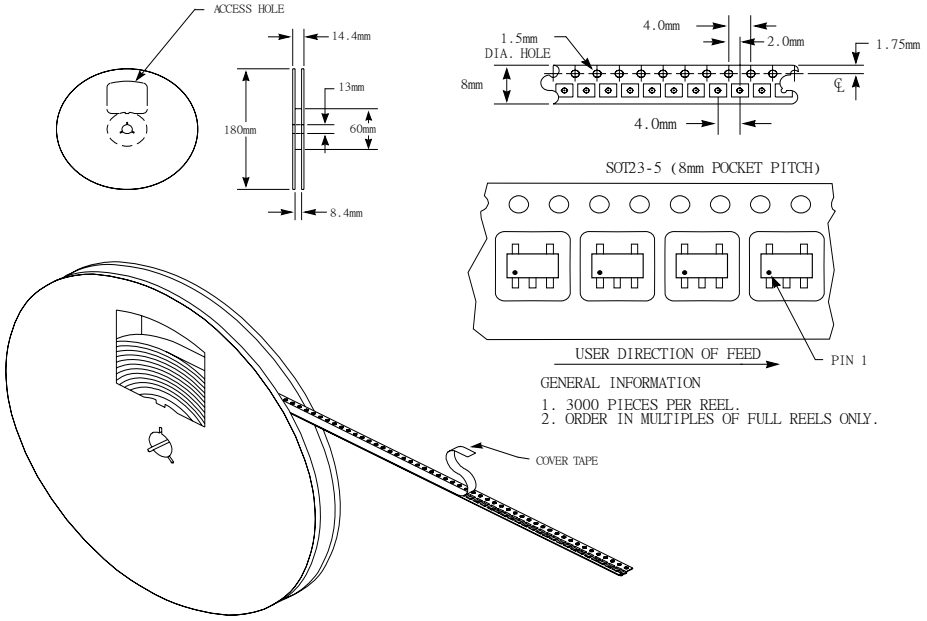
Revised: 02/23/17

Packing Options

Package Type	Description	Quantity	Added Suffix	Min. Order Qty.	Industry Standard
T023	SOT23-5 Tape & Reel Pack	3000	RP	3000	EIA-481-A

Tape and Reel Specification — SOT23-5

8mm TAPE AND REEL



SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Littelfuse®
Expertise Applied | Answers Delivered

TwinChip™ Series - DO-214

HF RoHS Pb e3

Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation

NOT APPLICABLE

Schematic Symbol

Description

TwinChip™ Series DO-214 are very low capacitance SIDACtor® thyristors designed to protect broadband equipment such as VoIP, DSL modems and DSLAMs from damaging overvoltage transients. This series provides a surface mount solution that enables equipment to comply with global regulatory standards, while limiting the impact to broadband signals.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Low distortion
- Fails short circuit when surged in excess of ratings
- 40% lower than comparable product
- RoHS Compliant and Halogen-Free
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA/968-A/B
- ITU K.20/21/45
- IEC 61000-4-5 2nd edition
- GR 1089 Intra-building
- YD/T 1082
- YD/T 993
- YD/T 950
- ITU K.20/21/45 Enhanced*
- GR 1089 Inter-building*

** Additional series resistance may be required to comply*

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	@1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P0642SALRP	P062A	58	77	120	800	2.2	8	25	45
P0722SALRP	P072A	65	88	120	800	2.2	8	20	45
P0902SALRP	P092A	75	98	120	800	2.2	8	20	40
P1102SALRP	P112A	90	130	120	800	2.2	8	15	35
P1302SALRP	P132A	120	160	120	800	2.2	8	15	35
P1502SALRP	P152A	140	180	120	800	2.2	8	15	30
P1802SALRP	P182A	170	220	120	800	2.2	8	10	30
P2302SALRP	P232A	190	260	120	800	2.2	8	10	25
P2602SALRP	P262A	220	300	120	800	2.2	8	10	25
P3002SALRP	P302A	280	360	120	800	2.2	8	10	25
P3502SALRP	P352A	320	400	120	800	2.2	8	10	20
P4202SALRP	P422A	380	500	120	800	2.2	8	10	20
P4802SALRP	P482A	440	600	120	800	2.2	8	5	20
P6002SALRP	P602A	550	700	120	800	2.2	8	5	20

Table continues on next page.

Revised: 02/23/17

Electrical Characteristics (continued)

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 A	@1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P0642SBLRP	P062B	58	77	120	800	2.2	8	25	45
P0722SBLRP	P072B	65	88	120	800	2.2	8	20	45
P0902SBLRP	P092B	75	98	120	800	2.2	8	20	40
P1102SBLRP	P112B	90	130	120	800	2.2	8	15	35
P1302SBLRP	P132B	120	160	120	800	2.2	8	15	35
P1502SBLRP	P152B	140	180	120	800	2.2	8	15	30
P1802SBLRP	P182B	170	220	120	800	2.2	8	10	30
P2302SBLRP	P232B	190	260	120	800	2.2	8	10	25
P2602SBLRP	P262B	220	300	120	800	2.2	8	10	25
P3002SBLRP	P302B	280	360	120	800	2.2	8	10	25
P3502SBLRP	P352B	320	400	120	800	2.2	8	10	20
P4202SBLRP	P422B	380	500	120	800	2.2	8	10	20
P4802SBLRP	P482B	440	600	120	800	2.2	8	5	20
P6002SBLRP	P602B	550	700	120	800	2.2	8	5	20
P3002SCLRP	P302C	280	360	120	800	2.2	8	20	35
P3502SCLRP	P352C	320	400	120	800	2.2	8	20	30
P4202SCLRP	P422C	380	500	120	800	2.2	8	15	30
P4802SCLRP	P482C	440	600	120	800	2.2	8	15	30
P6002SCLRP	P602C	550	700	120	800	2.2	8	10	25
P7002SCLRP*	P702C	640	850	120	800	2.2	8	10	30

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional.
- Part with * is under development

Surge Ratings

Series	I_{PP}									I_{TSM}	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]	50/60 Hz	
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs
A	20	150	150	90	50	75	75	45	75	20	500
B	25	250	250	150	100	100	125	80	100	25	500
C	50	500	400	200	150	200	175	100	200	30	500

Notes:

1 Current waveform in µs

2 Voltage waveform in µs

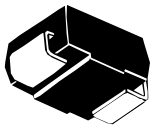
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

Additional Information

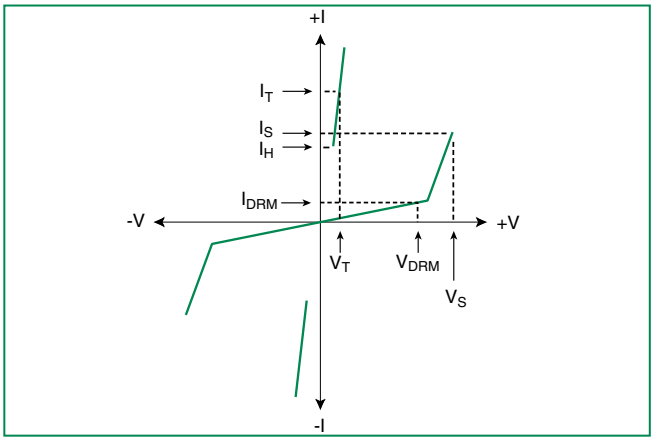
Datasheet | **Resources** | **Samples**

Revised: 02/23/17

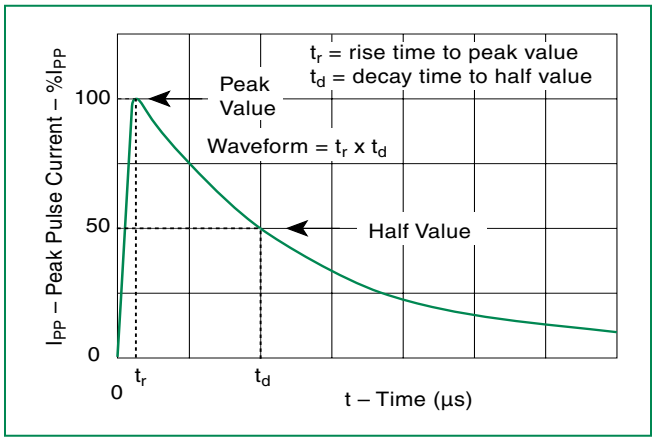
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
DO-214AA 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	90	°C/W

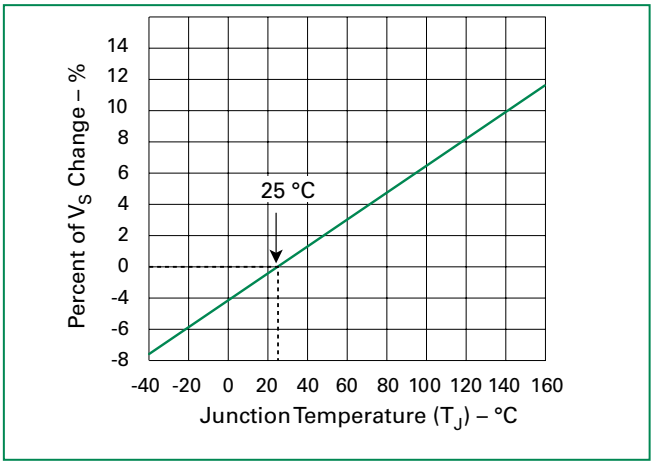
V-I Characteristics



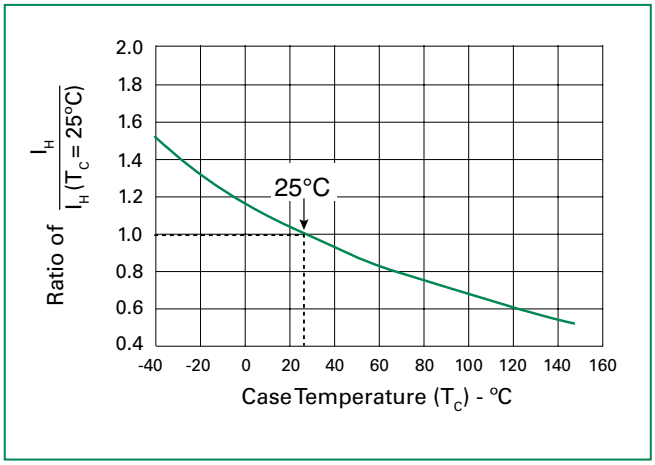
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

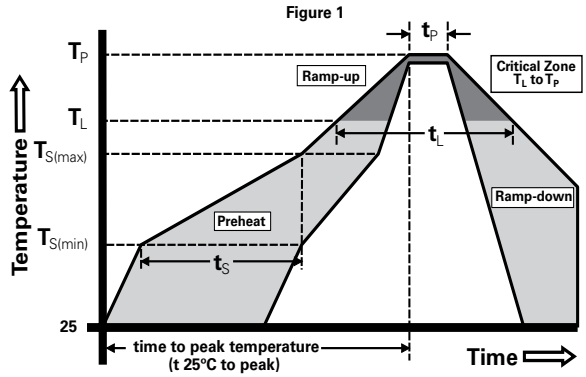


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

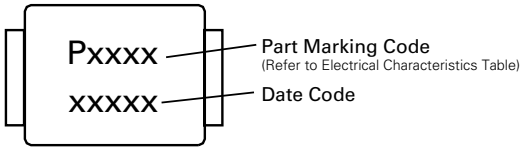
Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

Part Marking

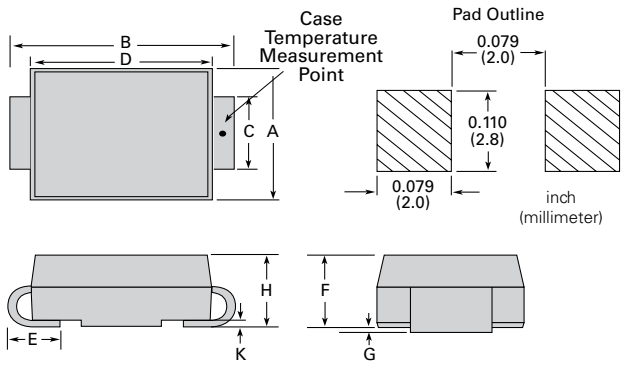


Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85% RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100% RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85% RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

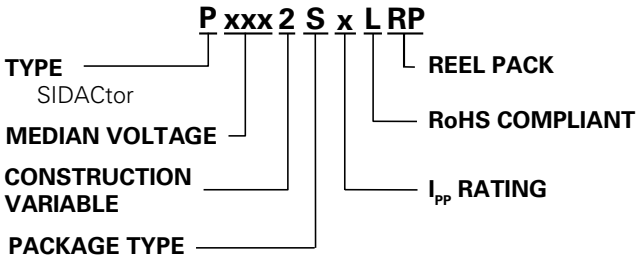
Revised: 02/23/17

Dimensions — DO-214AA



Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.130	0.156	3.30	3.95
B	0.201	0.220	5.10	5.60
C	0.077	0.087	1.95	2.20
D	0.159	0.181	4.05	4.60
E	0.030	0.063	0.75	1.60
F	0.075	0.096	1.90	2.45
G	0.002	0.008	0.05	0.20
H	0.077	0.104	1.95	2.65
K	0.006	0.016	0.15	0.41

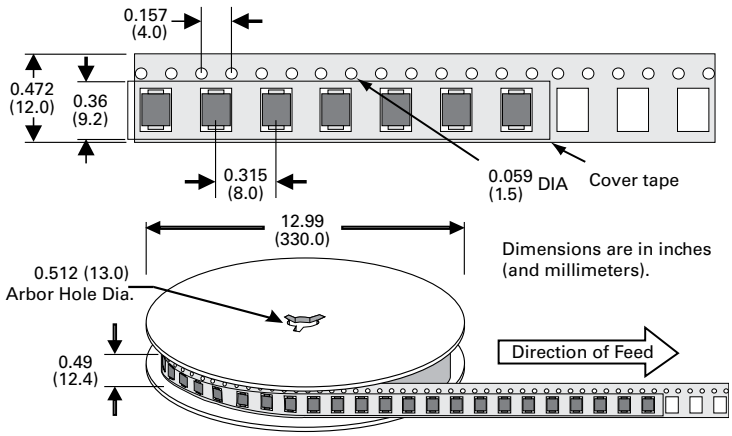
Part Numbering



Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
S	DO-214AA Tape & Reel	2500	RP	EIA-481-D

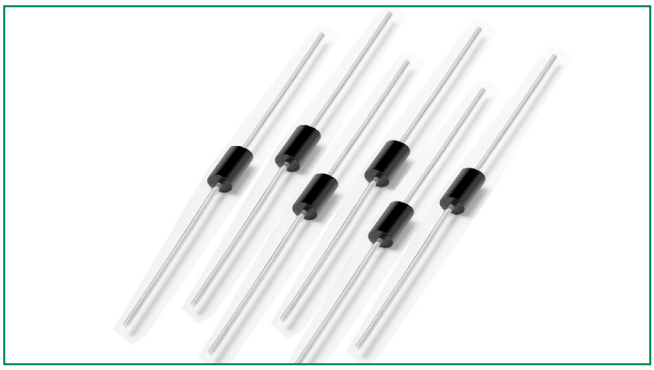
Tape and Reel Specification — DO-214AA



Littelfuse
Expertise Applied | Answers Delivered

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

TwinChip™ Series - DO-15



Description

TwinChip™ Series DO-15 are very low capacitance SIDACtor® thyristors are designed to protect broadband CPE equipment, such as VoIP and xDSL modems from damaging overvoltage transients. The series provides a through-hole solution that enables equipment to comply with global regulatory standards while limiting the impact to broadband signals.

Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation

NOT APPLICABLE

Schematic Symbol

Features & Benefits

- Differential protection
- Low insertion loss
- Low capitance
- GDT compatible axial footprint
- Low voltage overshoot
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- RoHS Compliant
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Basic Level
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

Electrical Characteristics

Part Number	Marking	V_{DRM} @ I_{DRM}=5µA	V_S @ 100V/µs	I_H	I_S	I_T	V_T @ I_T = 2.2 Amps	@1MHz @ 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P2602GBLRP	P262B	220	300	150	800	2.2	8	15	25
P3002GBLRP	P30B	280	360	150	800	2.2	8	10	20
P3502GBLRP	P352B	320	400	150	800	2.2	8	10	20
P4502GBLRP*	P452B	400	530	150	800	2.2	8	25	45

Notes:
- Absolute maximum ratings measured at T_A = 25°C (unless otherwise noted).
- Components are bi-directional.

Additional Information

Datasheet | **Resources** | **Samples**

Revised: 02/23/17

Surge Ratings

Series	I_{PP}			I_{TSM}
	10/160 [1] 10/160 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]	50 / 60 Hz
	A min	A min	A typ	A min
B	100	80	150	25

Notes:

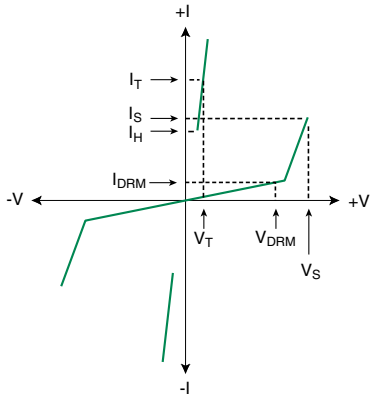
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

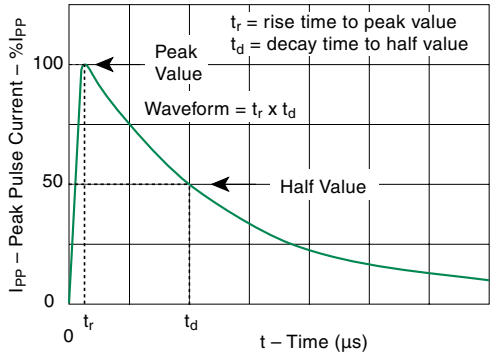
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
 DO-15	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	120	°C/W

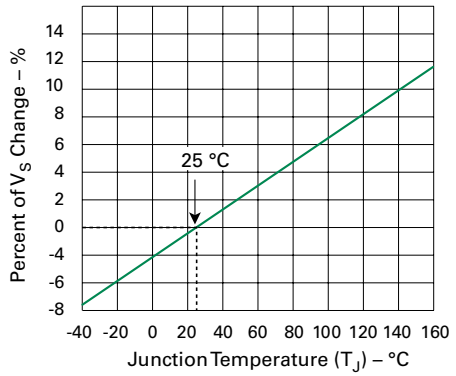
V-I Characteristics



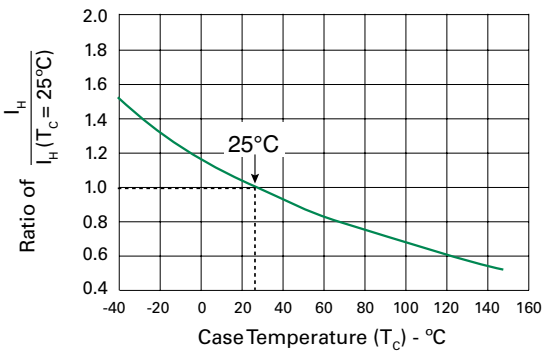
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

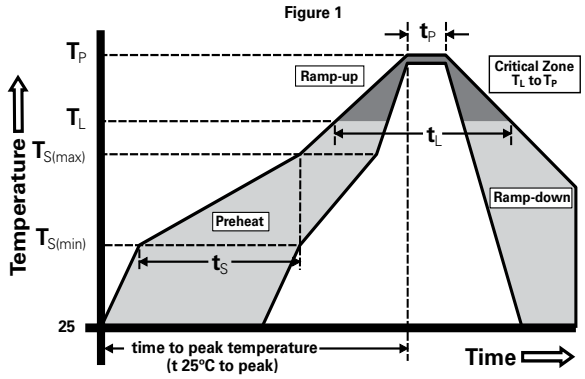


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Figure 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60-180 secs
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60-150 seconds
Peak Temperature (T_P)		260(+0/-5)°C
Time within 5°C of actual peak Temperature (t_p)		30 seconds max
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes max
Do not exceed		260°C

Figure 1



Physical Specifications

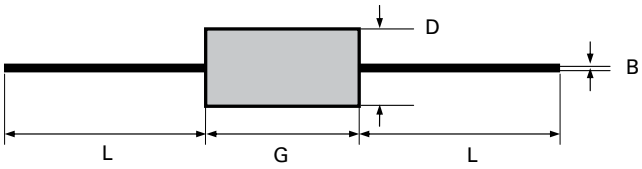
Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C peak). JEDEC-J-STD-020, Level 1

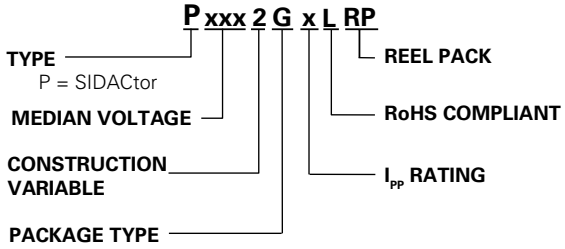
Revised: 02/23/17

Dimensions — DO-15

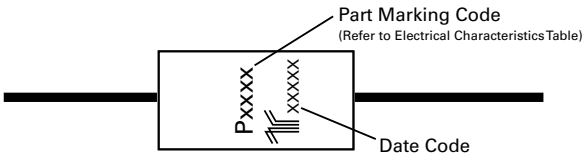


Dimension	Inches		Millimeters	
	min	max	min	max
B	0.028	0.034	0.711	0.864
D	0.12	0.14	3.048	3.556
G	0.235	0.27	5.969	6.858
L	1		25.4	

Part Numbering



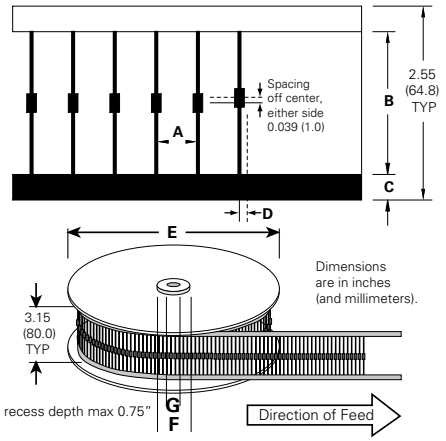
Part Marking



Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
G	DO-15 Axial Tape & Reel	5000	RP	EIA-RS-296-D

Tape and Reel Specification — DO-15



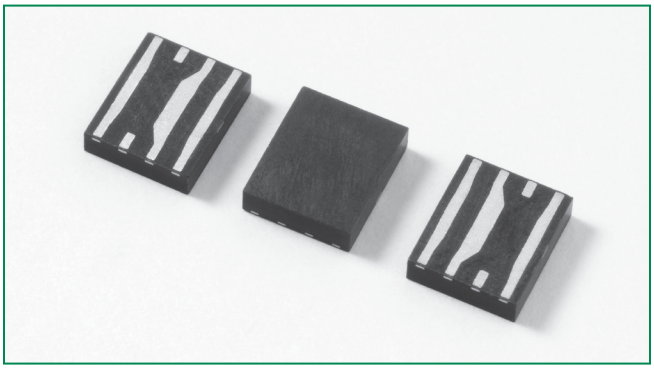
Symbols	Description	inch	mm
A	Component Spacing (lead to lead)	0.200 ± 0.020"	5.08 ± 0.508
B	Inner Tape Pitch	2.062 ± 0.059"	52.37 ± 1.498
C	Tape Width	0.250"	6.35
D	Max. Off Alignment	0.048"	1.219
E	Reel Dimension	13"	330.2
F	Max. Hub Recess	3"	76.19
G	Max. Abor Hole	0.68"	17.27

Littelfuse
Expertise Applied | Answers Delivered

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

SEP Biased Series - 5x6 QFN

HF RoHS



Description

The new SEP (SIDACtor Thyristor Ethernet/PoE Protector) series has a surge rating compatible with GR1089 Inter-building and ITU K.20/21 Enhanced protection requirements. Targeted for high-speed applications such as 10BaseT, 100BaseT, and 1000BaseT, the SEP series maintains signal quality while providing robust protection for Ethernet and PoE applications. This latest silicon design innovation results in a capacitive loading characteristic that is constant with respect to the voltage across the device. This reduces distortion caused by typical solid-state protection solutions. Offered in a surface-mount, QFN package, the SEP provides small package size without sacrificing power and surge handling capabilities.

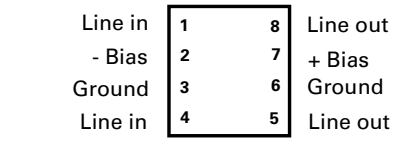
Agency Approvals

Agency	Agency File Number
	E133083

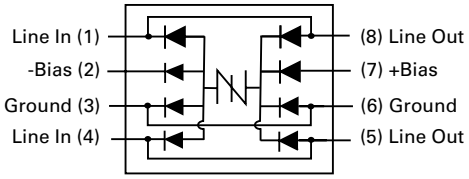
Features & Benefits

- Compatible with 1000Base-T
- Balanced overvoltage protection
- Low distortion
- Low insertion loss
- Low profile
- SO-8 footprint compatible
- Fails short circuit when surged in excess of ratings
- RoHS Compliant and Halogen-Free
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Pinout Designation



Schematic Symbol



Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- IEC 61000-4-5 2nd edition
- GR 1089 Inter-building
- GR 1089 Intra-building
- YD/T 1082
- YD/T 993
- YD/T 950

Electrical Characteristics

Part Number	Marking	V_{DRM}@ I_{DRM}=5µA	V_S@100V/µs	I_H	I_S	I_T@V_T	V_T@I_T= 2.2Amps	Capacitance
		V min	V max	mA min	mA max	A max	V max	
SEP0080Q38CB	SEP-8C	6	25	50	800	2.2	8	See Capacitance vs. Bias Voltage Graph
SEP0640Q38CB	SEP06C	58	77	150	800	2.2	8	
SEP0720Q38CB	SEP07C	65	88	150	800	2.2	8	
SEP0900Q38CB	SEP09C	75	98	150	800	2.2	8	

Notes:
- Absolute maximum ratings measured at T_A= 25ºC (unless otherwise noted).
- Devices are bi-directional (unless otherwise noted).

Additional Information

Datasheet | Resources | Samples

Revised: 02/23/17

50/60 Hz Ratings

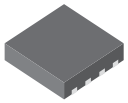
Parameter Name	Test Conditions	Value	Units
I_{TSM} Maximum non-repetitive on-state current, 50/60 Hz	0.5s	6.5	A
	1s	4.6	
	2s	3.4	
	5s	2.3	
	30s	1.3	
	900s	0.73	

Surge Ratings

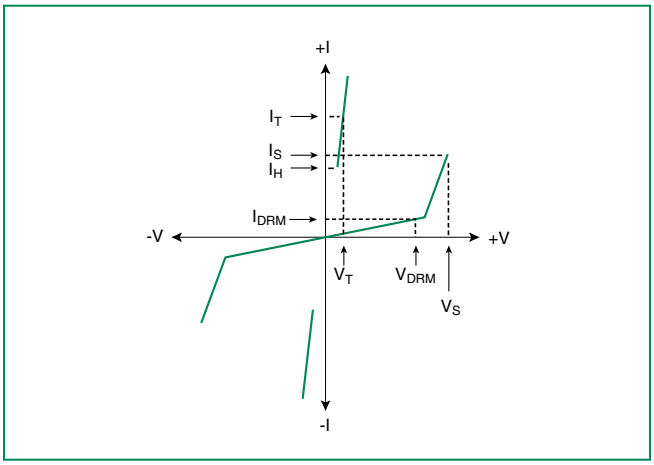
Series	I_{PP}				I_{TSM}
	2x10µs	1.2x50µs/8x20µs	10x700/5x310µs	10x1000µs	$600V_{RMS}$ 1 cycle
	A min	A min	A min	A min	A_{RMS}
C	500	400	200	100	30

Notes:
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The device must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

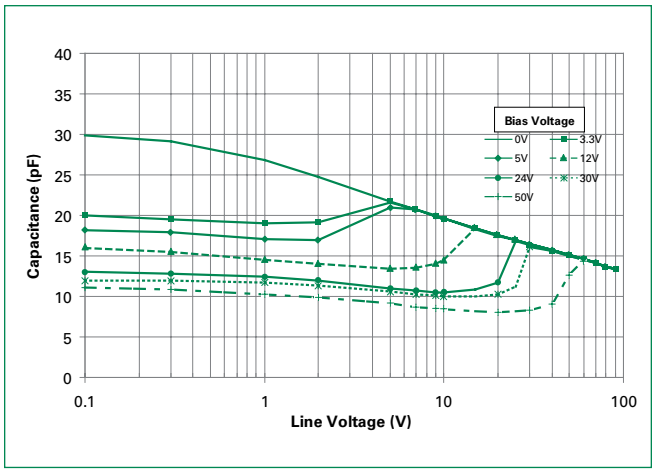
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
 5x6 QFN	T_J	Junction Temperature	-40 to +150	°C
	T_{STG}	Storage Temperature Range	-40 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	100	°C/W

V-I Characteristics



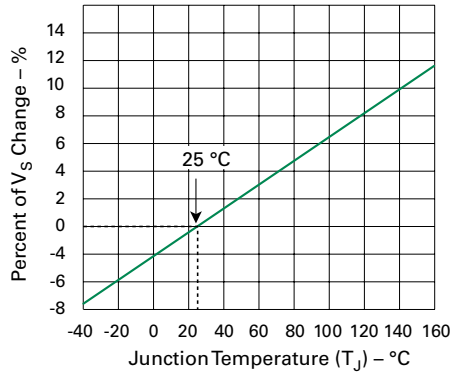
Capacitance vs. Bias Voltage*



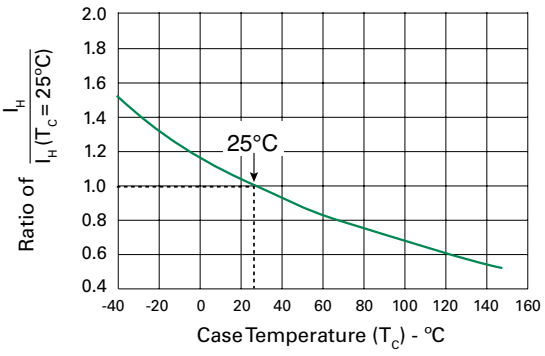
* Bias voltage must be lower than V_{DRM}

Revised: 02/23/17

Normalized V_S Change vs. Junction Temperature



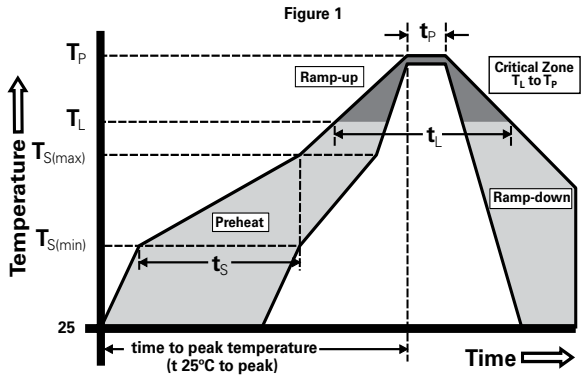
Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

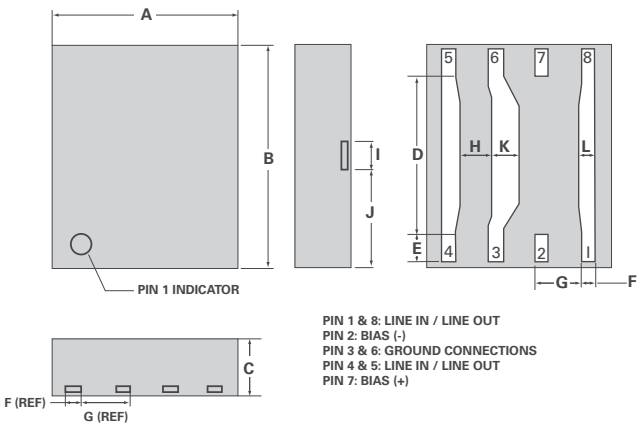
Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification 94V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

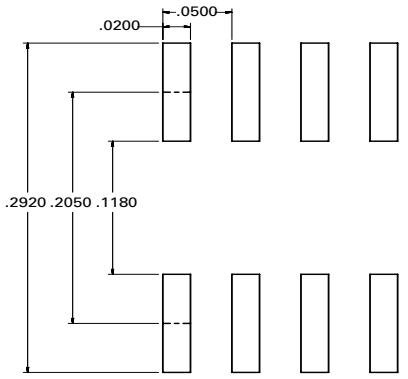
Revised: 02/23/17

Dimensions — 5x6 QFN

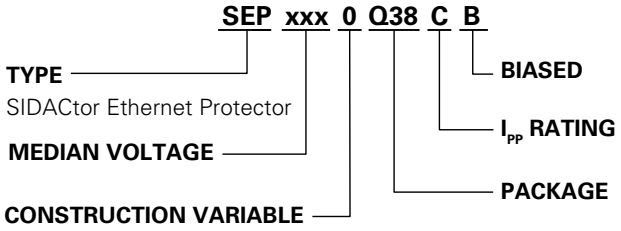


Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	0.187	0.207	4.745	5.253
B	0.226	0.246	5.745	6.253
C	0.054	0.064	1.374	1.628
D	0.165	0.171	4.199	4.351
E	0.027	0.033	0.686	0.838
F	0.011	0.017	0.279	0.432
G	0.047	0.053	1.194	1.346
H	0.032	0.038	0.800	0.953
I	0.027	0.033	0.686	0.838
J	0.100	0.106	2.540	2.692
K	0.027	0.033	0.686	0.838
L	0.015	0.021	0.381	0.533

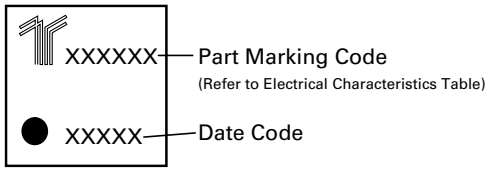
5x6 QFN Solder Pad Layout



Part Numbering



Part Marking



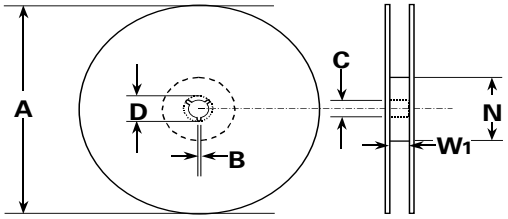
Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
Q38	5x6x1.5 QFN Tape and Reel	4,000	N / A	EIA-481-D

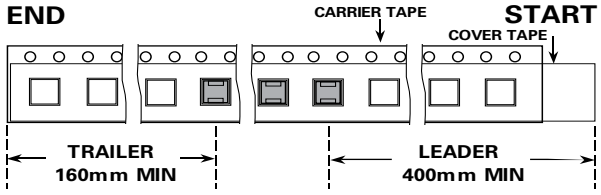
Revised: 02/23/17

Tape and Reel Specifications — 5x6 QFN

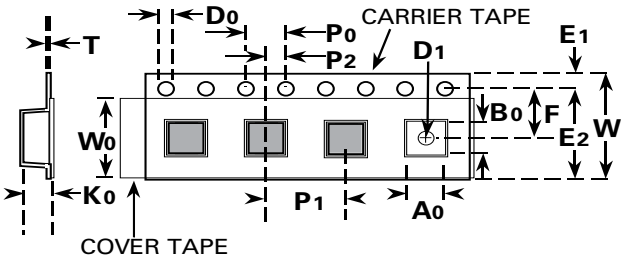
Reel Dimension



Tape Leader and Trailer Dimensions



Tape Dimension Items



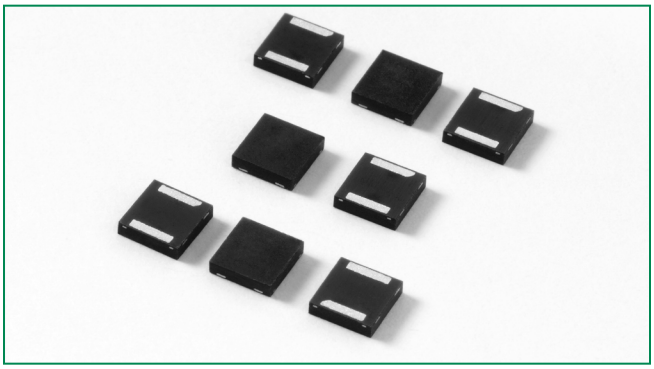
Symbols	Description	Inches		Millimeters	
		Min	Max	Min	Max
A	Reel Diameter	N/A	12.992	N/A	330.0
B	Drive Spoke Width	0.059	N/A	1.50	N/A
C	Arbor Hole Diameter	0.504	0.531	12.80	13.50
D	Drive Spoke Diameter	0.795	N/A	20.20	N/A
N	Hub Diameter	1.969	N/A	50.00	N/A
W_1	Reel Inner Width at Hub	0.488	0.567	12.40	14.40
A_0	Pocket Width at Bottom	0.204	0.212	5.20	5.40
B_0	Pocket Length at Bottom	0.244	0.252	6.20	6.40
D_0	Feed Hole Diameter	0.059	0.063	1.50	1.60
D_1	Pocket Hole Diameter	0.059	N/A	1.50	N/A
E_1	Feed Hole Position 1	0.065	0.073	1.65	1.85
E_2	Feed Hole Position 2	0.400	0.408	10.15	10.35
F	Feed Hole Center - Pocket Hole Center 2	0.212	0.220	5.40	5.60
K_0	Pocket Depth	0.067	0.075	1.70	1.90
P_0	Feed Hole Pitch	0.153	0.161	3.90	4.10
P_1	Component Spacing	0.311	0.319	7.90	8.10
P_2	Feed Hole Center - Pocket Hole Center 1	0.077	0.081	1.90	2.10
T	Carrier Tape Thickness	0.010	0.014	0.25	0.35
W	Embossed Carrier Tape Width	0.460	0.484	11.70	12.30
W_0	Cover Tape Width	0.358	0.366	9.10	9.30

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Littelfuse®
Expertise Applied | Answers Delivered

Q2L Series - 3x3 QFN

HF RoHS



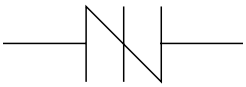
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation

Not Applicable

Schematic Symbol



Description

Q2L Series 3x3 QFN are low capacitance SIDACtor® thyristors designed to protect high density broadband equipment from damaging overvoltage transients.

The series provides a low profile surface solution that enables broadband equipment to comply with global regulatory standards while limiting the impact to broadband signals and board space.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Low capacitance
- Does not degrade surge capability after multiple surge events within limit.
- Small footprint
- Fails short circuit when surged in excess of ratings
- RoHS Compliant and Halogen-Free
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Enhanced Level*
- ITU K.20/21/45 Basic Level
- IEC 61000-4-5 2nd edition
- GR 1089 Inter-building*
- GR 1089 Intra-building
- YD/T 1082
- YD/T 993
- YD/T 950

* A/B-Rated parts require series resistance

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T@ I_T= 2.2Amps	Capacitance @1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P0080Q12ALRP	P-8A	6	25	50	800	2.2	5	25	55
P0300Q12ALRP	P03A	25	40	50	800	2.2	5	15	35
P0640Q12ALRP	P06A	58	77	150	800	2.2	5	40	60
P0720Q12ALRP	P07A	65	88	150	800	2.2	5	40	60
P0900Q12ALRP	P09A	75	98	150	800	2.2	5	35	55
P1100Q12ALRP	P11A	90	130	150	800	2.2	5	30	50
P1300Q12ALRP	P13A	120	160	150	800	2.2	5	25	45
P1500Q12ALRP	P15A	140	180	150	800	2.2	5	25	40
P1800Q12ALRP	P18A	170	220	150	800	2.2	5	25	35
P2300Q12ALRP	P23A	190	260	150	800	2.2	5	25	35
P2600Q12ALRP	P26A	220	300	150	800	2.2	5	25	35
P3100Q12ALRP	P31A	275	350	150	800	2.2	5	20	35
P3500Q12ALRP	P35A	320	400	150	800	2.2	5	20	30

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional.

Table continues on next page.

Revised: 02/23/17

Electrical Characteristics (continued)

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T@ I_T= 2.2Amps	Capacitance @1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P0080Q12BLRP	P-8B	6	25	50	800	2.2	5	25	55
P0300Q12BLRP	P03B	25	40	50	800	2.2	5	15	35
P0640Q12BLRP	P06B	58	77	150	800	2.2	5	40	60
P0720Q12BLRP	P07B	65	88	150	800	2.2	5	40	60
P0900Q12BLRP	P09B	75	98	150	800	2.2	5	35	55
P1100Q12BLRP	P11B	90	130	150	800	2.2	5	30	50
P1300Q12BLRP	P13B	120	160	150	800	2.2	5	25	45
P1500Q12BLRP	P15B	140	180	150	800	2.2	5	25	40
P1800Q12BLRP	P18B	170	220	150	800	2.2	5	25	35
P2300Q12BLRP	P23B	190	260	150	800	2.2	5	25	35
P2600Q12BLRP	P26B	220	300	150	800	2.2	5	25	35
P3100Q12BLRP	P31B	275	350	150	800	2.2	5	20	35
P3500Q12BLRP	P35B	320	400	150	800	2.2	5	20	30

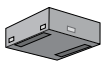
Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional.

Surge Ratings

Series	I_{PP}					I_{TSM}	di/dt
	2/10µs	1.2/50µs/8/20µs	10/160µs	10/560µs	10/1000µs	50 / 60 Hz	
	A min	A min	A min	A min	A min	A min	A/µs max
A	150	150	90	50	45	20	500
B	250	250	150	100	80	25	500

Notes:
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

Thermal Considerations

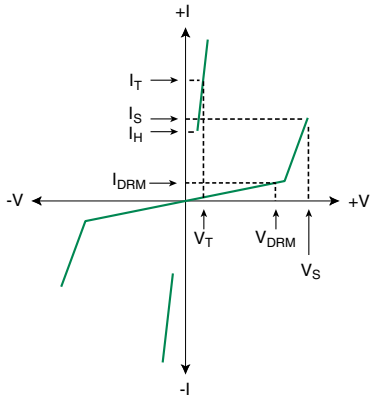
Package	Symbol	Parameter	Value	Unit
3x3 QFN 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	120	°C/W

Additional Information

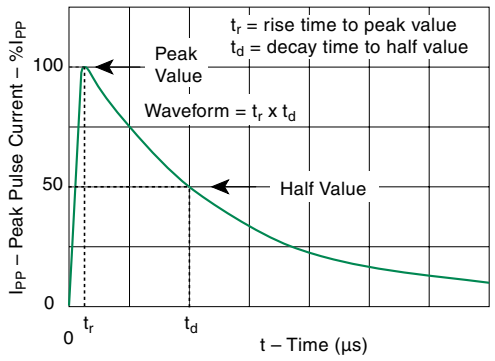
Datasheet | **Resources** | **Samples**

Revised: 02/23/17

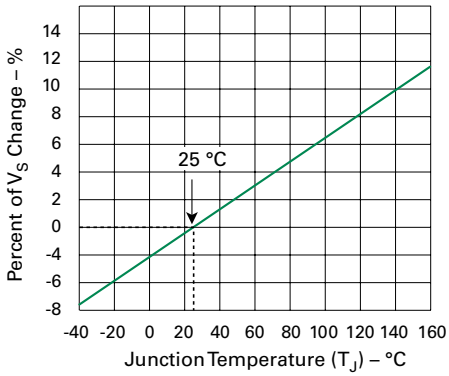
V-I Characteristics



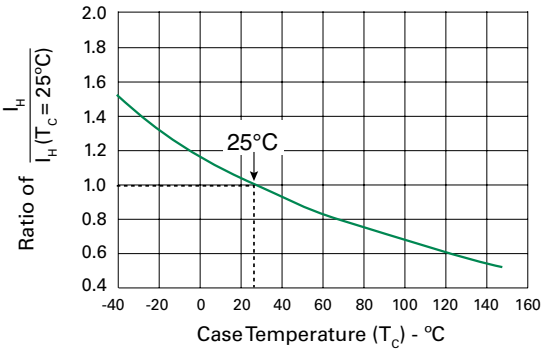
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



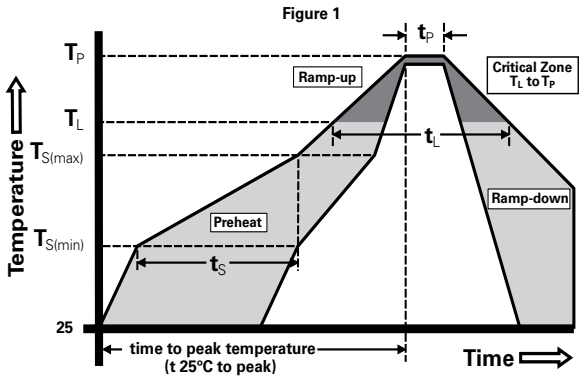
Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Revised: 02/23/17

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

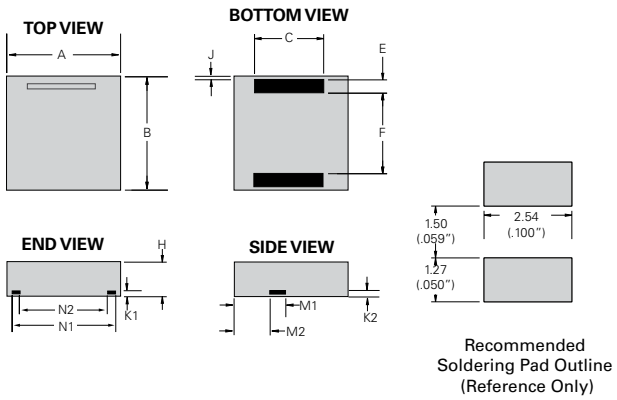
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

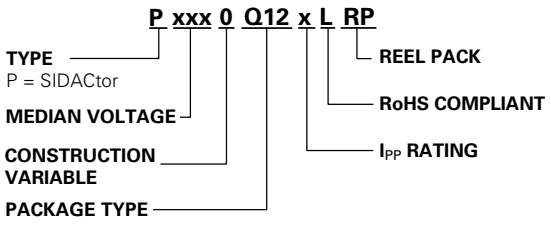
Dimensions — 3x3 QFN



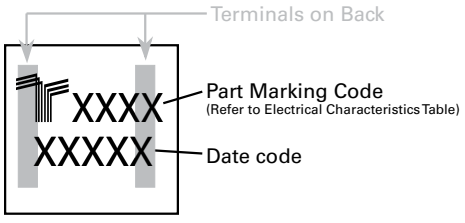
Recommended Soldering Pad Outline (Reference Only)

Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.114	0.122	2.900	3.100
B	0.114	0.122	2.900	3.100
C	0.075	0.083	1.900	2.100
E	0.011	0.019	0.285	0.485
F	0.076	0.084	1.930	2.130
H	0.035	0.043	0.900	1.100
J	0.000	0.008	0.000	0.200
K1	0.004	0.012	0.100	0.300
K2	0.004	0.012	0.100	0.300
M1	0.056	0.064	1.430	1.630
M2	0.038	0.046	0.970	1.170
N1	0.096	0.104	2.440	2.640
N2	0.082	0.090	2.080	2.280

Part Numbering



Part Marking



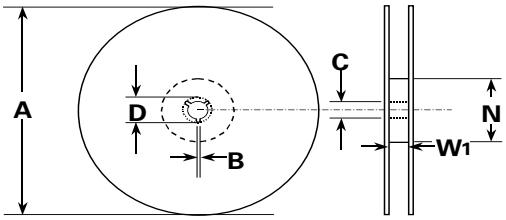
Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
Q12	3x3 QFN Tape and Reel Pack	5000	RP	EIA-481-D

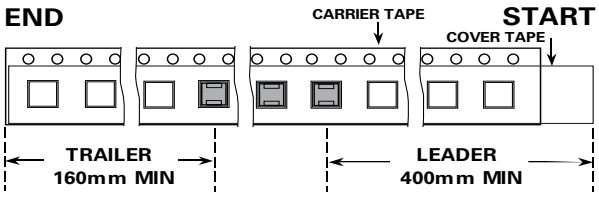
Revised: 02/23/17

Tape and Reel Dimensions — 3x3 QFN

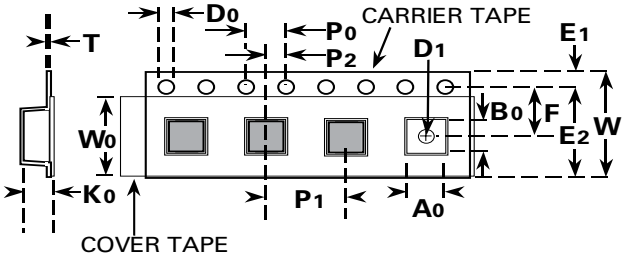
Reel Dimension



Tape Leader and Trailer Dimensions



Tape Dimension Items



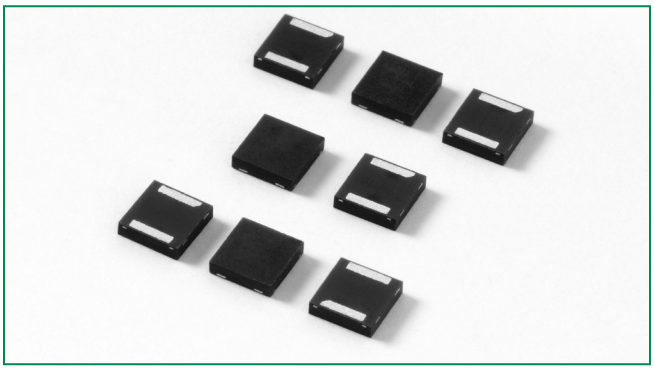
Symbols	Description	Inches		Millimeters	
		Min	Max	Min	Max
A	Reel Diameter	N/A	12.992	N/A	330.0
B	Drive Spoke Width	0.059	N/A	1.50	N/A
C	Arbor Hole Diameter	0.504	0.531	12.80	13.50
D	Drive Spoke Diameter	0.795	N/A	20.20	N/A
N	Hub Diameter	1.969	N/A	50.00	N/A
W_1	Reel Inner Width at Hub	0.488	0.567	12.40	14.40
A_0	Pocket Width at bottom	0.126	0.134	3.20	3.40
B_0	Pocket Length at bottom	0.126	0.134	3.20	3.40
D_0	Feed Hole Diameter	0.059	0.063	1.50	1.60
D_1	Pocket Hole Diameter	0.059	N/A	1.50	N/A
E_1	Feed hole position 1	0.065	0.073	1.65	1.85
E_2	Feed hole position 2	0.400	0.408	10.15	10.35
F	Feed hole center-Pocket hole	0.215	0.219	5.45	5.55
K_0	Pocket Depth	0.039	0.051	1.00	1.30
P_0	Feed Hole Pitch	0.153	0.161	3.90	4.10
P_1	Component Spacing	0.311	0.319	7.90	8.10
P_2	Feed hole center-Pocket hole	0.077	0.081	1.95	2.05
T	Carrier Tape Thickness	0.010	0.014	0.25	0.35
W	Embossed Carrier Tape Width	0.453	0.484	11.50	12.30
W_0	Cover Tape Width	0.358	0.366	9.10	9.30

Littelfuse
Expertise Applied | Answers Delivered

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Q2L Series - 3.3x3.3 QFN

HF RoHS



Description

Q2L Series 3.3x3.3 QFN are low capacitance SIDACtor® devices designed to protect high density broadband equipment from damaging overvoltage transients.

The series provides a low profile, chip scale surface mount solution that enables broadband equipment to comply with global regulatory standards while limiting the impact to broadband signals and board space.

Agency Approvals

Agency	Agency File Number
	E133083

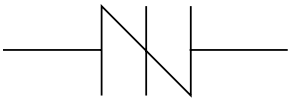
Features and Benefits

- Low profile
- Small footprint
- Low capacitance
- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- 2nd level interconnect is Pb-free per IPC/JEDEC J-STD-609A.01

Pinout Designation

Not Applicable

Schematic Symbol



Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-5
- YD/T 1082
- YD/T 993
- YD/T 950

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T@I_T= 2.2 Amps	Capacitance @1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P0080Q22CLRP	P-8C	6	25	50	800	2.2	5	35	75
P0300Q22CLRP	P03C	25	40	50	800	2.2	5	25	45
P0640Q22CLRP	P06C	58	77	150	800	2.2	5	55	85
P0720Q22CLRP	P07C	65	88	150	800	2.2	5	50	75
P0900Q22CLRP	P09C	75	98	150	800	2.2	5	45	70
P1100Q22CLRP	P11C	90	130	150	800	2.2	5	45	70
P1300Q22CLRP	P13C	120	160	150	800	2.2	5	40	60
P1500Q22CLRP	P15C	140	180	150	800	2.2	5	35	55
P1800Q22CLRP	P18C	170	220	150	800	2.2	5	35	50
P2300Q22CLRP	P23C	190	260	150	800	2.2	5	30	50
P2600Q22CLRP	P26C	220	300	150	800	2.2	5	30	45
P3100Q22CLRP	P31C	275	350	150	800	2.2	5	30	45
P3500Q22CLRP	P35C	320	400	150	800	2.2	5	25	40
P4500Q22CLRP	P45C	400	530	150	800	2.2	5	25	45
P4600Q22CLRP*	P46C	425	550	150	800	2.2	5	25	45

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Devices are bi-directional (unless otherwise noted).

Revised: 02/23/17

Surge Ratings

Series	2x10 [1] 2x10 [2]	8x20 [1] 1.2x50 [2]	10x160 [1] 10x160 [2]	10x560 [1] 10x560 [2]	10x1000 [1] 10x1000 [2]	5x310 [1] 10x700 [2]	I_{TSM} 50/60 Hz	di/dt
	A min	A min	A min	A min	A min	A min	A min	A/µs max
C	500	400	200	150	100	200 [3]	30	500

Notes:

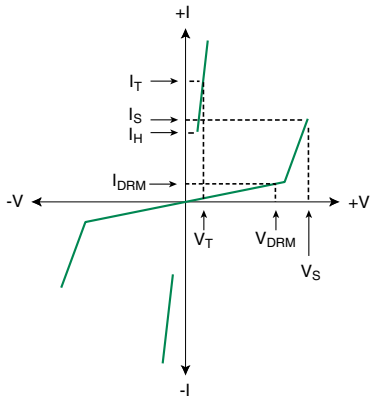
1 Current waveform in µs
2 Voltage waveform in µs
3 for surge rating of P4500Q22CLRP 10x700µs min=150A & typical=180A

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The device must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

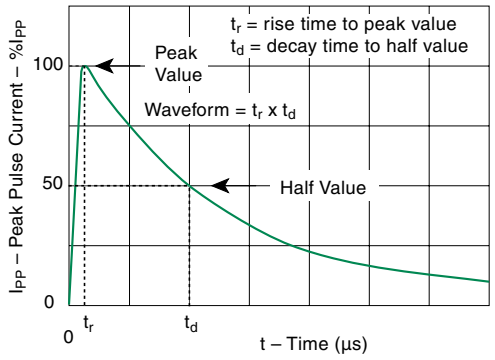
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
3.3 x 3.3 QFN 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	120	°C/W

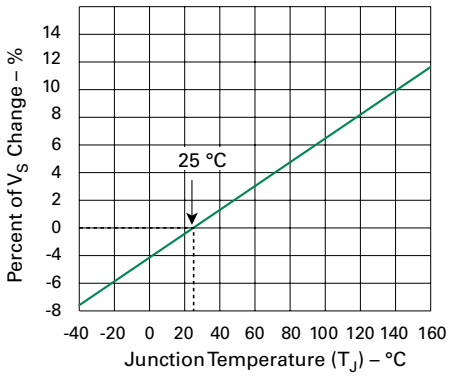
V-I Characteristics



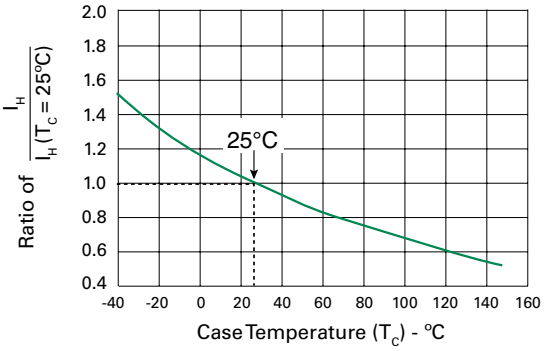
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature



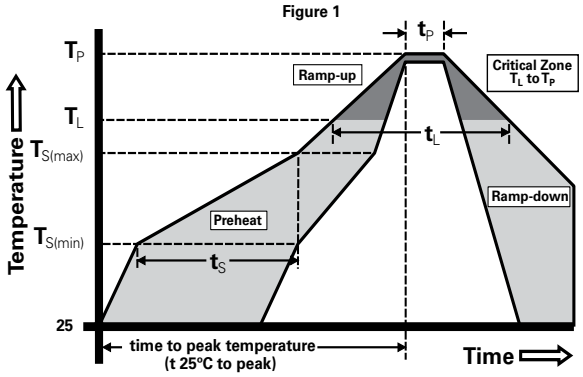
Revised: 02/23/17

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification 94V-0

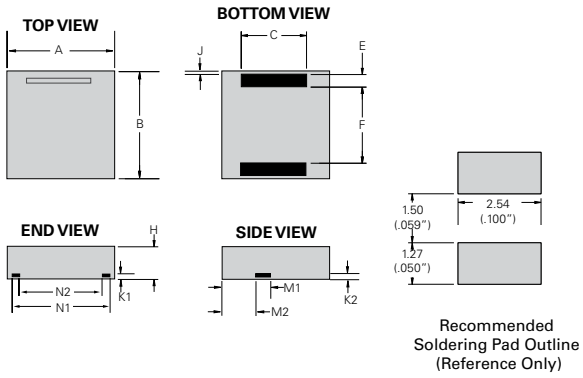
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85% RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85% RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Additional Information

Datasheet | **Resources** | **Samples**

Dimensions — 3.3x3.3 QFN

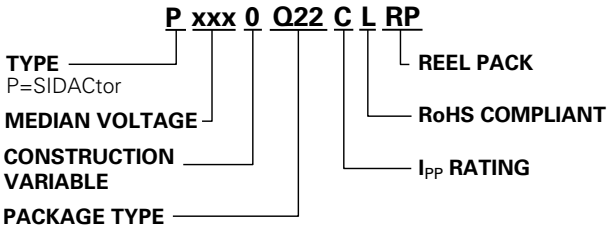


Recommended Soldering Pad Outline (Reference Only)

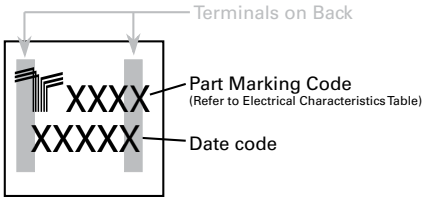
Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.126	0.134	3.200	3.400
B	0.126	0.134	3.200	3.400
C	0.075	0.083	1.900	2.100
E	0.011	0.019	0.285	0.485
F	0.088	0.096	2.230	2.430
H	0.035	0.043	0.900	1.100
J	0.000	0.008	0.000	0.200
K1	0.004	0.012	0.100	0.300
K2	0.004	0.012	0.100	0.300
M1	0.063	0.071	1.610	1.810
M2	0.045	0.053	1.153	1.353
N1	0.095	0.103	2.420	2.620
N2	0.082	0.090	2.080	2.280

Revised: 02/23/17

Part Numbering



Part Marking

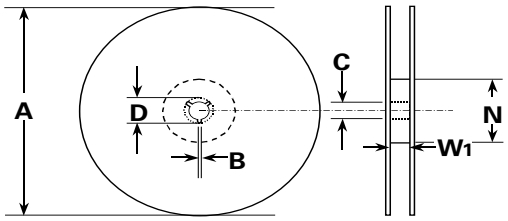


Packing Options

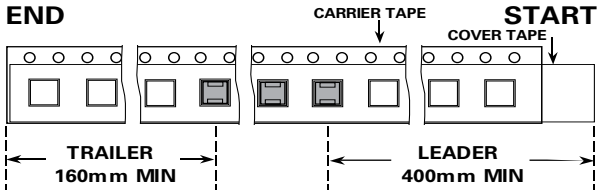
Package Type	Description	Quantity	Added Suffix	Industry Standard
Q22	3.3x3.3 QFN Tape and Reel Pack	5000	RP	EIA-481-D

Tape and Reel Specifications — 3.3x3.3 QFN

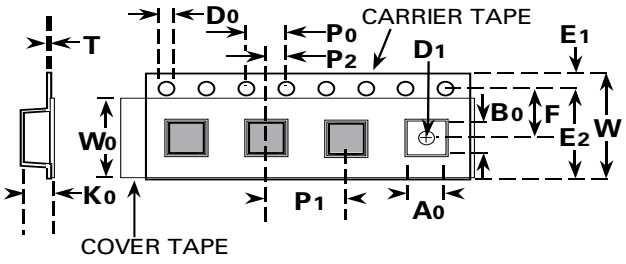
Reel Dimension



Tape Leader and Trailer Dimensions



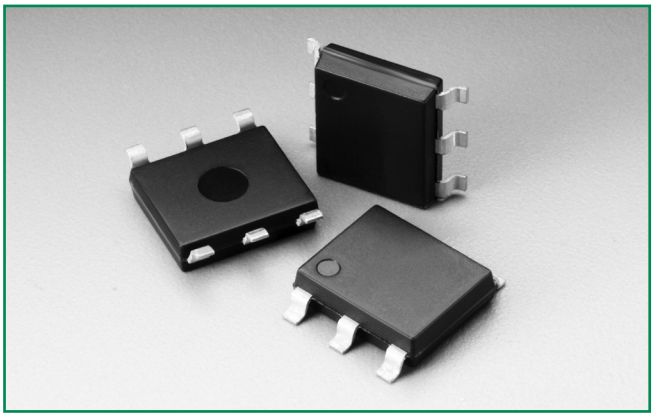
Tape Dimension Items



Symbols	Description	Inches		Millimeters	
		Min	Max	Min	Max
A	Reel Diameter	N/A	12.992	N/A	330.0
B	Drive Spoke Width	0.059	N/A	1.50	N/A
C	Arbor Hole Diameter	0.504	0.531	12.80	13.50
D	Drive Spoke Diameter	0.795	N/A	20.20	N/A
N	Hub Diameter	1.969	N/A	50.00	N/A
W_1	Reel Inner Width at Hub	0.488	0.567	12.40	14.40
A_0	Pocket Width at Bottom	0.138	0.146	3.50	3.70
B_0	Pocket Length at Bottom	0.138	0.146	3.50	3.70
D_0	Feed Hole Diameter	0.059	0.063	1.50	1.60
D_1	Pocket Hole Diameter	0.059	N/A	1.50	N/A
E_1	Feed Hole Position 1	0.065	0.073	1.65	1.85
E_2	Feed Hole Position 2	0.400	0.408	10.15	10.35
F	Feed Hole Center - Pocket Hole Center 2	0.215	0.219	5.45	5.55
K_0	Pocket Depth	0.039	0.051	1.00	1.30
P_0	Feed Hole Pitch	0.153	0.161	3.90	4.10
P_1	Component Spacing	0.311	0.319	7.90	8.10
P_2	Feed Hole Center - Pocket Hole Center 1	0.077	0.081	1.90	2.05
T	Carrier Tape Thickness	0.010	0.014	0.25	0.35
W	Embossed Carrier Tape Width	0.453	0.484	11.50	12.30
W_0	Cover Tape Width	0.358	0.366	9.10	9.30

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

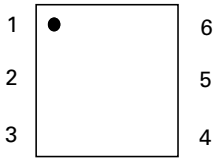
MC Multiport Series - MS-013



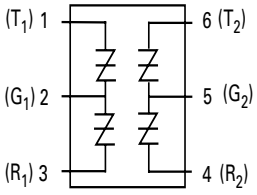
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Description

The MC Multiport Series MS-013 are low capacitance SIDACtor® thyristors designed to protect broadband equipment from damaging overvoltage transients.

The series provides a dual port surface mount solution that enables equipment to comply with various global regulatory standards while limiting the impact to broadband signals.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Two-pair protection
- 40% lower capacitance than our Baseband Protectors, for applications that demand greater signal integrity
- Replaces four discrete components
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Enhanced Level
- ITU K.20/21/45 Basic Level
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T= 2.2 Amps	Capacitance
		V	V	V	V	mA min	mA max	A max	V max	
		Pins 1-2, 3-2, 4-5, 6-5		Pins 1-3, 4-6						
P0084UCMCLxx	P0084UCMC	6	25	12	50	50	800	2.2	8	See Capacitance Values Table
P0304UCMCLxx	P0304UCMC	25	40	50	80	50	800	2.2	8	
P0644UCMCLxx	P0644UCMC	58	77	116	154	150	800	2.2	8	
P0724UCMCLxx	P0724UCMC	65	88	130	176	150	800	2.2	8	
P0904UCMCLxx	P0904UCMC	75	98	150	196	150	800	2.2	8	
P1104UCMCLxx	P1104UCMC	90	130	180	260	150	800	2.2	8	
P1304UCMCLxx	P1304UCMC	120	160	240	320	150	800	2.2	8	

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional.
- **XX** Part Number Suffix: **'TP'** (Tube Pack) or **'RP'** (Reel Pack).

Table continues on next page.

Revised: 02/23/17

Electrical Characteristics (continued)

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T= 2.2 Amps	Capacitance
		V	V	V	V	mA min	mA max	A max	V max	
		Pins 1-2, 3-2, 4-5, 6-5		Pins 1-3, 4-6						
P1504UCMCLxx	P1504UCMC	140	180	280	360	150	800	2.2	8	See Capacitance Values Table
P1804UCMCLxx	P1804UCMC	170	220	340	440	150	800	2.2	8	
P2304UCMCLxx	P2304UCMC	190	260	380	520	150	800	2.2	8	
P2604UCMCLxx	P2604UCMC	220	300	440	600	150	800	2.2	8	
P3104UCMCLxx	P3104UCMC	275	350	550	700	150	800	2.2	8	
P3504UCMCLxx	P3504UCMC	320	400	600	800	150	800	2.2	8	

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional.
- **XX** Part Number Suffix: '**TP'** (Tube Pack) or '**RP'** (Reel Pack).

Capacitance Values

Part Number	pF Pin 1-2 / 3-2 (4-5 / 6-5) Tip-Ground, Ring-Ground		pF Pin 1-3 (4-6) Tip-Ring	
	MIN	MAX	MIN	MAX
P0084UCMCLxx	35	75	20	45
P0304UCMCLxx	25	45	10	25
P0644UCMCLxx	55	85	30	50
P0724UCMCLxx	50	75	25	45
P0904UCMCLxx	45	70	25	40
P1104UCMCLxx	45	70	25	40
P1304UCMCLxx	40	60	20	35
P1504UCMCLxx	35	55	20	35
P1804UCMCLxx	35	50	15	30
P2304UCMCLxx	30	50	15	30
P2604UCMCLxx	30	45	15	30
P3104UCMCLxx	30	45	15	25
P3504UCMCLXx	25	40	15	25

Note: Off-state capacitance (C_O) is measured at 1 MHz with a 2 V bias.

Surge Ratings

Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
C	50	500	400	200	150	200	175	100	200	30	500

Notes:

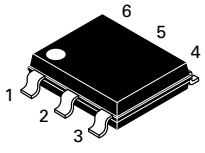
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

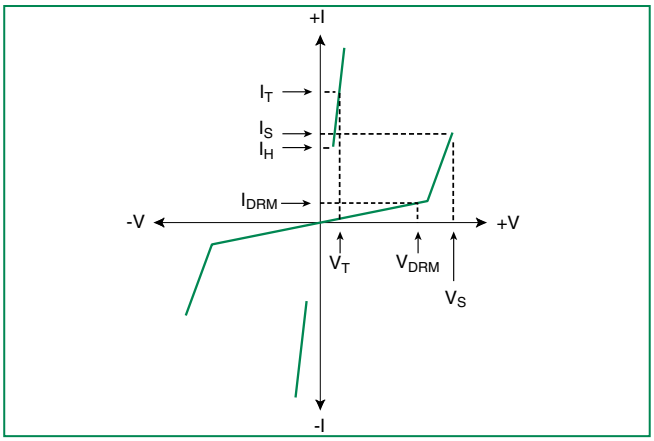
Revised: 02/23/17

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

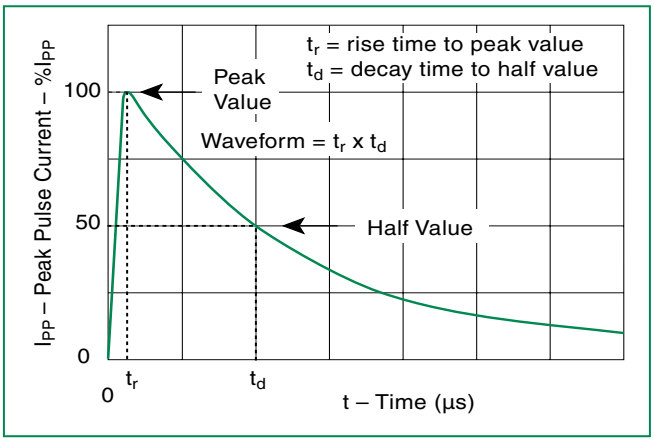
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified MS-013 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

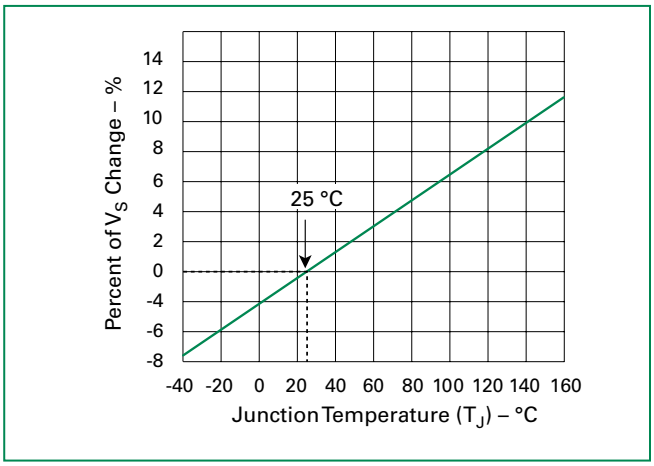
V-I Characteristics



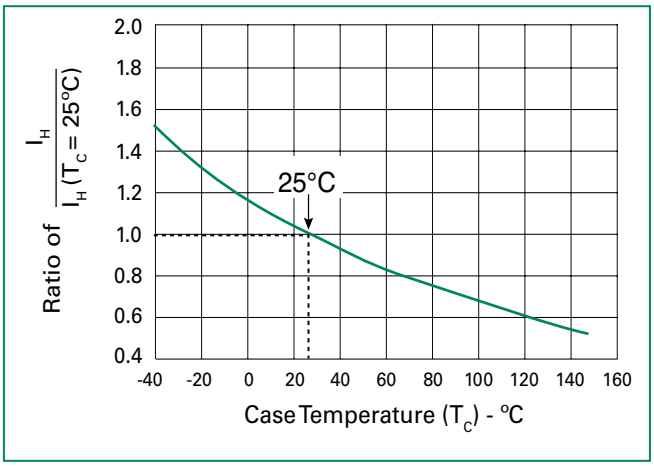
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature



Additional Information

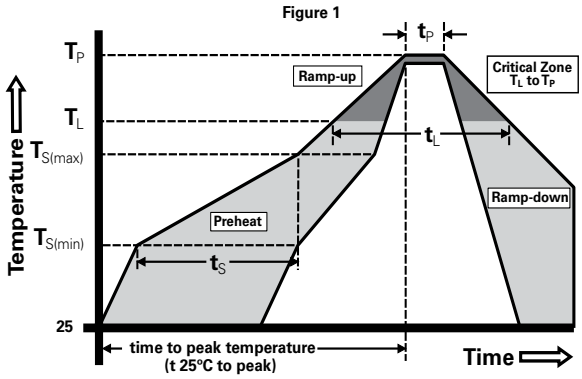
Datasheet | **Resources** | **Samples**

Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



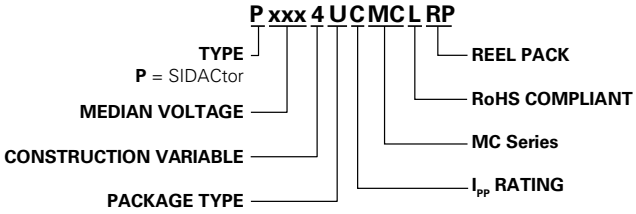
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

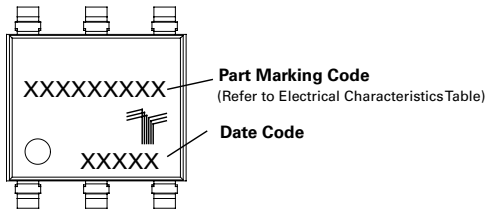
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering



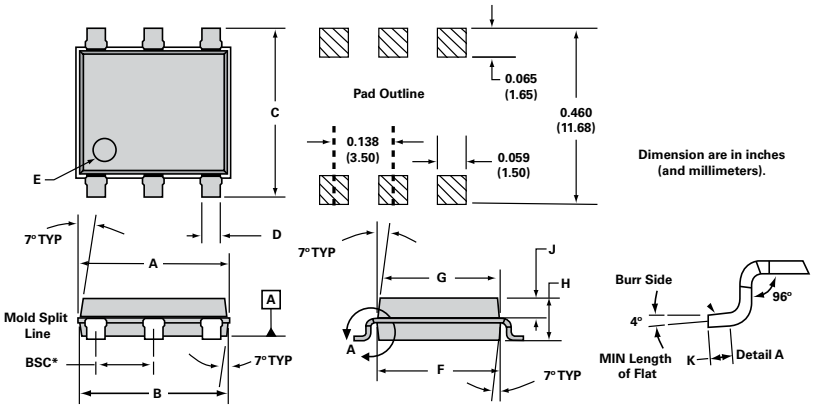
Part Marking



Revised: 02/23/17

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Dimensions — MS-013



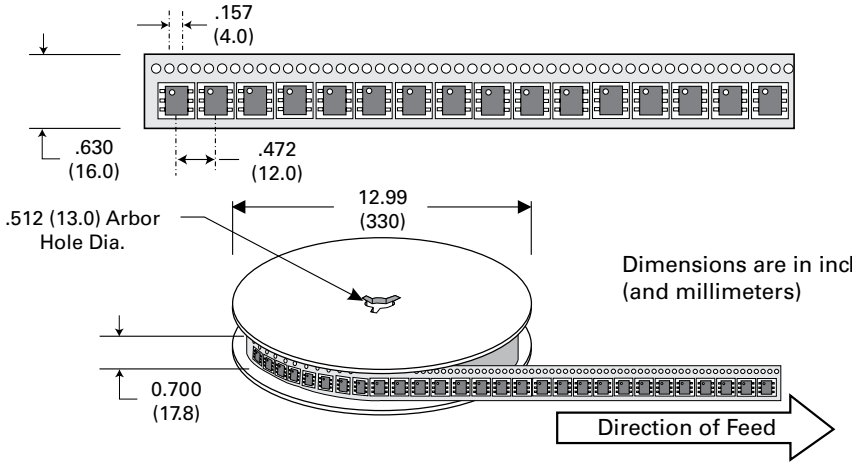
Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.360	0.364	9.14	9.25
B	0.352	0.356	8.94	9.04
C	0.400	0.412	10.16	10.46
D	0.043	0.045	1.09	1.13
E	0.047	0.055	1.19	1.40
F	0.293	0.297	7.44	7.54
G	0.289	0.293	7.34	7.44
H	0.089	0.093	2.26	2.36
J	0.041	0.049	1.04	1.24
K	0.020		0.51	
BSC*	0.133	0.143	3.38	3.63

* BSC = **B**asic **S**pacing between **C**enters

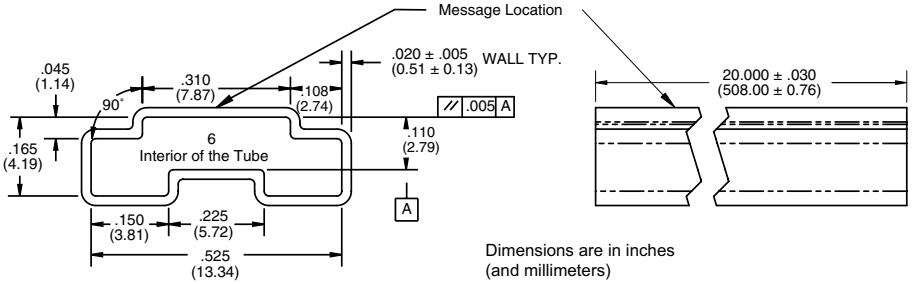
Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
U	Modified MS-013 6-pin Tape and Reel Pack	1500	RP	EIA-481-D
	Modified MS-013 6-pin Tube Pack	500 (50 per tube)	TP	N/A

Tape and Reel Specification — MS-013



Tube Pack Dimensions — MS-013



SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Littelfuse
Expertise Applied | Answers Delivered

MC Series - DO-214

Description

The MC Series DO-214 are low capacitance SIDACtor® components designed to protect broadband equipment such as VOIP, DSL modems and DSLAMs from damaging overvoltage transients.

The series provides a surface mount solution that enables equipment to comply with global regulatory standards while limiting the impact to broadband signals.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- 40% lower capacitance than our Baseband Protectors, for applications that demand greater signal integrity
- RoHS Compliant and Halogen-Free
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)
- Fails short circuit when surged in excess of ratings

Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation

NOT APPLICABLE

Schematic Symbol

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Enhanced Level*
- ITU K.20/21/45 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

*A-rated parts require series resistance

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	Capacitance @1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P0080SAMCLRP	P-8AM	6	25	50	800	2.2	4	10	35
P0220SAMCLRP	P02AM	15	32	50	800	2.2	4	10	35
P0300SAMCLRP	P03AM	25	40	50	800	2.2	4	10	35
P0080SCMCLRP	P-8CM	6	25	50	800	2.2	4	25	60
P0220SCMCLRP	P02CM	15	32	50	800	2.2	4	25	60
P0300SCMCLRP	P03CM	25	40	50	800	2.2	4	15	40
P0640SCMCLRP	P06CM	58	77	150	800	2.2	4	50	80
P0720SCMCLRP	P07CM	65	88	150	800	2.2	4	50	75
P0900SCMCLRP	P09CM	75	98	150	800	2.2	4	40	70
P1100SCMCLRP	P11CM	90	130	150	800	2.2	4	40	70
P1300SCMCLRP	P13CM	120	160	150	800	2.2	4	35	60
P1500SCMCLRP	P15CM	140	180	150	800	2.2	4	30	55
P1800SCMCLRP	P18CM	170	220	150	800	2.2	4	30	50
P2100SCMCLRP	P21CM	180	240	150	800	2.2	4	30	50
P2300SCMCLRP	P23CM	190	260	150	800	2.2	4	30	50
P2600SCMCLRP	P26CM	220	300	150	800	2.2	4	30	45
P3100SCMCLRP	P31CM	275	350	150	800	2.2	4	30	45
P3500SCMCLRP	P35CM	320	400	150	800	2.2	4	25	50
P4500SCMCLRP	P45CM	400	530	50	800	2.2	4	25	45

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional.

Revised: 02/23/17

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Surge Ratings

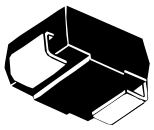
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
A	20	150	150	90	50	75	75	45	75	25	500
C	50	500	400	200	150	200	175	100	200 [3]	35	500

Notes:

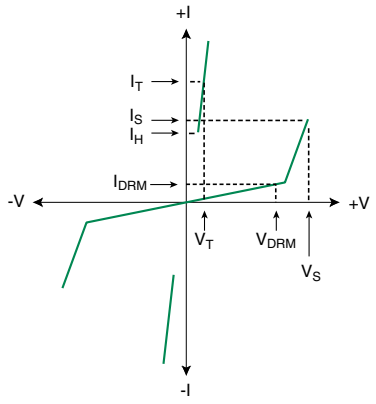
1 Current waveform in µs
2 Voltage waveform in µs
3 For surge rating of P4500SCMCLRP 10/700µs min=150A

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

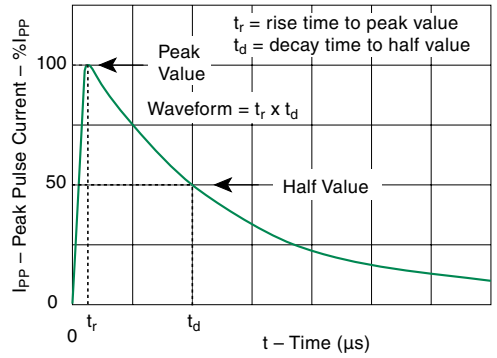
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
DO-214AA 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	90	°C/W

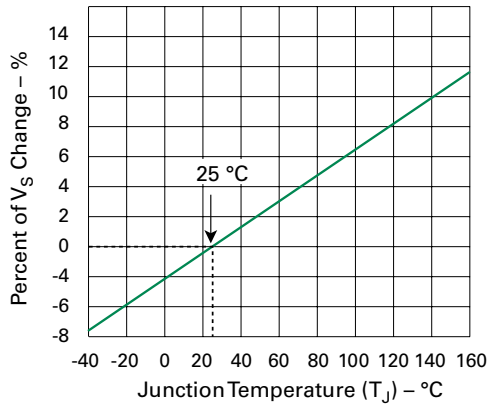
V-I Characteristics



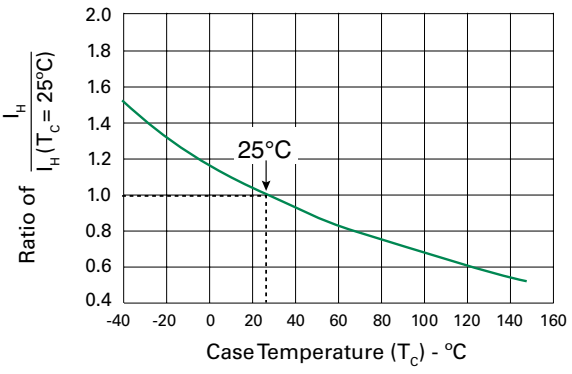
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

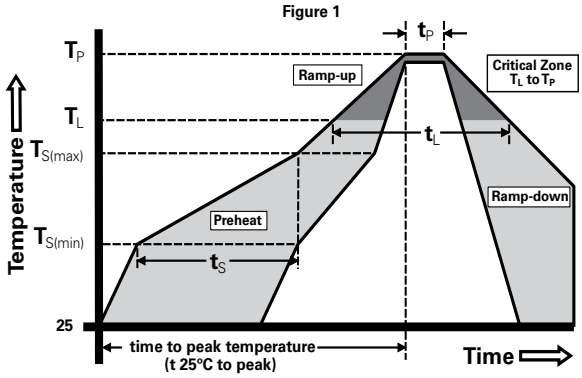


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85% RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100% RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85% RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

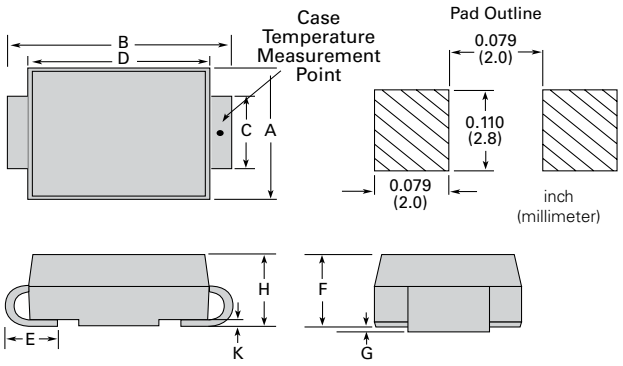
Additional Information

Datasheet | **Resources** | **Samples**

Revised: 02/23/17

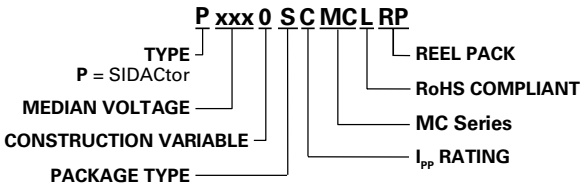
SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Dimensions — DO-214AA

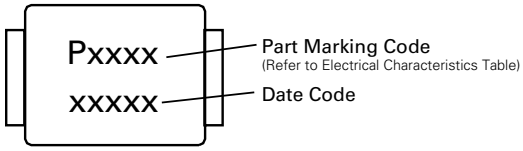


Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.130	0.156	3.30	3.95
B	0.201	0.220	5.10	5.60
C	0.077	0.087	1.95	2.20
D	0.159	0.181	4.05	4.60
E	0.030	0.063	0.75	1.60
F	0.075	0.096	1.90	2.45
G	0.002	0.008	0.05	0.20
H	0.077	0.104	1.95	2.65
K	0.006	0.016	0.15	0.41

Part Numbering



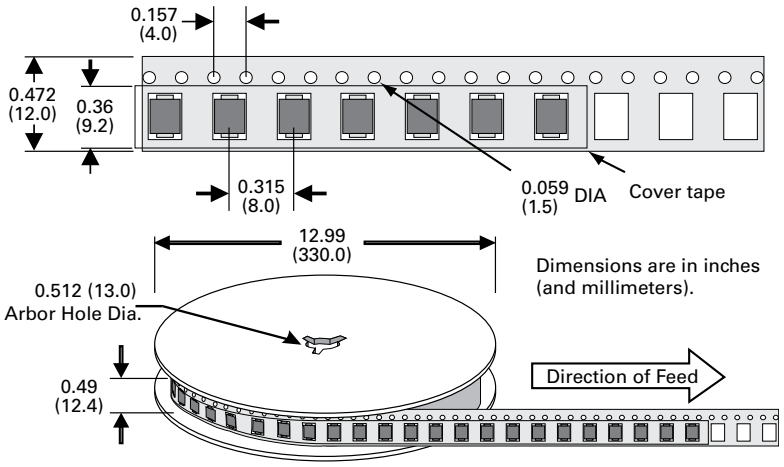
Part Marking



Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
S	DO-214AA Tape & Reel Pack	2500	N/A	EIA-481-D

Tape and Reel Specification — DO-214AA

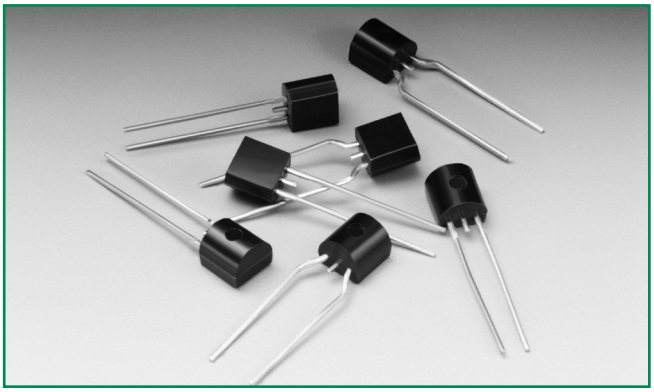


SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Littelfuse®
Expertise Applied | Answers Delivered

MC Series - TO-92

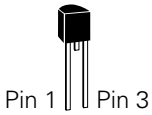
RoHS



Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol

Description

The MC Series TO-92 are low capacitance SIDACtor® thyristors designed to protect broadband CPE equipment such as VoIP and DSL Modems from damaging overvoltage transients.

The series provides a through-hole solution that enables CPE equipment to comply with global regulatory standards while limiting the impact to broadband signals.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit
- Fails short circuit when surged in excess of ratings
- RoHS Compliant
- 40% lower capacitance than our Baseband Protectors, for applications that demand greater signal integrity
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Enhanced Level
- ITU K.20/21/45 Basic Level
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	Capacitance @1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P0080ECMCLxxx	P0080ECMC	6	25	50	800	2.2	4	35	75
P0300ECMCLxxx	P0300ECMC	25	40	50	800	2.2	4	25	45
P0640ECMCLxxx	P0640ECMC	58	77	150	800	2.2	4	55	85
P0720ECMCLxxx	P0720ECMC	65	88	150	800	2.2	4	50	75
P0900ECMCLxxx	P0900ECMC	75	98	150	800	2.2	4	45	70
P1100ECMCLxxx	P1100ECMC	90	130	150	800	2.2	4	45	70
P1300ECMCLxxx	P1300ECMC	120	160	150	800	2.2	4	40	60
P1500ECMCLxxx	P1500ECMC	140	180	150	800	2.2	4	35	55
P1800ECMCLxxx	P1800ECMC	170	220	150	800	2.2	4	35	50
P2300ECMCLxxx	P2300ECMC	190	260	150	800	2.2	4	30	50
P2600ECMCLxxx	P2600ECMC	220	300	150	800	2.2	4	30	45
P3100ECMCLxxx	P3100ECMC	275	350	150	800	2.2	4	30	45
P3500ECMCLxxx	P3500ECMC	320	400	150	800	2.2	4	25	40

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional.
- **XXX** Part Number Suffix: '**AP**' (Ammo Pack), or '**RP1**' or '**RP2**' (Reel Pack),.

Revised: 02/23/17

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Surge Ratings

Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs Max
C	50	500	400	200	150	200	175	100	200	30	500

Notes:

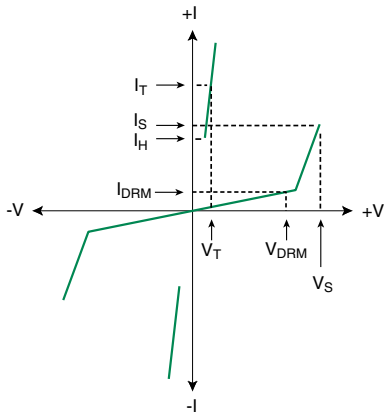
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

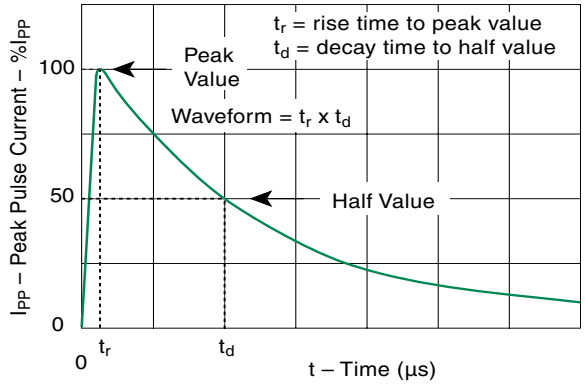
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
TO-92 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	90	°C/W

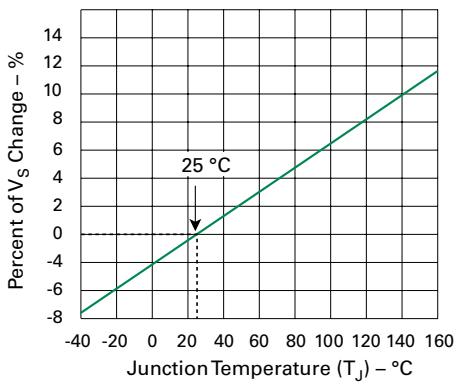
V-I Characteristics



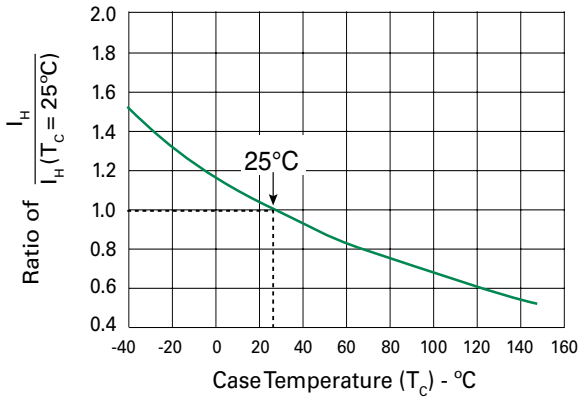
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

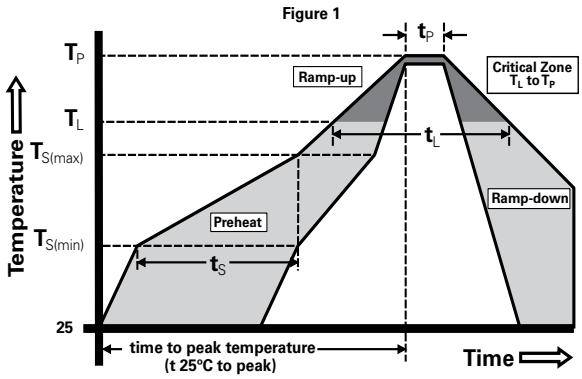


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

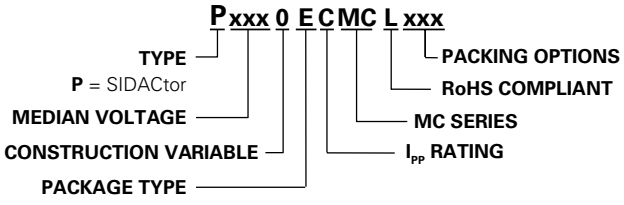
Additional Information

Datasheet | **Resources** | **Samples**

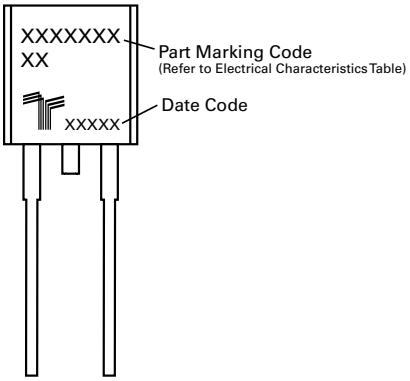
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering



Part Marking



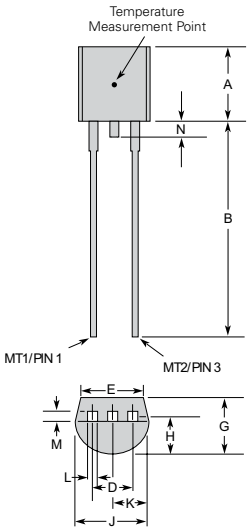
Revised: 02/23/17

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Packing Options

Package Type	Description	Packing Options Quantity	Added Suffix	Lead Spacing	Industry Standard
E	TO-92 Tape and Reel Pack	2000	RP1	0.1 inch (2.54mm)	EIA-481-D
			RP2	0.2 inch (5.08mm)	
	TO-92 Ammo Pack		AP	(Not applicable)	EIA-468-B
	TO-92 Bulk Pack		N/A	(Not applicable)	N/A

Dimensions — TO-92



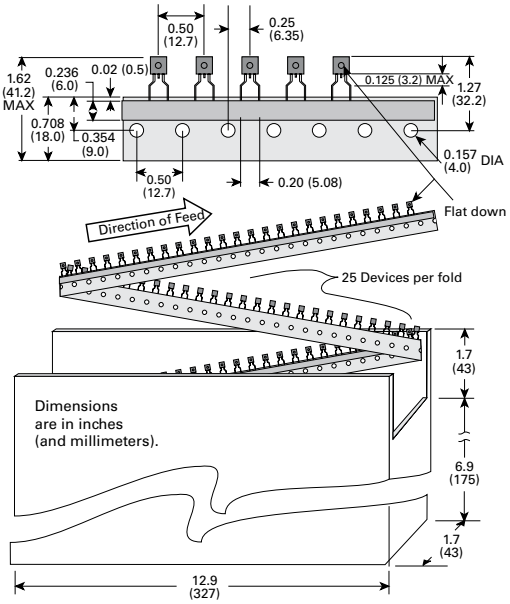
The TO-92 is designed to meet mechanical standards as set forth in JEDEC publication number 95.

	Inches		Millimeters	
	Min	Max	Min	Max
A	0.176	0.196	4.47	4.98
B	0.500		12.70	
D	0.095	0.105	2.41	2.67
E	0.150		3.81	
G	0.135	0.145	3.43	3.68
H	0.088	0.096	2.23	2.44
J	0.176	0.186	4.47	4.73
K	0.088	0.096	2.23	2.44
L	0.013	0.019	0.33	0.48
M	0.013	0.017	0.33	0.43
N		0.60		1.52

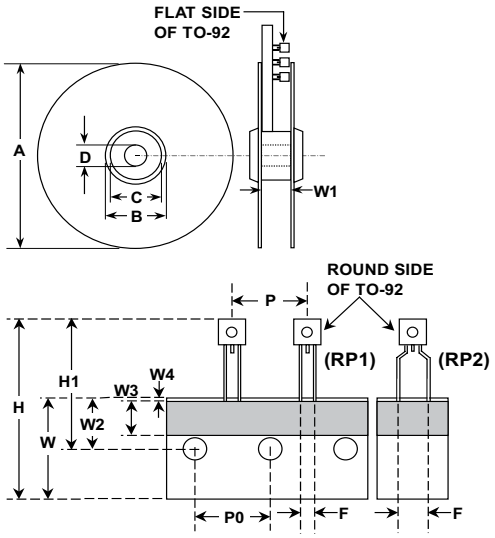
All leads are insulated from case. Case is electrically non-conductive. (Rated at 1600 $V_{(AC)\ RMS}$ for one minute from leads to case over the operating temperature range.)

Mold flash shall not exceed 0.13 mm per side.

Ammo Pack Specification — TO-92



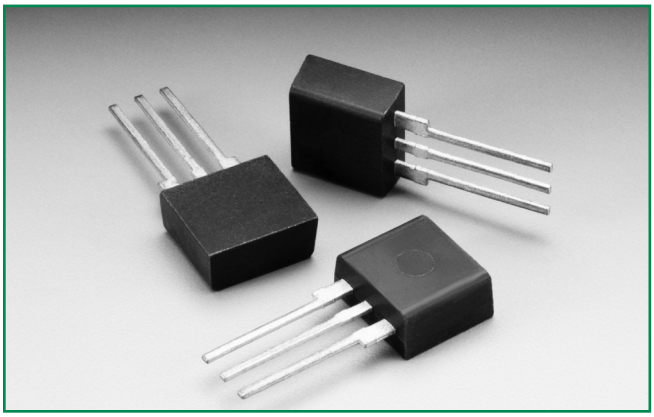
Tape and Reel Specification — TO-92



	Inches		Millimeters	
	Min	Max	Min	Max
A	N/A	14.173	N/A	360.0
B	4.016	N/A	102.0	N/A
C	3.386	N/A	86.0	N/A
D	0.795	N/A	20.2	N/A
W1	1.181	1.968	30.0	50.0
P	0.496	0.504	12.60	12.80
P0	0.498	0.502	12.65	12.75
F(for RP1)	0.090	0.110	2.29	2.80
F(for RP2)	0.182	0.244	4.63	6.19
H	N/A	1.673	N/A	42.50
H1	N/A	1.270	N/A	32.26
W	0.674	0.763	17.12	19.38
W2	0.354	0.370	8.25	9.75
W3	0.236	N/A	6.00	N/A
W4	0.020	N/A	0.50	N/A

Revised: 02/23/17

Balanced MC Series - Modified TO-220



Description

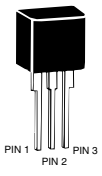
Balanced MC Series Modified TO-220 are low capacitance SIDACtor® components designed to protect broadband equipment from damaging overvoltage transients. The patented "Y" configuration also ensures balanced overvoltage protection that prevents a longitudinal to differential conversion.

The series provides a single port solution that enables equipment to comply with various global regulatory standards while limiting the impact to broadband signals.

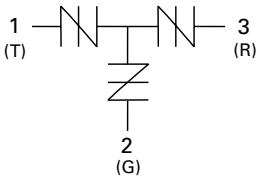
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Balanced overvoltage protection
- RoHS Compliant, Lead-Free, and Halogen-Free
- 40% lower capacitance than our Baseband Protectors, for applications that demand greater signal integrity
- Robust Modified TO-220 Package
- Custom lead forms available
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Enhanced Level
- ITU K.20/21/45 Basic
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-5
- YD/T 1082
- YD/T 993
- YD/T 950

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	Capacitance
		V min	V max	mA max	mA max	A max	V min	
		Pins 1-2, 3-2, 1-3		Pins 1-2, 3-2, 1-3				
P1553ACMCLxx	P1553ACMC	130	180	150	800	2.2	8	See Capacitance Values Table
P1803ACMCLxx	P1803ACMC	150	210	150	800	2.2	8	
P2103ACMCLxx	P2103ACMC	170	250	150	800	2.2	8	
P2353ACMCLxx	P2353ACMC	200	270	150	800	2.2	8	
P2703ACMCLxx	P2703ACMC	230	300	150	800	2.2	8	
P3203ACMCLxx	P3203ACMC	270	350	150	800	2.2	8	
P3403ACMCLxx	P3403ACMC	300	400	150	800	2.2	8	
P5103ACMCLxx	P5103ACMC	420	600	150	800	2.2	8	

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional (unless otherwise noted).
- **XX** Part Number Suffix: '**RP'** (Reel Pack), **Blank** (Bulk Pack), or **'60'** (Type 60 lead form, Bulk Pack. Special order item – contact factory.)

Revised: 02/23/17

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

Capacitance Values

Part Number	pF Pin 1-2 / 3-2 Tip-Ground, Ring-Ground		pF Pin 1-3 Tip-Ring	
	MIN	MAX	MIN	MAX
P1553ACMCLxx	30	55	20	35
P1803ACMCLxx	30	60	15	30
P2103ACMCLxx	30	45	15	30
P2353ACMCLxx	25	45	15	30
P2703ACMCLxx	25	40	15	30
P3203ACMCLxx	25	40	15	30
P3403ACMCLxx	20	35	15	25
P5103ACMCLxx	20	30	10	20

Note: Off-state capacitance (C_O) is measured at 1 MHz with a 2 V bias.

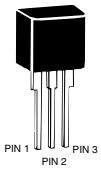
Surge Ratings

Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2x/0 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
C	50	500	400	200	150	200	175	100	200	30	500

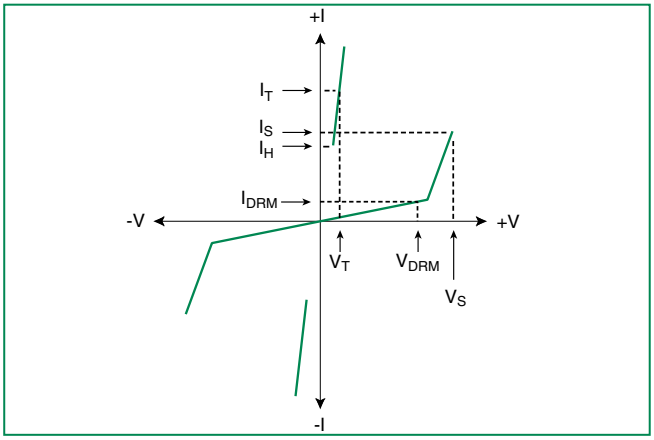
Notes:

1 Current waveform in µs
2 Voltage waveform in µs
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

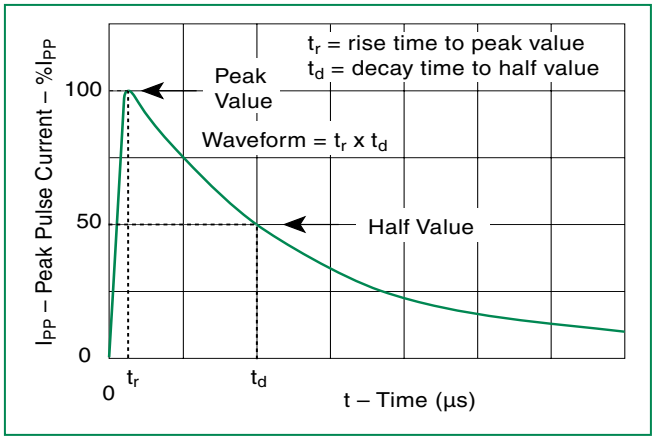
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified TO-220 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	50	°C/W

V-I Characteristics

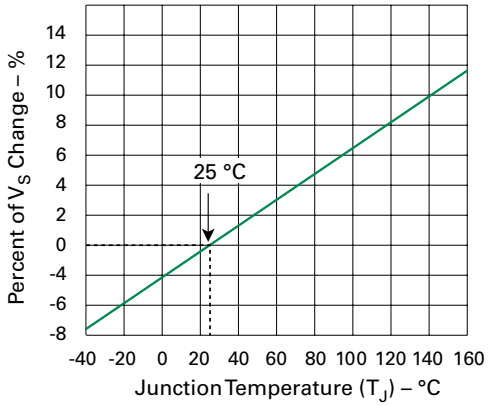


t_r x t_d Pulse Waveform

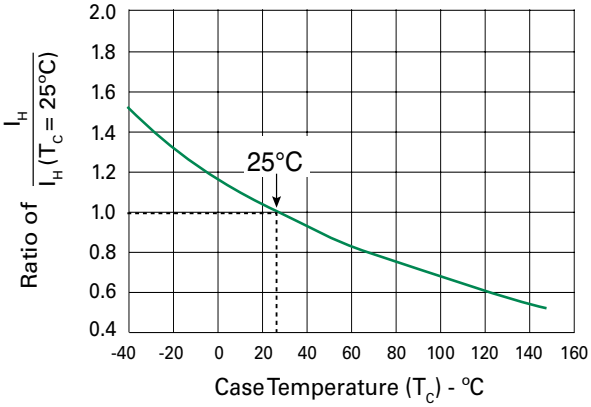


Revised: 02/23/17

Normalized V_S Change vs. Junction Temperature



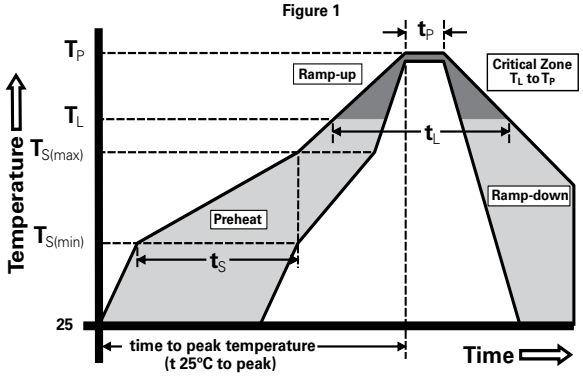
Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

Environmental Specifications

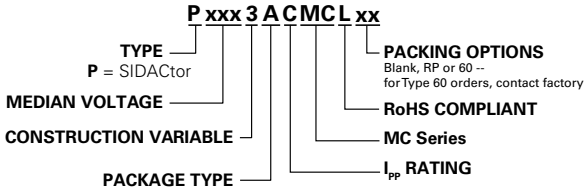
High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Revised: 02/23/17

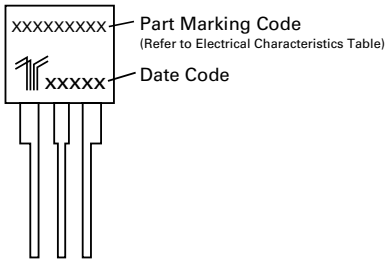
Littelfuse
Expertise Applied | Answers Delivered

SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

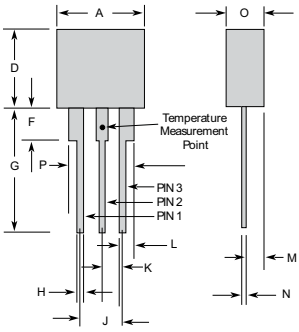
Part Numbering



Part Marking



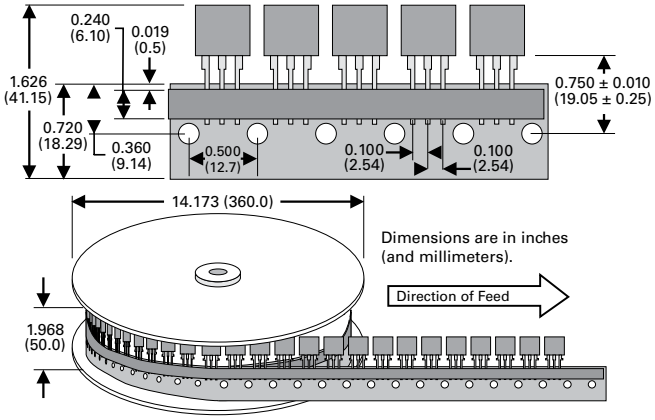
Dimensions - Modified TO-220



The modified TO-220 package is designed to meet mechanical standards as set forth in JEDEC publication number 95.

	Inches		Millimeters	
	Min	Max	Min	Max
A	0.400	0.410	10.16	10.42
D	0.360	0.375	9.14	9.53
F	0.110	0.130	2.80	3.30
G	0.540	0.575	13.71	14.61
H	0.025	0.035	0.63	0.89
J	0.195	0.205	4.95	5.21
K	0.095	0.105	2.41	2.67
L	0.060	0.075	1.52	1.90
M	0.070	0.085	1.78	2.16
N	0.018	0.024	0.46	0.61
O	0.178	0.188	4.52	4.78
P	0.290	0.310	7.37	7.87

Tape and Reel Specification — Modified TO-220



Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
A	Modified TO-220 Tape and Reel Pack	700	RP	EIA-468-B
	Modified TO-220 Bulk Pack	500	N/A	N/A
	Modified TO-220, Type 60 Lead Form Bulk Pack	500	60 (special order item, contact factory for details)	N/A

Additional Information

Datasheet | **Resources** | **Samples**

SIDACtor® Protection Thyristors
SLIC Protection

Littelfuse
Expertise Applied | Answers Delivered

Fixed Voltage Series - DO-214

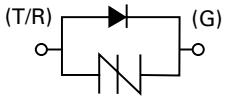
HF RoHS

Agency Approvals

Agency	Agency File Number
UL	E133083

Pinout Designation

Schematic Symbol



Description

Fixed Voltage Series DO-214 are uni-directional SIDACtor® components designed to protect SLICs (Subscriber Line Interface Circuit) from damaging overvoltage transients. The series provides single line protection using a fixed voltage switching component for negative surges. All positive surges are routed through an internal diode to a ground reference.

Features and Benefits

- RoHS compliant, lead-free, and halogen-free
- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Integrated diode for positive voltage surges
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building*
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

*A-rated parts require series resistance

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	V_F	Capacitance @1MHz, -2V bias	
		V min	V max	mA min	mA max	A max	V max	V max	pF	
									pF min	pF max
P0641SALRP	P61A	58	77	120	800	2.2	4	5	50	90
P0721SALRP	P71A	65	88	120	800	2.2	4	5	45	85
P0901SALRP	P91A	75	98	120	800	2.2	4	5	45	80
P1101SALRP	P01A	95	130	120	800	2.2	4	5	40	70
P1301SALRP	P131A	120	160	120	800	2.2	4	5	40	70
P1701SALRP	P17A	160	200	120	800	2.2	4	5	30	55
P0641SCLRP	P61C	58	77	120	800	2.2	4	5	65	200
P0721SCLRP	P71C	65	88	120	800	2.2	4	5	60	190
P0901SCLRP	P91C	75	98	120	800	2.2	4	5	60	180
P1101SCLRP	P01C	95	130	120	800	2.2	4	5	50	160
P1201SCLRP	P121C	105	140	120	800	2.2	4	5	50	160
P1301SCLRP	P131C	120	160	120	800	2.2	4	5	50	160
P1701SCLRP	P17C	160	200	120	800	2.2	4	5	40	130
P0641SDLRP	P61D	58	77	120	800	2.2	4	5	65	200
P0721SDLRP	P71D	65	88	120	800	2.2	4	5	60	190
P0901SDLRP	P91D	75	98	120	800	2.2	4	5	60	180
P1101SDLRP	P01D	95	130	120	800	2.2	4	5	50	160
P1301SDLRP	P131D	120	160	120	800	2.2	4	5	50	160
P1701SDLRP	P17D	160	200	120	800	2.2	4	5	40	130

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are not appropriate for positive ringing systems.

Revised: 02/23/17

SIDACtor® Protection Thyristors
SLIC Protection

Surge Ratings

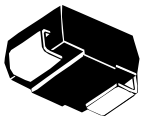
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [/]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
A	20	150	150	90	50	75	75	45	75	20	500
C	50	500	400	200	150	200	175	100	200	30	500
D	—	1000	800	—	—	—	—	200	350	50	1000

Notes:

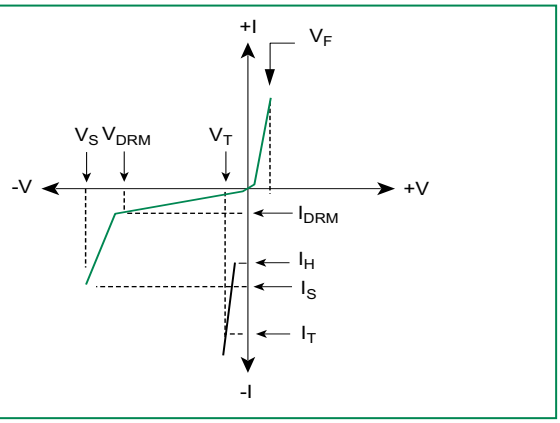
1 Current waveform in µs
2 Voltage waveform in µs
3 2/10 of P0641SDLRP and P0721SDLRP is 800A min

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

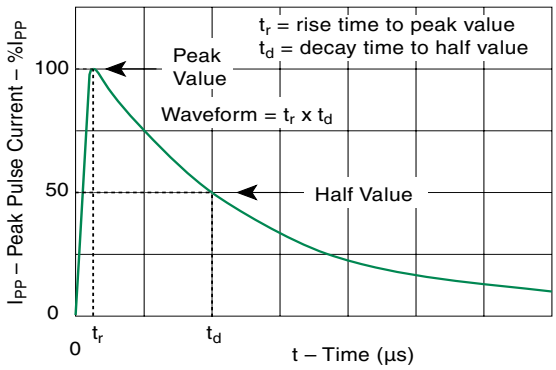
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
DO-214AA 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	90	°C/W

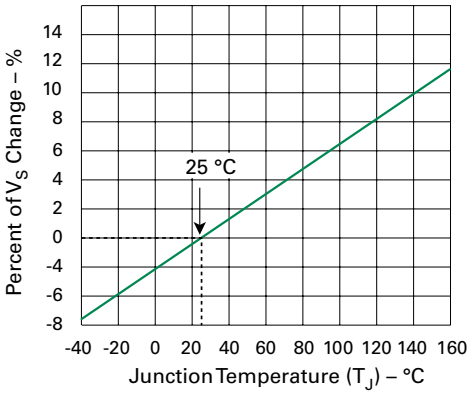
V-I Characteristics



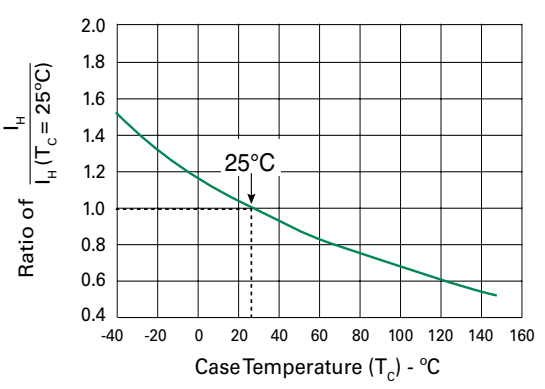
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

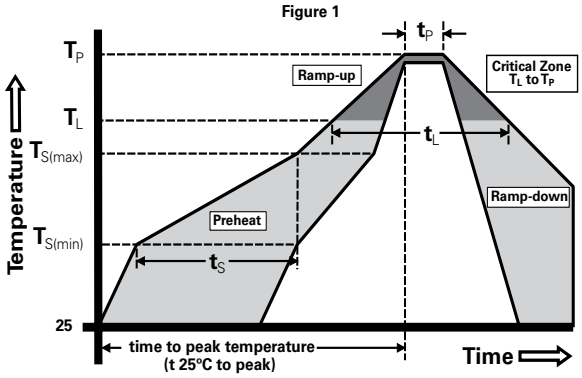


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification V-0

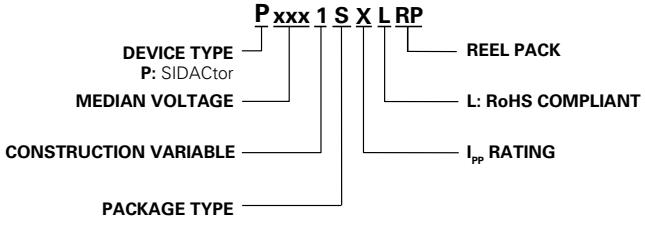
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

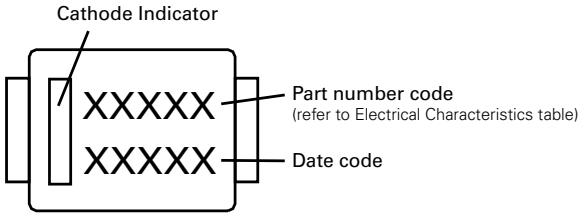
Additional Information

Datasheet | **Resources** | **Samples**

Part Numbering

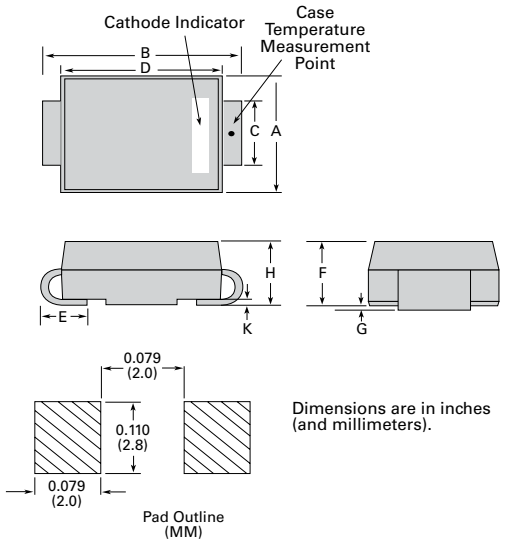


Part Marking



Revised: 02/23/17

Dimensions — DO-214AA

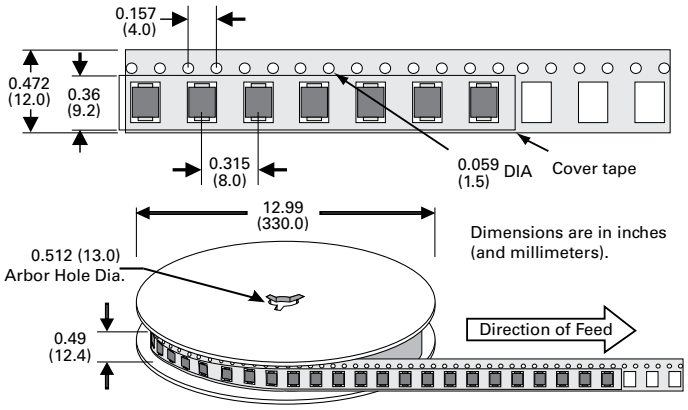


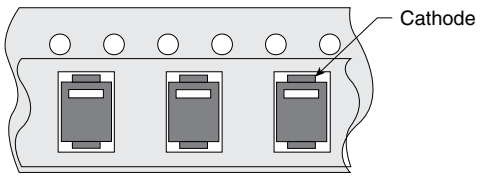
Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.130	0.156	3.30	3.95
B	0.201	0.220	5.10	5.60
C	0.077	0.087	1.95	2.20
D	0.159	0.181	4.05	4.60
E	0.030	0.063	0.75	1.60
F	0.075	0.096	1.90	2.45
G	0.002	0.008	0.05	0.20
H	0.077	0.104	1.95	2.65
K	0.006	0.016	0.15	0.41

Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
S	DO-214AA Tape & Reel Pack	2500	RP	EIA-481-D

Tape and Reel Specification — DO-214AA





SIDACtor® Protection Thyristors
SLIC Protection

Littelfuse®
Expertise Applied | Answers Delivered

Fixed Voltage TwinSLIC™ Series - Modified DO-214

HF RoHS

Description

Fixed Voltage Series Modified DO-214 are uni-directional SIDACtor® thyristors designed to protect SLICs (Subscriber Line Interface Circuit) from damaging overvoltage transients.

The series provides single port protection using fixed voltage switching components for negative surges. All positive surges are routed through internal diodes to a ground reference.

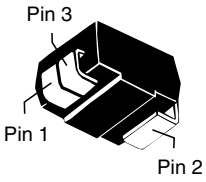
Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Integrated diodes for positive voltage surges
- Single-port protection
- RoHS Compliant and Halogen-Free
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

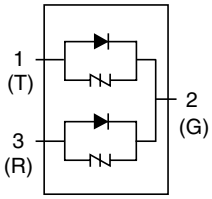
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level*
- ITU K.20/21 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

* Series resistance required

Additional Information

Datasheet | **Resources** | **Samples**

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	V_F	Capacitance
		V min	V max	mA min	mA max	A max	V max	V max	
		Pin 1-2, 3-2							
P0641CA2LRP	P62A	58	77	120	800	2.2	4	5	See Capacitance Values table
P0721CA2LRP	P72A	65	88	120	800	2.2	4	5	
P0901CA2LRP	P92A	75	98	120	800	2.2	4	5	
P1101CA2LRP	P02A	95	130	120	800	2.2	4	5	
P1301CA2LRP	P131A	120	160	120	800	2.2	4	5	
P1701CA2LRP	P17A	160	200	120	800	2.2	4	5	

Notes:
- Absolute maximum ratings measured at T_A = 25ºC (unless otherwise noted).
- Components are not appropriate for positive ringing systems.

Revised: 02/23/17

SIDACtor® Protection Thyristors
SLIC Protection

Capacitance Values

Part Number	pF Pin 1-2 / 3-2 Tip-Ground, Ring-Ground		pF Pin 1-3 Tip-Ring	
	MIN	MAX	MIN	MAX
P0641CA2LRP	40	70	20	45
P0721CA2LRP	35	70	20	45
P0901CA2LRP	30	65	20	40
P1101CA2LRP	25	55	15	35
P1301CA2LRP	25	45	15	30
P1701CA2LRP	25	40	15	25

Note: Off-state capacitance (C_O) is measured at 1 MHz with a 2 V bias.

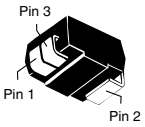
Surge Ratings

Series	I_{PP}									I_{TSM}	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]	50/60 Hz	
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
A	20	150	150	90	50	75	75	45	75	20	500

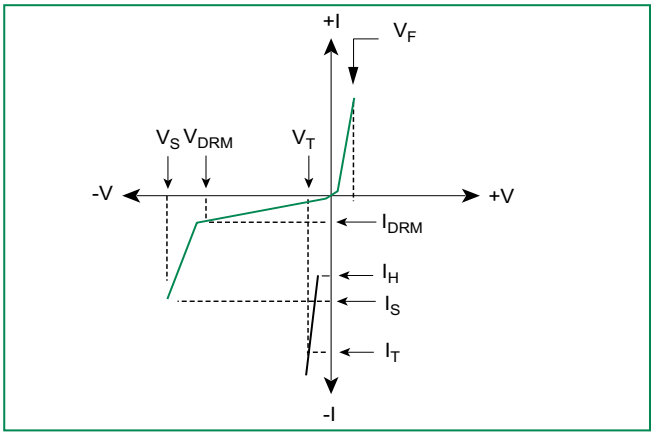
Notes:
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

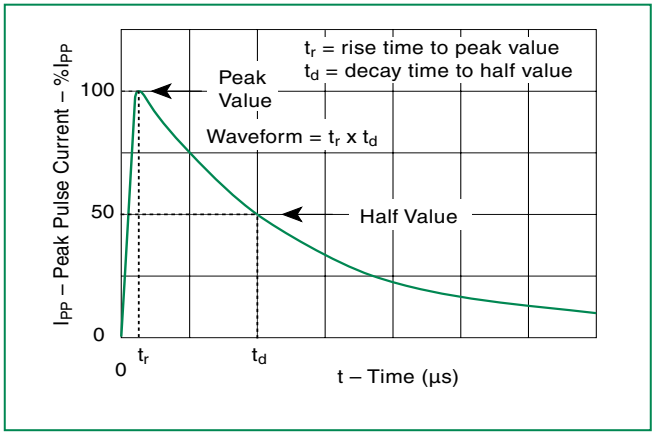
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified DO-214AA 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	85	°C/W

V-I Characteristics

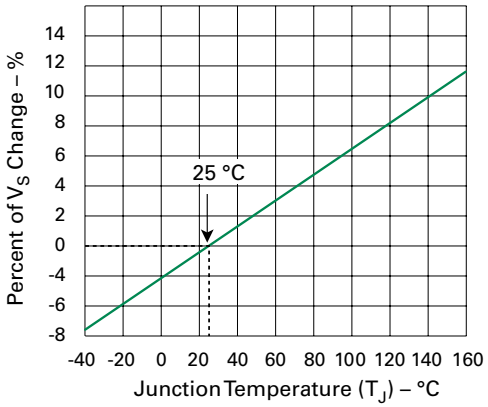


t_r x t_d Pulse Waveform

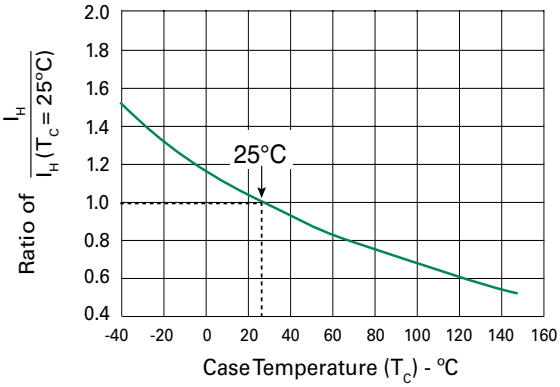


Revised: 02/23/17

Normalized V_S Change vs. Junction Temperature



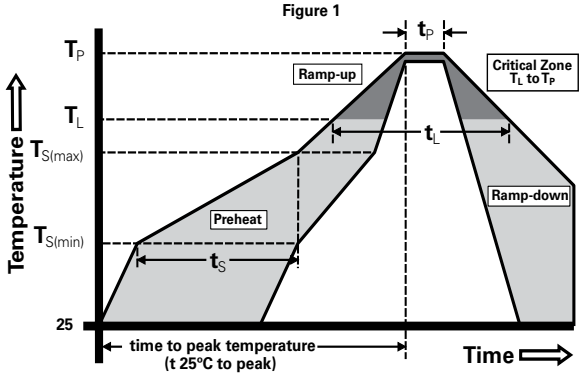
Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

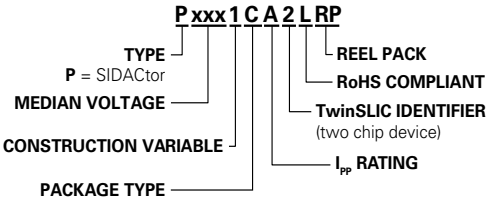
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C peak). JEDEC-J-STD-020, Level 1

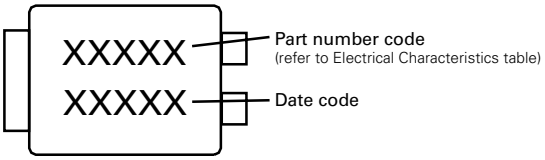
Revised: 02/23/17

SIDACtor® Protection Thyristors
SLIC Protection

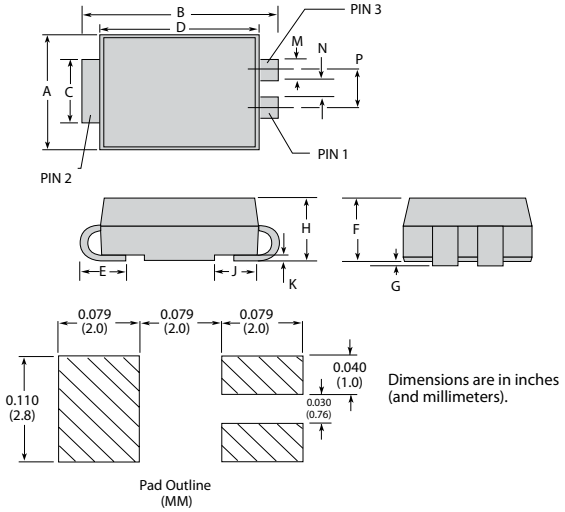
Part Numbering



Part Marking



Dimensions — Modified DO-214AA

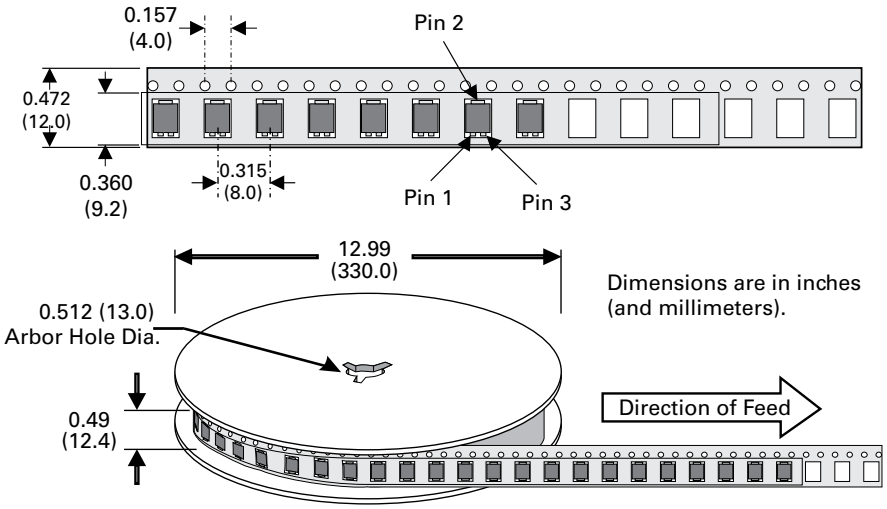


Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.130	0.156	3.30	3.95
B	0.201	0.220	5.10	5.60
C	0.077	0.087	1.95	2.20
D	0.159	0.181	4.05	4.60
E	0.030	0.063	0.75	1.60
F	0.075	0.096	1.90	2.45
G	0.002	0.008	0.05	0.20
H	0.077	0.104	1.95	2.65
K	0.006	0.016	0.15	0.41
M	0.022	0.028	0.56	0.71
N	0.027	0.033	0.69	0.84
P	0.052	0.058	1.32	1.47

Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
C	Modified DO-214AA 3-leaded Tape and Reel Pack	2500	RP	EIA-481-D

Tape and Reel Specification — Modified DO-214AA



SIDACtor® Protection Thyristors
SLIC Protection

Littelfuse®
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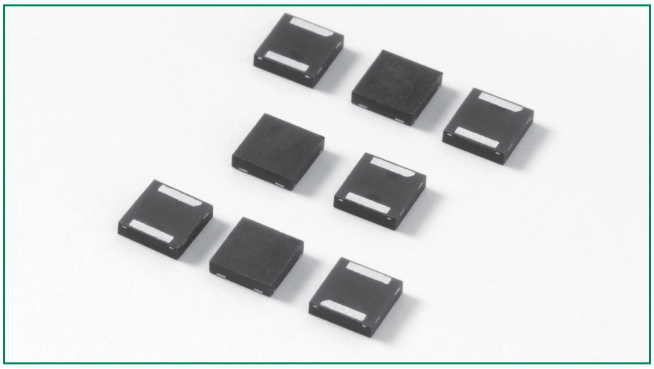
Fixed Voltage Q2L Series 3.3x3.3 QFN

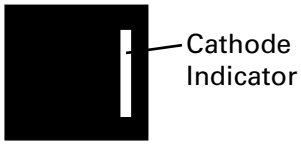
HF RoHS



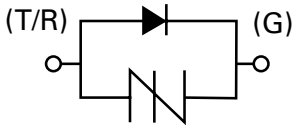
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Description

Fixed Voltage Q2L Series are uni-directional SIDACtor® thyristors designed to protect SLICs (Subscriber Line Interface Circuit) from damaging overvoltage transients.

The series provides single line protection using a fixed voltage switching component for negative surges. All positive surges are routed through an internal diode to a ground reference. The small size of the Q2L makes it ideal for high density applications.

Features and Benefits

- Integrated diode for positive voltage surges
- Low profile
- Small footprint QFN Package
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- RoHS Compliant and Halogen-Free
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/Enhanced Level
- ITU K.20/21/Basic Level
- GR 1089 Inter-building
- GR-1089 Intra-building
- IEC 61000-4-5 2nd editin
- YD/T 950
- YD/T 993
- YD/T 1082

Additional Information

Datasheet | **Resources** | **Samples**

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	V_F	Capacitance @1MHz @ 2V bias	
		V min	V max	mA min	mA max	A max	V max	V max	pF min	pF max
P0641Q22CLRP	P61C	58	77	120	800	2.2	4	5	35	75
P0721Q22CLRP	P71C	65	88	120	800	2.2	4	5	25	45
P0901Q22CLRP	P91C	75	98	120	800	2.2	4	5	55	85
P1101Q22CLRP	P10C	95	130	120	800	2.2	4	5	50	75
P1301Q22CLRP	P13C	120	160	120	800	2.2	4	5	45	70
P1701Q22CLRP	P17C	160	200	120	800	2.2	4	5	45	70

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are not appropriate for positive ringing systems.

Revised: 02/23/17

SIDACtor® Protection Thyristors
SLIC Protection

Surge Ratings

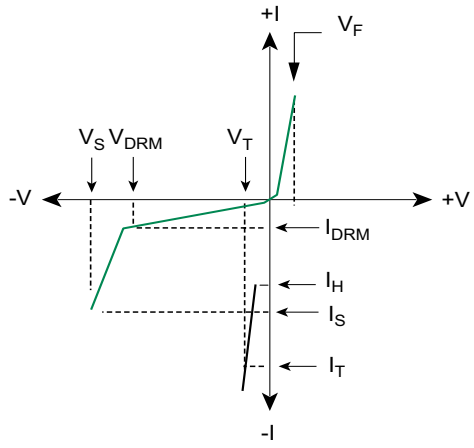
Series	I_{PP}					I_{TSM}	di/dt
	2/10µs	1.2/50µs/8/20µs	10/160µs	10/560µs	10/1000µs	50 / 60Hz	
	A min	A min	A min	A min	A min	A min	Amps/µs max
C	500	400	200	150	100	30	500

Notes:
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

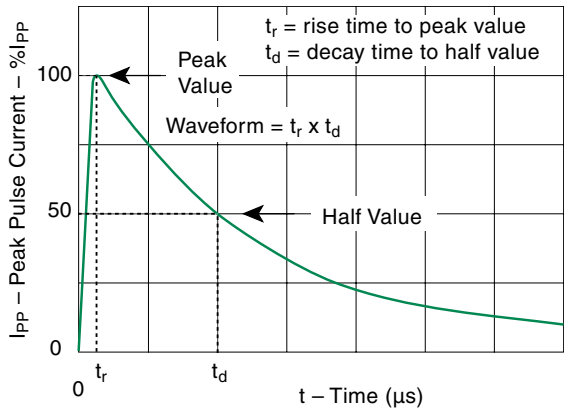
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
3.3x3.3 QFN 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	120	°C/W

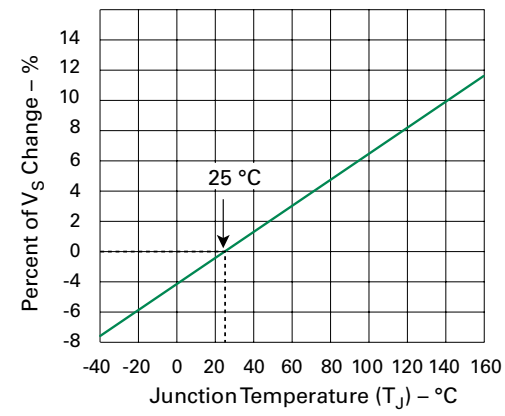
V-I Characteristics



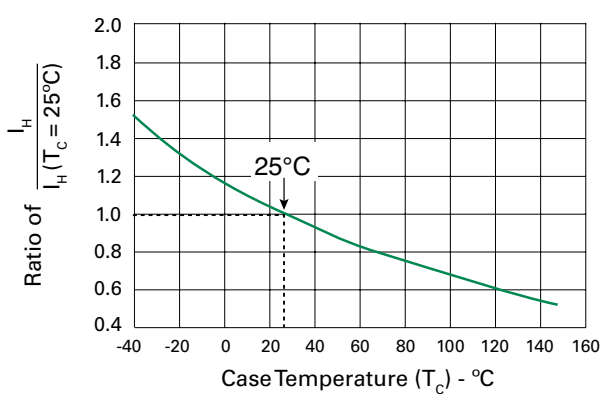
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

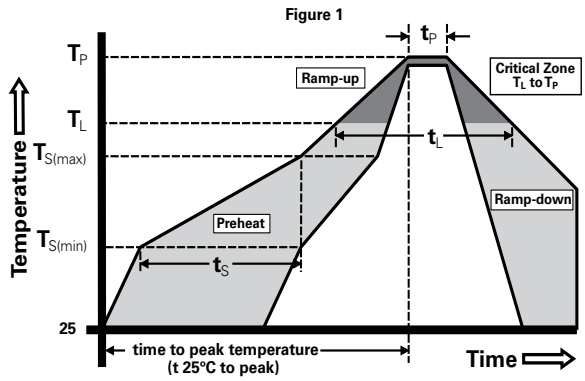


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



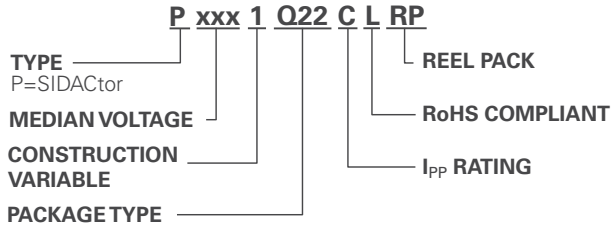
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

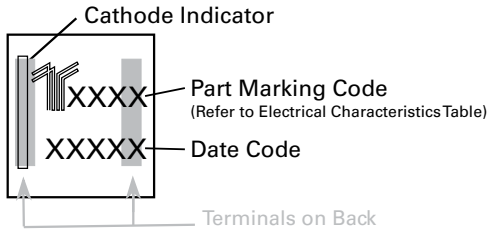
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{DC}) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering

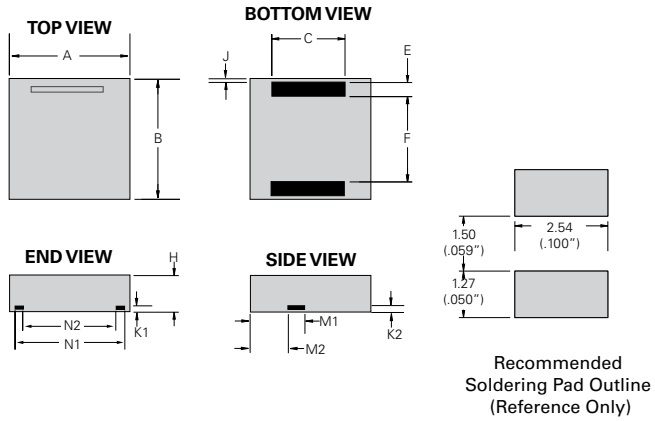


Part Marking



Revised: 02/23/17

Dimensions — 3.3x3.3 QFN



Recommended
Soldering Pad Outline
(Reference Only)

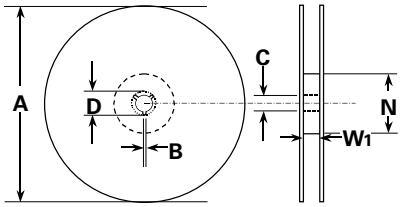
Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.126	0.134	3.200	3.400
B	0.126	0.134	3.200	3.400
C	0.075	0.083	1.900	2.100
E	0.011	0.019	0.285	0.485
F	0.088	0.096	2.230	2.430
H	0.035	0.043	0.900	1.100
J	0.000	0.008	0.000	0.200
K1	0.004	0.012	0.100	0.300
K2	0.004	0.012	0.100	0.300
M1	0.063	0.071	1.610	1.810
M2	0.045	0.053	1.153	1.353
N1	0.095	0.103	2.420	2.620
N2	0.082	0.090	2.080	2.280

Packing Options

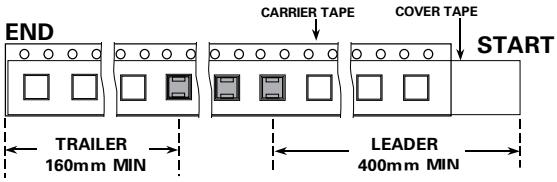
Package Type	Description	Quantity	Added Suffix	Industry Standard
Q22	3.3x3.3 QFN Tape and Reel Pack	5000	RP	EIA-481-D

Tape and Reel Dimension — 3.3x3.3 QFN

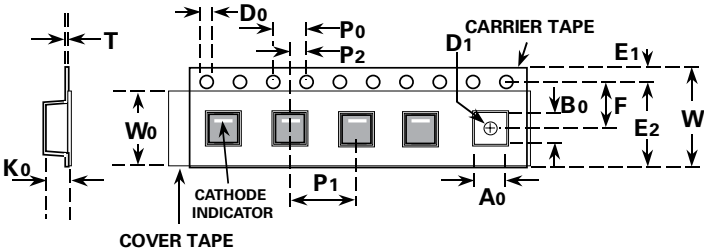
Reel Dimension



Tape Leader and Trailer Dimensions

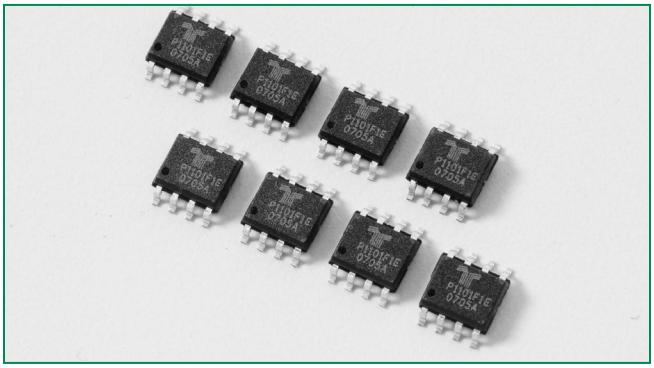


Tape Dimension Items



	Description	Inches		Millimeters	
		Min	Max	Min	Max
A	Reel Diameter	N/A	12.992	N/A	330.0
B	Drive Spoke Width	0.059	N/A	1.50	N/A
C	Arbor Hole Diameter	0.504	0.531	12.80	13.50
D	Drive Spoke Diameter	0.795	N/A	20.20	N/A
N	Hub Diameter	1.969	N/A	50.00	N/A
W_1	Reel Inner Width at Hub	0.488	0.567	12.40	14.40
A_0	Pocket Width at bottom	0.138	0.146	3.50	3.70
B_0	Pocket Length at bottom	0.138	0.146	3.50	3.70
D_0	Feed Hole Diameter	0.059	0.063	1.50	1.60
D_1	Pocket Hole Diameter	0.059	N/A	1.50	N/A
E_1	Feed hole position 1	0.065	0.073	1.65	1.85
E_2	Feed hole position 2	0.400	0.408	10.15	10.35
F	Feed hole center-Pocket hole	0.215	0.219	5.45	5.55
K_0	Pocket Depth	0.039	0.051	1.00	1.30
P_0	Feed Hole Pitch	0.153	0.161	3.90	4.10
P_1	Component Spacing	0.311	0.319	7.90	8.10
P_2	Feed hole center-Pocket hole	0.077	0.081	1.95	2.05
T	Carrier Tape Thickness	0.010	0.014	0.25	0.35
W	Embossed Carrier Tape Width	0.453	0.484	11.50	12.30
W_0	Cover Tape Width	0.358	0.366	9.10	9.30

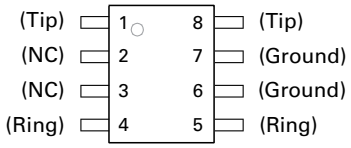
Fixed Voltage Enhanced Single Port Series - MS-012



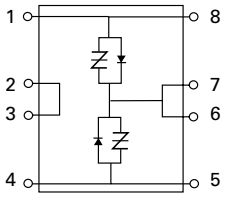
Agency Approvals

Agency	Agency File Number
UL	E133083

Pinout



Schematic Symbol



Description

The MS-012 packaged Fixed Voltage Enhanced Single Port Series are SIDACtor® components designed to protect sensitive SLICs (Subscriber Line Interface Circuit) from damaging overvoltage transients.

The series provides single port protection using a fixed voltage switching device for negative surges. Positive surges are routed though enhanced switching diodes to a ground reference. The series is also pin-to-pin compatible to industry standard programmable SO-8 SLIC protectors.

Features & Benefits

- Integrated fast switching diodes for positive voltage surges
- RoHS Compliant and Lead-Free
- Single port protection in one package
- Low voltage overshoot
- Low on-state voltage
- Pin-to-pin SO-8 compatible footprint
- Fails short circuit when surged in excess of ratings
- Does not degrade surge capability after multiple surge events within limit
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building*
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

* Series resistance required

Electrical Characteristics

Part Number	Marking	V_{DRM} @ I_{DRM}=5µA	V_S @ 100V/µs	I_H	I_S	I_T @ V_T	V_T @ I_T=1 Amps	V_F @ 25°	Capacitance
		V min	V max	mA min	mA max	A max	V max	V max	
P0641DF-1E	P0641F1E	58	77	150	800	1	5	5	See Capacitance Values Table
P0721DF-1E	P0721F1E	65	88	150	800	1	5	5	
P0901DF-1E	P0901F1E	75	98	150	800	1	5	5	
P0991DF-1E	P0991F1E	80	104	150	800	1	5	5	
P1001DF-1E	P1001F1E	85	110	150	800	1	5	5	
P1101DF-1E	P1101F1E	95	130	150	800	1	5	5	
P1301DF-1E	P1301F1E	120	160	150	800	1	5	5	
P1701DF-1E	P1701F1E	160	200	150	800	1	5	5	

Notes:
- Absolute maximum ratings measured at T_A = 25°C (unless otherwise noted).
- Components are not appropriate for positive ringing systems
- All electrical characteristics shown are defined from Tip (pins 1 & 8) to Ground (pins 6 & 7), and Ring (pins 4 & 5) to ground (pins 6 & 7)
- V_F < 8.5 volts @ 10 / 700µs, 37.5 Amps

Revised: 02/23/17

SIDACtor® Protection Thyristors
SLIC Protection

Capacitance Values

Part Number	pF Pin 1,8-6,7 / 4,5-6,7 Tip-Ground, Ring-Ground		pF Pin 1,8-4,5 Tip-Ring	
	MIN	MAX	MIN	MAX
P0641DF-1E	40	90	20	45
P0721DF-1E	35	85	20	45
P0901DF-1E	30	80	20	40
P0991DF-1E	25	75	15	35
P1001DF-1E	25	75	15	35
P1101DF-1E	25	70	15	30
P1301DF-1E	20	70	15	30
P1701DF-1E	20	70	15	30

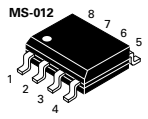
Note: Off-state capacitance (C_O) is measured at 1 MHz with a 2V bias

Surge Ratings

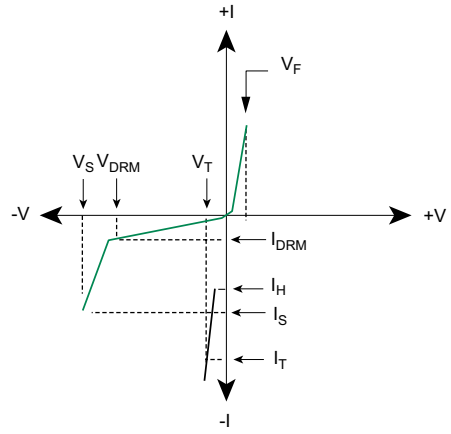
Series	I_{PP}				I_{TSM}	di/dt
	2/10µs	1.2/50µs/8/20µs	10/700/5/310µs	10/1000µs	600V_{RMS} 1s	
	A min	A min	A min	A min	A min	Amps/µs max
F	120	100	50	30	1	500

Notes:
- Peak pulse current rating (IPP) is repetitive and guaranteed for the life of the product that is in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

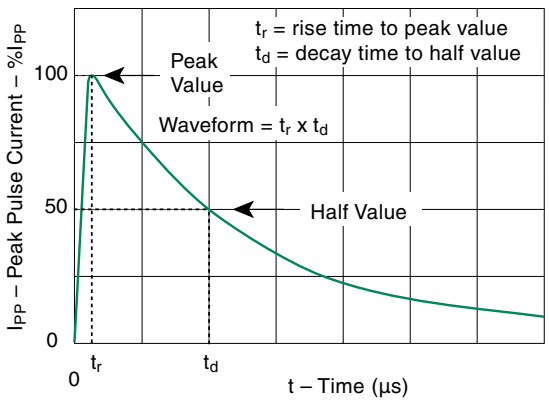
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	120	°C/W

V-I Characteristics

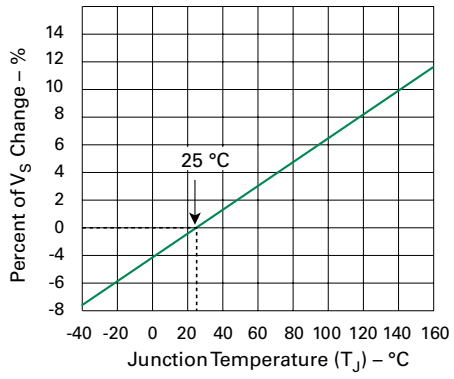


t_r x t_d Pulse Waveform

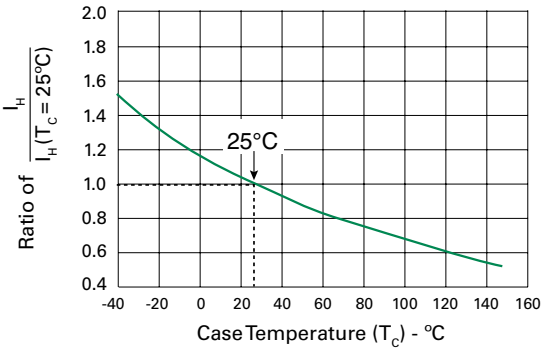


Revised: 02/23/17

Normalized V_S Change vs. Junction Temperature



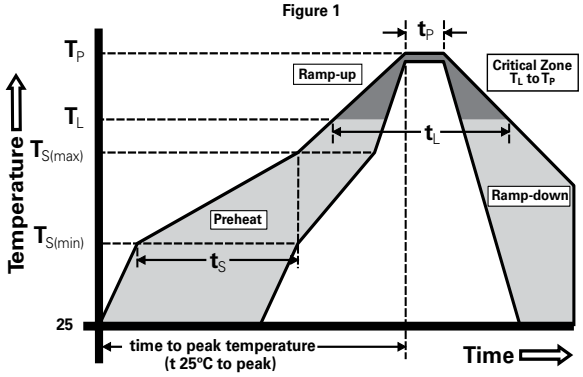
Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{DC}) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

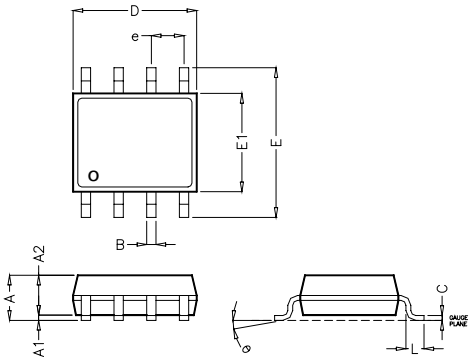
Additional Information

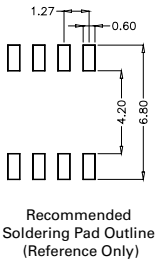
Datasheet | **Resources** | **Samples**

Revised: 02/23/17

SIDACtor® Protection Thyristors
SLIC Protection

Dimensions — MS-012



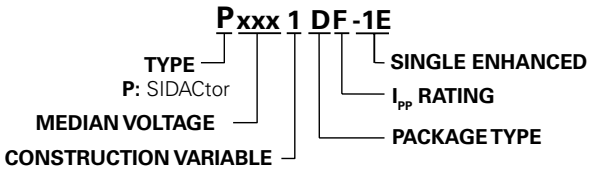


Recommended Soldering Pad Outline (Reference Only)

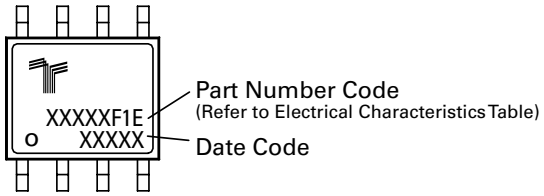
Dimension	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.043	0.065	1.25	1.65
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.17	0.25
D	0.189	0.197	4.80	5.00
E	0.228	0.244	5.80	6.20
E1	0.150	0.157	3.80	4.00
e	0.050 BSC*		1.27 BSC*	
L	0.016	0.050	0.40	1.27

* BSC = **B**asic **S**pacing between **C**enters

Part Numbering



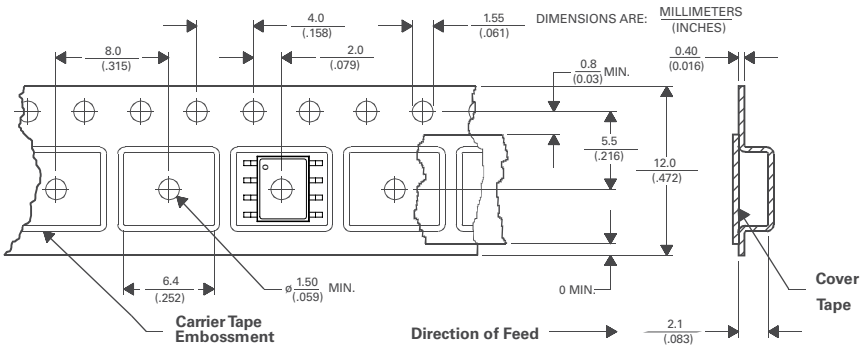
Part Marking

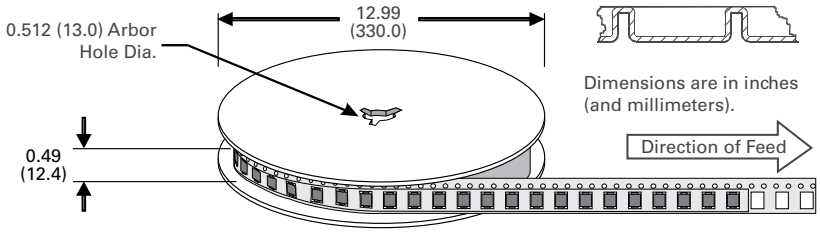


Packing Options

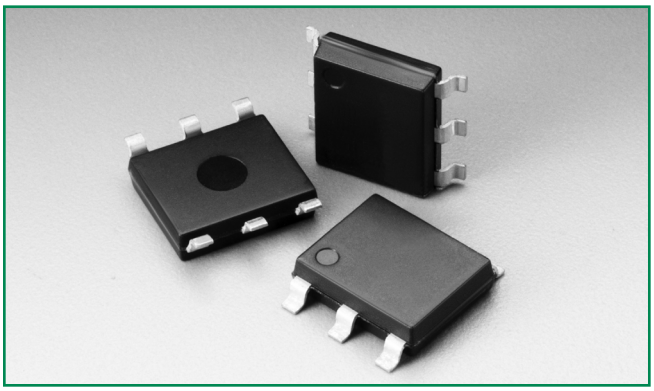
Package Type	Description	Quantity	Added Suffix	Industry Standard
D	MS-012 SMT 8-pin SOIC Tape and Reel Pack	2500	N/A	EIA-481-D

Tape and Reel Specifications — MS-012





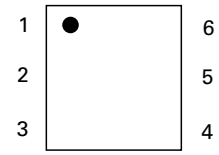
Fixed Voltage Multiport Series - MS-013



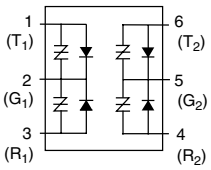
Agency Approvals

Agency	Agency File Number
UL	E133083

Pinout Designation



Schematic Symbol



Description

Fixed Voltage Multiport Series MS-013 are SIDACtor® components designed to protect sensitive SLIC (Subscriber Line Interface Circuit) devices from damaging overvoltage transients.

The series provides a high surge current rated dual port protection solution incorporating a fixed voltage switching threshold for negatives surges. All positive surges are routed through an internal diode to a ground reference.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Two-port protection
- Integrated diodes for positive voltage surges
- RoHS compliant and Halogen-free
- Replaces four discrete components
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level*
- ITU K.20/21 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5
- YD/T 1082
- YD/T 993
- YD/T 950

*A-rated parts require series resistance

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	V_F	Capacitance
		V min	V max	mA min	mA max	A max	V max	V max	
P0641UALxx	P0641UA	58	77	120	800	2.2	4	5	See Capacitance Values Table
P0721UALxx	P0721UA	65	88	120	800	2.2	4	5	
P0901UALxx	P0901UA	75	98	120	800	2.2	4	5	
P1101UALxx	P1101UA	95	130	120	800	2.2	4	5	
P1301UALxx	P1301UA	120	160	120	800	2.2	4	5	
P1701UALxx	P1701UA	160	200	120	800	2.2	4	5	
P0641UCLxx	P0641UC	58	77	120	800	2.2	4	5	
P0721UCLxx	P0721UC	65	88	120	800	2.2	4	5	
P0901UCLxx	P0901UC	75	98	120	800	2.2	4	5	
P1101UCLxx	P1101UC	95	130	120	800	2.2	4	5	
P1301UCLxx	P1301UC	120	160	120	800	2.2	4	5	
P1701UCLxx	P1701UC	160	200	120	800	2.2	4	5	

Notes:
- Absolute maximum ratings measured at T_A = 25°C (unless otherwise noted).
- Components are not appropriate for positive ringing systems
- All electrical characteristics shown are defined from Tip (pins 1 & 6) to Ground (pins 2 & 5), and Ring (pins 3 & 4) to Ground (pins 2 & 5)
- **XX =** Part Number Suffix: **'TP'** (Tube Pack) or **'RP'** (Reel Pack).

Revised: 02/23/17

SIDACtor® Protection Thyristors
SLIC Protection

Capacitance Values

Part Number	pF Pin 1-2 / 3-2 (4-5/6-5) Tip-Ground, Ring-Ground		pF Pin 1-3 (4-6) Tip-Ring	
	MIN	MAX	MIN	MAX
P0641UALxx	50	205	30	135
P0721UALxx	45	195	20	125
P0901UALxx	40	180	20	115
P1101UALxx	40	160	15	105
P1301UALxx	35	160	15	100
P1701UALxx	30	125	15	80
P0641UCLxx	65	205	40	130
P0721UCLxx	60	195	20	125
P0901UCLxx	60	180	20	115
P1101UCLxx	50	160	15	105
P1301UCLxx	35	160	15	100
P1701UCLxx	40	125	15	80

Note: Off-state capacitance (C_O) is measured at 1 MHz with a -2V bias.

Surge Ratings

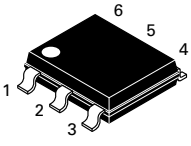
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
A	20	150	150	90	50	75	75	45	75	20	500
C	50	500	400	200	150	200	175	100	200	30	500

Notes:

1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

Thermal Considerations

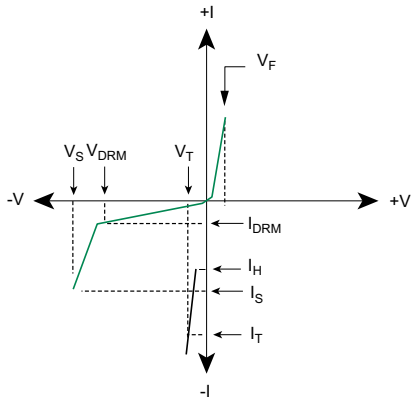
Package	Symbol	Parameter	Value	Unit
Modified MS-013 	T_J	Operating Junction Temperature Range	-40 to +125	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

Additional Information

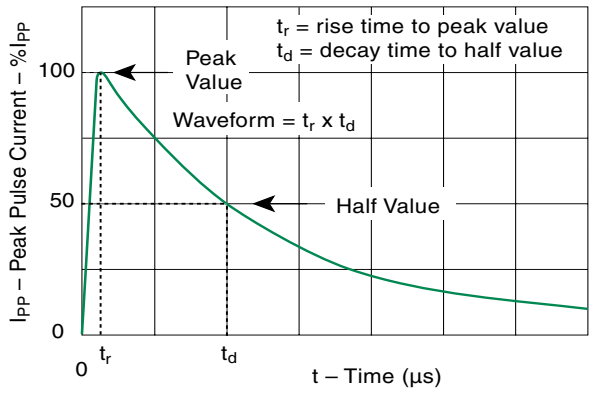
Datasheet | **Resources** | **Samples**

Revised: 02/23/17

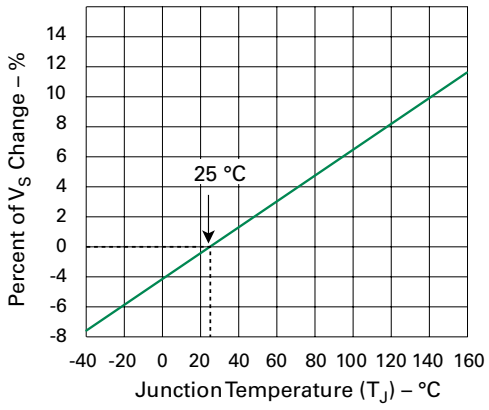
V-I Characteristics



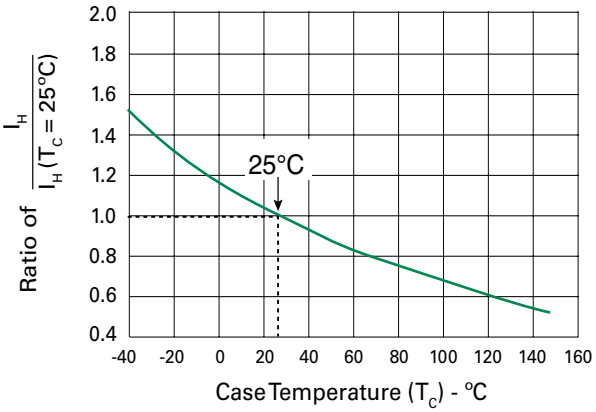
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

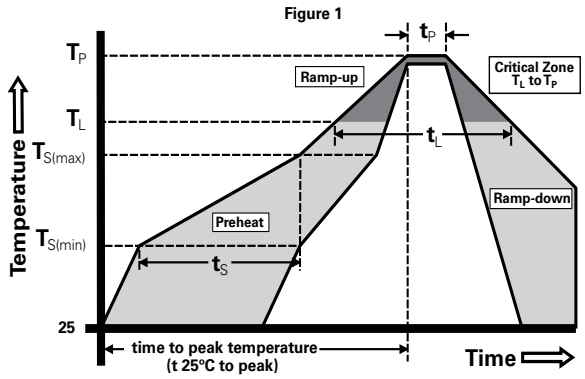


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



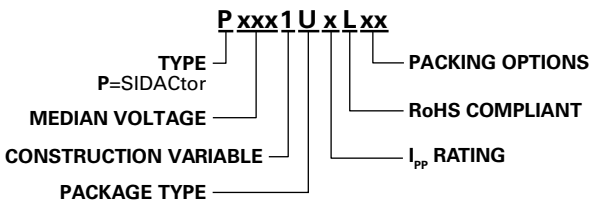
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

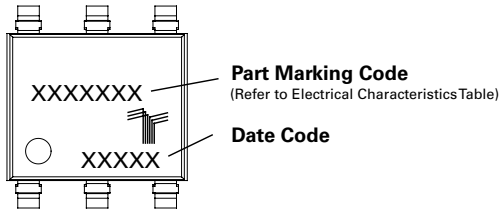
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{DC}) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering

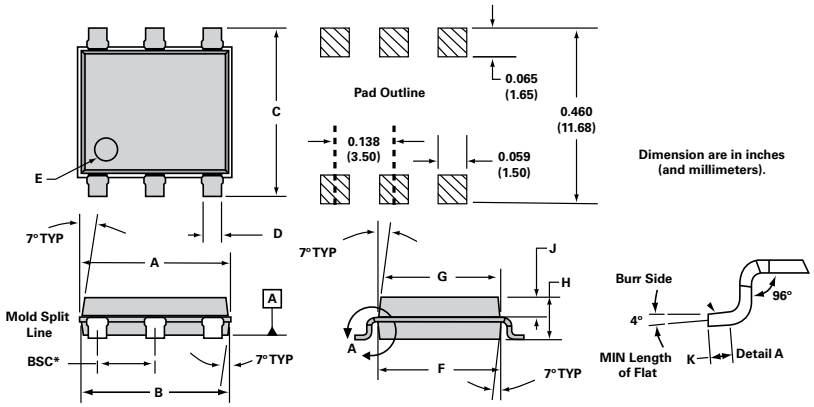


Part Marking



Revised: 02/23/17

Dimensions — MS-013



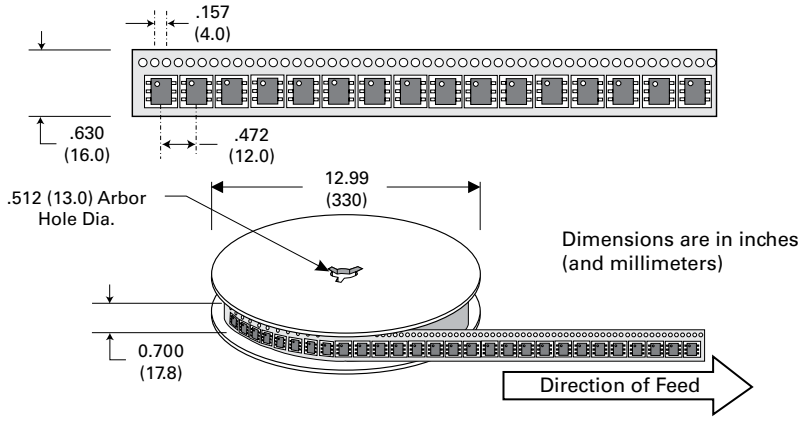
Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.360	0.364	9.14	9.25
B	0.352	0.356	8.94	9.04
C	0.400	0.412	10.16	10.46
D	0.043	0.045	1.09	1.13
E	0.047	0.055	1.19	1.40
F	0.293	0.297	7.44	7.54
G	0.289	0.293	7.34	7.44
H	0.089	0.093	2.26	2.36
J	0.041	0.049	1.04	1.24
K	0.020		0.51	
BSC*	0.133	0.143	3.38	3.63

* BSC = **B**asic **S**pacing between **C**enters

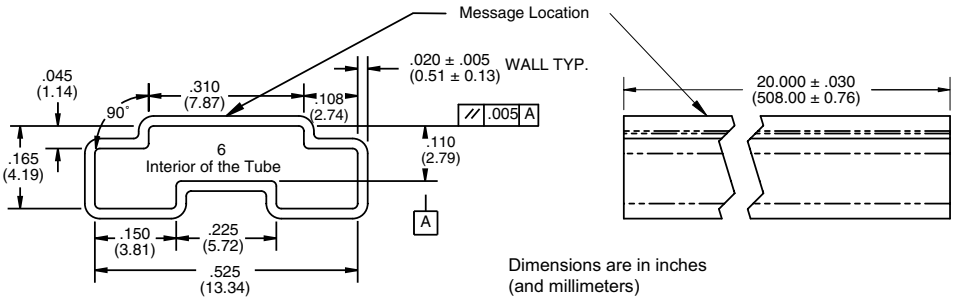
Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
U	Modified MS-013 6-pin Tape and Reel Pack	1500	RP	EIA-481-D
	Modified MS-013 6-pin Tube Pack	500 (50 per tube)	TP	N/A

Tape and Reel Specification — MS-013



Tube Pack Dimensions — MS-013



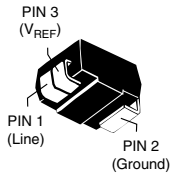
Battrax® Series Positive/Negative - Modified DO-214

HF RoHS

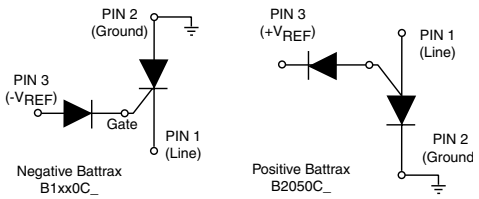
Agency Approvals

Agency	Agency File Number
UL	E133083

Pinout Designation



Schematic Symbol



Description

The Battrax® series offers programmable SIDACtor® overvoltage protection devices for SLIC applications. This series is offered in a negative Battrax version and a positive Battrax version. The B1xx0C_ is for a $-V_{REF}$ supply and the B2050C_ is for a $+V_{REF}$ supply. Designed using an SCR and a gate diode, the B1xx0C_ Battrax begins to conduct at $|-V_{REF}| + |-1.2\ V|$ while the B2050C_ Battrax begins to conduct at $|+V_{REF}| + |1.2\ V|$.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Robust surge current ratings
- Gate triggered tracking devices
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level*
- ITU K.20/21 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5
- YD/T 1082
- YD/T 993
- YD/T 950

*A-rated parts require series resistance

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	Capacitance*	
		V min	V max	mA min	mA max	A max	V max	pF	
								Min	Max
B1100CALRP	B10A	$I-V_{REF}I + I-1.2VI$	$I-V_{REF}I + I-10VI$	100	100	2.2	4	30	200
B1160CALRP	B16A	$I-V_{REF}I + I-1.2VI$	$I-V_{REF}I + I-10VI$	160	100	2.2	4	30	200
B1200CALRP	B12A	$I-V_{REF}I + I-1.2VI$	$I-V_{REF}I + I-10VI$	200	100	2.2	4	30	200
B2050CALRP	B25A	$I+V_{REF}I + I1.2VI$	$I+V_{REF}I + I10VI$	5	50	2.2	4	20	200
B1100CCLRP	B10C	$I-V_{REF}I + I-1.2VI$	$I-V_{REF}I + I-10VI$	100	100	2.2	4	30	200
B1160CCLRP	B16C	$I-V_{REF}I + I-1.2VI$	$I-V_{REF}I + I-10VI$	160	100	2.2	4	30	200
B1200CCLRP	B12C	$I-V_{REF}I + I-1.2VI$	$I-V_{REF}I + I-10VI$	200	100	2.2	4	30	200
B2050CCLRP	B25C	$I+V_{REF}I + I1.2VI$	$I+V_{REF}I + I10VI$	5	50	2.2	4	20	200

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Devices are uni-directional
- All electrical characteristics shown are defined from Tip (pin 1) to Ground (pin 2), and Ring (pin 1) to Ground (pin 2)
- V_{REF} Max Value for the negative Battrax is -200 V.
- V_{REF} Max Value for the positive Battrax is 110 V.
* Off-state capacitance (C_O) is measured across pins 1 & 2 at 1 MHz with a 2V bias.

Revised: 02/23/17

Surge Ratings

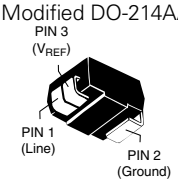
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2x310 [1] 0.5x700 [2]	2x10 [1] 2x10 [2]	8x20 [1] 1.2x50 [2]	10x160 [1] 10x160 [2]	10x560 [1] 10x560 [2]	5x320 [1] 9x720 [2]	10x360 [1] 10x360 [2]	10x1000 [1] 10x1000 [2]	5x310 [1] 10x700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
A	20	150	150	90	50	75	75	45	75	20	500
C	50	500	400	200	150	200	175	100	200	50	500

Notes:

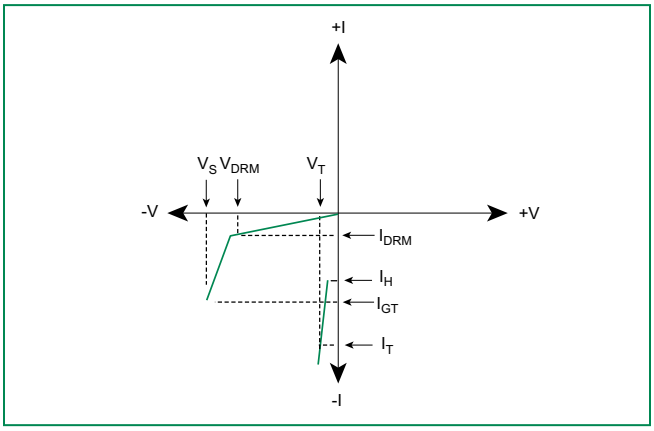
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C (I_{PP} rating assumes V_{REF} equals +/- 48 V)
- The device must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

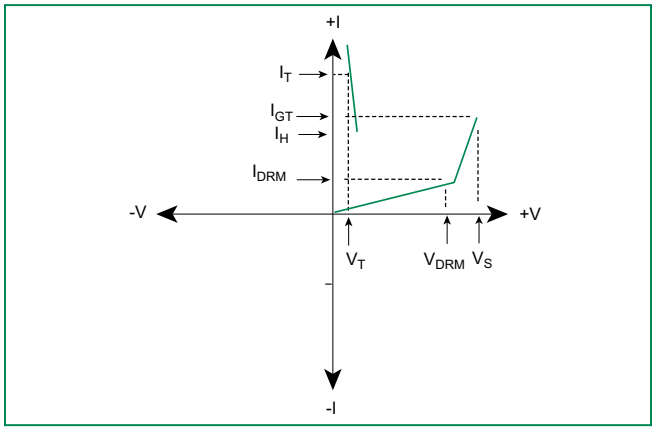
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified DO-214AA 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	85	°C/W

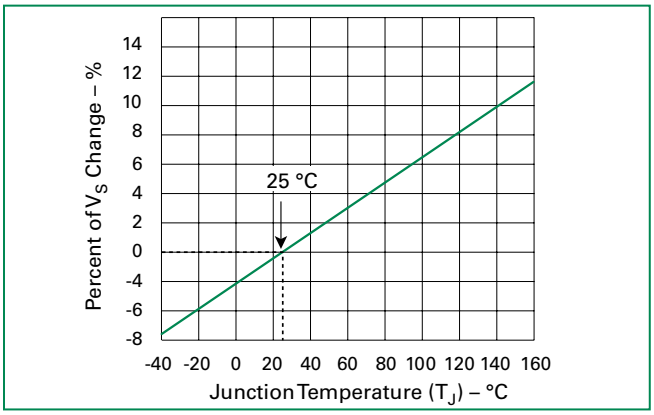
V-I Characteristics - Negative Battrax



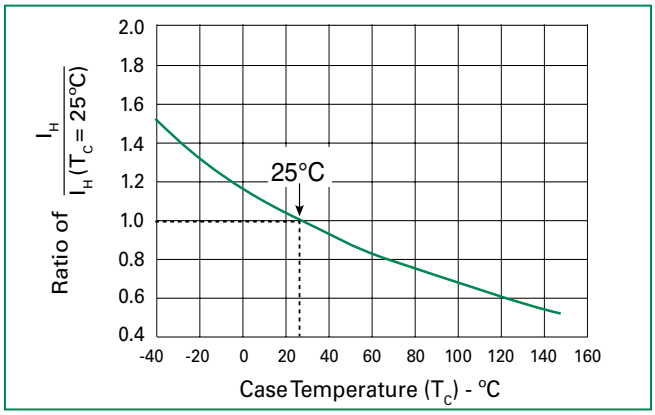
V-I Characteristics - Positive Battrax



Normalized V_S Change vs. Junction Temperature



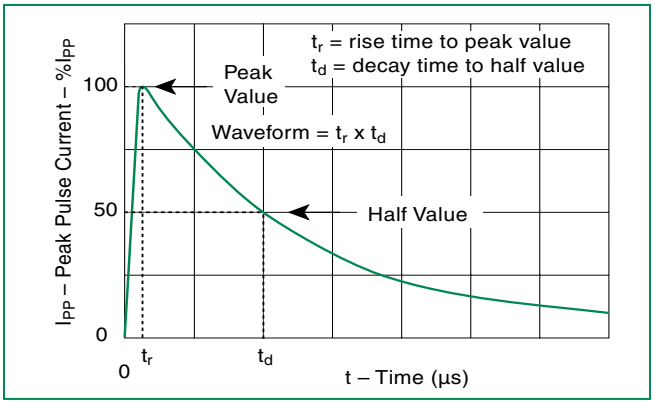
Normalized DC Holding Current vs. Case Temperature



Revised: 02/23/17

SIDACtor® Protection Thyristors
SLIC Protection

t_r x t_d Pulse Waveform



Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{REF} Max. (V_{DC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

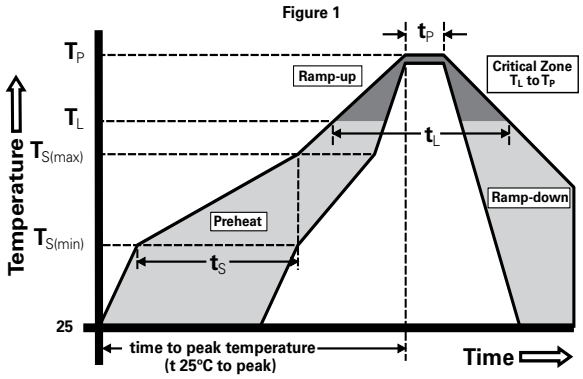
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification 94V-0

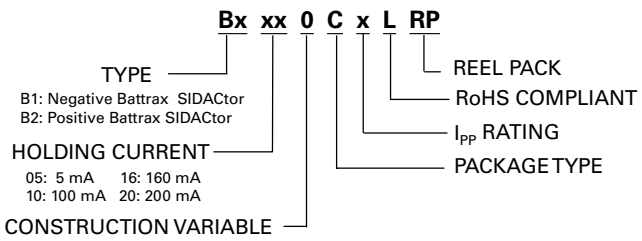
Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

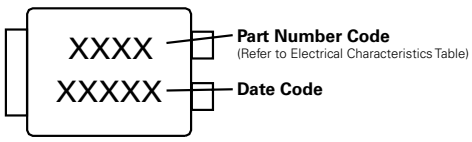
Figure 1



Part Numbering

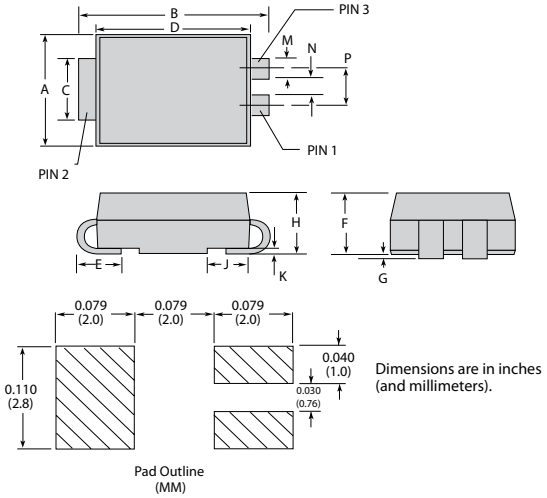


Part Marking



Revised: 02/23/17

Dimensions — Modified DO-214AA

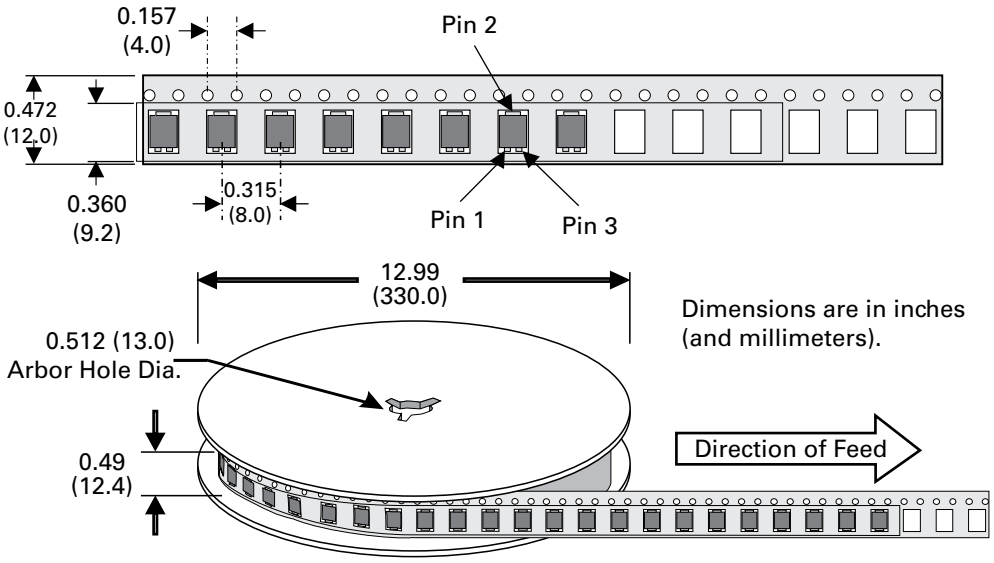


Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.130	0.156	3.30	3.95
B	0.201	0.220	5.10	5.60
C	0.077	0.087	1.95	2.20
D	0.159	0.181	4.05	4.60
E	0.030	0.063	0.75	1.60
F	0.075	0.096	1.90	2.45
G	0.002	0.008	0.05	0.20
H	0.077	0.104	1.95	2.65
K	0.006	0.016	0.15	0.41
M	0.022	0.028	0.56	0.71
N	0.027	0.033	0.69	0.84
P	0.052	0.058	1.32	1.47

Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
C	Modified DO-214AA 3-leaded Tape and Reel Pack	2500	RP	EIA-481-D

Tape and Reel Specification — Modified DO-214AA



Additional Information

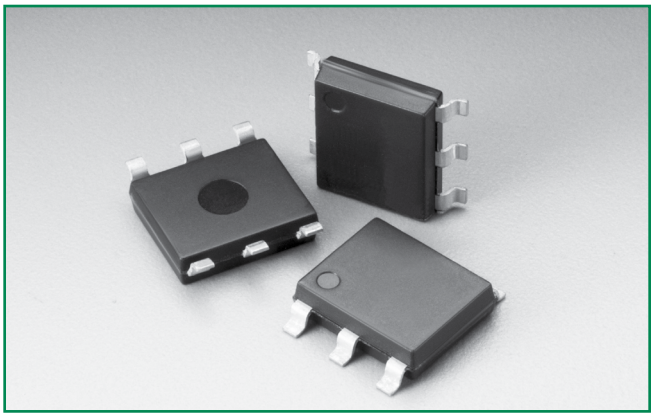
Datasheet | **Resources** | **Samples**

Revised: 02/23/17

Littelfuse
Expertise Applied | Answers Delivered

SIDACtor® Protection Thyristors
SLIC Protection

Battrax® Series - Single Port Negative - MS-013



Description

The Battrax® Protection Thyristor series offers programmable SIDACtor® overvoltage protection components for SLIC applications. The Single Port Negative Battrax® Protection Thyristor series provides a programmable device that is referenced to a negative voltage souce while internal diodes provide protection from positive surge events.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Single-port protection
- Gate triggered tracking device
- Integrated diodes for positive voltage protection
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)
- RoHS compliant and lead-free

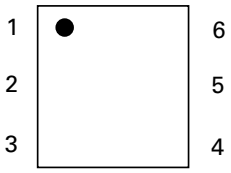
Agency Approvals

Agency	Agency File Number
	E133083

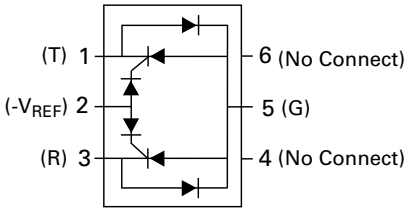
Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

Pinout Designation



Schematic Symbol



Additional Information

Datasheet | Resources | Samples

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	V_F	Capacitance*	
		V min	V max	mA min	mA max	A max	V max	V max	pF min	pF max
B1101UALxx	B1101UA	I-V_{REF}I + I-1.2VI	I-V_{REF}I + I-10VI	100	100	2.2	4	5	30	200
B1161UALxx	B1161UA	I-V_{REF}I + I-1.2VI	I-V_{REF}I + I-10VI	160	100	2.2	4	5	30	200
B1201UALxx	B1201UA	I-V_{REF}I + I-1.2VI	I-V_{REF}I + I-10VI	200	100	2.2	4	5	30	200
B1101UCLxx	B1101UC	I-V_{REF}I + I-1.2VI	I-V_{REF}I + I-10VI	100	100	2.2	4	5	30	200
B1161UCLxx	B1161UC	I-V_{REF}I + I-1.2VI	I-V_{REF}I + I-10VI	160	100	2.2	4	5	30	200
B1201UCLxx	B1201UC	I-V_{REF}I + I-1.2VI	I-V_{REF}I + I-10VI	200	100	2.2	4	5	30	200

Notes:
- Absolute maximum ratings measured at T_A= 25ºC (unless otherwise noted).
- Components are not appropriate for positive ringing systems.
- All electrical characteristics shown are defined from Tip (pin 1) to Ground (pin 5), and Ring (pin 3) to Ground (pin 5)
- V_{REF} Max Value for the negative Battrax is -200 V.
- **XX =** Part Number Suffix: **'TP'** (Tube Pack) or **'RP'** (Reel Pack).

* Off-state capacitance (C_O) is measured across pins 1 & 5 and 3 & 5 at 1 MHz with a 2V bias.

Revised: 02/23/17

Surge Ratings

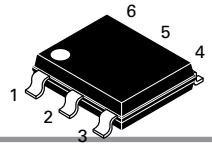
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
A	20	150	150	90	50	75	75	45	75	20	500
C	50	500	400	200	150	200	175	100	200	50	500

Notes:

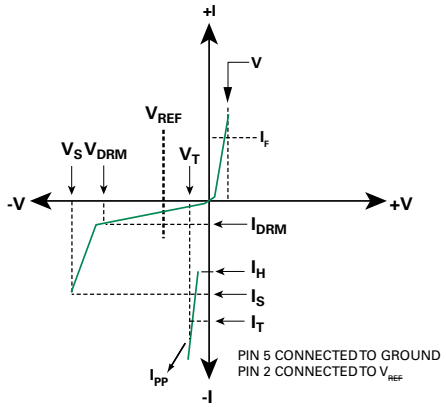
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C (I_{PP} rating assumes V_{REF} equals - 48 V)
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

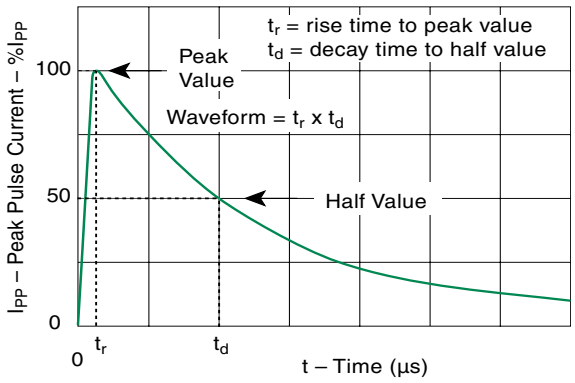
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified MS-013 	T_J	Operating Junction Temperature Range	-40 to +125	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

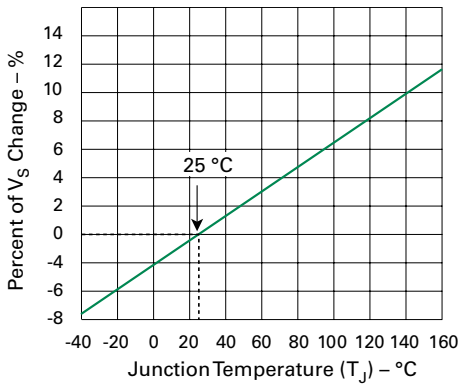
V-I Characteristics



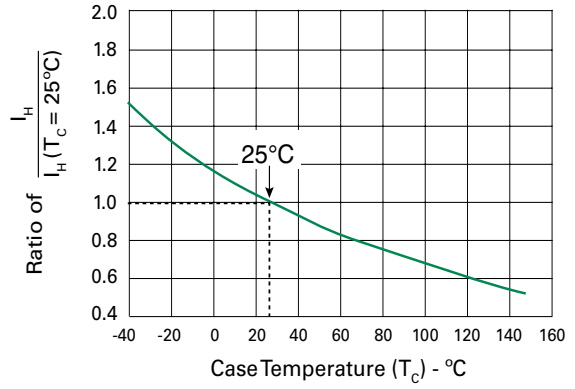
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

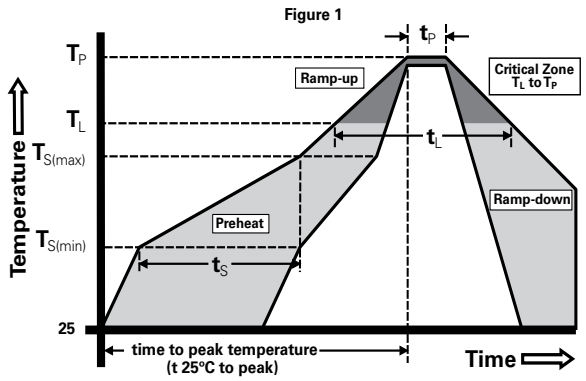


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



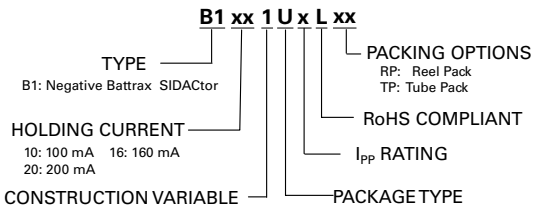
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

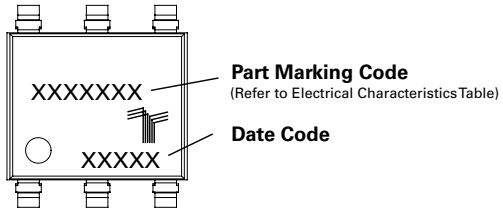
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{REF} Max. (V_{DC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85% RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100% RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85% RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering

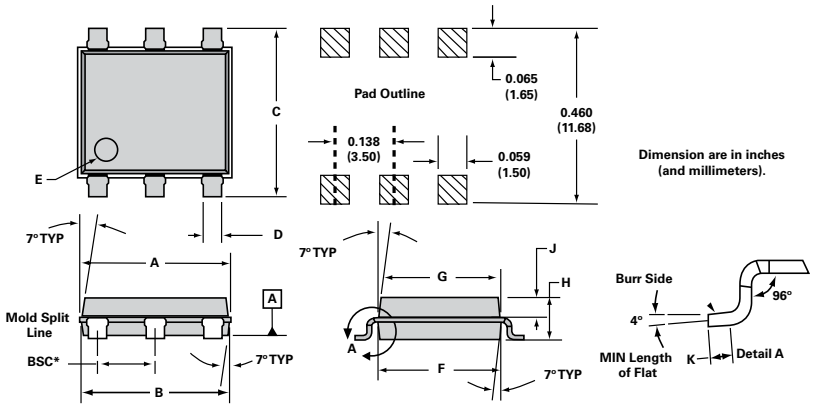


Part Marking



Revised: 02/23/17

Dimensions — MS-013



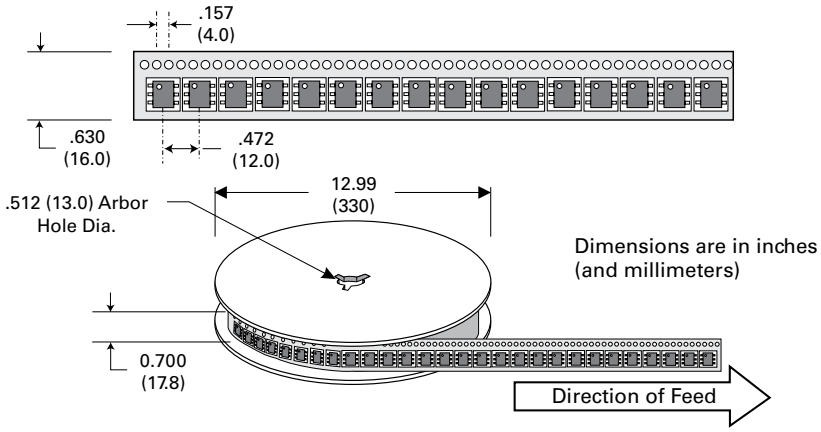
Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.360	0.364	9.14	9.25
B	0.352	0.356	8.94	9.04
C	0.400	0.412	10.16	10.46
D	0.043	0.045	1.09	1.13
E	0.047	0.055	1.19	1.40
F	0.293	0.297	7.44	7.54
G	0.289	0.293	7.34	7.44
H	0.089	0.093	2.26	2.36
J	0.041	0.049	1.04	1.24
K	0.020		0.51	
BSC*	0.133	0.143	3.38	3.63

* BSC = **B**asic **S**pacing between **C**enters

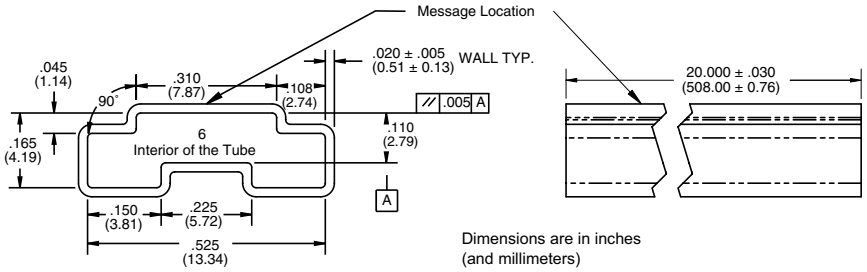
Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
U	Modified MS-013 6-pin Tape and Reel Pack	1500	RP	EIA-481-D
	Modified MS-013 6-pin Tube Pack	500 (50 per tube)	TP	N/A

Tape and Reel Specification — MS-013



Tube Pack Specification — MS-013



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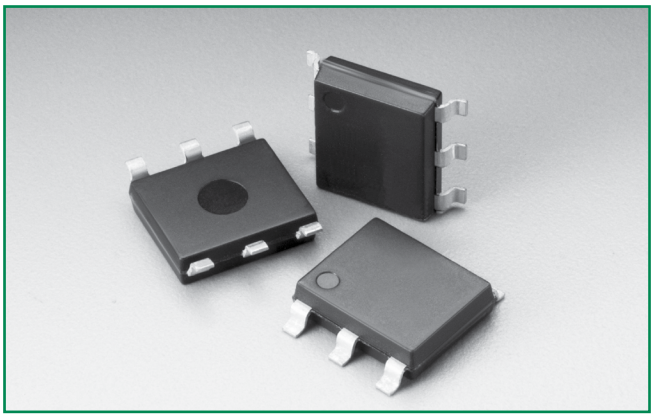
SIDACtor® Protection Thyristors
SLIC Protection

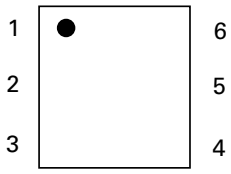
Battrax® Protection Thyristor Series Single Port Positive/Negative - MS-013



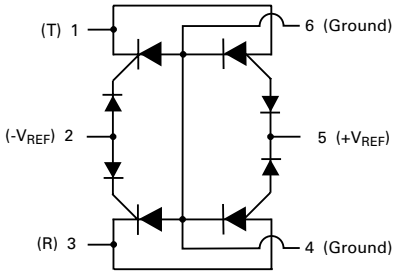
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Description

The Single Port Positive/Negative Battrax® Protection Thyristor Series are programmable SIDACtor® components designed to protect SLICs (Subscriber Line Interface Circuit) from damaging overvoltage transients.

This series is designed specifically to protect SLIC devices utilizing positive and negative ringing signals. This one device will protect a single port.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Low capacitance
- Positive and negative ringing compatible
- Single-port protect
- Gate trigger tracking device
- RoHS Compliant and Lead-Free
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

Additional Information

Datasheet | **Resources** | **Samples**

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	Capacitance*	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
B3104UCLxx	B3104UC	I±V_{REF}I + I±1.2VI	I±V_{REF}I + I±10VI	100	100	2.2	4	30	200
B3164UCLxx	B3164UC	I±V_{REF}I + I±1.2VI	I±V_{REF}I + I±10VI	160	100	2.2	4	30	200
B3204UCLxx	B3204UC	I±V_{REF}I + I±1.2VI	I±V_{REF}I + I±10VI	200	100	2.2	4	30	200

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional
- All electrical characteristics shown are defined from Tip (pin 1) to Ground (pin 4 & 6) and Ring (pin 3) to Ground (pin 4 & 6)
- V_{REF} Max Value for the negative Battrax is -200 V.
- V_{REF} Max Value for the positive Battrax is +110 V.
- **XX =** Part Number Suffix: **'TP'** (Tube Pack) or **'RP'** (Reel Pack).

* Off-state capacitance (C_O) is measured across pins 1 & 4,6 and 3 & 4,6 at 1 MHz with a 2V bias.

Revised: 02/23/17

Surge Ratings

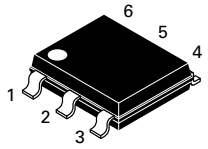
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
C	50	500	400	200	150	200	175	100	200	50	500

Notes:

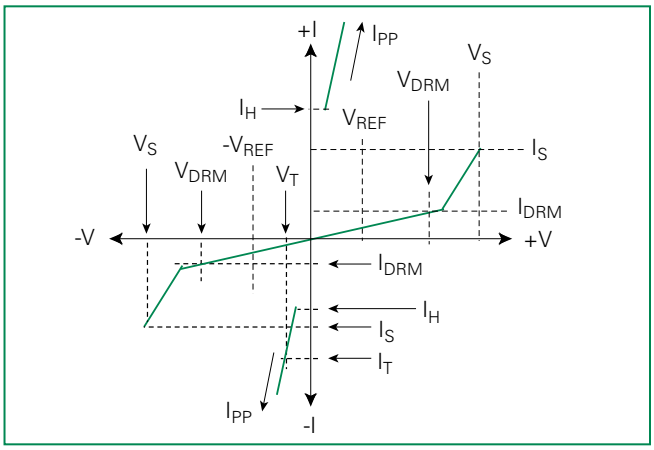
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C (I_{PP} rating assumes V_{REF} equals +/- 48 V)
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

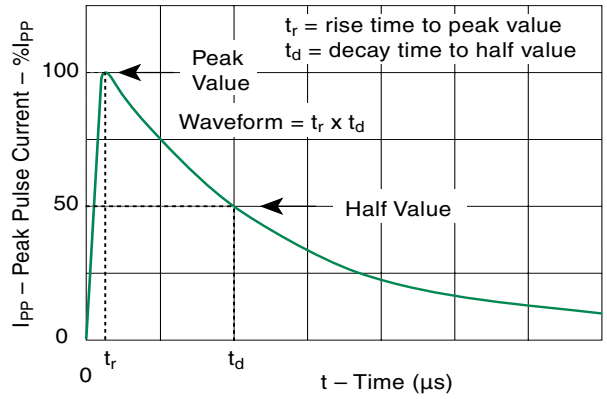
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified MS-013 	T_J	Operating Junction Temperature Range	-40 to +125	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

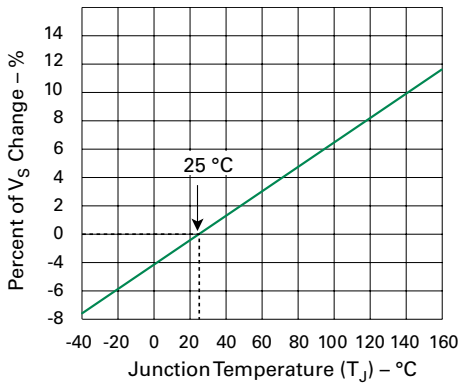
V-I Characteristics



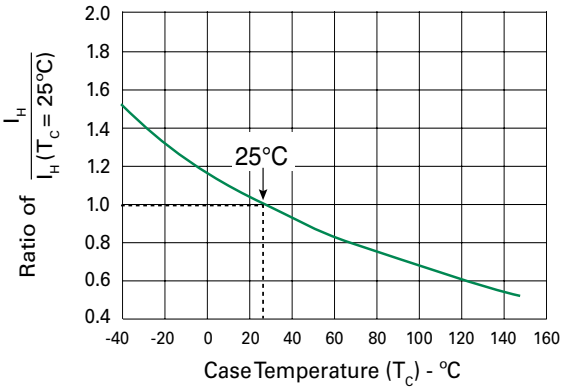
t_r x t_d Pulse Waveform



Normalized V_s Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

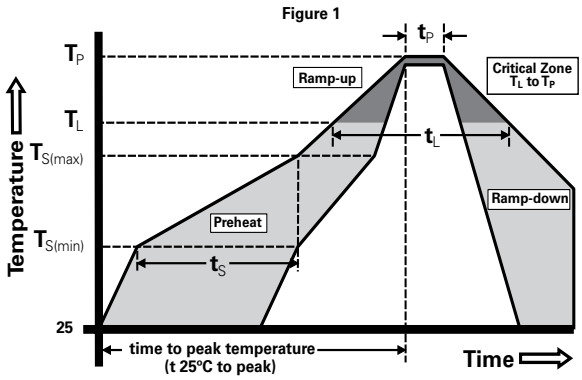


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



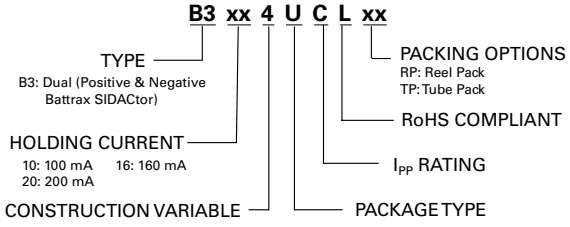
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

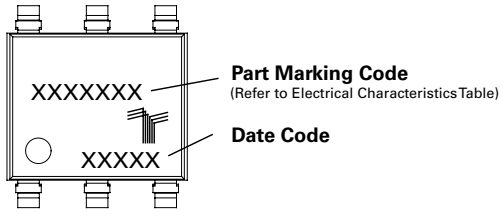
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{DC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85% RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100% RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85% RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering

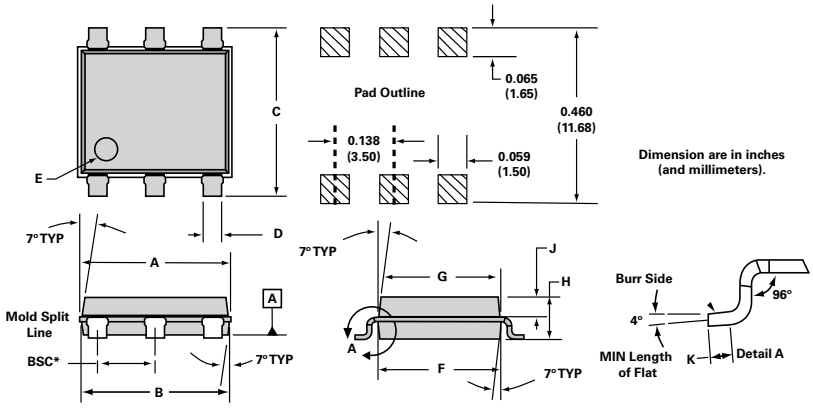


Part Marking



Revised: 02/23/17

Dimensions — MS-013



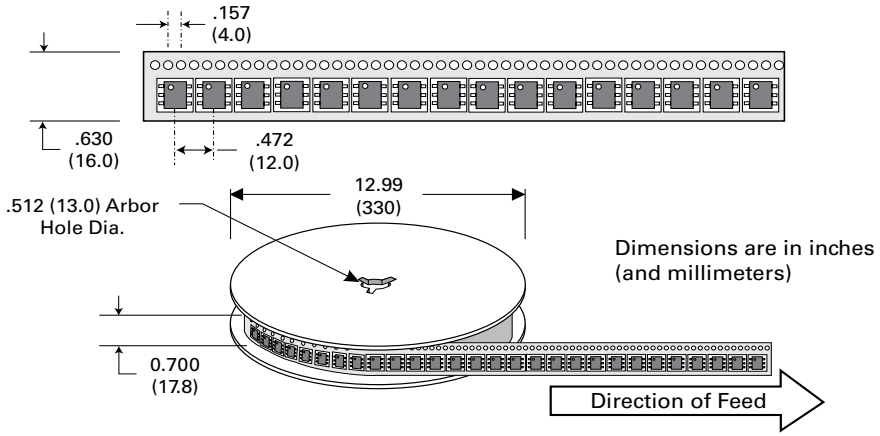
Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.360	0.364	9.14	9.25
B	0.352	0.356	8.94	9.04
C	0.400	0.412	10.16	10.46
D	0.043	0.045	1.09	1.13
E	0.047	0.055	1.19	1.40
F	0.293	0.297	7.44	7.54
G	0.289	0.293	7.34	7.44
H	0.089	0.093	2.26	2.36
J	0.041	0.049	1.04	1.24
K	0.020		0.51	
BSC*	0.133	0.143	3.38	3.63

* BSC = **B**asic **S**pacing between **C**enters

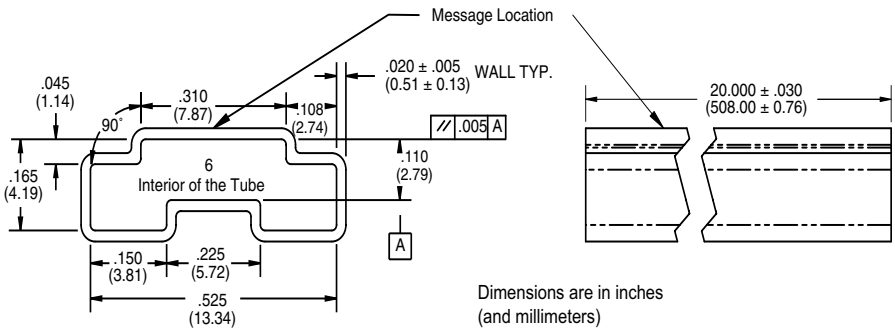
Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
U	Modified MS-013 6-pin Tape and Reel Pack	1500	RP	EIA-481-D
	Modified MS-013 6-pin Tube Pack	500 (50 per tube)	TP	N/A

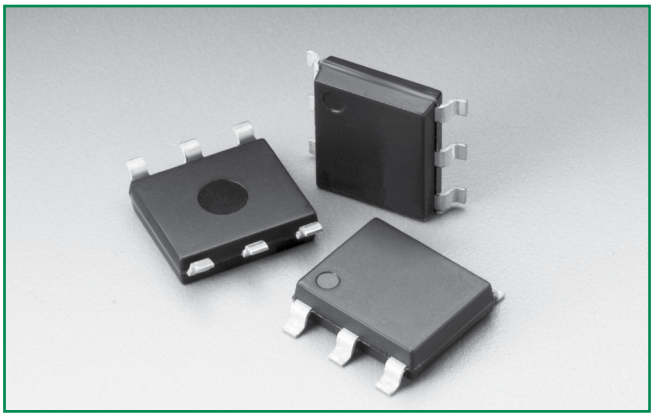
Tape and Reel Specification — MS-013



Tube Pack Specification — MS-013



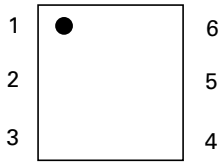
Battrax® Series - Dual Port Negative - MS-013



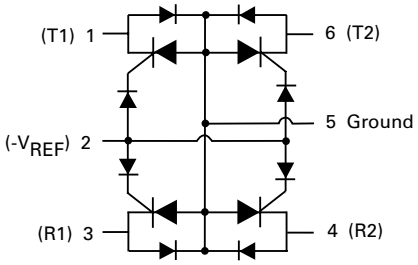
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Description

The Dual Port Negative Battrax® Protection Thyristor Series are programmable SIDACtor® components designed to protect SLICs (Subscriber Line Interface Circuit) from damaging overvoltage transients.

Dual port protection is provided by a programmable device that is referenced to a negative voltage souce while internal diodes provide protection from positive surge events.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- RoHS Compliant and Lead-Free
- Dual-port protection
- Gate trigger tracking device
- Fails short circuit when surged in excess of ratings
- Integrated diode for positive voltage surges
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

Additional Information

Datasheet | **Resources** | **Samples**

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	V_F	Capacitance*	
		V min	V max	mA min	mA max	A max	V max	V max	pF min	pF max
B1101UC4Lxx	B1101UC4	I-V_{REF}I + I-1.2VI	I-V_{REF}I + I-10VI	100	100	2.2	4	5	30	200
B1161UC4Lxx	B1161UC4	I-V_{REF}I + I-1.2VI	I-V_{REF}I + I-10VI	160	100	2.2	4	5	30	200
B1201UC4Lxx	B1201UC4	I-V_{REF}I + I-1.2VI	I-V_{REF}I + I-10VI	200	100	2.2	4	5	30	200

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are uni-directional
- All electrical characteristics shown are defined from Tip (pin 1 & 6) to Ground (pin 5) and Ring (pin 3 & 4) to Ground (pin 5)
- Components are polarity sensitive and are not appropriate for positive ringing systems.
- V_{REF} Max Value for the negative Battrax is -200 V.
- XX = Part Number Suffix: 'TP' (Tube Pack) or 'RP' (Reel Pack).

* Off-state capacitance (C_O) is measured across pins 1 & 5, 3 & 5, 4 & 5, and 6 & 5 at 1 MHz with a 2V bias.

Revised: 02/23/17

Surge Ratings

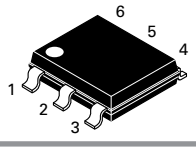
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
C	50	500	400	200	150	200	175	100	200	50	500

Notes:

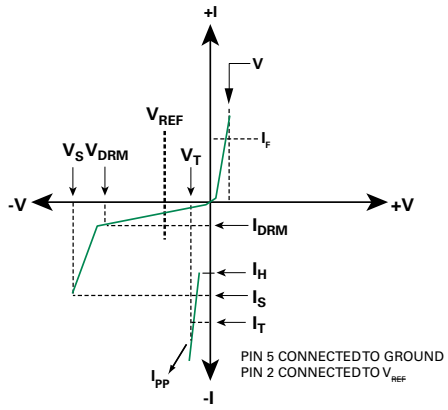
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C (I_{PP} rating assumes V_{REF} equals - 48 V)
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

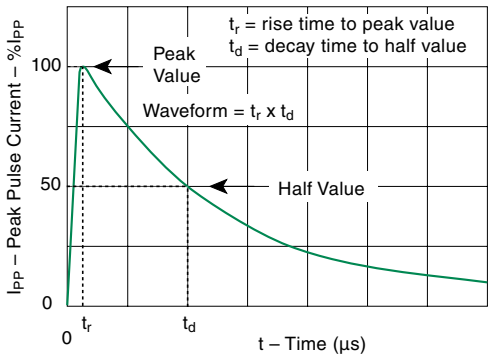
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified MS-013 	T_J	Operating Junction Temperature Range	-40 to +125	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

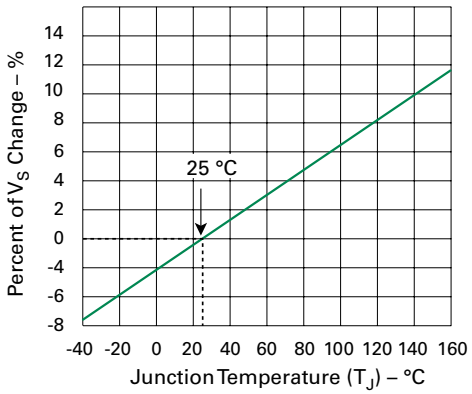
V-I Characteristics



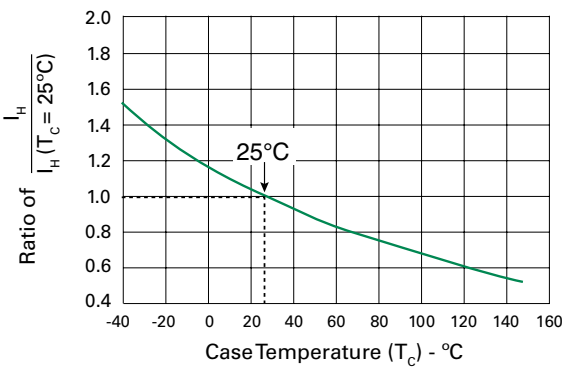
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

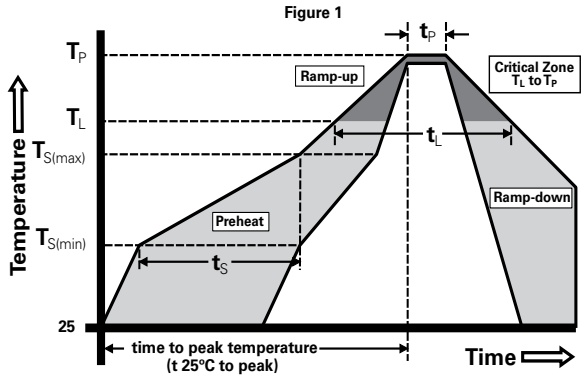


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



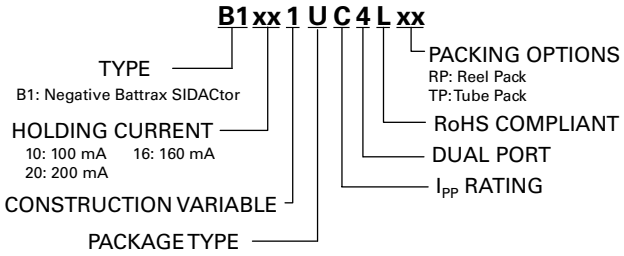
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

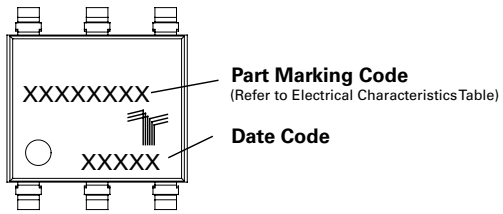
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{DC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering

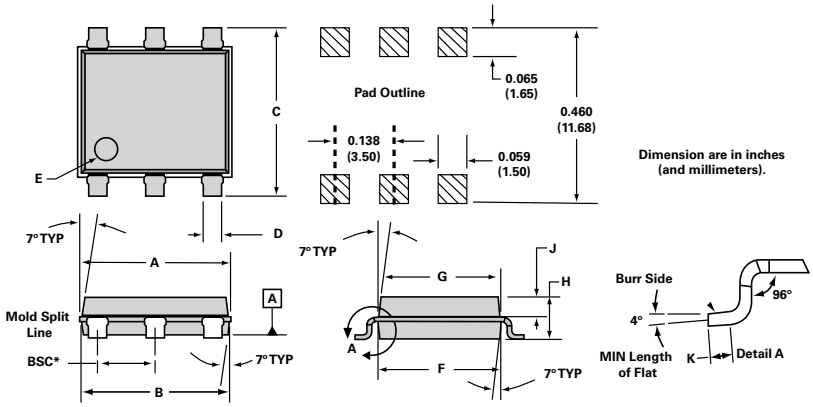


Part Marking



Revised: 02/23/17

Dimensions — MS-013



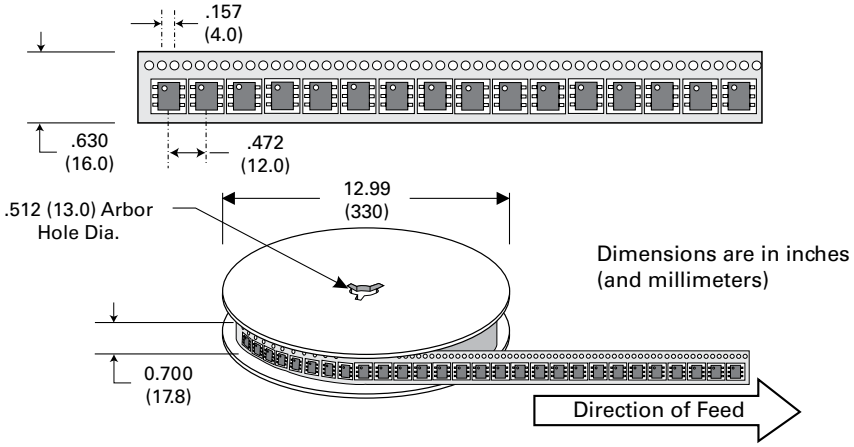
Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.360	0.364	9.14	9.25
B	0.352	0.356	8.94	9.04
C	0.400	0.412	10.16	10.46
D	0.043	0.045	1.09	1.13
E	0.047	0.055	1.19	1.40
F	0.293	0.297	7.44	7.54
G	0.289	0.293	7.34	7.44
H	0.089	0.093	2.26	2.36
J	0.041	0.049	1.04	1.24
K	0.020	---	0.51	---
BSC*	0.133	0.143	3.38	3.63

* BSC = **B**asic **S**pacing between **C**enters

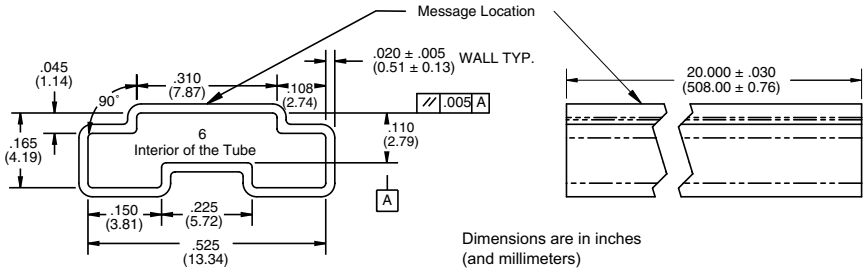
Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
U	Modified MS-013 6-pin Tape and Reel Pack	1500	RP	EIA-481-D
	Modified MS-013 6-pin Tube Pack	500 (50 per tube)	TP	N/A

Tape and Reel Specification — MS-013



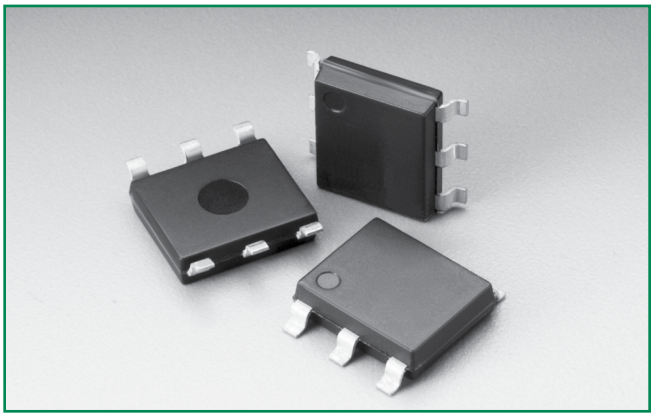
Tube Pack Specification — MS-013



Littelfuse
Expertise Applied | Answers Delivered

SIDACtor® Protection Thyristors
LCAS Protection

Asymmetrical Multiport Series - MS-013



Description

Asymmetrical Multiport Series are SIDACtor® components designed to protect LCAS (Line Circuit Access Switch) devices from damaging overvoltage transients.
The series provides a specialized asymmetrical dual port overvoltage protection solution that enables equipment to comply with various global requlatory standards.

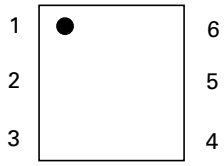
Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Replaces four discrete components
- Two-port protection
- RoHS Compliant, Lead-Free and Halogen Free
- LCAS specific tip and ring thresholds
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin (Sn) (IPC/JEDEC J-STD-609A.01)

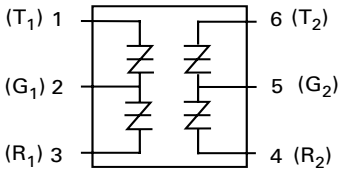
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level*
- ITU K.20/21 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

*A-rated parts require series resistance

Additional Information

Datasheet | **Resources** | **Samples**

Electrical Characteristics

Part Number	Part Marking	V_{DRM} @I_{DRM} = 5µA	V_S @100V/µs	V_{DRM} @I_{DRM} = 5µA	V_S @100V/µs	V_T@I_T = 2.2 Amps	I_S mA	I_T A	I_H mA
		V	V	V	V	V			
		Pins 2-3, 5-6		Pins 1-2, 4-5		Pins 1-2, 2-3, 4-5, 5-6			
A1220UA4Lxx	A1220UA4	100	130	180	220	4	800	2.2	120
A1225UA4Lxx	A1250UA4	100	130	230	290	4	800	2.2	120
A1220UC4Lxx	A1220UC4	100	130	180	220	4	800	2.2	120
A1225UC4Lxx	A1250UC4	100	130	230	290	4	800	2.2	120

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional.
- All electrical characteristics shown are defined from Tip to Ground (pin 1 to pin 2 and pin 6 to pin 5) and Ring to Ground (pin 3 to pin 2 and pin 4 to pin 5).
- XX = Part Number Suffix: 'TP' (Tube Pack) or 'RP' (Reel Pack).

Revised: 02/23/17

Capacitance Values

Part Number	pF Pin 1-2 / 4-5 Ring-Ground		pF Pin 3-2 / 6-5 Tip-Ground		pF Pin 1-3 (4-6) Tip-Ring	
	MIN	MAX	MIN	MAX	MIN	MAX
A1220UA4Lxx	15	25	30	50	5	20
A1225UA4Lxx	15	25	30	50	5	20
A1220UC4Lxx	35	50	60	90	20	35
A1225UC4Lxx	35	50	60	90	20	35

Note: Off-state capacitance (C_O) is measured at 1 MHz with a 2 V bias.

Surge Ratings

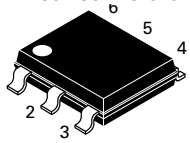
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
A	20	150	150	90	50	75	75	45	75	20	500
C	50	500	400	200	150	200	175	100	200	30	500

Notes:

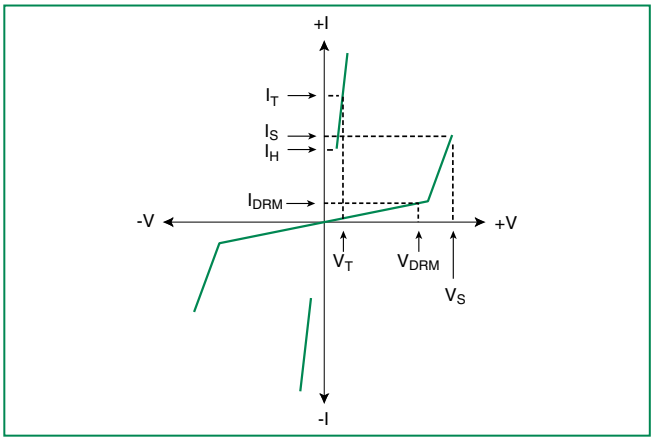
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

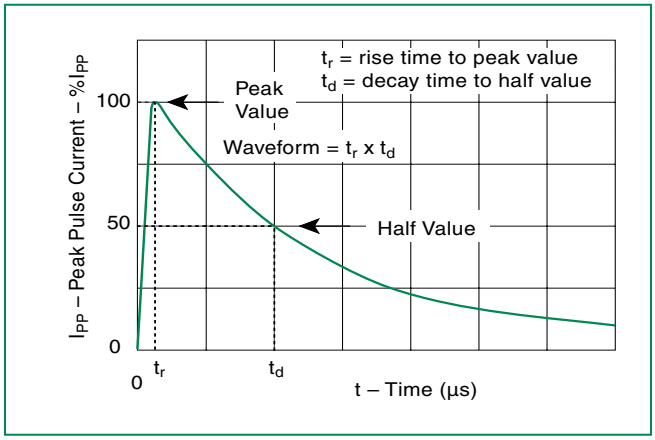
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified MS-013 	T_J	Operating Junction Temperature Range	-40 to +125	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

V-I Characteristics



t_r x t_d Pulse Waveform



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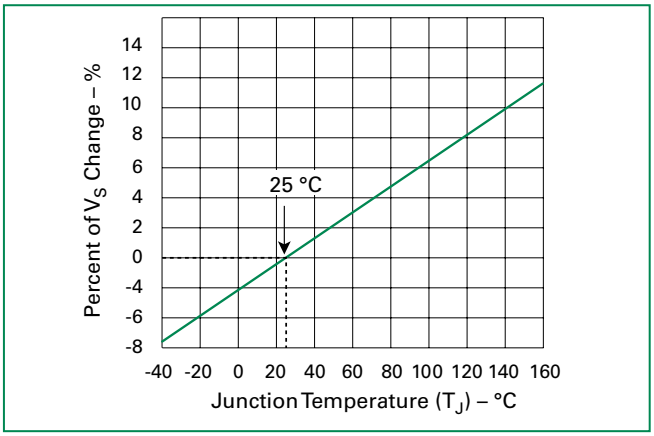
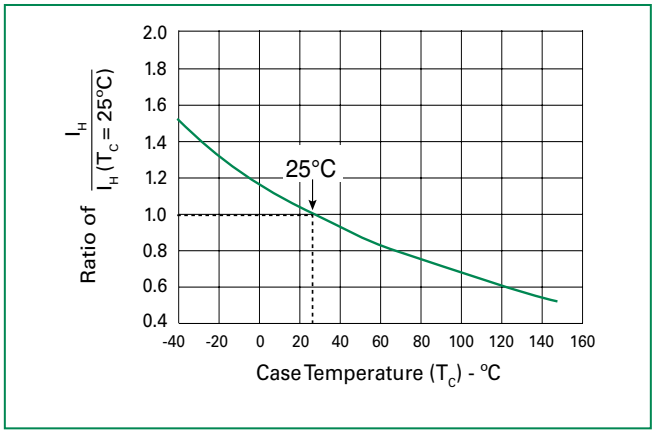
SIDACtor® Protection Thyristors
LCAS Protection

Normalized V_S Change vs. Junction Temperature



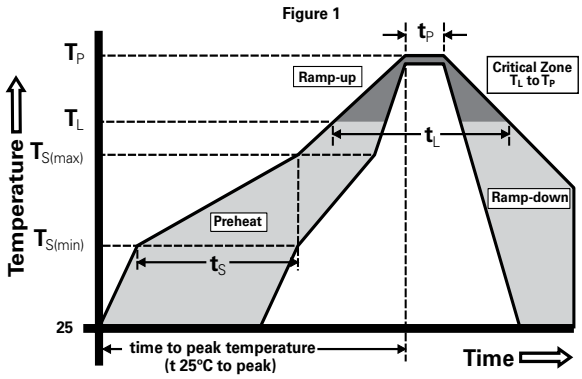
Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

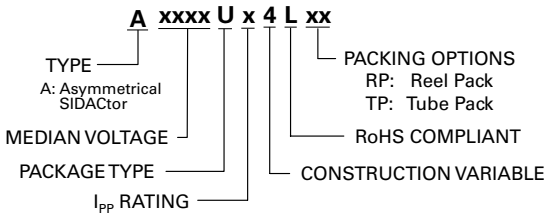
Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification V-0

Part Numbering

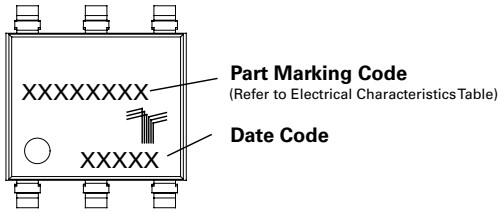


Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Revised: 02/23/17

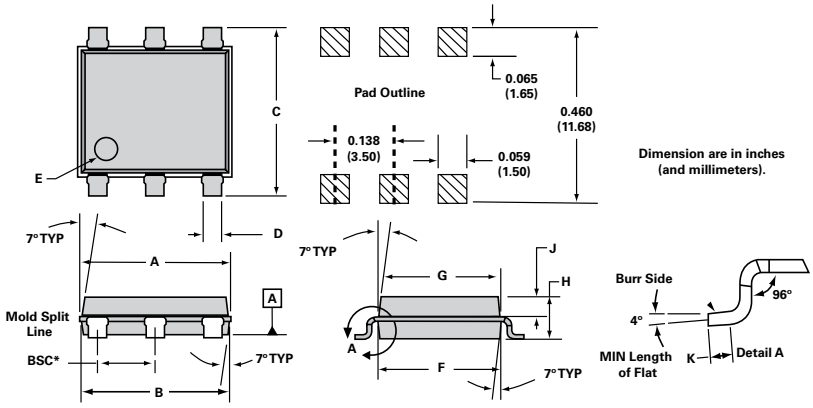
Part Marking



Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
U	Modified MS-013 6-pin Tape and Reel Pack	1500	RP	EIA-481-D
	Modified MS-013 6-pin Tube Pack	500 (50 per tube)	TP	N/A

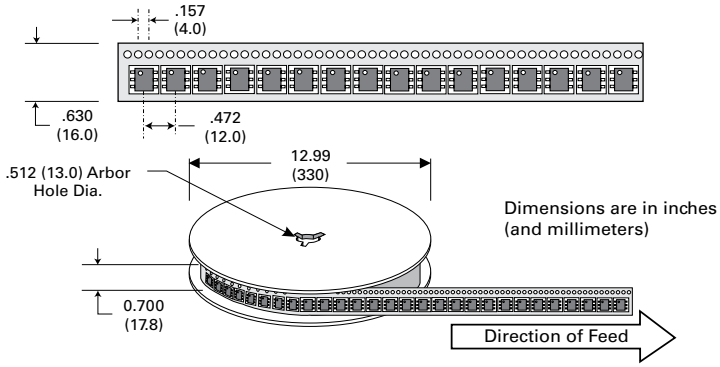
Dimensions — MS-013



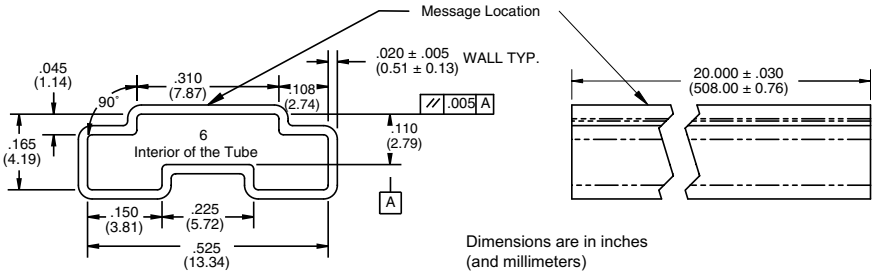
Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.360	0.364	9.14	9.25
B	0.352	0.356	8.94	9.04
C	0.400	0.412	10.16	10.46
D	0.043	0.045	1.09	1.13
E	0.047	0.055	1.19	1.40
F	0.293	0.297	7.44	7.54
G	0.289	0.293	7.34	7.44
H	0.089	0.093	2.26	2.36
J	0.041	0.049	1.04	1.24
K	0.020		0.51	
BSC*	0.133	0.143	3.38	3.63

* BSC = **B**asic **S**pacing between **C**enters

Tape and Reel Specification — MS-013



Tube Pack Specification — MS-013



SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

SIDACtor® Protection Thyristor Series - DO-214

Agency Approvals

AGENCY	AGENCY FILE NUMBER
UL	E133083

Pinout Designation

Not Applicable

Schematic Symbol

Description

Series DO-214AA are designed to protect baseband equipment such as modems, line cards, CPE and DSL from damaging overvoltage transients.

The series provides a surface mount solution that enables equipment to comply with global regulatory standards.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Low capacitance
- Fails short circuit when surged in excess of ratings
- 2nd level interconnect is Pb-free per IPC/JEDEC J-STD-609A.01
- RoHS compliant, lead-free and halogen-free.

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Enhanced Level*
- ITU K.20/21/45 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

*A/B-rated parts require series resistance

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	Capacitance @1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P0080SALRP	P-8A	6	25	50	800	2.2	4	20	35
P0220SALRP	P22A	15	32	50	800	2.2	4	20	40
P0300SALRP	P03A	25	40	50	800	2.2	4	15	40
P0640SALRP	P06A	58	77	150	800	2.2	4	15	40
P0720SALRP	P07A	65	88	150	800	2.2	4	15	40
P0900SALRP	P09A	75	98	150	800	2.2	4	15	40
P1100SALRP	P11A	90	130	150	800	2.2	4	15	40
P1300SALRP	P13A	120	160	150	800	2.2	4	15	40
P1500SALRP	P15A	140	180	150	800	2.2	4	15	40
P1800SALRP	P18A	170	220	150	800	2.2	4	15	35
P2100SALRP	P21A	180	240	150	800	2.2	4	15	35
P2300SALRP	P23A	190	260	150	800	2.2	4	15	35
P2600SALRP	P26A	220	300	150	800	2.2	4	15	35
P3100SALRP	P31A	275	350	150	800	2.2	4	15	35
P3500SALRP	P35A	320	400	150	800	2.2	4	15	35
P0080SBLRP	P-8B	6	25	50	800	2.2	4	20	50
P0220SBLRP	P22B	15	32	50	800	2.2	4	20	50
P0300SBLRP	P03B	25	40	50	800	2.2	4	15	50
P0640SBLRP	P06B	58	77	150	800	2.2	4	20	50
P0720SBLRP	P07B	65	88	150	800	2.2	4	20	50

Table continues on next page.

Revised: 02/23/17

Electrical Parameters (continued)

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	Capacitance @1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P0900SBLRP	P09B	75	98	150	800	2.2	4	20	50
P1100SBLRP	P11B	90	130	150	800	2.2	4	20	50
P1300SBLRP	P13B	120	160	150	800	2.2	4	20	50
P1500SBLRP	P15B	140	180	150	800	2.2	4	20	50
P1800SBLRP	P18B	170	220	150	800	2.2	4	20	50
P2100SBLRP	P21B	180	240	150	800	2.2	4	20	35
P2300SBLRP	P23B	190	260	150	800	2.2	4	20	50
P2600SBLRP	P26B	220	300	150	800	2.2	4	20	35
P3100SBLRP	P31B	275	350	150	800	2.2	4	20	35
P3500SBLRP	P35B	320	400	150	800	2.2	4	20	35
P4500SBLRP	P45B	400	530	150	800	2.2	4	20	50
P0080SCLRP	P-8C	6	25	50	800	2.2	4	25	70
P0220SCLRP	P22C	15	32	50	800	2.2	4	25	70
P0300SCLRP	P03C	25	40	50	800	2.2	4	20	50
P0640SCLRP	P06C	58	77	150	800	2.2	4	45	100
P0720SCLRP	P07C	65	88	150	800	2.2	4	45	100
P0900SCLRP	P09C	75	98	150	800	2.2	4	45	100
P1100SCLRP	P11C	90	130	150	800	2.2	4	45	90
P1300SCLRP	P13C	120	160	150	800	2.2	4	40	85
P1500SCLRP	P15C	140	180	150	800	2.2	4	25	70
P1800SCLRP	P18C	170	220	150	800	2.2	4	25	70
P2100SCLRP	P21C	180	240	150	800	2.2	4	25	70
P2300SCLRP	P23C	190	260	150	800	2.2	4	25	70
P2600SCLRP	P26C	220	300	150	800	2.2	4	30	70
P3100SCLRP	P31C	275	350	150	800	2.2	4	30	70
P3500SCLRP	P35C	320	400	150	800	2.2	4	25	65
P4500SCLRP	P45C	400	530	150	800	2.2	4	25	65
P4500SCLHLRP*	P45L	400	530	50	800	2.2	4	20	50

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional.
- * P4500SCLHLRP is low I_H product

Surge Ratings

Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	Amps/µs max
A	20	150	150	90	50	75	75	45	75	25	500
B	25	250	250	150	100	100	125	80	100	30	500
C	50	500	400	200	150	200	175	100	200 [3]	35	500

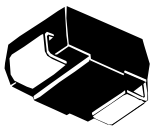
Notes:
1 Current waveform in µs
2 Voltage waveform in µs
3 For surge rating of P4500SCLRP 10/700µs min=150A & typical=180A
For surge rating of P4500SCLHLRP 10/700µs min=150A

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

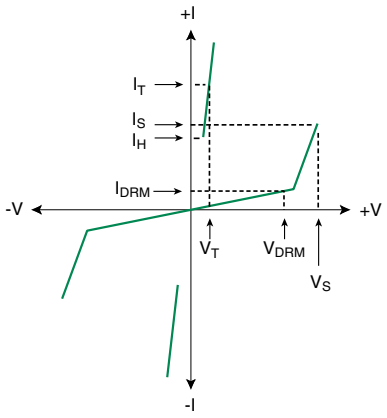
Revised: 02/23/17

SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

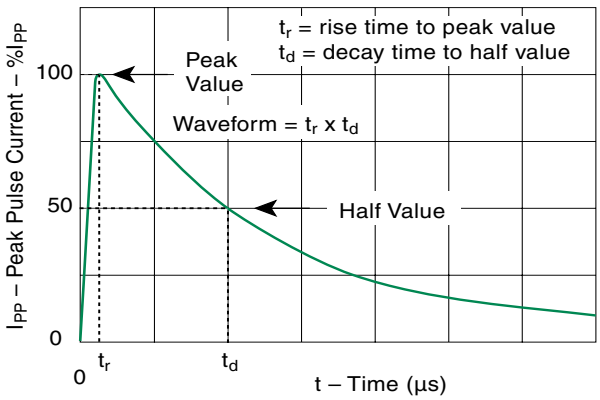
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
DO-214AA 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	90	°C/W

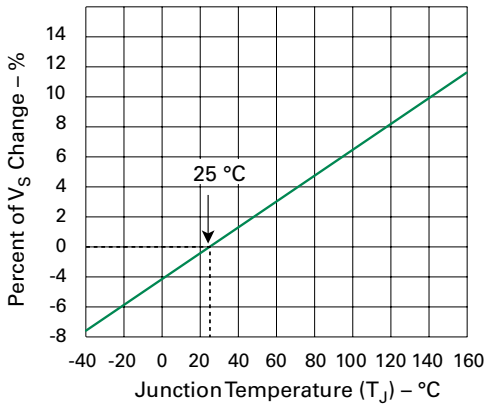
V-I Characteristics



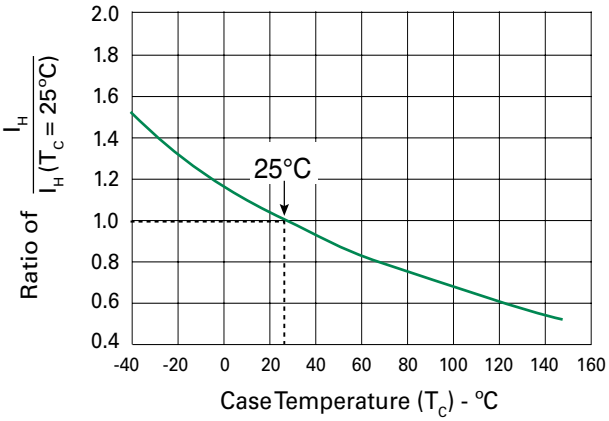
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature



Additional Information

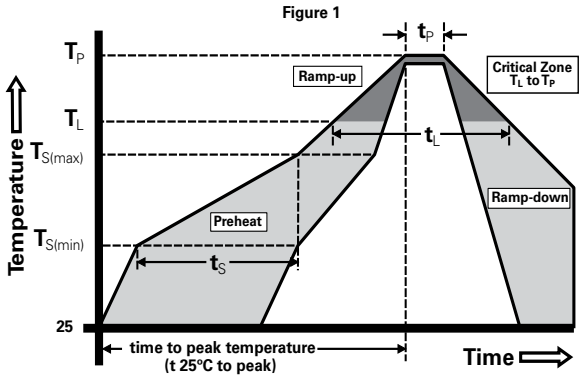
Datasheet | **Resources** | **Samples**

Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



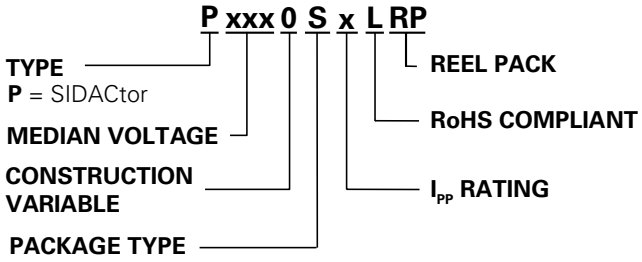
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification V-0

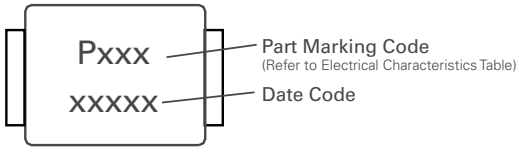
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering



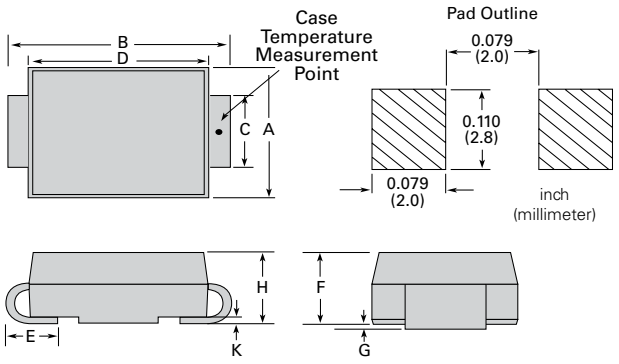
Part Marking



Revised: 02/23/17

SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

Dimensions — DO-214AA

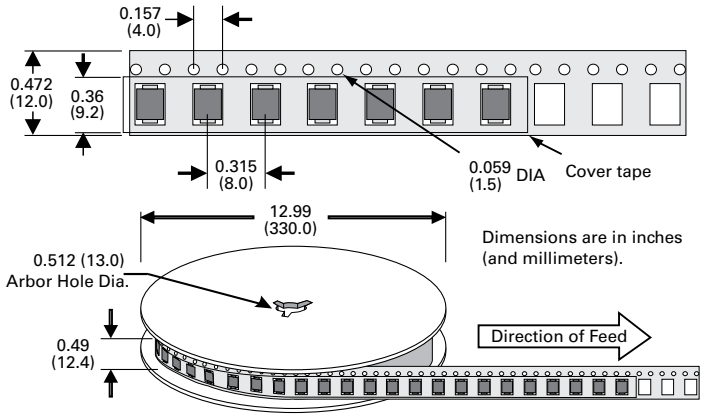


Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.130	0.156	3.30	3.95
B	0.201	0.220	5.10	5.60
C	0.077	0.087	1.95	2.20
D	0.159	0.181	4.05	4.60
E	0.030	0.063	0.75	1.60
F	0.075	0.096	1.90	2.45
G	0.002	0.008	0.05	0.20
H	0.077	0.104	1.95	2.65
H- P4500SCLHLRP	0.077	0.096	1.95	2.43
K	0.006	0.016	0.15	0.41

Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
S	DO-214AA Tape & Reel Pack	2500	RP	EIA-481-D

Tape and Reel Specification — DO-214AA

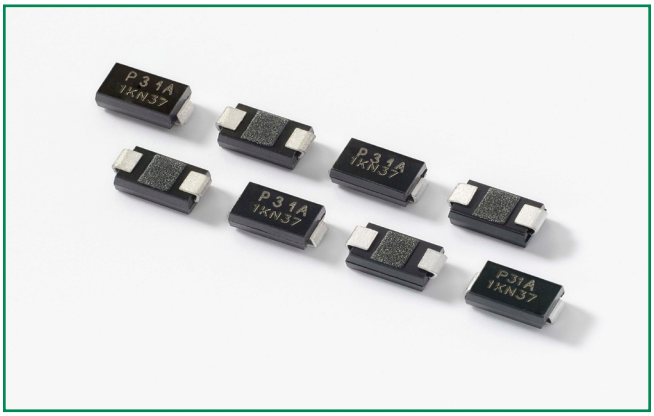


SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

Littelfuse
Expertise Applied | Answers Delivered

SIDACtor® Series - SMA

HF RoHS



Description

SIDACtor® SMA Thyristors Series are designed to protect baseband equipment such as phones, faxes, modems, line cards, CPE and DSL from damaging overvoltage transients.

The series provides a surface mount solution that enables equipment to comply with global regulatory standards.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- RoHS Compliant and Halogen-Free
- Fails short circuit when surged in excess of ratings
- Low capacitance
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Agency Approvals

Agency	Agency File Number
	E133083

Applicable Global Standards

- TIA-968-A*
- TIA-968-B*
- ITU K.20/21/45 Enhanced Level*
- ITU K.20/21/45 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

* Line impedance required to pass operationally

Schematic Symbol

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	Capacitance @1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P0080S1ALRP	P-8A	6	25	50	800	2.2	4	25	35
P0220S1ALRP	P22A	15	32	50	800	2.2	4	10	30
P0300S1ALRP	P03A	25	40	50	800	2.2	4	10	30
P0640S1ALRP	P06A	58	77	150	800	2.2	4	10	30
P1800S1ALRP	P18A	170	220	150	800	2.2	4	10	30
P2300S1ALRP	P23A	190	260	150	800	2.2	4	10	30
P2600S1ALRP	P26A	220	300	150	800	2.2	4	10	30
P3100S1ALRP	P31A	275	350	150	800	2.2	4	10	30
P3500S1ALRP	P35A	320	400	150	800	2.2	4	10	30
P0080S1BLRP	P-8B	6	25	50	800	2.2	4	20	35
P0220S1BLRP	P22B	15	32	50	800	2.2	4	10	30
P0300S1BLRP	P03B	25	40	50	800	2.2	4	10	30
P0640S1BLRP	P06B	58	77	120	800	2.2	4	10	30
P1800S1BLRP	P18B	170	220	120	800	2.2	4	10	30
P2300S1BLRP	P23B	190	260	120	800	2.2	4	10	30
P2600S1BLRP	P26B	220	300	120	800	2.2	4	10	30
P3100S1BLRP	P31B	275	350	120	800	2.2	4	10	30
P3500S1BLRP	P35B	320	400	120	800	2.2	4	10	30

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional (unless otherwise noted).

Revised: 02/23/17

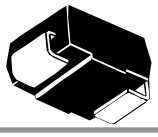
SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

Surge Ratings

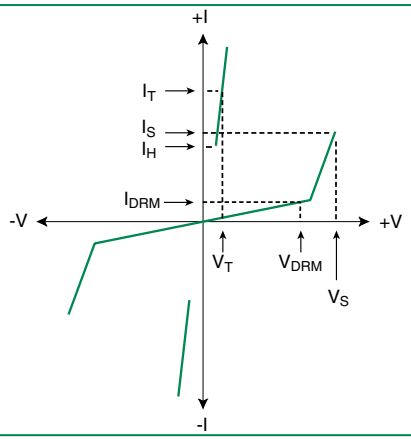
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	Amps/µs max
A	20	150	150	90	50	75	75	50	75	20	500
B	-	250	250	90	60	75	75	55	75	25	500

Notes:
1 Current waveform in µs
2 Voltage waveform in µs
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

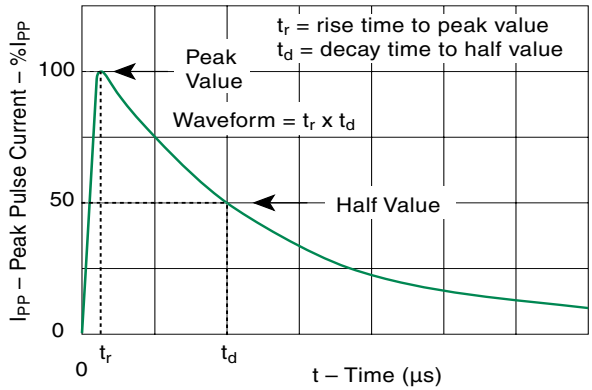
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
DO-214AC 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	90	°C/W

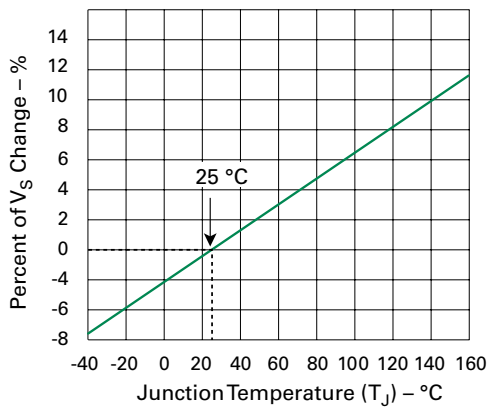
V-I Characteristics



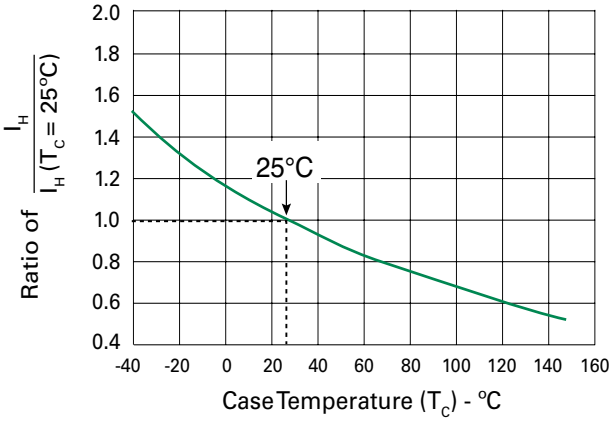
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

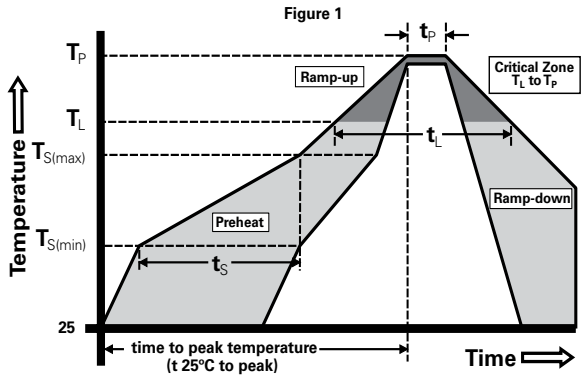


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

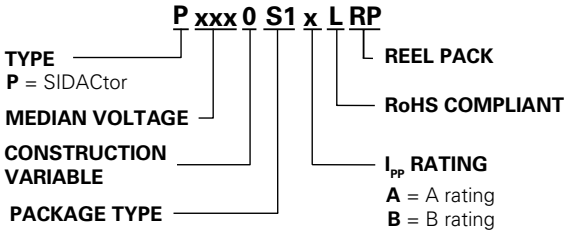
Additional Information

Datasheet | **Resources** | **Samples**

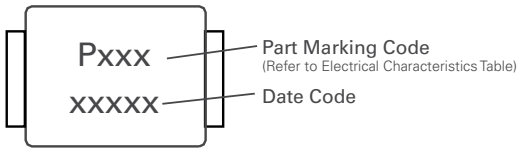
Revised: 02/23/17

SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

Part Numbering

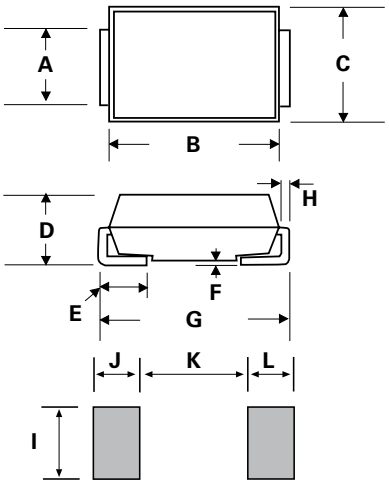


Part Marking



Dimensions

DO-214AC (SMA)

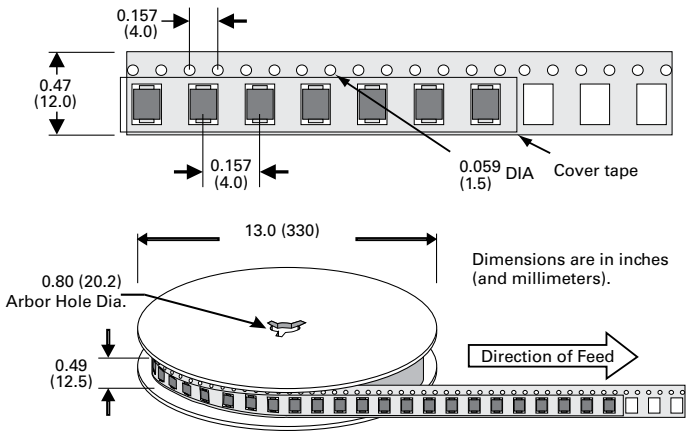


Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.049	0.065	1.250	1.650
B	0.157	0.177	3.990	4.500
C	0.100	0.110	2.540	2.790
D	0.078	0.090	1.980	2.290
E	0.030	0.060	0.780	1.520
F	-	0.008	-	0.203
G	0.194	0.208	4.930	5.280
H	0.006	0.012	0.152	0.305
I	0.070	-	1.800	-
J	0.082	-	2.100	-
K	-	0.090	-	2.300
L	0.082	-	2.100	-

Packing Options

Package Type	Description	Packing Options Quantity	Added Suffix	Industry Standard
S1	DO-214AC Tape & Reel Pack 12mm/13" tape	5000	RP	EIA-481

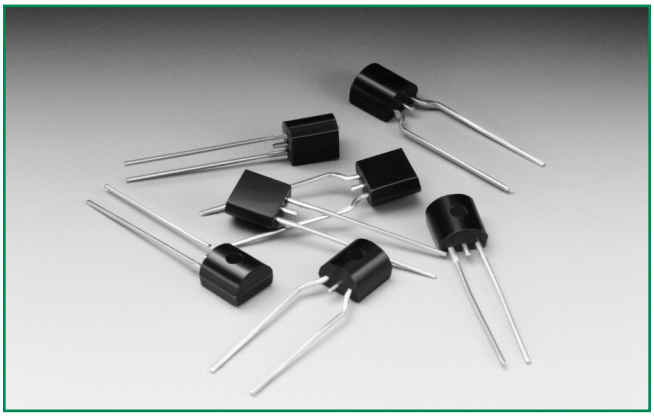
Tape and Reel Specification — DO-214AC



SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

Littelfuse
Expertise Applied | Answers Delivered

SIDACtor® Series - TO-92



Description

SIDACtor® Series TO-92 are designed to protect baseband equipment such as modems, line cards, CPE and DSL from damaging overvoltage transients.

The series provides a robust through-hole solution that enables equipment to comply with global regulatory standards.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Low capacitance
- 2nd level interconnect is Pb-free per IPC/ JEDEC J-STD-609A.01

Agency Approvals

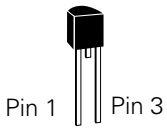
Agency	Agency File Number
UL	E133083

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level*
- ITU K.20/21 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5
- YD/T 1082
- YD/T 993
- YD/T 950

* A/B-rated parts require series resistance

Pinout Designation



Schematic Symbol

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	Capacitance @1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P0080EALxxx	P0080EA	6	25	50	800	2.2	4	25	150
P0300EALxxx	P0300EA	25	40	50	800	2.2	4	15	140
P0640EALxxx	P0640EA	58	77	150	800	2.2	4	40	60
P0720EALxxx	P0720EA	65	88	150	800	2.2	4	35	60
P0900EALxxx	P0900EA	75	98	150	800	2.2	4	35	55
P1100EALxxx	P1100EA	90	130	150	800	2.2	4	30	50
P1300EALxxx	P1300EA	120	160	150	800	2.2	4	25	45
P1500EALxxx	P1500EA	140	180	150	800	2.2	4	25	40
P1800EALxxx	P1800EA	170	220	150	800	2.2	4	25	35
P2300EALxxx	P2300EA	190	260	150	800	2.2	4	25	35
P2600EALxxx	P2600EA	220	300	150	800	2.2	4	20	35
P3100EALxxx	P3100EA	275	350	150	800	2.2	4	20	35
P3500EALxxx	P3500EA	320	400	150	800	2.2	4	20	35

Table continues on next page.

Revised: 02/23/17

Electrical Characteristics (continued)

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	Capacitance @1MHz, 2V bias	
		V Min	V Max	mA Min	mA Max	A Max	V Max	pF Min	pF Max
P0080EBLxxx	P0080EB	6	25	50	800	2.2	4	25	150
P0300EBLxxx	P0300EB	25	40	50	800	2.2	4	15	140
P0640EBLxxx	P0640EB	58	77	150	800	2.2	4	40	60
P0720EBLxxx	P0720EB	65	88	150	800	2.2	4	35	75
P0900EBLxxx	P0900EB	75	98	150	800	2.2	4	35	70
P1100EBLxxx	P1100EB	90	130	150	800	2.2	4	30	70
P1300EBLxxx	P1300EB	120	160	150	800	2.2	4	25	60
P1500EBLxxx	P1500EB	140	180	150	800	2.2	4	25	55
P1800EBLxxx	P1800EB	170	220	150	800	2.2	4	25	50
xxx	P2300EB	190	260	150	800	2.2	4	25	50
P2600EBLxxx	P2600EB	220	300	150	800	2.2	4	20	45
P3100EBLxxx	P3100EB	275	350	150	800	2.2	4	20	45
P3500EBLxxx	P3500EB	320	400	150	800	2.2	4	20	40
P0080ECLxxx	P0080EC	6	25	50	800	2.2	4	35	260
P0300ECLxxx	P0300EC	25	40	50	800	2.2	4	25	250
P0640ECLxxx	P0640EC	58	77	150	800	2.2	4	55	155
P0720ECLxxx	P0720EC	65	88	150	800	2.2	4	50	150
P0900ECLxxx	P0900EC	75	98	150	800	2.2	4	45	140
P1100ECLxxx	P1100EC	90	130	150	800	2.2	4	45	115
P1300ECLxxx	P1300EC	120	160	150	800	2.2	4	40	105
P1500ECLxxx	P1500EC	140	180	150	800	2.2	4	35	95
P1800ECLxxx	P1800EC	170	220	150	800	2.2	4	35	90
P2300ECLxxx	P2300EC	190	260	150	800	2.2	4	30	80
P2600ECLxxx	P2600EC	220	300	150	800	2.2	4	30	80
P3100ECLxxx	P3100EC	275	350	150	800	2.2	4	30	70
P3500ECLxxx	P3500EC	320	400	150	800	2.2	4	25	65

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Devices are bi-directional (unless otherwise noted).

Notes:
- xxx part number suffix: 'AP' = Ammo Pack, 'RP1' and 'RP2' = Reel Pack, blank = Bulk Pack

Surge Ratings

Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2x310 [1] 0.5x700 [2]	2x10 [1] 2x10 [2]	8x20 [1] 1.2x50 [2]	10x160 [1] 10x160 [2]	10x560 [1] 10x560 [2]	5x320 [1] 9x720 [2]	10x360 [1] 10x360 [2]	10x1000 [1] 10x1000 [2]	5x310 [1] 10x700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
A	20	150	150	90	50	75	75	45	75	20	500
B	25	250	250	150	100	100	125	80	100	25	500
C	50	500	400	200	150	200	175	100	200	30	500

Notes:

1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The device must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

Thermal Considerations

Package	Symbol	Parameter	Value	Unit
TO-92 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	90	°C/W

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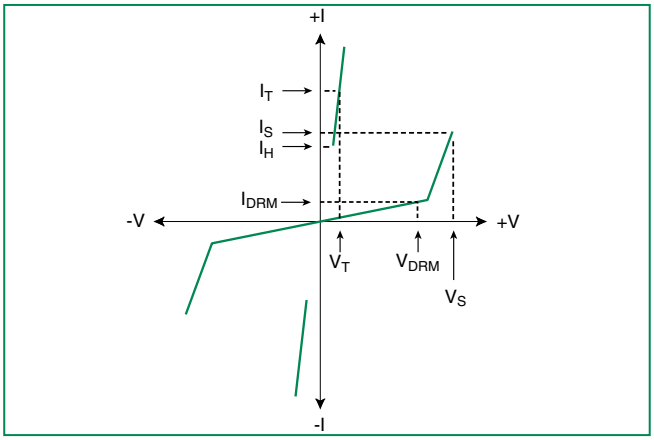
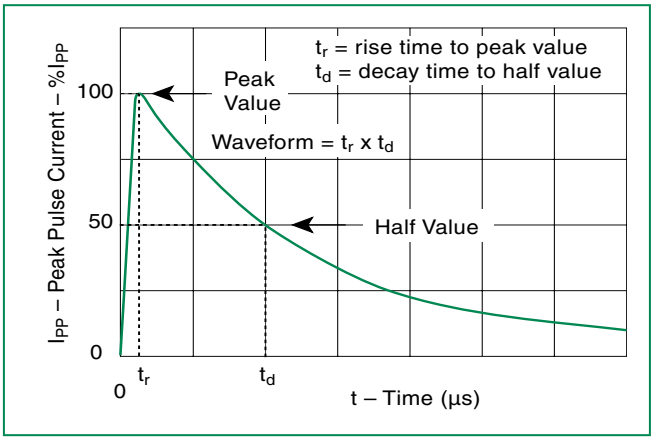
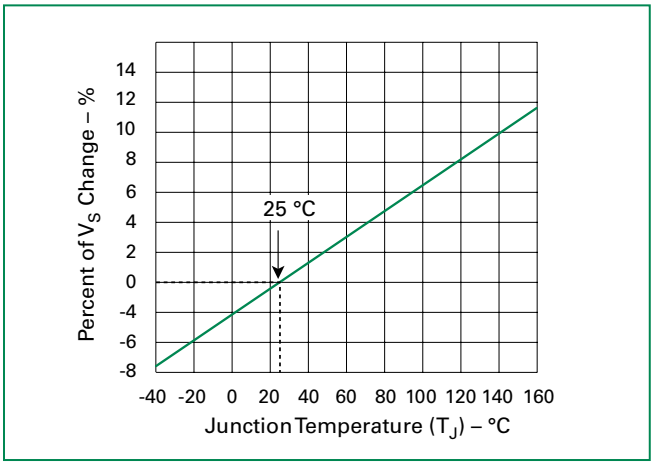
V-I Characteristics



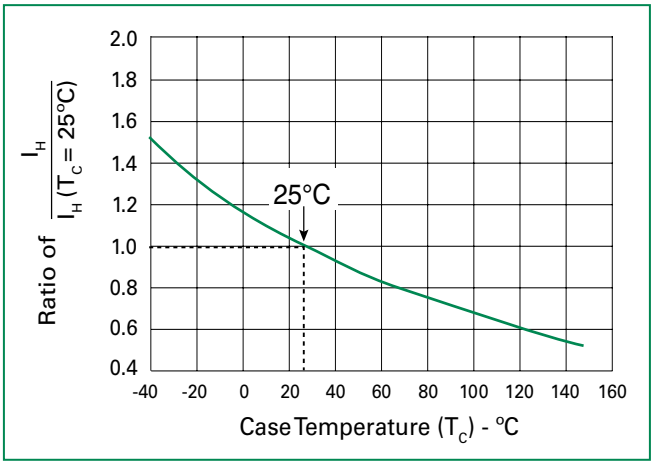
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



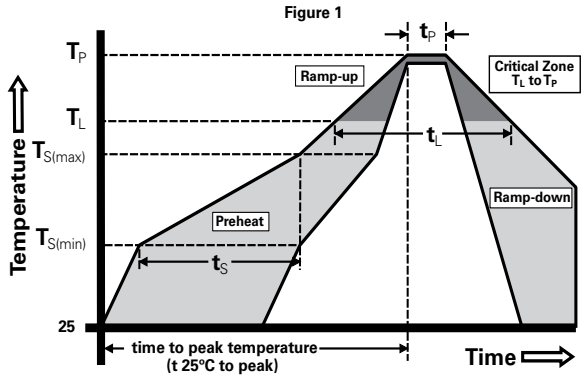
Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Revised: 02/23/17

SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

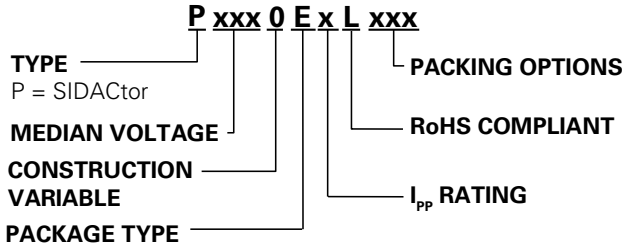
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification 94V-0

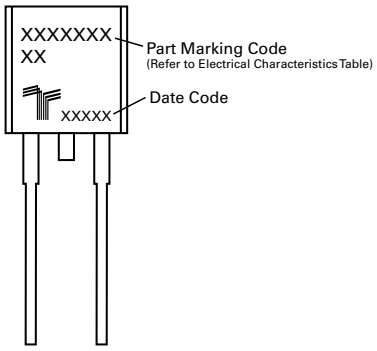
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering



Part Marking



Packing Options

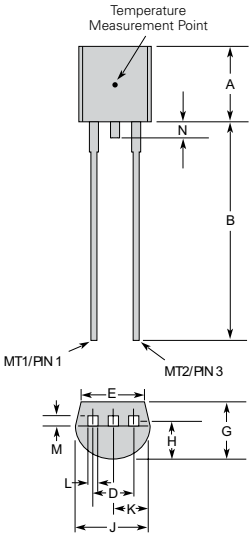
Package Type	Description	Packing Options Quantity	Added Suffix	Lead Spacing	Industry Standard
E	TO-92 Tape and Reel Pack	2000	RP1	0.1 inch (2.54mm)	EIA-481-D
			RP2	0.2 inch (5.08mm)	
	TO-92 Ammo Pack		AP		EIA-468-B
	TO-92 Bulk Pack		N/A		N/A

Additional Information

Datasheet | **Resources** | **Samples**

Revised: 02/23/17

Dimensions — TO-92



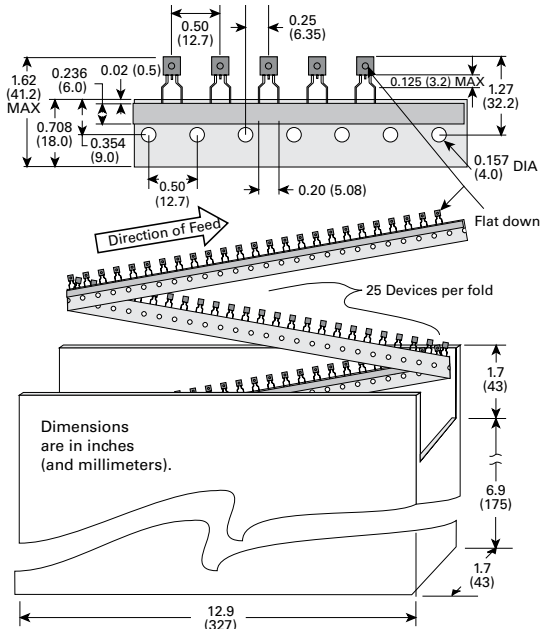
The TO-92 is designed to meet mechanical standards as set forth in JEDEC publication number 95.

	Inches		Millimeters	
	Min	Max	Min	Max
A	0.176	0.196	4.47	4.98
B	0.500		12.70	
D	0.095	0.105	2.41	2.67
E	0.150		3.81	
G	0.135	0.145	3.43	3.68
H	0.088	0.096	2.23	2.44
J	0.176	0.186	4.47	4.73
K	0.088	0.096	2.23	2.44
L	0.013	0.019	0.33	0.48
M	0.013	0.017	0.33	0.43
N		0.60		1.52

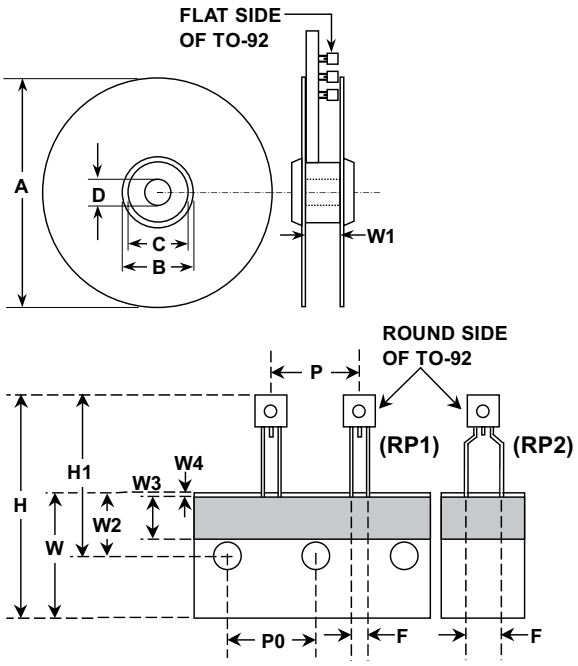
All leads are insulated from case. Case is electrically non-conductive. (Rated at 1600 $V_{(AC)\ RMS}$ for one minute from leads to case over the operating temperature range.)

Mold flash shall not exceed 0.13 mm per side.

Ammo Pack Specification — TO-92



Tape and Reel Specification — TO-92

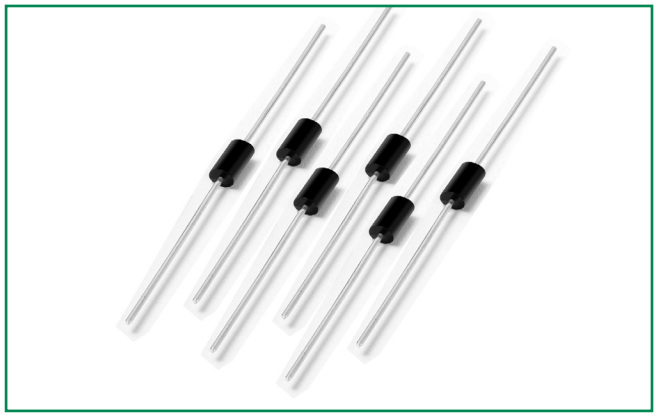


Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	N/A	14.173	N/A	360.0
B	4.016	N/A	102.0	N/A
C	3.386	N/A	86.0	N/A
D	0.795	N/A	20.2	N/A
W1	1.181	1.968	30.0	50.0
P	0.496	0.504	12.60	12.80
P0	0.498	0.502	12.65	12.75
F(for RP1)	0.090	0.110	2.29	2.80
F(for RP2)	0.182	0.244	4.63	6.19
H	N/A	1.673	N/A	42.50
H1	N/A	1.270	N/A	32.26
W	0.674	0.763	17.12	19.38
W2	0.354	0.370	8.25	9.75
W3	0.236	N/A	6.00	N/A
W4	0.020	N/A	0.50	N/A

Littelfuse
Expertise Applied | Answers Delivered

SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

SIDACtor® Series - DO-15



Description

The DO-15 series are designed to protect baseband equipment such as modems, line cards, CPE and DSL from damaging overvoltage transients.

The series provides a cost-effective through-hole solution that enables equipment to comply with global regulatory standards.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Low capacitance
- Fails short circuit when surged in excess of ratings
- 2nd level interconnect is Pb-free per IPC/ JEDEC J-STD-609A.01
- RoHS compliant, lead-free and halogen-free.

Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation

Not Applicable

Schematic Symbol

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Enhanced Level*
- ITU K.20/21/45 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

* A/B-rated parts require series resistance

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amps	Capacitance @1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P0080GALRP	P-8A	6	25	50	800	2.2	4	10	30
P1100GALRP	P11A	90	130	150	800	2.2	5	30	60
P1300GALRP	P13A	120	160	150	800	2.2	5	25	40
P1500GALRP	P15A	140	180	150	800	2.2	5	25	40
P1800GALRP	P18A	170	220	150	800	2.2	5	25	40
P2300GALRP	P23A	190	260	150	800	2.2	5	25	30
P2600GALRP	P26A	220	300	150	800	2.2	5	25	30
P3100GALRP	P31A	275	350	150	800	2.2	5	10	20
P3500GALRP	P35A	320	400	150	800	2.2	5	20	30
P1100GBLRP	P11B	90	130	150	800	2.2	5	30	60
P1300GBLRP	P13B	120	160	150	800	2.2	5	25	40
P1500GBLRP	P15B	140	180	150	800	2.2	5	25	40
P1800GBLRP	P18B	170	220	150	800	2.2	5	25	40
P2300GBLRP	P23B	190	260	150	800	2.2	5	25	30
P2600GBLRP	P26B	220	300	150	800	2.2	5	25	30
P3100GBLRP	P31B	275	350	150	800	2.2	5	20	30
P3500GBLRP	P35B	320	400	150	800	2.2	5	20	30
P4500GBLRP	P45B	400	530	150	800	2.2	5	20	45
P4500GCLRP	P45C	400	530	50	800	2.2	5	20	45

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional.

Revised: 02/23/17

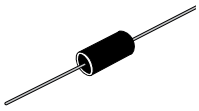
Surge Ratings

Series	I_{PP}			I_{TSM}
	10/560 [1] 10/560 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]	50 / 60 Hz
	Amps min	Amps min	Amps min	Amps min
A	50	45	-	20
B	100	80	100	25
C	-	-	150	25

Notes:

1 Current waveform in µs
2 Voltage waveform in µs
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40 to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

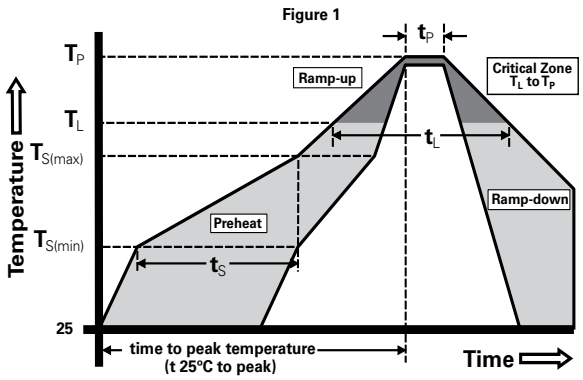
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
DO-15 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification V-0

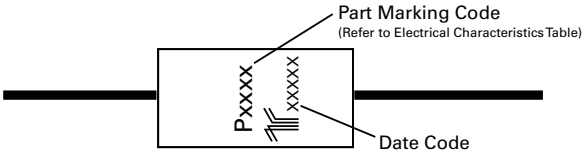
Additional Information

Datasheet | **Resources** | **Samples**

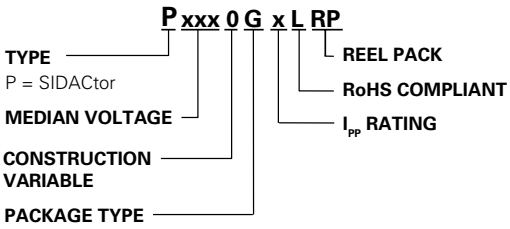
Revised: 02/23/17

SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

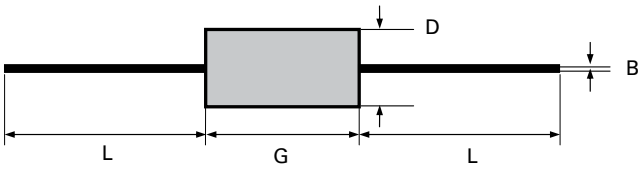
Part Marking



Part Numbering



Dimensions — DO-15



Dimension	Inches		Millimeters	
	MIN	MAX	MIN	MAX
B	0.028	0.034	0.711	0.864
D	0.12	0.14	3.048	3.556
G	0.235	0.27	5.969	6.858
L	1		25.4	

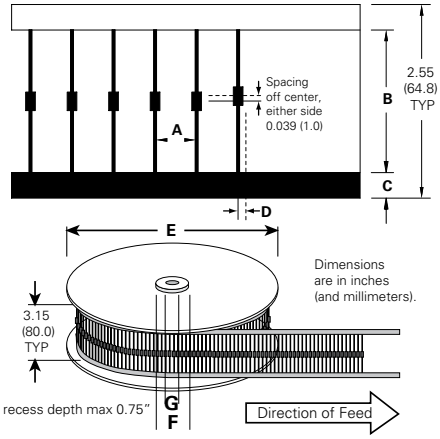
Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
G	DO-15 Axial Tape & Reel	5000	RP	EIA-RS-296-D

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Tape and Reel Specification — DO-15



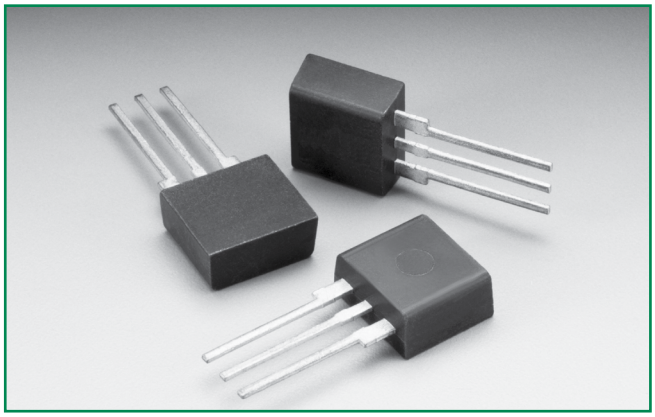
Symbols	Description	Inches	MM
A	Component Spacing (lead to lead)	0.200 ± 0.020"	5.08 ± 0.508
B	Inner Tape Pitch	2.062 ± 0.059"	52.37 ± 1.498
C	Tape Width	0.250"	6.35
D	Max. Off Alignment	0.048"	1.219
E	Reel Dimension	13"	330.2
F	Max. Hub Recess	3"	76.19
G	Max. Abor Hole	0.68"	17.27

Revised: 02/23/17

SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

Littelfuse
Expertise Applied | Answers Delivered

SIDACtor® Series - Modified TO-220



Description

The SIDACtor® Series Modified TO-220 thyristors are designed to protect baseband equipment from damaging overvoltage transients.

The series provides a robust single port through-hole solution that enables voice though DS-1 equipment to comply with various global regulatory standards.

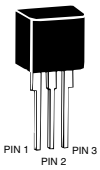
Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Modified TO-220 Package
- Fails short circuit when surged in excess of ratings
- Single-port protection
- Lead forms available
- RoHS Compliant
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

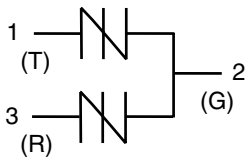
Agency Approvals

Agency	Agency File Number
UL	E133083

Pinout Designation



Schematic Symbol



Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level*
- ITU K.20/21 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

*A/B-rated parts require series resistance

Additional Information

Datasheet | **Resources** | **Samples**

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_T @I_T=2.2 A	I_H	I_S	I_T	Capacitance @1MHz, 2V bias	
		V min	V max	V min	V max	V max	mA min	mA max	A max	pF min	pf max
		Pins 1-2, 3-2		Pins 1-3		Pins 1-2, 3-2					
P0602AALxx	P0602AA	25	40	50	80	4	50	800	2.2	See Capacitance Values Table	
P1402AALxx	P1402AA	58	77	116	154	4	150	800	2.2		
P1602AALxx	P1602AA	65	95	130	190	4	150	800	2.2		
P2202AALxx	P2202AA	90	130	180	260	4	150	800	2.2		
P2702AALxx	P2702AA	120	160	240	320	4	150	800	2.2		
P3002AALxx	P3002AA	140	180	280	360	4	150	800	2.2		
P3602AALxx	P3602AA	170	220	340	440	4	150	800	2.2		
P4202AALxx	P4202AA	190	250	380	500	4	150	800	2.2		
P4802AALxx	P4802AA	220	300	440	600	4	150	800	2.2		
P6002AALxx	P6002AA	275	350	550	700	4	150	800	2.2		

Table continues on next page.

Revised: 02/23/17

Electrical Characteristics (continued)

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_T @I_T=2.2 A	I_H	I_S	I_T	Capacitance
		V min	V max	V min	V max	V max	mA min	mA max	A max	
		Pins 1-2, 3-2		Pins 1-3		Pins 1-2, 3-2				
P0602ABLxx	P0602AB	25	40	50	80	4	50	800	2.2	See Capacitance Values Table
P1402ABLxx	P1402AB	58	77	116	154	4	150	800	2.2	
P1602ABLxx	P1602AB	65	95	130	190	4	150	800	2.2	
P2202ABLxx	P2202AB	90	130	180	260	4	150	800	2.2	
P2702ABLxx	P2702AB	120	160	240	320	4	150	800	2.2	
P3002ABLxx	P3002AB	140	180	280	360	4	150	800	2.2	
P3602ABLxx	P3602AB	170	220	340	440	4	150	800	2.2	
P4202ABLxx	P4202AB	190	250	380	500	4	150	800	2.2	
P4802ABLxx	P4802AB	220	300	440	600	4	150	800	2.2	
P6002ABLxx	P6002AB	275	350	550	700	4	150	800	2.2	
P0602ACLxx	P0602AC	25	40	50	80	4	50	800	2.2	
P1402ACLxx	P1402AC	58	77	116	154	4	150	800	2.2	
P1602ACLxx	P1602AC	65	95	130	190	4	150	800	2.2	
P2202ACLxx	P2202AC	90	130	180	260	4	150	800	2.2	
P2702ACLxx	P2702AC	120	160	240	320	4	150	800	2.2	
P3002ACLxx	P3002AC	140	180	280	360	4	150	800	2.2	
P3602ACLxx	P3602AC	170	220	340	440	4	150	800	2.2	
P4202ACLxx	P4202AC	190	250	380	500	4	150	800	2.2	
P4802ACLxx	P4802AC	220	300	440	600	4	150	800	2.2	
P6002ACLxx	P6002AC	275	350	550	700	4	150	800	2.2	

Notes:
- Absolute maximum ratings measured at T_A= 25ºC (unless otherwise noted).
- Devices are bi-directional (unless otherwise noted).
- **XX** Part Number Suffix: **'RP'** (Reel Pack), **Blank** (Bulk Pack), or **'60'** (Type 60 lead form bulk pack)

Capacitance Values

Part Number	pF Pin 1-2, 3-2 Tip-Ground, Ring-Ground		pF Pin 1-3 Tip-Ring	
	MIN	MAX	MIN	MAX
P0602AALxx	15	145	10	90
P1402AALxx	40	60	20	35
P1602AALxx	35	60	20	35
P2202AALxx	30	50	15	30
P2702AALxx	25	45	15	25
P3002AALxx	25	40	15	25
P3602AALxx	25	35	10	20
P4202AALxx	25	35	10	20
P4802AALxx	20	35	10	20
P6002AALxx	20	35	10	20
P0602ABLxx	15	250	10	145
P1402ABLxx	40	155	20	90
P1602ABLxx	35	145	20	85
P2202ABLxx	30	115	15	65
P2702ABLxx	25	105	15	60
P3002ABLxx	25	95	15	55
P3602ABLxx	25	90	10	50
P4202ABLxx	25	85	10	50
P4802ABLxx	20	85	10	50
P6002ABLxx	20	80	10	45

Part Number	pF Pin 1-2, 3-2 Tip-Ground, Ring-Ground		pF Pin 1-3 Tip-Ring	
	MIN	MAX	MIN	MAX
P0602ACLxx	25	250	10	145
P1402ACLxx	55	155	30	90
P1602ACLxx	45	145	25	85
P2202ACLxx	45	115	25	65
P2702ACLxx	40	105	20	60
P3002ACLxx	35	95	20	55
P3602ACLxx	35	90	15	50
P4202ACLxx	30	85	15	50
P4802ACLxx	30	85	15	50
P6002ACLxx	30	80	15	45

Note: Off-state capacitance (C_O) is measured at 1 MHz with a 2 V bias.

Revised: 02/23/17

Surge Ratings

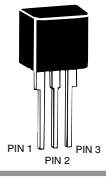
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2x310 [1] 0.5x700 [2]	2x10 [1] 2x10 [2]	8x20 [1] 1.2x50 [2]	10x160 [1] 10x160 [2]	10x560 [1] 10x560 [2]	5x320 [1] 9x720 [2]	10x360 [1] 10x360 [2]	10x1000 [1] 10x1000 [2]	5x310 [1] 10x700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
A	20	150	150	90	50	75	75	45	75	20	500
B	25	250	250	150	100	100	125	80	100	25	500
C	50	500	400	200	150	200	175	100	200	50	500

Notes:

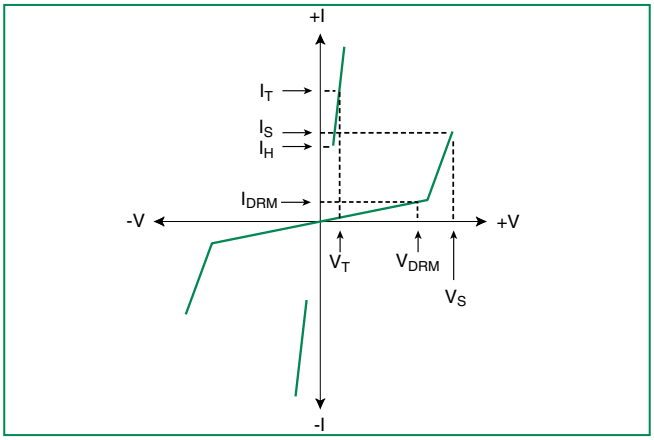
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The device must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

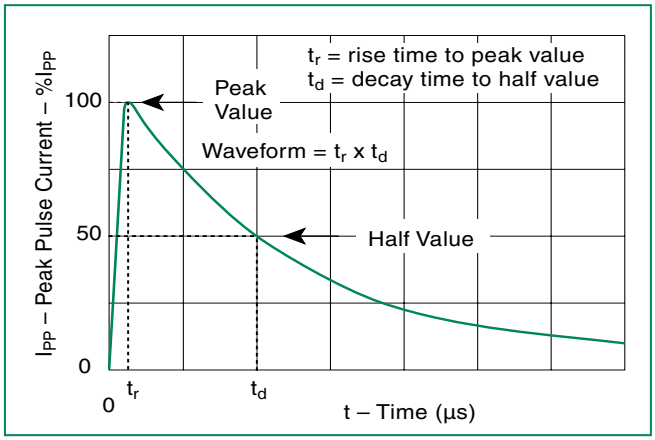
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified TO-220 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

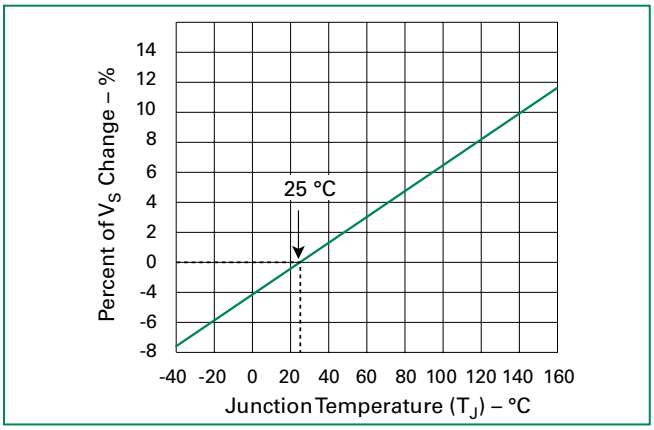
V-I Characteristics



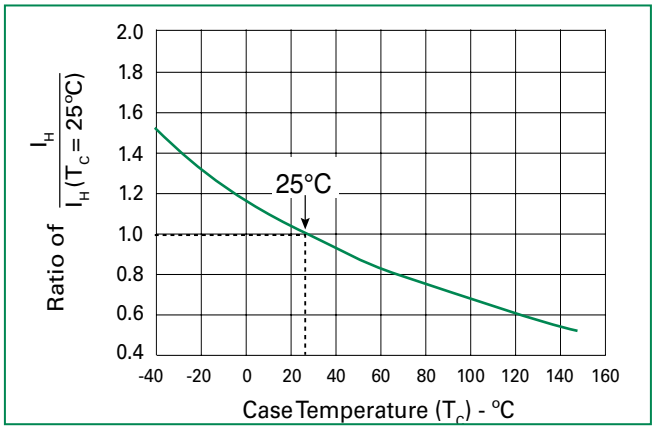
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

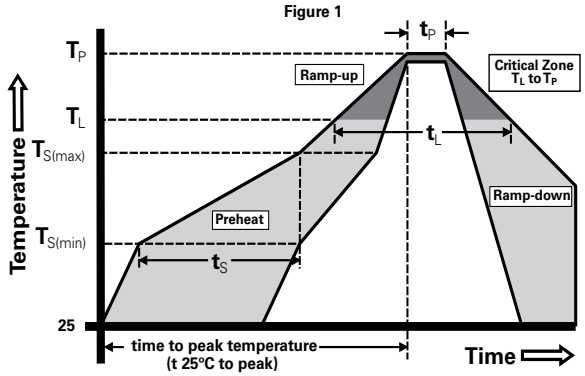


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



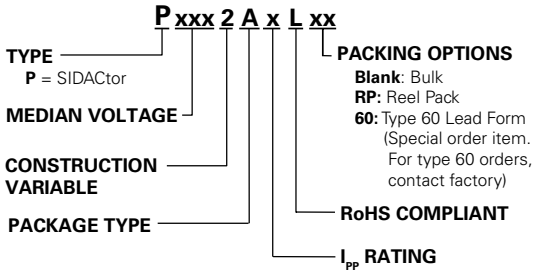
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

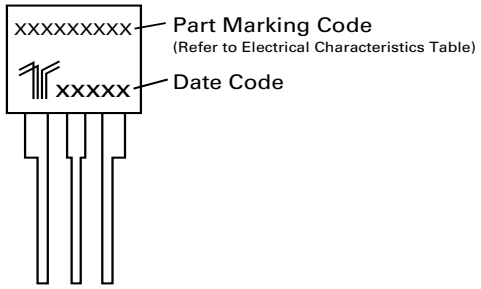
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering



Part Marking



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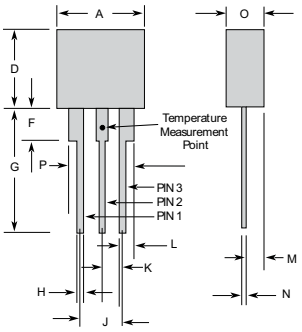
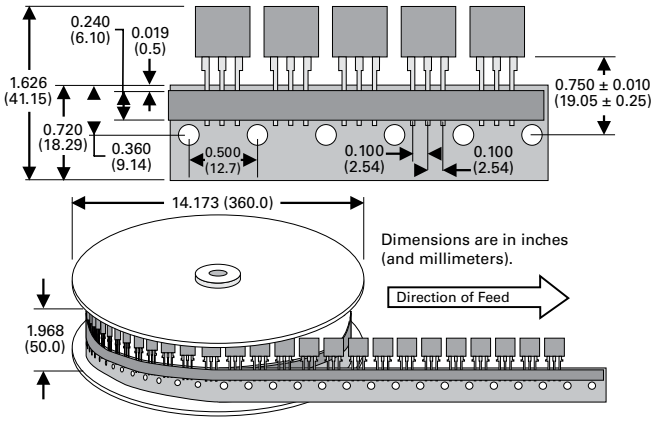
Dimensions - Modified TO-220



The modified TO-220 package is designed to meet mechanical standards as set forth in JEDEC publication number 95.

	Inches		Millimeters	
	Min	Max	Min	Max
A	0.400	0.410	10.16	10.42
D	0.360	0.375	9.14	9.53
F	0.110	0.130	2.80	3.30
G	0.540	0.575	13.71	14.61
H	0.025	0.035	0.63	0.89
J	0.195	0.205	4.95	5.21
K	0.095	0.105	2.41	2.67
L	0.060	0.075	1.52	1.90
M	0.070	0.085	1.78	2.16
N	0.018	0.024	0.46	0.61
O	0.178	0.188	4.52	4.78
P	0.290	0.310	7.37	7.87

Tape and Reel Specification — Modified TO-220

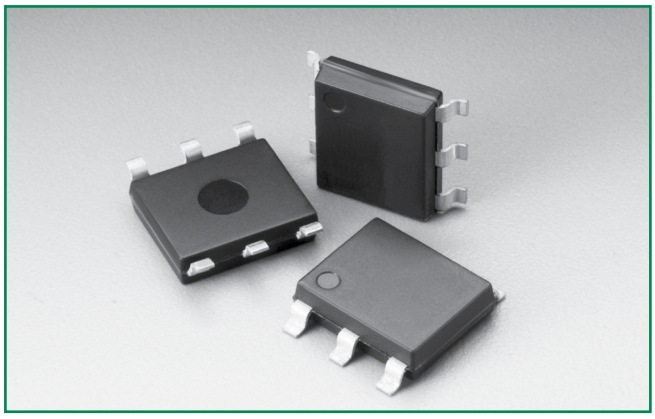


Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
A	Modified TO-220 Tape and Reel Pack	700	RP	EIA-468-B
	Modified TO-220 Bulk Pack	500	N/A	N/A
	Modified TO-220 Type 60 Lead Form Bulk Pack	500	60 (special order item, contact factory for details)	N/A

SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

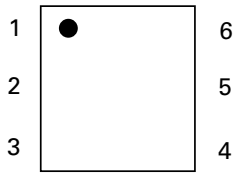
SIDACtor® Multiport Series - MS-013



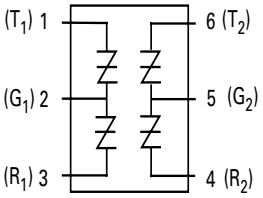
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Description

SIDACtor® Multiport Series thyristors MS-013 are designed to protect baseband equipment from overvoltage transients.

Targeted for voice through DS-1 applications, the series provides a dual port surface mount solution that enables equipment to comply with various global regulatory standards.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Replaces four discrete components
- Fails short circuit when surged in excess of ratings
- Low capacitance
- RoHS Compliant
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level*
- ITU K.20/21 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

*A-rated parts require series resistance

Additional Information

Datasheet | **Resources** | **Samples**

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_T @I_T=2.2 Amps	I_H	I_S	I_T	Capacitance
		V min	V max	V min	V max	V max	mA min	mA max	A max	
		Pins 1-2, 3-2, 4-5, 6-5		Pins 1-3, 4-6		Pins 1-2, 3-2, 4-5, 6-5				
P0084UALxx	P0084UA	6	25	12	50	4	50	800	2.2	See Capacitance Values Table
P0304UALxx	P0304UA	25	40	50	80	4	50	800	2.2	
P0644UALxx	P0644UA	58	77	116	154	4	150	800	2.2	
P0724UALxx	P0724UA	65	88	130	176	4	150	800	2.2	
P0904UALxx	P0904UA	75	98	150	196	4	150	800	2.2	
P1104UALxx	P1104UA	90	130	180	260	4	150	800	2.2	
P1304UALxx	P1304UA	120	160	240	320	4	150	800	2.2	
P1504UALxx	P1504UA	140	180	280	360	4	150	800	2.2	

Table continues on next page.

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Electrical Characteristics (continued)

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_T @I_T=2.2 Amps	I_H	I_S	I_T	Capacitance
		V min	V max	V min	V max	V max	mA min	mA max	A max	
		Pins 1-2, 3-2, 4-5, 6-5		Pins 1-3, 4-6		Pins 1-2, 3-2, 4-5, 6-5				
P1804UALxx	P1804UA	170	220	340	440	4	150	800	2.2	See Capacitance Values Table
P2304UALxx	P2304UA	190	260	380	520	4	150	800	2.2	
P2604UALxx	P2604UA	220	300	440	600	4	150	800	2.2	
P3104UALxx	P3104UA	275	350	550	700	4	150	800	2.2	
P3504UALxx	P3504UA	320	400	640	800	4	150	800	2.2	
P0084UCLxx	P0084UC	6	25	12	50	4	50	800	2.2	
P0304UCLxx	P0304UC	25	40	50	80	4	50	800	2.2	
P0644UCLxx	P0644UC	58	77	116	154	4	150	800	2.2	
P0724UCLxx	P0724UC	65	88	130	176	4	150	800	2.2	
P0904UCLxx	P0904UC	75	98	150	196	4	150	800	2.2	
P1104UCLxx	P1104UC	90	130	180	260	4	150	800	2.2	
P1304UCLxx	P1304UC	120	160	240	320	4	150	800	2.2	
P1504UCLxx	P1504UC	140	180	280	360	4	150	800	2.2	
P1804UCLxx	P1804UC	170	220	340	440	4	150	800	2.2	
P2304UCLxx	P2304UC	190	260	380	520	4	150	800	2.2	
P2604UCLxx	P2604UC	220	300	440	600	4	150	800	2.2	
P3104UCLxx	P3104UC	275	350	550	700	4	150	800	2.2	
P3504UCLxx	P3504UC	320	400	640	800	4	150	800	2.2	

Notes:
- Absolute maximum ratings measured at T_A= +25°C (unless otherwise noted).
- Components are bi-directional
- **XX =** Part Number Suffix: '**TP'** (Tube Pack) or '**RP'** (Reel Pack).

Capacitance Values

Part Number	Pin 1-2 / 3-2 (4-5 / 6-5) Tip-Ground, Ring-Ground		Pin 1-3 (4-6) Tip-Ring	
	pF min	pF max	pF min	pF max
P0084UALxx	25	155	15	90
P0304UALxx	15	140	10	90
P0644UALxx	40	60	20	35
P0724UALxx	35	60	20	35
P0904UALxx	35	55	20	30
P1104UALxx	30	50	15	30
P1304UALxx	25	45	15	25
P1504UALxx	25	40	15	25
P1804UALxx	25	35	10	20
P2304UALxx	25	35	10	20
P2604UALxx	20	35	10	20
P3104UALxx	20	35	10	20
P3504UALxx	20	35	10	20
P0084UCLxx	35	285	20	165
P0304UCLxx	25	250	10	145
P0644UCLxx	55	155	30	90
P0724UCLxx	50	145	25	85
P0904UCLxx	45	135	25	80
P1104UCLxx	45	115	25	65
P1304UCLxx	40	105	20	60
P1504UCLxx	35	95	20	55
P1804UCLxx	35	90	15	50
P2604UCLxx	30	85	15	50
P3104UCLxx	30	80	15	45
P3504UCLxx	25	75	15	45

Revised: 02/23/17

SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

Surge Ratings

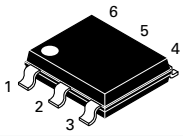
Series	I_{PP}									I_{TSM}	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]	50/60 Hz	
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
A	20	150	150	90	50	75	75	45	75	20	500
C	50	500	400	200	150	200	175	100	200	30	500

Notes:

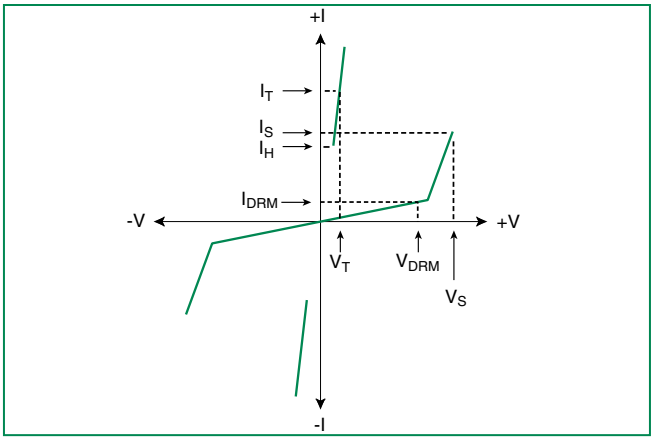
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

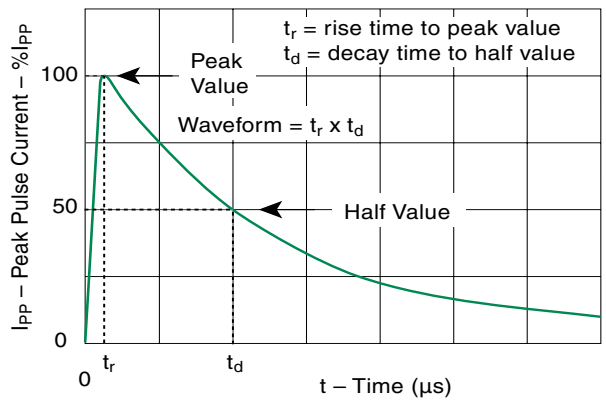
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified MS-013 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

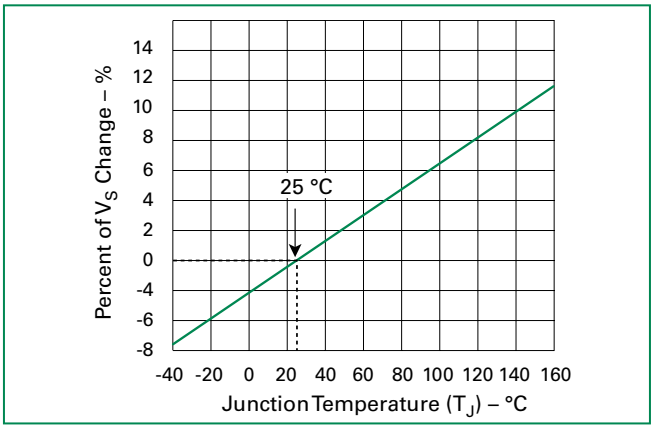
V-I Characteristics



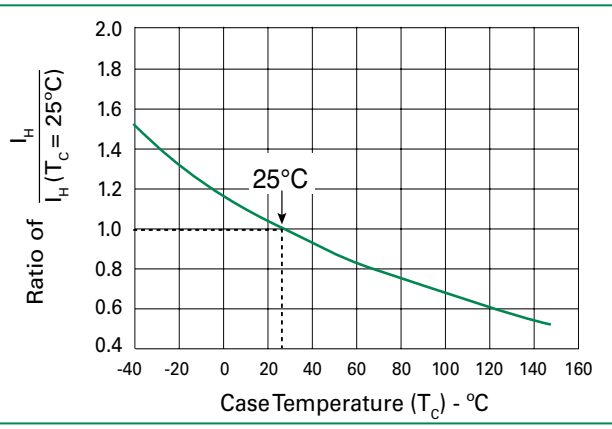
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

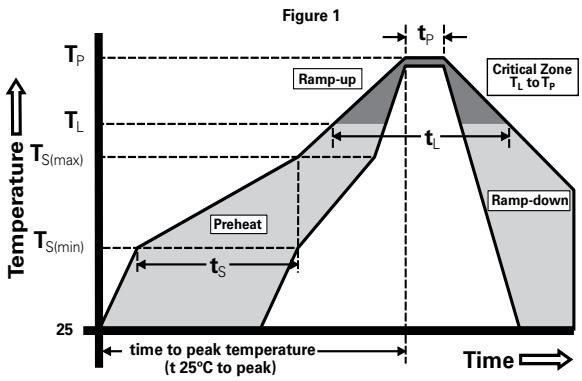


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



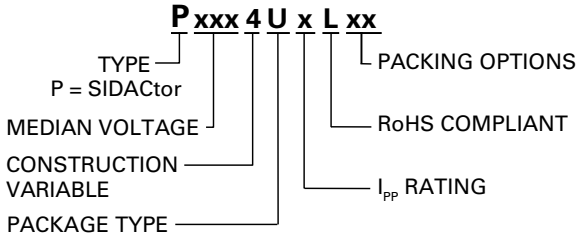
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

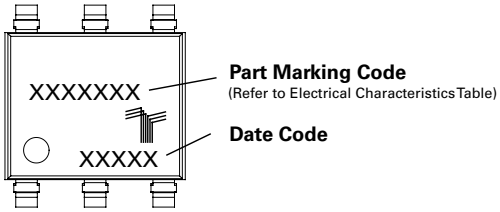
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering



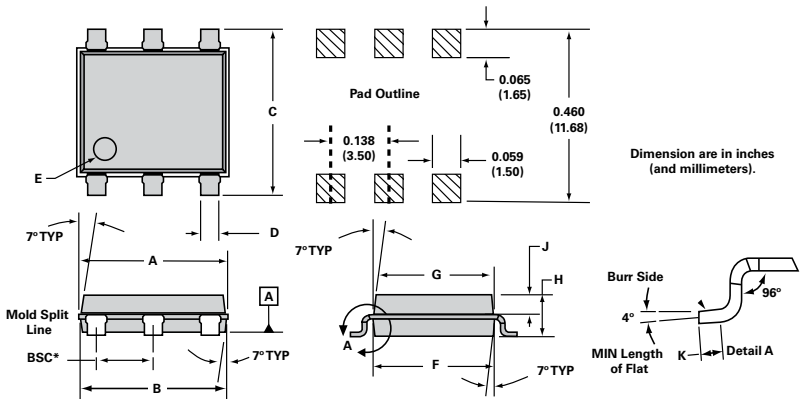
Part Marking



Revised: 02/23/17

SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

Dimensions — MS-013



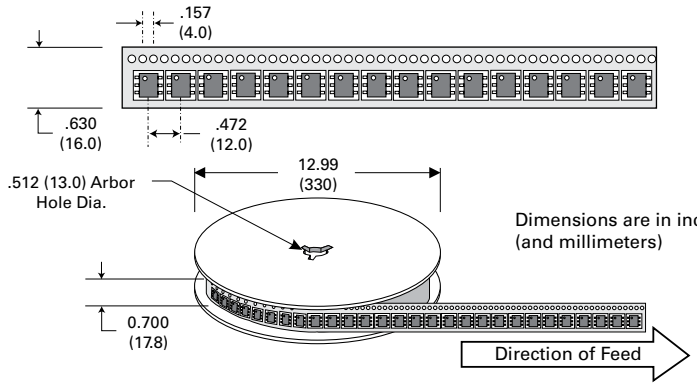
Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.360	0.364	9.14	9.25
B	0.352	0.356	8.94	9.04
C	0.400	0.412	10.16	10.46
D	0.043	0.045	1.09	1.13
E	0.047	0.055	1.19	1.40
F	0.293	0.297	7.44	7.54
G	0.289	0.293	7.34	7.44
H	0.089	0.093	2.26	2.36
J	0.041	0.049	1.04	1.24
K	0.020	---	0.51	---
BSC*	0.133	0.143	3.38	3.63

* BSC = **B**asic **S**pacing between **C**enters

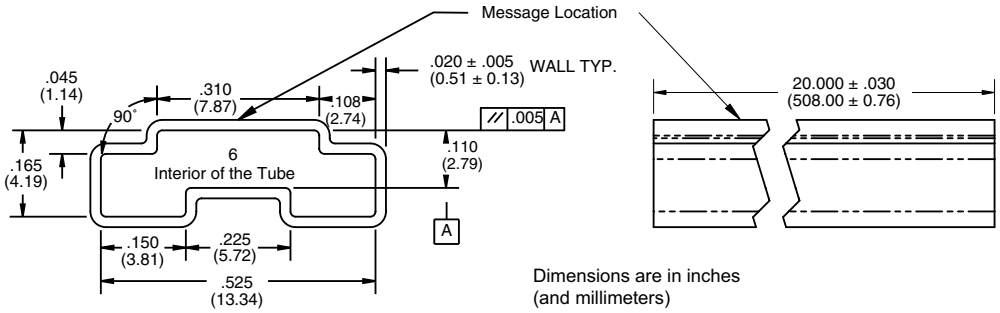
Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
U	Modified MS-013 6-pin Tape and Reel Pack	1500	RP	EIA-481-D
	Modified MS-013 6-pin Tube Pack	500 (50 per tube)	TP	N/A

Tape and Reel Specification — MS-013

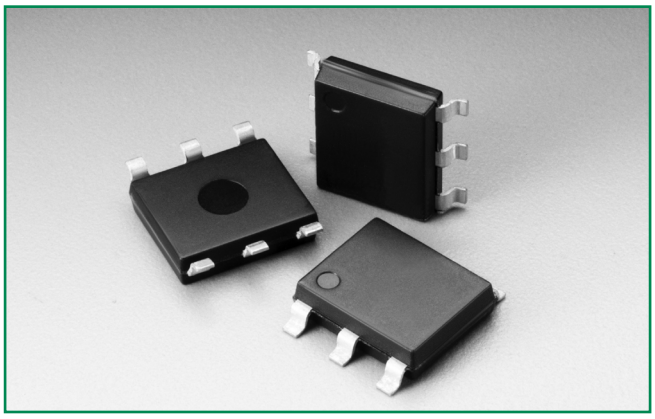


Tube Pack Specification — MS-013



Revised: 02/23/17

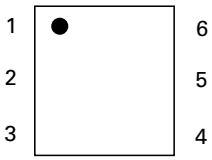
SIDACtor® Balanced Series - MS-013



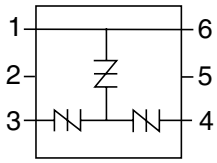
Agency Approvals

Agency	Agency File Number
UL	E133083

Pinout Designation



Schematic Symbol



Description

The SIDACtor® Balanced Series MS-013 are designed to protect baseband equipment from overvoltage transients. The patented "Y" configuration ensures balanced overvoltage protection that prevents a longitudinal to differential conversion.

The series provides a single port surface mount solution that enables voice through DS-1 equipment to comply with various global requlatory standards.

Features and Benefits

- Balanced overvoltage protection
- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Replaces three discrete components
- Meets UL/IEC 60950-1 creepage and clearance
- RoHS Compliant and Lead-Free
- 2nd level interconnect is Pb-free per IPC/JEDEC J-STD-609A.01

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Enhanced Level
- ITU K.20/21/45 Basic Level
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

Electrical Characteristics

Part Number	Part Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_T	I_S	I_T	I_H	Capacitance
		V min	V max	V min	V max	V max	mA max	A max	mA min	
		Pins 1 & 6-3, 1 & 6-4		Pins 3-4						
P1553UALxx	P1553UA	130	180	130	180	8	800	2.2	150	See Capacitance Values table
P1803UALxx	P1803UA	150	210	150	210	8	800	2.2	150	
P2103UALxx	P2103UA	170	250	170	250	8	800	2.2	150	
P2353UALxx	P2353UA	200	270	200	270	8	800	2.2	150	
P2703UALxx	P2703UA	230	300	230	300	8	800	2.2	150	
P3203UALxx	P3203UA	270	350	270	350	8	800	2.2	150	
P3403UALxx	P3403UA	300	400	300	400	8	800	2.2	150	
P5103UALxx	P5103UA	420	600	420	600	8	800	2.2	150	

Table continues on next page.

Notes:
- Absolute maximum ratings measured at T_A= +25°C (unless otherwise noted).
- Components are bi-directional.
- **XX =** Part Number Suffix: '**TP'** (Tube Pack) or '**RP'** (Reel Pack).

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Electrical Characteristics (continued)

Part Number	Part Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_T	I_S	I_T	I_H	Capacitance
		V min	V max	V min	V max	V max	mA max	A max	mA min	
		Pins 1 & 6-3, 1 & 6-4		Pins 3-4						
P1553UBLxx	P1553UB	130	180	130	180	8	800	2.2	150	See Capacitance Values table
P1803UBLxx	P1803UB	150	210	150	210	8	800	2.2	150	
P2103UBLxx	P2103UB	170	250	170	250	8	800	2.2	150	
P2353UBLxx	P2353UB	200	270	200	270	8	800	2.2	150	
P2703UBLxx	P2703UB	230	300	230	300	8	800	2.2	150	
P3203UBLxx	P3203UB	270	350	270	350	8	800	2.2	150	
P3403UBLxx	P3403UB	300	400	300	400	8	800	2.2	150	
P5103UBLxx	P5103UB	420	600	420	600	8	800	2.2	150	
P1553UCLxx	P1553UC	130	180	130	180	8	800	2.2	150	
P1803UCLxx	P1803UC	150	210	150	210	8	800	2.2	150	
P2103UCLxx	P2103UC	170	250	170	250	8	800	2.2	150	
P2353UCLxx	P2353UC	200	270	200	270	8	800	2.2	150	
P2703UCLxx	P2703UC	230	300	230	300	8	800	2.2	150	
P3203UCLxx	P3203UC	270	350	270	350	8	800	2.2	150	
P3403UCLxx	P3403UC	300	400	300	400	8	800	2.2	150	
P5103UCLxx	P5103UC	420	600	420	600	8	800	2.2	150	

Capacitance Values

Part Number	Pin 3-4 Tip-Ring		Pins 1 & 6-3, 1 & 6-4 Tip-Ground, Ring-Ground	
	pF min	pF max	pF min	pF max
P1553UALxx	20	95	10	60
P1803UALxx	20	85	10	55
P2103UALxx	15	85	10	55
P2353UALxx	15	75	10	50
P2703UALxx	15	75	10	50
P3203UALxx	15	70	10	45
P3403UALxx	15	65	10	45
P5103UALxx	10	60	10	40
P1553UBLxx	25	95	15	60
P1803UBLxx	25	85	15	55
P2103UBLxx	20	85	15	55
P2353UBLxx	20	75	15	50
P2703UBLxx	20	75	10	50
P3203UBLxx	20	70	10	45
P3403UBLxx	15	65	10	45
P5103UBLxx	15	60	10	40
P1553UCLxx	30	95	20	60
P1803UCLxx	30	85	15	55
P2103UCLxx	30	85	15	55
P2353UCLxx	25	75	15	50
P2703UCLxx	25	75	15	50
P3203UCLxx	25	70	15	45
P3403UCLxx	20	65	15	45
P5103UCLxx	20	60	10	40

Note: Off-state capacitance (C_O) is measured at 1 MHz with a 2 V bias.

Additional Information

Datasheet | **Resources** | **Samples**

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Surge Ratings

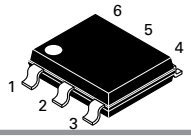
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/ µs max
A	20	150	150	90	50	75	75	45	75	20	500
B	25	250	250	150	100	100	125	80	100	25	500
C	50	500	400	200	150	200	175	100	200	50	500

Notes:

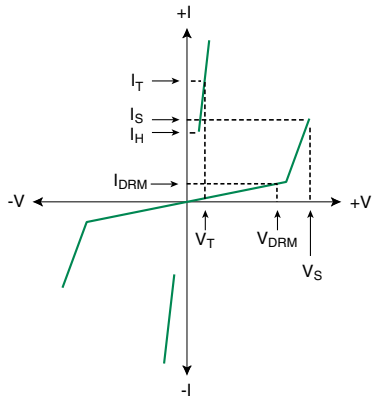
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40 to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

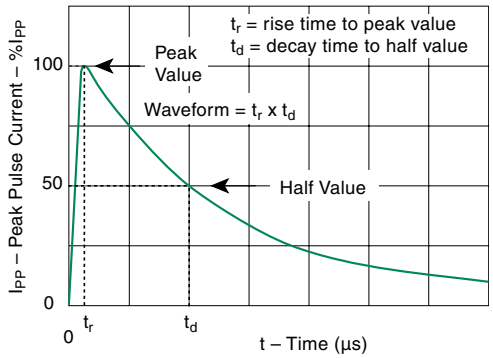
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified MS-013 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

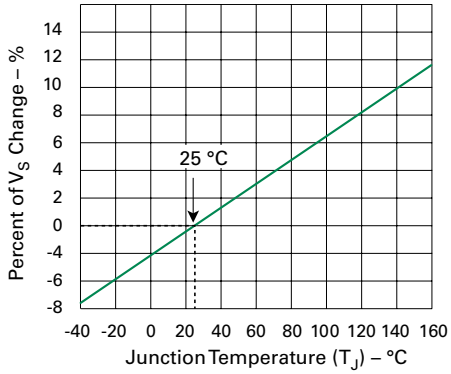
V-I Characteristics



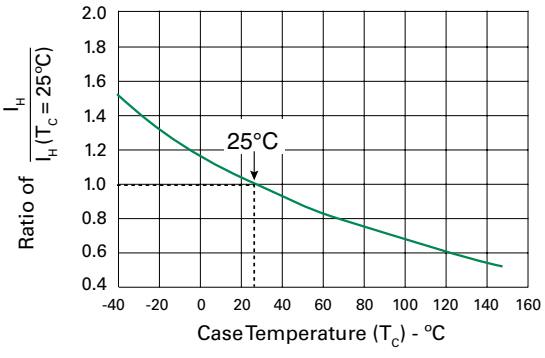
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature



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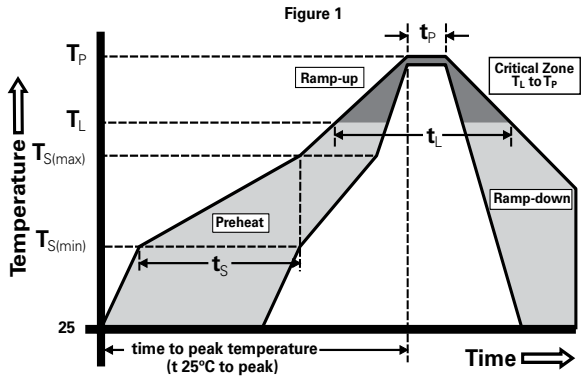
SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



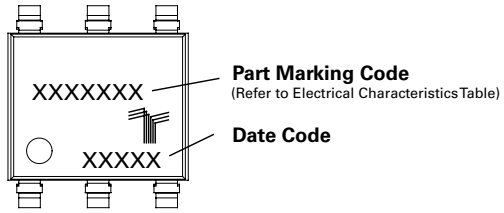
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

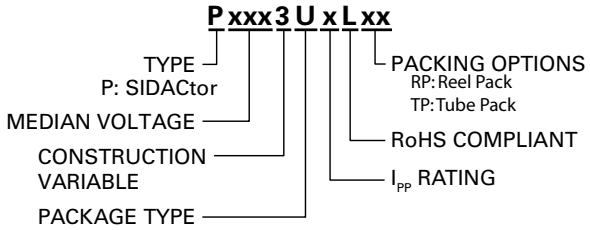
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Marking



Part Numbering



Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
U	Modified MS-013 6-pin Tape and Reel Pack	1500	RP	EIA-481-D
	Modified MS-013 6-pin Tube Pack	500 (50 per tube)	TP	N/A

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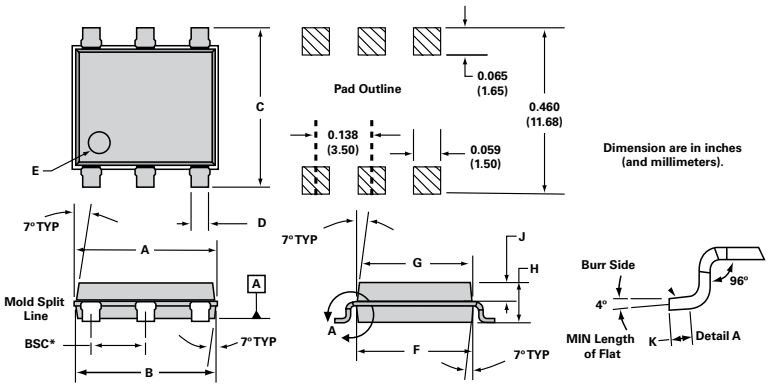
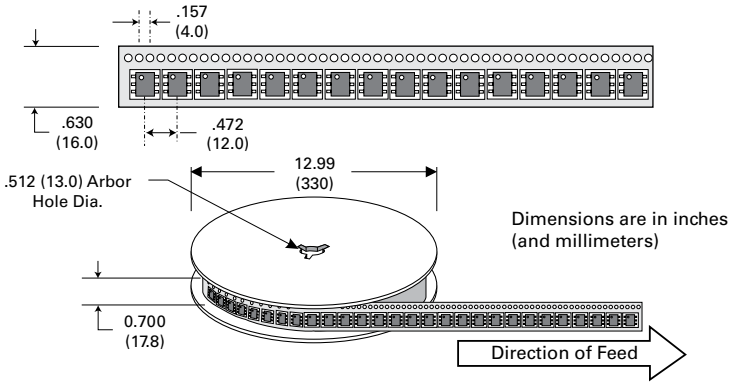
Dimensions — MS-013



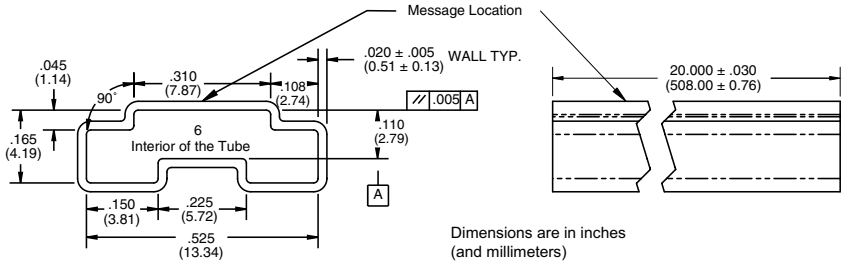
Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.360	0.364	9.14	9.25
B	0.352	0.356	8.94	9.04
C	0.400	0.412	10.16	10.46
D	0.043	0.045	1.09	1.13
E	0.047	0.055	1.19	1.40
F	0.293	0.297	7.44	7.54
G	0.289	0.293	7.34	7.44
H	0.089	0.093	2.26	2.36
J	0.041	0.049	1.04	1.24
K	0.020		0.51	
BSC*	0.133	0.143	3.38	3.63

* BSC = **B**asic **S**pacing between **C**enters

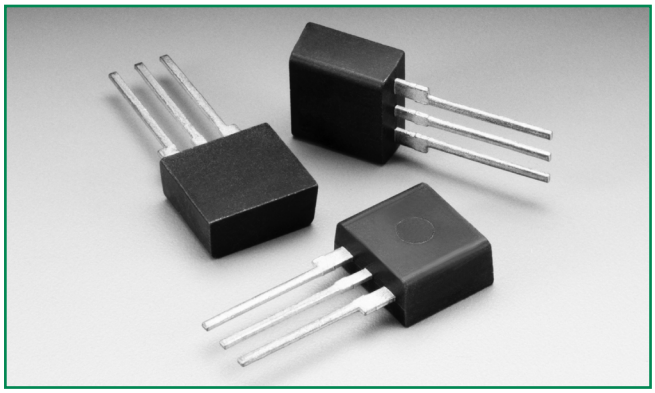
Tape and Reel Specification — MS-013



Tube Pack Specification — MS-013



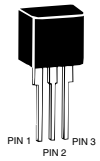
SIDACtor® Balanced Series - Modified TO-220



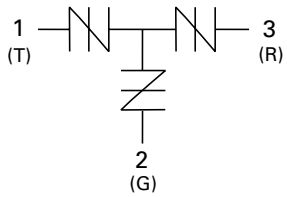
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Description

The SIDACtor® Balanced Series are designed to protect baseband equipment from damaging overvoltage transients. The patented "Y" configuration also ensures balanced overvoltage protection that prevents a longitudinal to differential conversion.

The series provides a single port through-hole solution that enables voice through DS-1 equipment to comply with various global requlatory standards.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Low capacitance
- Balanced overvoltage protection
- Single port protection
- Custom lead forms available
- RoHS Compliant and Lead-Free
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Enhanced Level*
- ITU K.20/21/45 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

*A/B-rated parts require series resistance

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T@I_T= 2.2 Amps	Capacitance
		V min	V max	V min	V max	mA min	mA max	A max	V max	
		Pins 1-2, 3-2		Pins 1-3						
P1553AALxx	P1553AA	130	180	130	180	150	800	2.2	8	See Capacitance Values table
P1803AALxx	P1803AA	150	210	150	210	150	800	2.2	8	
P2103AALxx	P2103AA	170	250	170	250	150	800	2.2	8	
P2353AALxx	P2353AA	200	270	200	270	150	800	2.2	8	
P2703AALxx	P2703AA	230	300	230	300	150	800	2.2	8	
P3203AALxx	P3203AA	270	350	270	350	150	800	2.2	8	
P3403AALxx	P3403AA	300	400	300	400	150	800	2.2	8	
P5103AALxx	P5103AA	420	600	420	600	150	800	2.2	8	
P1553ABLxx	P1553AB	130	180	130	180	150	800	2.2	8	
P1803ABLxx	P1803AB	150	210	150	210	150	800	2.2	8	
P2103ABLxx	P2103AB	170	250	170	250	150	800	2.2	8	

Table continues on next page.

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Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T@I_T= 2.2 Amps	Capacitance
		V min	V max	V min	V max	mA min	mA max	A max	V max	
		Pins 1-2, 3-2		Pins 1-3						
P2353ABLxx	P2353AB	200	270	200	270	150	800	2.2	8	See Capacitance Values table
P2703ABLxx	P2703AB	230	300	230	300	150	800	2.2	8	
P3203ABLxx	P3203AB	270	350	270	350	150	800	2.2	8	
P3403ABLxx	P3403AB	300	400	300	400	150	800	2.2	8	
P5103ABLxx	P5103AB	420	600	420	600	150	800	2.2	8	
P1553ACLxx	P1553AC	130	180	130	180	150	800	2.2	8	
P1803ACLxx	P1803AC	150	210	150	210	150	800	2.2	8	
P2103ACLxx	P2103AC	170	250	170	250	150	800	2.2	8	
P2353ACLxx	P2353AC	200	270	200	270	150	800	2.2	8	
P2703ACLxx	P2703AC	230	300	230	300	150	800	2.2	8	
P3203ACLxx	P3203AC	270	350	270	350	150	800	2.2	8	
P3403ACLxx	P3403AC	300	400	300	400	150	800	2.2	8	
P5103ACLxx	P5103AC	420	600	420	600	150	800	2.2	8	

Notes:
- Absolute maximum ratings measured at T_A= 25°C.
- Components are bi-directional.
- **XX** Part Number Suffix: **'RP'** (Reel Pack), **Blank** (Bulk Pack), or **'60'** (Type 60 lead form, Bulk Pack)

Capacitance Values

Part Number	pF Pin 1-2 / 3-2 Tip-Ground, Ring-Ground		pF Pin 1-3 Tip-Ring	
	MIN	MAX	MIN	MAX
P1553AALxx	10	45	10	30
P1803AALxx	20	40	10	30
P2103AALxx	15	35	10	25
P2353AALxx	15	35	10	25
P2703AALxx	15	35	10	25
P3203AALxx	15	30	10	20
P3403AALxx	15	30	10	20
P5103AALxx	10	60	10	40
P1553ABLxx	25	95	15	60
P1803ABLxx	25	85	15	55
P2103ABLxx	20	85	10	55
P2353ABLxx	20	75	15	50

Part Number	pF Pin 1-2 / 3-2 Tip-Ground, Ring-Ground		pF Pin 1-3 Tip-Ring	
	MIN	MAX	MIN	MAX
P2703ABLxx	20	75	10	50
P3203ABLxx	20	70	10	45
P3403ABLxx	15	65	10	45
P5103ABLxx	15	60	10	40
P1553ACLxx	30	95	20	60
P1803ACLxx	30	85	15	55
P2103ACLxx	30	85	15	55
P2353ACLxx	25	75	15	50
P2703ACLxx	25	75	15	50
P3203ACLxx	25	70	15	45
P3403ACLxx	20	65	15	45
P5103ACLxx	20	60	10	40

Note: Off-state capacitance (C_O) is measured at 1 MHz with a 2 V bias.

Surge Ratings

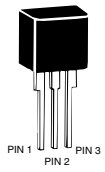
Series	I_{PP} 0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]	I_{TSM} 50/60 Hz	di/dt A
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
A	20	150	150	90	50	75	75	45	75	20	500
B	25	250	250	150	100	100	125	80	100	25	500
C	50	500	400	200	150	200	175	100	200	50	500

Notes:
1 Current waveform in µs
2 Voltage waveform in µs

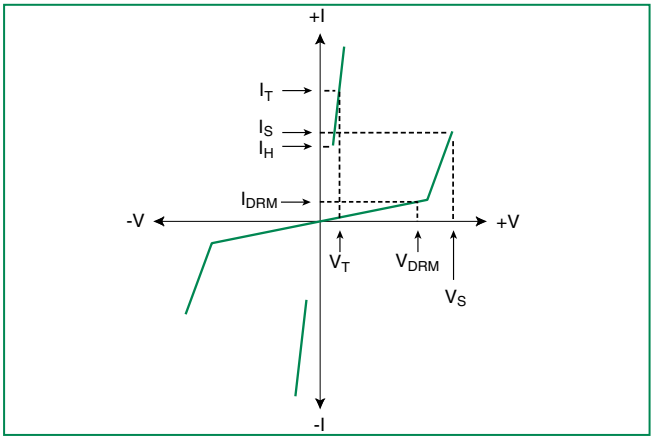
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

Revised: 02/23/17

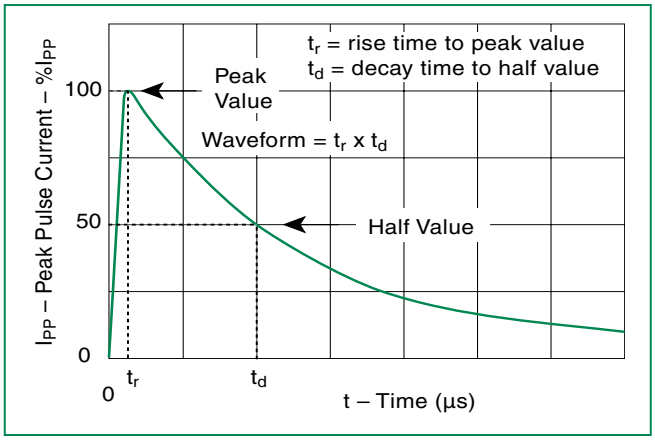
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified TO-220 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	50	°C/W

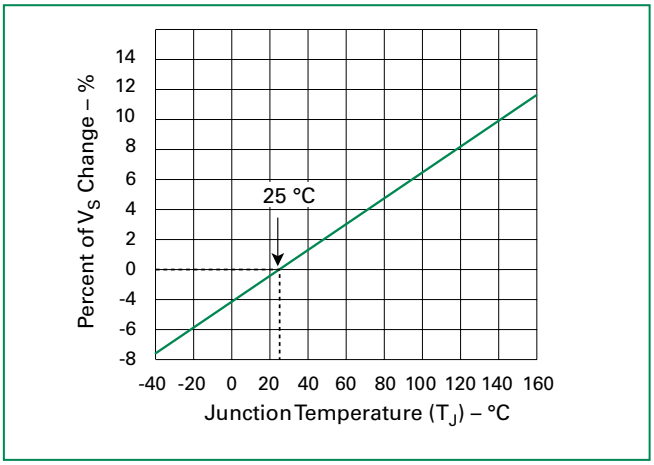
V-I Characteristics



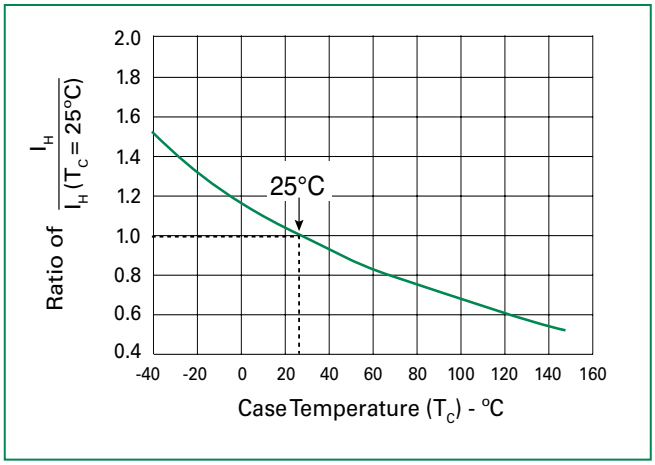
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

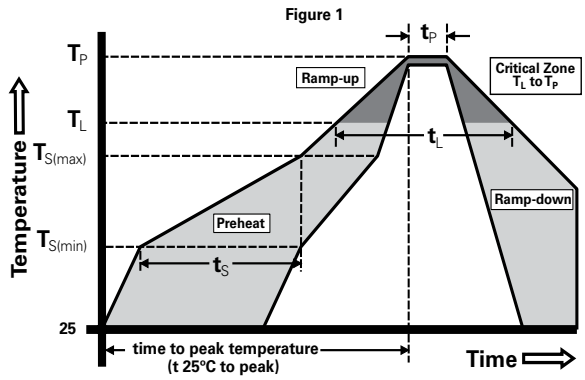


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



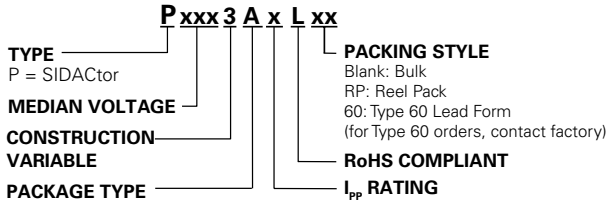
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

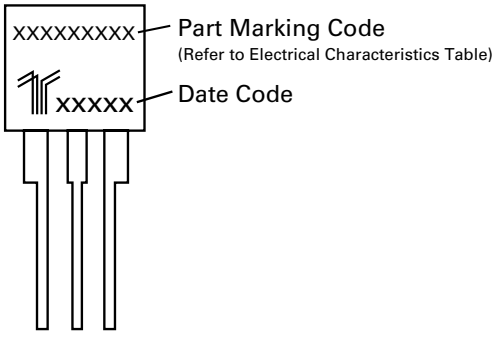
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering



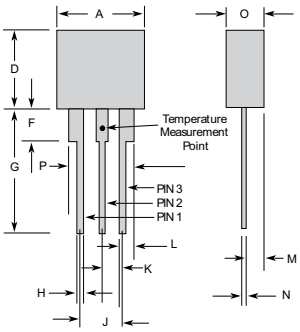
Part Marking



Revised: 02/23/17

SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

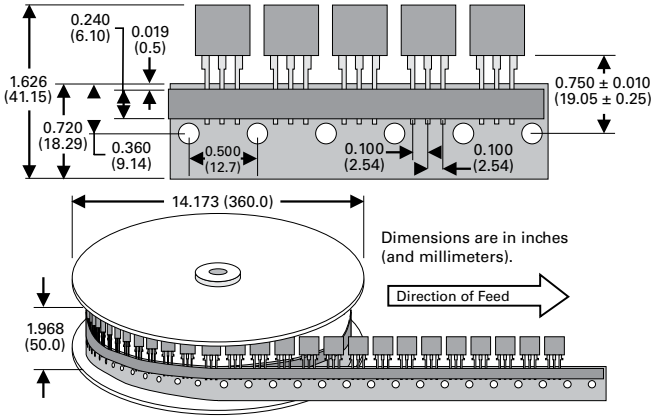
Dimensions - Modified TO-220



The modified TO-220 package is designed to meet mechanical standards as set forth in JEDEC publication number 95.

	Inches		Millimeters	
	Min	Max	Min	Max
A	0.400	0.410	10.16	10.42
D	0.360	0.375	9.14	9.53
F	0.110	0.130	2.80	3.30
G	0.540	0.575	13.71	14.61
H	0.025	0.035	0.63	0.89
J	0.195	0.205	4.95	5.21
K	0.095	0.105	2.41	2.67
L	0.060	0.075	1.52	1.90
M	0.070	0.085	1.78	2.16
N	0.018	0.024	0.46	0.61
O	0.178	0.188	4.52	4.78
P	0.290	0.310	7.37	7.87

Tape and Reel Specification — Modified TO-220



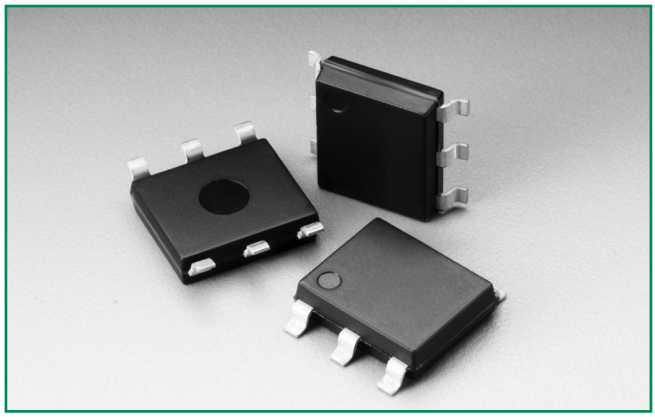
Packing Options

Package Type	Description	Packaging Quantity	Added Suffix	Industry Standard
A	Modified TO-220 Tape and Reel Pack	700	RP	EIA-468-B
	Modified TO-220 Bulk Pack	500	N / A (no suffix required)	EIA-468-B
	Modified TO-220 Type 60 Lead Form Bulk Pack	500	60 (special order item, contact factory for details)	N/A

Additional Information

Datasheet | **Resources** | **Samples**

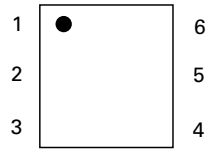
SIDACtor® Balanced Multiport Series - MS-013



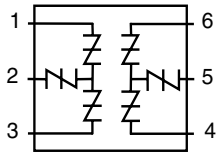
Agency Approvals

Agency	Agency File Number
UL	E133083

Pinout Designation



Schematic Diagram



Description

SIDACtor® Balanced Multiport Series MS-013 are designed to protect baseband equipment from overvoltage transients. The patented "Y" configuration ensures balanced overvoltage protection that prevents longitudinal to differential conversions.

The series provides overvoltage protection that prevents longitudinal to differential conversions.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Low capacitance
- Replaces six discrete devices
- Balanced overvoltage protection
- Meets UL/IEC 60950-1 creepage and clearance
- Two-port protection
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)
- RoHS compliant and lead-free

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Enhanced Level*
- ITU K.20/21/45 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

*A/B-rated parts require series resistance

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_T @I_T=2.2 A	I_H	I_S	I_T	Capacitance
		V min	V max	V min	V max	V max	mA min	mA max	A max	
		Pins 1-2, 3-2, 4-5, 6-5		Pins 1-3, 4-6		Pins 1-2, 3-2, 4-5, 6-5				
A2106UA6Lxx	A2106UA6	170	250	50	80	8	120	800	2.2	See Capacitance Values Table
A5030UA6Lxx	A5030UA6	400	550	270	340	8	150	800	2.2	
A2106UB6Lxx	A2106UB6	170	250	50	80	8	120	800	2.2	
A5030UB6Lxx	A5030UB6	400	550	270	340	8	150	800	2.2	
A2106UC6Lxx	A2106UC6	170	250	50	80	8	120	800	2.2	
A3614UC6Lxx	A3614UC6	333	427	116	154	8	150	800	2.2	
A5030UC6Lxx	A5030UC6	400	550	270	340	8	150	800	2.2	
P1556UALxx	P1556UA	130	180	130	180	8	150	800	2.2	
P1806UALxx	P1806UA	150	210	150	210	8	150	800	2.2	
P2106UALxx	P2106UA	170	250	170	250	8	150	800	2.2	
P2356UALxx	P2356UA	200	270	200	270	8	150	800	2.2	
P2706UALxx	P2706UA	230	300	230	300	8	150	800	2.2	
P3206UALxx	P3206UA	270	350	270	350	8	150	800	2.2	
P3406UALxx	P3406UA	300	400	300	400	8	150	800	2.2	

Table continues on next page.

Revised: 02/23/17

Electrical Characteristics (continued)

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_T @I_T=2.2 A	I_H	I_S	I_T	Capacitance
		V min	V max	V min	V max	V max	mA min	mA max	A max	
		Pins 1-2, 3-2, 4-5, 6-5		Pins 1-3, 4-6		Pins 1-2, 3-2, 4-5, 6-5				
P5106UALxx	P5106UA	420	600	420	600	8	150	800	2.2	See Capacitance Values Table
P1556UBLxx	P1556UB	130	180	130	180	8	150	800	2.2	
P1806UBLxx	P1806UB	150	210	150	210	8	150	800	2.2	
P2106UBLxx	P2106UB	170	250	170	250	8	150	800	2.2	
P2356UBLxx	P2356UB	200	270	200	270	8	150	800	2.2	
P2706UBLxx	P2706UB	230	300	230	300	8	150	800	2.2	
P3206UBLxx	P3206UB	270	350	270	350	8	150	800	2.2	
P3406UBLxx	P3406UB	300	400	300	400	8	150	800	2.2	
P5106UBLxx	P5106UB	420	600	420	600	8	150	800	2.2	
P1556UCLxx	P1556UC	130	180	130	180	8	150	800	2.2	
P1806UCLxx	P1806UC	150	210	150	210	8	150	800	2.2	
P2106UCLxx	P2106UC	170	250	170	250	8	150	800	2.2	
P2356UCLxx	P2356UC	200	270	200	270	8	150	800	2.2	
P2706UCLxx	P2706UC	230	300	230	300	8	150	800	2.2	
P3206UCLxx	P3206UC	270	350	270	350	8	150	800	2.2	
P3406UCLxx	P3406UC	300	400	300	400	8	150	800	2.2	
P5106UCLxx	P5106UC	420	600	420	600	8	150	800	2.2	

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional (some are asymmetrical).
- XX = Part Number Suffix: 'TP' (Tube Pack) or 'RP' (Reel Pack).

Surge Ratings

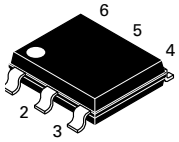
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
A	20	150	150	90	50	75	75	45	75	20	500
B	25	250	250	150	100	100	125	80	100	25	500
C	50	500	400	200	150	200	175	100	200	30	500

Notes:

1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40 to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified MS-013 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

Revised: 02/23/17

Capacitance Values

Part Number	pF Pin 1-2 / 3-2 (4-5 / 6-5) Tip-Ground, Ring-Ground		pF Pin 1-3 (4-6) Tip-Ring	
	MIN	MAX	MIN	MAX
A2106UA6Lxx	20	60	10	30
A5030UA6Lxx	15	35	10	45
A2106UB6Lxx	20	60	10	30
A5030UB6Lxx	15	35	10	45
A2106UC6Lxx	20	70	10	45
A3614UC6Lxx	25	40	25	35
A5030UC6Lxx	25	40	20	35
P1556UALxx	20	45	10	30
P1806UALxx	20	40	10	30
P2106UALxx	15	35	10	25
P2356UALxx	15	35	10	25
P2706UALxx	15	35	10	25
P3206UALxx	15	30	10	20
P3406UALxx	15	30	10	20
P5106UALxx	10	20	5	15
P1556UBLxx	20	45	10	30
P1806UBLxx	20	40	10	30
P2106UBLxx	15	35	10	25
P2356UBLxx	15	35	10	25
P2706UBLxx	15	35	10	25
P3206UBLxx	15	30	10	20
P3406UBLxx	15	30	10	20
P5106UBLxx	10	20	5	15
P1556UCLxx	30	55	20	35
P1806UCLxx	30	50	15	35
P2106UCLxx	30	45	15	30
P2356UCLxx	25	40	15	30
P2706UCLxx	25	40	15	30
P3206UCLxx	20	35	15	25
P3406UCLxx	20	35	15	25
P5106UCLxx	20	30	10	20

Note: Off-state capacitance (C_O) is measured at 1 MHz with a 2 V bias.

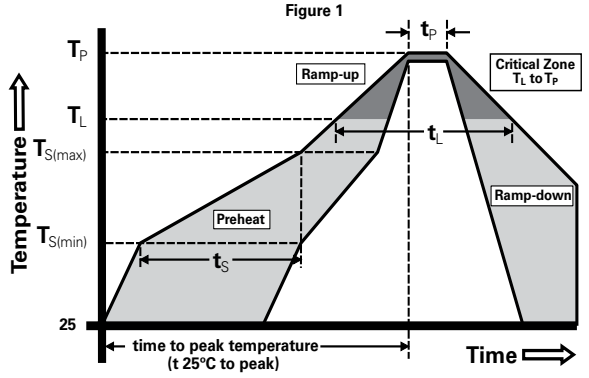
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Environmental Specifications

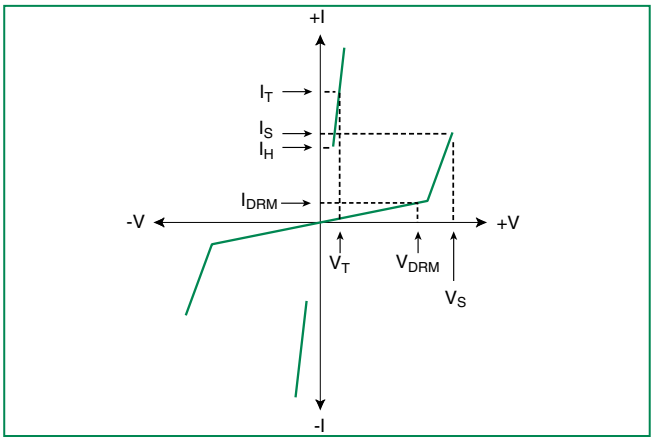
High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Revised: 02/23/17

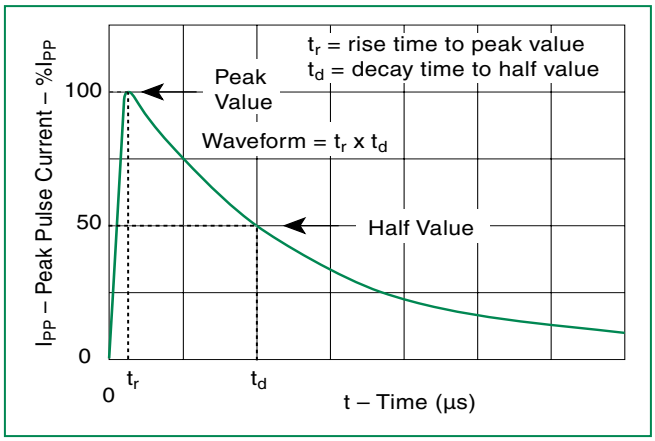
Littelfuse
Expertise Applied | Answers Delivered

SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

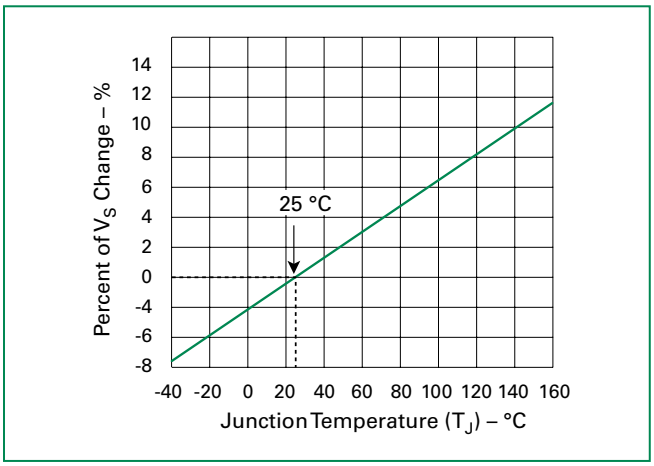
V-I Characteristics



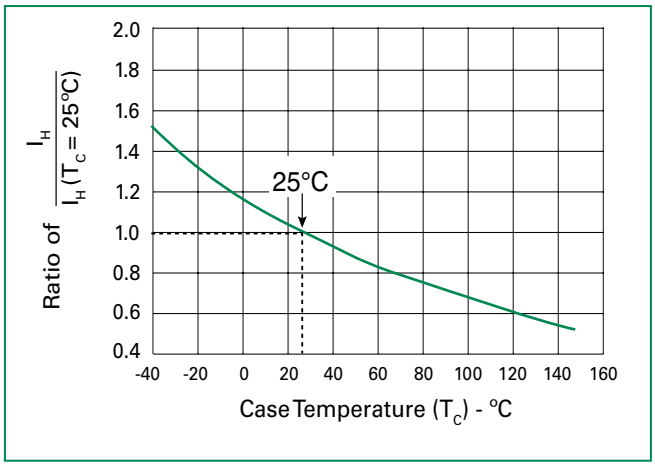
t_r x t_d Pulse Waveform



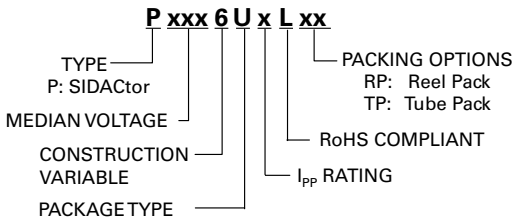
Normalized V_S Change vs. Junction Temperature

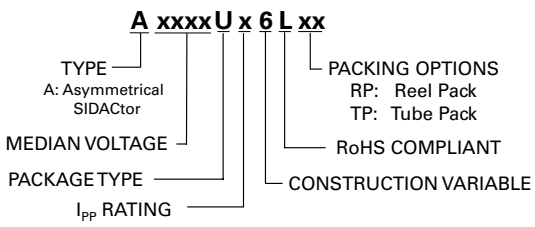


Normalized DC Holding Current vs. Case Temperature

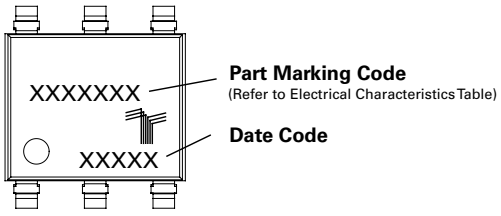


Part Numbering





Part Marking

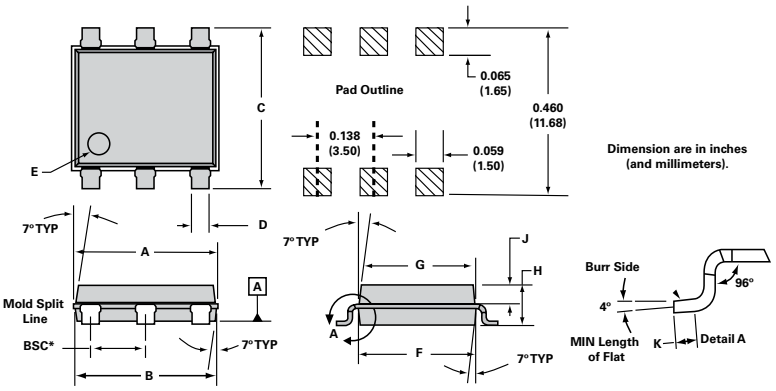


Additional Information

Datasheet | **Resources** | **Samples**

Revised: 02/23/17

Dimensions — MS-013



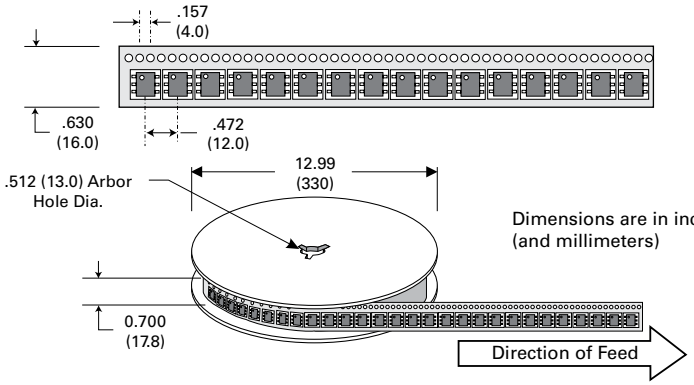
Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.360	0.364	9.14	9.25
B	0.352	0.356	8.94	9.04
C	0.400	0.412	10.16	10.46
D	0.043	0.045	1.09	1.13
E	0.047	0.055	1.19	1.40
F	0.293	0.297	7.44	7.54
G	0.289	0.293	7.34	7.44
H	0.089	0.093	2.26	2.36
J	0.041	0.049	1.04	1.24
K	0.020		0.51	
BSC*	0.133	0.143	3.38	3.63

* BSC = **B**asic **S**pacing between **C**enters

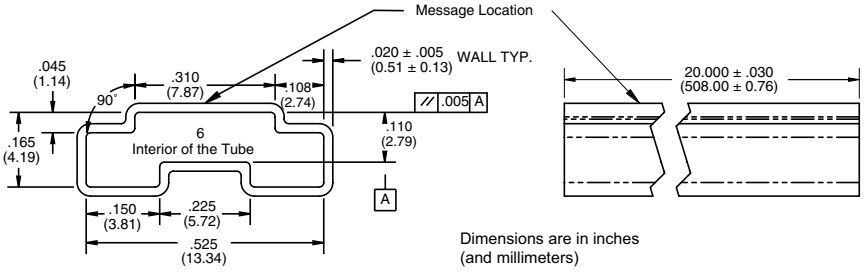
Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
U	Modified MS-013 6-pin Tape and Reel Pack	1500	RP	EIA-481-D
	Modified MS-013 6-pin Tube Pack	500 (50 per tube)	TP	N/A

Tape and Reel Specification — MS-013

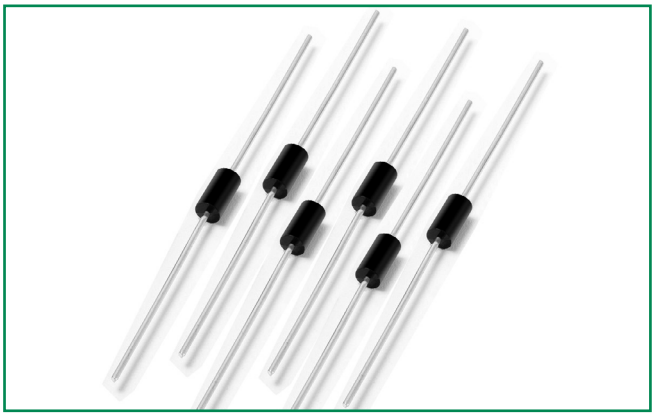


Tube Pack Specification — MS-013



SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

T10A Series - DO-15



Agency Approvals

Agency	Agency File Number
	E128662 (68V-270V)

Pinout Designation

Not Applicable

Schematic Symbol

Description

T10A Series are SIDACtor® thyristors designed to protect baseband equipment such as modems, line cards, CPE and DSL from damaging overvoltage transients.

The series provides a cost effective through-hole solution that enables equipment to comply with global regulatory standards.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- RoHS Compliant
- Fails short circuit when surged in excess of ratings
- Low capacitance
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Enhanced Level*
- ITU K.20/21/45 Basic Level
- GR 1089 Inter-building*
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

*A-rated parts require series resistance

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amp	Capacitance @ 1MHz, 2V Bias
		V Min	V Max	mA Min	mA Max	A Max	V Max	pF Typ
T10A060Bxx	T10A060B	50	84	120	800	2.2	4	50
T10A060Exx	T10A060E	50	84	180	800	2.2	4	50
T10A062xx	T10A062	56	86	150	800	2.2	4	50
T10A068xx	T10A068	61	94	150	800	2.2	4	50
T10A080Bxx	T10A080B	70	125	120	800	2.2	4	43
T10A080Exx	T10A080E	70	125	180	800	2.2	4	43
T10A100xx	T10A100	90	140	150	800	2.2	4	43
T10A110Bxx	T10A110B	100	142	120	800	2.2	4	38
T10A110Exx	T10A110E	100	142	180	800	2.2	4	38
T10A120xx	T10A120	108	168	150	800	2.2	4	38
T10A130xx	T10A130	117	178	150	800	2.2	4	38
T10A140Bxx	T10A140B	120	178	120	800	2.2	4	34
T10A140Exx	T10A140E	120	178	180	800	2.2	4	34
T10A180xx	T10A180	170	220	150	800	2.2	4	34
T10A180Bxx	T10A180B	170	220	120	800	2.2	4	32
T10A180Exx	T10A180E	170	220	180	800	2.2	4	32
T10A200xx	T10A200	180	275	150	800	2.2	4	30
T10A220xx	T10A220	200	275	150	800	2.2	4	30

Table continues on next page.

Revised: 02/23/17

Electrical Characteristics (continued)

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amp	Capacitance @ 1MHz, 2V Bias
		V Min	V Max	mA Min	mA Max	A Max	V Max	pF Typ
T10A220Bxx	T10A220B	200	275	120	800	2.2	4	30
T10A220Exx	T10A220E	200	275	180	800	2.2	4	30
T10A240xx	T10A240	216	330	150	800	2.2	4	30
T10A270xx	T10A270	245	370	150	800	2.2	4	30
T10A270Bxx	T10A270B	245	370	120	800	2.2	4	30
T10A270Exx	T10A270E	245	370	180	800	2.2	4	30

Notes:

- Absolute maximum ratings measured at T_A= 25°C.
- Components are bi-directional (unless otherwise noted).
- **XX** Part Number Suffix: "**RP**" (Reel Pack) or **Blank** (Bulk Pack)

Surge Ratings

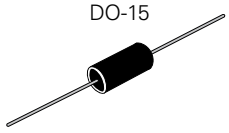
Series	I_{PP}			I_{TSM} 50/60 Hz	di/dt
	8/20[1] 1.2/50[2]	5/310[1] 10/700[2]	10/1000[1] 10/1000[2]		
	A min	A min	A min	A min	A/µs max
A	100	37.5	50	20	100

Notes:

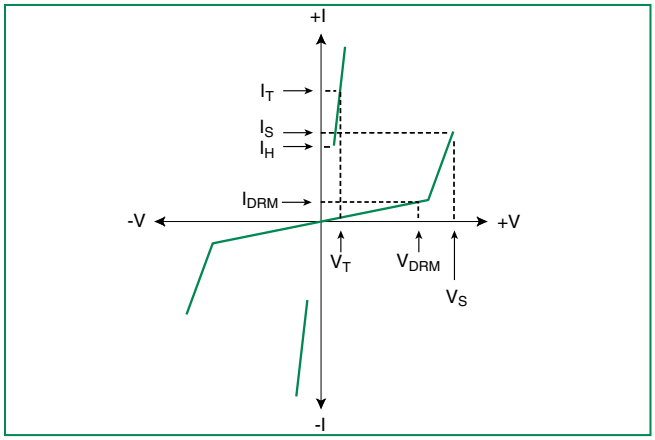
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed of the product in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

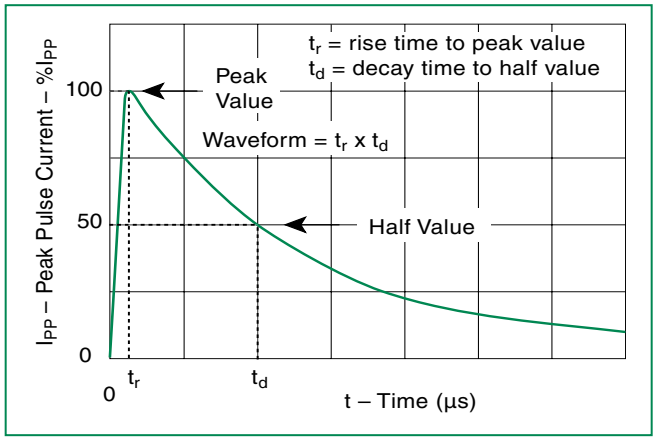
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
DO-15 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	120	°C/W

V-I Characteristics



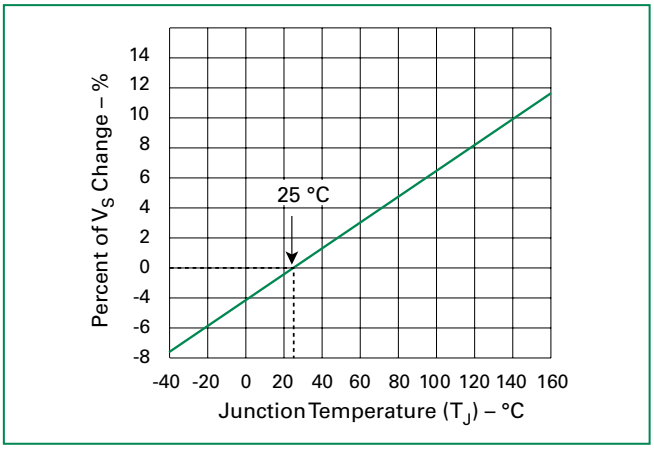
t_r x t_d Pulse Waveform



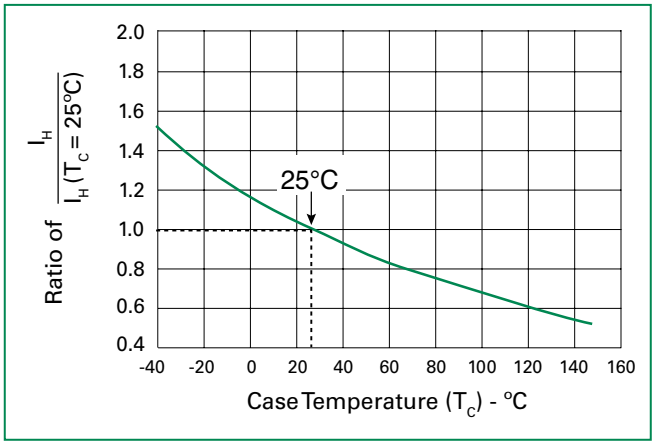
Revised: 02/23/17

SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

Normalized V_S Change vs. Junction Temperature



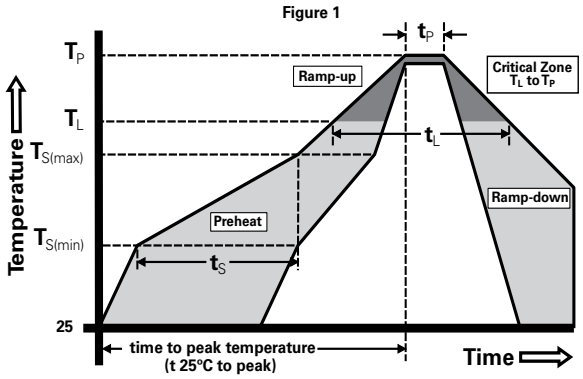
Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Revised: 02/23/17

Part Numbering

T10A xxx x xx

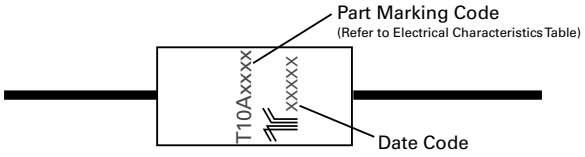
TYPE
T10A = SIDACtor T10A series

MEDIAN VOLTAGE

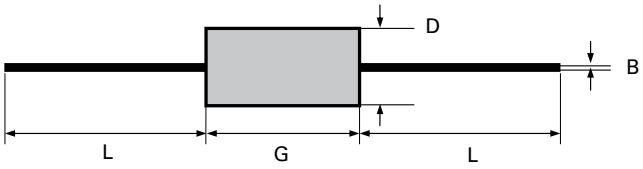
PACKING OPTIONS
Blank: Bulk
RP: Reel Pack

HOLDING CURRENT:
Blank: 150mA
B: 120mA
E: 180mA

Part Marking



Dimensions — DO-15

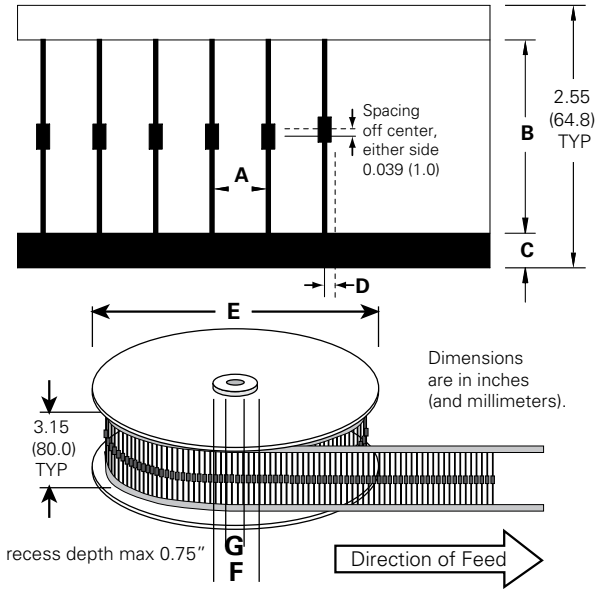


Dimension	Inches		Millimeters	
	MIN	MAX	MIN	MAX
B	0.028	0.034	0.711	0.864
D	0.12	0.14	3.048	3.556
G	0.235	0.27	5.969	6.858
L	1		25.4	

Packing Options

Package Type	Description	Packaging Quantity	Added Suffix	Industry Standard
T10A	DO-15 Tape and Reel Pack	1000	RP	EIA-RS-296-D
	DO-15 Bulk Pack	500	N/A	N/A

Tape and Reel Specification — DO-15



Symbols	Description	Inches	MM
A	Component Spacing (lead to lead)	0.200 ± 0.020"	5.08 ± 0.508
B	Inner Tape Pitch	2.062 ± 0.059"	52.37 ± 1.498
C	Tape Width	0.250"	6.35
D	Max. Off Alignment	0.048"	1.219
E	Reel Dimension	13"	330.2
F	Max. Hub Recess	3"	76.19
G	Max. Abor Hole	0.68"	17.27

Additional Information

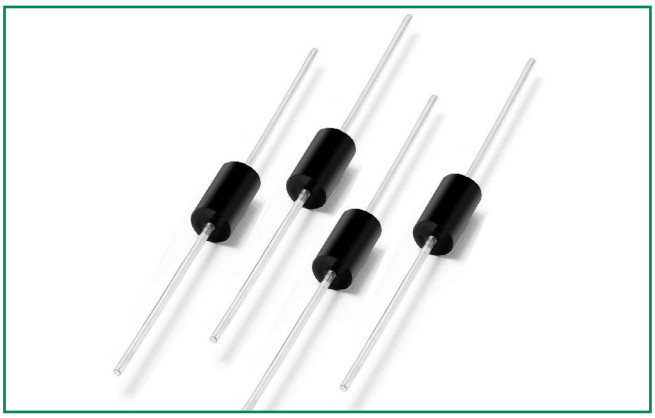
Datasheet | **Resources** | **Samples**

Revised: 02/23/17

Littelfuse
Expertise Applied | Answers Delivered

SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

T10B Series - DO-201



Agency Approvals

Agency	Agency File Number
	E128662

Pinout Designation

Not Applicable

Schematic Symbol

Description

T10B Series are SIDACtor® thyristors designed to protect baseband equipment such as modems, line cards, CPE and DSL from damaging overvoltage transients.

The series provides a robust and cost effective through-hole solution that enables equipment to comply with global regulatory standards

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- High Surge Current Rating
- RoHS Compliant
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Enhanced Level
- ITU K.20/21/45 Basic Level
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 Amp	Capacitance @1MHZ, 2V Bias
		V Min	V Max	mA Min	mA Max	A Max	V Max	pF
T10B080Bxx	T10B080B	70	125	120	800	2.2	4	60
T10B110Bxx	T10B110B	100	142	120	800	2.2	4	55
T10B140Bxx	T10B140B	120	178	120	800	2.2	4	48
T10B180Bxx	T10B180B	170	220	120	800	2.2	4	44
T10B220Bxx	T10B220B	200	275	120	800	2.2	4	41
T10B270Bxx	T10B270B	240	370	120	800	2.2	4	36
T10B080Exx	T10B080E	70	125	180	800	2.2	4	60
T10B110Exx	T10B110E	100	142	180	800	2.2	4	55
T10B140Exx	T10B140E	120	178	180	800	2.2	4	48
T10B180Exx	T10B180E	170	220	180	800	2.2	4	44
T10B220Exx	T10B220E	200	275	180	800	2.2	4	41
T10B270Exx	T10B270E	240	370	180	800	2.2	4	36

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional.
- **XX** Part Number Suffix: **'RP'** (Reel Pack), **Blank** (Bulk Pack), or **'60'** (Type 60 lead form, Bulk Pack)

Revised: 02/23/17

Surge Ratings

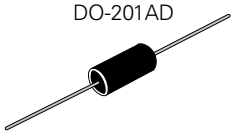
Series	I_{PP}			I_{TSM} 50/60 Hz	di/dt
	8/20[1] 1.2/50[2]	5/310[1] 10/700[2]	10/1000[1] 10/1000[2]		
	A min	A min	A min	A min	A/µs max
B	250	125	100	30	500

Notes:

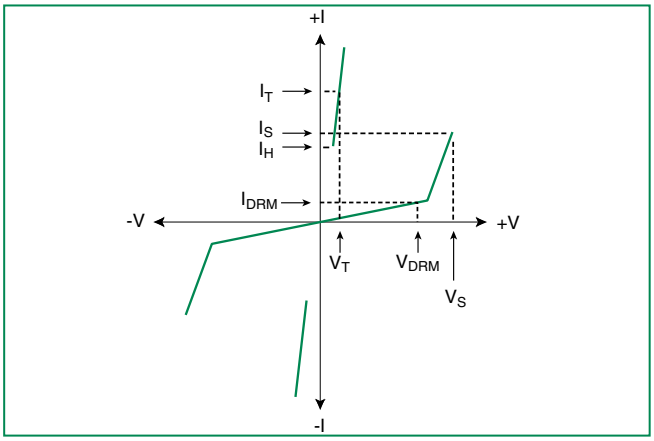
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

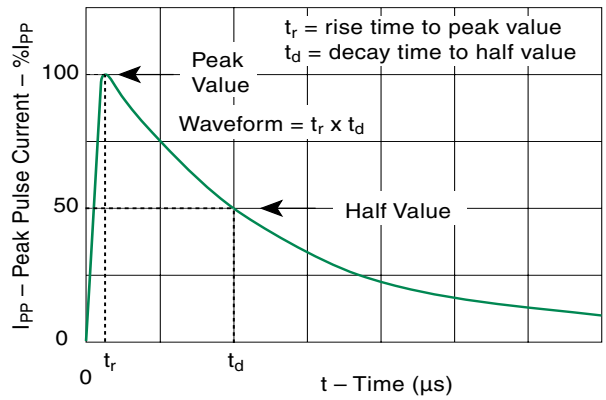
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
DO-201AD 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	120	°C/W

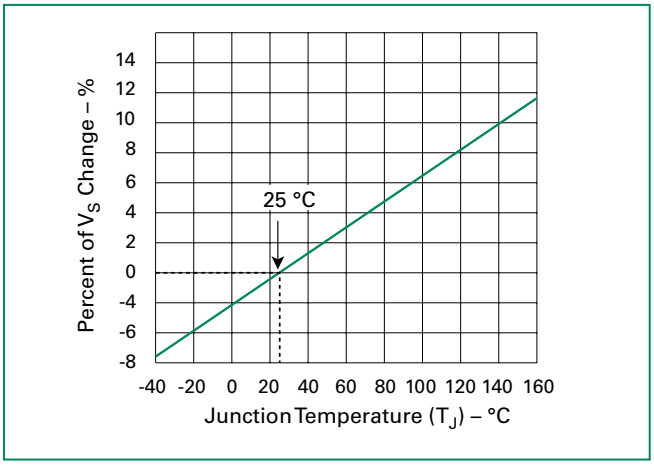
V-I Characteristics



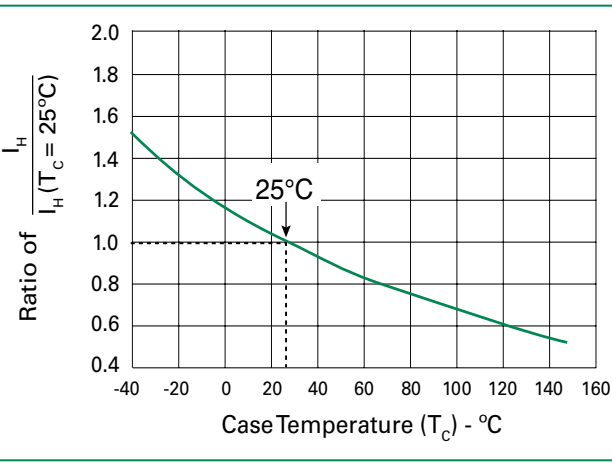
t_r x t_d Pulse Waveform



Normalized V_s Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

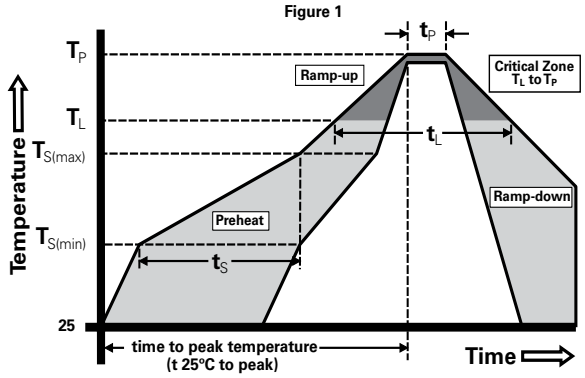


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Revised: 02/23/17

SIDACtor® Protection Thyristors
Baseband Protection (Voice-DS1)

Littelfuse
Expertise Applied | Answers Delivered

Part Numbering

T10B xxx x xx

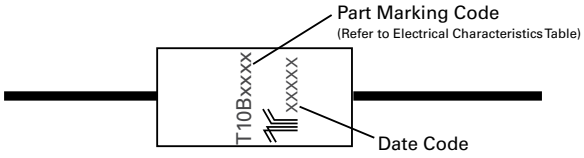
TYPE
T10B: SIDACtor T10B series

MEDIAN VOLTAGE

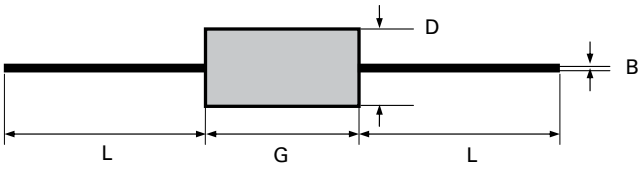
PACKING OPTIONS
Blank: Bulk Pack
RP: Reel Pack

HOLDING CURRENT
B: 120mA
E: 180mA

Part Marking



Dimensions — DO-201AD

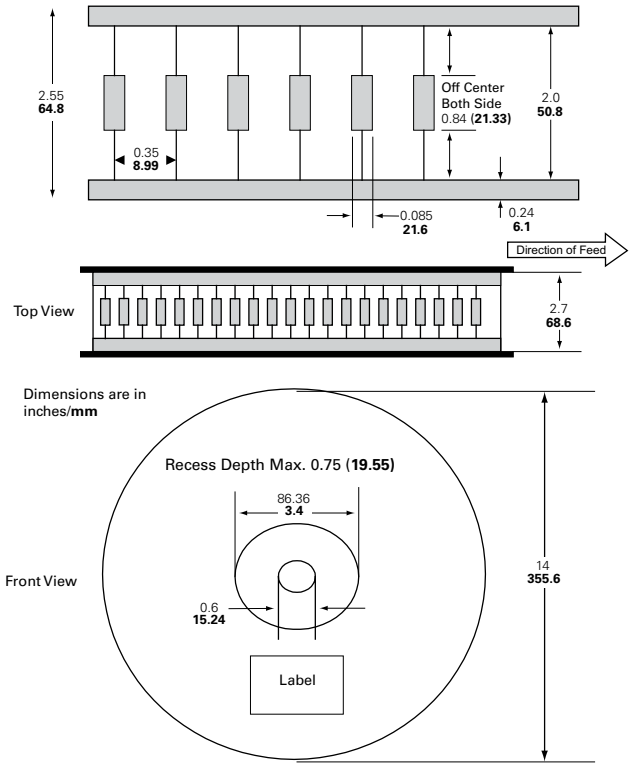


Dimension	Inches		Millimeters	
	MIN	MAX	MIN	MAX
B	0.028	0.042	0.711	1.067
D	0.190	0.205	4.826	5.207
G	0.360	0.375	9.146	9.527
L	1		25.4	

Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
T10B	DO-201AD Tape and Reel Pack	1000	RP	EIA-RS-296-D
	DO-201AD Bulk Pack	500	N/A	N/A

Tape and Reel Specification — DO-201AD



Additional Information

Datasheet | **Resources** | **Samples**

Revised: 02/23/17

Littelfuse
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SIDACtor® Protection Thyristors
High Surge Current Protection

High Surge Current Series - DO-214

Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation

Not Applicable

Schematic Symbol

Description

The High Surge Current DO-214 Series are SIDACtor® thyristors designed to protect equipment located in hostile environments from overvoltage transients.

The series provides a 200A 10/1000 µs rated surface mount solution that enables equipment to comply with enhanced surge requirments now specified in regulatory and customer requirements.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- 200A 10x1000 Surge Rating
- 1000A 2x10 Surge Rating
- RoHS Compliant and Halogen-Free
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/45 Enhanced Level
- ITU K.20/21/45 Basic Level
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-5 2nd edition
- YD/T 1082
- YD/T 993
- YD/T 950

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_{T**}	V_T @I_T=2.2A	Capacitance @1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pf min	pF max
P0080SDLRP	P-8D	6	25	50	800	2.2	4	50	150
P0640SDLRP	P06D	58	77	50	800	2.2	4	100	160
P0720SDLRP	P07D	65	88	50	800	2.2	4	100	150
P0900SDLRP	P09D	75	98	50	800	2.2	4	95	140
P1100SDLRP	P11D	90	130	50	800	2.2	4	75	115
P1300SDLRP	P13D	120	160	50	800	2.2	4	65	100
P1500SDLRP	P15D	140	180	50	800	2.2	4	60	90
P1800SDLRP	P18D	170	220	50	800	2.2	4	50	90
P2300SDLRP	P23D	190	260	50	800	2.2	4	50	80
P2600SDLRP	P26D	220	300	50	800	2.2	4	50	75
P3100SDLRP	P31D	275	350	50	800	2.2	4	45	70
P3500SDLRP	P35D	320	400	50	800	2.2	4	45	65

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bi-directional (unless otherwise noted).
** Will meet 4.4A power cross requirement without fire hazard.

Revised: 02/23/17

Surge Ratings

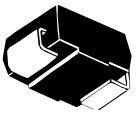
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
D	—	1000	800	—	—	—	—	200	350	50	1000

Notes:

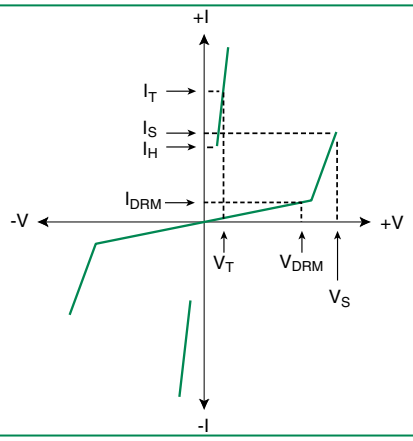
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product that remains in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

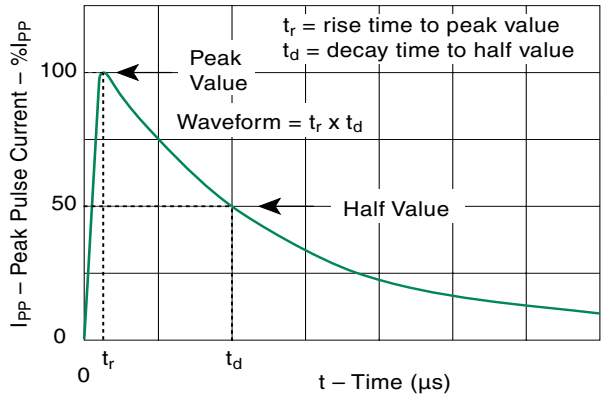
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
DO-214AA 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	90	°C/W

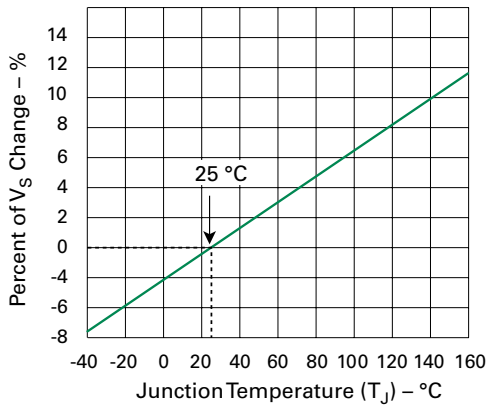
V-I Characteristics



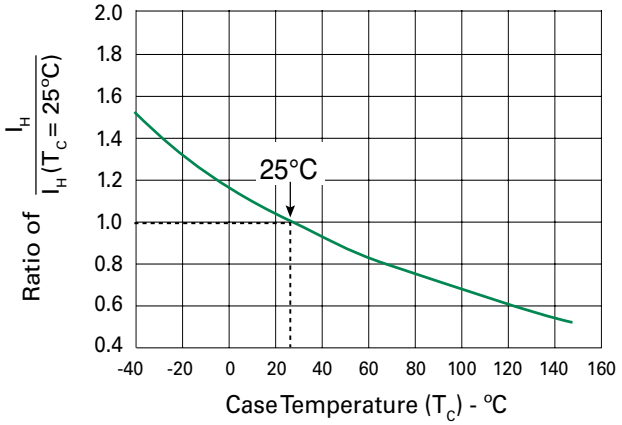
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature

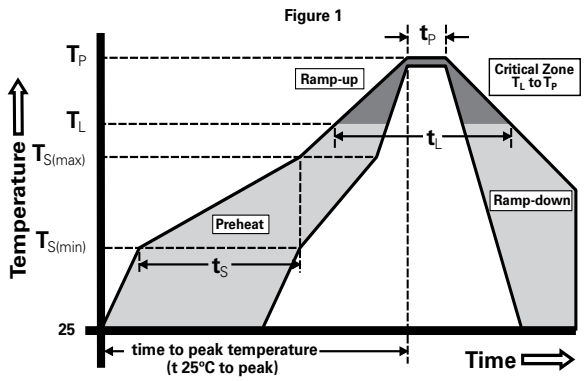


Revised: 02/23/17

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



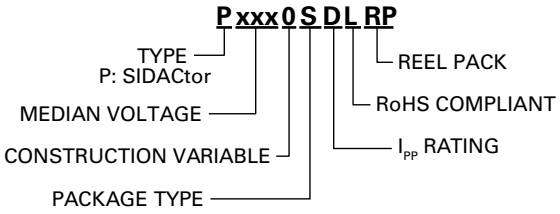
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0 per Underwriters Laboratories

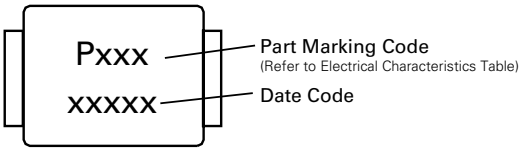
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering

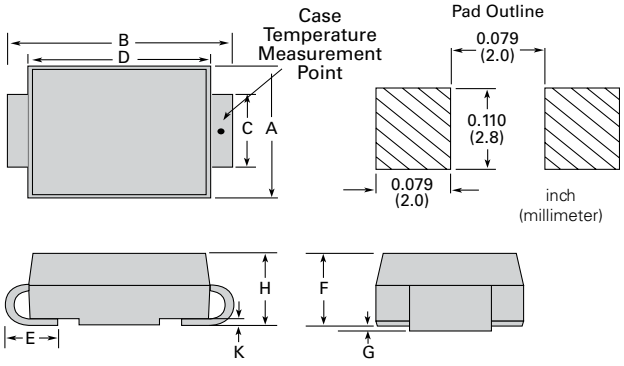


Part Marking



Revised: 02/23/17

Dimensions — DO-214AA

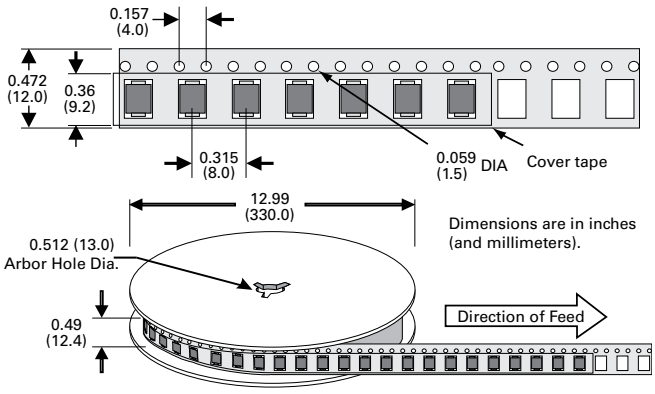


Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.130	0.156	3.30	3.95
B	0.201	0.220	5.10	5.60
C	0.077	0.087	1.95	2.20
D	0.159	0.181	4.05	4.60
E	0.030	0.063	0.75	1.60
F	0.075	0.096	1.90	2.45
G	0.002	0.008	0.05	0.20
H	0.077	0.104	1.95	2.65
K	0.006	0.016	0.15	0.41

Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
S	DO-214AA Tape and Reel Pack	2500	RP	EIA-481-D

Tape and Reel Specification — DO-214AA



Additional Information

Datasheet | **Resources** | **Samples**

Revised: 02/23/17

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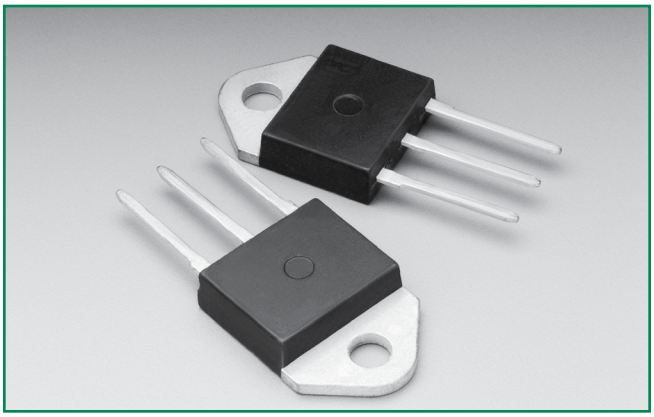
SIDACtor® Protection Thyristors
High Surge Current Protection

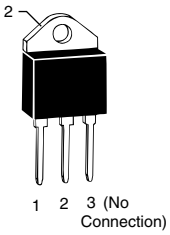
5kA Series - TO-218



Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol

Description

The 5kA Series are SIDACtor® components designed to protect equipment located in high exposure environments from severe overvoltage transients.

Packaged in a robust TO-218 package, the 5kA Series is ideal for use in data interface and AC power line for CATV amplifiers, Telecom Base Station equipment and Cell Towers.

Features and Benefits

- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of rating
- Rugged TO-218 package
- 5000A 8/20 µs surge rating
- 2nd level interconnect is Pb-free per IPC/JEDEC J-STD-609A
- RoHS compliant, lead-free and halogen-free

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21/.45 Enhanced Level
- ITU K.20/21/.45 Basic Level
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-5
- YD/T 1082
- YD/T 993
- YD/T 950

Additional Information

Datasheet | **Resources** | **Samples**

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H	I_S	I_T	V_T @I_T=2.2 A	Capacitance @1MHz, 2V bias	
		V min	V max	mA min	mA max	A max	V max	pF min	pF max
P1500MEL	P1500ME	140	180	50	800	2.2/25	4	400	650
P1900MEL	P1900ME	155	220	50	800	2.2/25	4	400	650
P2300MEL	P2300ME	180	260	50	800	2.2/25	4	350	600
P3800MEL	P3800ME	350	430	50	800	2.2/25	4	300	500

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Devices are bi-directional (unless otherwise noted).
- I_T is a free air rating and heat sink is at 25A

Revised: 02/23/17

Surge Ratings

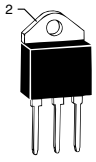
Series	I_{PP} 8/20[1] 1.2/50[2] A min	I_{TSM} 50 / 60 Hz A min	di/dt A/µs max
E	5000[3]	400	630

Notes:

1 Current waveform in µs
2 Voltage waveform in µs
3. For surge rating of P3800MEL, it is minimum 4kA and typical 5kA @8/20µs.

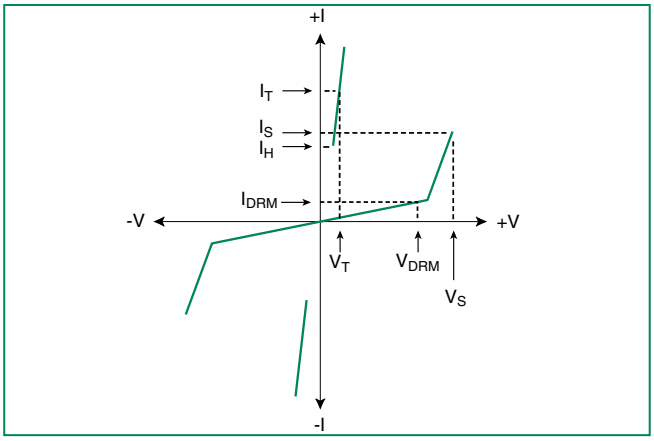
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The device must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

Thermal Conditions

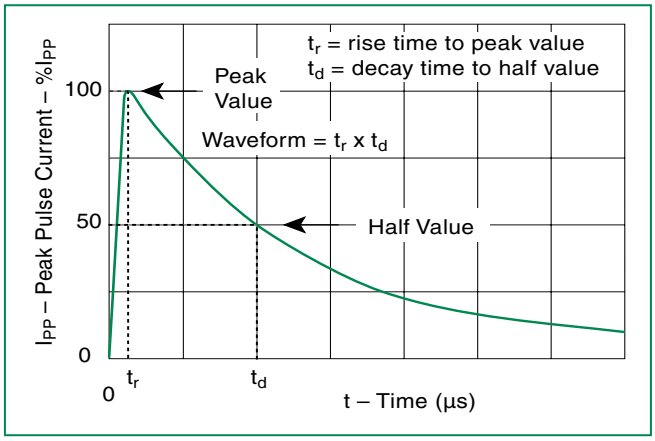
Package	Symbol	Parameter	Value	Unit
TO-218 	$T_{JØ}$	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	T_C	Maximum Case Temperature	100	°C
	$R_{\theta JC}$*	Thermal Resistance: Junction to Case	1.7	°C/W
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	56	°C/W

*$R_{\theta JC}$ rating assumes the use of a heat sink and on state mode for extended time at 25 A, with average power dissipation of 29 W.

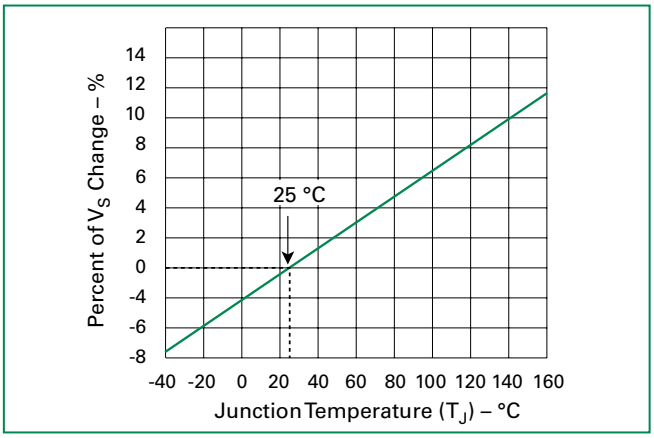
V-I Characteristics



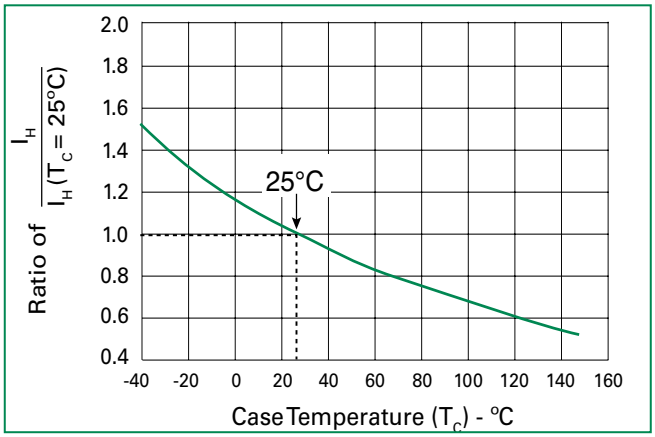
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature



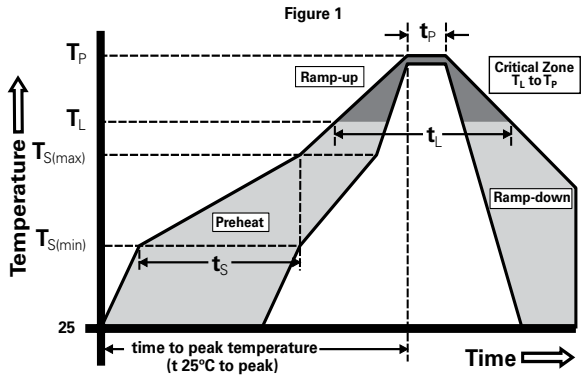
Revised: 02/23/17

SIDACtor® Protection Thyristors
High Surge Current Protection

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



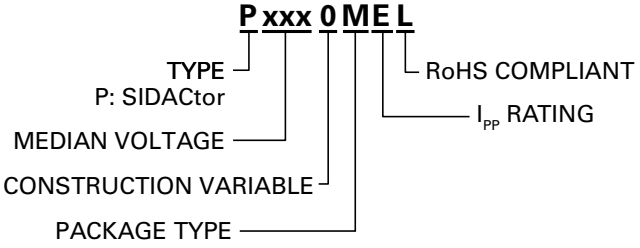
Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification V-0

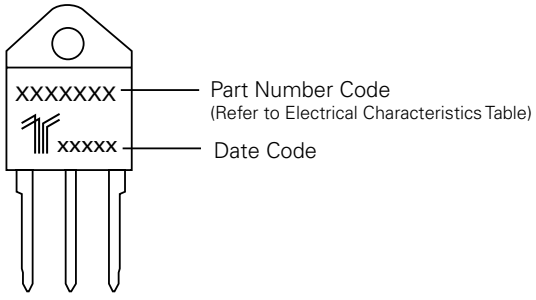
Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering

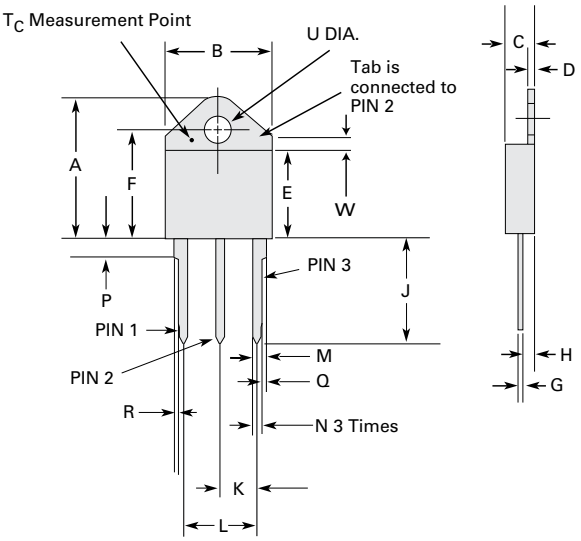


Part Marking



Revised: 02/23/17

Dimensions — TO-218



Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.810	0.835	20.57	21.21
B	0.610	0.630	15.49	16.00
C	0.178	0.188	4.52	4.78
D	0.055	0.070	1.40	1.78
E	0.487	0.497	12.37	12.62
F	0.635	0.655	16.13	16.64
G	0.022	0.029	0.56	0.74
H	0.075	0.095	1.91	2.41
J	0.575	0.625	14.61	15.88
K	0.211	0.219	5.36	5.56
L	0.422	0.437	10.72	11.10
M	0.058	0.068	1,47	6.73
N	0.045	0.055	1.14	1.40
P	0.095	0.115	2.41	2.92
R	0.008	0.016	0.20	0.41
U	0.161	0.165	4.1	4.2
W	0.085	0.095	2.17	2.42

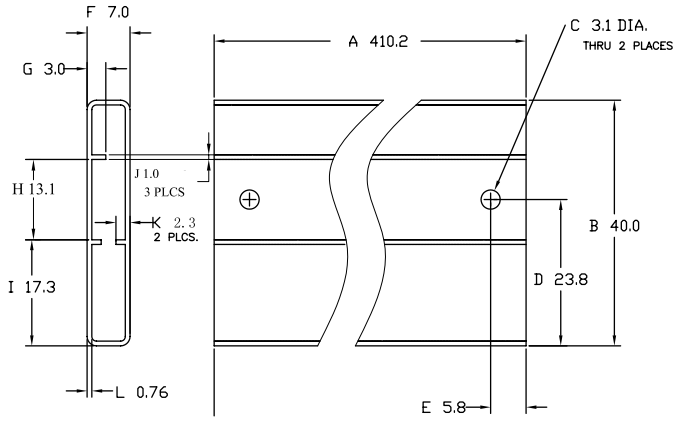
Notes:

- Mold flash shall not exceed 0.13 mm per side.
- Maximum torque to be applied to mounting tab is 8 in-lbs. (0.904 Nm).
- Pin 3 has no connection.
- Tab is non-isolated (connects to middle pin).

Packing Options

Package Type	Description	Packing Options Quantity	Added Suffix	Industry Standard
M	TO-218 (ME) Tube Pack	250(25 per tube/10 tubes per box)	N/A	N/A

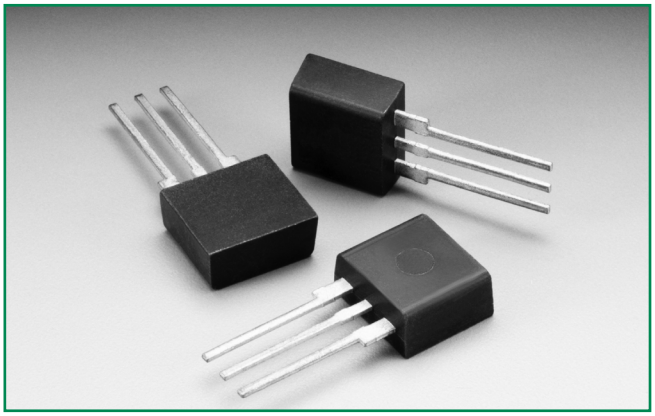
Tube Pack Specification — TO-218



Littelfuse
Expertise Applied | Answers Delivered

SIDACtor® Protection Thyristors
High Surge Current Protection

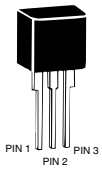
SIDACtor® Primary Protection Series - Modified TO-220



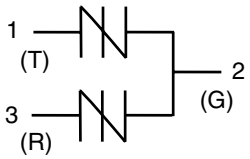
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Description

The SIDACtor® Primary Protection Series Modified TO-220 thyristors are components designed for use in primary protection applications.

The series provides a single port overvoltage solution that enables applications to comply with GR-974 and a range of other global regulatory standards. Please contact Littelfuse to discuss your particular application and regulatory requirements.

Features and Benefits

- High holding current options available
- Failsafe option available
- Low voltage overshoot when surged in excess of ratings
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- RoHS Compliant and Halogen-Free
- Fails short circuit
- Single-port protection
- Modified TO-220 Package
- Lead forms available
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- GR-974
- UL 497
- ITU K.28

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	V_T @I_T=2.2 A	I_H*	I_S	I_T	Capacitance @1MHz, 2V bias	
		V min	V max	V min	V max	V max	mA min	mA max	A max	pF min	pF max
		Pins 1-2, 3-2		Pins 1-3		Pins 1-2, 3-2					
P0602ACLxx	P0602AC	25	40	50	80	4	50	800	2.2	See Capacitance Values Table	
P1402ACLxx	P1402AC	58	77	116	154	4	150	800	2.2		
P1602ACLxx	P1602AC	65	95	130	190	4	150	800	2.2		
P2202ACLxx	P2202AC	90	130	180	260	4	150	800	2.2		
P2702ACLxx	P2702AC	120	160	240	320	4	150	800	2.2		
P3002ACLxx	P3002AC	140	180	280	360	4	150	800	2.2		
P3602ACLxx	P3602AC	170	220	340	440	4	150	800	2.2		
P4202ACLxx	P4202AC	190	250	380	500	4	150	800	2.2		
P4802ACLxx	P4802AC	220	300	440	600	4	150	800	2.2		
P6002ACLxx	P6002AC	275	350	550	700	4	150	800	2.2		

Notes:
* Higher holding current available by special order. Contact Littelfuse for additional information.
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Devices are bi-directional (unless otherwise noted).
- **xx** Part Number Suffix: **'RP'** (Reel pack), **Blank** (Bulk pack), **'60'** (Type 60 lead form bulk pack), **'FS1'** (Failsafe option bulk pack). Refer to Part Numbering section for additional details.

Revised: 02/23/17

Surge Ratings

Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2x310 [1] 0.5x700 [2]	2x10 [1] 2x10 [2]	8x20 [1] 1.2x50 [2]	10x160 [1] 10x160 [2]	10x560 [1] 10x560 [2]	5x320 [1] 9x720 [2]	10x360 [1] 10x360 [2]	10x1000 [1] 10x1000 [2]	5x310 [1] 10x700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs min
C	50	500	400	200	150	200	175	100	200	50	500

Notes:

1 Current waveform in µs
2 Voltage waveform in µs

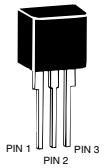
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The device must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

Capacitance Values

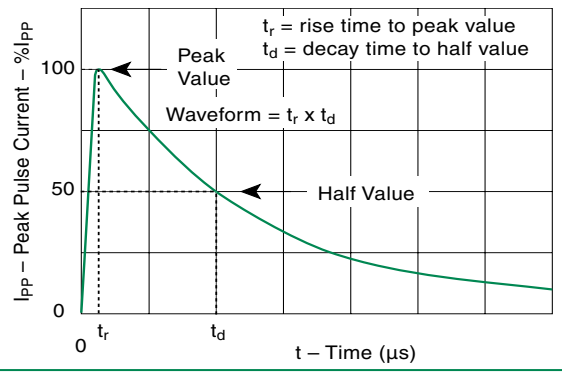
Part Number	Pin 1-2 / 3-2 Tip-Ground, Ring-Ground		Pin 1-3 Tip-Ring	
	pF min	pF max	pF min	pF max
P0602ACLxx	35	65	20	40
P1402ACLxx	105	155	60	90
P1602ACLxx	95	145	50	85
P2202ACLxx	75	115	40	65
P2702ACLxx	70	105	40	60
P3002ACLxx	65	95	35	55
P3602ACLxx	65	90	35	50
P4202ACLxx	60	85	35	50
P4802ACLxx	60	85	30	50
P6002ACLxx	55	80	30	45

Note: Off-state capacitance (C_O) is measured at 1 MHz with a 2 V bias.

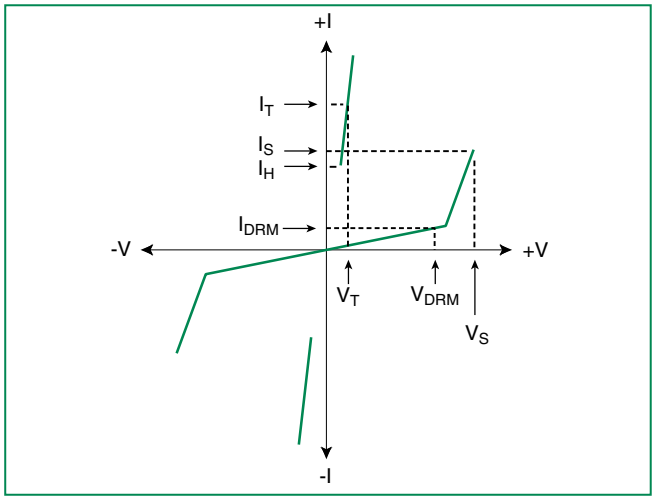
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified TO-220 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	60	°C/W

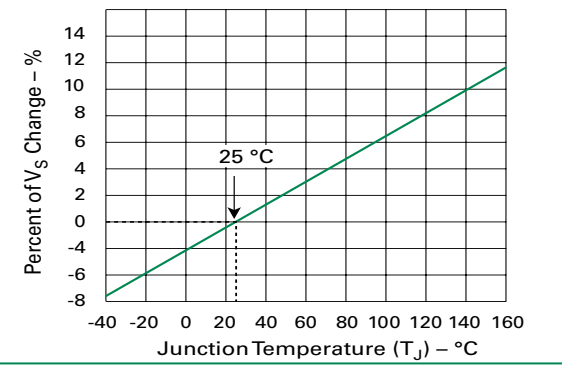
t_r x t_d Pulse Waveform



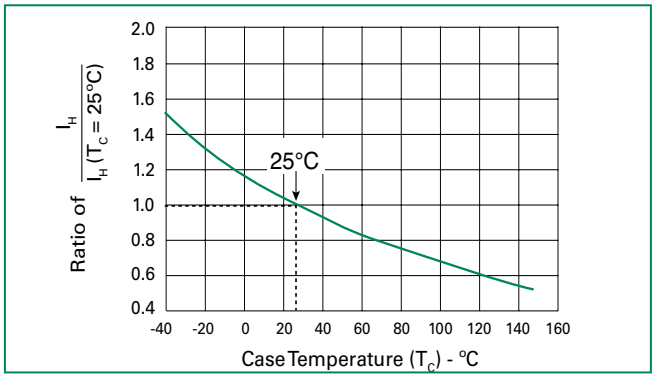
V-I Characteristics



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature



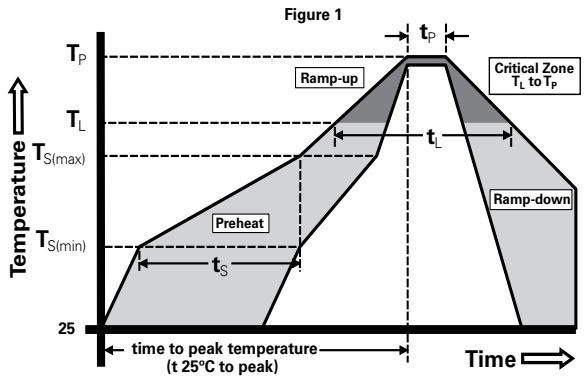
Revised: 02/23/17

SIDACtor® Protection Thyristors
High Surge Current Protection

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85% RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100% RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85% RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

Part Numbering

P xxx 2 A C L xx

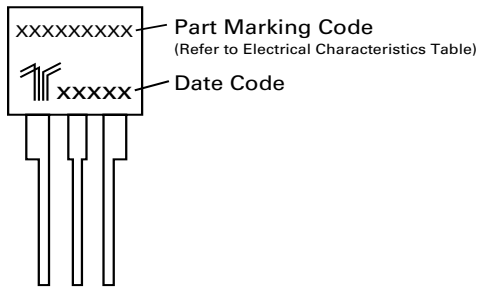
- **TYPE** — **P** = SIDACtor
- **MEDIAN VOLTAGE**
- **CONSTRUCTION VARIABLE**
- **PACKAGE TYPE**
- **PACKING OPTIONS** — **Blank**: Bulk; **RP:** Reel Pack; **60:** Type 60 Lead Form (for type 60 orders, contact factory).
- **RoHS COMPLIANT**
- **I_{PP} RATING**

P xxx 2 A C L FS1

- **TYPE** — **P** = SIDACtor
- **MEDIAN VOLTAGE**
- **CONSTRUCTION VARIABLE**
- **PACKAGE TYPE**
- **FAILSAFE OPTION***
- **RoHS COMPLIANT**
- **I_{PP} RATING**

* Failsafe devices are only offered in bulk pack, reel pack not available.

Part Marking

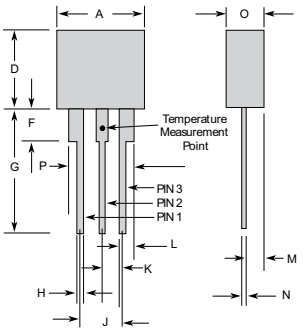


Additional Information

Datasheet | Resources | Samples

Revised: 02/23/17

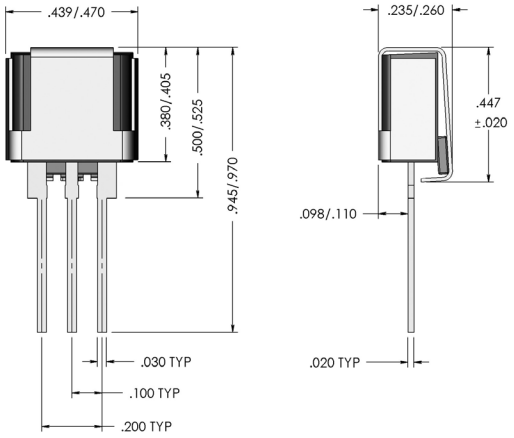
Dimensions - Modified TO-220



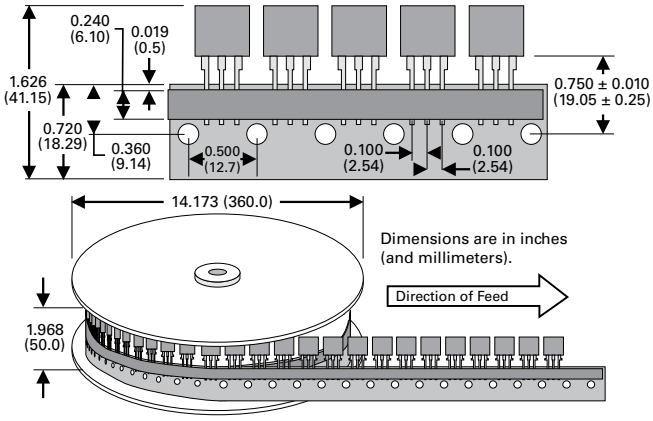
The modified TO-220 package is designed to meet mechanical standards as set forth in JEDEC publication number 95.

	Inches		Millimeters	
	Min	Max	Min	Max
A	0.400	0.410	10.16	10.42
D	0.360	0.375	9.14	9.53
F	0.110	0.130	2.80	3.30
G	0.540	0.575	13.71	14.61
H	0.025	0.035	0.63	0.89
J	0.195	0.205	4.95	5.21
K	0.095	0.105	2.41	2.67
L	0.060	0.075	1.52	1.90
M	0.070	0.085	1.78	2.16
N	0.018	0.024	0.46	0.61
O	0.178	0.188	4.52	4.78
P	0.290	0.310	7.37	7.87

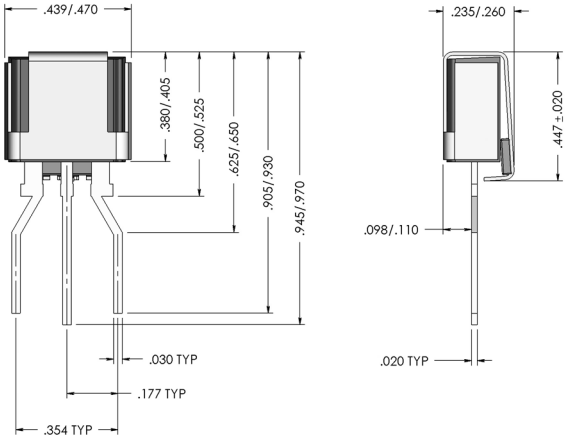
Dimensions - Modified TO-220 with Failsafe



Tape and Reel Specification - Modified TO-220



Dimensions - Modified TO-220 Type 60 with Failsafe



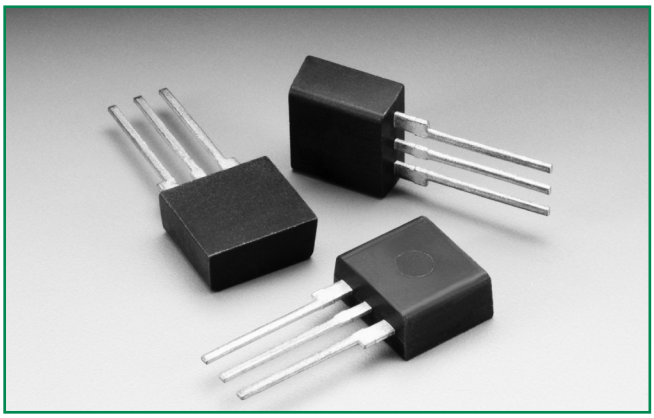
Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
A	Modified TO-220 Tape and Reel Pack	700	RP	EIA-468-B
	Modified TO-220 Bulk Pack	500	(no added suffix)	N/A
	Modified TO-220 Type 60 Lead Form Bulk Pack	500	60 (special order item, contact factory for details)	N/A

Littelfuse
Expertise Applied | Answers Delivered

SIDACtor® Protection Thyristors
High Surge Current Protection

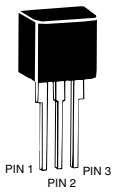
SIDACtor® Primary Protection Balanced Series - Modified TO-220



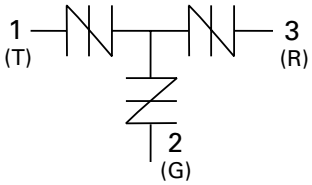
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation



Schematic Symbol



Description

The SIDACtor® Primary Protection Balanced Series Modified TO-220 thyristors are components designed for use in primary protection applications.

The series provides a single port overvoltage solution that enables applications to comply with the balance requirements of GR-974 and GTS-8700. Please contact Littelfuse to discuss your particular application and regulatory requirements.

Features and Benefits

- High holding current options available
- Balanced overvoltage protection
- Failsafe option available
- Low voltage overshoot
- Low on-state voltage
- Does not degrade surge capability after multiple surge events within limit.
- Fails short circuit when surged in excess of ratings
- Single-port protection
- Modified TO-220 Package
- Lead forms available
- RoHS Compliant
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) IPC/JEDEC J-STD-609A.01

Applicable Global Standards

- GR-974
- GTS-8700
- UL 497
- ITU K.28

Electrical Characteristics

Part Number	Marking	V_{DRM} @I_{DRM}=5µA	V_S @100V/µs	I_H*	I_S	I_T	V_T@I_T= 2.2 Amps	Capacitance			
								Pin 1-2 / 3-2 Tip-Ground, Ring-Ground		Pin 1-3 Tip-Ring	
		V min	V max	mA	mA	A	V max				
		Pins 1-2, 3-2, 1-3		min	max	max		pF min	pF max	pF min	pF max
P1553ACLxx	P1553AC	130	180	150	800	2.2	8	65	95	40	60
P1803ACLxx	P1803AC	150	210	150	800	2.2	8	55	85	35	55
P2103ACLxx	P2103AC	170	250	150	800	2.2	8	55	85	30	55
P2353ACLxx	P2353AC	200	270	150	800	2.2	8	50	75	30	50
P2703ACLxx	P2703AC	230	300	150	800	2.2	8	50	75	30	50
P3203ACLxx	P3203AC	270	350	150	800	2.2	8	45	70	25	45
P3403ACLxx	P3403AC	300	400	150	800	2.2	8	45	65	25	45
P5103ACLxx	P5103AC	420	600	150	800	2.2	8	40	60	20	40

Notes:
* Higher holding current available by special order. Contact Littelfuse for additional information.
- Absolute maximum ratings measured at T_A= 25ºC (unless otherwise noted).
- Components are bi-directional.
- Off-state capacitance (C_O) is measured at 1 MHz with a 2 V bias.
- **xx** Part Number Suffix: **'RP'** (Reel pack), **Blank** (Bulk pack), **'60'** (Type 60 lead form bulk pack), **'FS1'** (Failsafe option bulk pack). Refer to Part Numbering section for additional details.

Revised: 02/23/17

Surge Ratings

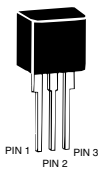
Series	I_{PP}									I_{TSM} 50/60 Hz	di/dt
	0.2/310 [1] 0.5/700 [2]	2/10 [1] 2/10 [2]	8/20 [1] 1.2/50 [2]	10/160 [1] 10/160 [2]	10/560 [1] 10/560 [2]	5/320 [1] 9/720 [2]	10/360 [1] 10/360 [2]	10/1000 [1] 10/1000 [2]	5/310 [1] 10/700 [2]		
	A min	A min	A min	A min	A min	A min	A min	A min	A min	A min	A/µs max
C	50	500	400	200	150	200	175	100	200	50	500

Notes:

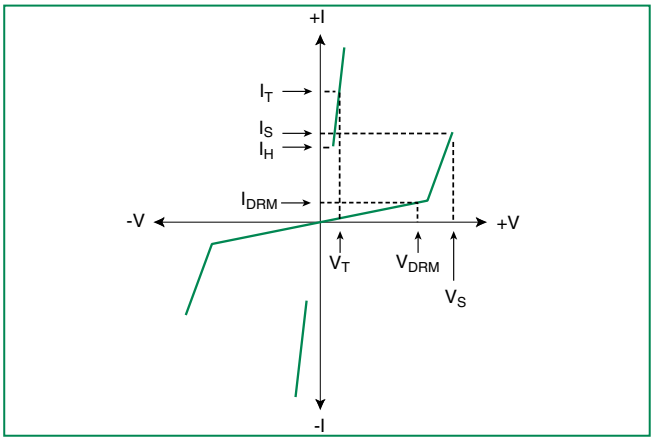
1 Current waveform in µs
2 Voltage waveform in µs

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product in thermal equilibrium.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The component must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

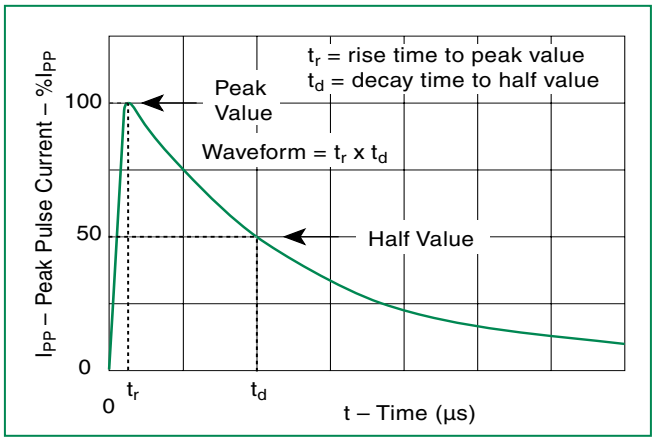
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
Modified TO-220 	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_S	Storage Temperature Range	-65 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	50	°C/W

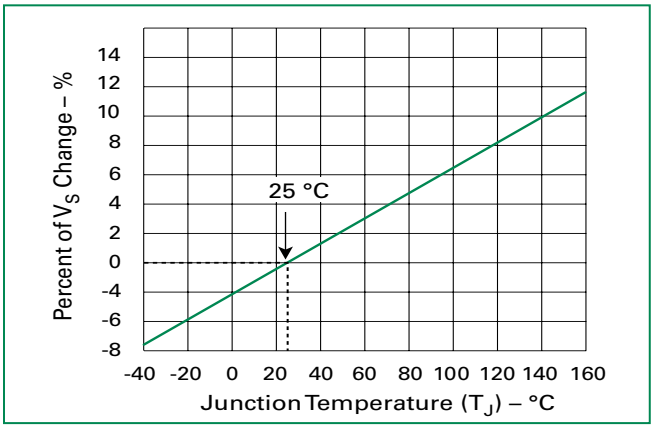
V-I Characteristics



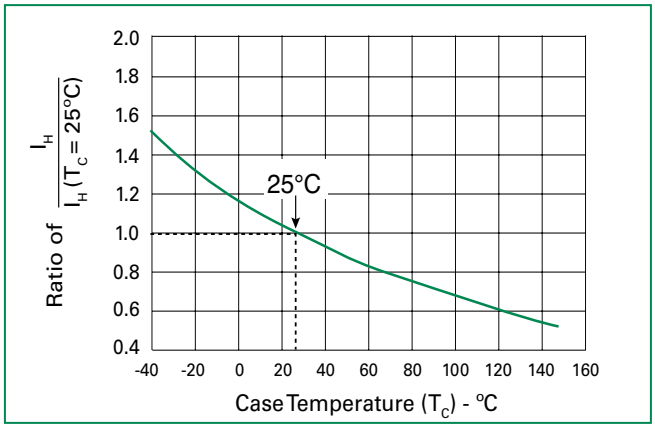
t_r x t_d Pulse Waveform



Normalized V_S Change vs. Junction Temperature



Normalized DC Holding Current vs. Case Temperature



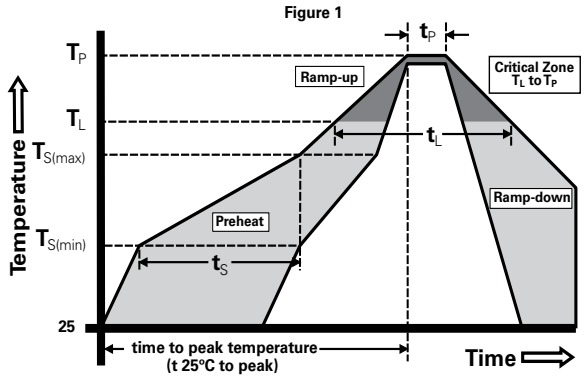
Revised: 02/23/17

SIDACtor® Protection Thyristors
High Surge Current Protection

Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



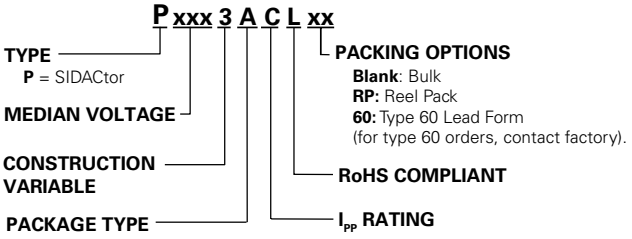
Physical Specifications

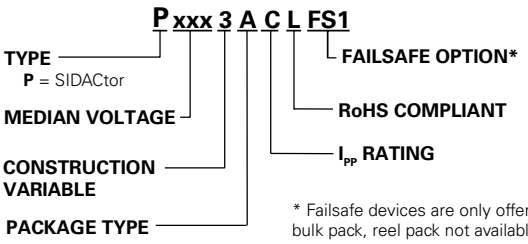
Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized epoxy meeting flammability classification V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85% RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100% RH, 2atm, 24 up to 168 hrs. EIA/JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85% RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

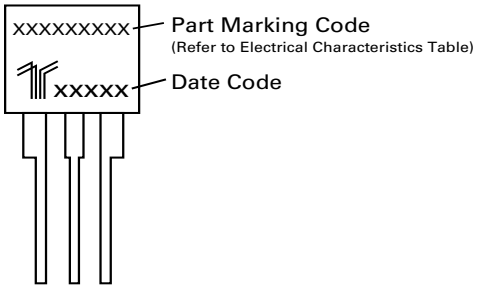
Part Numbering





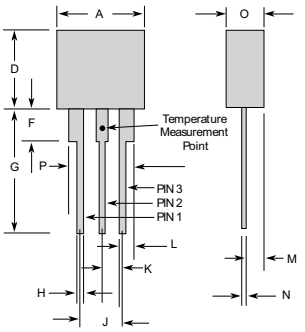
* Failsafe devices are only offered in bulk pack, reel pack not available.

Part Marking



Revised: 02/23/17

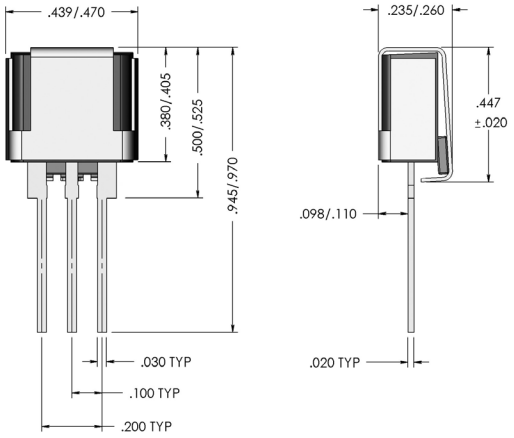
Dimensions - Modified TO-220



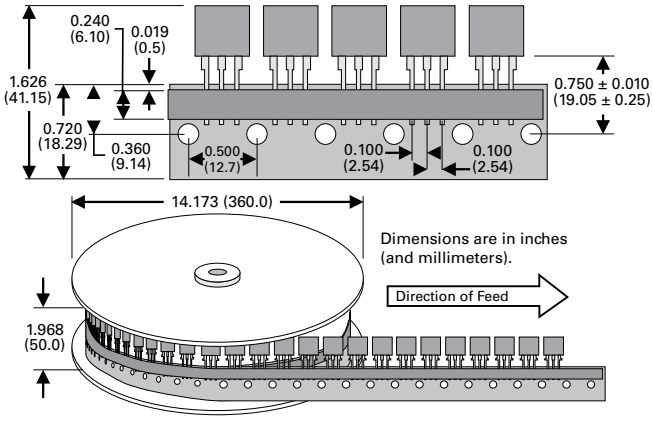
The modified TO-220 package is designed to meet mechanical standards as set forth in JEDEC publication number 95.

	Inches		Millimeters	
	Min	Max	Min	Max
A	0.400	0.410	10.16	10.42
D	0.360	0.375	9.14	9.53
F	0.110	0.130	2.80	3.30
G	0.540	0.575	13.71	14.61
H	0.025	0.035	0.63	0.89
J	0.195	0.205	4.95	5.21
K	0.095	0.105	2.41	2.67
L	0.060	0.075	1.52	1.90
M	0.070	0.085	1.78	2.16
N	0.018	0.024	0.46	0.61
O	0.178	0.188	4.52	4.78
P	0.290	0.310	7.37	7.87

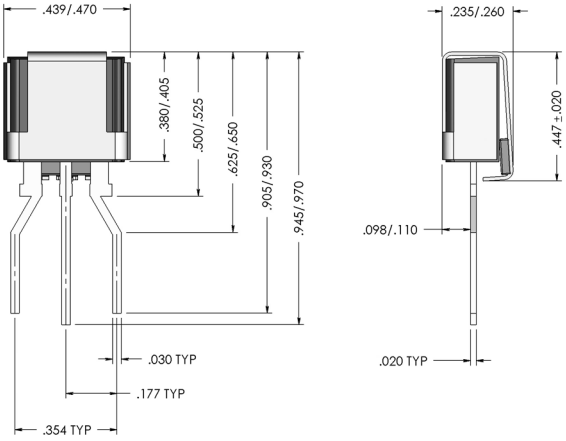
Dimensions - Modified TO-220 with Failsafe



Tape and Reel Specification - Modified TO-220



Dimensions - Modified TO-220 Type 60 with Failsafe



Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
A	Modified TO-220 Tape and Reel Pack	700	RP	EIA-468-B
	Modified TO-220 Bulk Pack	500	(no added suffix)	N/A
	Modified TO-220 Type 60 Lead Form Bulk Pack	500	60 (special order item, contact factory for details)	N/A

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