MAX78630+PPM
Energy Measurement Processor for Polyphase Monitoring Systems

DATA SHEET

GENERAL DESCRIPTION

The MAX78630+PPM is an energy measurement processor for polyphase power-monitoring systems. It is designed for real-time monitoring for a variety of typical three-phase configurations in industrial applications. It is available in a 32-pin TQFN package with an exposed pad.

The MAX78630+PPM provides up to six analog inputs for interfacing to voltage and current sensors. Scaled voltages from the sensors are fed to the single converter front-end using a high-resolution delta-sigma converter. Supported current sensors include current transformers (CTs), Rogowski coils, and resistive shunts.

An embedded 24-bit measurement processor and firmware perform all necessary computations and data formatting for accurate reporting to the host. With integrated flash memory for storing nonvolatile calibration coefficients and device configuration settings, the MAX78630+PPM can be a completely autonomous solution.

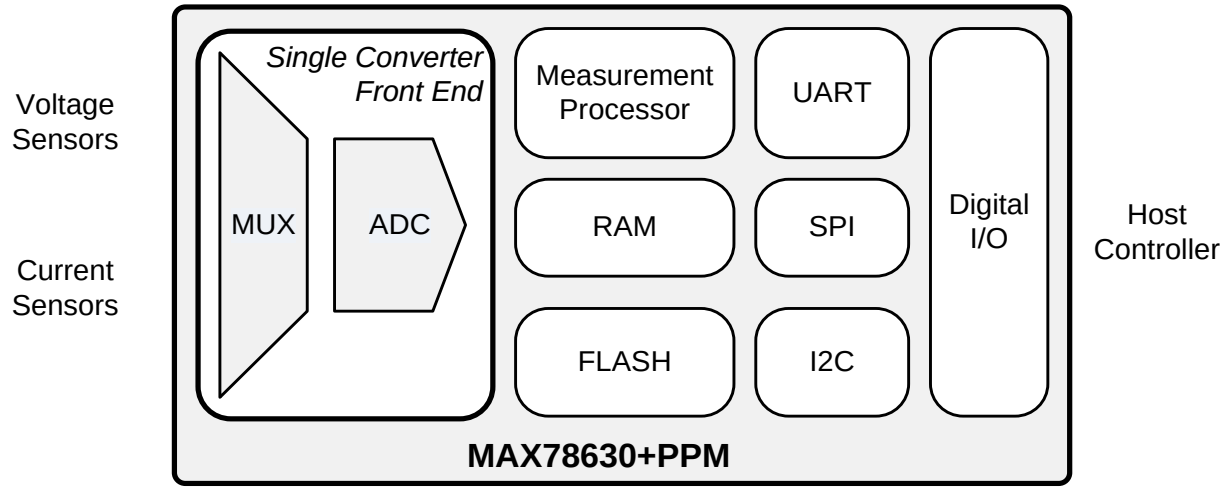
The MAX78630+PPM is designed to interface to the host processor via the UART interface. Alternatively, SPI or I^2C can also be used.

APPLICATIONS

- Building Automation Systems (Commercial, Industrial)
- Inverters and Renewable Energy Systems

BENEFITS AND FEATURES

- Six Configurable Analog Inputs for Monitoring a Variety of Delta- and Wye-Connected Three-Phase Topologies
- Supports Current Transformers (CTs), Resistive Shunts, and Rogowski Coils
- Delta-Sigma ADC with Precision Voltage Reference and On-Chip Temperature Sensor
- Internal or External Oscillator Timing Reference
- SPI, I^2C, or UART Interface Options with Configurable I/O Pins for Alarm Signaling, Address Pins, or User Control
- 24-Bit Measurement Processor with Integrated Firmware and Flash Memory for Nonvolatile Storage of Calibration and Configuration Parameters
- Supports Extraction of Individual Harmonics
- Small 32-TQFN Package and Reduced Bill of Materials



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Electrical Specifications

Absolute Maximum Ratings

(All voltages with respect to ground.)

Supplies and Ground Pins:	
V_{3P3D}, V_{3P3A}	-0.5V to 4.6V
GNDD, GNDA	-0.5V to +0.5V
Analog Input Pins:	
AV1, AV2, AV3, AI1, AI2, AI3	-10mA to +10mA -0.5V to (V_{3P3} + 0.5V)
Oscillator Pins:	
XIN, XOUT	-10mA to +10mA -0.5V to 3.0V
Digital Pins:	
DIO0 through DIO15; *Digital Pins configured as outputs*	-30mA to +30mA, -0.5 to (V_{3P3D} + 0.5V)
DIO0 through DIO15, $\overline{\text{RESET}}$; *Digital Pins configured as inputs*	-10mA to +10mA, -0.5V to +6V
Temperatures:	
Operating Junction Temperature	
Peak, 100ms	+140°C
Continuous	+125°C
Storage Temperature Range	-45°C to +165°C
Lead Temperature (soldering, 10s)	+260°C
Soldering Temperature (reflow)	+300°C
ESD Stress on All Pins	±4kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended External Components

NAME	FROM	TO	FUNCTION	VALUE	UNITS
XTAL	XIN	XOUT	20.000MHz	20.000	MHz
CXS	XIN	GNDD	Load capacitor for crystal (exact value depends on crystal specifications and parasitic capacitance of board)	18 ±10%	pF
CXL	XOUT	GNDD		18 ±10%	pF

Recommended Operating Conditions

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V Supply Voltage (V_{3P3})	Normal operation	3.0	3.3	3.6	V
Operating Temperature		-40		+85	°C

Performance Specifications

Note that production tests are performed at room temperature.

Input Logic Levels

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital High-Level Input Voltage (V_{IH})		2			V
Digital Low-Level Input Voltage (V_{IL})				0.8	V

Output Logic Levels

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital High-Level Output Voltage (V_{OH})	I_{LOAD} = 1mA	V_{3P3} - 0.4			V
	I_{LOAD} = 10mA	V_{3P3} - 0.6			V
Digital Low-Level Output Voltage (V_{OL})	I_{LOAD} = 1mA	0		0.4	V
	I_{LOAD} = 10mA			0.5	V

Supply Current

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{3P3D} and V_{3P3A} Current (Compounded)	Normal operation, V_{3P3} = 3.3V		8.1	10.3	mA

Crystal Oscillator

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
XIN to XOUT Capacitance	(Note 1)		3		pF
Capacitance to GNDD (Note 1)	XIN		5		pF
	XOUT		5		

Note 1: Guaranteed by design; not subject to test.

Internal RC Oscillator

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Nominal Frequency			20.000		MHz
Accuracy	V_{3P3} = 3.0V, 3.6V; T_A = -40°C to +85°C		±1.5	±1.75	%

ADC Converter, V_{3P3} Referenced

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Usable Input Range (V_{IN} - V_{3P3})		-250		+250	mV peak
THD (First 10 Harmonics)	V_{IN} = 65Hz, 64kpts FFT, Blackman-Harris window		-85		dB
Input Impedance	V_{IN} = 65Hz	30		90	kΩ
Temperature Coefficient of Input Impedance	V_{IN} = 65Hz (Note 1)		1.7		Ω/°C
ADC Gain Error vs. %Power Supply Variation $\frac{10^6 \Delta Nout_{PK}\, 357nV/V_{IN}}{100 \Delta V3P3A/3.3}$	V_{IN} = 200mVpk, 65Hz; V_{3P3} = 3.0V, 3.6V			50	ppm/%
Input Offset (V_{IN} - V_{3P3})		-10		+10	mV

[1] Guaranteed by design; not subject to test.

Timing Specifications

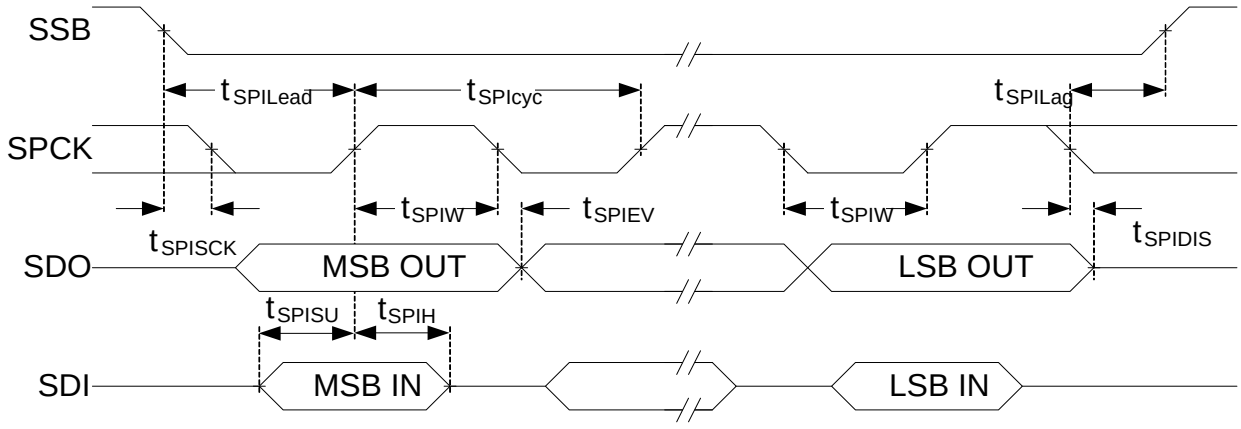
Reset

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Pulse Fall Time	(Note 1)		1		µs
Reset Pulse Width	(Note 1)		5		µs

SPI Slave Port

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SPCK Cycle Time (t_{SPIcyc})		1			µs
Enable Lead Time ($t_{SPILead}$)		15			ns
Enable Lag Time (t_{SPILag})		0			ns
SPCK Pulse Width (t_{SPIW})	High	250			ns
	Low	250			
SSB to First SPCK Fall (t_{SPISCK})	Ignore if SPCK is low when SSB falls (Note 1)		2		ns
Disable Time (t_{SPIDIS})	(Note 1)		0		ns
SPCK to Data Out (SDO) (t_{SPIEV})				25	ns
Data Input Setup Time (SDI) (t_{SPISU})		10			ns
Data Input Hold Time (SDI) (t_{SPIH})		5			ns

Note 1: Guaranteed by design, not subject to test.



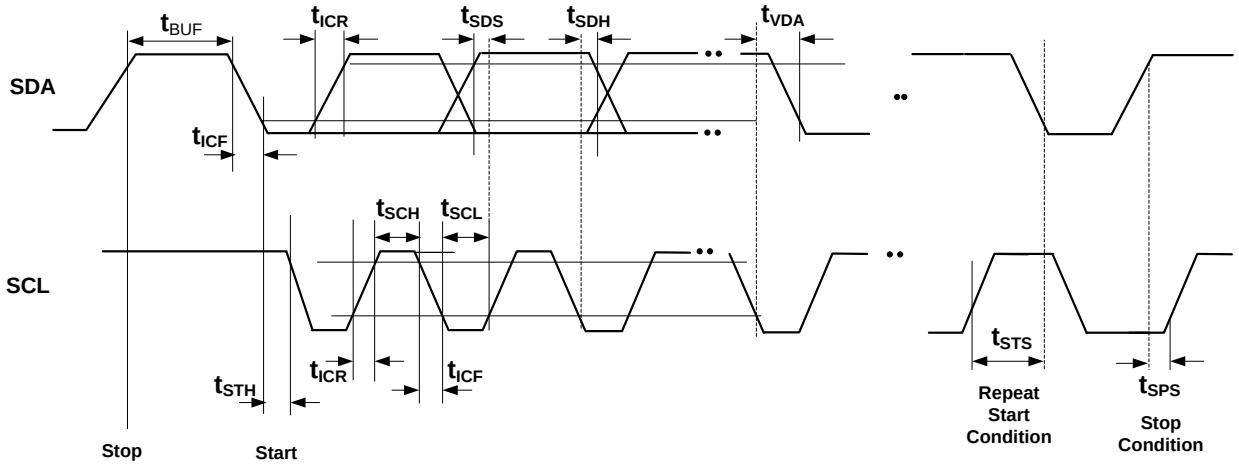
I²C Slave Port

(Note 1)

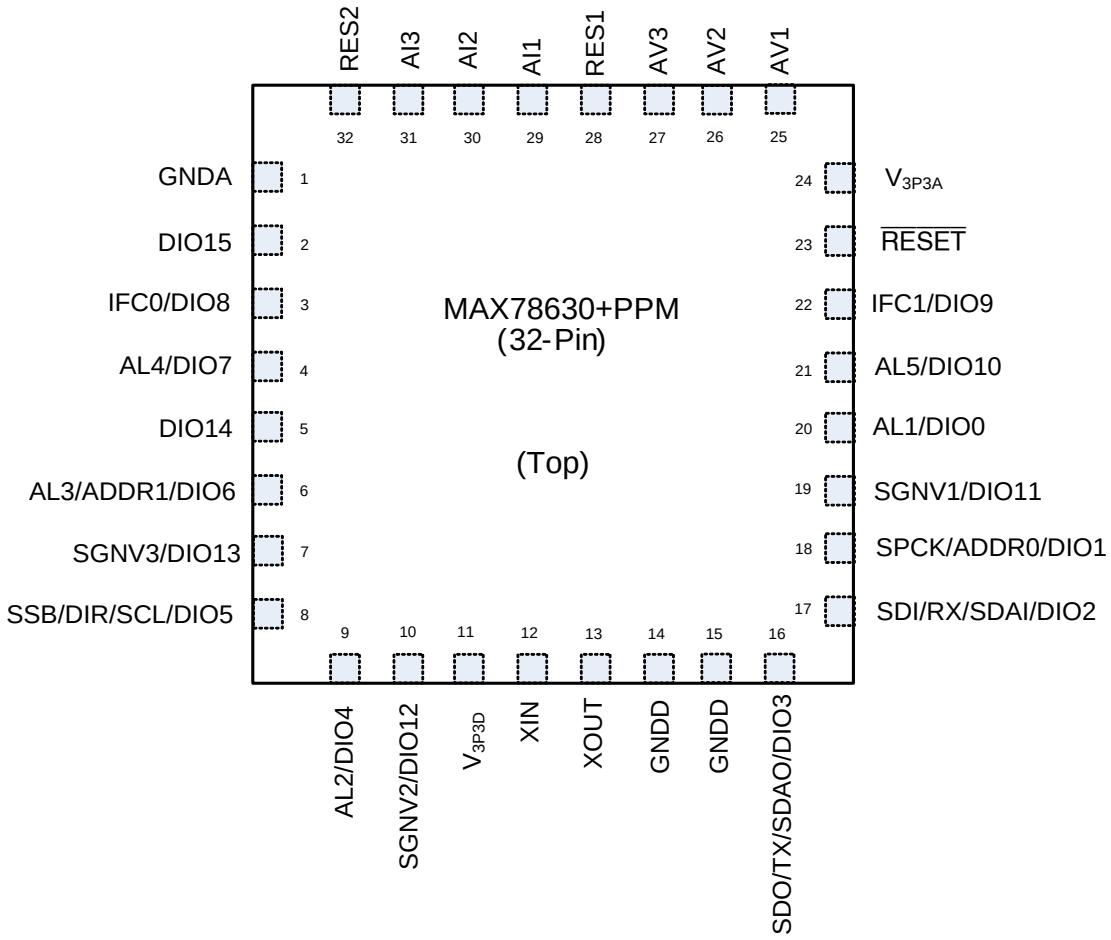
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Bus Idle (Free) Time Between Transmissions (STOP/START) (t_{BUF})		1500			ns
I²C Input Fall Time (t_{ICF})	(Note 2)	20		300	ns
I²C Input Rise Time (t_{ICR})	(Note 2)	20		300	ns
I²C START or Repeated START Condition Hold Time (t_{STH})		500			ns
I²C START or Repeated START Condition Setup Time (t_{STS})		600			ns
I²C Clock High Time (t_{SCH})		600			ns
I²C Clock Low Time (t_{SCL})		1300			ns
I²C Serial Data Setup Time (t_{SDS})		100			ns
I²C Serial Data Hold Time (t_{SDH})		10			ns
I²C Valid Data Time (t_{VDA}): SCL Low to SDA Output Valid ACK Signal from SCL Low to SDA (Out) Low				900	ns

Note 1: Guaranteed by design, not subject to test

Note 2: Dependent on bus capacitance.



Pin Configuration



Pin	Signal	Function	Pin	Signal	Function
1	GNDA	GROUND (Analog)	17	SDI/RX/SDAI/ DIO2	SPI DATA IN / UART RX/ I2C Data In / Digital I/O
2	DIO15	Digital I/O	18	SPCK/ADDR0/ DIO1	SPI CLOCK IN / I2C/Multi-Point UART Address/ Digital I/O
3	IFC0/DIO8	IFC1/SPI (1=IFC1 pin; 0=SPI) (1) / Digital I/O	19	SGNV1 / DIO11	Sign of AV1 Output / Digital I/O
4	AL4/DIO7	Alarm Output / Digital I/O	20	AL1/DIO0	Alarm Output / Digital I/O
5	DIO14	Digital I/O	21	AL5/DIO10	Alarm Output / Digital I/O
6	AL3/ADDR1/ DIO6	I2C/ UART Address / Alarm Output / Digital I/O	22	IFC1//DIO9	I^2C/UART (1=I^2C;0=UART) (1) / Digital I/O
7	SGNV3 / DIO13	Sign of AV3 Output / Digital I/O	23	$\overline{\text{RESET}}$	Reset Input
8	SSB/DIR/SCL/ DIO5	Slave Select (SPI) / RS485 TX-RX / I2C Serial Clock/ Digital I/O	24	V_{3P3A}	3.3VDC Supply (Analog)
9	AL2/DIO4	Alarm Output / Digital I/O	25	AV1	Voltage Input (Phase 1)
10	SGNV2 / DIO12	Sign of AV2 Output / Digital I/O	26	AV2	Voltage Input (Phase 2)
11	V_{3P3D}	3.3VDC Supply (Digital)	27	AV3	Voltage Input (Phase 3)
12	XIN	Crystal Oscillator Driver Input	28	RES1	Reserved for future use. Tie to V3P3A
13	XOUT	Crystal Oscillator Driver Output	29	AI1	Current Input (Phase 1)
14	GNDD	GROUND (Digital)	30	AI2	Current Input (Phase 2)
15	GNDD	GROUND (Digital)	31	AI3	Current Input (Phase 3)
16	SDO/TX/ SDAO/DIO3	SPI DATA OUT/ UART TX/ I2C Data Out / Digital I/O	32	RES2	Reserved for future use. Tie to V3P3A

Notes:

1) **IFC0** and **IFC1** pins are sampled at power-on to select the communication peripheral as follows:
   IFC0 = 0 to select SPI; **IFC1** = X (Don't Care)
   IFC0 = 1, **IFC1** =0 to select UART/RS485; **IFC1** = 1 to select I^2C

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+4	**21-0140**	**90-0012**

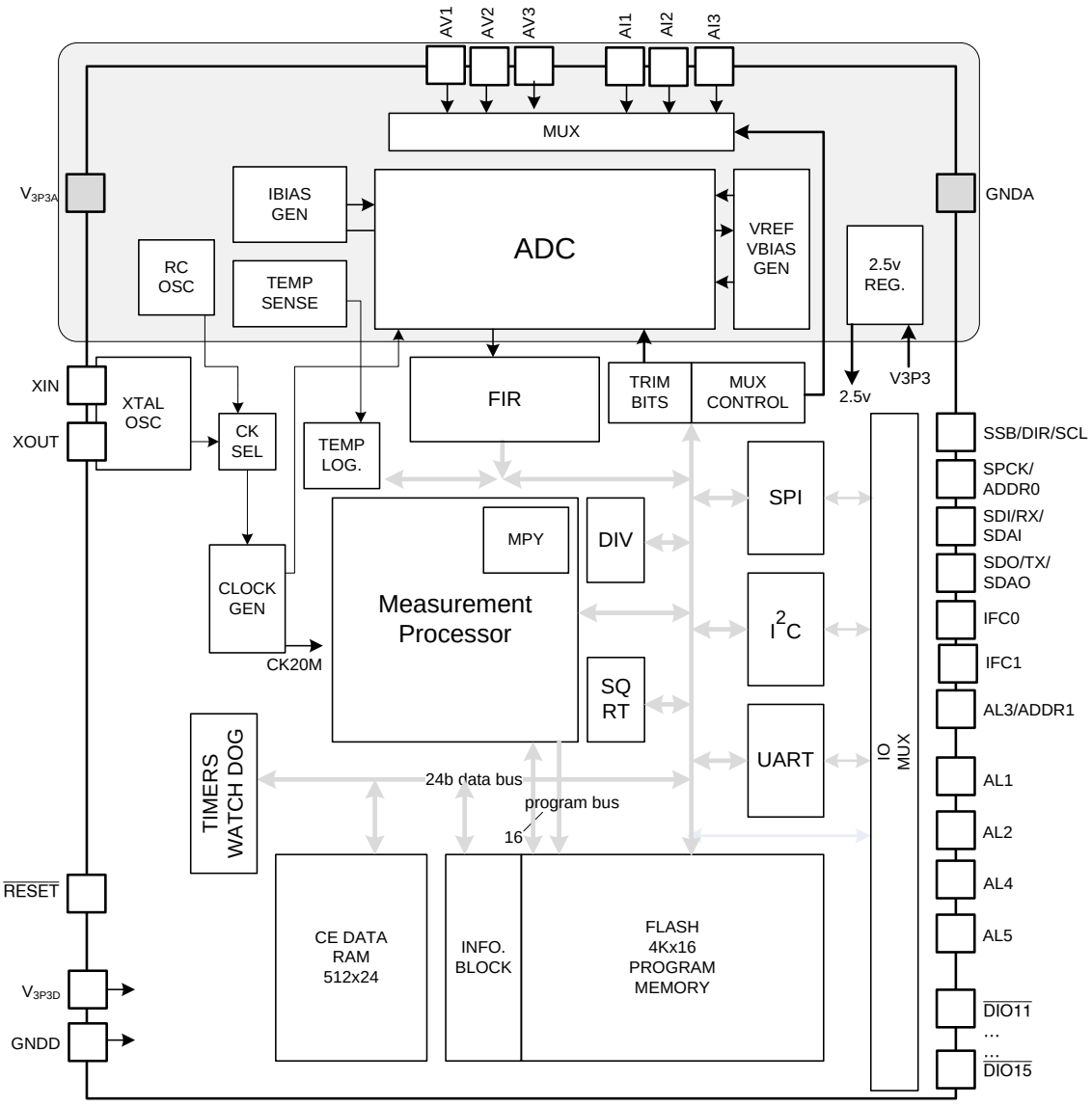
On-Chip Resources Overview

The MAX78630+PPM device integrates all the hardware blocks required for accurate AC power and energy measurement. Included on the device are:

- Oscillator and clock management logic
- Power-on reset, watchdog timer, and reset circuitry
- High-accuracy Analog Front End (AFE) with trimmed voltage reference and temperature sensor
- 24-bit measurement processor with RAM and flash memory
- UART, SPI and I^2C serial communication interfaces and multipurpose Digital I/O

IC Block Diagram

The following is a block diagram of the hardware resources available on the MAX78630+PPM.

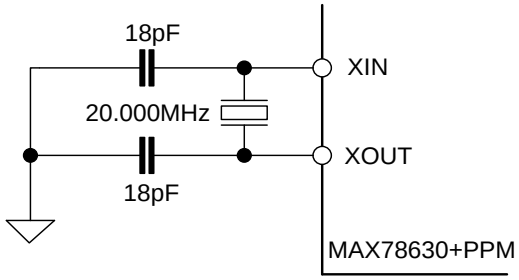


Clock Management

The device can be clocked by oscillator circuitry that relies on an external crystal or, as a backup source, by a trimmed internal RC oscillator. The internal RC oscillator provides an accurate clock source for UART baud rate generation.

The chip hardware automatically handles the clock sources logic and distributes the clock to the rest of the device. Upon reset or power-on, the device will utilize the internal RC oscillator circuit for the first 1024 clock cycles, allowing the external crystal adequate time to start-up. The device will then automatically select the external clock, if available. It will also automatically switch back to the internal oscillator in the event of a failure with the external oscillator. This condition is also monitored by the processor and available to the user in the STATUS register.

The MAX78630+PPM external clock circuitry requires a 20.000MHz crystal. The circuitry includes two 18pF ceramic capacitors. The figure below shows the typical connection of the external crystal. This oscillator is self biasing and therefore an external resistor should NOT be connected across the crystal.



An external 20MHz system clock signal can also be utilized instead of the crystal. In this case, the external clock should be connected to the XOUT pin while the XIN pin should be connected to GNDD.

Alternatively, if no external crystal or clock is utilized, the XOUT pin should be connected to GNDD and the XIN pin left unconnected.

Power-On Reset, Watchdog-Timer, and Reset Circuitry

Power-On RESET (POR)

An on-chip Power-On Reset (POR) block monitors the supply voltage (V3P3D) and initializes the internal digital circuitry at power-on. Once V3P3D is above the minimum operating threshold, the POR circuit triggers and initiates a reset sequence. It will also issue a reset to the digital circuitry if the supply voltage falls below the minimum operating level.

Watchdog Timer (WDT)

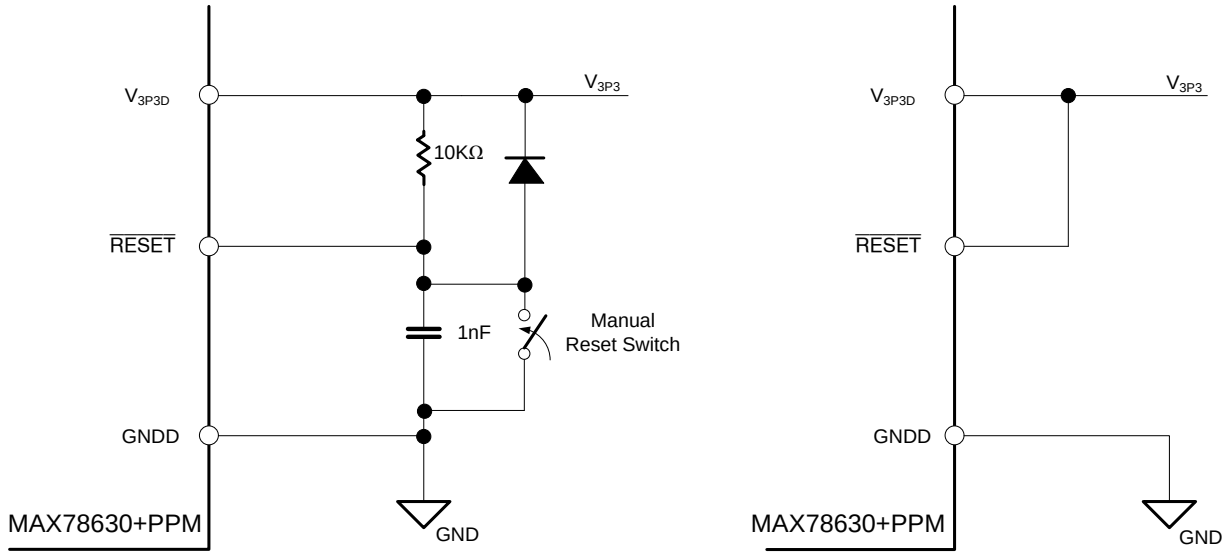
A Watchdog Timer (WDT) block detects any software processing errors. The embedded software periodically refreshes the free-running watchdog timer to prevent it from timing out. If the WDT times out, it is an indication that software is no longer being executed in the intended sequence; thus, a system reset is initiated.

External Reset Pin ($\overline{\text{RESET}}$ Pin)

In addition to the internal sources, a reset can be forced by applying a low level to the $\overline{\text{RESET}}$ pin. If the $\overline{\text{RESET}}$ pin is pulled low, all digital activities in the device stop, except the clock management circuitry and oscillators, which continue to run. The external reset input is filtered to prevent spurious reset events in noisy environments. The reset does not occur until $\overline{\text{RESET}}$ has been held low for at least 1 µs.

Once initiated, the reset mode persists until the $\overline{\text{RESET}}$ is set high and the reset timer times out (4096 clock cycles). At the completion of the reset sequence, the internal reset is released and the processor begins executing from address 0.

If not used, the $\overline{\text{RESET}}$ pin can be connected either directly or through a pull-up resistor to V3P3D supply. A simple connection diagram is shown below.



a) $\overline{\text{RESET}}$ External Connection Example

b) Unused $\overline{\text{RESET}}$ Connection Example

Analog Front-End and Conversion

The Analog Front-End (AFE) of the MAX78630+PPM includes an input multiplexer, optional pre-amplifier gain stage, Delta-Sigma A/D Converter, bias current references, voltage references, temperature sensor, and several voltage fault comparators.

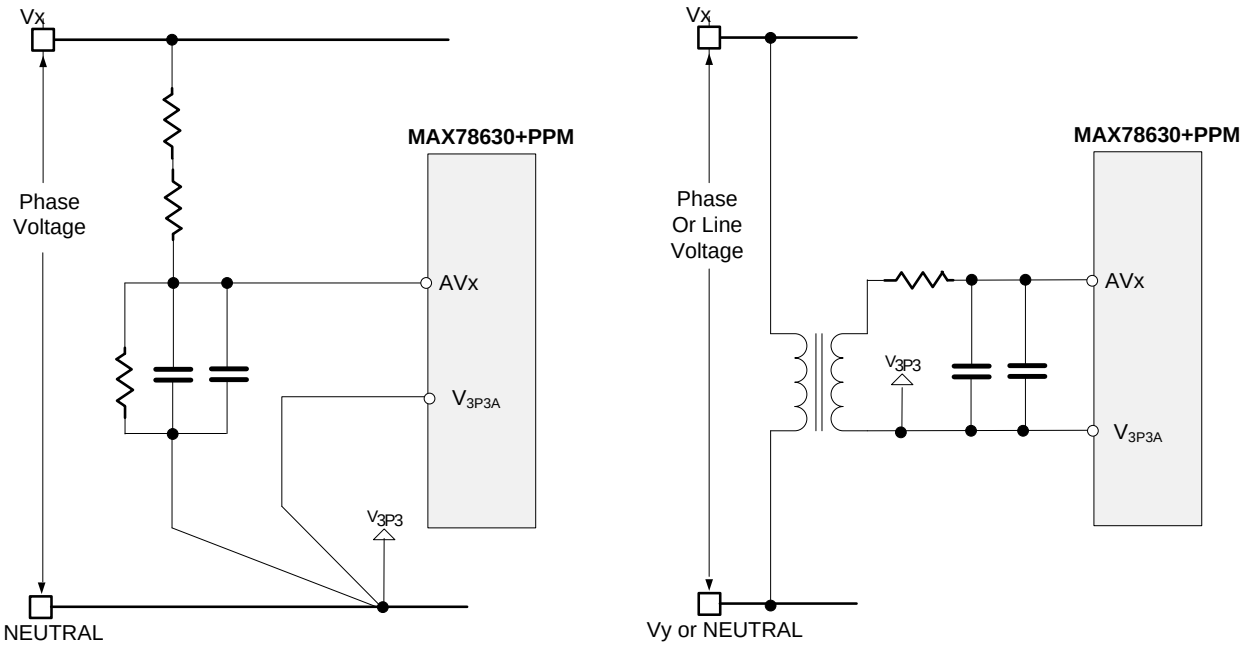
Analog Inputs

Up to six external sensors can be connected to the MAX78630+PPM. The full-scale signal level that can be applied to any analog input pin with respect to V_{3P3A} is ±250 mVpk. Considering a sinusoidal AC waveform, the maximum RMS voltage applied to the inputs pins is:

$$\text{rmsMAX} = \frac{250mVpk}{\sqrt{2}} = 176.78\text{mVrms}$$

Voltage Inputs

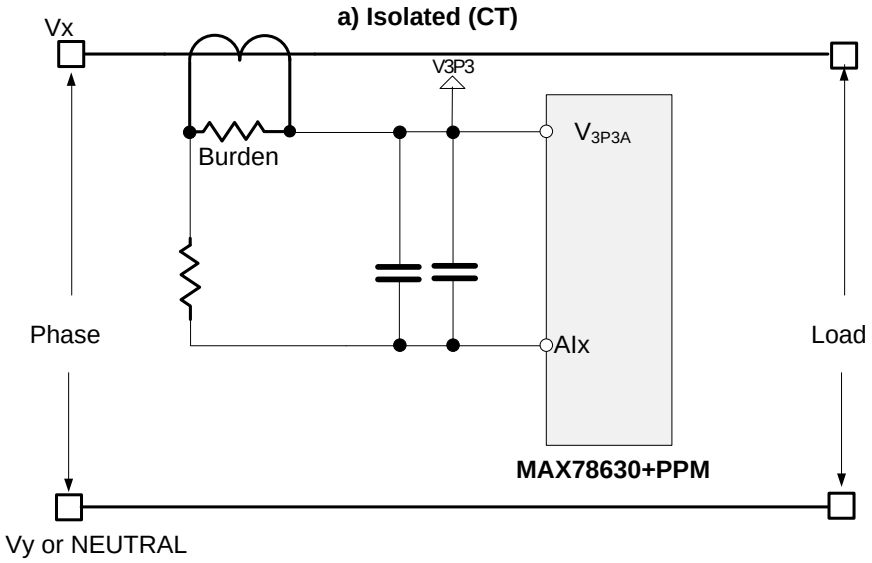
Three single-ended input pins (AVA, AVB and AVC) can be connected to external voltage sensors. The figure below shows example signal conditioning circuits for a voltage input in both isolated (via voltage transformers) and non-isolated (via a resistor divider circuit) cases. Complete system diagrams for wye- and a delta-connected three-phase system are shown in the Applications Examples section of this document. Consult application notes for more information on component selection and PCB design considerations.

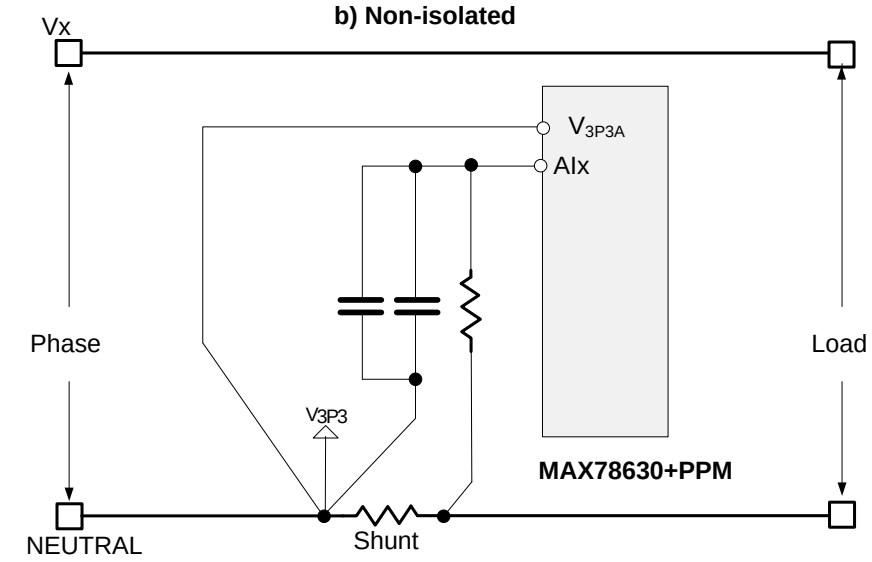


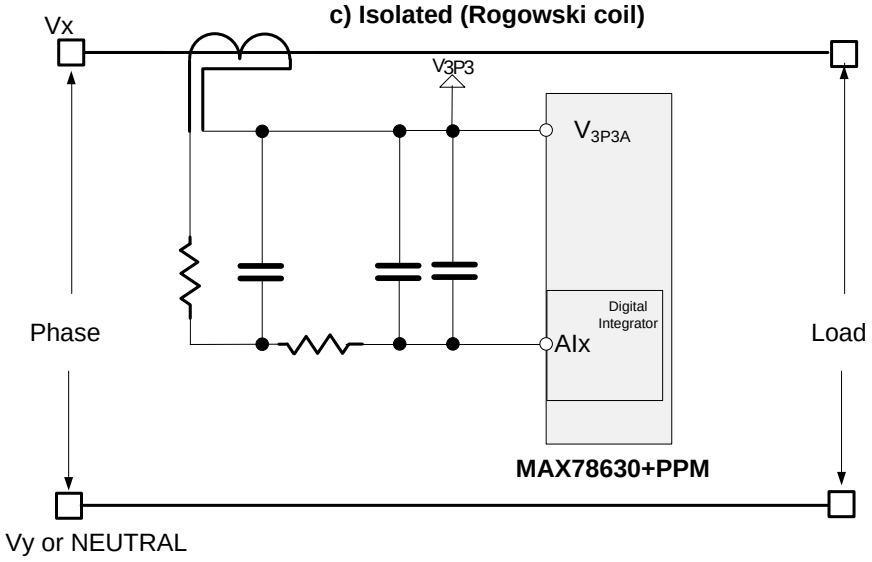
a) Non-isolated **b) Isolated**

Current Inputs

Similarly, three single-ended input pins (AIA, AIB and AIC) can be connected to external current sensors. The figure on the following page shows example signal conditioning circuits for a current input. One diagram each is shown for measurement via a resistive shunt (a), a current transformer (b) and a Rogowski coil (c). The latter requires the user to enable the built-in digital integrator and implement a lowpass filter. Complete system diagrams for wye- and a delta-connected three-phase system are shown in the Applications Examples section of this document. Consult application notes for more information on component selection and PCB design considerations.


a) Isolated (CT)
Vx
V3P3
Burden
V_{3P3A}
Phase
AIx
Load
MAX78630+PPM
Vy or NEUTRAL


b) Non-isolated
Vx
V_{3P3A}
AIx
Phase
Load
V3P3
MAX78630+PPM
NEUTRAL
Shunt


c) Isolated (Rogowski coil)
Vx
V3P3
V_{3P3A}
Digital Integrator
Phase
AIx
Load
MAX78630+PPM
Vy or NEUTRAL

Delta-Sigma A/D Converter

A second-order Delta-Sigma converter digitizes the analog inputs. The converted data is then processed through an FIR filter.

Voltage Reference

The device includes an on-chip precision band-gap voltage reference that incorporates auto-zero techniques as well as production trims to minimize errors caused by component mismatch and drift. The voltage reference is digitally compensated over temperature.

Die Temperature Measurement

The device includes an on-chip die temperature sensor used for digital compensation of the voltage reference. It is also used to report temperature information to the user.

24-Bit Measurement Processor

The MAX78630+PPM integrates a fixed-point 24-bit signal processor that performs all the digital signal processing necessary for energy measurement, alarm generation, calibration, compensation, etc. Functionality and operation of the device is determined by the firmware and described in the Functional Description and Operation section.

Flash and RAM

The MAX78630+PPM includes 8KB of on-chip flash memory. The flash memory primarily contains program code, but also stores coefficients, calibration data, and configuration settings. The MAX78630+PPM includes 1.5KB of on-chip RAM which contains the values of input and output registers and is utilized by the FW for its operations.

Digital I/O Pins

There are a total of sixteen digital input/outputs (DIOs) on the MAX78630+PPM device. Some are dedicated to serial interface communications and configuration. Others are multi-purpose I/O that can be used as a simple output under user control or routed to special purpose internal signals, such as alarm signaling.

Communication Interfaces

The MAX78630+PPM includes three communication interface options: UART, SPI, and I2C. Since the I/O pins are shared, only one mode is supported at a time. Interface configuration and address pins are sampled at power-on or reset to determine which interface will be active and to set device addresses.

Functional Description and Operation

This section describes the MAX78630+PPM functionality. It includes measurements and relevant calculations, alarms, auxiliary functions such as calibrations, zero-crossing, etc.

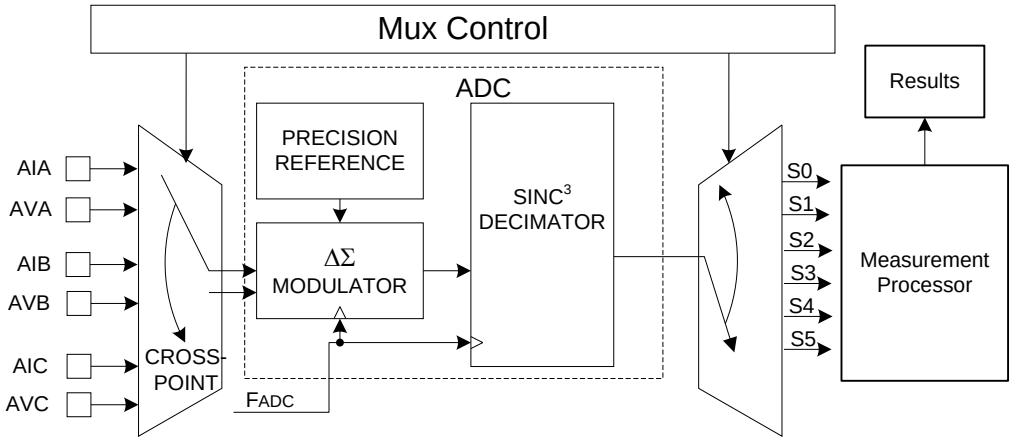
A set of input (write), output (read) and read/write registers are provided to allow access to calculated data and alarms and to configure the device. The input (write) registers values can be saved into flash memory through a specific command. The values saved into flash memory will be loaded in these registers at reset or power-on as defaults.

Measurement Interface

The MAX78630+PPM incorporates a flexible measurement interface for simplified integration into any system. This section describes the configuration and signal conditioning of the analog inputs.

AFE Input Multiplexer

The MAX78630+PPM samples six (6) external sensors with an effective sample rate of 2.7ksps for each multiplexer slot. Three analog input pins are defined as single ended voltage inputs and three as single ended current inputs.



Sensor Slot	Analog Input Pins	Input Type
S5	AIA	Current
S4	AVA	Voltage
S3	AIB	Current
S2	AVB	Voltage
S1	AIC	Current
S0	AVC	Voltage

Highpass Filters and Offset Removal

Offset registers for each analog input contain values to be subtracted from the raw ADC outputs for the purpose of removing inherent system DC offsets from any calculated power and RMS values. These registers are signed fixed-point numbers with a possible range of -1.0 to 1.0-LSB. They default to 0 and can be either manually changed by the user or by the integrated offset calibration routines.

Register	Description
V1_OFFS	Voltage Input AV1 Offset Calibration
V2_ OFFS	Voltage Input AV2 Offset Calibration
V3_ OFFS	Voltage Input AV3 Offset Calibration
I1_OFFS	Current Input AI1 Offset Calibration
I2_ OFFS	Current Input AI2 Offset Calibration
I3_ OFFS	Current Input AI3 Offset Calibration

Alternatively, the user can enable an integrated highpass filter (HPF) to dynamically update the offset registers every accumulation interval. During each accumulation interval (or low-rate cycle) the HPF calculates the median or DC average of each input. Adjustable coefficients determine what portion of the measured offset is combined with the previous offset value.

The HPF_COEF_I and HPF_COEF_V registers contain signed fixed point numbers with a usable range of 0 to 1.0-LSB (negative values are not supported). By default, they are initialized to 0.5 (0x400000) meaning the new offset value will come from ½ of the measured offset and ½ will come from the previous offset value. Setting them to 1.0 (0x7FFFFF) causes the entire measured offset to be applied to the offset register enabling lump-sum offset removal. Setting them to zero disables any dynamic update of the offset registers by the HPF. The HPF coefficients apply to all three channels (current or voltage).

Register	Description
HPF_COEF_I	HPF coefficient for AIA, AIB and AIC current inputs
HPF_COEF_V	HPF coefficient for AVA, AVB and AVC voltage inputs

Using the offset calibration routine will automatically set the filter coefficients to zero to disable the HPF.

Enabling the Software Integrators for Rogowski Coil Current Sensors

Rogowski Coil current sensors produce an output signal that is proportional to the derivative of current over time. Therefore, an integration filter is required to reconstruct the original current signal. The MAX78630+PPM provides such integrators and a configuration bit for each of the three current inputs to enable this feature.

Register[Bit]	Description
Config[EN_ROGA]	Enables the software integrator for input AIA
Config[EN_ROGB]	Enables the software integrator for input AIB
Config[EN_ROGC]	Enables the software integrator for input AIC

Enabling the software integrator will automatically disable the HPF and offset correction.

Gain Correction

The system (sensors) and the MAX78630+PPM device inherently have gain errors that can be corrected by using the gain registers. These registers can be directly accessed and modified by an external host processor or automatically updated by an integrated self calibration routine.

Input gain registers are signed fixed-point numbers with the binary point to the left of bit 21. They are set to 1.0 by default and have a usable range of 0 to 4.0-LSB (negative values are not supported). The gain equation for each input X can be described as Y=gain*X.

Register	Description
V1_GAIN	Voltage Input AV1 Gain Calibration.
V2_GAIN	Voltage Input AV2 Gain Calibration
V3_GAIN	Voltage Input AV3 Gain Calibration.
I1_GAIN	Current Input AI1 Gain Calibration
I2_GAIN	Current Input AI2 Gain Calibration
I3_GAIN	Current Input AI3 Gain Calibration

Die Temperature Compensation

The MAX78630+PPM has an on-chip temperature sensor that can be used by the measurement processor for monitoring the voltage reference error and made available to the user in the TEMPC register.

Setting the Temperature Compensation (TC) bit in the Command Register allows the firmware to further adjust the system gain based on measured die temperature. Die temperature offset is typically calibrated by the user during the calibration stage. Die temperature gain is set to a factory default value for most applications, but can be adjusted by the user.

Register	Description
T_OFFS	Die Temperature Offset Calibration.
T_GAIN	Die Temperature Slope Calibration. Set by factory.

Voltage Reference Gain Adjustment

The on-chip precision bandgap voltage reference incorporates auto-zero techniques as well as production trims to maximize measurement accuracy. It can be assumed that the part is trimmed at 22°C to produce a uniform voltage reference gain at that temperature. The voltage reference is digitally compensated over changes in measured die temperature using a quadratic equation.

Phase Compensation

Phase compensation registers are used to compensate for phase errors or time delays between the voltage input source and respective current source that are introduced by the off-chip sensor circuit. The user configurable registers are signed fixed point numbers with the binary point to the left of bit 21. Values are in units of high rate (2.7kHz) sample delays so each integer unit of delay is 370µs with a total possible delay of +/- 4 samples (approximately +/- 32° at 60Hz).

Register	Description
PHASECOMP1	Phase (delay) compensation for input current AI1
PHASECOMP2	Phase (delay) compensation for input current AI2
PHASECOMP3	Phase (delay) compensation for input current AI3

Voltage Input Configuration

The MAX78630+PPM supports multiple analog input configurations for determining the voltages in a three-phase system. The CONFIG register is used to instruct the MAX78630+PPM how to compute them.

CONFIG Bits	Name	Function
22	INV_AV3	Invert voltage samples AV3
21	INV_AV2	Invert voltage samples AV2
20	INV_AV1	Invert voltage samples AV1
5	VDELTA	Compute Line-to-Line voltages
4:3	VPHASE	Missing sensor on voltage input 00: none missing 01: AV1 10: AV2 11: AV3

The VDELTA bit must be set whenever the voltage sensors measure phase voltages (line-to-neutral), but the load is connected in a Delta configuration. The MAX78630+PPM then computes line-to-line voltages from the inputs and uses those for all other computations.

The VPHASE setting determines how many voltage sensors are present, and in which phases. If three sensors are used, these bits should be set to zero. If two sensors are used, settings 01, 10 and 11 indicate the phase with no voltage sensor. This phase will then be computed such that VA+VB+VC equals to zero. Note that using two voltage sensors is not recommended in Wye-connected systems, as the above equation may not necessarily be true.

The INV_AVx bits instruct the MAX78630+PPM to invert every sample of the corresponding voltage input, before performing any other computations based on the VDELTA and VPHASE settings.

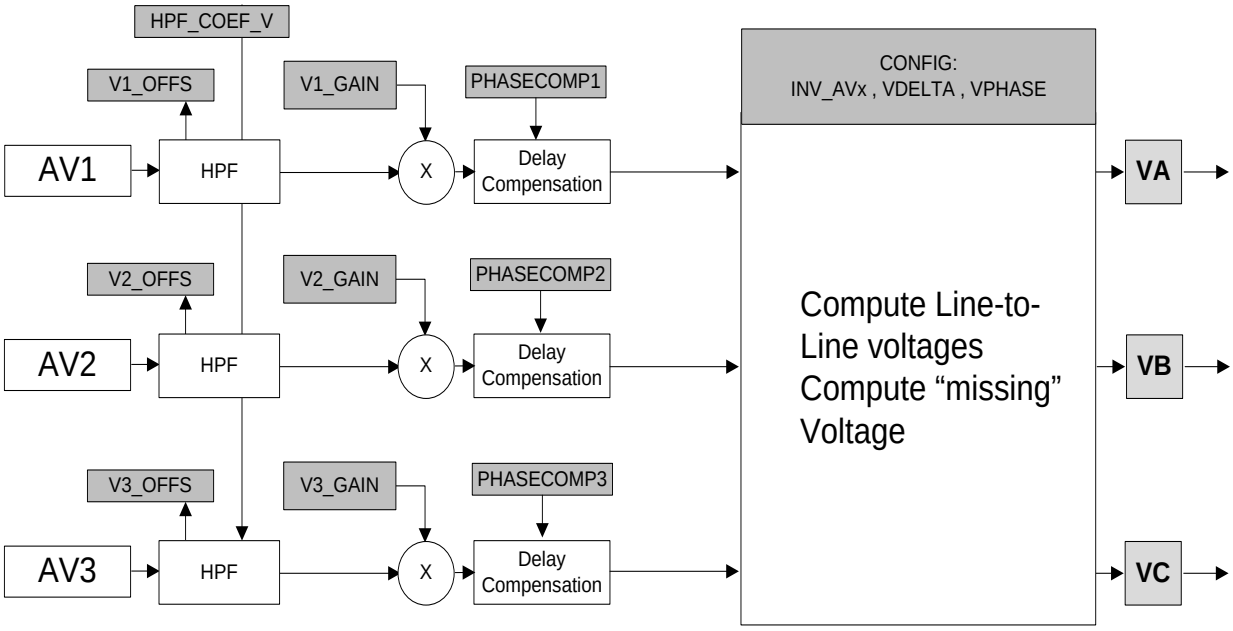
VDELTA	VPHASE	Voltage equations
0	00	VA, VB and VC measured on AV1, AV2 and AV3 inputs
0	01	VB and VC measured on AV2 and AV3 VA = VC - VB
0	10	VA and VC measured on AV1 and AV3 VB = VA - VC
0	11	VA and VB measured on AV1 and AV2 VC = VB - VA
1	00	Compute Line-to-Line voltages at high-rate VA ⇐ VC – VA = VCA VB ⇐ VA – VB = VAB VC ⇐ VB – VC = VBC
1	01 10 11	Invalid settings

Note: **INV_AVx** settings are applied before these computations

The Applications Examples section provides the required settings for the different configurations.

Voltage Input Flowchart

The figure below illustrates the computational flowchart for VA, VB, and VC. The values for the voltage input configuration register can be saved in flash memory and automatically restored at power-on or reset.



Current Input Configuration

The MAX78630+PPM supports multiple analog input configurations for determining the currents in a three-phase system. The CONFIG register is used to instruct the MAX78630+PPM how to compute them.

CONFIG Bits	Name	Function
2	INEUTRAL	Configuration uses a current sensor in the Neutral conductor. This sensor replaces the missing sensor (see IPHASE setting)
1:0	IPHASE	Missing sensor on current input 00: none missing 01: AI1 10: AI2 11: AI3

The IPHASE setting determines how many line current sensors are present, and for which phases. If three sensors are used, these bits should be set to zero. If two sensors are used, settings 01, 10 and 11 indicate the phase without a line current sensor. The current for this phase will then be computed according to the INEUTRAL and VDELTA settings. If VDELTA is cleared and IN can be assumed to be zero, the current is computed such that IA+IB+IC = 0. If VDELTA is set, the current in this phase is the difference between the two other currents (INEUTRAL must be cleared in these two cases).

When the INEUTRAL bit is set, a sensor in the neutral conductor replaces one of the three line current sensors. IN is directly measured from a sensor placed in the neutral conductor and the MAX78630+PPM calculates the current for the input with no line current sensor, such that IA+IB+IC = IN (IPHASE cannot be 00).

INEUTRAL	IPHASE	Current equations
0	00	IA, IB and IC measured on AI1, AI2 and AI3 inputs
0	01	IB and IC measured on AI2 and AI3 if VDELTA = 0 ⇨ IA = -(IB + IC) if VDELTA = 1 ⇨ IA = IB - IC
0	10	IA and IC measured on AI1 and AI3 if VDELTA = 0 ⇨ IB = -(IC + IA) if VDELTA = 1 ⇨ IB = IC – IA
0	11	IA and IB measured on AI1 and AI2 if VDELTA = 0 ⇨ IC = -(IA + IB) if VDELTA = 1 ⇨ IC = IA - IB
1	00	Invalid setting
1	01	IB and IC measured on AI2 and AI3 IN measured on AI1 IA = IN - (IB + IC)
1	10	IA and IC measured on AI1 and AI3 IN measured on AI2 IB = IN - (IC + IA)
1	11	IA and IB measured on AI1 and AI2 IN measured on AI3 IC = IN - (IA + IB)

The Applications Examples section provides the required settings for different configurations.

Pre-amp

By default, the full-scale signal that can be applied to the current inputs is V_{3P3A} ±250mVpk (176.78mV_{RMS}). This setting provides the widest dynamic range and is recommended for most applications.

For applications requiring a much lower value shunt resistor, an optional pre-amplifier with an 8x gain is included for the current inputs. The maximum input signal that can be applied to the current inputs in this case is ±31.25mVpk.

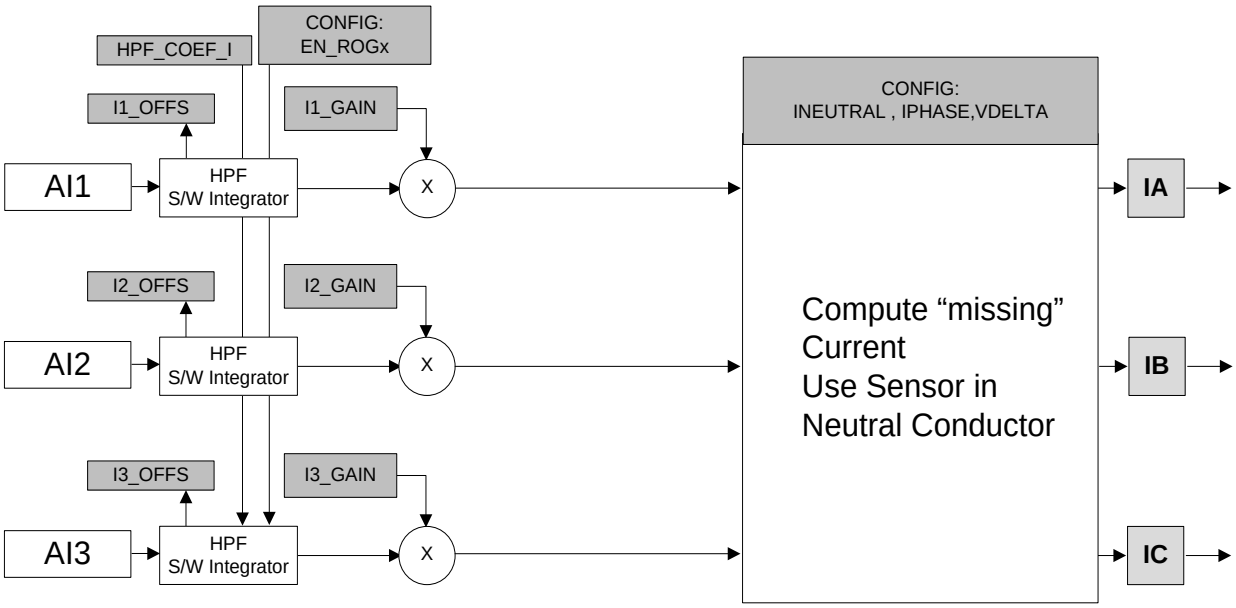
The CONFIG register is used to enable the Pre-amp.

CONFIG Bits	Name	Function
9	EN_PREAMPC	Enables the Pre-amp on input AIC
11	EN_PREAMPB	Enables the Pre-amp on input AIB
13	EN_PREAMPA	Enables the Pre-amp on input AIA

The gain is set by a ratio of internal resistors with one of the resistors in series from the input pad to the pre-amp itself. As such, the device must only be directly connected to a shunt with minimal resistance when using the pre-amp.

Current Input Flowchart

The figure below illustrates the computational flowchart for IA, IB and IC. The values for current input configuration register can be saved in flash memory and automatically restored at power-on or reset.



Data Refresh Rates

Instantaneous voltage and current measurement results are updated at the sample rate of 2.7kS/s and are generally not useful unless accessed with a high speed interface such as SPI. The CYCLE register is a 24-bit counter that increments every high-rate sample update and resets when low rate results are updated.

Low rate results, updated at a user configurable rate (also referred to as accumulation interval), are typically used and more suitable for most applications. The FRAME register is a counter that increments every accumulation interval. A data ready indicator in the STATUS register indicates when new data is available. Optionally, this indicator can be made available as a signal on one of the five Alarm output pins.

The high rate samples in one accumulation interval are averaged to produce a low-rate result, increasing their accuracy and repeatability. Low rate results include RMS voltages and currents, frequency, power, energy, and power factor. The accumulation interval can be based on a fixed number of ADC samples or locked to the incoming line voltage cycles.

If Line Lock is disabled, the accumulation interval defaults to a fixed time interval defined by the number of samples defined in the SAMPLES register (default of 540 samples or 0.2 seconds).

When the Line-Lock bit in the Command Register is set, and a valid AC voltage signal is present, the actual accumulation interval is stretched to the next positive zero crossing of the reference line voltage after the defined number of samples has been reached. If there is not a valid AC signal present and line lock is enabled, there is a 100 sample timeout implemented that would limit the accumulation interval to SAMPLES+100.

The DIVISOR register records the actual duration (number of high rate samples) of the last low rate interval whether or not Line-Lock is enabled.

Zero-crossing detection and line frequency for the purpose of determining the accumulation interval are derived from a composite signal $V_{ZC} = VA - 0.5 \cdot VB - 0.25 \cdot VC$. For a three-phase system, this signal oscillates at the line frequency as long as any of the three voltages is present.

Scaling Registers and Result Formats

All voltage, current and power data is reported in binary full-scale units with a value range of -1.0 to 1.0 less one LSB (S.23 format). For voltages and currents, all full scale register readings correspond to the max analog input of 250mVpk (or 31.25mVpk with 8x gain from the pre-amp). As an example, if 230V-peak at the input to the voltage-divider gives 250mV-peak at the chip input, one would get a full scale register reading of 1.0-LSB for instantaneous voltage. Similarly, if 30A at the sensor input provides 250mV to the chip input, a full scale register value of 1.0-1LSB for instantaneous current would correspond to 30A. Full scale power corresponds to the result of full scale current and voltage so in this example, full scale watts is 230 x 30 or 6900 watts.

Power Factors are reported as binary fixed-point number, with a range of -2 to +2 less one LSB (format S.22). Crest Factors are reported as binary fixed-point numbers, with a range of 0 to +256 less one LSB (format S.16).

Frequency data is reported as binary fixed-point number, with a range of 0 to +256Hz less one LSB (format S.16). Temperature data has a fixed scaling with a range of -16384°C to +16384°C less one LSB (format S.10). Energy data scaling is described in a different section of this document.

Nonvolatile registers (IFSCALE and VFSCALE) are provided for storing the real-world current and voltage levels that apply to the full scale register readings for any given board design. Any host application can then format the measurement results to any data format as needed. The usage of these nonvolatile scratchpad registers is user defined and their content has no effect on the internal operations of the device.

Calibration

The MAX78630+PPM provides integrated calibration routines to modify gain and offset coefficients. The user can setup and initiate a calibration routine through the Command Register. On a successful calibration, the command bits are cleared in the Command Register, leaving only the system setup bits. In case of a failed calibration, the bit in the Command Register corresponding to the failed calibration is left set. When in calibration mode, the line-lock bit should be set for best results.

The calibration routines will write the new coefficients to the relevant registers. The user can then save the new coefficients into flash memory as defaults using the flash access command in the Command Register.

See the Command Register section for more information on using commands.

Voltage and Current Gain Calibration

In order to calibrate the gain parameters for voltage and current channels, a reference AC signal must be applied to the channel to be calibrated. The RMS value corresponding to the applied reference signal must be entered in the relevant target register (V_TARGET, I_TARGET). Considering calibration is done with low rate RMS results, the value of the target register should never be set to a value above 70.7% of full-scale.

Initially, the value of the gain is set to unity for the selected channels. RMS values are then calculated on all inputs and averaged over the number of measurement cycles set by the CALCYCS register. The new gain is calculated by dividing the appropriate Target register value by the averaged measured value. The new gain is then written to the select Gain registers unless an error occurred.

Note that there is only one V_TARGET register for voltages. It is possible to calibrate multiple or all voltage channels simultaneously, if and only if the same RMS voltage value is applied to each corresponding input. Analogous considerations apply to the current channels, which are calibrated via the I_TARGET register.

Offset Calibration

To calibrate offset, all signals should be removed from all analog inputs although it is possible to do the calibration in the presence of AC signals. In the command, the user also specifies which channel(s) to calibrate. Target registers are not used for Offset calibration.

During the calibration process, each input is accumulated over the entire calibration interval as specified by the CALCYCS register. The result is divided by the total number of samples and written to the appropriate offset register, if selected in the calibration command. Using the Offset Calibration command will set the respective HPF coefficients to zero thereby fixing the offset registers to their calibrated values.

Die Temperature Calibration

To re-calibrate the on-chip temperature sensor offset, the user must first write the known chip temperature to the T_TARGET register. Next, the user initiates the Temperature Calibration Command in the Command Register. This will update the T_OFFS offset parameter with a new offset based on the known temperature supplied by the user. The T_GAIN gain register is set by the factory and not updated with this routine.

Voltage Channel Measurements

Instantaneous voltage measurements are updated every sample, while RMS voltages are updated every accumulation interval (n samples).

Register	Description	Time Scale
VA VB VC	Instantaneous Voltage @ time t	1 sample
VA_RMS VB_RMS VC_RMS	RMS Voltage of last interval	1 interval
VT_RMS	Average of VA_RMS, VB_RMS, VC_RMS	

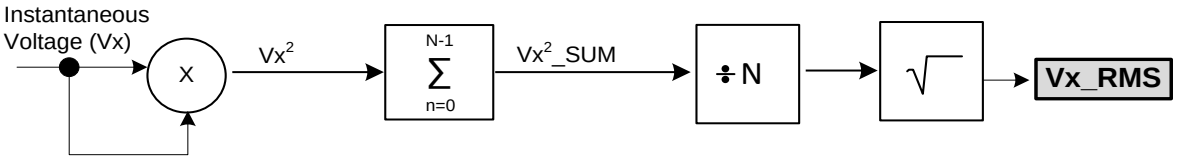
Note that the VDELTA and VPHASE settings in the CONFIG register affect how the instantaneous and averaged values are computed as described in the Voltage Input Configuration section.

Additionally, an AC voltage frequency measurement is also available and is updated every 64 line cycles.

Register	Description	Time Scale
FREQ	AC Voltage Frequency	64 voltage line cycles

RMS Voltage

The MAX78630+PPM reports true RMS measurements for each input. An RMS value is obtained by performing the sum of the squares of instantaneous values over a time interval (accumulation interval) and then performing a square root of the result after dividing by the number of samples in the interval.



Line Frequency

This output is a measurement of the fundamental frequency of the AC voltage source. It is derived from a composite signal and therefore applies to all three phases (it is a single reading per device).

Current Channel Measurements

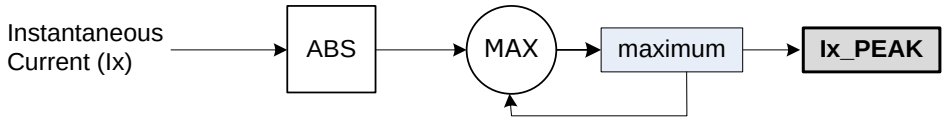
Instantaneous current measurements are updated every sample, while peak currents and RMS currents are updated every accumulation interval (n samples).

Register	Description	Time Scale
IA IB IC	Instantaneous Current	1 sample
IA_PEAK IB_PEAK IC_PEAK	Peak Current	1 interval
IA_RMS IB_RMS IC_RMS	RMS Current	
IT_RMS	Average of IA_RMS, IB_RMS, IC_RMS	

Note that the INEUTRAL and IPHASE settings in the CONFIG register affect how the instantaneous and averaged values are computed as described in the Current Input Configuration section.

Peak Current

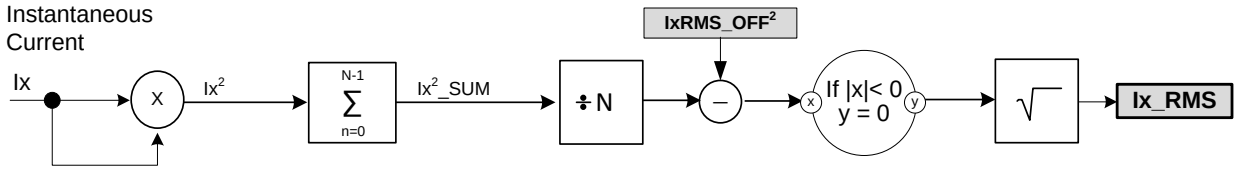
This output is a capture of the largest magnitude instantaneous current load sample.



RMS Current

The MAX78630+PPM reports true RMS measurements for current inputs. The RMS current is obtained by performing the sum of the squares of the instantaneous voltage samples over the accumulation interval and then performing a square root of the result after dividing by the number of samples in the interval.

An optional “RMS offset” for the current channels can be adjusted to reduce errors due to noise or system offsets (crosstalk) exhibited at low input amplitudes. Full scale values in the IxRMS_OFFS registers are squared and subtracted from the accumulated/divided squares. If the resulting RMS value is negative, zero is used.



Current and Voltage Imbalance

Imbalance of a three-phase system is typically defined as the percentage of the maximum deviation of any of the phases from the average of the phases.

Voltage imbalance is obtained from Vx_RMS and VT_RMS as

$$VIMBAL\% = \frac{\max\{|VARMS - VTRMS|, |VBRMS - VTRMS|, |VCRMS - VTRMS|\}}{VTRMS} \cdot 100$$

Current imbalance is obtained from Ix_RMS and IT_RMS as

$$IIMBAL\% = \frac{\max\{|IARMS - ITRMS|, |IBRMS - ITRMS|, |ICRMS - ITRMS|\}}{ITRMS} \cdot 100$$

The MAX78630+PPM monitors the deviation of any phase from the average value. It generates an alarm if the deviation exceeds user programmable threshold; V_IMB_MAX for voltages and I_IMB_MAX for currents.
The thresholds are expressed as binary full-scale units with a value range of 0.0 to 1.0 less one LSB (S.23 format). 1.0 thus corresponds to 100% imbalance.

Example: generate an alarm if voltage imbalance exceeds 1.5%.

$$\mathrm{V_{IMB_{MAX}}} = \mathrm{int}\left(\frac{1.5}{100} \cdot 2^{23}\right) = 125{,}829 = \mathrm{0x1EB85}$$

Power Calculations

This section describes the detailed flow of power calculations in the MAX78630+PPM. The table below lists the available measurement results for AC power.

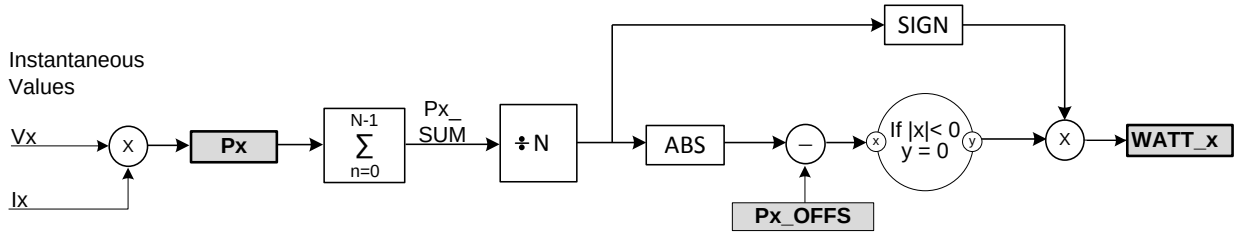
Register	Description	Time Scale
WATT_A WATT_B WATT_C	Average Active Power (P)	1 interval
VAR_A VAR_B VAR_C	Average Reactive Power (Q)	
VA_A VA_B VA_C	Apparent Power (S)	
PF_A PF_B PF_C	Power Factor	
WATT_T	Average of WATT_A, WATT_B, WATT_C	
VAR_T	Average of VAR_A, VAR_B, VAR_C	
VA_T	**1** Average of VA_A, VA_B, VA_C	
PF_T	Total power factor: Equal to WATT_T / VA_T	

Note that the voltage and current configuration settings in the CONFIG register affect the physical meaning of the computed power results. The Applications Examples section provides further details on these results.

Active Power (P)

The instantaneous power results (PA, PB, PC) are obtained by multiplying aligned instantaneous voltage and current samples. The sum of these results are then averaged over N samples (accumulation time) to compute the average active power (WATT_A, WATT_B, WATT_C).

The value in the Px_OFFS register is the “Power Offset” for the power calculations. Full scale values in the Px_OFFS register are subtracted from the magnitude of the averaged active power. If the resulting active power value results in a sign change, zero watts are reported



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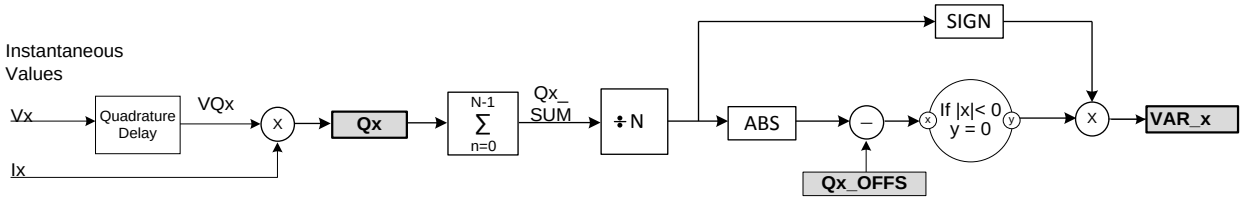
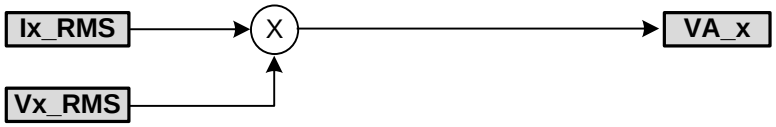
Reactive Power (Q)

Instantaneous reactive power results are calculated by multiplying the instantaneous samples of current and the instantaneous quadrature voltage. The sum of these results are then averaged over N samples (accumulation time) to compute the average reactive power (VAR_A, VAR_B, VAR_C). A reactive power offset (Qx_OFFS) is also provided for each channel.



Apparent Power (S)

The apparent power, also referred as Volt-Amps, is the product of low rate RMS voltage and current results. Offsets applied to RMS current will affect apparent power results.



Power Factor (PF)

The power factor registers capture the ratio of active power to apparent power for the most recent accumulation interval. The sign of power factor is determined by the sign of active power.

$$\mathrm{PF\_x} = \frac{\mathrm{WATT\_x}}{\mathrm{VA\_x}}$$

Totals of Active Power, Reactive Power, Apparent Power, and Power Factor

The total power results in a three-phase system depend on how the AC source, the load and the sensors are configured. As an example, in Wye connected systems, the totals are computed as the sum of all three per-phase results. In many Delta configurations, the total power is the sum of two “per-phase” results only, and the third per-phase result must be ignored. The MAX78630+PPM requires a setting to indicate how the totals are to be computed. The PPHASE bits in the CONFIG register serve this purpose.

CONFIG Bits	Name	Function
7:6	PPHASE	Ignore phase for total power computations 00: none 01: phase A 10: phase B 11: phase C

When PPHASE is not 00, the MAX78630 will compute the totals of two phases only, as is typically done when only line currents are available in a Delta-connected load. In such cases, the total apparent power is correctly scaled by a factor of $\sqrt{3}/2$. In order to prevent overflows, all totals are computed as averages and must be multiplied by two by the host.
When PPHASE is equal to 00, all totals are computed as averages and must be multiplied by three by the host.

PPHASE	Total Active Power	Total Reactive Power	Total Apparent Power
	$\mathrm{WATT\_T} =$	$\mathrm{VAR\_T} =$	$\mathrm{VA\_T} =$
00	$\frac{(\mathrm{WATT\_A} + \mathrm{WATT\_B} + \mathrm{WATT\_C})}{3}$	$\frac{(\mathrm{VAR\_A} + \mathrm{VAR\_B} + \mathrm{VAR\_C})}{3}$	$\frac{(\mathrm{VA\_A} + \mathrm{VA\_B} + \mathrm{VA\_C})}{3}$
01	$\frac{(\mathrm{WATT\_B} + \mathrm{WATT\_C})}{2}$	$\frac{(\mathrm{VAR\_B} + \mathrm{VAR\_C})}{2}$	$\frac{\sqrt{3}}{2} \cdot \frac{(\mathrm{VA\_B} + \mathrm{VA\_C})}{2}$
10	$\frac{(\mathrm{WATT\_A} + \mathrm{WATT\_C})}{2}$	$\frac{(\mathrm{VAR\_A} + \mathrm{VAR\_C})}{2}$	$\frac{\sqrt{3}}{2} \cdot \frac{(\mathrm{VA\_A} + \mathrm{VA\_C})}{2}$
11	$\frac{(\mathrm{WATT\_A} + \mathrm{WATT\_B})}{2}$	$\frac{(\mathrm{VAR\_A} + \mathrm{VAR\_B})}{2}$	$\frac{\sqrt{3}}{2} \cdot \frac{(\mathrm{VA\_A} + \mathrm{VA\_B})}{2}$

The total power factor is computed as

$$\mathrm{PF\_T} = \frac{\mathrm{WATT\_T}}{\mathrm{VA\_T}}$$

Specific examples and the required settings are further described in the Applications Examples section.

Fundamental and Harmonic Calculations

The MAX78630+PPM includes the ability to separate low rate voltage, current, active power, and reactive power measurement results into fundamental and total harmonic components. These outputs can also be used to track individual harmonics as well as the total value excluding the selected harmonic.

Register	Description	Time Scale
VFUND_A VFUND_B VFUND_C	Voltage content at specified harmonic	1 interval
IFUND_A IFUND_B IFUND_C	Current content at specified harmonic	
PFUND_A PFUND_B PFUND_C	Active Power content at specified harmonic	
QFUND_A QFUND_B QFUND_C	Reactive Power content at specified harmonic	
VHARM_A VHARM_B VHARM_C	Voltage content not at specified harmonic	
IHARM_A IHARM_B IHARM_C	Current content not at specified harmonic	
PHARM_A PHARM_B PHARM_C	Active Power content not at specified harmonic	
QHARM_A QHARM_B QHARM_C	Reactive Power content not at specified harmonic	

The HARM register is used to select the single harmonic to extract. This input register is set by default to 0x000001 selecting the first harmonic (also known as the fundamental frequency). This setting provides the user with fundamental result and the total harmonic distortion (THD) of the harmonics

By setting the value in the HARM register to a higher harmonic, the fundamental result registers will contain measurement results of the selected harmonic. The harmonics result registers will report the measurement of the remaining harmonics. For any given accumulation interval, the magnitude of measurement result IA_RMS would be the sum of IFUND_A and IHARM_A.

Energy Calculations

Energy calculations are included in the MAX78630+PPM to minimize the traffic on the host interface and simplify system design. Low rate power measurement results are multiplied by the number of samples (register DIVISOR) to calculate the energy in the last accumulation interval. Energy results are summed together until a user defined “bucket size” is reached. For every bucket of energy is reached, the value in the energy counter register is incremented by one.

All energy counter registers are low rate 24-bit output registers that contain values calculated over multiple accumulation intervals. Both import (positive) and export (negative) results are provided for active and reactive energy.

Register	Description
WHA_POS WHB_POS WHC_POS	Positive Active Energy Counter, per phase
WHA_NEG WHB_NEG WHC_NEG	Negative Active Energy Counter, per phase
VARHA_POS VARHB_POS VARHC_POS	Positive Reactive Energy Counter, per phase
VARHA_NEG VARHB_NEG VARHC_NEG	Negative Reactive Energy Counter, per phase

Energy results are cleared upon any power down or reset and can be manually cleared by the external host using the REN bit in the COMMAND register. The CYCLES register can be used to detect device resets (loss of energy data) or to track time between energy reads.

Bucket Size for Energy Counters

The BUCKET register allows the user to define the unit of measure for the energy counter registers. It is an unsigned 48-bit fixed-point number with 24 bits for the integer part and 24 bits for the fractional part.

	High word							Low word					
Bit Position	23	22	…	2	1	0	.	23	22	21	…	1	0
Value	2^{23}	2^{22}	…	23^{2}	2^{1}	2^{0}		2^{-1}	2^{-2}	2^{-3}	…	2^{-23}	2^{-24}

The units should be set large enough to keep the accumulators and counters from overflowing too quickly. To increment the energy counters in watt-hours for example, the value in BUCKET should be equal to the number of seconds in an hour (3600) multiplied by the Sample Rate (2.7kS/s) and divided by Full Scale Watts (VSCALE x ISCALE).

Watt-hours (Wh) Bucket = (3600s x 2.7kS/s) / (VSCALE x ISCALE)

Full Scale Watts is defined by the sensors being used (see the Scaling Registers section). As an example, if the voltage sources are 400Vpk at full scale (VSCALE) and the currents are 30Apk at full scale (ISCALE), then full scale watts would be 12000 (VSCALE x ISCALE). The bucket value can be saved to flash memory as the register default.

Examples:
For the ISCALE and VSCALE values given above, a:

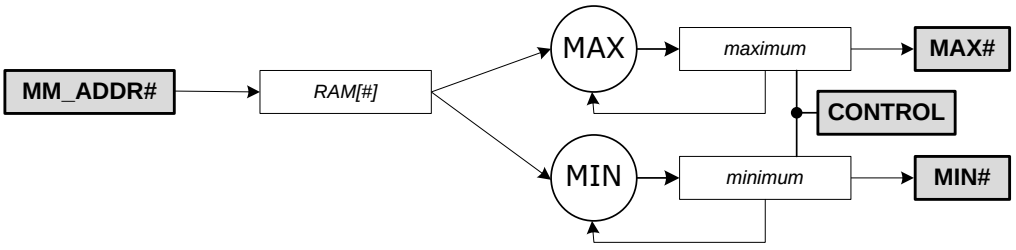
1. Watt-hour bucket equals to 3600*2700/ (400*30) = 810. The hexadecimal value that must be written to the BUCKET register is, after shifting 24 bits (multiplying by 2^{23}) to the left to align with the integer part: BUCKET = 0x00032A.000000
2. kilo-Watt-hour bucket equals to 3600*2700/ (400*30/1000) = 810000. The hexadecimal value that must be written to the BUCKET register is, after shifting 24 bits (multiplying by 2^{24}) to the left to align with the integer part: BUCKET = 0x0C5C10.000000

Min/Max Tracking

The MAX78630+PPM provides a set of output registers for tracking the minimum and/or maximum values of up to eight (8) different low rate measurement results over multiple accumulation intervals .
The user can select which measurements to track through an address table. The values in MM_ADDR# are word addresses for all host interfaces and can be saved to flash memory by the user as the register defaults. Results are stored in RAM and cleared upon any power down or reset and can be cleared by the host using the RTRK bit in the COMMAND register.

Register	Description	Time Scale
MM_ADDR0	Word addresses to track minimum and maximum values. A value of zero disables tracking for that address slot.	–
MM_ADDR1		
MM_ADDR2		
MM_ADDR3		
MM_ADDR4		
*MM_ADDR5		
*MM_ADDR6		
*MM_ADDR7		
MIN0	Minimum low rate value at MM_ADDR#.	multiple intervals
MIN1		
MIN2		
MIN3		
MIN4		
*MIN5		
*MIN6		
*MIN7		
MAX0	Maximum low rate value at MM_ADDR#.	multiple intervals
MAX1		
MAX2		
MAX3		
MAX4		
*MAX5		
*MAX6		
*MAX7		

*NOTE: When using Rogowski coils, restriction on the use of MIN/MAX functionality apply. For each current input with a Rogowski coil sensor, one of the MIN/MAX registers 5, 6 and 7 cannot be used to track minima and maxima. See the Register Locations section for more details.



Voltage Sag Detection

The MAX78630+PPM implements a voltage sag detection function for each of the three phases. When a phase voltage drops below a programmable threshold, a corresponding alarm is generated.

The firmware computes the following indicator to detect whether the voltage falls below the threshold.

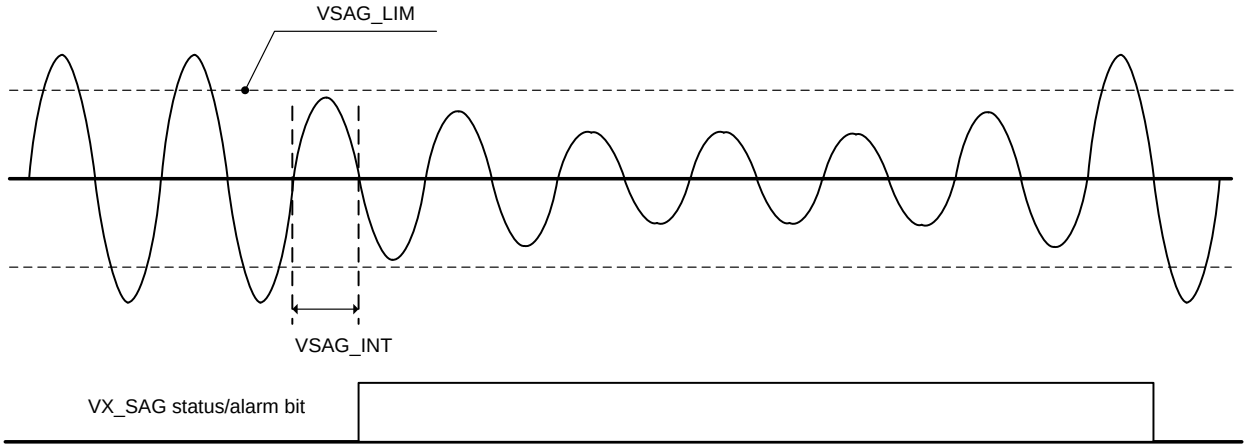
$$V_{SAGX} = \sum_{n=0}^{VSAG\_INT-1} (v_{Xn}{}^2 - VSAG\_LIM^2)$$

where

- VSAG_LIM is the user-settable RMS value of the voltage threshold
- VSAG_INT is the user-settable number of high-rate samples over which the indicators should be computed. For optimal performance, this should be set so that the resulting interval is an integer multiple of the line period (at least one half line period)
- X is the phase (A,B,C)

If V_{SAGX} becomes negative, the firmware sets the VX_SAG bit for the corresponding phase in the STATUS register. If VX_SAG is enabled in a MASK register, the corresponding AL pin will also be asserted low. If the VX_SAG bit is set in the STICKY register, then the alarm bit will remain set and any unmasked AL pin will remain low until the VX_SAG alarm is cleared via the STATUS_CLEAR register or the MAX78630+PPM is reset. If the VX_SAG bit is cleared in the STICKY register, then the alarm bit will be automatically cleared and any unmasked AL pin set high as soon as the indicator V_{SAGX} is greater than the programmable threshold.

The sag detection can be used to monitor or record the quality of the power line or utilize the sag alarm pin to notify external devices (for example a host microprocessor) of a pending power-down. The external device can then enter a power-down mode (for example saving data or recording the event) before a Power outage. The figure below shows a SAG event and how the alarm bit is set by the firmware (in the case of the STICKY register bit cleared).



Example:

Set the detection interval to one-half of a line cycle (60Hz line frequency).

$$VSAG\_INT = \frac{T_{line}}{2} \Big/ \frac{1}{f_{sample}} = \frac{f_{sample}}{2f_{line}} = \frac{2700}{2 \cdot 60} = 22$$

Voltage Sign Outputs

The MAX78630+PPM can optionally output the sign of the phase or line voltages VA, VB, VC on dedicated DIO pins. This functionality is enabled individually for each phase by setting the VSGNA, VSGNB and VSGNC bits in the CONFIG register. If a VSGNx bit is set, the sign of the voltage Vx drives the state of the corresponding SGNVx digital output pin. The time delay of the sign output versus the sign of the actual voltage is approximately 1.20ms. Resetting a VSGNx bit disables this functionality and makes the corresponding DIO pin available as a general purpose input/output.

Alarm Monitoring

Low rate alarm conditions are determined every accumulation interval. If results for Die Temperature, AC Frequency, or RMS Voltage exceeds or drops below user configurable thresholds, then a respective alarm bit in the STATUS register is set. For RMS Current results, a maximum threshold is provided for detecting over current conditions with the load. For Power Factor results, a minimum threshold is provided.

Register	Description
T_MAX	Threshold value which Temperature must exceed to trigger alarm.
T_MIN	Threshold value which Temperature must drop below to trigger alarm.
F_MAX	Threshold value which Frequency must exceed to trigger alarm.
F_MIN	Threshold value which Frequency must drop below to trigger alarm.
VRMS_MAX	Threshold value which RMS Voltage must exceed to trigger alarm.
VRMS_MIN	Threshold value which RMS Voltage must drop below to trigger alarm.
IRMS_MAX	Threshold value which RMS current must exceed to trigger alarm.
PF_MIN	Threshold value which power factor must drop below to trigger alarm.

Imbalance of the three voltages and three currents is monitored and reported via dedicated alarm bits if they exceed respective maximum threshold V_IMB_MAX and I_IMB_MAX. Refer to the Current and Voltage Imbalance section or details.

Register	Description
V_IMB_MAX	Percentage Threshold value which Voltage Imbalance must exceed to trigger alarm.
I_IMB_MAX	Percentage Threshold value which Current Imbalance must exceed to trigger alarm.

The STATUS register also provides Sag voltage alarms. A configurable RMS voltage threshold and selectable Interval is provided as described below and in the Voltage Sag Detection section.

Register	Description
VSAG_LIM	Threshold value (in RMS) which voltage must go below to trigger a Sag alarm.
VSAG_INT	Interval (in samples) over which the voltage must be below the threshold. Should be set in increments of half cycles (i.e. 22 samples per half cycle at 60Hz).

Status Registers

The STATUS register is used to monitor the status of the device and user configurable alarms. All other registers mentioned in this section share the same bit descriptions.

The STICKY register determines which alarm/status bits are sticky and which track the current status of the condition. Each alarm bit defined as sticky will (once triggered) hold its alarm status until the user clears it using the STATUS_RESET register. Any sticky bit not set will allow the respective status bit to clear when the condition clears.

The STATUS_SET and the STATUS_RESET registers allow the user to force status bits on or off respectively without fear of affecting unintended bits. A bit set in the STATUS_SET register will set the respective bit in the STATUS register and a bit set in the STATUS_RESET register will clear it. STATUS_SET and STATUS_RESET are both cleared after the status bit is set or reset.

The following table lists the bit mapping for the all status related registers.

Bit	Name	Stick-able?	Description
23	DRDY	Always	New low rate results (data) ready
22	OV_FREQ	Yes	Frequency over High Limit
21	UN_FREQ	Yes	Under Low Frequency Limit
20	OV_TEMP	Yes	Temperature over High Limit
19	UN_TEMP	Yes	Under Low Temperature Limit
18	OV_VRMSC	Yes	RMS Voltage C Over Limit
17	UN_VRMSC	Yes	RMS Voltage C Under Limit
16	OV_VRMSB	Yes	RMS Voltage B Over Limit
15	UN_VRMSB	Yes	RMS Voltage B Under Limit
14	OV_VRMSA	Yes	RMS Voltage A Over Limit
13	UN_VRMSA	Yes	RMS Voltage A Under Limit
12	UN_PFC	Yes	Power Factor C Under Limit
11	UN_PFB	Yes	Power Factor B Under Limit
10	UN_PFA	Yes	Power Factor A Under Limit
9	OV_IRMSC	Yes	RMS Current C Over Limit
8	OV_IRMSB	Yes	RMS Current B Over Limit
7	OV_IRMSA	Yes	RMS Current A Over Limit
6	VC_SAG	Yes	Voltage C Sag Condition Detected
5	VB_SAG	Yes	Voltage B Sag Condition Detected
4	VA_SAG	Yes	Voltage A Sag Condition Detected
3	V_IMBAL	Yes	Voltage Imbalance Detected
2	I_IMBAL	Yes	Current Imbalance Detected
1	XSTATE	No	External Oscillator is clocking source
0	RESET	Always	Set by device after any type of reset

Digital IO Functionality

The DIO_STATE register contains the current status of the DIOs. The user can use this register to read the state of a DIO (if configured as an input) or control the state of the DIO (if configured as an output).

NOTE: Some pins are used as serial interface pins and may not be capable of user control. During reset, all DIOs are configured as inputs.

Pin Name	DIO Bit	SPI	UART	I^2C	Alternate Function	MASK Register
AL1/DIO0	0	---			AL1	MASK1
SPCK/ADDR0/DIO1	1	SPCK	ADDR0	ADDR0	---	---
SDI/RX/SDAI/DIO2	2	SDI	RXD	SDAI	---	---
SDO/TX/SDAO/DIO3	3	SDO	TXD	SDAO	---	---
AL2/DIO4	4	---			AL2	MASK2
SSB/DIR/SCL//DIO5	5	SSB	RS485 DIR	SCL	---	---
AL3/ADDR1/DIO6	6	---	ADDR1	ADDR1	AL3	MASK3
AL4/DIO7	7	---			AL4	MASK4
IFC0/DIO8	8	IFC0 (at reset)			---	---
IFC1/DIO9	9	IFC1 (at reset)			---	---
AL5/DIO10	10	---			AL5	MASK5
SGNV1/DIO11	11	---			SGNV1	CONFIG
SGNV2/DIO12	12	---			SGNV2	CONFIG
SGNV3/DIO13	13	---			SGNV3	CONFIG
DIO14	14	---			---	---
DIO15	15	---			---	---

Interface configuration pins (IFC0, IFC1) and address pins (MP6/ADDR1, SPCK/ADDR0) are input pins sampled at the end of a reset to select the serial host interface and set device addresses (for I^2C and UART modes). If the IFC0 pin is low, the device will operate in the SPI mode. Otherwise, the state of IFC1 and the ADDR# pins determine the operating mode and device address.

> These pins MUST remain configured as an input if directly connecting to GND/V_{3P3D}. Otherwise, it is recommended to use external pull-up or pull-down resistors accordingly.

DIO Direction

The DIO_DIR register sets the direction of the pins, where “1” is input and “0” is output. The same bit definition as in the DIO_STATE register is used. If a DIO defined as an input is unconnected, internal pull-ups will assert the respective DIO bit in the DIO_STATE register.

DIO Polarity

DIOs configured as outputs are by default active LOW. The logic “0” state is ON. This can be modified using the DIO_POL register using the same bit definition as the DIO_STATE register. Any corresponding bit set in the DIO_POL register will invert the same DIO output so that it becomes active high.

Alarm Pins

The MAX78630+PPM provides five MASK registers for signaling the status of any STATUS bit to one of five Alarm (ALx) DIO pins. These MASK registers have the same bit mapping as the STATUS register. The user must first enable the respective ALx pin as an output before the DIO can be driven to its active state.

Pin Name	Register	Description
AL1	MASK1	A combination of a bit set in both the STATUS register and a MASK register causes the assigned ALx pin to be activated (default active-low).
AL2	MASK2	
AL3	MASK3	
AL4	MASK4	
AL5	MASK5	

Command Register

The Command Register is located at address 0x00. Use this register to perform specific tasks such as saving coefficients and nonvolatile register defaults into flash memory. It also allows initiation of integrated calibration routines.

VALUE (hex)	Description
00xxxx	Normal operation
CAxxxx/CBxxxx	Calibration commands
ACCxxx	Flash access commands

Normal Operation

The general settings command allows the user to enable functions such as Line Lock mode etc.

Bit(s)	Value	Description
23:16	0x00	“General settings” command used during normal operation.
7	REN	1= reset all energy accumulators. This bit automatically clears to zero when the reset completes.
6	RTRK	1= reset the minima and maxima registers for all monitored variables. This bit automatically clears to zero when the reset completes.
5	LL	Line Lock 1= lock to line cycle; 0= independent.
4	TC	Temperature Compensation. Should be set to “1” for proper operation.

Calibration Command

The Calibration Command starts the calibration process for the selected inputs. It is assumed that appropriate input signals and target values are applied. When a gain calibration process completes, bits 23:17 are cleared along with bits associated with channels that calibrated successfully. When an offset calibration completes, 23:17 are cleared but the corresponding offset bits will remain set.

Bit(s)	Value	Description
23:17	0x65	“Calibrate” Command.
16		1 = Calibrate Voltage for Phase C, 0 = no action
15		1 = Calibrate Voltage for Phase B, 0 = no action
14		1 = Calibrate Voltage for Phase A, 0 = no action
13		1 = Calibrate Current for Phase C, 0 = no action
12		1 = Calibrate Current for Phase B, 0 = no action
11		1 = Calibrate Current for Phase A, 0 = no action
10		1 = Calibrate Temperature, 0 = no action
9		Calibrate Offset versus Gain (0 = calibrate Gain; 1 = calibrate Offset)
5	LL	Lock Sample Period to Line Cycle.
4	TC	Temperature Compensation. Should be set to “1” for proper operation.

Note
During calibration, the “line-lock” bit should be set for best results.

Examples:

1) Calibrate gains of voltage and current of Phase A, with the “line-lock” bit set.
   Start Command: COMMAND = 0xCA.4830
   Successful Calibration: COMMAND is reset to 0x00.0030
   Calibration of current failed: COMMAND is reset to 0x00.0830

2) Calibrate gains of all three voltages, with the “line-lock” bit set
   Start Command: COMMAND = 0xCB.C030
   Successful Calibration: COMMAND is reset to 0x00.0030
   Calibration of voltages B and C failed: COMMAND is reset to 0x01.8030

Save to Flash Command

Use the ACC command to save to flash the calibration coefficients and defaults for nonvolatile registers. Upon reset or power-on, the values stored in flash will become new system defaults. The following table describes the ACC command bits:

Bit(s)	Value	Description
23:12	0xACC	“Access” Command.
11:8	0x2	2: Save defaults to flash memory for NV registers.
5	LL	Line Lock Bit.
4	1	Must be set to “1” for proper operation

Note that the LL bit (5) in this command will be stored into flash memory as well, so the desired behavior must be included.
After execution of this command, The MAX78630+PPM resets the COMMAND register bits [23:8] to zero.

Example:

Save all current settings to flash memory, to make then permanent. Operation after the next reset should be with LL bit set and TC cleared.

COMMAND = 0xAC.C230

After execution of this command, The MAX78630+PPM resets the COMMAND register to 0x00.0030.

Configuration Register

A CONFIG register is provided for system settings, such as sensor configuration, current sensor type, power computations and hardware gains.

Bit(s)	Name	Description
23	----	Reserved for future use, write as zeroes
22	INV_AV3	Invert voltage samples AV3
21	INV_AV2	Invert voltage samples AV2
20	INV_AV1	Invert voltage samples AV1
19	VSGNC	Drive SGNV3/DIO13 with sign of voltage C
18	VSGNB	Drive SGNV2/DIO12 with sign of voltage B
17	VSGNA	Drive SGNV1/DIO11 with sign of voltage A
16	EN_ROGC	Enable Software Integrator on Current input AI3
15	EN_ROGB	Enable Software Integrator on Current input AI2
14	EN_ROGA	Enable Software Integrator on Current input AI1
13	EN_PREAMPA	Enable Pre-Amp on Current input AI1
12	----	Reserved for future use, write as zero
11	EN_PREAMPB	Enable Pre-Amp on Current input AI2
10	----	Reserved for future use, write as zero
9	EN_PREAMPC	Enable Pre-Amp on Current input AI3
8	----	Reserved for future use, write as zero
7:6	PPHASE	Ignore phase for total power computations 00: none 01: phase A 10: phase B 11: phase C
5	VDELTA	Compute delta voltage between phases
4:3	VPHASE	Missing sensor on voltage input 00: none missing 01: AV1 10: AV2 11: AV3
2	INEUTRAL	Current sensor in neutral leg.
1:0	IPHASE	Missing sensor on current input 00: none missing 01: AI1 10: AI2 11: AI3

Application Examples

The MAX78630+PPM supports various three-phase topologies via appropriate setting of the CONFIG register. This section describes connection diagrams, firmware settings and output data. In the system diagrams the following convention is used:

- A current sensor is shown as
  - a shunt resistor, if a non-isolated measurement is taken
  - a transformer plus a burden resistor, if an isolated measurement is taken. The transformer depicts either a current transformer (CT) or a Rogowski-coil measurement. In the latter case, the burden resistor is not required and the EN_ROGx bit in the CONFIG register must be set accordingly.
- Voltage sensors are shown as
  - Resistor divider networks, if a non-isolated measurement is taken
  - Transformers, if an isolated measurement is taken.

Configuration diagrams are grouped into three main categories:

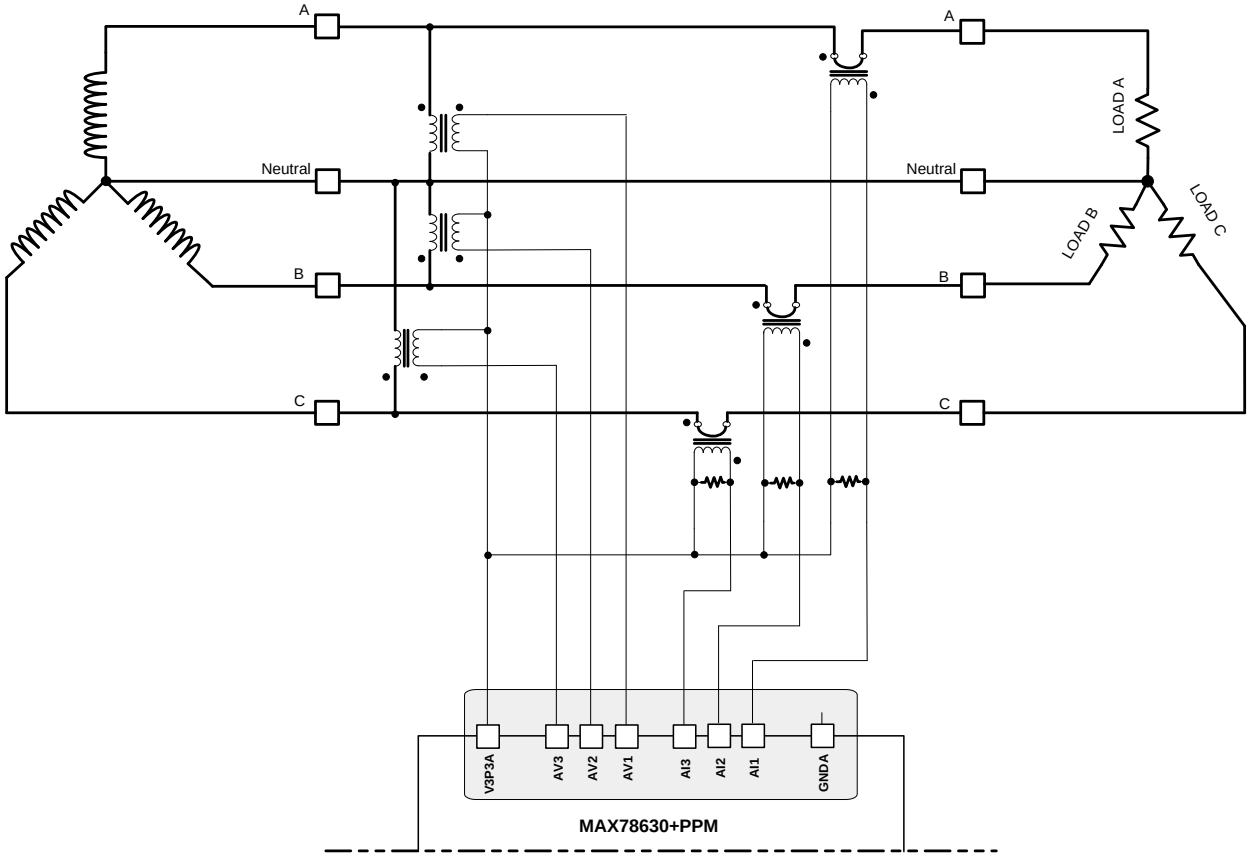
1) Wye-connected source, wye-connected load (Y-Y)
2) Delta-connected source, delta-connected load (Δ-Δ)
3) Wye-connected source, delta-connected load (Y-Δ)

Note: This section is intended to show combinations of configurations and sensors and to describe the settings and operation of the MAX78630+PPM. This list is not exhaustive.

Wye-Connected Source, Wye-Connected Load (Y-Y)

These configurations require measurement of all three phases (voltage and current) in order to determine the power. Therefore, six sensors are necessary.

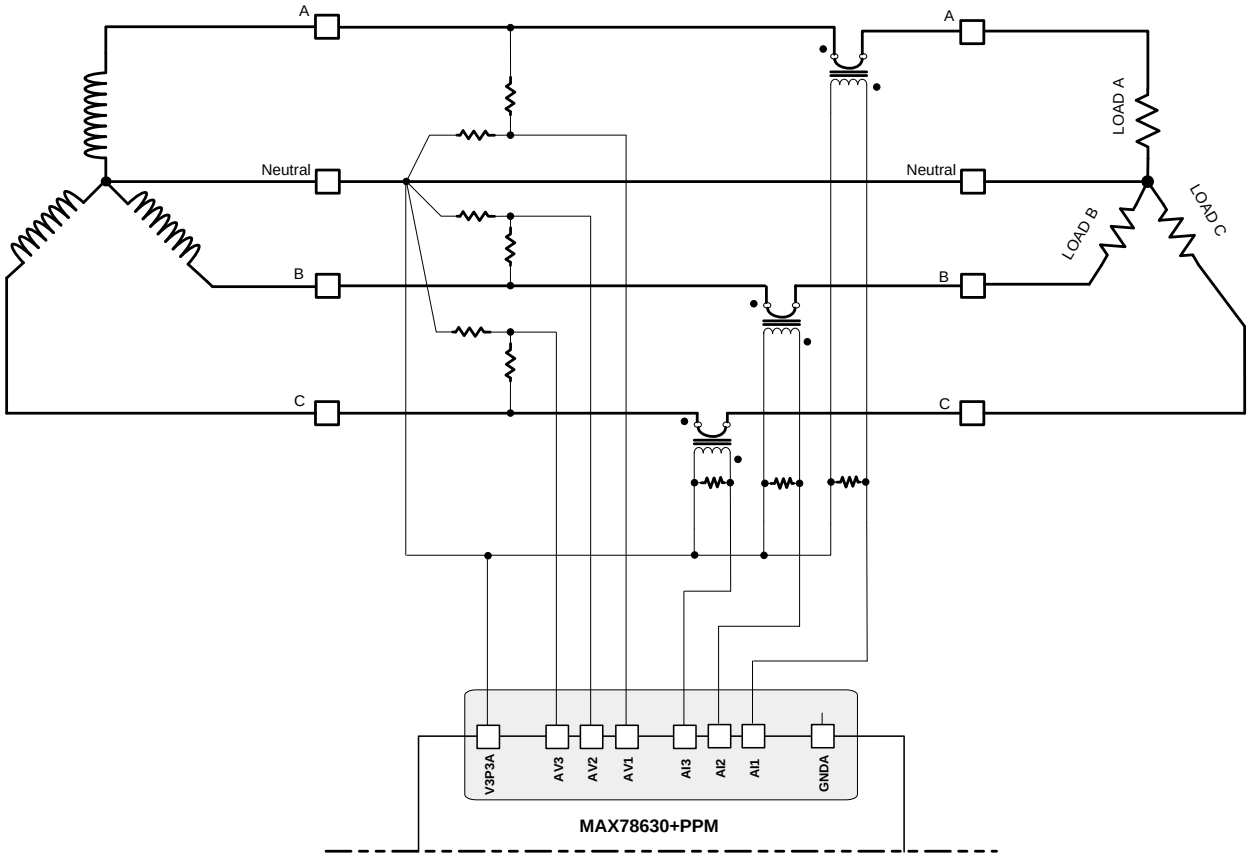
Isolated Configuration, 3 VTs, 3 CTs



CONFIG[22:20,7:0] hex 0XXX00	INV_AV[CBA]	PPHASE	VDELTA	VPHASE	INEUTRAL	IPHASE
	000	00	0	00	0	00

Outputs	Phase A	Phase B	Phase C	Total = Sum of	Comment
Voltages	VA	VB	VC	---	Line-To-Neutral Voltages
Currents	IA	IB	IC	---	Phase currents
Power (P, Q, S) computed from:	VA*IA	VB*IB	VC*IC	all three	

Non-Isolated Configuration, 3 Voltage-Dividers, 3 CTs

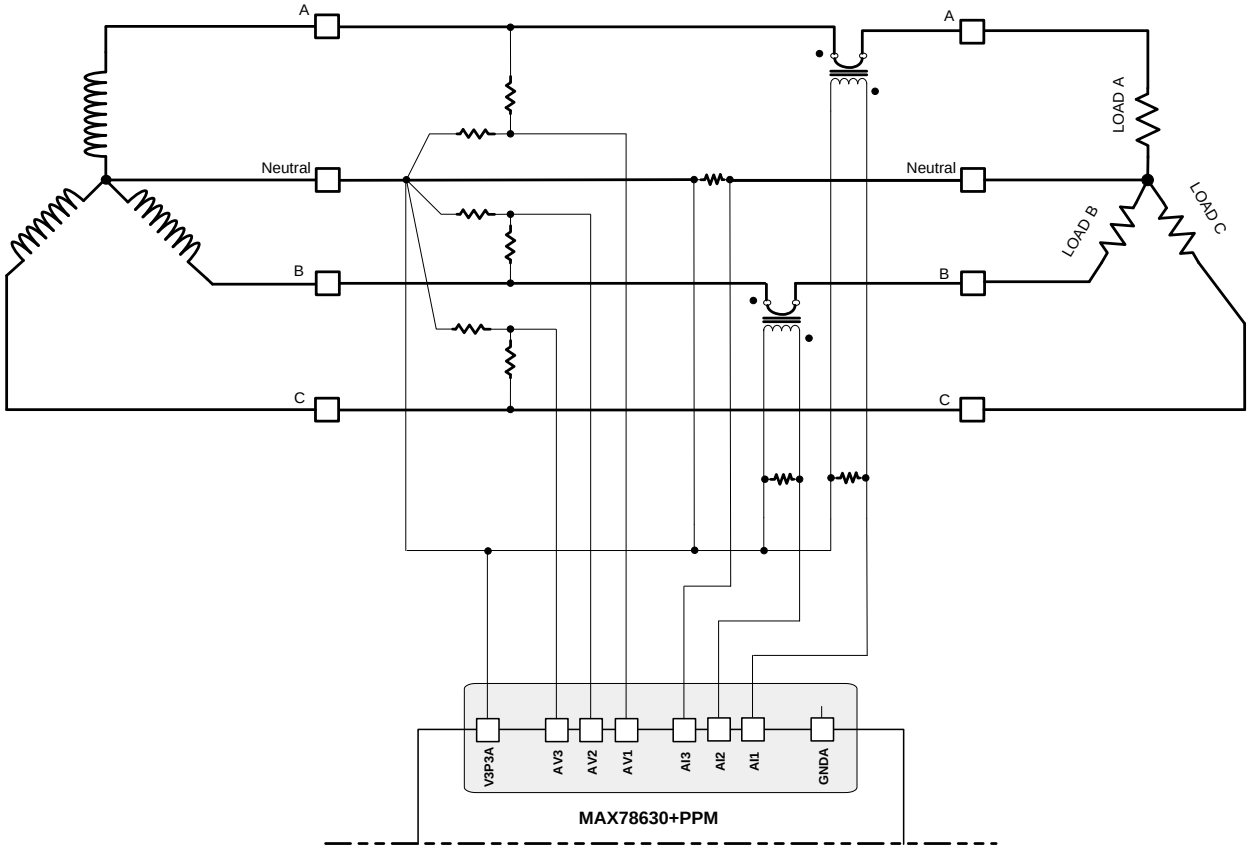


CONFIG[22:20,7:0] hex 0XXX00	INV_AV[CBA]	PPHASE	VDELTA	VPHASE	INEUTRAL	IPHASE
	000	00	0	00	0	00

Outputs	Phase A	Phase B	Phase C	Total = Sum of	Comment
Voltages	VA	VB	VC	---	Line-To-Neutral Voltages
Currents	IA	IB	IC	---	Phase currents
Power (P, Q, S) computed from:	VA*IA	VB*IB	VC*IC	all three	

Non-Isolated, 3 Voltage-Dividers, 2 CTs, 1 Shunt

This configuration eliminates one current transformer (phase C in the diagram) and replaces it with a shunt resistor in the neutral line.

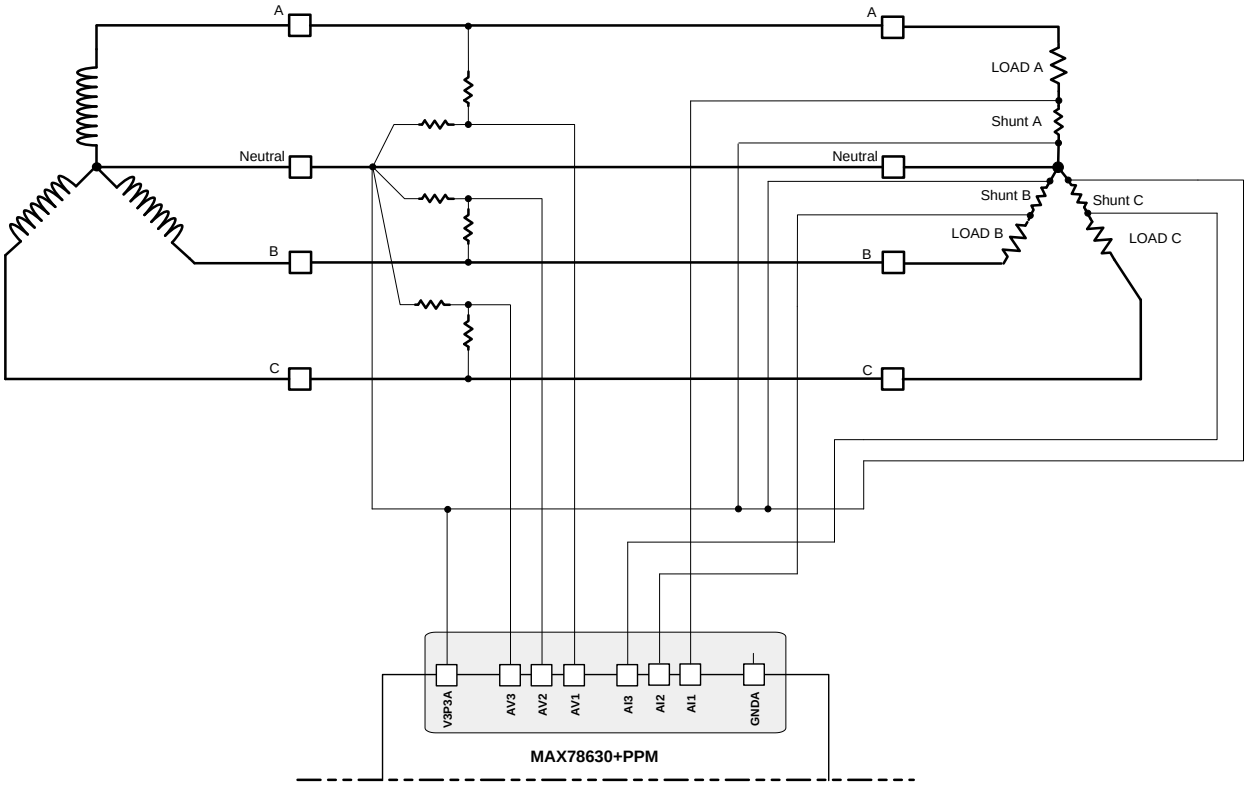


CONFIG[22:20,7:0] hex 0XXX07	INV_AV[CBA]	PPHASE	VDELTA	VPHASE	INEUTRAL	IPHASE
	000	00	0	00	1	11

Outputs	Phase A	Phase B	Phase C	Neutral	Total = Sum of	Comment
Voltages	VA	VB	VC	---	---	Line-To-Neutral Voltages
Currents	IA	IB	IC = IN – IA - IB	IN = measured from AIC	---	Phase currents
Power (P, Q, S) computed from:	VA*IA	VB*IB	VC*IC	---	all three	

Non-Isolated, 3 Voltage-Dividers, 3 Shunts

This configuration eliminates all CTs and replaces them with shunt resistors that are referenced to Neutral.



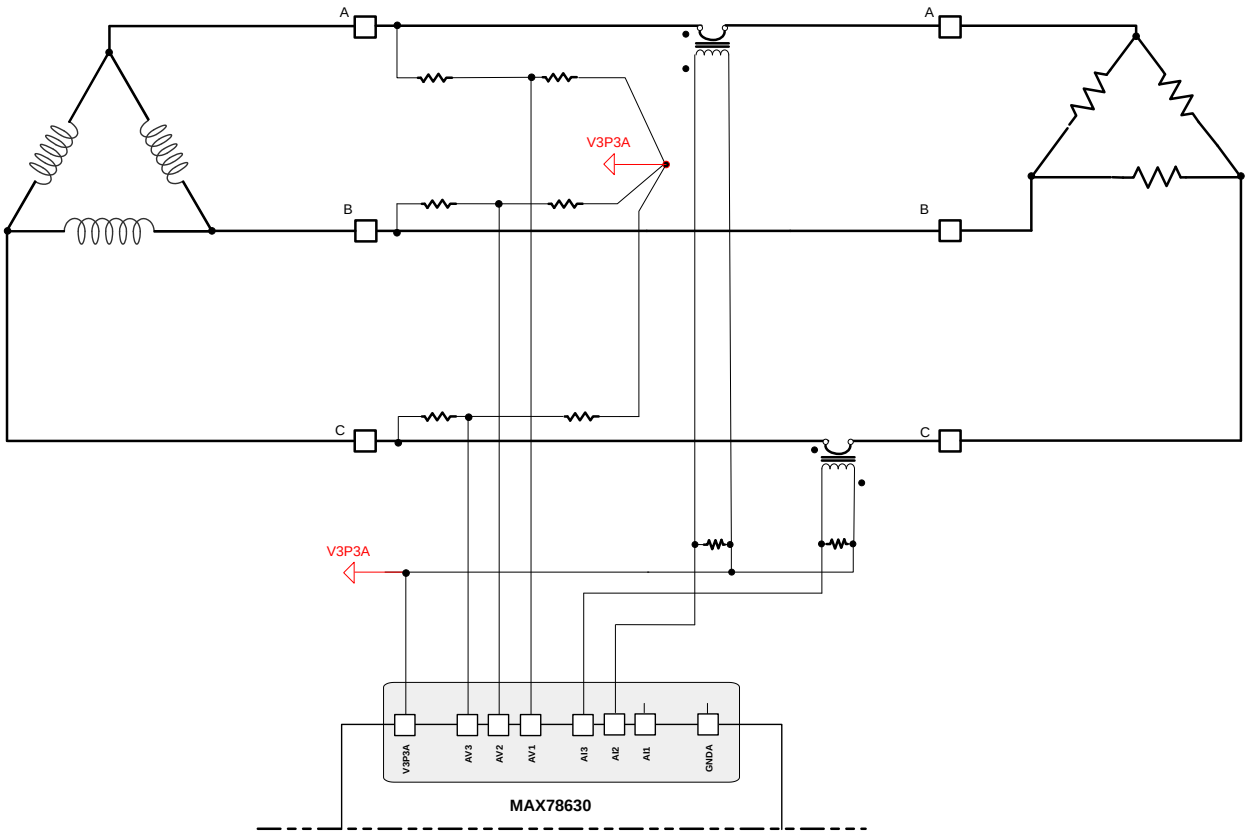
CONFIG[22:20,7:0] hex 0XXX00	INV_AV[CBA]	PPHASE	VDELTA	VPHASE	INEUTRAL	IPHASE
	000	00	0	00	0	00

Outputs	Phase A	Phase B	Phase C	Total = Sum of	Comment
Voltages	VA	VB	VC	---	Line-To-Neutral Voltages
Currents	IA	IB	IC	---	Phase currents
Power (P, Q, S) computed from:	VA*IA	VB*IB	VC*IC	all three	

Delta-Connected Source, Delta-Connected Load (Δ-Δ)

Delta configurations allow for the option to use 2 voltage sensors and/or 2 current sensors instead of 3. The firmware supports these configurations, as well as addition of the third sensor in order to detect fault conditions. Furthermore, the firmware supports placement of the current sensors in either the lines or in the phases.

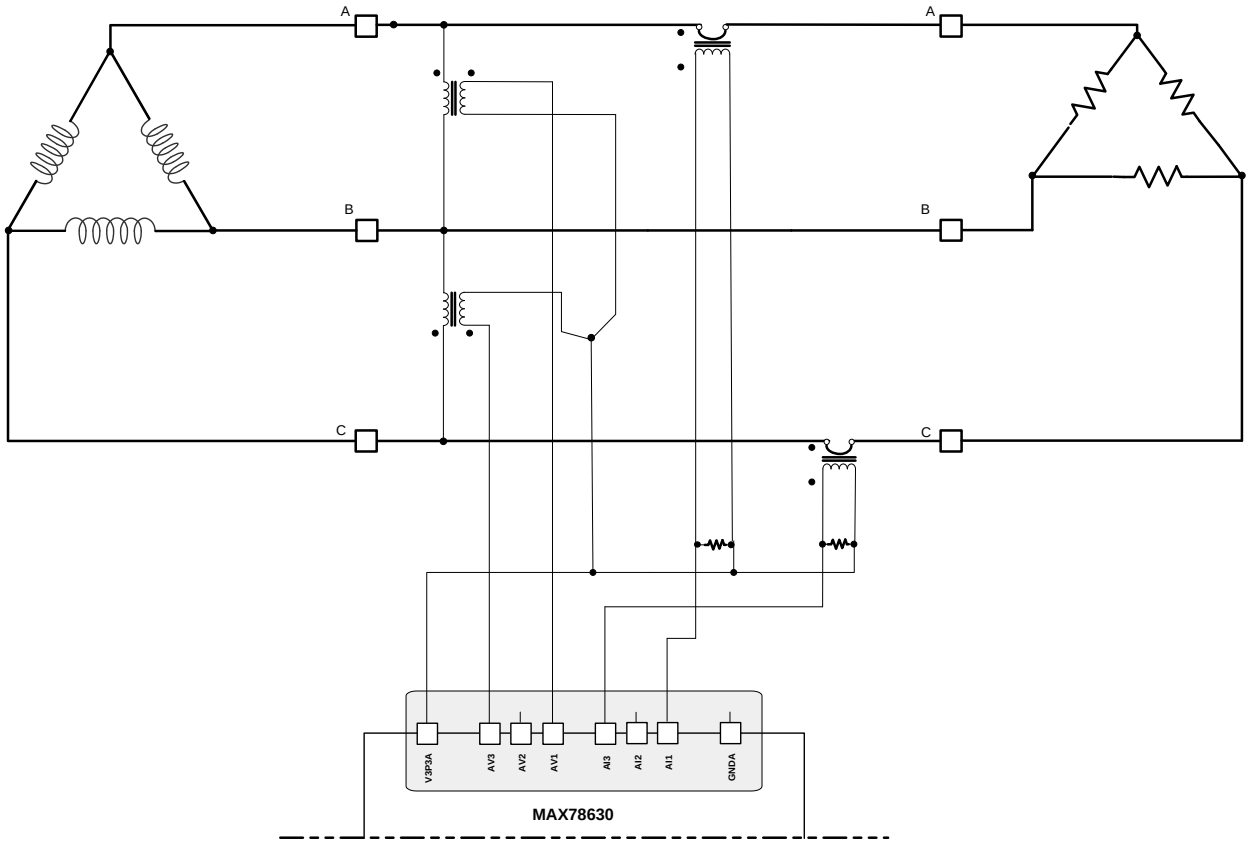
Non-Isolated, 2 CTs, Voltage-Dividers Referenced to V3P3, Line Current Measurements
This configuration maintains high-impedance as seen from all phases by referencing measurements to a virtual or floating center point. Note that the Line-to-Line voltages must be computed from the voltages at the ADC inputs of the device, and therefore VDELTA must be set to "1".



CONFIG[22:20,7:0] hex 0XXX61	INV_AV[CBA]	PPHASE	VDELTA	VPHASE	INEUTRAL	IPHASE
	000	01	1	00	0	01

Outputs	Phase A	Phase B	Phase C	Total = Sum of	Comment
Voltages	VCA = VC – VA	VAB = VA - VB	VBC = VB - VC	---	Line-To-Line Voltages
Currents	IB = IA + IC	IA	-IC	---	Line currents
Power (P, Q, S) computed from:	--- (not needed)	VAB*IA	-VBC*IC	VAB*IA + VCB * IC	Per-phase powers cannot be determined, only total power

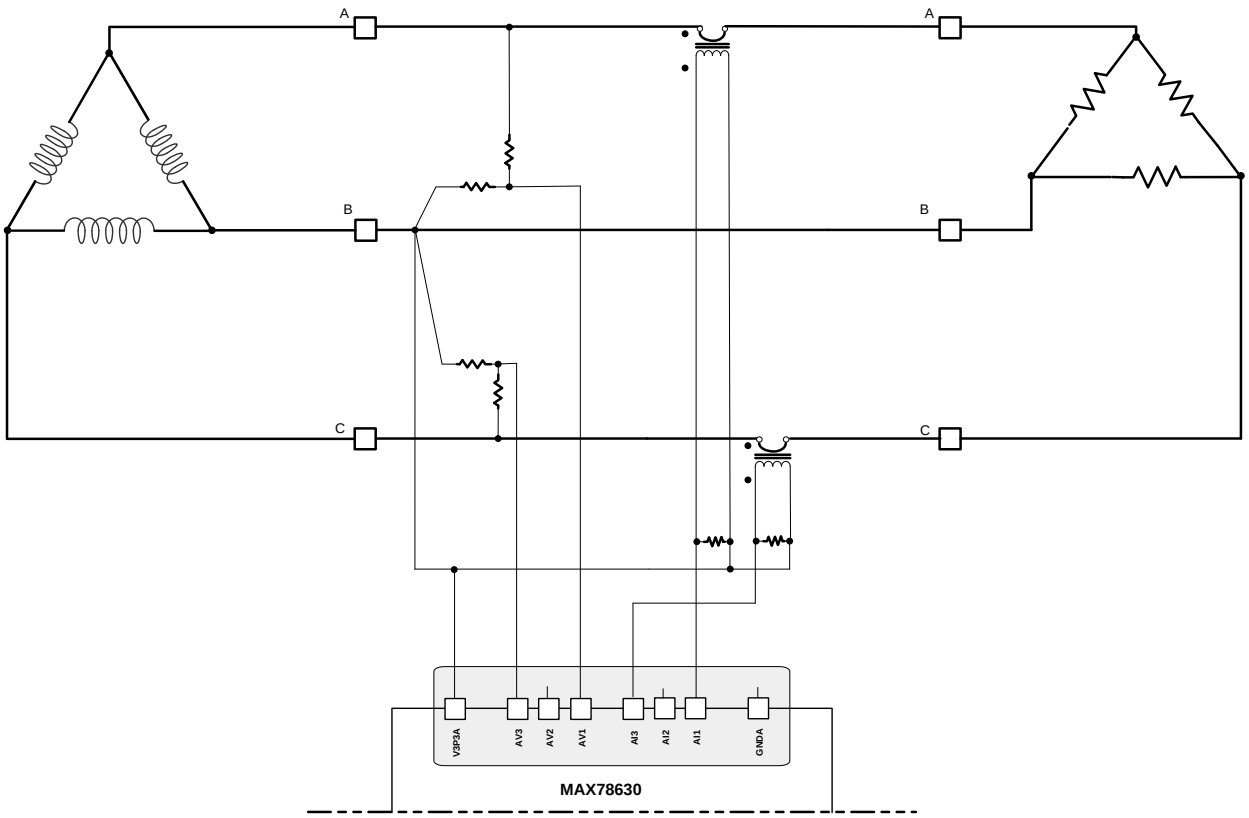
Isolated Configuration, 2 VTs, 2 CTs, Line Current Measurement



CONFIG[22:20,7:0] hex 0XXX92	INV_AV[CBA]	PPHASE	VDELTA	VPHASE	INEUTRAL	IPHASE
	000	10	0	10	0	10

Outputs	Phase A	Phase B	Phase C	Total = Sum of	Comment
Voltages	VAB	VAC = VAB– VCB	VCB	---	Line-To-Line Voltages
Currents	IA	IB = - IC – IA	IC	---	Line currents
Power (P, Q, S) computed from:	VAB*IA	--- (not needed)	VCB * IC	VAB*IA + VBC * IC	Per-phase powers cannot be determined, only total power

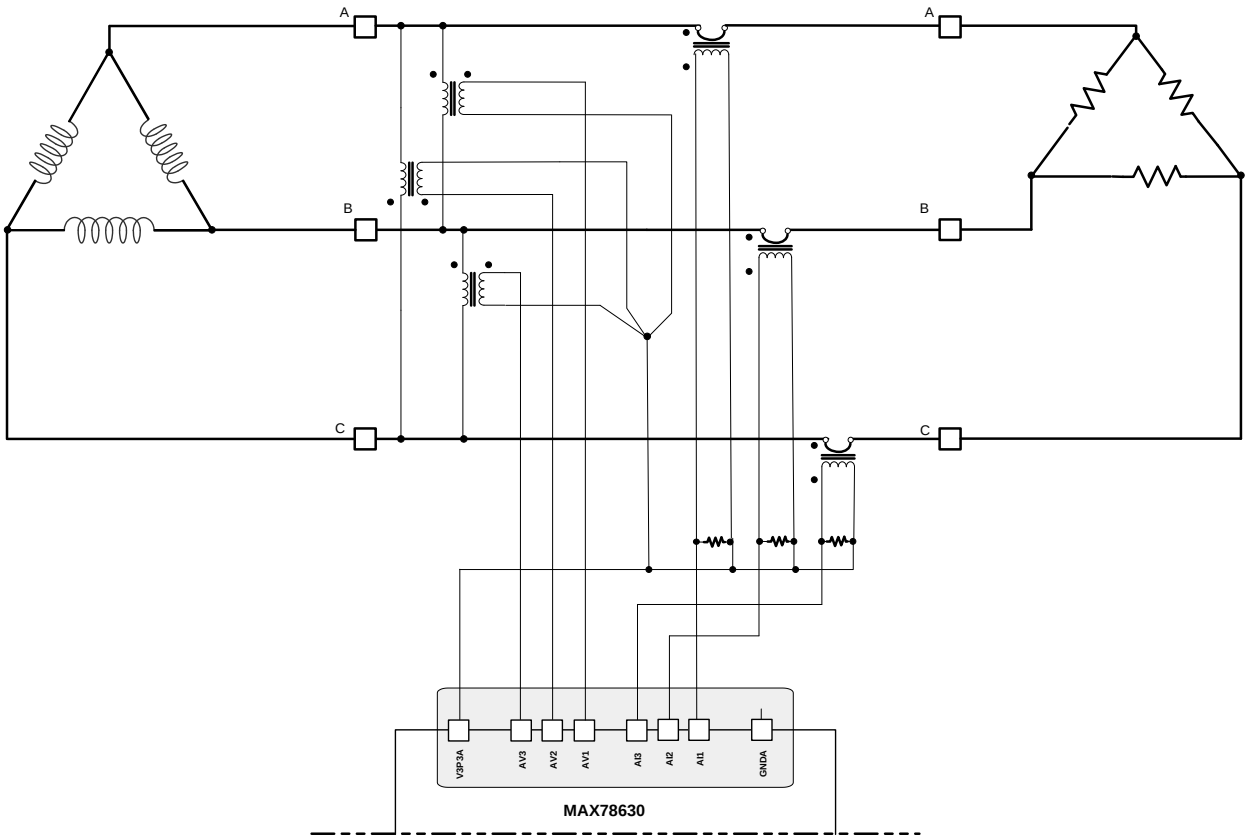
Non-Isolated, 2 Voltage-Dividers Referenced to Line, 2 CTs, Line Current Measurements



CONFIG[22:20,7:0] hex 0XXX92	INV_AV[CBA]	PPHASE	VDELTA	VPHASE	INEUTRAL	IPHASE
	000	10	0	10	0	10

Outputs	Phase A	Phase B	Phase C	Total = Sum of	Comment
Voltages	VAB	VAC = – VAB - VCB	VCB	---	Line-To-Line Voltages
Currents	IA	IB = – IA - IC	IC	---	Line currents
Power (P, Q, S) computed from:	VAB*IA	--- (not needed)	VCB * IC	VAB*IA + VCB * IC	Per-phase powers cannot be determined, only total power

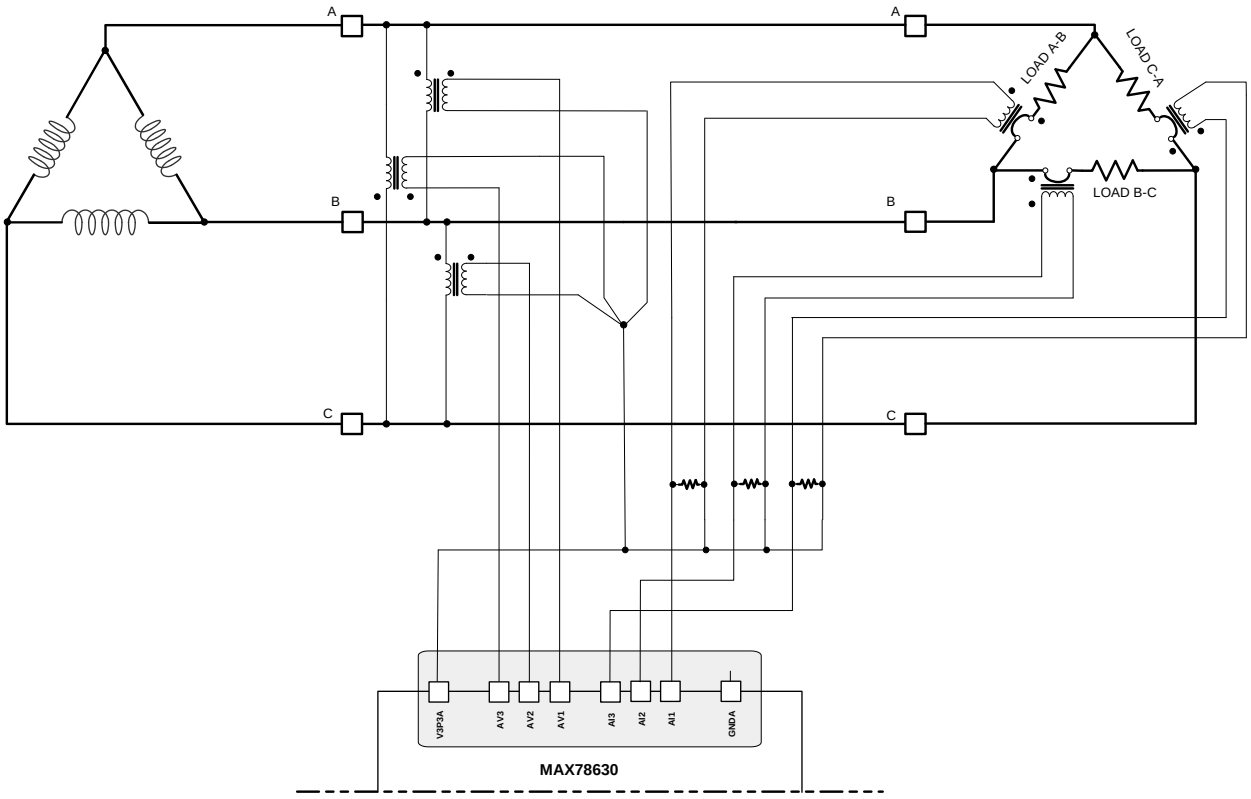
Fully Isolated, 3 VTs, 3 CTs, Line Current Measurement



CONFIG[22:20,7:0] hex 4XXX80	INV_AV[CBA]	PPHASE	VDELTA	VPHASE	INEUTRAL	IPHASE
	100	10	0	00	0	00

Outputs	Phase A	Phase B	Phase C	Total = Sum of	Comment
Voltages	VAB	VCA	-VBC	---	Line-To-Line Voltages
Currents	IA	IB	IC	---	Line currents
Power (P, Q, S) computed from:	VAB*IA	--- (not needed)	-VBC * IC	VAB*IA + VCB * IC	Per-phase powers cannot be determined, only total power

Fully Isolated, 3 VTs, 3 CTs, Phase Current Measurement

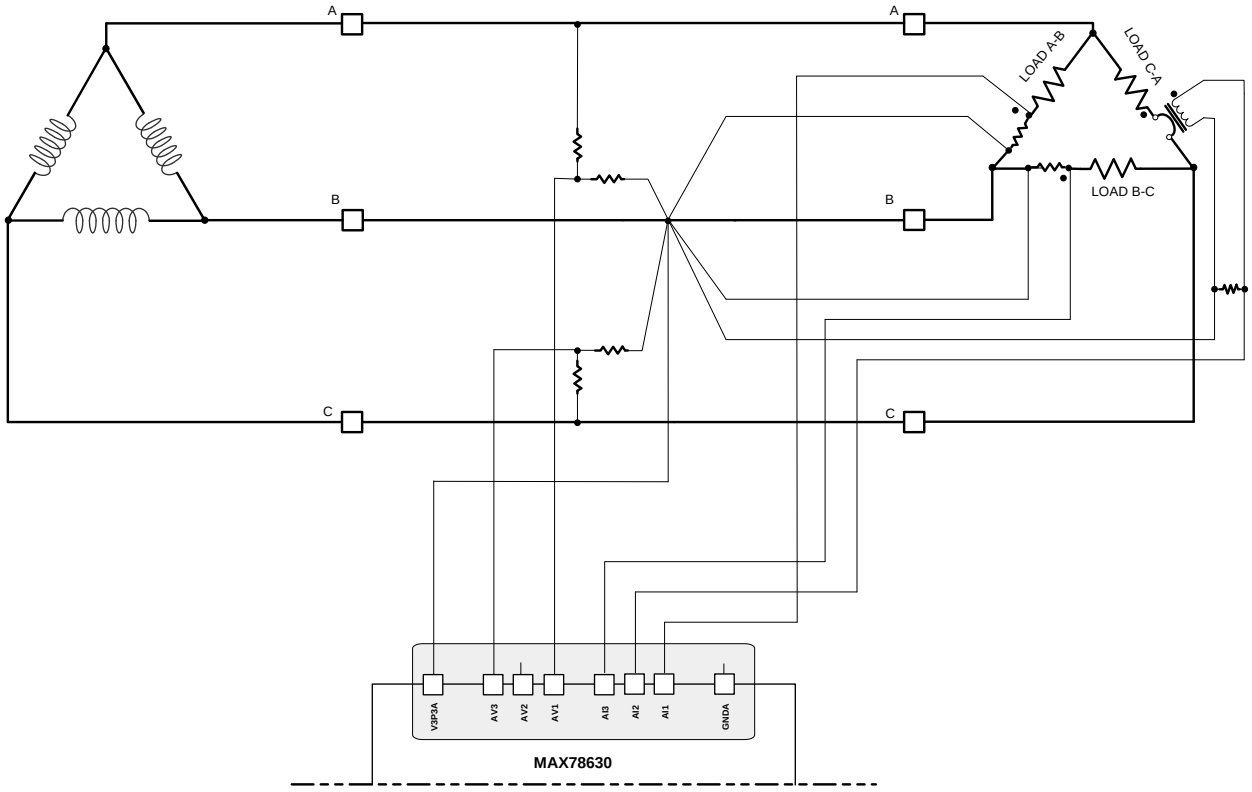


CONFIG[22:20,7:0] hex 0XXX00	INV_AV[CBA]	PPHASE	VDELTA	VPHASE	INEUTRAL	IPHASE
	000	00	0	00	0	00

Outputs	Phase A	Phase B	Phase C	Total = Sum of	Comment
Voltages	VAB	VBC	VCA	---	Line-To-Line Voltages
Currents	IAB	IBC	ICA	---	Phase currents
Power (P, Q, S) computed from:	VAB*IAB	VBC*IBC	VCA*ICA	all three	

Non-Isolated, 1 CT, 2 Shunts and 2 Voltage-Dividers, All Referenced to Phase

This configuration replaces two of the three current transformers with shunts, in this example referenced to phase B.



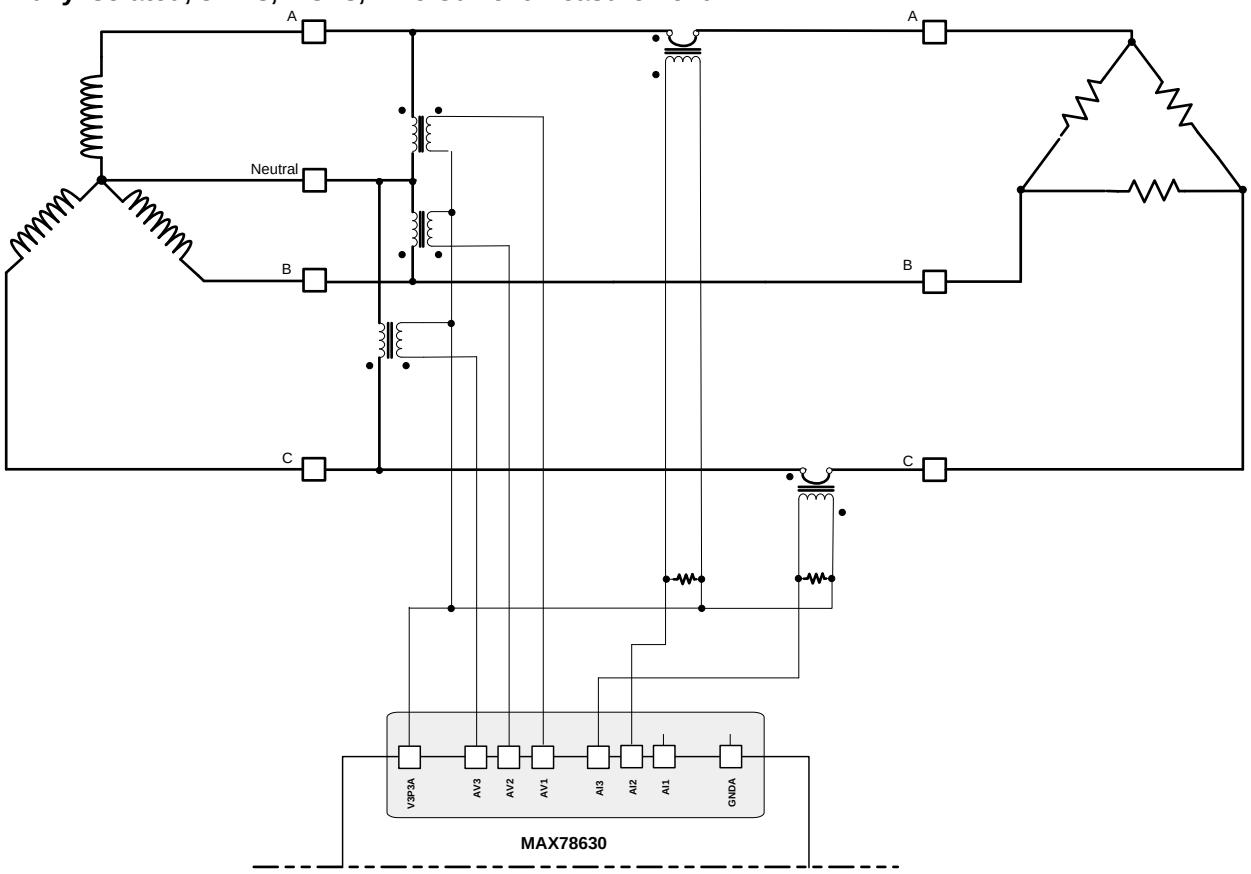
CONFIG[22:20,7:0] hex 0XXX10	INV_AV[CBA]	PPHASE	VDELTA	VPHASE	INEUTRAL	IPHASE
	000	00	0	10	0	00

Outputs	Phase A	Phase B	Phase C	Total = Sum of	Comment
Voltages	VAB	VAC = VAB - VCB	VCB	---	Line-To-Line Voltages
Currents	IAB	IAC	ICB	---	Phase currents
Power (P, Q, S) computed from:	VAB*IAB	VAC*IAC	VCB*ICB	all three	

Wye-Connected Source, Delta-Connected Load (Y-Δ)

Y-Δ configurations can be treated just like the Δ-Δ configurations. The phase voltages can be transformed to line-to-line voltages via the VDELTA configuration bit. Consequently, load-side configuration as seen in the previous section can be used in Y-Δ systems as well. As an example, the fully isolated configuration is shown below.

Fully Isolated, 3 VTs, 2 CTs, Line Current Measurement



CONFIG[22:20,7:0] hex 0XXX61	INV_AV[CBA]	PPHASE	VDELTA	VPHASE	INEUTRAL	IPHASE
	000	01	1	00	0	01

Outputs	Phase A	Phase B	Phase C	Total = Sum of	Comment
Voltages	VCA = VC – VA	VAB = VA - VB	VBC = VB - VC	---	Line-To-Line Voltages
Currents	IB = IA + IC	IA	-IC	---	Line currents
Power (P, Q, S) computed from:	--- (not needed)	VAB*IA	-VBC*IC	VAB*IA + VCB * IC	Per-phase powers cannot be determined, only total power

Register Access

All user registers are contained in a 256 word (24-bits each) area of the on-chip RAM and can be accessed through the UART, SPI, or I^2C interfaces. These registers are byte-addressable via the UART interface and word-addressable via the SPI and I^2C interfaces.

These registers consist of read (output), write (input), and read/write in the case of the Command Register. **Writing to reserved registers or to unspecified memory locations could result in device malfunction or unexpected results.**

Data Types

The input and output registers have different data types, depending on their assignment and functions. The notation used indicates whether the number is signed, unsigned, or bit-mapped and the location of the binary point.

INT Indicates a 24-bit integer with a range of 0 to 16777215 typically used for counters or Boolean registers with 24 independent bit values.

S Indicates a signed fixed point value.

. Indicates a fixed point number.

nn Indicates the number of bits to the right of the binary point.

Example: S.21 is a 24-bit signed fixed-point number with 21 fraction bits to the right of the binary point and a range of -4.0 to $4-2^{-21}$

Bit Position	**23**	**22**	**21**	**.**	**20**	**19**	**18**	**17**	**…**	**2**	**1**	**0**
Bit Multiplier	Sign bit (-2^2)	2^1	2^0		2^{-1}	2^{-2}	2^{-3}	2^{-4}	…	2^{-19}	2^{-20}	2^{-21}
Max Value	0	1	1		1	1	1	1	1	1	1	1
Min Value	1	0	0		0	0	0	0	0	0	0	0

Register Locations

Use Word addresses for I^2C and SPI interfaces and Byte addresses for the SSI (UART) protocol. Nonvolatile (NV) register defaults are indicated with a 'Y'. All other registers are initialized as described in the Functional Description.

Word Addr (hex)	Byte Addr (hex)	Register	Type	NV	Description
0	0	COMMAND	INT	Y	Selects modes, functions, or options
1	3	CONFIG	INT	Y	Selects input configuration
2	6	FW_VERSION	INT		Hardware and Firmware version
3	9	SAMPLES	INT	Y	Minimum high-rate samples per accumulation interval
4	C	DIVISOR	INT		Actual samples in previous accumulation interval
5	F	CYCLE	INT		High-rate sample counter
6	12	FRAME	INT		Low-rate sample counter
7	15	STATUS	INT		Alarm and device status bits
8	18	STATUS_CLEAR	INT		Used to reset alarm/status bits
9	1B	STATUS_SET	INT		Used to set/force alarm/status bits
A	1E	MASK1	INT	Y	Alarm/status mask for AL1 output pin
B	21	MASK2	INT	Y	Alarm/status mask for AL2 output pin
C	24	MASK3	INT	Y	Alarm/status mask for AL3 output pin
D	27	MASK4	INT	Y	Alarm/status mask for AL4 output pin
E	2A	MASK5	INT	Y	Alarm/status mask for AL5 output pin
F	2D	STICKY	INT	Y	Alarm/status bits to hold until cleared by host
10	30	DIO_STATE	INT		State of DIO pins
11	33	DIO_DIR	INT	Y	Direction of DIO pins. 1=Input ; 0=Output
12	36	DIO_POL	INT	Y	Polarity of DIO pins. 1=Active High ; 0=Active Low
13	39	CALCYCS	INT	Y	Number of calibration cycles to average
14	3C	HPF_COEF_I	S.23	Y	Current input HPF coefficient. Positive values only
15	3F	HPF_COEF_V	S.23	Y	Voltage input HPF coefficient. Positive values only
16	42	PHASECOMP1	S.21	Y	Phase compensation (+/-4 samples) for AV1 input
17	45	PHASECOMP2	S.21	Y	Phase compensation (+/-4 samples) for AV2 input
18	48	PHASECOMP3	S.22	Y	Phase compensation (+/-4 samples) for AV3 input
19	4B	HARM	INT	Y	Harmonic Selector, default: 1 (fundamental)
1A	4E	DEVADDR	INT	Y	High order address bits for I2C and UART interfaces
1B	51	BAUD	INT	Y	Baud rate for UART interface
1C	54	I1_GAIN	S.21	Y	Current Gain Calibration.Positive values only
1D	57	I2_GAIN	S.21	Y	Current Gain Calibration.Positive values only
1E	5A	I3_GAIN	S.21	Y	Current Gain Calibration.Positive values only
1F	5D	V1_GAIN	S.21	Y	Voltage Gain Calibration. Positive values only
20	60	V2_GAIN	S.21	Y	Voltage Gain Calibration. Positive values only

Word Addr (hex)	Byte Addr (hex)	Register	Type	NV	Description
21	63	V3_GAIN	S.21	Y	Voltage Gain Calibration. Positive values only
22	66	I1_OFFS	S.23	Y	Current Offset Calibration
23	69	I2_OFFS	S.23	Y	Current Offset Calibration
24	6C	I3_OFFS	S.23	Y	Current Offset Calibration
25	6F	V1_OFFS	S.23	Y	Voltage Offset Calibration
26	72	V2_OFFS	S.23	Y	Voltage Offset Calibration
27	75	V3_OFFS	S.23	Y	Voltage Offset Calibration
28	78	T_GAIN		Y	Temperature Slope Calibration
29	7B	T_OFFS		Y	Temperature Offset Calibration
2A	7E	VSAG_INT	INT	Y	Voltage sag detect interval (high-rate samples)
2B	81	V_IMB_MAX	S.23	Y	Voltage imbalance alarm limit. Positive values only
2C	84	I_IMB_MAX	S.23	Y	Current imbalance alarm limit. Positive values only
2D	87	VA	S.23		Instantaneous Voltage
2E	8A	VB	S.23		Instantaneous Voltage
2F	8D	VC	S.23		Instantaneous Voltage
30	90	VA_RMS	S.23		RMS Voltage
31	93	VB_RMS	S.23		RMS Voltage
32	96	VC_RMS	S.23		RMS Voltage
33	99	VT_RMS	S.23		RMS Voltage average (Total / 3)
34	9C	VFUND_A	S.23		Fundamental Voltage
35	9F	VFUND_B	S.23		Fundamental Voltage
36	A2	VFUND_C	S.23		Fundamental Voltage
37	A5	VHARM_A	S.23		Harmonic Voltage
38	A8	VHARM_B	S.23		Harmonic Voltage
39	AB	VHARM_C	S.23		Harmonic Voltage
3A	AE	V_TARGET	S.23	Y	Calibration Target for Voltages. Positive values only
3B	B1	VRMS_MIN	S.23	Y	Voltage lower alarm limit. Positive values only
3C	B4	VRMS_MAX	S.23	Y	Voltage upper alarm limit. Positive values only
3D	B7	VSAG_LIM	S.23	Y	RMS Voltage Sag threshold. Positive values only
3E	BA	IA	S.23		Instantaneous Current
3F	BD	IB	S.23		Instantaneous Current
40	C0	IC	S.23		Instantaneous Current
41	C3	IARMS_OFF	S.23	Y	RMS Current dynamic offset adjust. Positive values only
42	C6	IBRMS_OFF	S.23	Y	RMS Current dynamic offset adjust. Positive values only
43	C9	ICRMS_OFF	S.23	Y	RMS Current dynamic offset adjust. Positive values only
44	CC	IA_PEAK	S.23		Peak Current

Word Addr (hex)	Byte Addr (hex)	Register	Type	NV	Description
45	CF	IB_PEAK	S.23		Peak Current
46	D2	IC_PEAK	S.23		Peak Current
47	D5	IA_RMS	S.23		RMS Current
48	D8	IB_RMS	S.23		RMS Current
49	DB	IC_RMS	S.23		RMS Current
4A	DE	IT_RMS	S.23		RMS Current average (Total / 3)
4B	E1	IFUND_A	S.23		Fundamental Current
4C	E4	IFUND_B	S.23		Fundamental Current
4D	E7	IFUND_C	S.23		Fundamental Current
4E	EA	IHARM_A	S.23		Harmonic Current
4F	ED	IHARM_B	S.23		Harmonic Current
50	F0	IHARM_C	S.23		Harmonic Current
51	F3	IRMS_MAX	S.23	Y	Current upper alarm limit. Positive values only
52	F6	I_TARGET	S.23	Y	Calibration Target for Currents. Positive values only
53	F9	QFUND_A	S.23		Fundamental Reactive Power
54	FC	QFUND_B	S.23		Fundamental Reactive Power
55	FF	QFUND_C	S.23		Fundamental Reactive Power
56	102	QHARM_A	S.23		Harmonic Reactive Power
57	105	QHARM_B	S.23		Harmonic Reactive Power
58	108	QHARM_C	S.23		Harmonic Reactive Power
59	10B	QA_OFFS	S.23	Y	Reactive Power dynamic offset adjust. Positive values only
5A	10E	QB_OFFS	S.23	Y	Reactive Power dynamic offset adjust. Positive values only
5B	111	QC_OFFS	S.23	Y	Reactive Power dynamic offset adjust. Positive values only
5C	114	PA_OFFS	S.23	Y	Active Power dynamic offset adjust. Positive values only
5D	117	PB_OFFS	S.23	Y	Active Power dynamic offset adjust. Positive values only
5E	11A	PC_OFFS	S.23	Y	Active Power dynamic offset adjust. Positive values only
5F	11D	WATT_A	S.23		Active Power
60	120	WATT_B	S.23		Active Power
61	123	WATT_C	S.23		Active Power
62	126	VAR_A	S.23		Reactive Power
63	129	VAR_B	S.23		Reactive Power
64	12C	VAR_C	S.23		Reactive Power
65	12F	VA_A	S.23		Apparent Power
66	132	VA_B	S.23		Apparent Power
67	135	VA_C	S.23		Apparent Power

Word Addr (hex)	Byte Addr (hex)	Register	Type	NV	Description
68	138	WATT_T	S.23		Active Power average (Total / 3)
69	13B	VAR_T	S.23		Reactive Power average (Total / 3)
6A	13E	VA_T	S.23		Apparent Power average (Total / 3)
6B	141	IFSCALE	INT	Y	Scratch register (see Scaling Registers section)
6C	144	VSCALE	INT	Y	Scratch register (see Scaling Registers section)
6E	14A	PFUND_A	S.23		Fundamental Power
6F	14D	PFUND_B	S.23		Fundamental Power
70	150	PFUND_C	S.23		Fundamental Power
71	153	PHARM_A	S.23		Harmonic Power
72	156	PHARM_B	S.23		Harmonic Power
73	159	PHARM_C	S.23		Harmonic Power
74	15C	VAFUNDA			Fundamental Volt Amperes
75	15F	VAFUNDB			Fundamental Volt Amperes
76	162	VAFUNDC			Fundamental Volt Amperes
77	165	PFA	S.22		Power Factor
78	168	PFB	S.22		Power Factor
79	16B	PFC	S.22		Power Factor
7A	16E	PF_T	S.22		Total Power Factor
7B	171	PF_MIN	S.22	Y	Power Factor lower alarm limit
7C	174	TEMPC	S.10		Chip Temperature (Celsius°)
7D	177	T_TARGET	S.10	Y	Temperature calibration target
7E	17A	T_MIN	S.10	Y	Temperature Alarm Lower Limit
7F	17D	T_MAX	S.10	Y	Temperature Alarm Upper Limit
80	180	FREQ	S.16		Line Frequency
81	183	F_MIN	S.16	Y	Frequency Alarm Lower Limit
82	186	F_MAX	S.16	Y	Frequency Alarm Upper Limit
83	189	MIN0			Minimum Recorded Value 1
84	18C	MIN1			Minimum Recorded Value 2
85	18F	MIN2			Minimum Recorded Value 3
86	192	MIN3			Minimum Recorded Value 4
87	195	MIN4			Minimum Recorded Value 5
88	198	MIN5			Minimum Recorded Value 6 (reserved when EN_ROGA =1)
89	19B	MIN6			Minimum Recorded Value 7 (reserved when EN_ROGB =1)
8A	19E	MIN7			Minimum Recorded Value 8 (reserved when EN_ROGC =1)
8B	1A1	MAX0			Maximum Recorded Value 1
8C	1A4	MAX1			Maximum Recorded Value 2
8D	1A7	MAX2			Maximum Recorded Value 3

Word Addr (hex)	Byte Addr (hex)	Register	Type	NV	Description
8E	1AA	MAX3			Maximum Recorded Value 4
8F	1AD	MAX4			Maximum Recorded Value 5
90	1B0	MAX5			Maximum Recorded Value 6 (reserved when EN_ROGA =1)
91	1B3	MAX6			Maximum Recorded Value 7 (reserved when EN_ROGB =1)
92	1B6	MAX7			Maximum Recorded Value 8 (reserved when EN_ROGC =1)
93	1B9	MMADDR0	INT	Y	Min/Max Monitor address 1
94	1BC	MMADDR1	INT	Y	Min/Max Monitor address 2
95	1BF	MMADDR2	INT	Y	Min/Max Monitor address 3
96	1C2	MMADDR3	INT	Y	Min/Max Monitor address 4
97	1C5	MMADDR4	INT	Y	Min/Max Monitor address 5
98	1C8	MMADDR5	INT	Y	Min/Max Monitor address 6
99	1CB	MMADDR6	INT	Y	Min/Max Monitor address 7
9A	1CE	MMADDR7	INT	Y	Min/Max Monitor address 8
9B	1D1	BUCKET	INT	Y	Energy Bucket Size – Low word
9C	1D4	BUCKET	INT	Y	Energy Bucket Size – High word
9F	1DD	WHA_POS	INT		Received Active Energy Counter
A2	1E6	WHA_NEG	INT		Delivered Active Energy Counter
A5	1EF	WHB_POS	INT		Received Active Energy Counter
A8	1F8	WHB_NEG	INT		Delivered Active Energy Counter
AB	201	WHC_POS	INT		Received Active Energy Counter
AE	20A	WHC_NEG	INT		Delivered Active Energy Counter
B1	213	VARHA_POS	INT		Reactive Energy Leading Counter
B4	21C	VARHA_NEG	INT		Reactive Energy Lagging Counter
B7	225	VARHB_POS	INT		Reactive Energy Leading Counter
BA	22E	VARHB_NEG	INT		Reactive Energy Lagging Counter
BD	237	VARHC_POS	INT		Reactive Energy Leading Counter
C0	240	VARHC_NEG	INT		Reactive Energy Lagging Counter

Serial Interfaces

All user registers are contained in a 256 word (24-bits each) area of the on-chip RAM and can be accessed through the UART, SPI, or I^2C interfaces. While access to a single byte is possible with some interfaces, it is highly recommended that the user access words (or multiple words) of data with each transaction.

Only one interface can be active at a time. The interface selection pins are sampled at the end of a reset sequence to determine the operating mode.

Interface Mode	IFC0	IFC1
SPI	0	X (don't care)
UART	1	0
I^2C	1	1

UART Interface

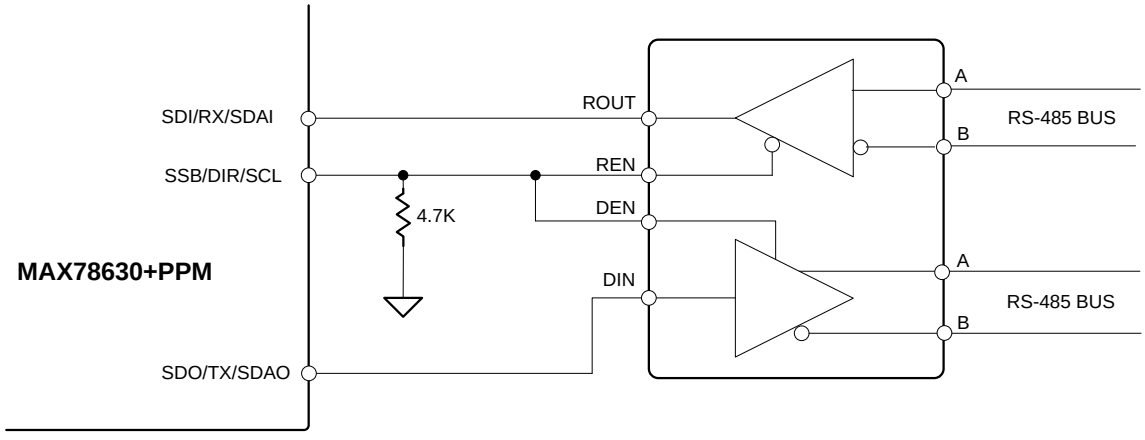
The device implements a simple serial interface (SSI) protocol on the UART interface that features:

- Support for single and multi-point communications
- Transmit (direction) control for an RS-485 transceiver
- Efficient use of a low bandwidth serial interface
- Data integrity checking

The default configuration is 38400 baud, 8-bit, no-parity, 1 stop-bit, no flow control. The value in the BAUD register determines the baud rate to be used. Example: To select a 9600 baud rate, the user writes a decimal 9600 to the BAUD register. The new rate will not take effect immediately. It must be saved to flash and will take effect at the next reset. The maximum BAUD value is limited to 115200.

RS-485 Support

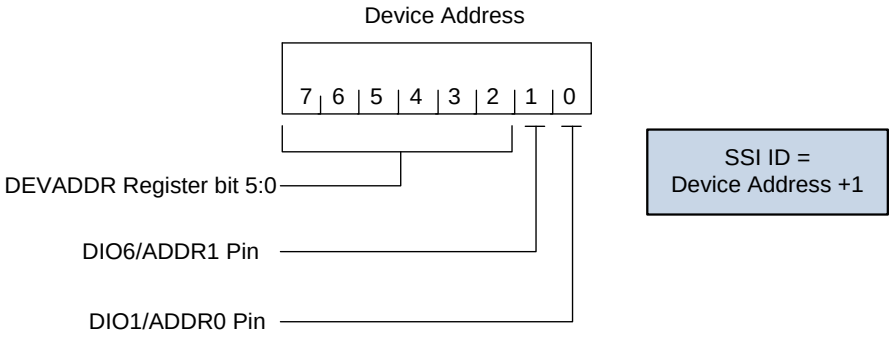
The SSB/DIR/SCL pin is used to drive an RS-485 transceiver output enable or direction pin. The implemented protocol supports a full-duplex 4-wire RS-485 bus.



Device Address Configuration

The SSI protocol utilizes 8-bit addressing for multi-point communications. The usable SSI ID range is 1 to 254. In multi-point systems with more than 4 targets, the user must configure device address bits in the DEVADDR according to the formula SSI ID = Device Address +1.

A device address of 'FF' is not supported. DEVADDR [23:6] bit are not used and must be set to 1.



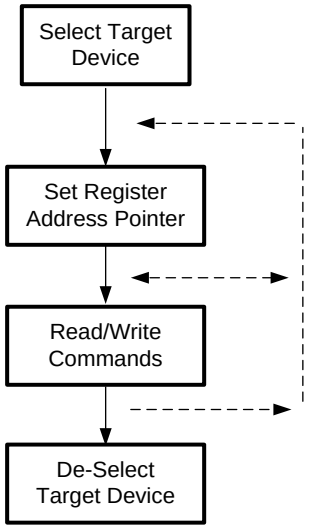
SSI Protocol Description

The SSI protocol is command response system supporting a single master and one or more targets. The host (master) sends commands to a selected target that first verifies the integrity of the packet before sending a reply or executing a command. Failure to decode a host packet will cause the selected target to send a fail code. If the condition of a received packet is uncertain, no reply is sent.

Each target must have a unique SSI ID. Zero is not a valid SSI ID for a target device as it is used by the host to de-select all target devices.

With both address pins low on the MAX78630+PPM, the SSI ID defaults to 1 and is the “Selected” device following a reset. This configuration is intended for single target (point-to-point) systems that do not require the use of device addressing or selecting targets.

In multi-point systems, the master will typically de-select all target devices by selecting SSI ID #0. The master must then select the target with a valid SSI ID and get an acknowledgement from the slave before setting the target’s register address pointer and performing read or write operations. If no target is selected, no reply is sent. The SSB/DIR/SCL pin is asserted while the device is selected. The sequence of operation is shown in the following diagram.



Master Packets

Master packets always start with the 1-byte header (0xAA) for synchronization purposes. The master then sends the byte count of the entire packet (up to 255 byte packets) followed by the payload (up to 253 bytes) and a 1-byte modulo-256 checksum of all packet bytes for data integrity checking.

The payload can contain either a single command or multiple commands if the target is already selected. It can also include device addresses, register addresses, and data. All multi-byte payloads are sent and received least-significant-byte first.

Master Packet Command Summary

Command	Parameters	Description
0 - 7F		(invalid)
80 - 9F		(not used)
A0		Clear address
A1	[byte-L]	Set Read/Write address bits [7:0]
A2	[byte-H]	Set Read/Write address bits [15:8]
A3	[byte-L][byte-H]	Set Read/Write address bits [15:0]
A4 - AF		(reserved for larger address targets)
B0 - BF		(not used)
C0		De-select Target (target will Acknowledge)
C1 - CE		Select target 1 to 14 (target will Acknowledge)
CF	[byte]	Select target 0 to 255 (target will Acknowledge)
D0	[data...]	Write bytes set by remainder of Byte Count
D1 - DF	[data...]	Write 1 to 15 bytes
E0	[byte]	Read 0 to 255 bytes
E1 – EF		Read 1 to 15 bytes
F0 - FF		(not used)

Users only need to implement commands they actually need or intend to use. For example, only one address command is required – either 0xA1 for systems with 8 address bits or less or 0xA3 for systems with 9 to 16 address bits. Likewise, only one write, read, or select target command needs to be implemented. Select Target is not needed in systems with only one target.

Command Payload Examples

Device Selection

PAYLOAD	
0xCF Command	SSI ID

Register Address Pointer Selection

PAYLOAD	
0xA3 Command	Register Address (2 Bytes)

Small Read Command (3 bytes)

PAYLOAD
0xE3 Command

Large Read Command (30 bytes)

PAYLOAD	
0xE0 Command	0x1E (30 bytes)

Small Write Command (3 bytes)

PAYLOAD	
0xD3 Command	3 Bytes of Data

Large Write Command (30 bytes)

Byte Count	PAYLOAD	
0x21 (34 bytes)	0xD0 Command	30 Bytes of Data

After each read or write operation, the internal address pointer is incremented to point to the address that followed the target of the previous read or write operation.

Slave Packets

The type of slave packet depends upon the type of command from the master device and the successful execution by the slave device. Standard replies include “Acknowledge” and “Acknowledge with Data”.

ACKNOWLEDGE without data

ACKNOWLEDGE with data	BYTE COUNT	READ DATA	CHECK SUM

If no data is expected from the slave or there is a fail code, a single byte reply is sent. If a successfully decoded command is expected to reply with data, the slave sends a packet format similar to the master packet where the header is replaced with a Reply Code and the payload contains the read data.

Reply Code	Definition
0xAA	Acknowledge with data
0xAB	Acknowledge with data (half duplex)
0xAD	Acknowledge without data.
0xB0	Negative Acknowledge (NACK).
0xBC	Command not implemented.
0xBD	Checksum failed.
0xBF	Buffer overflow (or packet too long).
- timeout -	Any condition too difficult to handle with a reply.

Failure to decode a host packet will cause the selected target to send a fail code (0xB0 – 0xBF) acknowledgement depending on mode of failure. Masters wishing to simplify could accept any unimplemented fail code as a Negative Acknowledge.

If no target is selected or the condition of a received packet is uncertain, no reply is sent. Timeouts can also occur when data is corrupt or no target is selected. The master should implement the appropriate timeout control logic after approximately 50 byte times at the current baud rate. When a first reply byte is received, the master should check to see if it is an SSI header or an Acknowledge. If so, the timeout timer is reset, and each subsequent receive byte will also reset the timer. If no byte is received within the timeout interval, the master can expect the slave timed out and re-send a new command.

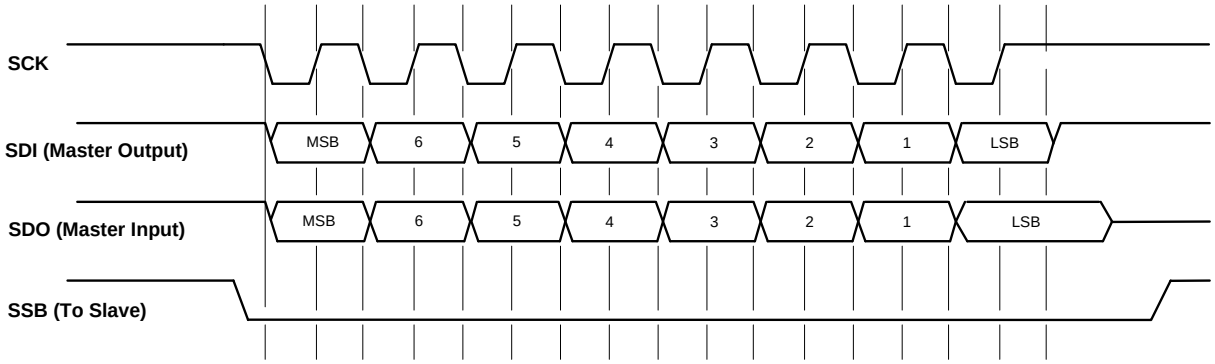
SPI Interface

The MAX78630+PPM SPI can be configured as slave only. Once the SPI interface is activated, it utilizes the following pins:

SSB: Slave select (SS) is an input and active low signal
SCK: Serial Data Clock (SCK) input
SDO: Master Input/Slave Output (MISO), serial data output
SDI: Master Output/Slave Input (MOSI), serial data input

Clock Polarity and Phase

The figure below shows a single-byte transaction on the SPI bus. The data is shifted on the falling edge of the serial data clock and latched (captured) on the rising edge.



SPI Protocol

The SPI allows access to the read and write registers. The first byte that the master needs to transmit to the MAX78630+PPM (slave) is the control byte. The control byte allows setting the number of words to be transferred and the most significant bits of the register address:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NBRACC[3:0]				ADDR7	ADDR6	0	1

ADDR7 and ADDR6 bits select bit 7 and 6 of the 8-bit register address to be accessed by the following data transactions. The read and write register are contained in a 256 words (24-bit) area of the on-chip RAM.

NBRACC[3:0] represents the number of words (3-bytes) accesses to be performed by subsequent data transactions. The actual number of data addresses accessed per data transaction is NBRACC + 1. For single address access, the field is set at 0. NBRACC is reset to 0 when the operation (multiple reads or writes) is completed. NBRACC must be set to a non-zero value prior to each multiple word transaction.

The second byte determines the direction of the transfer and the higher bits of the address. After that, data bytes are shifted in or out depending on the content of the first two control bytes. The complete transaction is structured as follows:

Byte Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	NBRACC[3:0]				ADDR7	ADDR6	0	1
2	ADDR[5:0]						R/W	0
3	DATA[23:16] @ Addr							
4	DATA[15:8] @ Addr							
5	DATA[7:0] @ Addr							
6	DATA[23:16] @ Addr + 1							
7	DATA[15:8] @ Addr +1							
8	DATA[7:0] @ Addr +1							
…	…							
(NbrAcc*3)+3	DATA[23:16] @ Addr + NbrAcc							
(NbrAcc*3)+4	DATA[15:8] + NbrAcc							
(NbrAcc*3)+5	DATA[7:0] + NbrAcc							

R/W: Defines the directionality of the transaction (Read = 0; Write = 1);
ADDR[5:0]: Indicates the remainder of the address to access.

The following are some transaction examples.

Example 1: Write access of address 0x14.

Byte Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	NbrAcc[3:0] = 0x00				Addr7=0	Addr6=0	0	1
2	Addr[5:0] = 0x14						WR=1	0
3	Data[23:16] @ 0x14							
4	Data[15:8] @ 0x14							
5	Data[7:0] @ 0x14							

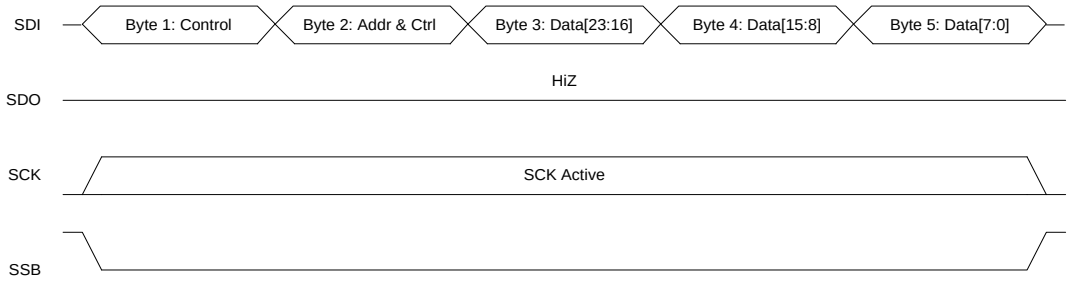
Example 2: Read access of address 0x17 and 0x18.

Byte Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	NbrAcc[3:0] = 0x01				Addr7=0	Addr6=0	0	1
2	Addr[5:0] = 0x17						RD=0	0
3	Data[23:16] @ 0x17							
4	Data[15:8] @ 0x17							
5	Data[7:0] @ 0x17							
6	Data[23:16] @ 0x18							
7	Data[15:8] @ 0x18							
8	Data[7:0] @ 0x18							

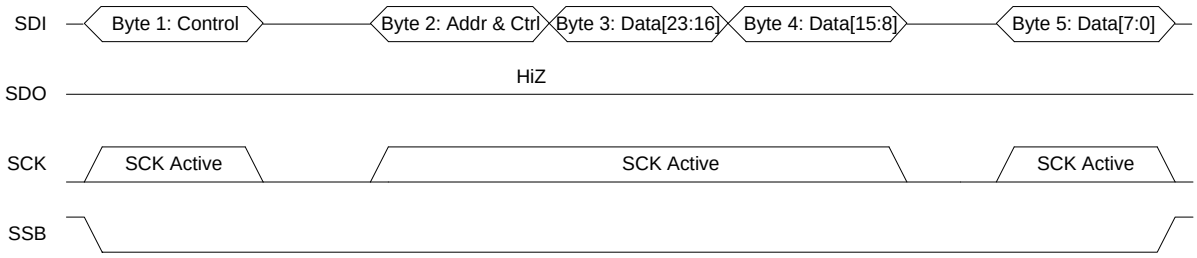
Example 3: Non-Contiguous Read accesses of address 0x17 and 0x0A.

Byte#	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	NbrAcc[3:0] = 0x00				Addr7=0	Addr6=0	0	1
2	Addr[5:0] = 0x17						RD=0	0
3	Data[23:16] @ 0x17							
4	Data[15:8] @ 0x17							
5	Data[7:0] @ 0x17							
6	NbrAcc[3:0] = 0x00				Addr7=0	Addr6=0	0	1
7	Addr[5:0] = 0x0A						W=1	0
8	Data[23:16] @ 0x0A							
9	Data[15:8] @ 0x0A							
10	Data[7:0] @ 0x0A							

The timing of the transaction can be organized in different ways depending on the host capabilities. The above transaction can be a succession of bytes as shown in the diagram below. Those bytes are carried by a continuously active SCK, with eight clock periods per byte.

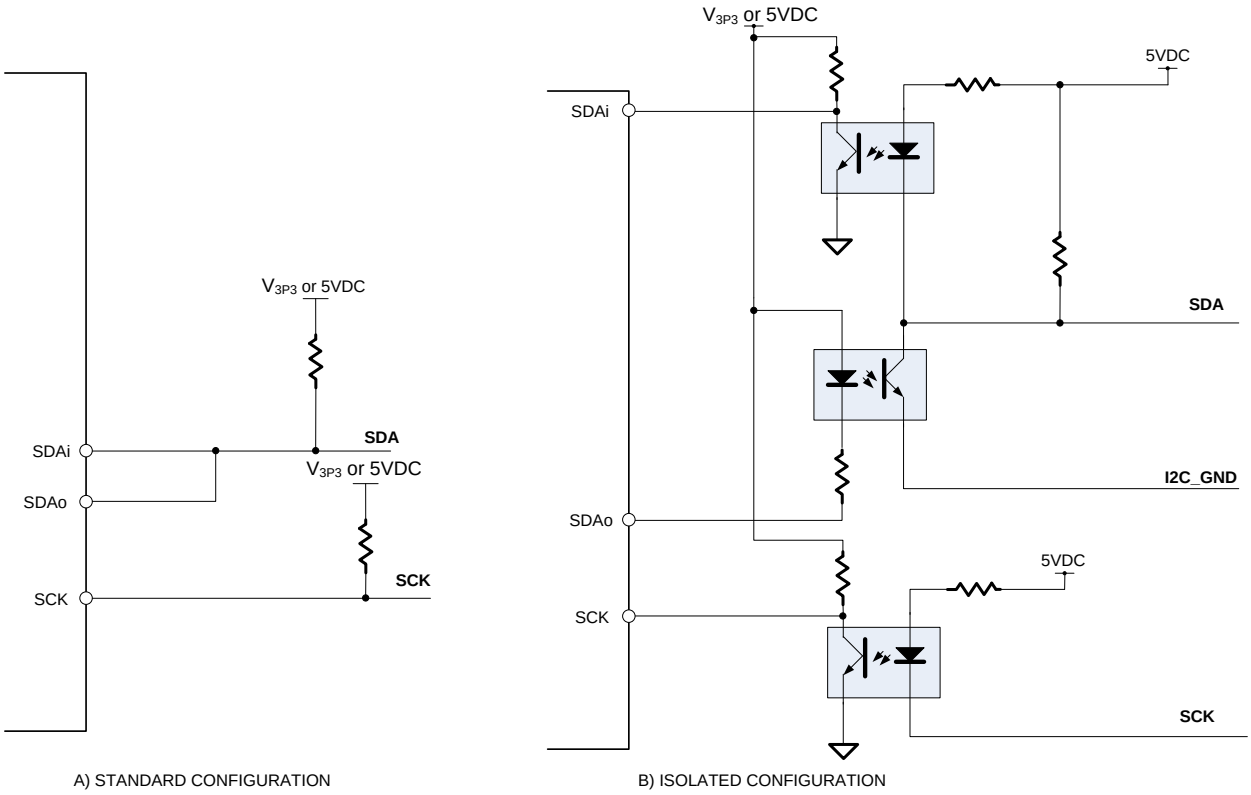


The host also has the possibility to space out the bytes transmitted. In such a case, SCK is inactive during the “in-between-bytes” gap, as illustrated below. Note that the figure shows two gaps, one between the configuration and the data transactions and another between bytes within the data transaction. The placement of those gaps is strictly for the purpose of illustrating the concept.



I²C Interface

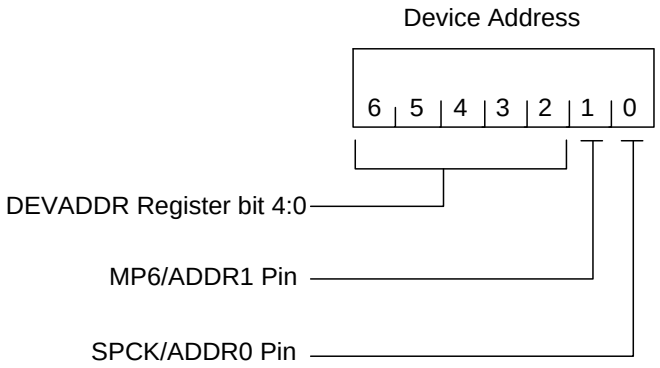
The MAX78630+PPM has an I²C interface available at the SDAI, SDAO, and SCL pins. The interface supports I²C slave mode with a 7-bit address and operates at a data rate up to 400 kHz. The figure below shows two possible configurations. Configuration A is the standard configuration. The double pin for SDA also allows for isolated configuration B.



Device Address Configuration

By default, there are only four possible addresses for the MAX78630+PPM as defined by two external address pins. To expand the potential address of the device to the entire 7-bit address range for I²C, one must first set bits [11:5] in the DEVADDR register. Bits 6 through 2 of the device address can then be defined by the lower 5-bits of the DEVADDR register (bits 4:0).

DEVADDR bits 23 through 12 are not used and should be set to 0.

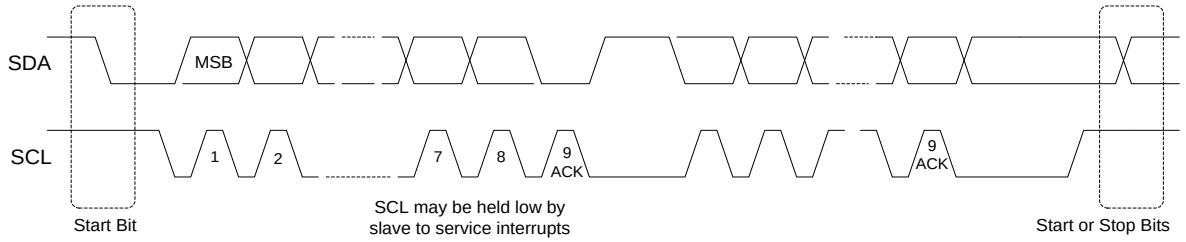


Bus Characteristics

- A data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

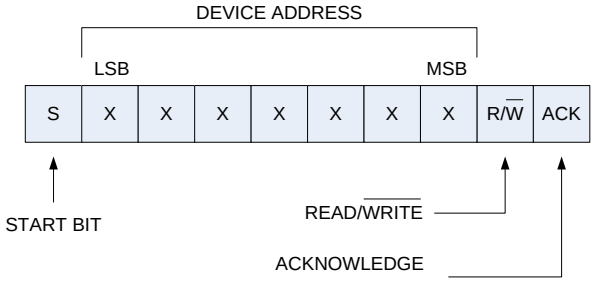
Bus Conditions:

- **Bus not Busy (I)**: Both data and clock lines are HIGH indicating an Idle Condition.
- **Start Data Transfer (S)**: a HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.
- **Stop Data Transfer (P):** a LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.
- **Data Valid:** The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition.
- **Acknowledge (A):** Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this Acknowledge bit. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (MAX78630+PPM) will leave the data line HIGH to enable the master to generate the STOP condition.



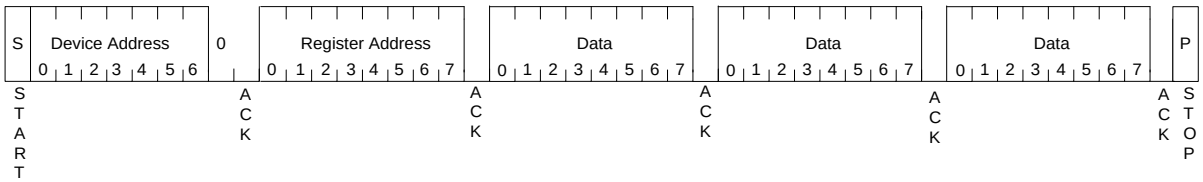
Device Addressing

A control byte is the first byte received following the START condition from the master device.
The control byte consists of a seven bit address and a bit (LSB) indicating the type of access (0=write; 1=read).

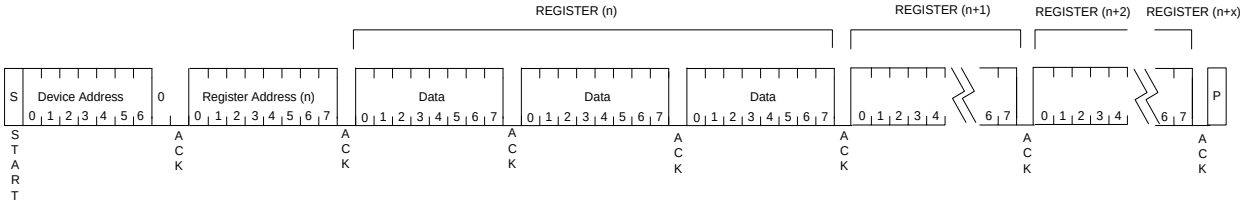


Write Operations

Following the START (S) condition from the master, the device address (7-bits) and the R/W bit (logic low for write) are clocked onto the bus by the master. This indicates to the addressed slave receiver that the register address will follow after it has generated an acknowledge bit (A) during the ninth clock cycle. Therefore, the next byte transmitted by the master is the register address and will be written into the address pointer of the MAX78630+PPM. After receiving another acknowledge (A) signal from the MAX78630+PPM, the master device will transmit the data byte(s) to be written into the addressed memory location. The data transfer ends when the master generates a stop (P) condition. This initiates the internal write cycle. The example below shows a 3-byte data write (24-bit register write).



Upon receiving a STOP (P) condition, the internal register address pointer will be incremented. The write access can be extended to multiple sequential registers. The figure below shows a single transaction with multiple registers written sequentially.

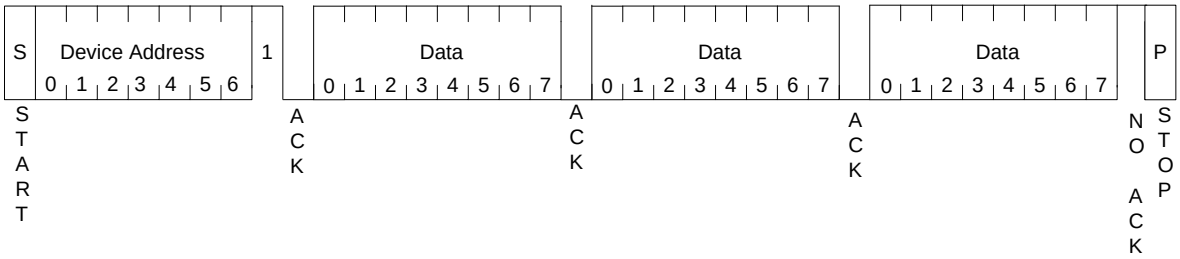


Read Operations

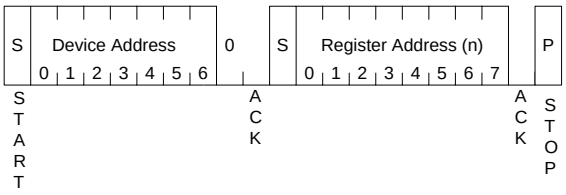
Read operations are initiated in the same way as write operations with the exception that the R/W bit of the control byte is set to one. There are two basic types of read operations: current address read and random read.

Current Address Read: the MAX78630+PPM contains an address counter that maintains the address of the last register accessed, internally incremented by one when the stop bit is received. Therefore, if the previous read access was to register address n, the next current address read operation would access data from address n + 1.

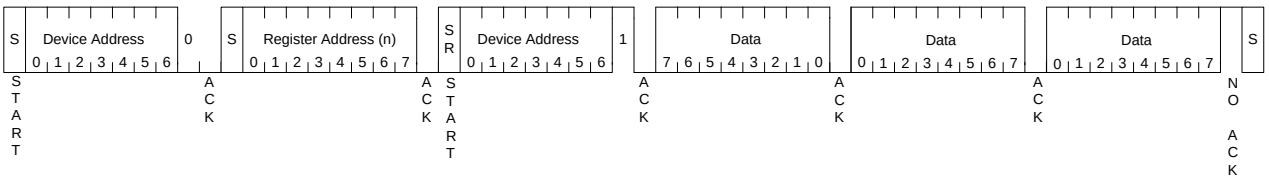
Upon receipt of the control byte with R/W bit set to one, the MAX78630+PPM issues an acknowledge (A) and transmits the eight bit data byte. The master will not acknowledge the transfer, but generates a STOP condition to end the transfer and the MAX78630+PPM will discontinue the transmission.



This read operation is not limited to 3 bytes but can be extended until the register address pointer reaches its maximum value. If the register address pointer has not been set by previous operations, it is necessary to set it issuing a command as follows:



Random Read: random read operations allow the master to access any register in a random manner. To perform this operation, the register address must be set as part of the write operation. After the address is sent, the master generates a start condition following the acknowledge response. This sequence completes the write operation. The master should issue the control byte again this time, with the R/W bit set to 1 to indicate a read operation. The MAX78630+PPM will issue the acknowledge response, and transmit the data. At the end of the transaction the master will not acknowledge the transfer and generate a STOP condition.



This read operation is not limited to 3 bytes but can be extended until the register address pointer reaches its maximum value.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX78630+PPM/D00	-40°C to +85°C	32 TQFN-EP*	EMP
MAX78630+PPM/D00T	-40°C to +85°C	32 TQFN-EP*	EMP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Contact Information

For more information about the MAX78630+PPM or other Maxim Integrated products, go to: **www.maximintegrated.com/support**.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/13	Initial release	—