19-5000; Rev 4; 7/10

# 6/8/10-Channel, 10-Bit, Nonvolatile Programmable Gamma and VCOM Reference Voltages



## General Description

The MAX9665/MAX9666/MAX9667 provide multiple programmable reference voltages for gamma correction in TFT LCDs and a programmable reference voltage for VCOM adjustment. All gamma and VCOM reference voltages have a 10-bit digital-to-analog converter (DAC) and buffer with high peak current. This reduces the recovery time of the output voltage when critical levels and patterns are displayed.

These devices include multiple-time programmable (MTP) memory to store gamma and VCOM codes on the chip, eliminating the need for external EEPROM. The MTP memory supports up to 300 write operations.

The MAX9665/MAX9666/MAX9667 feature an I²C interface to control the programmable reference voltages and a single-wire interface to toggle the VCOM reference voltage up or down.

## Applications

TFT LCDs

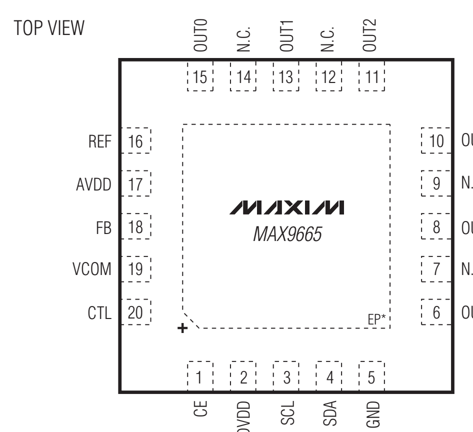
## Ordering Information

| PART | GAMMA CHANNELS | TEMP RANGE | PIN-PACKAGE |
|---|---|---|---|
| **MAX9665**ETP+ | 6 | -40°C to +85°C | 20 TQFN-EP* |
| **MAX9666**ETP+ | 8 | -40°C to +85°C | 20 TQFN-EP* |
| **MAX9667**ETP+ | 10 | -40°C to +85°C | 20 TQFN-EP* |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

**EP = Exposed pad.*

## Pin Configurations




**THIN QFN**
**5mm x 5mm**

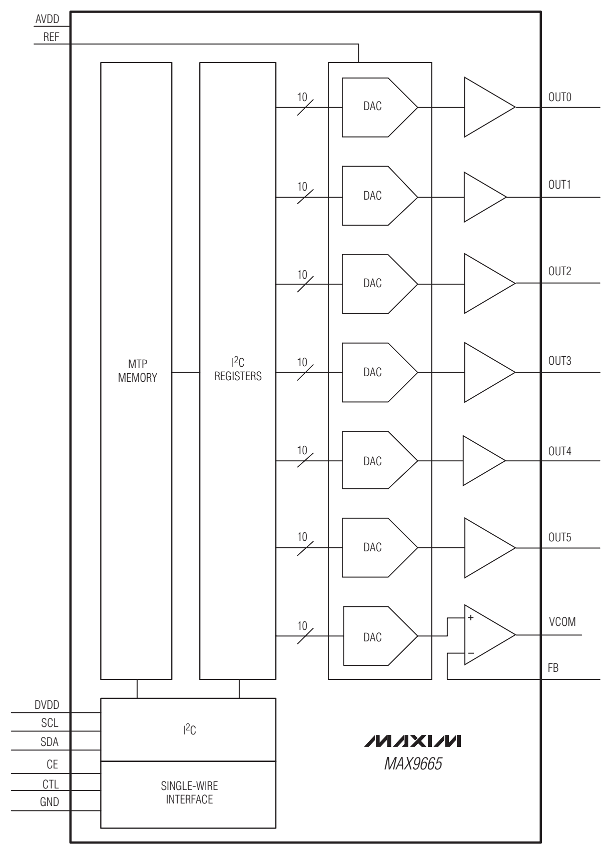
*EP = EXPOSED PAD. CONNECT TO DIGITAL GROUND PLANE.

*Pin Configurations continued at end of data sheet.*

## Features

- ♦ **6/8/10 Channels Gamma Correction, 10-Bit Resolution**
- ♦ **VCOM Driver**
- ♦ **Integrated Multiple-Time Programmable Memory**
- ♦ **DAC Reference Input**
- ♦ **Single-Wire and I²C Programming of VCOM Reference**
- ♦ **950mA Peak Transient Current on VCOM Channel**

## Functional Diagrams




*Functional Diagrams continued at end of data sheet.*

# 6/8/10-Channel, 10-Bit, Nonvolatile Programmable Gamma and VCOM Reference Voltages

## ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- AVDD to GND ....................................................-0.3V to +22V
- DVDD to GND......................................................-0.3V to +4V

Outputs
- OUT0–OUT9, VCOM to GND .............-0.3V to ($V_{AVDD}$ + 0.3V)

Inputs
- SDA, SCL, CE to GND..........................................-0.3V to +4V
- CTL, REF to GND ..............................................-0.3V to +22V
- FB to GND ..........................................-0.3V to ($V_{AVDD}$ + 0.3V)

Continuous Current
- OUT0–OUT9, VCOM..................................................±400mA
- All Other Pins ...............................................................±50mA

Continuous Power Dissipation ($T_A$ = +70°C)
- 20-Pin TQFN (derate 25.6mW/°C above +70°C) ....2051.3mW

Junction-to-Case Thermal Resistance ($\theta_{JC}$) (Note 1)
- 20-Pin TQFN..................................................................6°C/W

Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) (Note 1)
- 20-Pin TQFN................................................................39°C/W

Operating Temperature Range ...........................-40°C to +85°C
Junction Temperature .....................................................+150°C
Storage Temperature Range .............................-65°C to +150°C
Lead Temperature (soldering, 10s) .................................+300°C
Soldering Temperature (reflow) ......................................+260°C

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{AVDD}$ = $V_{REF}$ = 15.7V, $V_{DVDD}$ = 3.3V, $V_{GND}$ = 0V, VCOM connected to FB, CTL = DVDD/2, no load, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SUPPLIES** | | | | | | |
| Analog-Supply Voltage Range | $V_{AVDD}$ | Guaranteed by power-supply rejection ratio specification (Note 3) | 9 | | 20 | V |
| Analog-Supply Voltage Range for Programming MTP | $V_{AVDD\_MTP}$ | | 15 | | 20 | V |
| Digital-Supply Voltage Range | $V_{DVDD}$ | | 2.7 | | 3.6 | V |
| Analog Quiescent Current | $I_{AVDD}$ | MAX9665 | | 12 | 22 | mA |
| | | MAX9666 | | 14 | 24 | |
| | | MAX9667 | | 16 | 26 | |
| Digital Quiescent Current | $I_{DVDD}$ | No SCL or SDA transitions | | 450 | 900 | µA |
| DVDD Undervoltage Lockout | UVLO | | | 2.3 | 2.6 | V |
| **DAC** | | | | | | |
| Resolution | | | 10 | | | Bits |
| Integral Nonlinearity Error | INL | $T_A$ = +25°C, 16 ≤ CODE ≤ 1008 | | | 1 | LSB |
| Differential Nonlinearity Error | DNL | $T_A$ = +25°C, 16 ≤ CODE ≤ 1008 | | | 1 | LSB |
| REF Input Resistance | | | | 384 | | kΩ |
| **GAMMA OUTPUTS (Note 4)** | | | | | | |
| Short-Circuit Current | $I_{SC}$ | Output to AVDD or GND, $T_A$ = +25°C | 100 | 400 | | mA |
| Maximum Capacitive Load | | Placed directly at output | | 300 | | pF |
| Output Impedance | $Z_O$ | Output resistance when output is disabled | | 84 | | kΩ |
| Load Regulation | $R_{EG}$ | -5mA to +5mA | | 0.5 | | mV/mA |
| Total Output Error | | $T_A$ = +25°C, measured at code = 512 | -40 | | +40 | mV |
| Slew Rate | SR | 5V swing, measure 10% to 90% | | 22 | | V/µs |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD}$ = $V_{REF}$ = 15.7V, $V_{DVDD}$ = 3.3V, $V_{GND}$ = 0V, VCOM connected to FB, CTL = DVDD/2, no load, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Low Output Voltage | $V_{MIN}$ | Sinking 4mA, $T_A$ = +25°C | | 0.1 | 0.15 | V |
| High Output Voltage | $V_{MAX}$ | Sourcing 4mA, $T_A$ = +25°C | $V_{AVDD}$ - 0.15 | $V_{AVDD}$ - 0.1 | | V |
| Power-Supply Rejection Ratio | PSRR | To AVDD, f = 60kHz, REF and AVDD shorted | | 40 | | dB |
| | | 9V < $V_{AVDD}$ < 20V, $V_{REF}$ = 9V | 60 | 90 | | |
| Channel-to-Channel Isolation | $C_{XTLK}$ | f = 5MHz, all channels to all channels | | 80 | | dB |
| **GAMMA OUTPUTS (Note 5)** | | | | | | |
| Short-Circuit Current | $I_{SC}$ | Outputs to AVDD or GND, $T_A$ = +25°C | 50 | 200 | | mA |
| Maximum Capacitive Load | | Placed directly at output | | 300 | | pF |
| Output Impedance | $Z_O$ | Output resistance when output is disabled | | 84 | | kΩ |
| Load Regulation | $R_{EG}$ | -5mA to +5mA | | 0.50 | | mV/mA |
| Total Output Error | | $T_A$ = +25°C, measured at code = 512 | -40 | | +40 | mV |
| Slew Rate | SR | Swing $5V_{P-P}$ at input, 10% to 90% measurement on output | | 22 | | V/µs |
| Low Output Voltage | $V_{MIN}$ | Sinking 4mA | | 0.15 | 0.2 | V |
| High Output Voltage | $V_{MAX}$ | Sourcing 4mA | $V_{AVDD}$ - 0.2 | $V_{AVDD}$ - 0.15 | | V |
| Power-Supply Rejection Ratio | PSRR | To AVDD, f = 60kHz, REF and AVDD shorted | | 40 | | dB |
| | | 9V < $V_{AVDD}$ < 20V, $V_{REF}$ = 9V | 60 | 90 | | |
| Thermal Shutdown | | | | 160 | | °C |
| Thermal-Shutdown Hysteresis | | | | 15 | | °C |
| Channel-to-Channel Isolation | $C_{XTLK}$ | f = 5MHz, all channels to all channels | | 80 | | dB |
| **VCOM OUTPUT** | | | | | | |
| Short-Circuit Current | $I_{SC}$ | Outputs to AVDD or GND, $T_A$ = +25°C | 50 | 200 | | mA |
| Maximum Capacitive Load | | Placed directly at output | | 300 | | pF |
| Output Impedance | $Z_O$ | Output resistance when output is disabled | | 84 | | kΩ |
| Load Regulation | $R_{EG}$ | -5mA to +5mA | | ±0.2 | | mV/mA |
| Total Output Error | | $T_A$ = +25°C, measured at code = 512 | -50 | 1 | +50 | mV |
| Slew Rate | SR | Swing $4V_{P-P}$ at VCOM, 10% to 90%, $R_L$ = 10kΩ, $C_L$ = 50pF (Note 6) | | 100 | | V/µs |
| Low Output Voltage | $V_{MIN}$ | Sinking 4mA | | 0.15 | 0.2 | V |
| High Output Voltage | $V_{MAX}$ | Sourcing 4mA | $V_{AVDD}$ - 0.2 | $V_{AVDD}$ - 0.15 | | V |
| Power-Supply Rejection Ratio | PSRR | To AVDD, f = 60kHz, REF and AVDD shorted | | 40 | | dB |
| | | 9V < $V_{AVDD}$ < 20V, $V_{REF}$ = 9V | 70 | | | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD}$ = $V_{REF}$ = 15.7V, $V_{DVDD}$ = 3.3V, $V_{GND}$ = 0V, VCOM connected to FB, CTL = DVDD/2, no load, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SINGLE-WIRE INTERFACE** | | | | | | |
| CE Input Low Voltage | | 2.6V < $V_{DVDD}$ < 3.6V | | | 0.3 x $V_{DVDD}$ | V |
| CE Input High Voltage | | 2.6V < $V_{DVDD}$ < 3.6V | 0.7 x $V_{DVDD}$ | | | V |
| CE Startup Time | | (Note 7) | | | 1 | ms |
| CTL High Voltage | | 2.6V < $V_{DVDD}$ < 3.6V | 0.7 x $V_{DVDD}$ | | 0.82 x $V_{DVDD}$ | V |
| CTL Float Votlage | | 2.6V < $V_{DVDD}$ < 3.6V | 0.4 x $V_{DVDD}$ | | 0.62 x $V_{DVDD}$ | V |
| CTL Low Voltage | | 2.6V < $V_{DVDD}$ < 3.6V | 0.2 x $V_{DVDD}$ | | 0.32 x $V_{DVDD}$ | V |
| CTL Rejected Pulse Width | | | 20 | | | µs |
| CTL Typical Pulse Width | | | | 50 | | µs |
| CTL Minimum Pulse Width | | | | | 200 | µs |
| CTL Minimum Time Between Pulses | | | | | 10 | µs |
| CTL Input Current | | CTL = GND | -10 | | | µA |
| | | CTL = DVDD | | | +10 | |
| **LOGIC INPUTS AND OUTPUTS (SDA, SCL)** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 0.7 x $V_{DVDD}$ | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.3 x $V_{DVDD}$ | V |
| Input Leakage Current | $I_{IH}$, $I_{IL}$ | $V_{SDA/SCL}$ = 0V or $V_{DVDD}$ | -10 | +0.01 | +10 | µA |
| Input Capacitance | | (Note 7) | | 5 | | pF |
| Power-Down Input Current | $I_{SDA/SCL}$ | $V_{DVDD}$ = 0V, $V_{SDA/SCL}$ = 1.98V | -10 | | +10 | µA |
| SDA Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 6mA | | | 0.4 | V |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD}$ = $V_{REF}$ = 15.7V, $V_{DVDD}$ = 3.3V, $V_{GND}$ = 0V, VCOM connected to FB, CTL = DVDD/2, no load, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **I²C TIMING CHARACTERISTICS (Figure 4)** | | | | | | |
| Serial-Clock Frequency | $f_{SCL}$ | | 0 | | 400 | kHz |
| Bus Free Time Between STOP and START Conditions | $t_{BUF}$ | | 1.3 | | | µs |
| Hold Time (Repeated) START Condition | $t_{HD,STA}$ | | 0.6 | | | µs |
| SCL Pulse-Width Low | $t_{LOW}$ | | 1.3 | | | µs |
| SCL Pulse-Width High | $t_{HIGH}$ | | 0.6 | | | µs |
| Setup Time for a Repeated START Condition | $t_{SU,STA}$ | | 0.6 | | | µs |
| Data Hold Time | $t_{HD,DAT}$ | | 0 | | 900 | ns |
| Data Setup Time | $t_{SU,DAT}$ | | 100 | | | ns |
| SDA and SCL Receiving Rise Time | $t_R$ | (Note 8) | 20 + 0.1$C_B$ | | 300 | ns |
| SDA and SCL Receiving Fall Time | $t_F$ | (Note 8) | 20 + 0.1$C_B$ | | 300 | ns |
| SDA Transmitting Fall Time | $t_{F,TX}$ | (Note 8) | 20 + 0.1$C_B$ | | 250 | ns |
| Setup Time for STOP Condition | $t_{SU,STO}$ | | 0.6 | | | µs |
| Bus Capacitance | $C_B$ | | | | 400 | pF |
| Pulse Width of Suppressed Spike | $t_{SP}$ | | 0 | | 50 | ns |

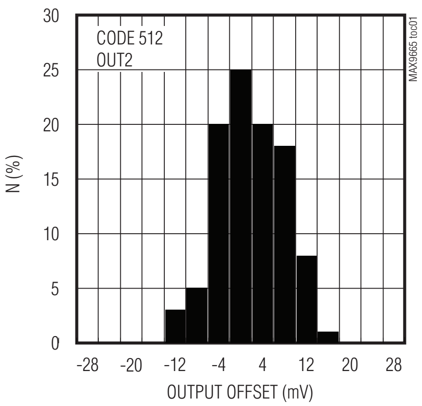
**Note 2:** All devices are 100% production tested at $T_A$ = +25°C. Specifications over temperature limits are guaranteed by design.
**Note 3:** For AVDD below 15.6V, internal LDO must be externally adjusted to meet LDO dropout specification.
**Note 4:** This section applies to OUT0, OUT2, OUT3, and OUT5 of the MAX9665; OUT0, OUT3, OUT4, and OUT7 of the MAX9666; OUT0, OUT4, OUT5, and OUT9 of the MAX9667.
**Note 5:** This section applies to OUT1 and OUT4 of the MAX9665; OUT1, OUT2, OUT5, and OUT6 of the MAX9666; OUT1, OUT2, OUT3, OUT6, OUT7, and OUT8 of the MAX9667.
**Note 6:** Measured with the VCOM amplifier configured as an inverting unity-gain amplifier. $R_F$ = $R_{IN}$ = 10kΩ.
**Note 7:** Guaranteed by design. Not production tested.
**Note 8:** $C_B$ is in pF.

# 6/8/10-Channel, 10-Bit, Nonvolatile Programmable Gamma and VCOM Reference Voltages

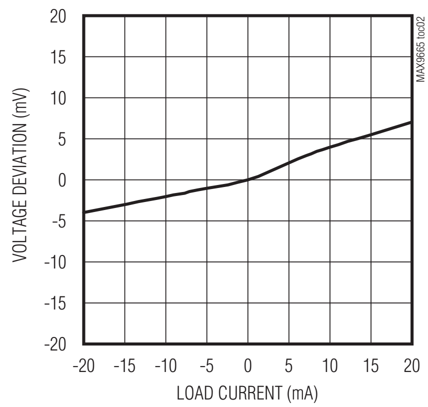
## Typical Operating Characteristics

($V_{AVDD}$ = $V_{REF}$ = 15.7V, $V_{DVDD}$ = 3.3V, $V_{GND}$ = 0V, VCOM connected to FB, CTL = DVDD/2, no load, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

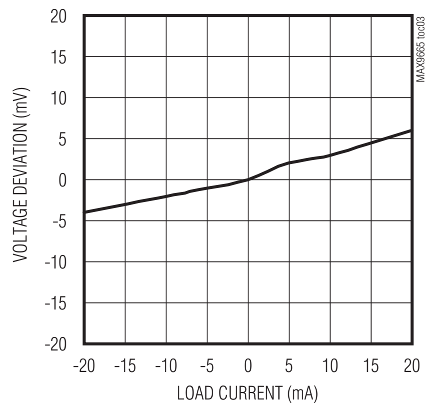
**OUTPUT OFFSET VOLTAGE DISTRIBUTION**



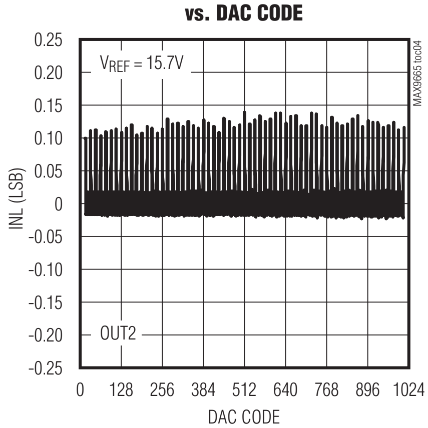

**GAMMA LOAD REGULATION**



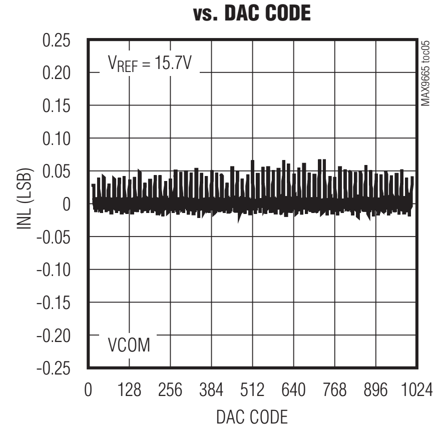

**VCOM LOAD REGULATION**



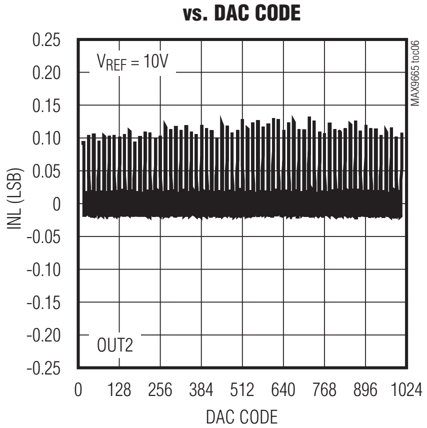

**INTEGRAL NONLINEARITY vs. DAC CODE**



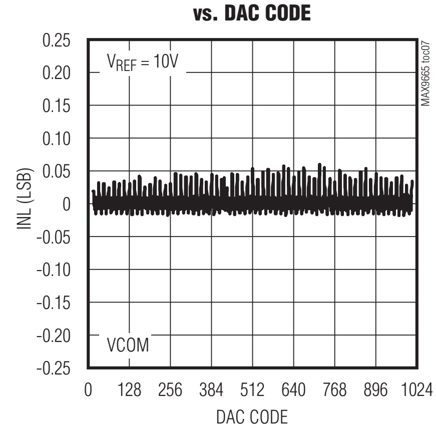

**INTEGRAL NONLINEARITY vs. DAC CODE**




**INTEGRAL NONLINEARITY vs. DAC CODE**



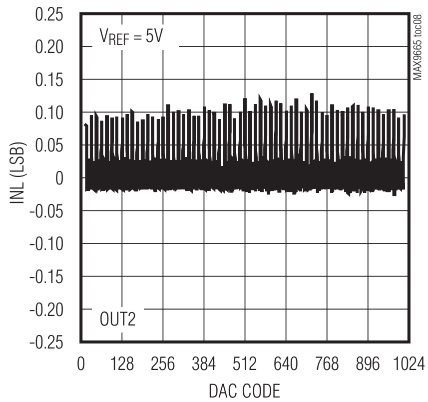

**INTEGRAL NONLINEARITY vs. DAC CODE**



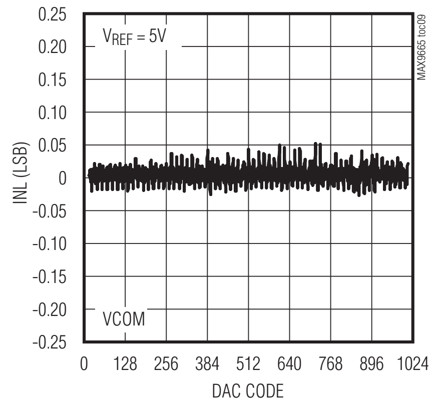
## Typical Operating Characteristics (continued)

($V_{AVDD}$ = $V_{REF}$ = 15.7V, $V_{DVDD}$ = 3.3V, $V_{GND}$ = 0V, VCOM connected to FB, CTL = DVDD/2, no load, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

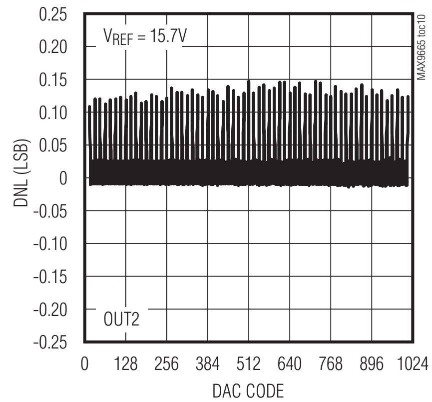
**INTEGRAL NONLINEARITY vs. DAC CODE**



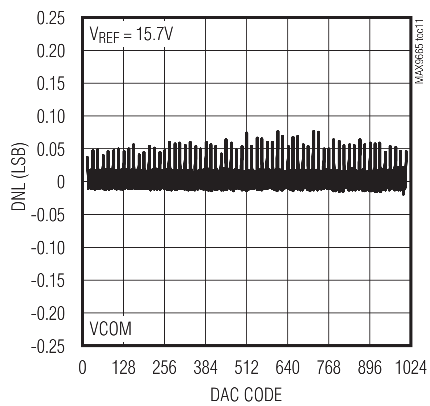

**INTEGRAL NONLINEARITY vs. DAC CODE**



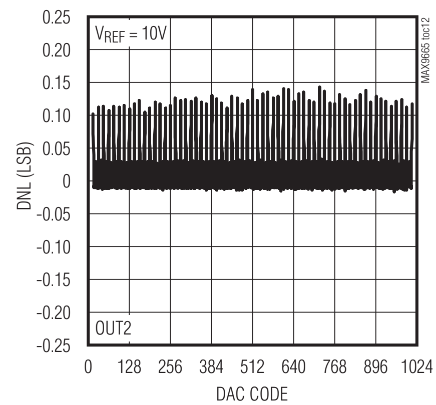

**DIFFERENTIAL NONLINEARITY vs. DAC CODE**



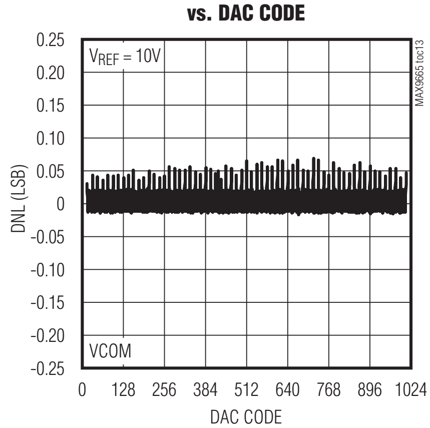

**DIFFERENTIAL NONLINEARITY vs. DAC CODE**



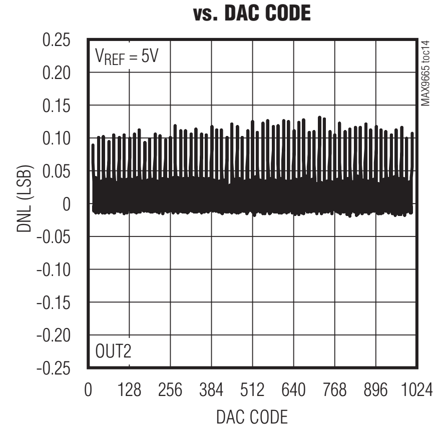

**DIFFERENTIAL NONLINEARITY vs. DAC CODE**




**DIFFERENTIAL NONLINEARITY vs. DAC CODE**




**DIFFERENTIAL NONLINEARITY vs. DAC CODE**

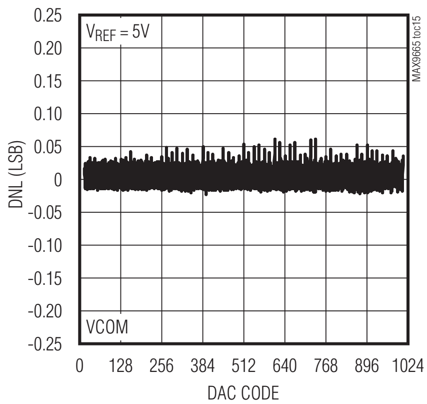


# 6/8/10-Channel, 10-Bit, Nonvolatile Programmable Gamma and VCOM Reference Voltages

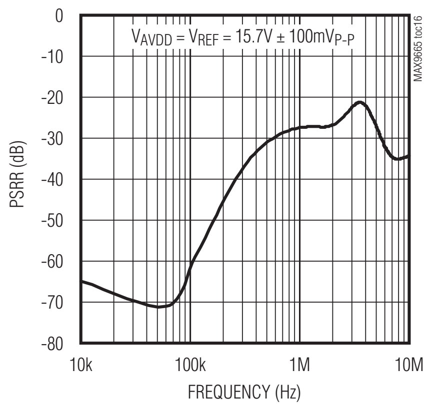
## Typical Operating Characteristics (continued)

($V_{AVDD}$ = $V_{REF}$ = 15.7V, $V_{DVDD}$ = 3.3V, $V_{GND}$ = 0V, VCOM connected to FB, CTL = DVDD/2, no load, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

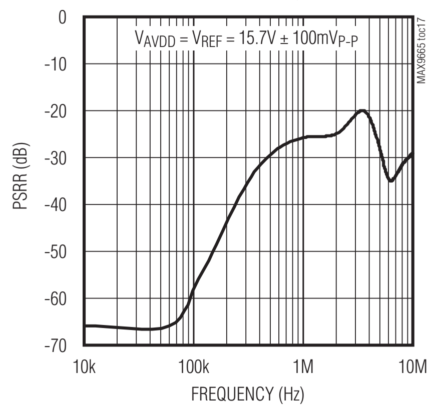
**DIFFERENTIAL NONLINEARITY vs. DAC CODE**



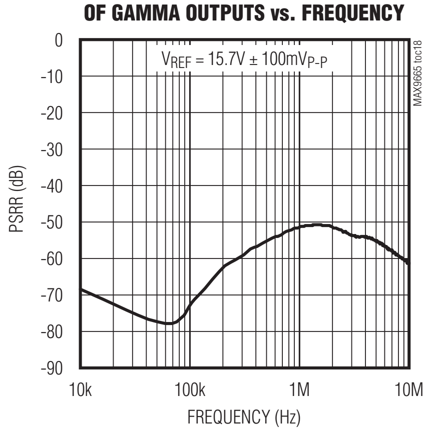

**POWER-SUPPLY REJECTION RATIO OF GAMMA OUTPUTS vs. FREQUENCY**



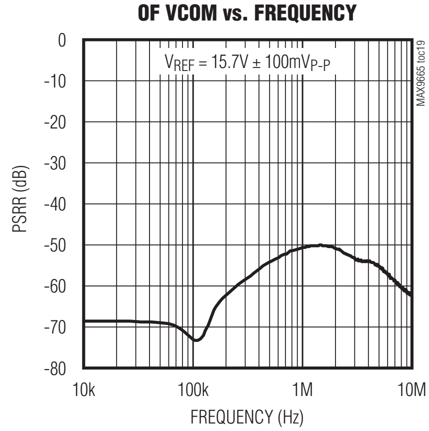

**POWER-SUPPLY REJECTION RATIO OF VCOM vs. FREQUENCY**



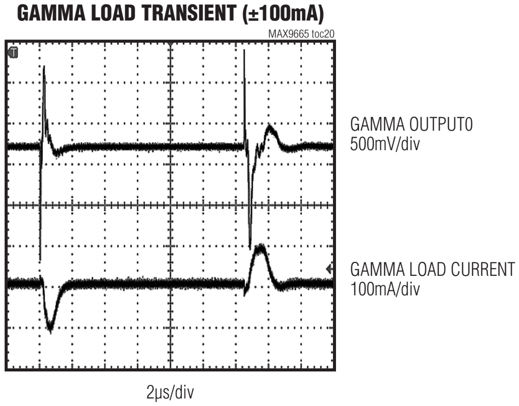

**REF POWER-SUPPLY REJECTION RATIO OF GAMMA OUTPUTS vs. FREQUENCY**



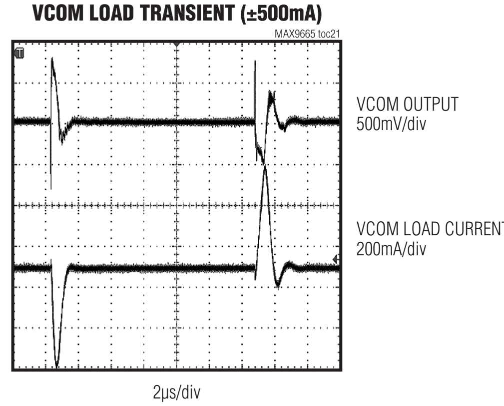

**REF POWER-SUPPLY REJECTION RATIO OF VCOM vs. FREQUENCY**




**GAMMA LOAD TRANSIENT (±100mA)**




**VCOM LOAD TRANSIENT (±500mA)**



## Pin Description

| PIN | | | NAME | FUNCTION |
|---|---|---|---|---|
| MAX9665 | MAX9666 | MAX9667 | | |
| 1 | 1 | 1 | CE | Single-Wire Control Interface Enable. Connect CE to DVDD to enable the CTL input. Connect CE to GND to disable the CTL input and reduce the supply current. |
| 2 | 2 | 2 | DVDD | Digital Supply Input. Bypass to GND with 0.1µF capacitor. |
| 3 | 3 | 3 | SCL | $I^2C$ Serial-Clock Input |
| 4 | 4 | 4 | SDA | $I^2C$ Serial-Data Input/Output |
| 5 | 5 | 5 | GND | Ground |
| — | — | 6 | OUT9 | Gamma Output 9 |
| — | — | 7 | OUT8 | Gamma Output 8 |
| — | 6 | 8 | OUT7 | Gamma Output 7 |
| — | 7 | 9 | OUT6 | Gamma Output 6 |
| 6 | 8 | 10 | OUT5 | Gamma Output 5 |
| 8 | 10 | 11 | OUT4 | Gamma Output 4 |
| 10 | 11 | 12 | OUT3 | Gamma Output 3 |
| 11 | 13 | 13 | OUT2 | Gamma Output 2 |
| 13 | 14 | 14 | OUT1 | Gamma Output 1 |
| 15 | 15 | 15 | OUT0 | Gamma Output 0 |
| 16 | 16 | 16 | REF | Reference Input |
| 17 | 17 | 17 | AVDD | Analog Supply Input. Bypass AVDD to GND with a minimum 0.1µF capacitor. |
| 18 | 18 | 18 | FB | VCOM Amplifier Negative Input |
| 19 | 19 | 19 | VCOM | VCOM Amplifier Output |
| 20 | 20 | 20 | CTL | VCOM Adjustment and Multiple-Time Programmable Memory Control. CTL sets the internal DAC code and programs the MTP memory. A pulse-control method is used to adjust the VCOM level. See the *VCOM Adjustment (CTL)* section. To program the DAC setting into the MTP memory as the power-on default, drive CTL to the MTP programming voltage using the correct timing and voltage ramp rates. See the *MTP Programming (CTL)* section. |
| 7, 9, 12, 14 | 9, 12 | — | N.C. | No Connection. Not internally connected. |
| — | — | — | EP | Exposed Pad. The exposed pad must be connected to GND. |

## Detailed Description

The MAX9665/MAX9666/MAX9667 are a family of multichannel, programmable reference voltages. Each channel has a 10-bit DAC to create the reference voltage. One channel has an operational amplifier that follows the DAC while all other channels have a buffer after the DAC. The user can program the DAC codes into on-chip nonvolatile memory, which is called multiple-time programmable (MTP) memory since data can be written into it up to 300 times.

The MAX9665/MAX9666/MAX9667 provide the gamma, VCOM, and level shifter reference voltages in a LCD panel. A single chip can potentially replace a discrete digital variable resistor (DVR), VCOM amplifier, gamma buffers, high-voltage linear regulator, and resistor strings. The high-voltage linear regulator can be eliminated because the DAC contains a lowpass filter that reduces horizontal line frequency noise by 40dB. Power sequencing is well-controlled since a single chip generates all the various reference voltages needed for the LCD panel.

Each part has an $I^2C$ interface for programming both the MTP memory and the $I^2C$ registers. For compatibility with legacy flicker adjustment production equipment, these devices include a single-wire interface that is compatible with the MAX1512.

With the MTP memory and the $I^2C$ interface, these devices enable automatic gamma and flicker calibration on a panel-by-panel basis on the production line. Contact your Maxim representative for more details.

### 10-Bit Digital-to-Analog Converters

The reference input, REF, accepts a DC voltage between ground (GND) and the analog supply voltage (AVDD). The voltage at REF sets the full-scale output of the DACs. Determine the output voltage using the following equations:

$$V_{OUT} = (V_{REF} \times CODE)/2^N$$

where CODE is the numeric value of the DAC's binary input code and N is the bits of resolution. For the MAX9665 family, N = 10 and CODE ranges from 0 to 1023.

Note that even if REF is less than AVDD, the DAC can never output REF because the maximum value of CODE is always one LSB less than the reference. For example, if REF = 16V and CODE = 1023, then the output voltage is:

$$V_{OUT} = (16V \times 1023)/2^{10} = 15.98438V$$

### Gamma Buffers

There are two types of DAC output buffers: 5mA and 10mA. The 5mA buffer is guaranteed to source or sink 5mA of DC current within 0.2V of the supplies, and the 10mA buffer does the same with 10mA. The 10mA buffers should be attached to the ends of the resistor ladders that set the transfer function of the source driver (look at the connections from OUT0, OUT4, OUT5, and OUT9 on the typical operating circuit of the MAX9667). The 5mA buffers should be attached to the middle tap points of the resistor ladder because those places require less current than the ends (see the connections from OUT1, OUT2, OUT7, and OUT8 on the typical operating circuit of the MAX9667).

If the 10mA buffers cannot provide enough current to drive the ends of the resistor ladders, attach an additional resistor from the nearest supply. For example, at the very top of the resistor ladder, attach an additional resistor to AVDD. At the very bottom of the resistor ladder, attach an additional resistor to GND. The MAX9665/MAX9666/MAX9667 greatly diminish any noise from the AVDD supply through the discrete resistor because the high-frequency noise from REF has been attenuated, and the buffers have excellent AC PSRR. See Figure 1.

The source drivers can kick back a great deal of current to the buffer outputs during a horizontal line change or a polarity switch. The 5mA DAC output buffers can source/sink 200mA of peak transient current, and the 10mA DAC output buffers can source/sink 400mA of peak transient current to reduce the recovery time of the output voltages when critical levels and patterns are displayed.

### VCOM Amplifier

The operational amplifier attached to the bottom DAC holds the VCOM voltage stable while providing the ability to source and sink 400mA into the backplane of a TFT-LCD panel. The operational amplifier can directly drive the capacitive load of the TFT-LCD backplane without the need for a series resistor in most cases. The VCOM amplifier has current limiting on its output to protect its bond wires.

The output (VCOM) and negative input (FB) of the operational amplifier are typically connected together in a unity-gain configuration. If higher output current is required, add an npn emitter follower and a pnp emitter follower in the feedback loop.

If a higher, closed-loop gain is desired, add feedback resistors as shown in Figure 2.

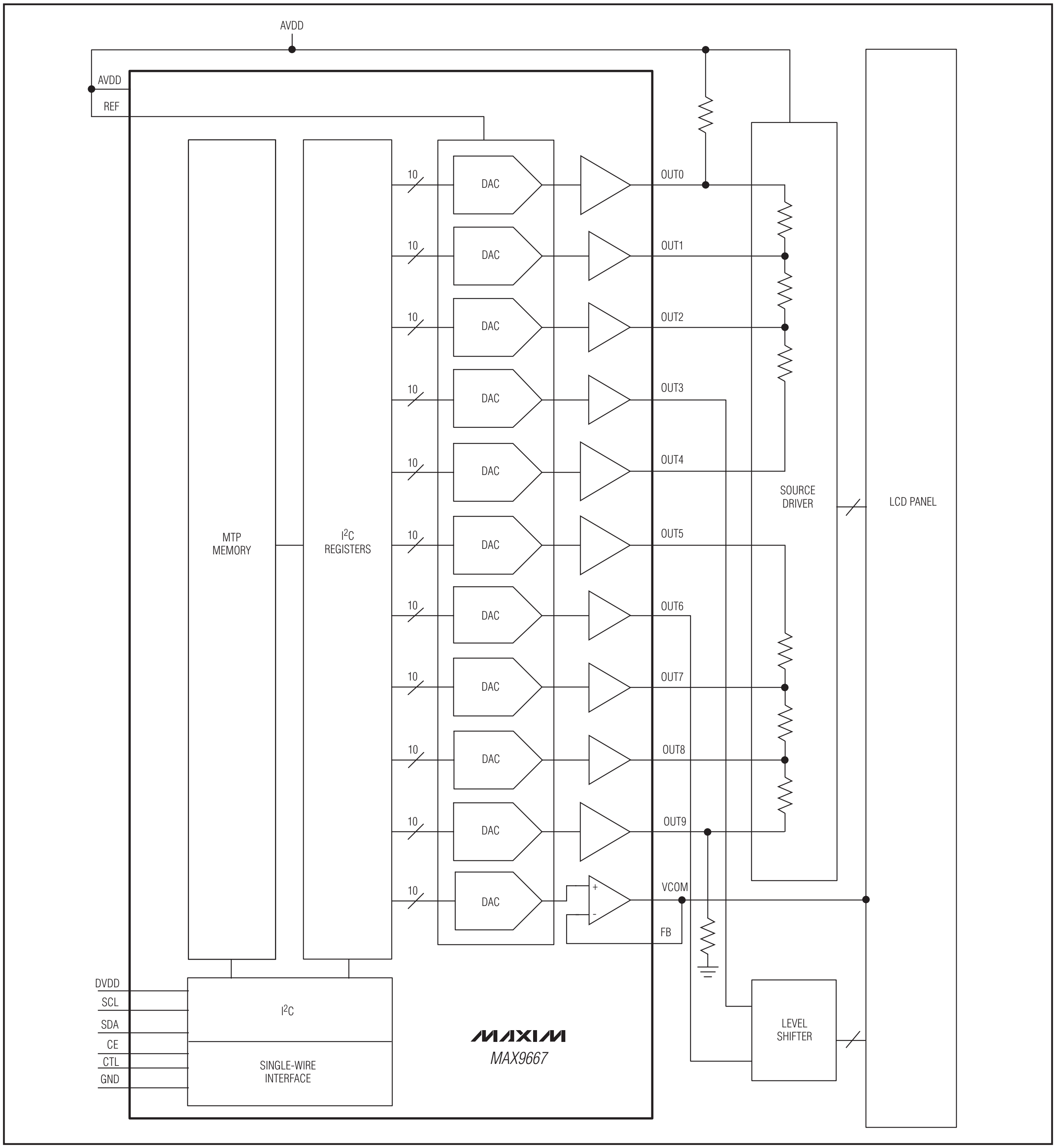



*Figure 1. Pullup and Pulldown Resistors Attached to Source Driver*

# 6/8/10-Channel, 10-Bit, Nonvolatile Programmable Gamma and VCOM Reference Voltages

### Multiple-Time Programmable (MTP) Memory

MTP memory, which is a form of nonvolatile memory, stores the DAC code values even when the chip is not powered. When the chip is powered up, the code values are automatically transferred from MTP memory to the I²C registers. See the *Power-On Reset (POR)/Power-Up* section for more details.

The user can program DAC codes into MTP memory for up to 300 times. In conventional TFT-LCD applications, a resistor string creates the gamma voltages. MTP memory eliminates the resistor string and the need to change manually the resistor values when searching for the optimal gamma curve for a new TFT-LCD panel model.

### Power-On Reset (POR)/Power-Up

The POR circuit that monitors DVDD ensures that all I²C registers are reset to their MTP values upon power-up or POR. Once DVDD rises above 2.4V (typ), the POR circuit releases the I²C registers and the values stored in MTP are loaded. Should DVDD drop to less than 2.4V typical, then the contents of the registers can no longer be guaranteed and a reset is generated. When DVDD rises back above the POR voltage, the values stored in MTP are loaded back into the I²C registers.

The transfer time of the MTP registers to I²C registers is 300µs typical and is less than 400µs in the worst case. During this time, AVDD should not be powered up, and the I²C does not acknowledge any commands (the I²C only starts acknowledging commands after all registers have been loaded from MTP).

### Thermal Protection

When the die temperature reaches +165°C, all gamma buffers except for the middle ones are disabled. See Table 1.

When the die cools down by 15°C, all the buffers are enabled again.

The VCOM operational amplifier does not have thermal protection.

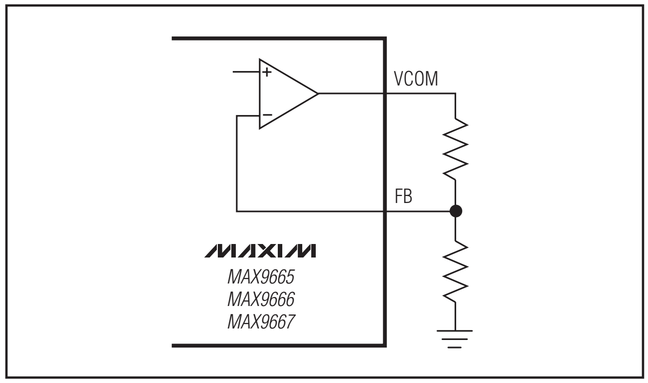



*Figure 2. VCOM Operational Amplifier with Feedback Resistors*

## Digital Interfaces

The MAX9665/MAX9666/MAX9667 have two digital interfaces: I²C and single-wire. Through the I²C interface, the user can change all the registers and program MTP memory. The I²C interface is the more general purpose of the two interfaces.

The single-wire interface, which is compatible with the MAX1512 digital interface, is included to support TFT-LCD production lines that depend upon the single-wire interface to adjust the VCOM voltage to minimize flicker. Note that the single-wire interface cannot program the gamma registers or gamma MTP memory.

### Interoperability Between the Single-Wire Interface and the I²C Interface

To prevent any collision between the single-wire interface and the I²C interface, operation through one interface is only allowed if the other is in the idle state. For example, if the I²C interface is in the middle of executing a command, any input through the single-wire interface is ignored. Conversely, if the single-wire interface is in the middle of executing a command, the I²C interface does not acknowledge any commands.

**Table 1. Buffer Output Status During Thermal Shutdown**

| PART | ENABLED | DISABLED |
|---|---|---|
| MAX9665 | OUT2 and OUT3 | OUT0, OUT1, OUT4, OUT5 |
| MAX9666 | OUT3 and OUT4 | OUT0, OUT1, OUT2, OUT5, OUT6, OUT7 |
| MAX9667 | OUT4 and OUT5 | OUT0, OUT1, OUT2, OUT3, OUT6, OUT7, OUT8, OUT9 |

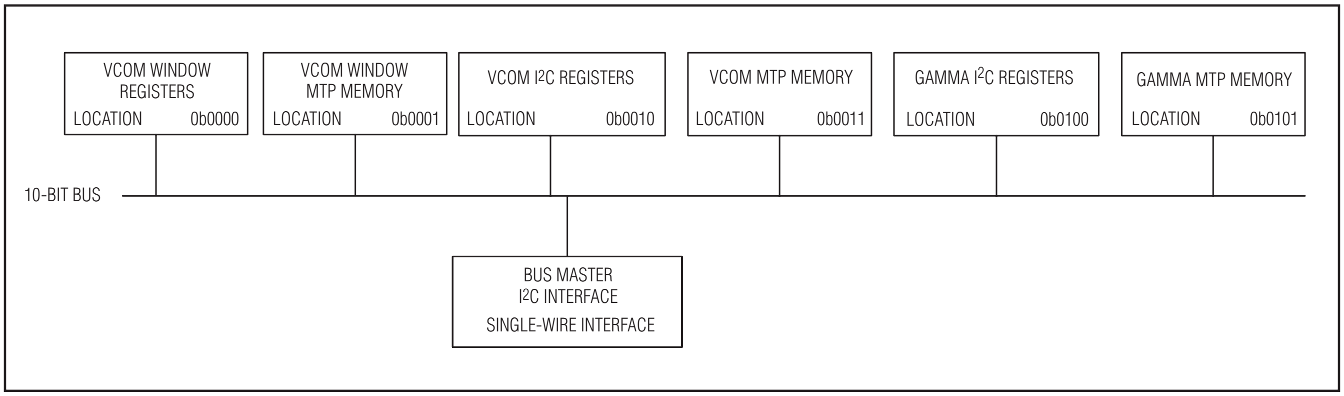



*Figure 3. 10-Bit Bus*

### Bus Architecture

The internal memory, both volatile and nonvolatile, is divided into blocks that are connected by a 10-bit bus (Figure 3).

The $I^2C$ registers (volatile memory) are 8 bits wide. Two $I^2C$ registers are needed to hold one 10-bit DAC code. The $I^2C$ registers are separated into blocks that are distinguished by whether they hold VCOM DAC codes or gamma DAC codes. MTP memory (nonvolatile memory) is organized in the same manner. The VCOM MTP memory has enough bits to store the single VCOM DAC code. Likewise, the gamma MTP memory has enough bits to store all of the gamma DAC codes. Each block connected to the 10-bit bus has a unique location number with one exception. The block that contains the bus master, $I^2C$ interface, and the single-wire interface does not store any data, and hence, it does not have a location number.

Although the external $I^2C$ interface transfers data in units of 8 bits (1 byte), the internal bus that connects the $I^2C$ registers, MTP memory, and digital interfaces is 10 bits wide because the DAC code size is 10 bits. The 10-bit bus can also accommodate data transfers of fewer than 10 bits since communication to the outside world is through either an 8-bit $I^2C$ interface or a 1-bit single-wire interface. Writing a single byte to any address location is ignored.

The 10-bit bus connects together registers, MTP memories, and digital interfaces. The bus master resides in the same block as the $I^2C$ interface and the single-wire interface.

### VCOM MTP Programming

#### Through the $I^2C$ Interface

To program VCOM MTP memory, the $I^2C$ master must first write the DAC code that is to be stored into the VCOM $I^2C$ registers. Next, the $I^2C$ master must send a command to move the data in the VCOM $I^2C$ registers to the VCOM MTP memory, thereby finishing the programming.

To read VCOM MTP memory, the $I^2C$ master must issue a command to move the data in the VCOM MTP memory to the VCOM $I^2C$ registers. Then it can read the two VCOM $I^2C$ registers.

To program gamma MTP memory, the $I^2C$ master must first write the complete set of gamma DAC codes into the gamma $I^2C$ registers. For example, six gamma DAC codes must be written into the MAX9665 since it has six gamma outputs. Next, the $I^2C$ master must send a command to move the data in the gamma $I^2C$ registers to the gamma MTP memory.

To read gamma MTP memory, the $I^2C$ master must issue a command to move the data in the gamma MTP memory to the gamma $I^2C$ registers. Then it can read the gamma $I^2C$ registers.

During MTP programming, the parts do not respond to the $I^2C$ interface. The part generates an acknowledge to the MTP programming command, but the $I^2C$ interface does not generate further acknowledge signals until MTP programming is complete.

If the analog supply voltage is not greater than the minimum required for MTP programming, the $I^2C$ still acknowledges the MTP write command, but MTP programming is disabled. The $I^2C$ continues to acknowledge and process non-MTP write commands.

See the *Register Description* section for further explanation on how to execute commands.

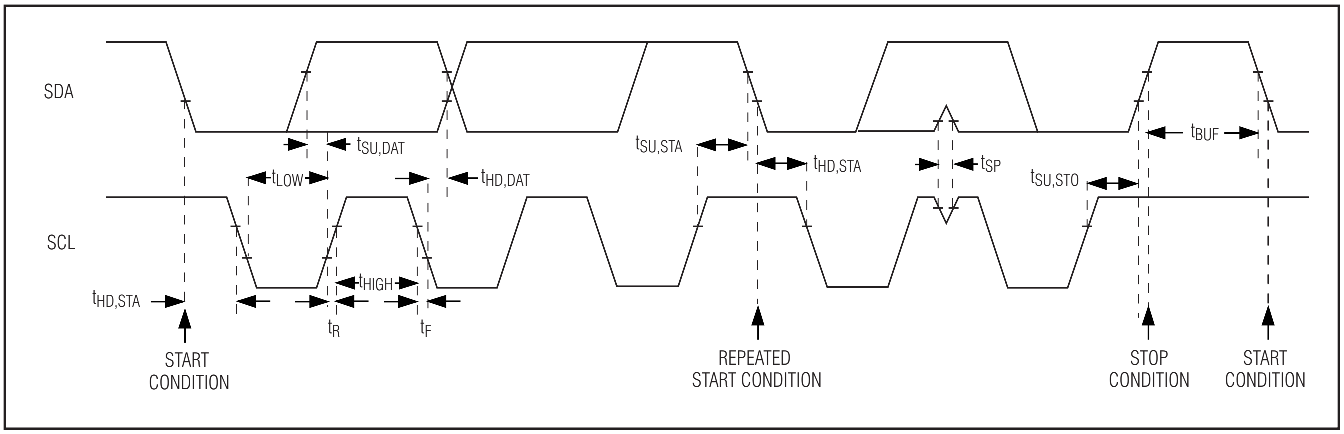



*Figure 4. I²C Serial-Interface Timing Diagram*

### *Through the Single-Wire Interface*

For VCOM MTP programming through the single-wire interface, see the *Single-Wire Interface* section.

### *VCOM Programming Range*

Two registers, VCOMMIN and VCOMMAX, are provided to set the minimum and maximum VCOM register value. These two registers are accessed through the I²C interface and can be written to and read from MTP memory. If any adjustment, either through I²C or the single-wire interface takes the VCOM register value less than VCOMMIN, then the value in VCOMMIN is stored in the VCOM register. Similarly, if any adjustment, either through I²C or the single-wire interface takes the VCOM register value greater than VCOMMAX, then the value in VCOMMAX is stored in the VCOM register.

## *I²C Interface*

The MAX9665/MAX9666/MAX9667 feature an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the devices and the master at clock rates up to 400kHz. Figure 4 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. A master device writes data to the devices by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX9665/MAX9666/MAX9667 is 8 bits long and followed by an acknowledge clock pulse. A master reading data from the devices transmits the proper slave address followed by a series of nine SCL pulses. The devices transmit data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on the SDA bus. SCL operates as only an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the devices from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

### *Bit Transfer*

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

### *START and STOP Conditions*

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 5). A START condition from the master signals the beginning of a transmission to the MAX9665/MAX9666/MAX9667. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

*SMBus is a trademark of Intel Corp.*

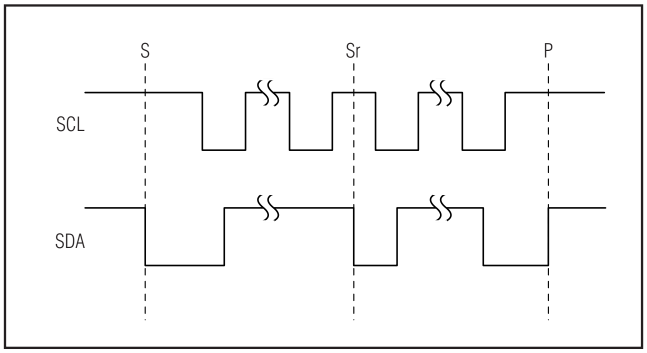


*Figure 5. START, STOP, and REPEATED START Conditions*

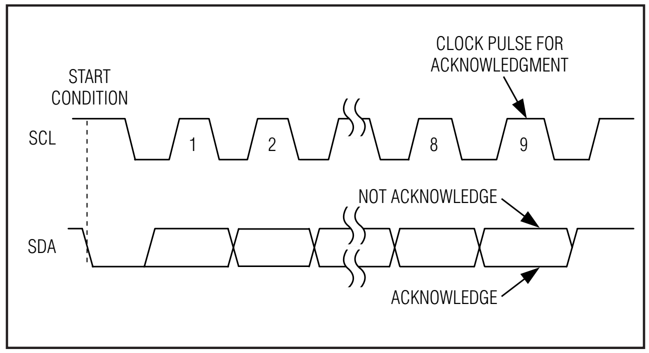


*Figure 6. Acknowledge*

### *Early STOP Conditions*

The MAX9665/MAX9666/MAX9667 recognize a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

### *Slave Address*

The slave address is defined as the 7 most significant bits (MSBs) followed by the read/write (R/$\overline{W}$) bit. Set the R/$\overline{W}$ bit to 1 to configure the MAX9665/MAX9666/MAX9667 to read mode. Set the R/$\overline{W}$ bit to 0 to configure the MAX9665/MAX9666/MAX9667 to write mode. The address is the first byte of information sent to the MAX9665/MAX9666/MAX9667 after the START condition. The MAX9665/MAX9666/MAX9667 slave address is 0x9E for writing and 0x9F for reading.

### *Acknowledge*

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9665/MAX9666/MAX9667 use to handshake receipt of each byte of data when in write mode (see Figure 6). The MAX9665/MAX9666/MAX9667 pull down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may retry communication. The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the MAX9665/MAX9666/MAX9667 are in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX9665/MAX9666/MAX9667, followed by a STOP condition.

## Table 2. Slave ID Description

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | WRITE ADDRESS (hex) | READ ADDRESS (hex) |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | R/$\overline{W}$ | 0x9E | 0x9F |

### Write Data Format

A write to the MAX9665/MAX9666/MAX9667 consists of transmitting a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one data byte of data to configure the internal register address pointer, one or more data bytes, and a STOP condition. Figure 7 illustrates the frame format for writing one byte of data to the MAX9665/MAX9666/MAX9667.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX9665/MAX9666/MAX9667. The MAX9665/MAX9666/MAX9667 acknowledge receipt of the address byte during the master-generated ninth SCL pulse.

The second byte transmitted from the master configures the MAX9665/MAX9666/MAX9667's internal register address pointer. The pointer tells the MAX9665/MAX9666/MAX9667 where to write the next byte of data. An acknowledge pulse is sent by the MAX9665/MAX9666/MAX9667 upon receipt of the address pointer data.

The third byte sent to the MAX9665/MAX9666/MAX9667 contains the data that is written to the chosen register. An acknowledge pulse from the MAX9665/MAX9666/MAX9667 signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential register address locations within one continuous frame. The master signals the end of transmission by issuing a STOP condition.

### Read Data Format

The master presets the address pointer by first sending the MAX9665/MAX9666/MAX9667's slave address with the R/$\overline{W}$ bit set to 0 followed by the register address after a START condition. The MAX9665/MAX9666/MAX9667 acknowledge receipt of the slave address and the register address by pulling SDA low during the ninth SCL clock pulse. A REPEATED START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX9665/MAX9666/MAX9667 transmit the contents of the specified register. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from the register address location set by the previous transaction and not 0x00 and subsequent reads autoincrement the address pointer until the next STOP condition. Attempting to read from register addresses higher than the highest valid address locations (0x13 for MAX9665, 0x17 for MAX9666, 0x1B for MAX9667) in repeated reads from a dummy register containing all one data. The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figures 8 and 9 illustrate the frame format for reading data from the MAX9665/MAX9666/MAX9667.

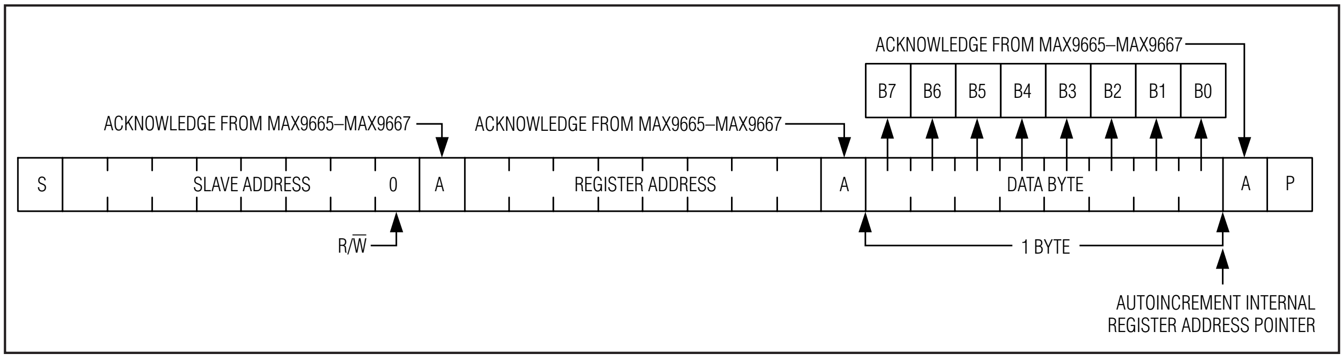



*Figure 7. Writing One Byte of Data to the MAX9665/MAX9666/MAX9667*

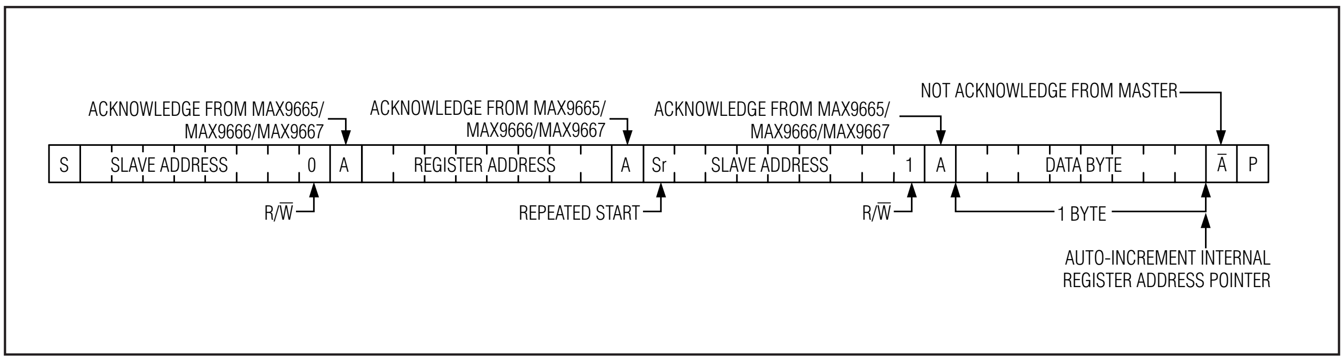



*Figure 8. Reading One Indexed Byte of Data from the MAX9665/MAX9666/MAX9667*

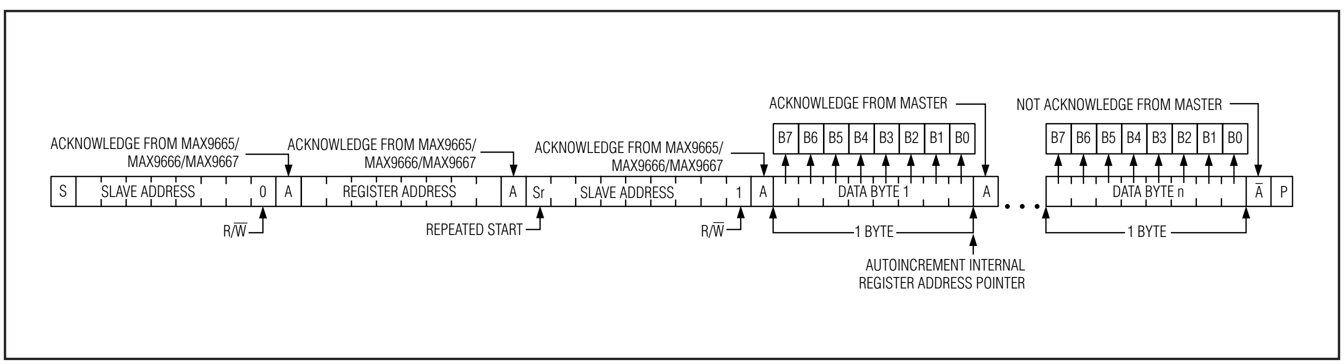



*Figure 9. Reading n Bytes of Indexed Data from the MAX9665/MAX9666/MAX9667*

# 6/8/10-Channel, 10-Bit, Nonvolatile Programmable Gamma and VCOM Reference Voltages

### *Register Map*

The I²C interface was architected for 8-bit systems. With the increase in DAC resolution from 8 bits to 10 bits, 2 bytes must be transferred to get 10 bits. Therefore, the word size is 2 bytes (16 bits) in the register map. Byte order is big endian. The least significant byte (LSB) holds the bottom 8 bits of the 10-bit data, while the most significant byte (MSB) holds the top 2 bits of the 10-bit data. The I²C stores each 10-bit DAC code in two 8-bit registers, as shown in the register maps of Tables 3, 4, and 5.

## Table 3. Register Map for MAX9665

| LEAST SIGNIFICANT BYTE | | MOST SIGNIFICANT BYTE | | COMMENTS |
|---|---|---|---|---|
| REGISTER ADDRESS | REGISTER NAME | REGISTER ADDRESS | REGISTER NAME | |
| 0x01 | CMD_OPND | 0x00 | CMD_OPRN | Command |
| 0x03 | VCOMMIN_L | 0x02 | VCOMMIN_M | VCOM (minimum) |
| 0x05 | VCOMMAX_L | 0x04 | VCOMMAX_M | VCOM (maximum) |
| 0x07 | VCOM_L | 0x06 | VCOM_M | VCOM |
| 0x09 | GMA0_L | 0x08 | GMA0_M | Gamma 0 |
| 0x0B | GMA1_L | 0x0A | GMA1_M | Gamma 1 |
| 0x0D | GMA2_L | 0x0C | GMA2_M | Gamma 2 |
| 0x0F | GMA3_L | 0x0E | GMA3_M | Gamma 3 |
| 0x11 | GMA4_L | 0x10 | GMA4_M | Gamma 4 |
| 0x13 | GMA5_L | 0x12 | GMA5_M | Gamma 5 |

## Table 4. Register Map for MAX9666

| LEAST SIGNIFICANT BYTE | | MOST SIGNIFICANT BYTE | | COMMENTS |
|---|---|---|---|---|
| REGISTER ADDRESS | REGISTER NAME | REGISTER ADDRESS | REGISTER NAME | |
| 0x01 | CMD_OPND | 0x00 | CMD_OPRN | Command |
| 0x03 | VCOMMIN_L | 0x02 | VCOMMIN_M | VCOM (minimum) |
| 0x05 | VCOMMAX_L | 0x04 | VCOMMAX_M | VCOM (maximum) |
| 0x07 | VCOM_L | 0x06 | VCOM_M | VCOM |
| 0x09 | GMA0_L | 0x08 | GMA0_M | Gamma 0 |
| 0x0B | GMA1_L | 0x0A | GMA1_M | Gamma 1 |
| 0x0D | GMA2_L | 0x0C | GMA2_M | Gamma 2 |
| 0x0F | GMA3_L | 0x0E | GMA3_M | Gamma 3 |
| 0x11 | GMA4_L | 0x10 | GMA4_M | Gamma 4 |
| 0x13 | GMA5_L | 0x12 | GMA5_M | Gamma 5 |
| 0x15 | GMA6_L | 0x14 | GMA6_M | Gamma 6 |
| 0x17 | GMA7_L | 0x16 | GMA7_M | Gamma 7 |

### Table 5. Register Map for MAX9667

| LEAST SIGNIFICANT BYTE | | MOST SIGNIFICANT BYTE | | COMMENTS |
|---|---|---|---|---|
| REGISTER ADDRESS | REGISTER NAME | REGISTER ADDRESS | REGISTER NAME | |
| 0x01 | CMD_OPND | 0x00 | CMD_OPRN | Command |
| 0x03 | VCOMMIN_L | 0x02 | VCOMMIN_M | VCOM (minimum) |
| 0x05 | VCOMMAX_L | 0x04 | VCOMMAX_M | VCOM (maximum) |
| 0x07 | VCOM_L | 0x06 | VCOM_M | VCOM |
| 0x09 | GMA0_L | 0x08 | GMA0_M | Gamma 0 |
| 0x0B | GMA1_L | 0x0A | GMA1_M | Gamma 1 |
| 0x0D | GMA2_L | 0x0C | GMA2_M | Gamma 2 |
| 0x0F | GMA3_L | 0x0E | GMA3_M | Gamma 3 |
| 0x11 | GMA4_L | 0x10 | GMA4_M | Gamma 4 |
| 0x13 | GMA5_L | 0x12 | GMA5_M | Gamma 5 |
| 0x15 | GMA6_L | 0x14 | GMA6_M | Gamma 6 |
| 0x17 | GMA7_L | 0x16 | GMA7_M | Gamma 7 |
| 0x19 | GMA8_L | 0x18 | GMA8_M | Gamma 8 |
| 0x1B | GMA9_L | 0x1A | GMA9_M | Gamma 9 |

#### *Register Description*

The I²C registers either hold DAC codes or commands (see Tables 6, 7, and 8). After power-up, the digital circuitry loads the values stored in MTP memory into the VCOM and gamma registers. This process takes approximately 350µs. During this time, the I²C does not respond to any commands (either from the user or from the single-wire interface). To ensure the gamma chip does not reverse bias, the source driver, the VCOM DAC code, and the gamma DAC codes upon power-up are as shown in the Tables 6, 7, and 8.

The I²C master can write a command such as MOV (move) into a pair of command registers. To execute a valid command, the command operation (CMD_OPRN) and command operand (CMD_OPND) registers must be written to sequentially in the same I²C transaction (between the same I²C start/stop).

The form of the command is shown below:

| Operation | Operands |
|---|---|

To move data from gamma registers to gamma MTP memory, use the following command (essentially, data is being written into MTP memory):

| MOV | MOV Gamma Registers | Gamma MTP |
|---|---|---|

MOV is the operation. Gamma registers and gamma MTP memory are operands. Both the operation and the operands must be assembled into machine code that is written into the command registers. The machine code for the operation must be written into the command operation register (CMD_OPRN). The machine code for the operands (if there are any) must be written into command operand register (CMD_OPND). Table 9 shows the list of operations and operands.

## Table 6. MAX9665 Register Description

| REGISTER ADDRESS | REGISTER NAME | REGISTER DESCRIPTION | BIT | | | | | | | | POWER-ON RESET VALUE | MTP FACTORY INITIALIZATION VALUE | READ AND WRITE? |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
| 0x00 | CMD_OPRN | Command operation | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | Not applicable | Write only |
| 0x01 | CMD_OPND | Command operand | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | Not applicable | Write only |
| 0x02 | VCOMMIN_M | VCOMMIN (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x00 | 0x00 | Read and write |
| 0x03 | VCOMMIN_L | VCOMMIN (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | 0x00 | Read and write |
| 0x04 | VCOMMAX_M | VCOMMAX (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x03 | 0x03 | Read and write |
| 0x05 | VCOMMAX_L | VCOMMAX (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0xFF | 0xFF | Read and write |
| 0x06 | VCOM_M | VCOM (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x02 | 0x02 | Read and write |
| 0x07 | VCOM_L | VCOM (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | 0x00 | Read and write |
| 0x08 | GMA0_M | Gamma 0 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x03 | 0x03 | Read and write |
| 0x09 | GMA0_L | Gamma 0 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x80 | 0x80 | Read and write |
| 0x0A | GMA1_M | Gamma 1 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x03 | 0x03 | Read and write |
| 0x0B | GMA1_L | Gamma 1 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | 0x00 | Read and write |
| 0x0C | GMA2_M | Gamma 2 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x02 | 0x02 | Read and write |

***Note:** d0, d1, d2, d3, d4, d5, d6, d7, d8, d9 = valid data bits; x = don't care.*

## Table 6. MAX9665 Register Description (continued)

| REGISTER ADDRESS | REGISTER NAME | REGISTER DESCRIPTION | BIT | | | | | | | | POWER-ON RESET VALUE | MTP FACTORY INITIALIZATION VALUE | READ AND WRITE? |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
| 0x0D | GMA2_L | Gamma 2 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x80 | 0x80 | Read and write |
| 0x0E | GMA3_M | Gamma 3 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x01 | 0x01 | Read and write |
| 0x0F | GMA3_L | Gamma 3 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x80 | 0x80 | Read and write |
| 0x10 | GMA4_M | Gamma 4 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x01 | 0x01 | Read and write |
| 0x11 | GMA4_L | Gamma 4 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | 0x00 | Read and write |
| 0x12 | GMA5_M | Gamma 5 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x00 | 0x00 | Read and write |
| 0x13 | GMA5_L | Gamma 5 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x80 | 0x80 | Read and write |

***Note:*** *d0, d1, d2, d3, d4, d5, d6, d7, d8, d9 = valid data bits; x = don't care.*

# 6/8/10-Channel, 10-Bit, Nonvolatile Programmable Gamma and VCOM Reference Voltages

## Table 7. MAX9666 Register Description

| REGISTER ADDRESS | REGISTER NAME | REGISTER DESCRIPTION | BIT | | | | | | | | POWER-ON RESET VALUE | MTP FACTORY INITIALIZATION VALUE | READ AND WRITE? |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
| 0x00 | CMD_OPRN | Command operation | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | Not applicable | Write only |
| 0x01 | CMD_OPND | Command operand | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | Not applicable | Write only |
| 0x02 | VCOMMIN_M | VCOMMIN (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x00 | 0x00 | Read and write |
| 0x03 | VCOMMIN_L | VCOMMIN (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | 0x00 | Read and write |
| 0x04 | VCOMMAX_M | VCOMMAX (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x03 | 0x03 | Read and write |
| 0x05 | VCOMMAX_L | VCOMMAX (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0xFF | 0xFF | Read and write |
| 0x06 | VCOM_M | VCOM (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x02 | 0x02 | Read and write |
| 0x07 | VCOM_L | VCOM (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | 0x00 | Read and write |
| 0x08 | GMA0_M | Gamma 0 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x03 | 0x03 | Read and write |
| 0x09 | GMA0_L | Gamma 0 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x80 | 0x80 | Read and write |

***Note:*** *d0, d1, d2, d3, d4, d5, d6, d7, d8, d9 = valid data bits; x = don't care.*

## Table 7. MAX9666 Register Description (continued)

| REGISTER ADDRESS | REGISTER NAME | REGISTER DESCRIPTION | BIT | | | | | | | | POWER-ON RESET VALUE | MTP FACTORY INITIALIZATION VALUE | READ AND WRITE? |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
| 0x0A | GMA1_M | Gamma 1 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x03 | 0x03 | Read and write |
| 0x0B | GMA1_L | Gamma 1 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x40 | 0x40 | Read and write |
| 0x0C | GMA2_M | Gamma 2 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x03 | 0x03 | Read and write |
| 0x0D | GMA2_L | Gamma 2 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | 0x00 | Read and write |
| 0x0E | GMA3_M | Gamma 3 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x02 | 0x02 | Read and write |
| 0x0F | GMA3_L | Gamma 3 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x80 | 0x80 | Read and write |
| 0x10 | GMA4_M | Gamma 4 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x01 | 0x01 | Read and write |
| 0x11 | GMA4_L | Gamma 4 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x80 | 0x80 | Read and write |
| 0x12 | GMA5_M | Gamma 5 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x01 | 0x01 | Read and write |

***Note:*** *d0, d1, d2, d3, d4, d5, d6, d7, d8, d9 = valid data bits; x = don't care.*

# 6/8/10-Channel, 10-Bit, Nonvolatile Programmable Gamma and VCOM Reference Voltages

## Table 7. MAX9666 Register Description (continued)

| REGISTER ADDRESS | REGISTER NAME | REGISTER DESCRIPTION | BIT | | | | | | | | POWER-ON RESET VALUE | MTP FACTORY INITIALIZATION VALUE | READ AND WRITE? |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
| 0x13 | GMA5_L | Gamma 5 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | 0x00 | Read and write |
| 0x14 | GMA6_M | Gamma 6 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x00 | 0x00 | Read and write |
| 0x15 | GMA6_L | Gamma 6 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0xC0 | 0xC0 | Read and write |
| 0x16 | GMA7_M | Gamma 7 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x00 | 0x00 | Read and write |
| 0x17 | GMA7_L | Gamma 7 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x80 | 0x80 | Read and write |

***Note:** d0, d1, d2, d3, d4, d5, d6, d7, d8, d9 = valid data bits; x = don't care.*

## Table 8. MAX9667 Register Description

| REGISTER ADDRESS | REGISTER NAME | REGISTER DESCRIPTION | BIT | | | | | | | | POWER-ON RESET VALUE | MTP FACTORY INITIALIZATION VALUE | READ AND WRITE? |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
| 0x00 | CMD_OPRN | Command operation | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | Not applicable | Write only |
| 0x01 | CMD_OPND | Command operand | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | Not applicable | Write only |
| 0x02 | VCOMMIN_M | VCOMMIN (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x00 | 0x00 | Read and write |
| 0x03 | VCOMMIN_L | VCOMMIN (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | 0x00 | Read and write |
| 0x04 | VCOMMAX_M | VCOMMAX (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x03 | 0x03 | Read and write |
| 0x05 | VCOMMAX_L | VCOMMAX (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0xFF | 0xFF | Read and write |
| 0x06 | VCOM_M | VCOM (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x02 | 0x02 | Read and write |
| 0x07 | VCOM_L | VCOM (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | 0x00 | Read and write |
| 0x08 | GMA0_M | Gamma 0 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x03 | 0x03 | Read and write |
| 0x09 | GMA0_L | Gamma 0 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x80 | 0x80 | Read and write |
| 0x0A | GMA1_M | Gamma 1 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x03 | 0x03 | Read and write |
| 0x0B | GMA1_L | Gamma 1 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x40 | 0x40 | Read and write |

***Note:*** *d0, d1, d2, d3, d4, d5, d6, d7, d8, d9 = valid data bits; x = don't care.*

# 6/8/10-Channel, 10-Bit, Nonvolatile Programmable Gamma and VCOM Reference Voltages

## Table 8. MAX9667 Register Description (continued)

| REGISTER ADDRESS | REGISTER NAME | REGISTER DESCRIPTION | BIT | | | | | | | | POWER-ON RESET VALUE | MTP FACTORY INITIALIZATION VALUE | READ AND WRITE? |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
| 0x0C | GMA2_M | Gamma 2 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x03 | 0x03 | Read and write |
| 0x0D | GMA2_L | Gamma 2 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | 0x00 | Read and write |
| 0x0E | GMA3_M | Gamma 3 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x02 | 0x02 | Read and write |
| 0x0F | GMA3_L | Gamma 3 (least significant byte) | d7 | d6 | d5 | D4 | d3 | d2 | d1 | d0 | 0xC0 | 0xC0 | Read and write |
| 0x10 | GMA4_M | Gamma 4 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x02 | 0x02 | Read and write |
| 0x11 | GMA4_L | Gamma 4 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x80 | 0x80 | Read and write |
| 0x12 | GMA5_M | Gamma 5 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x01 | 0x01 | Read and write |
| 0x13 | GMA5_L | Gamma 5 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x80 | 0x80 | Read and write |
| 0x14 | GMA6_M | Gamma 6 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x01 | 0x01 | Read and write |
| 0x15 | GMA6_L | Gamma 6 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x40 | 0x40 | Read and write |

***Note:*** *d0, d1, d2, d3, d4, d5, d6, d7, d8, d9 = valid data bits; x = don't care.*

## Table 8. MAX9667 Register Description (continued)

| REGISTER ADDRESS | REGISTER NAME | REGISTER DESCRIPTION | BIT | | | | | | | | POWER-ON RESET VALUE | MTP FACTORY INITIALIZATION VALUE | READ AND WRITE? |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
| 0x16 | GMA7_M | Gamma 7 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x01 | 0x01 | Read and write |
| 0x17 | GMA7_L | Gamma 7 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x00 | 0x00 | Read and write |
| 0x18 | GMA8_M | Gamma 8 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x00 | 0x00 | Read and write |
| 0x19 | GMA8_L | Gamma 8 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0xC0 | 0xC0 | Read and write |
| 0x1A | GMA9_M | Gamma 9 (most significant byte) | x | x | x | x | x | x | d9 | d8 | 0x00 | 0x00 | Read and write |
| 0x1B | GMA9_L | Gamma 9 (least significant byte) | d7 | d6 | d5 | d4 | d3 | d2 | d1 | d0 | 0x80 | 0x80 | Read and write |

***Note:*** *d0, d1, d2, d3, d4, d5, d6, d7, d8, d9 = valid data bits; x = don't care.*

## Table 9. Command Set

| MACHINE CODE FOR OPERATION* | OPERATION | OPERANDS | DESCRIPTION |
|---|---|---|---|
| 0x00 | NOP | None | No operation. |
| 0x01 | MOV | Source, destination | Move data in source location to destination location. Source location is bits 4 through 7, and destination location is bits 0 through 3. Source locations and destination locations must be of the same type. For example, commands that move data from the VCOM registers to the gamma registers and vice-versa are not valid, and the I²C interface issues a NACK. |

**Write to I²C Register 0x00.*

## Table 10. Example Commands for MOV Operation

| $I^2C$ REGISTER ADDRESS | 0x00 | 0x01 |
|---|---|---|
| Operation: Move Gamma register value to Gamma MTP memory | 0x01 | 0x45 |
| Operation: Move VCOM MTP memory to VCOM register | 0x01 | 0x32 |
| Operation: Move all register values to MTP memory | 0x01 | 0x67 |

For a move (MOV) command, 0x01 should be written into $I^2C$ register 0x00, and the source and destination written in $I^2C$ register 0x01. See Table 10 for examples. The upper 4 bits (7 to 4) designate the source, and the lower 4 bits (3 to 0) destination, per Table 11.

It takes 30ms (typ) and 32ms (max) to move one $I^2C$ register to MTP memory. Thus, it needs 400ms (typ) and 450ms (max) to program all $I^2C$ registers to MTP memory for VCOM window, VCOM, and gamma.

The command operand and operation registers must be written to consecutively, otherwise the command does not execute.

### *Single-Wire Interface*

The MAX9665/MAX9666/MAX9667 have a single-wire interface that is compatible with the MAX1512 interface.

## Table 11. Source and Destination Locations for MOV Command

| LOCATION CODE | DESCRIPTION |
|---|---|
| 0b0000 | VCOM Window Registers |
| 0b0001 | VCOM Window MTP Memory |
| 0b0010 | VCOM Register |
| 0b0011 | VCOM MTP Memory |
| 0b0100 | Gamma Registers |
| 0b0101 | Gamma MTP Memory |
| 0b0110 | All Registers |
| 0b0111 | All MTP Memory |

### *VCOM Adjustment (CTL)*

Pulse CTL low for more than 200µs to increment the DAC setting, which lowers the VCOM level by 1 least-significant bit (LSB) (Figure 10). Similarly, pulse CTL high for more than 200µs, which raises the VCOM level by 1 LSB.

To avoid unintentional VCOM adjustment, the parts are guaranteed to reject CTL pulses shorter than 20µs. In addition, to avoid the possibility of a single false pulse caused by power-up sequencing between DVDD and CTL, the very first pulse is ignored.

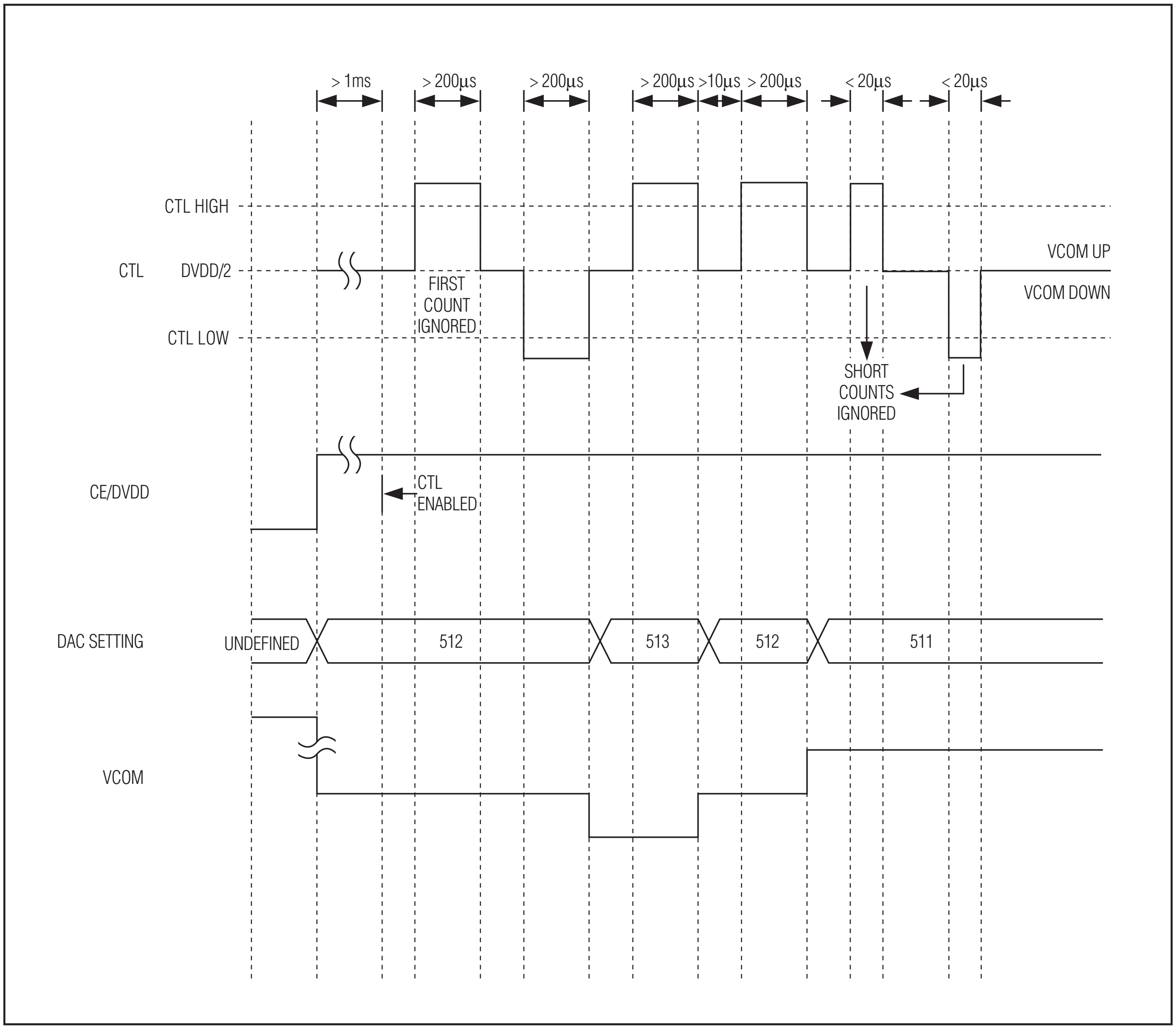



*Figure 10. VCOM Adjustment*

### MTP Programming (CTL)

To program the MTP memory, apply the MTP programming waveform through the CTL interface (Figure 11). Unlike the MAX1512, the control interface only delivers DAC adjustment commands, not programming power. AVDD must be valid for MTP programming to occur. If AVDD is not valid for MTP programming, the single-wire interface is in shutdown.

To apply the MTP programming waveform, carefully ramp CTL from midscale (DVDD/2) to the programming voltage, $V_{P-P}$, in 7.5ms as shown in Figure 11. If the ramp is generated digitally, use at least 45 steps to achieve the required 320mV ramp resolution. During the ramp time, VCOM adjustment is disabled and the MTP cell is biased in preparation for programming. After reaching $V_{P-P}$, hold CTL at $V_{P-P}$ for 1ms. During the MTP program time, the MTP memory stores the DAC setting. Next, drive CTL to ground in less than 1ms and hold for at least 200µs. Finally, drive CTL to DVDD/2 to complete the write cycle. The MTP memory is factory set to half scale. Follow the MTP programming specification in Table 12 to guarantee reliable MTP memory programming. Violating the specifications can damage the MTP memory or affect data retention.

Table 12 shows the timing and voltage parameters for MTP programming. This table is used for programming through the single-wire interface.

### Single-Wire Interface Enable/Disable (CE)

The single-wire interface can be disabled to reduce the DVDD supply current. Connect CE to GND to reduce the typical supply current from 450µA to 320µA. Connect CE to DVDD to enable the single-wire interface.

The programming circuit in Figure 12 drives CE high to enable the CTL input when it is connected. When the programming circuit is not connected, CE is pulled low through resistor $R_{CE}$, which disables the CTL input. The CTL input is relatively immune to noise and brief voltage transients. It can be safely left continuously enabled if higher supply current is acceptable.

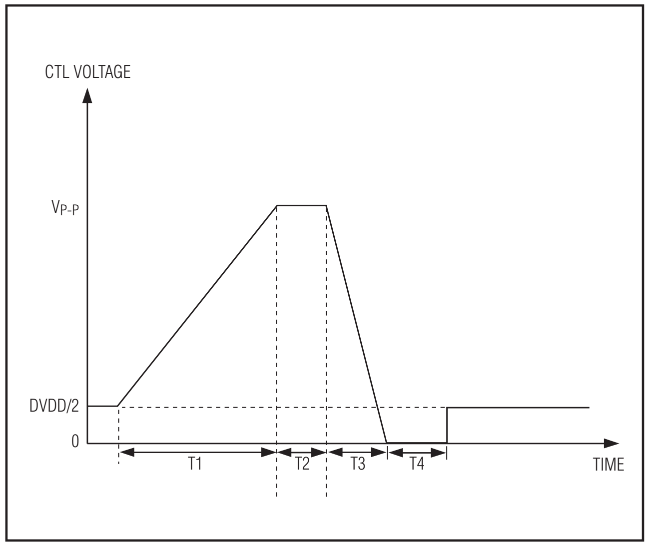



*Figure 11. MTP Memory Programming*

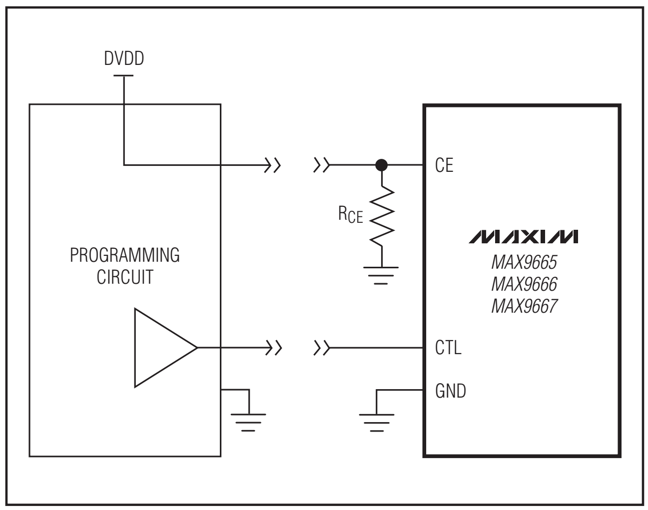



*Figure 12. Optional Circuit to Drive CE*

## Table 12. MTP Memory Programming Specifications

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| CTL Programming Voltage | $V_{P-P}$ | 15.25 | 15.5 | 15.75 | V |
| CTL Programming Ramp | T1 | 7.0 | 7.5 | 8.0 | ms |
| MTP Memory Program Time | T2 | 0.9 | 1.0 | 1.1 | ms |
| $V_{P-P}$ Fall Time | T3 | 10 | — | 1000 | µs |
| Done Hold Time | T4 | 200 | — | — | µs |

## Applications Information

### *Power-Up and Power-Down*

Figure 13 below shows the power-up sequence. The digital supply must be powered up first. The analog supply should not be powered up for at least 350µs (min) after the digital supply has been powered up. During this time, the MTP register values are loaded into the $I^2C$ registers and the default $I^2C$ register values are overwritten. Once AVDD is above approximately 8V, the output buffers have enough headroom and power up proportionally with the AVDD.

For power-down, AVDD must be lowered first to 0V, and then DVDD can safely be powered down.

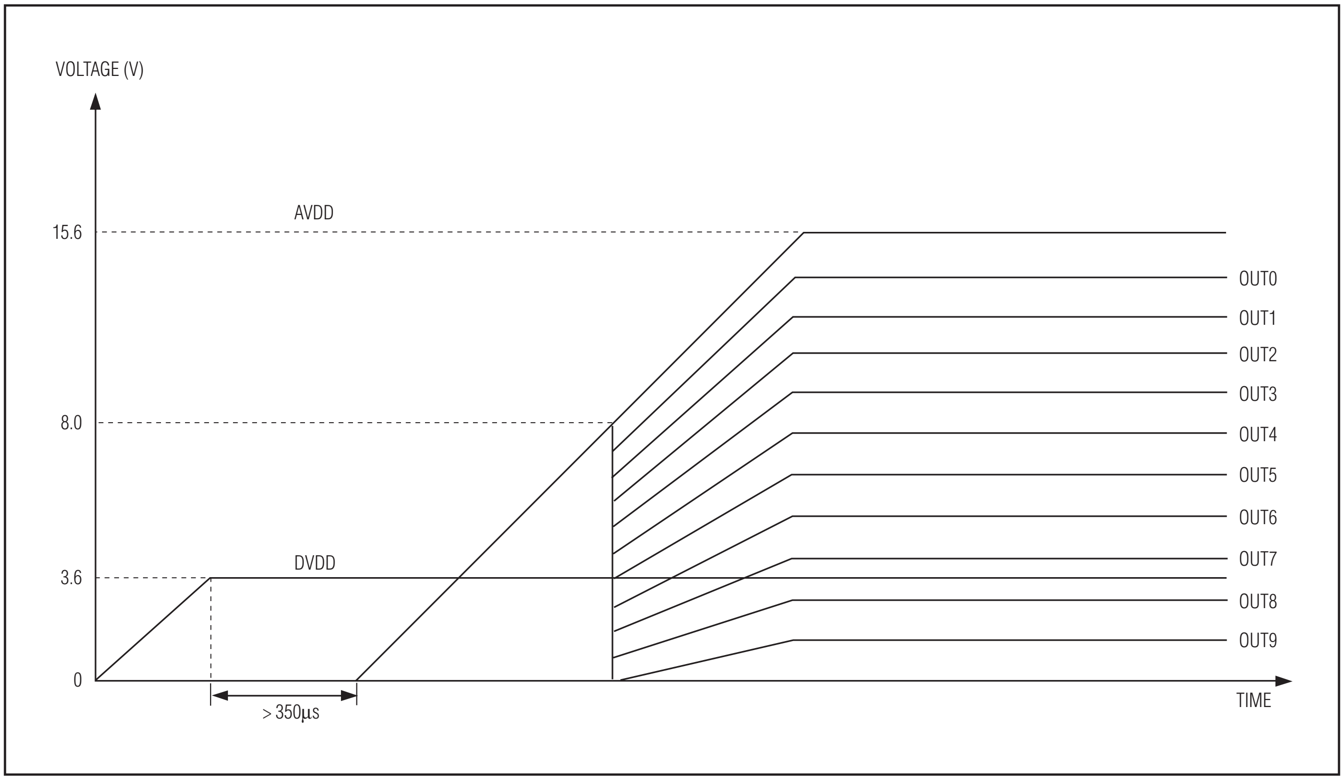



*Figure 13. Power-Up Sequence*

### Electrostatic Discharge (CTL, CE)

Often, CTL and CE are exposed at the panel connector and are therefore subject to electrostatic discharge (ESD). Resistor-capacitor (RC) filters can be employed at these inputs to improve their ESD performance (Figure 14).

If the CE panel connector is to be left unconnected after programming, be sure to include a resistor to ground ($R_{CE}$) to ensure a valid logic-low on CE. The time constant for a CE filter is not critical, but the driving resistor must have a much lower resistance than $R_{CE}$ to properly drive CE. If a filter is used at the CTL panel connector, its RC time-constant should be short enough to avoid interfering with CTL pulses or MTP memory programming timing. A time constant less than 200µs does not interfere with MTP memory programming. To avoid interfering with CTL pulses, make the time constant small compared to the CTL pulse width needed.

### Leakage Current (CTL)

The CTL pin is internally biased to DVDD/2, but it is sensitive to leakage currents above 0.1µA. When CTL is not driven, avoid leakage currents around the CTL pin. Otherwise, reinforce the DVDD/2 set point with an external resistive voltage-divider.

### Power Supplies and Bypass Capacitors

The MAX9665/MAX9666/MAX9667 operate from a single 9V to 20V analog supply and a 2.5V to 3.6V digital supply. Bypass AVDD to GND with 0.1µF and 10µF capacitors in parallel. Use an extensive ground plane to ensure optimum performance. Bypass DVDD to GND with a 0.1µF capacitor. Refer to the MAX9665/MAX9666/MAX9667 evaluation kit for a proven PCB layout.

### Layout and Grounding

The exposed pad on the TQFN package is electrically connected to GND. Solder the exposed pad to a ground plane to provide a low thermal resistance to ground for heat dissipation. Do not route traces under these packages.

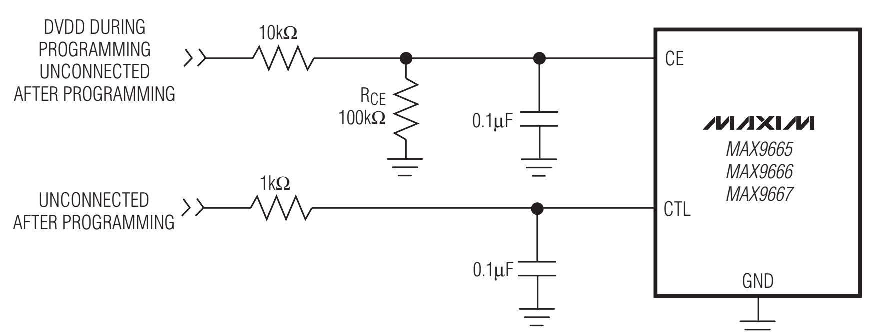
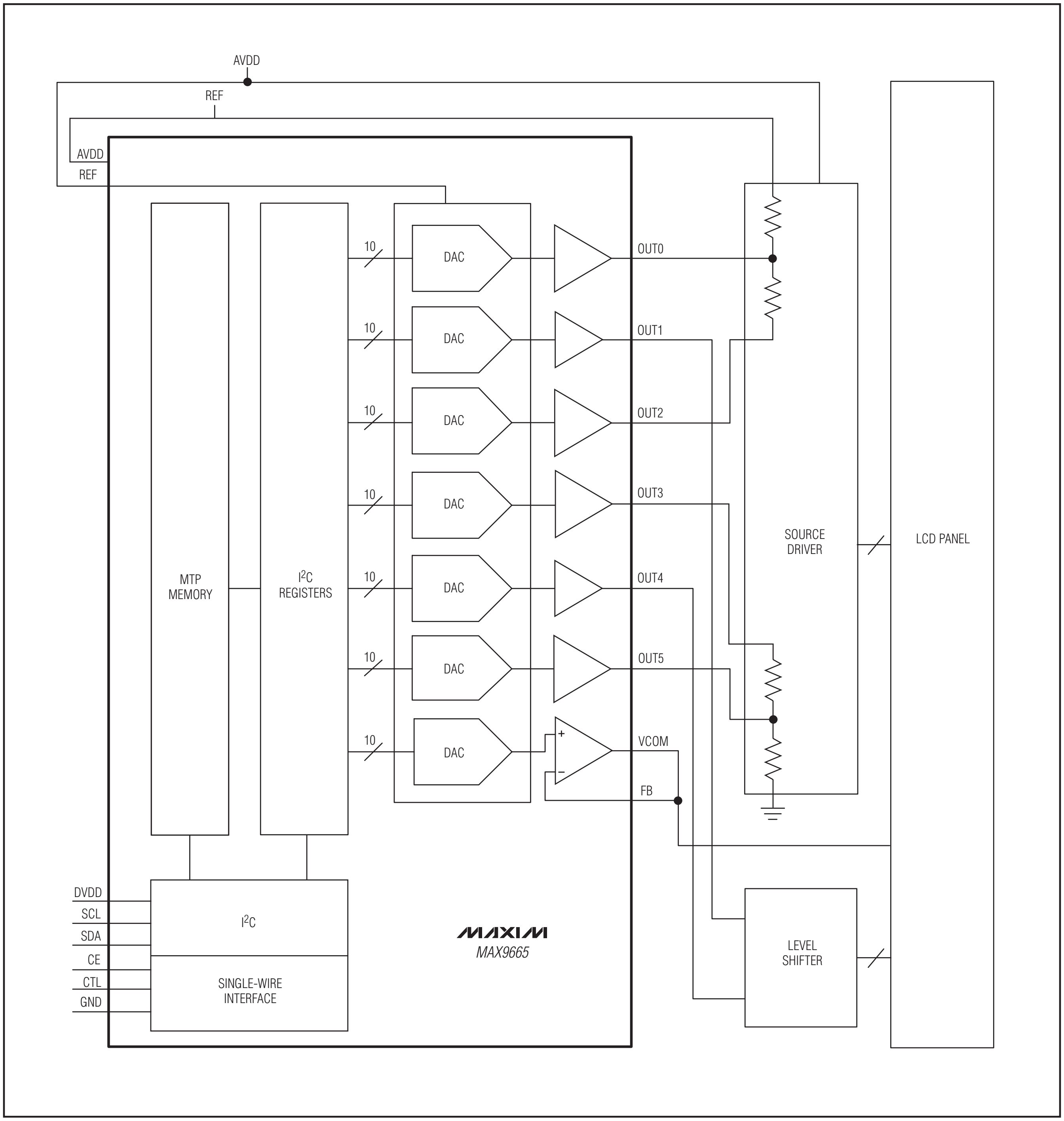
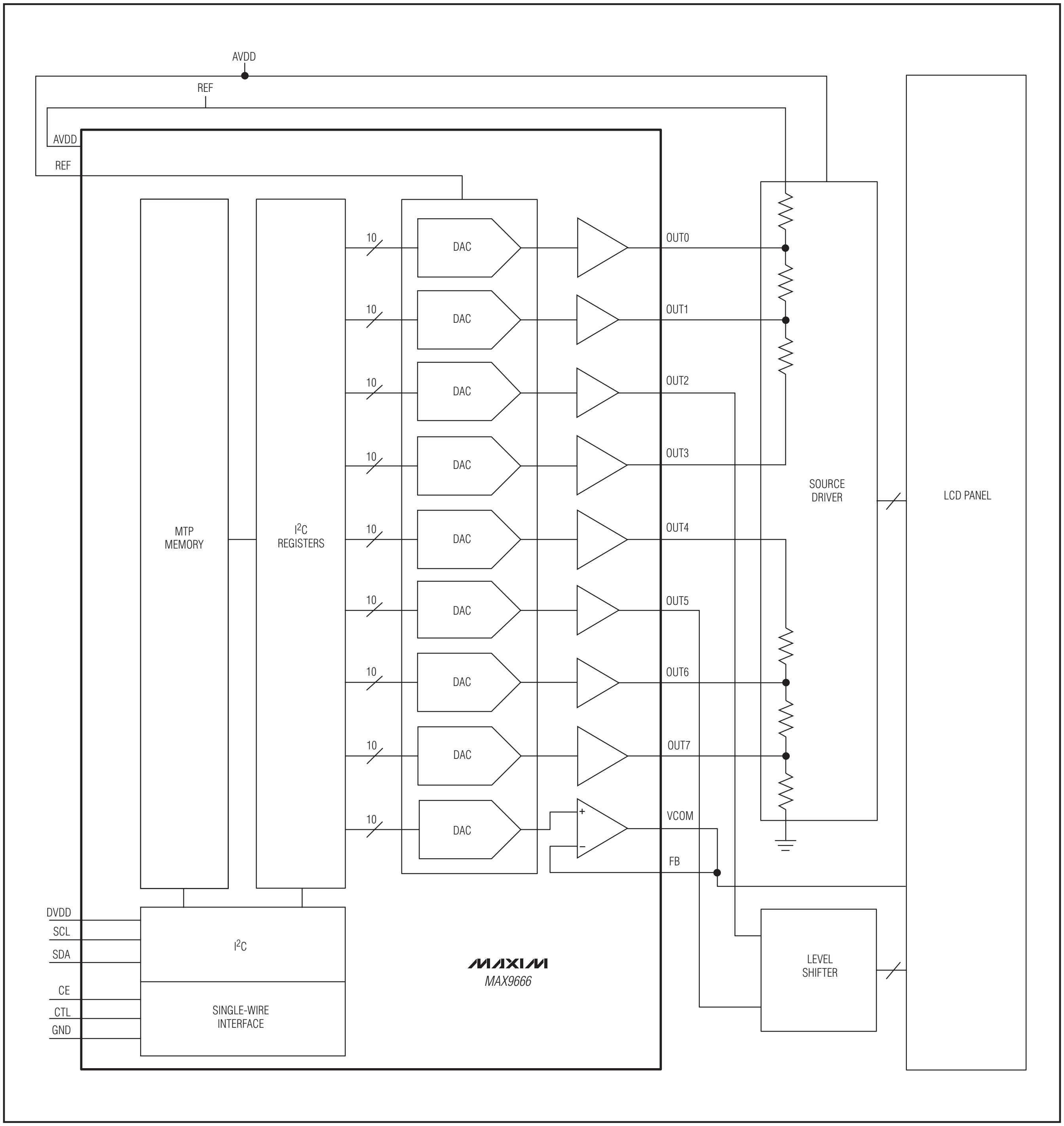



*Figure 14. Improved EOS/Surge Performance*

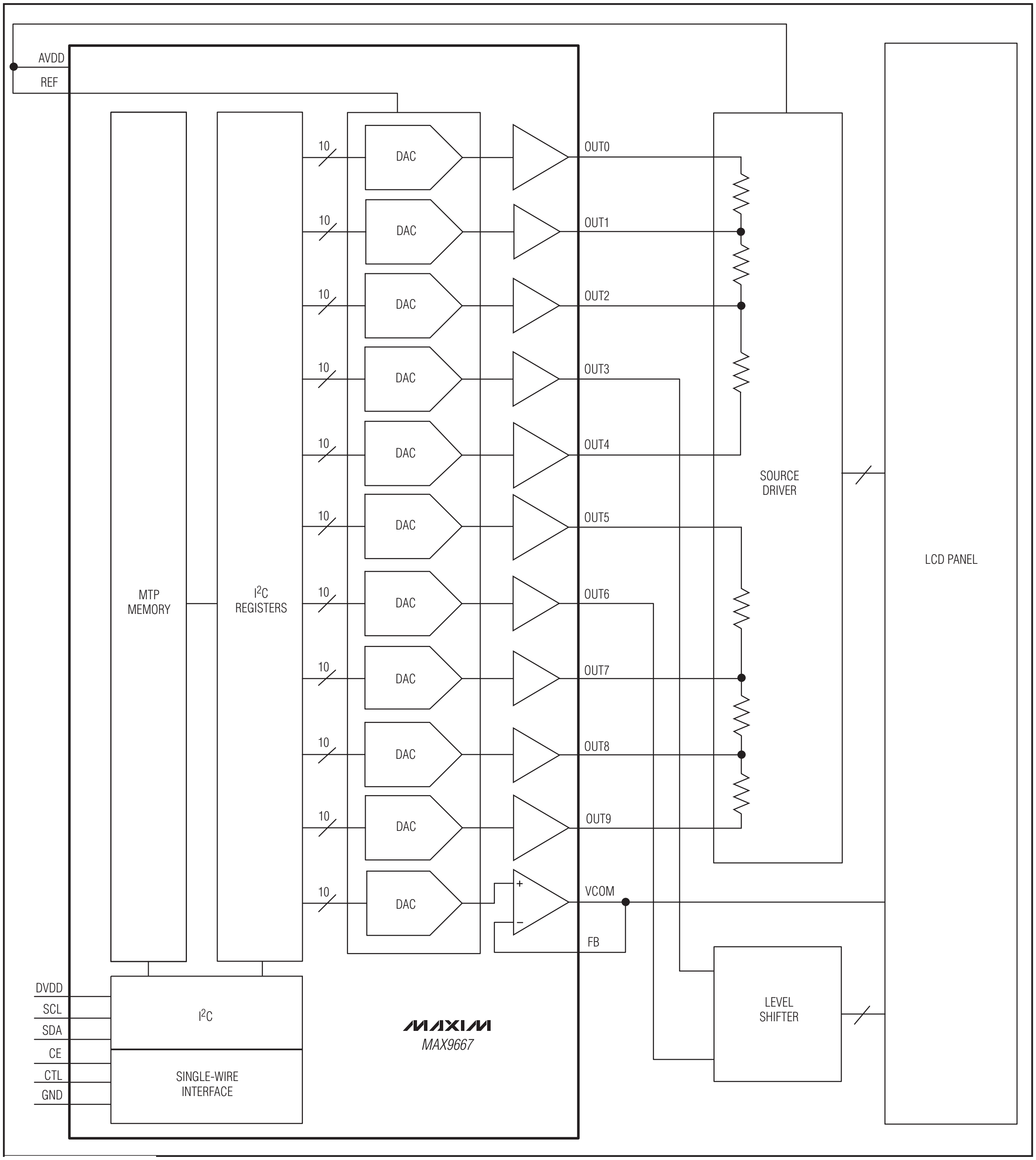
## Typical Operating Circuits



## Typical Operating Circuits (continued)

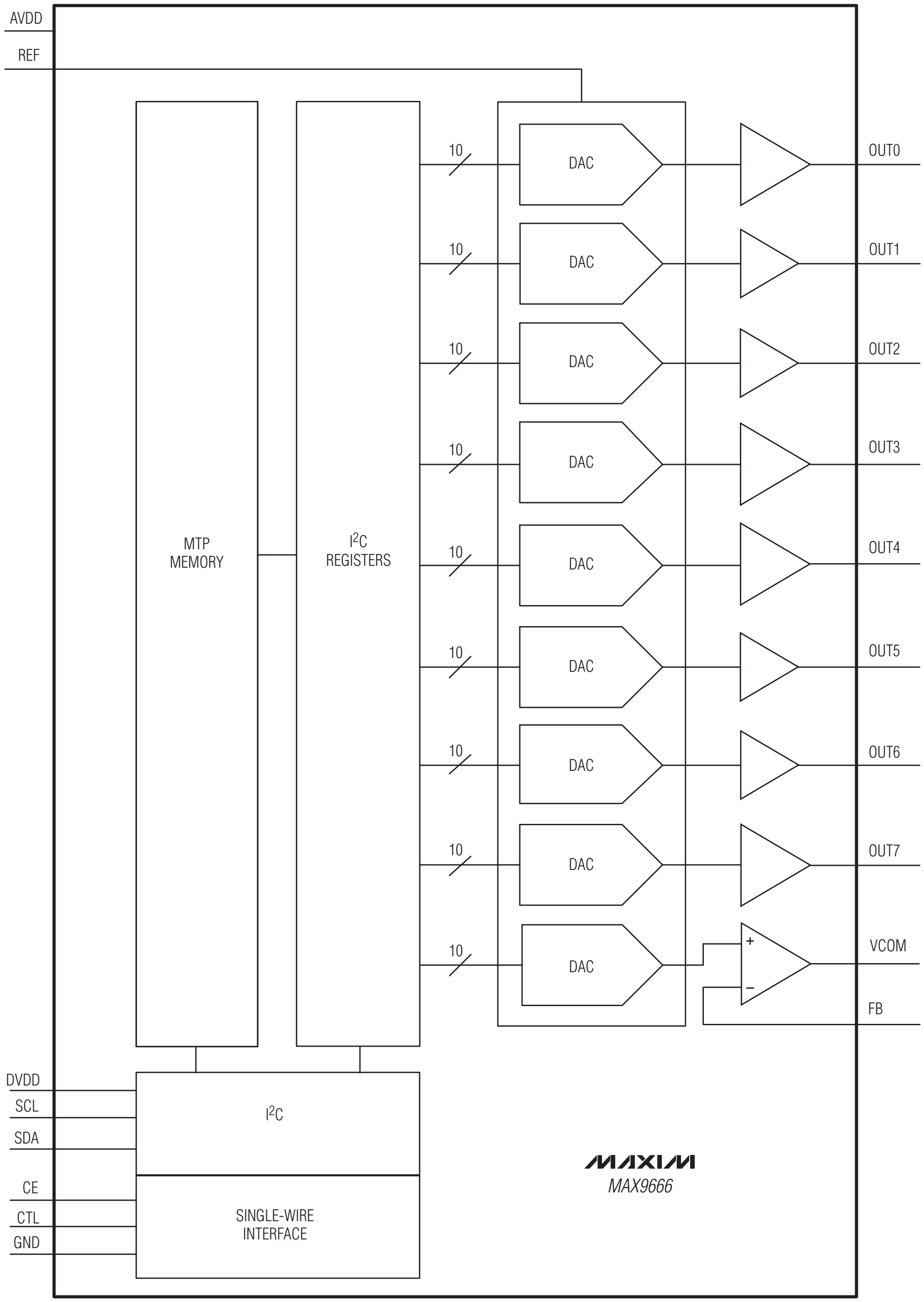


## Typical Operating Circuits (continued)

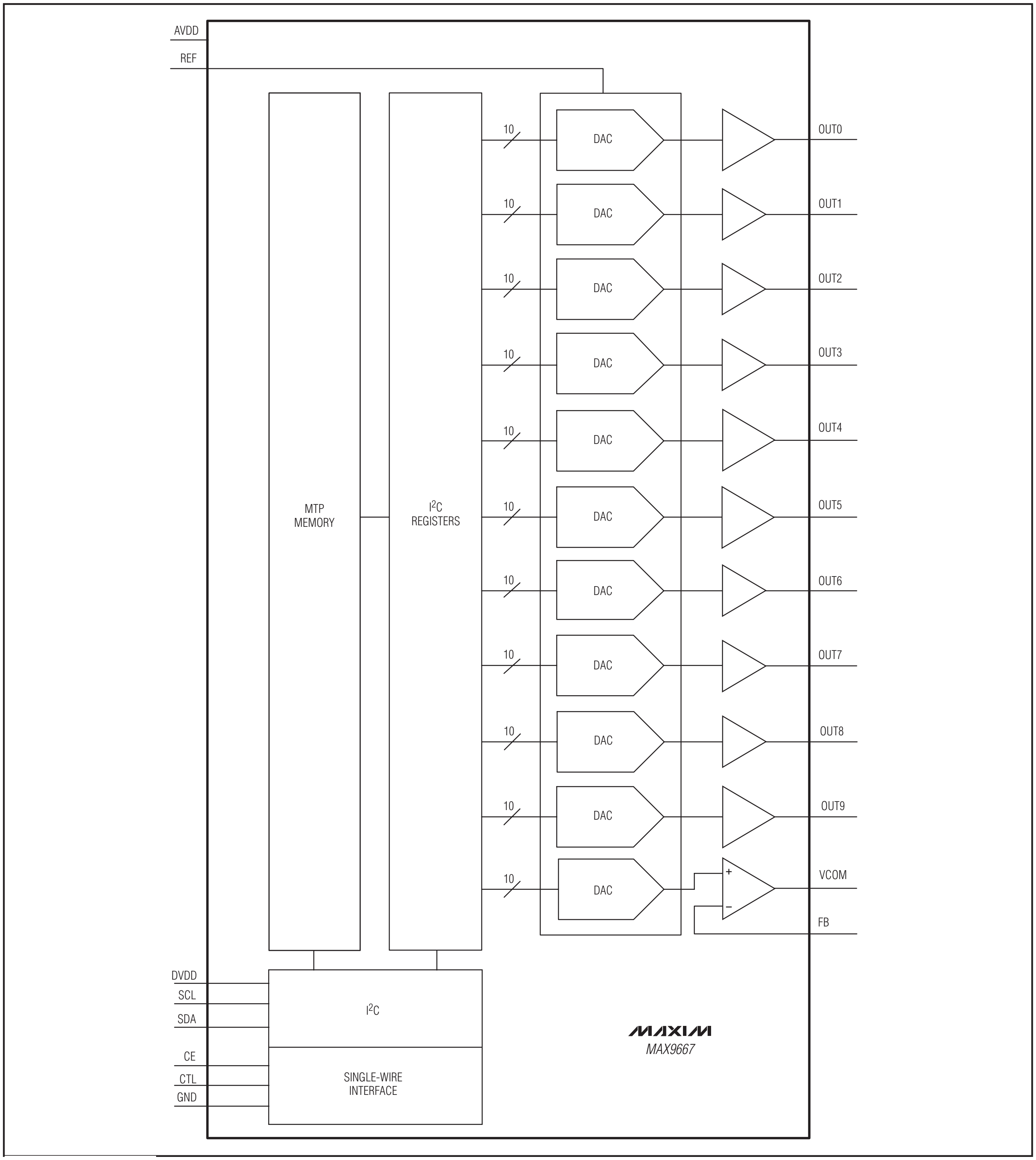


# 6/8/10-Channel, 10-Bit, Nonvolatile Programmable Gamma and VCOM Reference Voltages

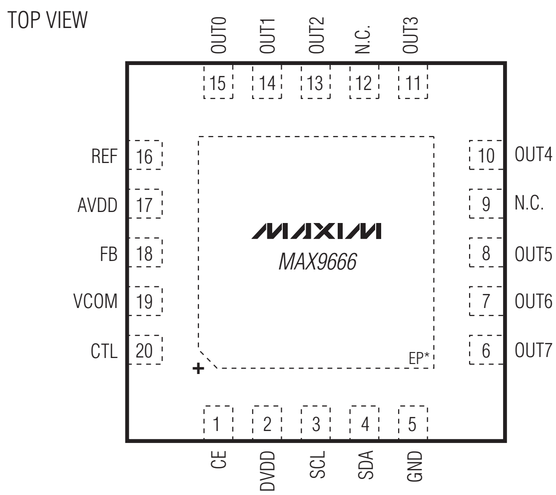
## Functional Diagrams (continued)



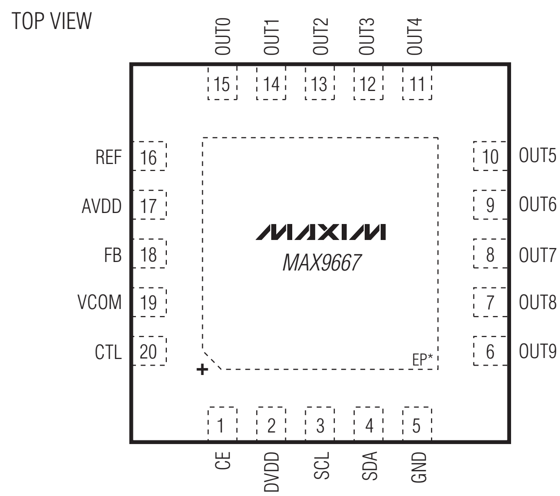
## Functional Diagrams (continued)



## Pin Configurations (continued)




**THIN QFN**
**5mm x 5mm**



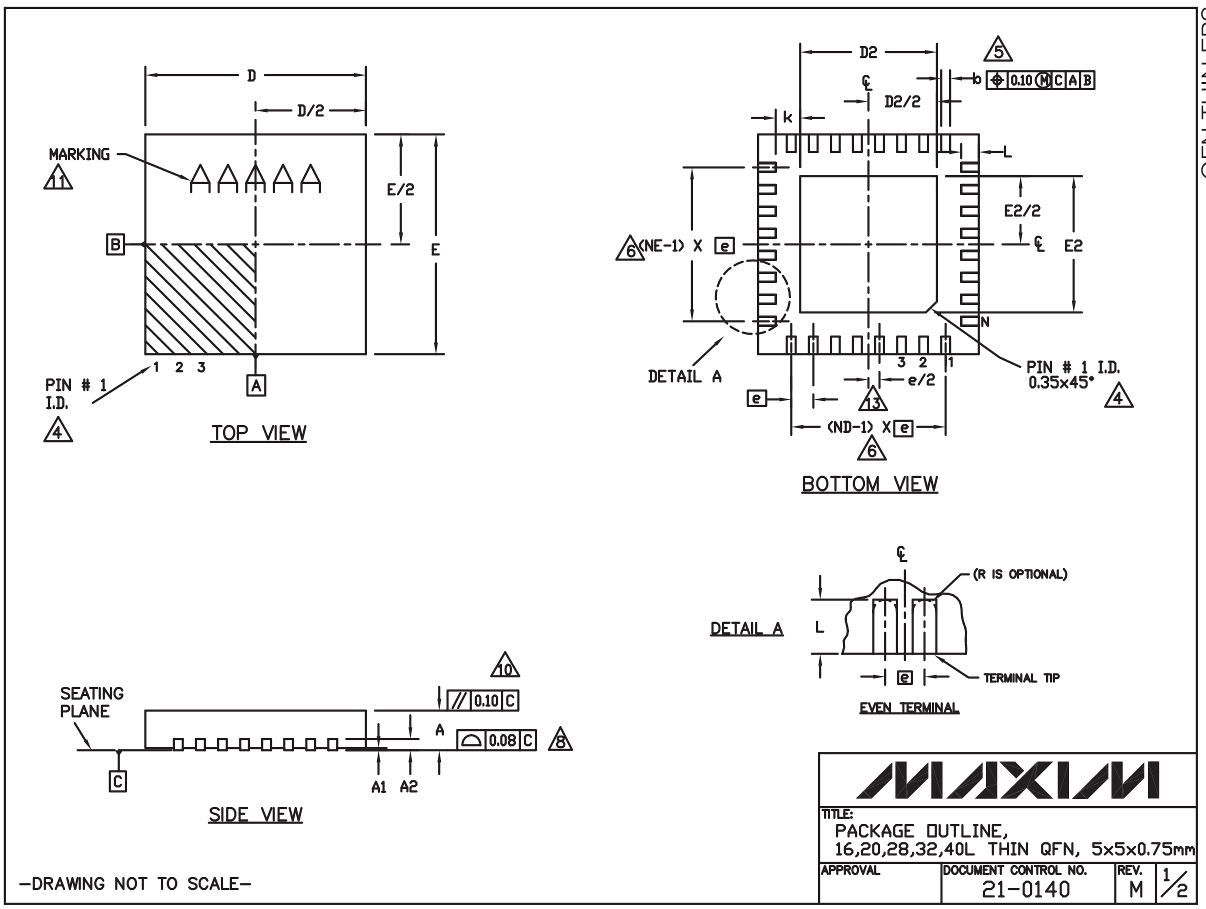

**THIN QFN**
**5mm x 5mm**

*EP = EXPOSED PAD. CONNECT TO DIGITAL GROUND PLANE.

## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 20 TQFN-EP | T2055+3 | **21-0140** | **90-0121** |



## Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

**COMMON DIMENSIONS**

| PKG. | 16L 5x5 | | | 20L 5x5 | | | 28L 5x5 | | | 32L 5x5 | | | 40L 5x5 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SYMBOL | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 |
| A2 | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 | 0.15 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 |
| E | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 |
| e | 0.80 BSC. | | | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | | 0.40 BSC. | | |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - |
| L | 0.30 | 0.40 | 0.50 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 | 0.30 | 0.40 | 0.50 |
| N | 16 | | | 20 | | | 28 | | | 32 | | | 40 | | |
| ND | 4 | | | 5 | | | 7 | | | 8 | | | 10 | | |
| NE | 4 | | | 5 | | | 7 | | | 8 | | | 10 | | |
| JEDEC | WHHB | | | WHHC | | | WHHD-1 | | | WHHD-2 | | | ----- | | |

**EXPOSED PAD VARIATIONS**

| PKG. CODES | D2 | | | E2 | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T1655-2 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T1655-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T1655-4 | 2.19 | 2.29 | 2.39 | 2.19 | 2.29 | 2.39 |
| T165N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-5 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2055MN-5 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-3 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-4 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-5 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-6 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-7 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-8 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855N-1 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T3255-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255M-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255-5 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T4055-1 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055-2 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055N-1 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055MN-1 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.75mm

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0140 | M | 2/2 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 10/09 | Initial release | — |
| 1 | 11/09 | Added soldering temperature (reflow) and made minor updates | 1, 2, 10, 38 |
| 2 | 1/10 | Updated MTP write qualification and MOV command description | 1, 10, 12, 28, 30 |
| 3 | 3/10 | Corrected various errors and added soldering temperature | 1, 2, 3, 5–9, 15–20, 22, 25, 30, 31, 33, 38 |
| 4 | 7/10 | Corrected terminology in TOCs 2 and 3 and typos | 6, 16, 17 |