DSC2010

discera

Low-Jitter Configurable CMOS Oscillator

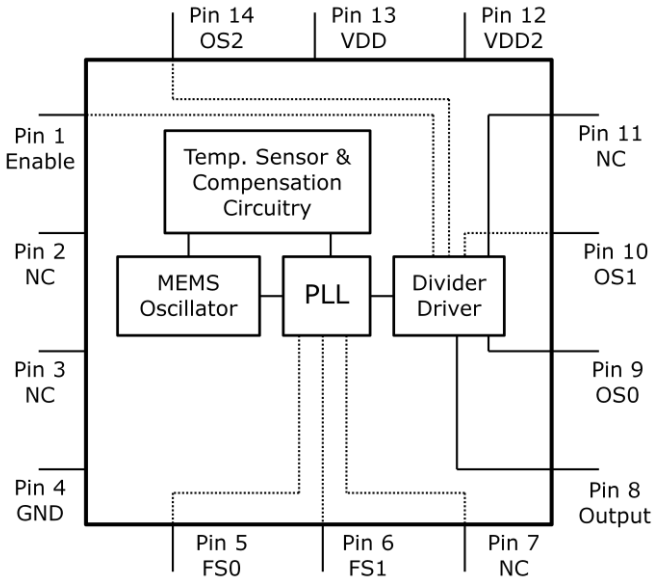
www.discera.com

General Description

The DSC2010 series of high performance CMOS oscillators utilize a proven silicon MEMS technology to provide excellent jitter and stability while incorporating additional device functionality. The DSC2010 allows the user to easily modify the frequency and drive strength of the oscillator using pins. The DSC2010 has provision for up to four user-defined pre-programmed, pin-selectable output frequencies, and eight pin-selectable output drive levels to help reduce EMI.

DSC2010 is packaged in a 14-pin 3.2x2.5 mm QFN package and available in temperature grades from Ext. Commercial to Automotive.

Block Diagram



Features

- **Low RMS Phase Jitter: <1 ps (typ)**
- **High Stability: ±10, ±25, ±50 ppm**
- **Wide Temperature Range**
  - Automotive: -55° to 125° C
  - Ext. Industrial: -40° to 105° C
  - Industrial: -40° to 85° C
  - Ext. commercial: -20° to 70° C
- **High Supply Noise Rejection: -50 dBc**
- **Pin-Selectable Configurations**
  - 3-bit Output Drive Strength
  - 2-bit Output Frequency Combinations
- **Short Lead Times: 2 Weeks**
- **Wide Freq. Range:**
  - CMOS Output: 2.3 to 170 MHz
- **Miniature Footprint of 3.2x2.5mm**
- **Excellent Shock & Vibration Immunity**
  - Qualified to MIL-STD-883
- **High Reliability**
  - 20x better MTF than quartz oscillators
- **Supply Range of 2.25 to 3.6 V**
- **Lead Free & RoHS Compliant**

Applications

- **Consumer Electronics**
- **Storage Area Networks**
  - SATA, SAS, Fibre Channel
- **Passive Optical Networks**
  - EPON, 10G-EPON, GPON, 10G-PON
- **Ethernet**
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- **HD/SD/SDI Video & Surveillance**
- **PCI Express**

Pin Description

Pin No.	Pin Name	Pin Type	Description
1	Enable	I	Enables outputs when high and disables when low
2	NC	NA	Leave unconnected or grounded
3	NC	NA	Leave unconnected or grounded
4	GND	Power	Ground
5	FS0	I	Least significant bit for frequency selection
6	FS1	I	Most significant bit for frequency selection
7	NC	NA	Leave unconnected or grounded
8	Output	O	CMOS output
9	OS0	I	Least significant bit for output drive strength selection
10	OS1	I	Middle bit for output drive strength selection
11	NC	NA	Leave unconnected or grounded
12	VDD2	Power	Power Supply
13	VDD	Power	Power Supply
14	OS2	I	Most significant bit for output drive strength selection

Operational Description

The DSC2010 is a CMOS oscillator consisting of a MEMS resonator and a support PLL IC. The CMOS output is generated through independent 8-bit programmable dividers from the output of the internal PLL.

The actual frequency output by the DSC2010 is controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for up to four different frequencies. Two control pins (FS0 – FS1) select the output frequency. Discera supports customer defined versions of the DSC2010. Standard frequency options are described in the following sections.

When Enable (pin 1) is floated or connected to VDD, the DSC2010 is in operational mode. Driving Enable to ground will disable the output driver (hi-impedance mode).

The DSC2010 has programmable output drive strength. Using three control pins (OS0-OS2) the drive strength can be adjusted to match circuit board impedances to reduce power supply noise, overshoot/undershoot and EMI. Table 1 displays typical rise / fall times for the output with a 15pf load capacitance as a function of these control pins at VDD=3.3V and room temperature.

Table 1. Rise/Fall times for drive strengths

	Output Drive Strength Bits [OS2, OS1, OS0] - Default [**111**]							
	000	001	010	011	100	101	110	**111**
tr (ns)	2.1	1.7	1.6	1.4	1.3	1.3	1.2	**1.1**
tf (ns)	2.5	2.4	2.4	2.2	1.8	1.6	1.4	**1.4**

Output Clock Frequencies

Table 2 lists the standard frequency configurations and the associated ordering information to be used in conjunction with the ordering code. Customer defined combinations are available.

Table 2. Pre-programmed pin-selectable output frequency combinations

Ordering Info	Freq (MHz)	Freq Select Bits [FS1, FS0] – **Default is [11]**			
		00	01	10	**11**
A0001	f_{OUT}	27	24	148.5	**74.25**
A0002	f_{OUT}	155.52	106.25	156.25	**125**
A0003	f_{OUT}	25	75	125	**150**
A0004	f_{OUT}	72	74.25	36	**108**
A0005	f_{OUT}	27	50	0*	**0***
A0006	f_{OUT}	16	13.56	0*	**0***
A0007	f_{OUT}	96	55	0*	**0***
A0008	f_{OUT}	25	50	0*	**0***
A0009	f_{OUT}	55.296	27.648	0*	**0***
A00010	f_{OUT}	27.648	55.296	0*	**0***
A000X	f_{OUT}	Contact factory for additional configurations.			

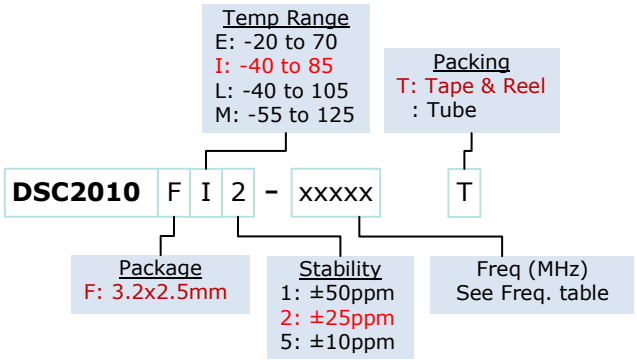
Frequency select bit are weakly tied high so if left unconnected the default setting will be [11] and the device will output the associated frequency highlighted in **Bold**.
0* – denotes invalid selection, output frequency is not specified.

Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V_{DD}+0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD HBM MM CDM	-	 4000 400 1500	V	

Note: 1000+ years of data retention on internal memory

Ordering Code

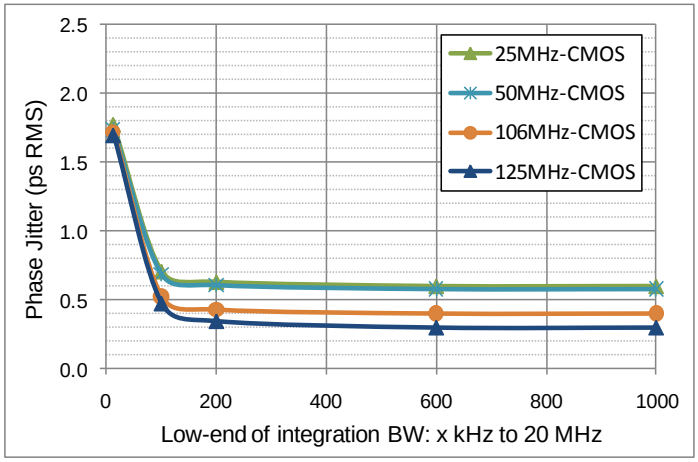


Specifications (Unless specified otherwise: T=25° C, max CMOS drive strength)

Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage[1]	V_{DD}		2.25		3.6	V
Supply Current	I_{DD}	EN pin low – output is disabled		21	23	mA
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±10 ±25 ±50	ppm
Aging	Δf	1 year @25°C			±5	ppm
Startup Time[2]	t_{SU}	T=25°C			5	ms
Input Logic Levels Input logic high Input logic low	 V_{IH} V_{IL}		 0.75xV_{DD} -		 - 0.25xV_{DD}	V
Output Disable Time[3]	t_{DA}				5	ns
Output Enable Time	t_{EN}				20	ns
Pull-Up Resistor[4]		Pull-up exists on all digital IO		40		kΩ
CMOS Output						
Supply Current[4]	I_{DD}	EN pin high – output is enabled C_L=15pF, F_O=125 MHz		31	35	mA
Output Logic Levels Output logic high Output logic low	 V_{OH} V_{OL}	I=±6mA	 0.9xV_{DD} -		 - 0.1xV_{DD}	V
Output Transition time[3] Rise Time Fall Time	 t_R t_F	20% to 80% C_L=15pf		 1.1 1.3	 2 2	ns
Frequency	f_0	Commercial/Industrial temp range Automotive temp range	2.3		170 100	MHz
Output Duty Cycle	SYM		45		55	%
Period Jitter	J_{PER}	F_O=125 MHz		3		ps_{RMS}
Integrated Phase Noise	J_{CC}	200kHz to 20MHz @ 125MHz 100kHz to 20MHz @ 125MHz 12kHz to 20MHz @ 125MHz		0.3 0.38 1.7	 2	ps_{RMS}

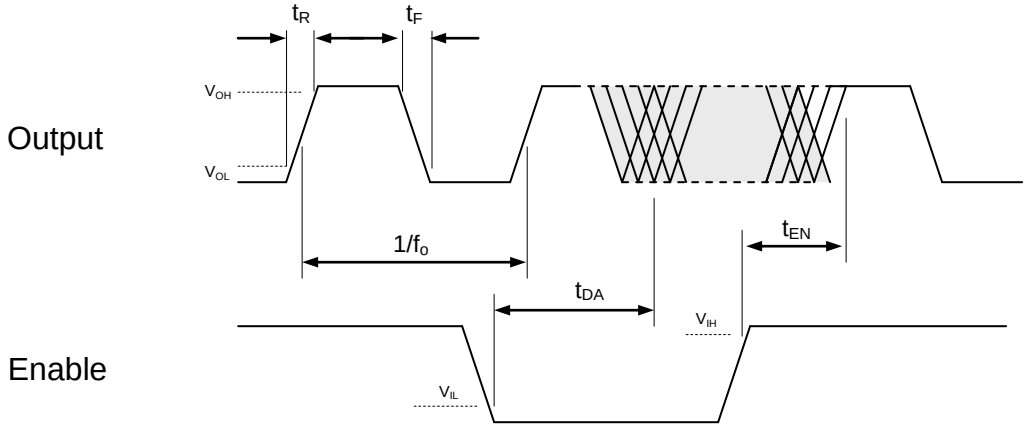
Notes:
1. Pin 4 V_{DD} should be filtered with 0.01uf capacitor.
2. t_{su} is time to 100PPM stable output frequency after V_{DD} is applied and outputs are enabled.
3. Output Waveform and Test Circuit figures below define the parameters.
4. Output is enabled if Enable pad is floated or not connected.

Nominal Performance Parameters (Unless specified otherwise: T=25° C, V_{DD}=3.3 V)

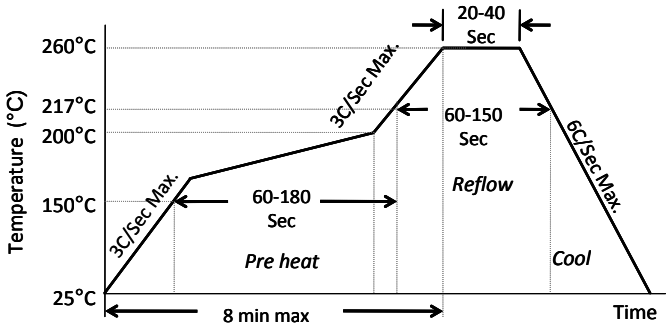


CMOS Phase jitter (integrated phase noise)

Output Waveform: CMOS



Solder Reflow Profile



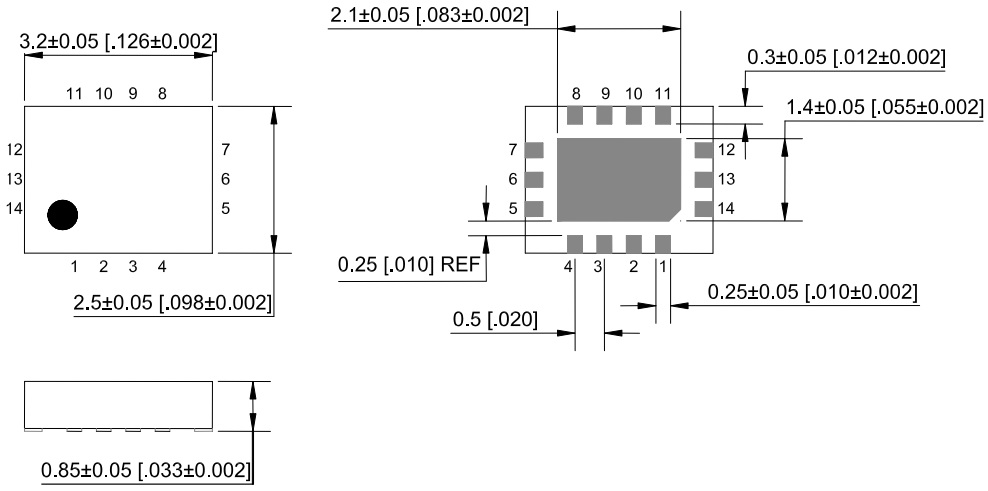
MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

Package Dimensions

3.2 x 2.5 mm 14 Lead Plastic Package

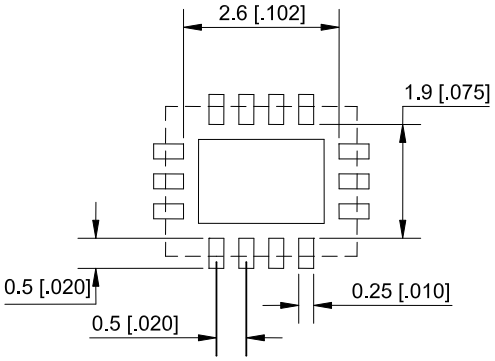
External Dimensions

units: mm[inch]



Recommended Solder Pad Layout

units: mm[inch]



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